

CS 250 Spring 2017 Homework 01 SOLUTION

Due 11:58pm Wednesday, January 18, 2017

Submit your typewritten file in PDF format to Blackboard.

The policy for all homework assignments this semester is as follows. Please sign, which you may do by typing in your name.

In the following I have not represented the work of another person as my own nor have I knowingly or actively assist another person in violating this standard.

(Signed) _____

1. How many distinct one-input Boolean functions are there?

Answer: With one Boolean input there are two distinct input values: 0 and 1. For each input value there are two choices for defining the output: 0 and 1. Therefore, the number of distinct Boolean function truth tables corresponding to the input possibilities 0 and 1 is $2*2 = 2^2 = 4$. The general formula for the number of distinct k-input Boolean functions is 2^k .

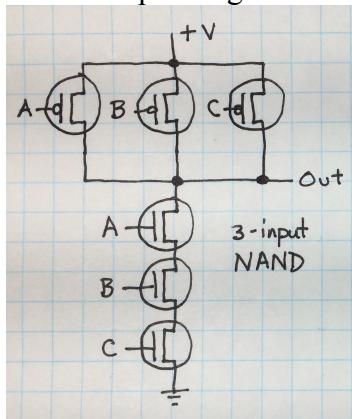
2. What is the truth table for the three-input NAND function? Extend the two-input NAND circuit in the text Figure 2.5 to accept three inputs and draw a schematic.

[Diagrams are a way of life for describing computer hardware designs and computer software logic flows. For CS 250 homework answers that require a schematic, I suggest that you hand-draw your answer neatly, then photograph or scan it, and import that image into the solution document you will print and turn in.]

Answer: The truth table for 3-input NAND is:

A	B	C	$(ABC)'$	Conduction path to Out is from
0	0	0	1	+V thru A, B, and C
0	0	1	1	+V thru A and B
0	1	0	1	+V thru A and C
0	1	1	1	+V through A
1	0	0	1	+V through B and C
1	0	1	1	+V through B
1	1	0	1	+V through C
1	1	1	0	Ground thru C,B, A

and corresponding CMOS transistor circuit is:

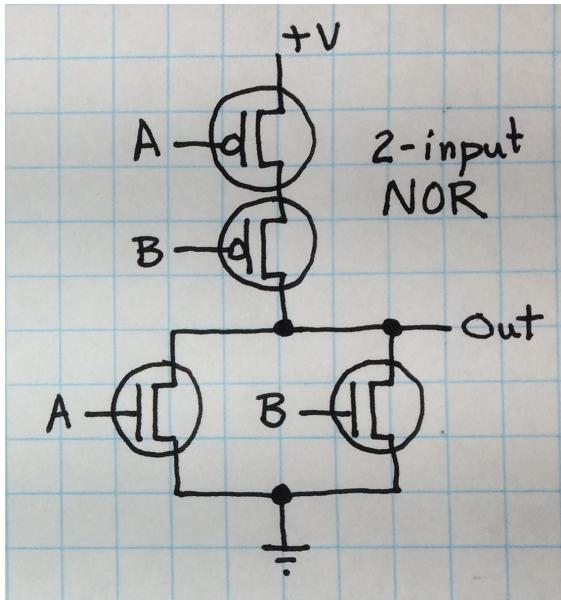


3. Using exactly 4 CMOS transistors, design and then draw a schematic for a NOR circuit. Comment on the relationship you see between the NAND circuit presented in class and our textbook and the NOR circuit that you develop.

Answer: The truth table for NOR is

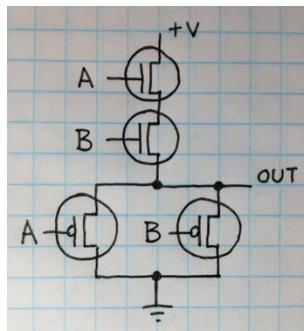
Row number	A	B	$(A+B)'$
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	0

The only time a 2-input NOR gate should output a high voltage value (a logical 1) is when *both* inputs are 0 (row number 0 in the table). All other input cases (rows 1, 2, and 3) should output a low voltage (a logical 0). For our voltage divider gate design paradigm this means that when the gate output should be high voltage (logic 1) then the path between the gate output and the supply voltage should pass through two MOSFETs in series, one for each input, A and B, and the two MOSFETs should each turn ON with a low (zero) input. For the path between the gate output and ground (zero) we want either A or B to trigger a conduction path, so we want parallel MOSFETs of the type that turn ON with a 1 input. Thus, the circuit is



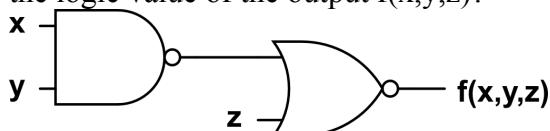
Compared to the NAND circuit in the text, the NOR circuit uses a MOSFETs in series circuit for the R_1 portion of our lecture slides voltage divider circuit, rather than a parallel MOSFET circuit. The NOR also uses a parallel MOSFETs circuit for the R_2 portion of the voltage divider, rather than the series MOSFET circuit of the NAND gate. Finally, the type of MOSFETs used for the R_1 and R_2 portions of the voltage divider are the opposite in the NOR circuit of their placement in the NAND circuit. There is a circuit “duality” between NAND and NOR: to convert one gate circuit into the other, simply exchange series and parallel structures and exchange high-active (On) and low-active (Off) MOSFET types. This circuit duality holds true for 3-input NAND and NOR as well.

4. Name the Boolean function that this circuit implements.



Answer: AND

5. Let the input logic values to the following circuit be $x=\text{Don't Care}$, $y=0$, and $z=1$. What is the logic value of the output $f(x,y,z)$?



Answer: $f(x,y,z)=0$ because any logic value for x NAND ($y=0$) yields a NAND gate output of 1. 1 NAND $z = z' = 1' = 0$.

6. Under what conditions does a full adder generate Sum = 0 and Carry out = 1 from Augend, Addend, and Carry in? Show your answer in the form of a table.

Answer:

Augend	Addend	Carry in	Sum	Carry out
1	1	0	0	1
0	1	1	0	1
1	0	1	0	1

7. What is the key idea that shows how to use fundamentally analog circuits so that they behave digitally?

Answer: Design the circuit to accept inputs falling within two voltage bands corresponding to logic signals 0 and 1. Design the circuit to have a sufficient voltage gap between the bands to prevent noise from causing a 0 to be confused with a 1 and vice versa. Finally, design the circuit to produce outputs that are of higher digital quality than the minimum acceptable quality of inputs.

8. What principle allows for the simplification of descriptions of hardware by omission of unimportant detail?

Answer: Abstraction.

9. You are given (zero cost of acquisition) a Cray-2 and an iPad 2 and quality places to operate them. Assume that both computers have the same application program that you wish to run. Assertion: Since these computers are equally fast, you have no preference as to which one you use. State whether you agree or disagree with the assertion and explain why.

Answer: We should disagree with the Assertion because the cost of operation differs substantially between these two computers. Using the Cray-2 requires purchasing far more electrical energy to accomplish the same computational task than does using the iPad 2. For the same reason, Purdue University removes its massive cluster computers when they complete five years of service. A five-year-old cluster typically uses so much more electricity than a new cluster that a business case analysis easily shows cost savings from removing the old machine from campus.