jCS 250 Spring 2017 - Lab 02
Due in lab Jan. 31 through Feb. 03, 2017
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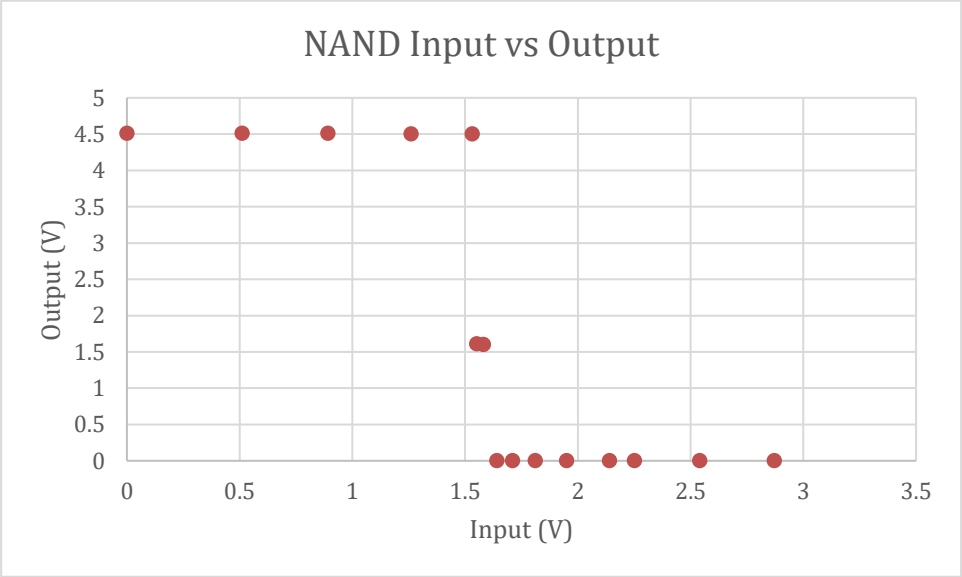
In-Lab Experiments, Part 1

1. [5 points] As you turn the potentiometer knob to move terminal 2 from terminal 1 (connected to the 470 ohm resistor) towards terminal 3 (connected to ground), the Analog Input voltage linearly changes from 5 volts to 0 volts. Carefully observe Red LED1 and Red LED2. Describe the behavior of the two LEDs with respect to the action of the potentiometer.
   When the potentiometer is turned completely counter clockwise, the LED is fully lit. As I turn the knob clockwise, LED 1 slowly dims till the potentiometer is halfway. Then LED 1 switches off and LED 2 switches on dimly, slowly getting brighter as the knob is being turned clockwise. LED 1 dims and brightens slower than LED 2.

2. [15 points] Plot your data point pairs (NAND1 input voltage from potentiometer, NAND1 output voltage). Comment on the shape of the function NAND1 output voltage = f(NAND1 input voltage from potentiometer) displayed in your plot. Does f show digital behavior?



   Yes, this behaves digitally because the output switches from a logic low to logic high with little twist of the potentiometer.

3. [10 points] NAND1 produces a high quality (more digital) output signal despite the many poor quality logic 0 and logic 1 voltages and voltages within the gap between the valid logic levels that the potentiometer voltage provides to NAND1. Why is the behavior of NAND1 to a poor quality input so important to computer circuits comprised of billions of transistors?
   The following input of the NAND output needs a clear high or low signal in order to operate properly and the NAND1 gives a clear logic low and logic high as an output despite the low quality inputs.

In-Lab Experiments, Part 2

4. [10 points] Fill in the following table with your observations from Part 2 experiments.

Clock source	Typical number of bounces observed from LEDs A, B, C, D (74163 output)
Clock 1 (potentiometer)	6 or 7 per 16 modulo count
Clock 2 (SPST switch)	1 or 2 per 16 modulo count
Clock 3 (SPDT switch)	Too many to count per 16 modulo count
Clock 4 or 5 (SR Q or Q')	0

Take Home Questions

5. [10 points] Why is skipping consecutive numbers in the output of the 74163 counter an indication of switch bounce?
   The counter counts per rising edge, where the bounce of contact creates multiple rising edges, therefor accounting for the skipping consecutive numbers.

6. [10 points] If the 74163 advances the count by 1 for a single Clock 3 input this means that the switch did not bounce that time. True or False? Explain your answer.
   False, there is the case where the counter would skip a full 16 modulo plus 1. If quick enough, we would think it did not bounce.

7. [10 points] What is the mathematical expression for the number of bounces observed by the 74163 chip circuitry as contrasted with the number of bounces that your eyes are capable or observing by examining the 74163 output using LEDs A, B, C, and D?
   The relationship of the number of bounces that happen vs the number we see is modulo 16. Observed = Actual % 16 because of the 4 bit counter.

8. [10 points] How does the memory capability of the SR latch (NAND2 and NAND3) transform the bouncing SPDT switch input into a bounce-free output?
   The memory capability stores the same input value as the switch bounces. This output ensures that any bounce will not change the output.

9. [20 points, 5 points each of the four parts] Design a logic circuit to compute the function F(A,B,C) = 1 when at least two of the A, B, and C inputs are logic value 1. Show the following for F(A,B,C): (1) truth table, (2) K-Map, (3) minimized Boolean expressions in both SOP and POS form, (4) draw schematics for both the SOP and POS expressions using NAND and NOR gates, respectively.

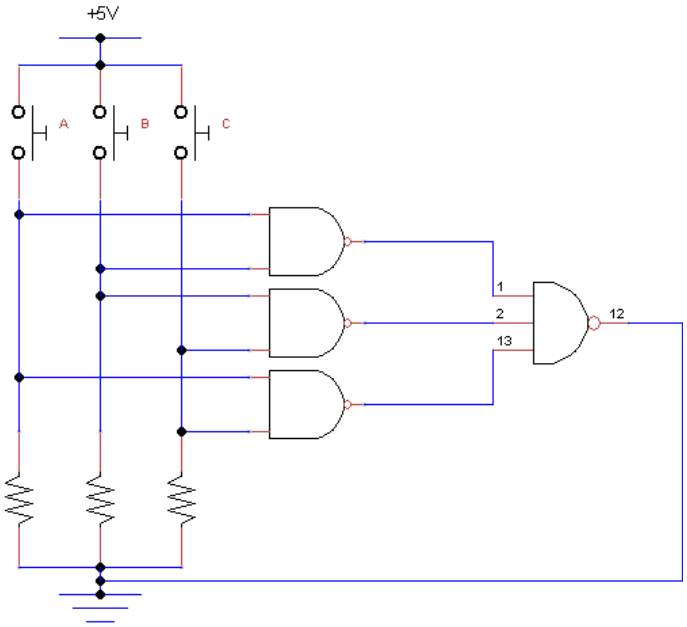
A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

C\AB	00	01	11	10
0	0	0	1	0
0	0	1	1	1

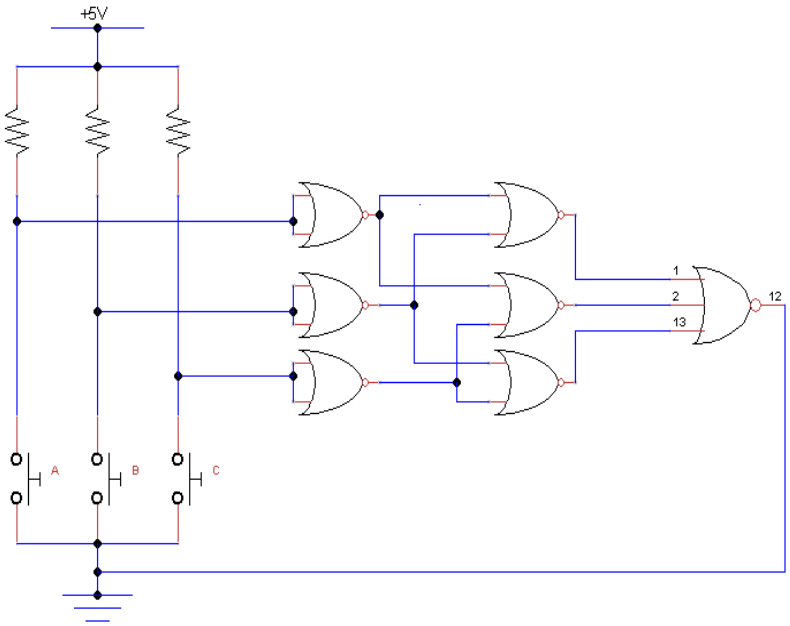
CS250 Spring 2017 Lab 02 Assignment

SOP: AB + BC + AC
POS: (A` + B`)*(A` + C')*(B` + C')

SOP



POS



**The POS representation can actually be reduced from using 6 2-input NOR gates to 3 when the input is switched to active high, therefor being more efficient. I wanted to diagram the one that matches the POS statement shown.