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A Combined Techniques of PC + MPC + APC to Achieve Higher Error Correction Probability and Throughput over APC and MPC Techniques

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Abstract
A new combined technique of Packet Combining (PC), Modified Packet Combining (MPC) and Aggressive Packet Combining (APC) is presented for improving the performance of MPC and APC. The proposed protocol consists of three blocks; PC block, MPC block, and APC block. Two copies of the same packet are sent from transmitter to receiver (Rx). If both the copies are found as erroneous then PC technique is used to correct the original copy in the PC block and if it is not obtained a successful copy then the Rx requests for a third copy. Again, if the third copy is found as erroneous then MPC and APC techniques are implemented in the MPC and APC blocks respectively. In order to get fast error correction and also to utilize the half-corrected or resultant copies instead of discarding the received erroneous copies, MPC block uses the resultant copies of the PC block and APC block also uses the resultant copies of MPC block. Thus, the proposed protocol is simulated using MATLAB and the simulation results obtain better performance by adopting the evaluation metrics of the probability of packet error correction, packet throughput and energy consumption over conventional MPC and APC techniques.

Keywords PC · MPC · APC · XOR operation · ARQ · Bit error rate · S/W ARQ

1 Introduction

Backward Error Correction (BEC) and Forward Error Correction (FEC) are two reliable strategies for data transfer from source to destination in the network. However, FEC method is more suitable for long distance wireless communication whereas BEC method is used for data transfer in wired communication as it is cost effective because an erroneous copy is corrected by retransmission from the transmitter. Several researches have been attempted to apply BEC in wireless communication as BEC is

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cost effective. BEC is implemented by automatic repeat request (ARQ) [1–3]. In data communication, the Stop and Wait (S/W), Go-Back-N and Selective Repeat of ARQ techniques have been implemented for error control [4–7]. The important parameter to measure one of the three techniques is throughput efficiency. In these ARQ techniques, the Rx recovers the original copy by means of retransmission of duplicate copies. BEC uses error detection code unlike FEC that is costly as it consumes higher bandwidth for using error correction code. In order to realize the best of all, it is decisively desirable to employ ARQ in modified schemes i.e. (BEC + FEC) to combat the error in wireless networks. The bit error rate of wireless channels is high [8–10] in the range of 10^{-2}–10^{-4}. For enabling a reasonable performance in radio link bit error rate requires to be within a range of 10^{-6}–10^{-8} [11]. In order to achieve the desirable quality in high bit error rate wireless channels, two modified ARQ schemes have been found in the literature: Multiple Route Packet combining scheme [12] and Aggressive Packet Combining Scheme (APC) [12]. APC does not address of improving throughput rather attempts to lower down complexities of handheld device, power consumption and bandwidth utilization in the uplink. Chakraborty [13–15] well suggested a simple and an elegant scheme based on BEC technique, called Packet Combining (PC) technique. The technique aims to fast error correction process. Several modifications of PC are also found in literature and these are Modified Packet Combining Scheme [16], Packet Reverse Packet Combining Scheme [17] and Error Forecasting PC [18]. In PC technique, error correction is done with two erroneous copies by the receiver. This scheme is appropriate when probability of Bit Error Rate (BER) is lower. In PC, the erroneous copies are XORed in order to identify the erroneous bit position. Once the error position(s) is (are) identified, bit by bit inversion process is carried out. The limitation of PC is: the technique fails when error(s) location(s) is at the same position of erroneous copies which is also called hidden error. Thus, the throughput of PC is 50% with one bit error correction capability. On the other hand, MPC works on three erroneous copies after storing at the receiver and performs XOR operation in order to find out the minimum number of bit-erroneous location among the pair-wise erroneous copies. Thus, MPC provides higher error correction capability by correcting two bits error but lower throughput than PC.

The bit error rate of wireless channels is high. Thus, in uplink data communication, by characteristics the transmitter may retransmit a particular packet multiple times before the receiver receives the correct one. Each and every retransmission consumes communication bandwidth and transmission energy. The bandwidth is a scarce/valuable resource because many portable computers may be sharing a limited free space spectrum. The energy is also a scarce/valuable resource because the portable computer is usually powered by battery. Therefore, to utilize the bandwidth and battery energy efficiently it is desirable to reduce the number of retransmissions.

In conventional BEC, the receiver discards the erroneous packet and requests the transmitter for a retransmission. However, an erroneous packet may contain both erroneous bits and correct bits and hence it may still contain useful information. The receiver may be able to combine this information from multiple erroneous copies to recover the correct packet. Wicker [19] proposed the majority packet combining scheme. This scheme performs bit-by-bit majority voting on the erroneous copies and then performs error detection on the resulting combined packet. If the combined packet is found to be correct, the receiver accepts it; otherwise, the receiver requests the transmitter for a retransmission. Several researchers have also been modified the APC technique in order to get higher throughput and higher error correction capability [20–26] but still found the lack of utilizing the processed erroneous copies i.e. resultant copies from PC or MPC techniques.

Thus, in order to utilize the resultant erroneous copies and fast error correction the combined technique of PC, MPC and APC is proposed. The contribution of the manuscript is firstly sent the two duplicate copies of the original packet from Tx to Rx. If either of the copies is found correct copy then the remaining copy is discarded the and the Tx is used to request for next packet. If both the copies are received as erroneous copies then PC block performs conventional PC technique (XOR operation[1]) and the Rx will be requested for third duplicate copy if PC technique fails to recover the original copy. If the third copy is found as the correct copy then the Rx will discard the previously received copies from PC block. Secondly, if the third copy is also found as erroneous then the three erroneous copies perform pair wise XOR operation[2] and XOR operation[3] in the MPC block. In order to get fast error correction, the MPC block uses the resultant copies from PC block and then APC block also uses the resultant copies from MPC block. Thus, the combined technique yields better results over conventional MPC and APC techniques. Lastly, from the simulation results, the proposed protocol also provides Cost Performance Index (CPI) in terms of probability of packet error correction and packet throughput in Tables 8 and 9. The CPI values are found greater than 1and hence; the proposed protocol is found higher quality and more reliability in terms of probability of packet error correction and packet throughput over conventional MPC and APC techniques.

The manuscript is divided into six sections and organized as follows: Related works comprise Packet Combining, Modified Packet Combining Scheme and Aggressive Packet Combining scheme that are described in Sect. 2. Sections 3 and 4 discuss about proposed scheme and numerical analysis of probability of packet error correction, throughput, and energy consumption. Section 5 explains about simulation results and conclusion is discussed in Sect. 6.

2 Related Works

2.1 Packet Combining Scheme (PC)

In this technique, if the packet is received erroneously then the receiver stores the erroneous copy and Rx requests for duplicate copy by sending NACK to the Tx. If the duplicate copy is obtained the original copy then the Rx requests for next packet. If the Rx is not found the original copy then it stores the duplicate copy and performs XOR operation ($\oplus$) of two erroneous copies for locating erroneous bit positions. Let the original packet is "10101010". Assume the Rx receives on first transmission copy as "00101010" which is an erroneous. Assume the Rx receives the copy on retransmission as "10101000" which is also an erroneous. Now XOR operation is performed with the two erroneous copies.

Table 1 Modified packet combining scheme

Copies of erroneous pairs	Erroneous bits (y)	Erroneous detected position
[C-2 $\oplus$ C-1]	1 bit	6th position from MSB
[C-1 $\oplus$ C-3]	2 bits	5th and 7th positions from MSB
[C-3 $\oplus$ C-2]	3 bits	5,6 and 7th positions from MSB

$$
\begin{array}{c}
00101010 \\
\oplus \\
10101000 \\
\cdots\cdots\cdots \\
10000010
\end{array}
$$

Error locations are identified at 1st and 7th positions from MSB. Bit inversion technique (converts 0–1 or 1 to 0) is performed on two erroneous copies at identified locations. Finally, it checks for error detection and hence it may get the original copy.

Assume original copy: "00001111" and also assume that Rx receives the first and second erroneous copy as "00000111" and "00000111".

$$
\begin{array}{c}
00000111 \\
\oplus \\
00000111 \\
\cdots\cdots\cdots \\
00000000
\end{array}
$$

(PC technique fails to identify the erroneous bit location due to erroneous occurred at the same bit position also called hidden error). Thus, PC requires discarding the whole erroneous copies and it repeats the same technique.

2.2 Modified Packet Combining Scheme (MPC)

The MPC technique is used to enhance the error correction done by PC. In this scheme, three erroneous copies are XORed in a pair wise in order to find the bit error location. The three erroneous copies are assumed as Copy (C) C-1, C-2 and C-3and then pair wise XOR operation is carried out among (C-2 $\oplus$ C-1), (C-3 $\oplus$ C-2) and (C-1 $\oplus$ C-3) to locate the erroneous bit position.

Assume an original packet "11100111" is received as three erroneous copies at the C-1 = 11101111. The example is shown below:

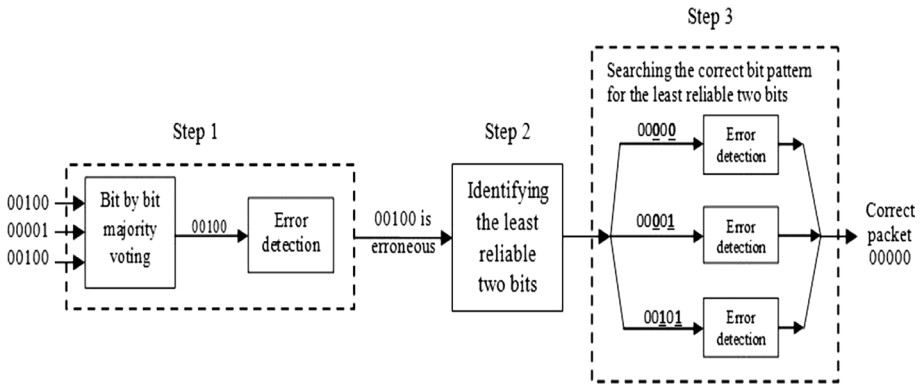

Fig. 1 Block diagram of conventional APC

$$C\text{-}2 = 11101011$$
$$C\text{-}3 = 11100101$$

Now performing XOR operation between

$$C\text{-}2 \oplus C\text{-}1 = 00000100$$

$$C - 3 \oplus C - 2 = 00001110$$

$$C\text{-}1 \oplus C - 3 = 00001010$$

The ascending orders based on common erroneous bit positions are indicated by XOR operation which is clearly indicated in Table 1. Thus, error correction will start from C-1 and if necessary then C-3 and it will be followed by C-2. However, if the above process fails to recover the original copy then the same procedure will be repeated after discarding all the erroneous copies.

2.3 Aggressive Packet Combining Scheme (APC)

APC is an extension technique of Majority Packet Combining for performing higher error control in a wireless network. It consists of three steps and it is illustrated as follow:

Step 1: Let the three erroneous copies CP_1^{err}: 00100, CP_2^{err}: 00001 and CP_3^{err}: 00100 are buffered at the receiver and then it performs bit by bit majority voting and resultants bits are checked by error detection block whether it is erroneous bit exist or not. If the Step 1 recovers the original copy then receiver requests for next packet, if not then Step 2 and Step 3 will be performed.
Step 2: This step performs to find the least reliable bits from Step 1. And the brief example is explained in Fig. 1. In this case 3rd and 5th bits from MSB are detected as the two least reliable bits.

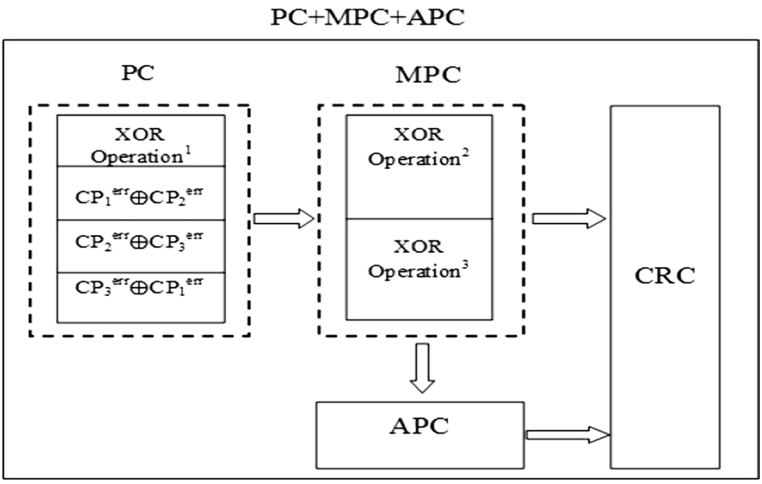

Fig. 2 Block diagram of proposed work

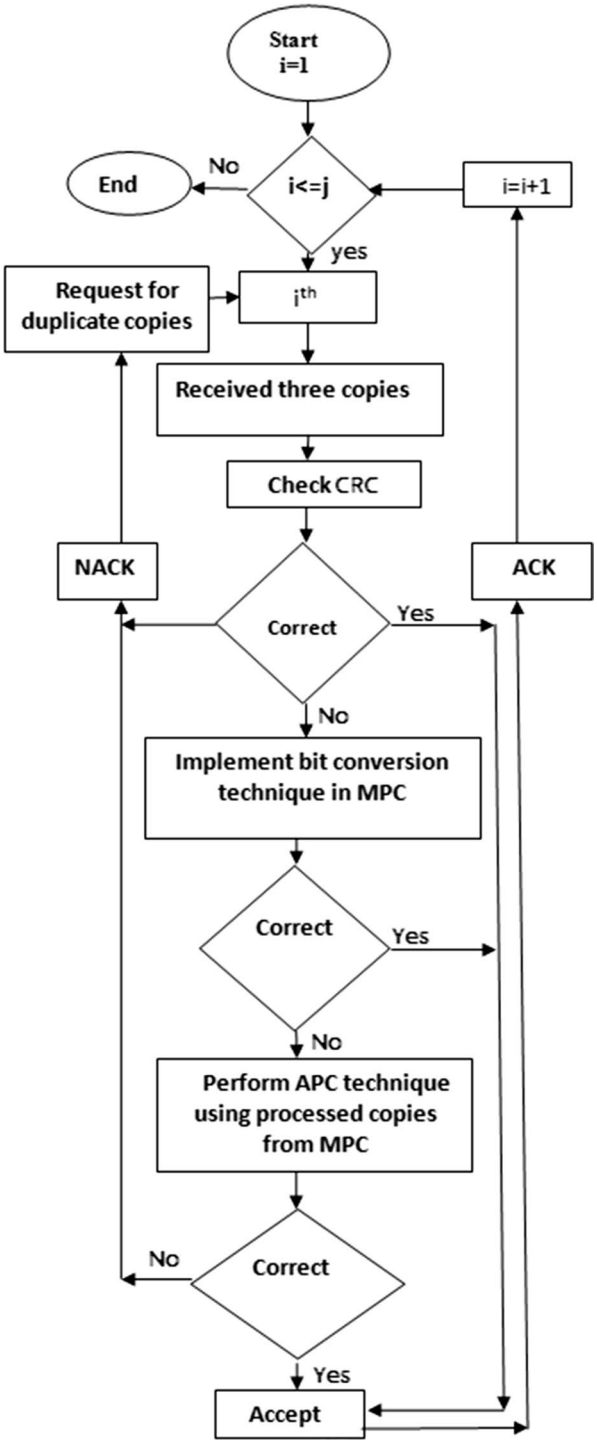

Fig. 3 Flow Chart of the proposed work

Table 2 The example of proposed scheme under PC and MPC blocks with original copy, $\mathbf{O^r = 11111}$

Example 1 Original copy O^r=11111	PC block	MPC block		Output
No. of rounds	XOR operation[1]	XOR operation[2]	XOR operation[3]	
1st round CP_1^{err} =01011and CP_2^{err}=01101	01011 01101 …… 00110	X^1=01111 01101 ……... 00010	X^1=01111 X^2=01111 …… 00000	01111 (Not Correct copy)
2nd round CP_2^{err}=01101 and CP_3^{err}=10111	01101 10111 …… 11010	Y^1=**1**1111 10111 …….. 01000	Y^1=**1**1111 Y^2=11111 …… 00000	11111 (Correct copy)
3rd round CP_3^{err}=10111 and CP_1^{err} =01011	10111 01011 …… 11100	Z^1=**000**11 01011 …… 01000	Z^1=**000**11 Z^2=00011 …… 00000	00011 (Not correct copy)

Step 3: This step is used to find the correct bit sequences for the least reliable bits. In this case, 00, 01, 10 are the possible correct bit pattern which can be obtained from 2^l-1 and 'l' is the number of least reliable bit. Thus, error detection block checks all the possible bit sequence whether it is correct copy or not. Finally, "00000" bit sequence is found as correct copy.

3 Proposed Protocol

The main notion of the proposed scheme is to reduce the retransmission of the duplicate copies by increasing the probability of packet error correction. Firstly, the PC technique is used to perform XOR operation among two received erroneous copies (let CP_1^{err} and CP_2^{err}). If PC technique fails to recover the original copy then it will not discard the whole erroneous copies and it will request for next duplicate copies. If the third copy is obtained the correct copy then Rx discards the received erroneous copies; and if the Rx is not obtained the original copy then it will buffer the erroneous copy and it will continue to perform pair-wise XOR operation (let $CP_2^{err} \oplus CP_3^{err}$; and $CP_3^{err} \oplus CP_1^{err}$) in order to find the erroneous bit position. It is also well known from the literature that MPC is the modified technique of PC and thus the pair-wise XOR operation is nothing but PC technique. Therefore, the basic logic that implementing in the proposed protocol is to utilize the half-corrected copies or resultant copies from PC block instead of discarding the half-corrected copies. Thus, in the proposed protocol, we have combined the PC, MPC and APC in order to utilize the resultant copies and also for fast error recovery by increasing the probability of packet error correction, packet throughput and finally the system consumes less communication energy if it reduces the retransmission of duplicate copies. The Figs. 2 and 3 show the block diagram and flow diagram of the proposed scheme. The block diagram consists of three blocks viz. PC, MPC and APC. The MPC block uses the resultant copies from PC and APC block uses the resultant copies from MPC. The Tables 2, 3, 4, 5, 6 and 7 show the comparative examples of the proposed protocol and the conventional techniques.

The stepwise procedure of the proposed scheme is given below:

Table 3 The example of proposed scheme under APC block with original copy, $\mathbf{O^r = 11111}$

APC block			
Majority voting of X^1, Y^1 and Z^1	Number of least reliable bits (l)	Number of searching correct bit patterns ($2^l - 1$)	Output
01111 11111 00011 …….. **011**11(Not correct copy)	3	000 001 010 100 101 110 **111**	11111 (correct copy)

1. The proposed protocol consists of Rth rounds and each round is categorized into XOR operation[1] under PC block and also XOR operation[2] and XOR operation[3] under MPC block.
2. In the 1st, 2nd and 3rd rounds, PC performs paired wise XOR operation[1] of CP_1^{err} and CP_2^{err}; CP_2^{err} and CP_3^{err}; and CP_3^{err} and CP_1^{err}. Thus, the erroneous bit locations can be identified.
3. The X^1 operation converts the possible erroneous bit locations in CP_1^{err} in such a way that if 0 then 1 or 1 then 0 but not both i.e. if $1 \rightarrow 0$ *but* $0 \rightarrow 0$ *or if* $0 \rightarrow 1$ *but* $1 \rightarrow 1$ and then paired wise XOR operation[2] will be performed with CP_2^{err} to minimize the erroneous bit location.
4. Similarly X^2 operation converts the possible erroneous bit locations in CP_2^{err} in such a way that if 0 then 1 or 1 then 0 but not both i.e. if $1 \rightarrow 0$ *but* $0 \rightarrow 0$ *or if* $0 \rightarrow 1$ *but* $1 \rightarrow 1$ and then XOR operation[3] will be performed with X^1. Finally, CRC operation is performed to check whether it is an original copy or not.
5. The 2nd and 3rd rounds of MPC block also perform similar operation to step 3 and step 4 i.e. the bit conversion technique of $X^1 = Y^1 = Z^1$ and also $X^2 = Y^2 = Z^2$.
6. In APC block, X^1, Y^1 and Z^1 or X^2, Y^2 and Z^2 from the resultants of MPC block performs APC technique which is similar to the technique of conventional APC but the copies are half corrected erroneous copies instead of CP_1^{err}, CP_2^{err}, and CP_3^{err}. Tables 2 and 5 show the example of PC and MPC of the proposed scheme. Tables 3, 4, 6 and 7 illustrate the compared examples of proposed scheme of APC and conventional APC.

Table 4 The example of conventional APC with original copy, $\mathbf{O^r = 11111}$

Conventional APC scheme				
Majority voting of $CP_1^{err} = 01011$, $CP_2^{err} = 01101$, $CP_3^{err} = 10111$	Number of least reliable bits (l)	Number of searching correct bit pattern ($2^l - 1$)		Output
01011 01101 10111 …….. **0111**1(Not correct copy)	4	0000 0001 0010 0100 0101 0110 0111 1000	1001 1010 1011 1100 1101 1110 **1111**	11111 (correct copy)

Algorithm: Proposed scheme

/* Error control (detection and correction) to be performed by receiver*/

/* Buffered the erroneous copies instead of discarding the received erroneous copies CP_1^{err}, CP_2^{err} and CP_3^{err} ****/***

/*Assumed all the ACK and NACK packets are error free and always successfully transmission*/

Input: $CP_i^{err}{}_{i=1,2,3...m}$***, where m is odd integers***

Output: Success or failure

if *(PC block stores three erroneous copies (*CP_1^{err}, CP_2^{err} *and* CP_3^{err}*))* ***then***

{

XOR operation[1] will be performed of each round

{

$CP_1^{err} \oplus CP_2^{err}$ *&&* $CP_2^{err} \oplus CP_3^{err}$ *&&* $CP_3^{err} \oplus CP_1^{err}$

if *(XOR operation[1] recovers the original copy)* ***then***

{

Request for next packet

}

Else

{

XOR operation[2] followed by XOR operation[3] under MPC block will be performed of each round and also X^1, Y^1 *and* Z^1 *or* X^2, Y^2 *and* Z^2 *copies from MPC block will be performed APC technique in APC block,*

}

}

if *(XOR operation[2] || XOR operation[3] || APC technique success CRC test)* ***then***

{

Request for next packet

}

Else

{

Request two copies of same packet by sending NACK and same procedure will be repeated for five erroneous copies.

}

}

The Tables 2 and 3 show the examples of proposed scheme and Table 4 shows the conventional APC technique when an original copy, $O^r = 11111$ transmits from Tx to Rx. In Table 2, erroneous copies are buffered in PC block as $CP_1^{err} = 01011$ and $CP_2^{err} = 01101$ (erroneous bits are marked in red color) and XOR operation[1] is used to perform in the 1st round in order to identify the erroneous bit location. Assume that XOR operation[1] under PC block fails to recover the original copy and therefore it requests for third copy. Let the third erroneous copy as $CP_3^{err} = 10111$ is received and it performs pair-wise XOR operations of $CP_2^{err} = 01101$ and $CP_3^{err} = 10111$, $CP_3^{err} = 10111$ and $CP_1^{err} = 01011$ in 2nd and 3rd rounds under PC block. From the 1st, 2nd, and 3rd rounds the erroneous bits are identified (marked as underlined). The MPC block uses the resultant copies from PC block and it converts CP_1^{err} into X^1, CP_2^{err} into Y^1 and CP_3^{err} into Z^1 and they are performed XOR operation[2] under MPC block and it can reduce the number of erroneous bits. The MPC block performs XOR operation[3] ($X^1 \oplus X^2$, $Y^1 \oplus Y^2$, and $Z^1 \oplus Z^2$) in each round and finally, MPC block recovers the original copy in the 2nd round under XOR operation[2]. Again from Table 2, we show an example that if conventional MPC implements then the number of erroneous bits found in the 1st, 2nd and 3rd rounds are $CP_1^{err} \oplus CP_2^{err} = 2$, $CP_2^{err} \oplus CP_3^{err} = 3$ and $CP_3^{err} \oplus CP_1^{err} = 3$ but the proposed scheme under MPC block reduces the number of erroneous bit i.e. 1st round (X^1 v $CP_2^{err} = 1$), 2nd round ($Y^1 \oplus CP_3^{err} = 1$) and 3rd round ($CP_3^{err} \oplus Z^1 = 1$). Similarly, Tables 5, 6 and 7 are also detailed another example when Tx transmits an original copy, $O^r = 00011$. It also reduces the number of erroneous bits when

Table 5 The example of proposed scheme under PC and MPC blocks with original copy, $\mathbf{O^r = 00011}$

Example 1 Original copy O^r=00011	PC block	MPC block		Output
No. of rounds	XOR operation[1]	XOR operation[2]	XOR operation[3]	
1st round CP_1^{err} =11011and CP_2^{err}=10011	11011 10011 …… 01000	X^1=**00**011 10011 …….. 10000	X^1=**00**011 X^2=**0**0011 …… 00000	00011 (correct copy)
2nd round CP_2^{err}=10011 and CP_3^{err}=00000	10011 00000 …… 10011	Y^1=**00**011 00000 …….. 00011	Y^1=**00**011 Y^2=000**11** …… 00000	00011 (correct copy)
3rd round CP_3^{err}=00000 and CP_1^{err} =11011	00000 11011 …… 11011	Z^1=110**11** 11011 …….. 00000	No error detection	11011 (Not correct copy)

comparing both the conventional MPC and proposed scheme under MPC block and finally it recovers the original copy in the 1st round by XOR opeartion[2].

In Tables 3 and 4 show the comparative examples of proposed scheme under APC block and conventional APC scheme. The resultant copies X^1, Y^1 and Z^1 from MPC perform majority voting and it detects the number of least reliable bits ($l=3$) but in conventional APC the majority voting has been done among the erroneous copies i.e. CP_1^{err}, CP_2^{err} and CP_3^{err} and found the value of $l=4$. Thus, we can see that the number of least reliable bits can be reduced by proposed scheme and hence the searching bit pattern can also be reduced to $2^{l-i}-1$, $i=1,2,3\ldots l$. Similarly, From Tables 6 and 7, another example is shown and the value of l is also reduced.

4 Numerical Analysis

It is assumed that the three erroneous copies are received and stored in the buffer. Let the packet size of the erroneous copy is 'n' and 'p_e' is the probability of BER. Let k_r denotes the number of error bits in the rth corrupted copies and $p(k_r)$ is the probability of having k_r error bits at the rth corrupted copies, where $r \geq 2$ [27].

Table 6 Proposed example of APC block with original copy, $\mathbf{O^r = 00011}$

APC block of proposed scheme				
Majority voting of X^1, Y^1 and Z^1	Number of least reliable bits (l)	Number of searching correct bit patterns ($2^l - 1$)		Output
00111 00011 11011 …… **000**11	3	**000** 001 010 110	101 110 111	00011(correct copy)

Table 7 Example of conventional APC with original copy, $\mathbf{O^r = 00011}$

Conventional APC scheme					
Majority voting of $CP_1^{err} = 11011$ $CP_2^{err} = 10011$, $CP_3^{err} = 00000$	Number of least reliable bits	Number of searching correct bit patterns (2^{l}-1)			Output
11011	4	0000	0101	1011	00011(correct copy)
10011		0001	0110	1100	
00000		0010	0111	1101	
……		**0011**	1000	1110	
10011(correct copy)		0100	1001	1111	
			1010		

The probability of successfully getting at least one original copy by the PC, MPC and APC techniques if they perform independently at the receiver and it is given by Eq. (1)

$$PEC_{prop} = PEC_{prop} = \frac{\left(1 - PE_x\right) \cdot PE_{PC} \cdot PE_{MPC} \cdot PE_{APC}}{PE_x} \tag{1}$$

where PEx is the probability of packet error (PPE) and x = PC, MPC and APC

The proposed protocol performs r number of paired wise XOR operation in PC and MPC blocks from the received erroneous copies. Thus, Eq. (2) gives the probability of two corrupted copies consist of k_i and k_j error bits ($i < j$), where the erroneous bits are random and independent events.

$$p_{i,j}(h) = \left[1 - \frac{\sum_{k_i=1}^{n} \sum_{k_j=k_i}^{n-k_i} \binom{n}{k_i}\binom{n-k_i}{k_j}}{\sum_{k_i=1}^{n} \sum_{k_j=k_i}^{n} \binom{n}{k_i}\binom{n}{k_j}}\right] \tag{2}$$

Since, the occurrences of error bits in the corrupted packets are independent events. Thus, the proposed work provides the conditional probability h_r when the CP_i^{err}, i = 1, 2, and 3 arrives at the receiver which performs 'r' pair-wise XOR operation. Thus, h_r can be given by Eq. (3)

$$h_r = \left[\frac{\sum_{k_1=1}^{n} \sum_{k_2=1}^{n} \cdots \sum_{k_r=1}^{n} p(k_1)p(k_2)\cdots p(k_r) \prod_{1 \le i,j \le r} P_{i,j}(h)}{[1 - (1-\alpha)^n]^r \prod_{l=2}^{r-1} h_l}\right] \tag{3}$$

Again, the proposed protocol also performs an APC technique from the processed or half corrected copies after MPC technique failed to obtain the original copy. Equation (4) gives the probability of packet error correction of the proposed protocol.

$$p_r^{prop}(ec) = \left[1 - \sum_{i=1}^{r-1} p_i^{prop}\right]\left[\left(1 - p_e\right)^n + \left(1 - \left(1 - p_e\right)\right)^n \cdot \left(1 - h_r\right)\right].$$

$$\left[1 - \left[1 - \left(1 - p_e\right)^n\right]^3 \cdot \left(1 - h_r\right)\right] \tag{4}$$

Thus, in order to compare the overall packet error probability of the proposed scheme and the conventional APC, the total packet error probability of the proposed scheme is

Table 8 CPI at packet size (n) = 128 bits

Bit error rate (*Pe*)	Cost performance index (CPI)			
	Proposed protocol over conventional MPC		Proposed protocol over conventional APC	
	x	y	x	y
0.006	1.014	1.037	1.190	1.076
0.008	1.053	1.076	1.342	1.452

Note: x = probability of packet error correction, y = packet throughput

Table 9 CPI at packet size (n) = 256 bits

Bit error rate (*Pe*)	Cost performance index (CPI)			
	Proposed protocol over conventional MPC		Proposed protocol over conventional APC	
	x	*y*	*x*	*y*
0.006	1.203	1.250	1.801	2.0
0.008	1.361	1.910	2.345	2.56

given by the difference of packet error probability of the conventional APC and the probability of the packet error correction of the proposed protocol and it is given by Eq. (5).

$$PE_{pro} = \left[1 - (1 - Pe)^n\right]^3 - \left[p_r^{prop}(ec)\right] \tag{5}$$

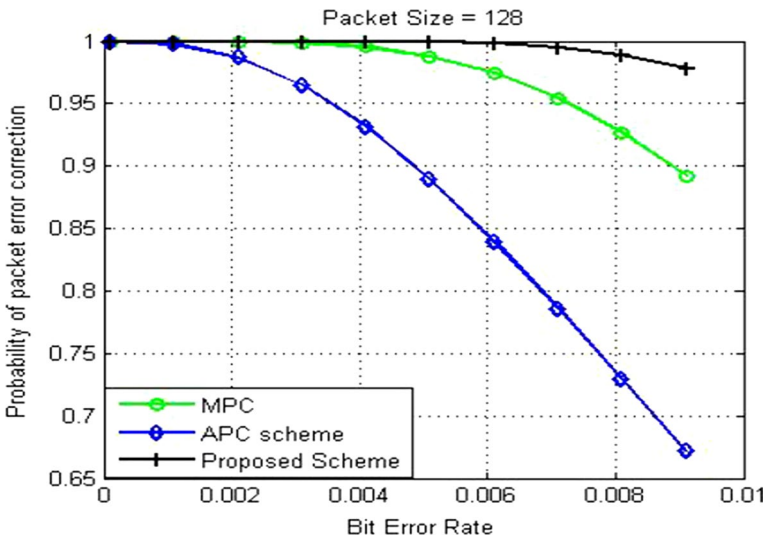

Fig. 4 PPEC with packet size (128 bits)

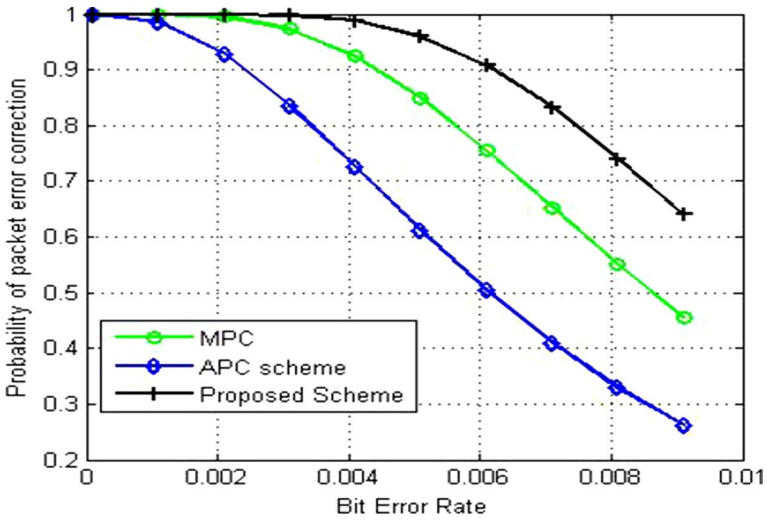

Fig. 5 PPEC with packet size (256 bits)

where $PE_{APC} = \left[1-(1-Pe)^n\right] \times \left[1-(1-Pe)^n\right] \times \left[1-(1-Pe)^n\right] = \left[1-(1-Pe)^n\right]^3$

From Eq. (5), the packet throughput efficiency [28] of the proposed protocol can be given by Eq. (6)

$$T_{pro} = \frac{1 - PE_{pro}}{3 + PE_{pro}} \tag{6}$$

Let the energy consumption is higher if the probability of packet error is higher. Therefore, the energy consumption (E) of the proposed scheme can be determined by Eq. (7)

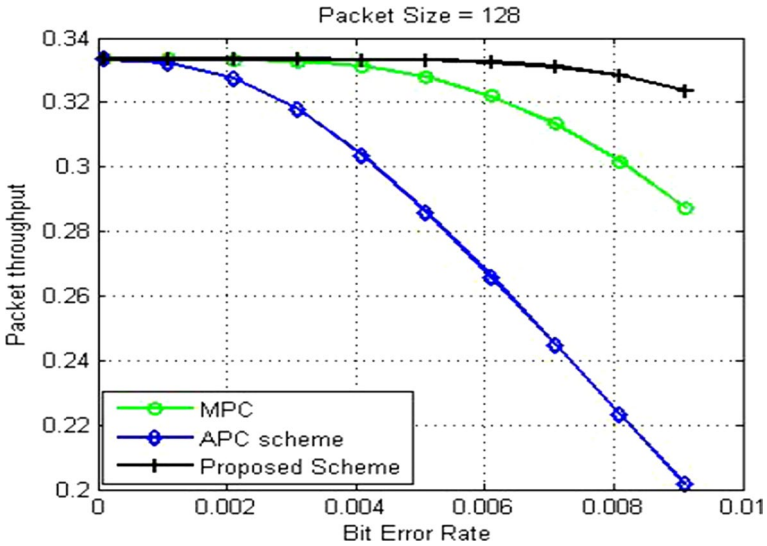

Fig. 6 Packet throughput of 128 bits packet size

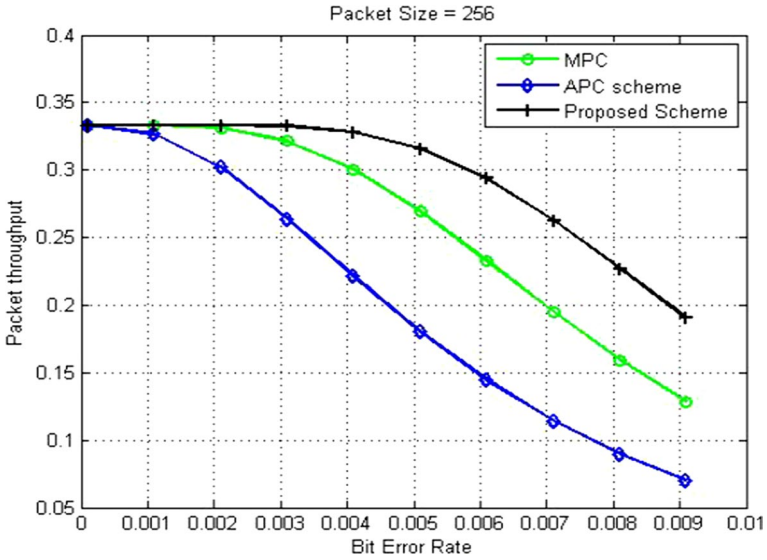

Fig. 7 Packet throughput of 256 bits packet size

$$E = \frac{1}{\left[1 - PE_{pro}\right]} \tag{7}$$

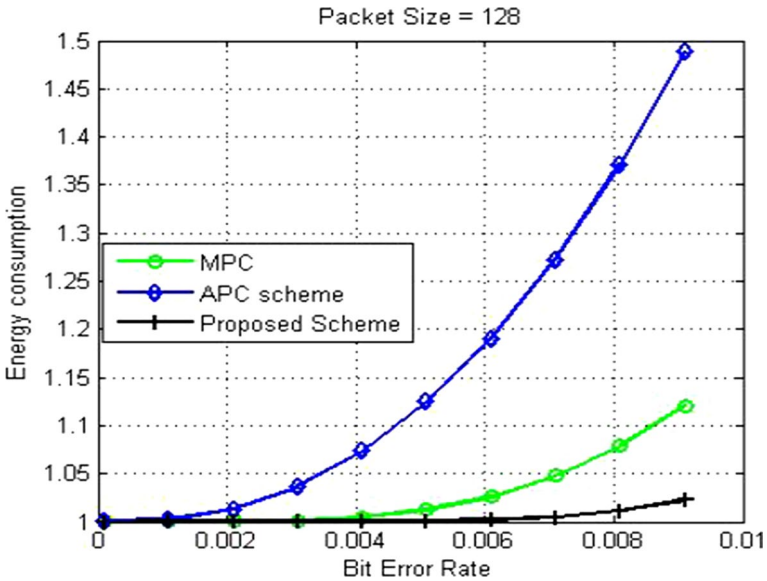

Fig. 8 Energy consumption with 128 packet size

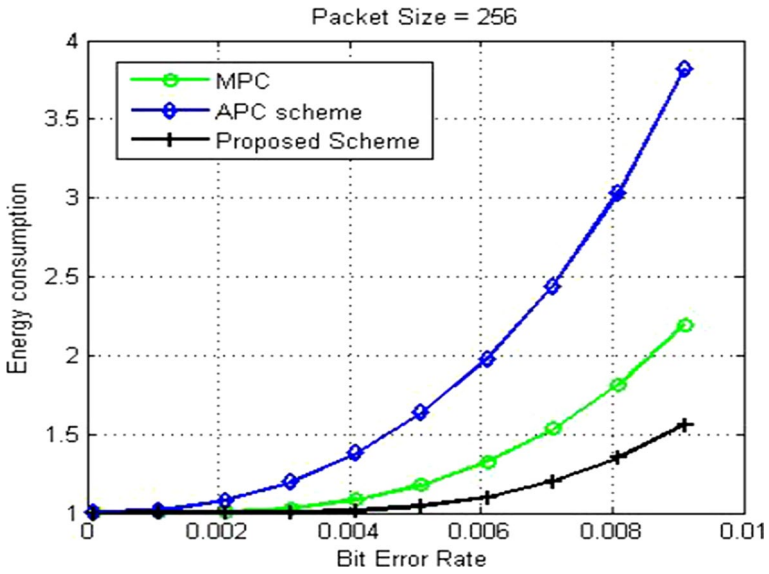

Fig. 9 Energy consumption with 256 bits packet size

5 Simulation Results

In simulation, the BER values of 10^{-4}–10^{-2} and Packet size of 128 and 256 bits are used as the input data for the analysis of probability of packet error correction, packet throughput and the energy consumption and the results of Figs. 4 and 5 show that the proposed scheme provides higher probability of packet error correction. The results of Figs. 6 and 7 also prove that the proposed technique provides higher packet throughput over conventional MPC and APC. Finally, the Figs. 8 and 9 illustrate the energy consumption of proposed scheme with the conventional MPC and APC techniques. The result shows that the proposed scheme also consumes lesser energy.

6 Conclusion

The conventional PC, MPC and APC techniques have been studied and reported for error control in the wireline and wireless networks. In order to increase the PPEC and packet throughput of conventional MPC and APC, the combined technique is studied by utilizing the resultant copies or half-corrected copies by PC and MPC techniques. The proposed protocol is simulated using MATLAB and in the simulation, the proposed scheme is compared with the conventional APC and MPC and it provides higher PPEC and packet throughput by reducing the number of erroneous bit location as well as the value of l (number of least reliable bits) when BER is increased. Thus, the proposed protocol can reduce the number of searching correct bit pattern from $2^l - 1$ to $2^{l-i} - 1, i = 1, 2, 3 \ldots l$ and also the cost performance Index (CPI) value is obtained higher when the BER values are higher. Hence, the proposed scheme enhances the performance of conventional MPC and APC and consumes relatively less energy as well.

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