J. Inst. Eng. India Ser. B (April 2020) 101(2):107–116
https://doi.org/10.1007/s40031-020-00443-y

ORIGINAL CONTRIBUTION

A Combined Technique of SC + MPC + APC to Achieve Higher Error Correction Probability and Throughput Over APC and MPC Techniques in a Wireless Network

Sanjit Ningthoujam[1] · Swarnendu K. Chakraborty[2]

Received: 11 October 2018 / Accepted: 11 April 2020 / Published online: 3 May 2020

Abstract In this paper, we present the combined techniques of Selection Combining (SC), Modified Packet Combining (MPC) and Aggressive Packet Combining (APC) for higher probability of packet error correction and packet throughput in three branches diversity system (multi-path) over conventional MPC and APC techniques. The three copies of the same packet are used to transmit from transmitter (Tx) to receiver (Rx) in three paths. Like in conventional SC technique, the Rx checks all the received copies individually from three paths whether the received copies are correct or not using frame checking sequences. If any one of the received copies is obtained, the correct copy then it will discard the remaining copies and request for next packet; otherwise the received erroneous copies will be combined. The combined erroneous copies perform '*r*' number of pair-wise XORed after the erroneous copies are performed bit converted in MPC technique. If '*r*' pair-wise XOR operations fail to recover the original copy, then APC technique implements with the converted bit stream. Thus, the simulation results using MATLAB obtain better performance in terms of probability of packet error correction and packet throughput over conventional MPC and APC schemes.

Keywords SC · MPC · APC · BER · ARQ · XOR operation

✉ Sanjit Ningthoujam
sanjit.n@vitap.ac.in

Swarnendu K. Chakraborty
swarnendu.chakraborty@gmail.com

[1] School of Computer Science and Engineering, VIT University, Amaravati, Andhra Pradesh, India

[2] Dept. of Computer Science and Engineering, NIT, Yupia, Arunachal Pradesh, India

Introduction

Backward error correction (BEC) and forward error correction (FEC) are two reliable strategies for data transfer from source to destination [1–3]. However, FEC method is more suitable for long distance wireless communication, whereas BEC method is used for data transfer in wired communication as it is cost effective because an erroneous copy is corrected by retransmission from the transmitter. In ARQ (automatic repeat request) methods, if the receiver receives an erroneous copy then it discards the erroneous copy and acknowledges by sending the negative acknowledgement (NACK). In order to recover the correct copy by storing the erroneous copies, PC is well studied [4]. Error correction is done with two erroneous copies by the receiver. This scheme is appropriate when probability of bit error rate (BER) is lower. In PC, the erroneous copies are XORed in order to identify the erroneous bit position. Once the error position(s) is (are) identified, bit-by-bit inversion process is carried out. The limitation of PC is: the technique fails when error(s) location(s) is at the same position of erroneous copies which is also called hidden error. Thus, the throughput of PC is 50% with one bit error correction capability. On the other hand [5], MPC works on three erroneous copies after storing at the receiver and performs XOR operation in order to find out the minimum number of bit-erroneous location among the combined erroneous copies. Thus, MPC provides higher error correction capability by correcting two bits error but lower throughput than PC. For improving ARQ techniques [6], selection combining (SC) was studied and reported in the literature. The scheme has been implemented for improving performance for combating fading in mobile communication systems. Prior to SC, ideal selection combining scheme (ISC) was also reported and it chose the branch with the best signal-to-noise ratio (SNR) to the output. However, the scheme was impractical due to the needing of a continuous channel monitoring as the selection has been done at every symbol period. The performance of ARQ techniques normally measured in terms of throughput efficiency but the SC measured in terms of average bit error rate.

For improving the throughput of normal ARQ protocols, APC scheme was implemented [7] in a wireless network. In this scheme, firstly bit-by-bit majority logic is performed among the erroneous copies in order to produce combined packet and original copy as well. Secondly, it identifies the least reliable bits which are used to search the correct bit pattern. Thus, the maximum throughput that can be attained by APC is only 33% if the scheme is recovered in the original copy. However, several researchers have also been studied and conclusively established different modification techniques of ARQ and APC [8–17] to improve the error control and system performance in a wireless network but lacked of addressing the concept of half-corrected erroneous copies from either PC or MPC techniques. The main motive of the proposed work is not only combining of the erroneous copies but also to utilize the processed erroneous copies in SC and MPC techniques instead of discarding the processed copies. Thus, the conventional APC is implemented with the processed erroneous copies and it can reduce the number of average searching correct bit sequences after the value of '*l*' (the number of least reliable value) is reduced.

The manuscript is divided into five sections and categorized as follows. "Related Works" are explained in second section. The third section describes the "Proposed Work" and the "Numerical and Simulation Analysis" are discussed in fourth section. Finally, "Conclusion" is discussed in fifth section.

Related Works

Majority Packet Combining Scheme

S.B Wicker proposed the majority packet combining scheme. This scheme performs bit-by-bit majority voting on the received erroneous copies and then performs error detection on the resulting combined packet. If the combined packet is found to be correct, the receiver accepts it; otherwise, the receiver requests the transmitter for the duplicate copies. If this technique fails to obtain the original copy then discards the whole copies.

From this majority combining scheme, Leung has been proposed the technique called aggressive packet combining scheme (APC) for error control in uplink data communication (Fig. 1).

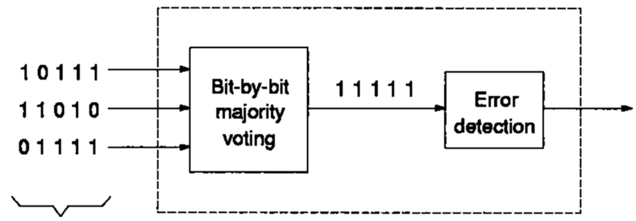

Fig. 1 Majority packet combining. In this example, it can recover the correct packet [5]

Aggressive Packet Combining Scheme

Leung has been introduced an extension technique of majority packet combining called aggressive packet combining (APC) for performing higher error control in a wireless network. It consists of three steps and illustrated as follows:

Step 1: Let the three erroneous copies CP_1^{err}: 00100, CP_2^{err}: 00001 and CP_3^{err}: 00100 are buffered at the receiver and then it performs bit-by-bit majority voting and resultants bits are checked by error detection block whether it is erroneous bit exist or not. If the Step 1 recovers the original copy then receiver requests for next packet, if not; Step 2 and Step 3 will be performed.

Step 2: This step performs to find the least reliable bits from Step 1. And the brief example is explained in Fig. 2. In this case, 3rd and 5th bits from MSB are detected as the two least reliable bits.

Step 3: This step is used to find the correct bit sequence for the least reliable bits. In this case, 00, 01, 10 are the possible correct bit patterns which can be obtained from 2^l-1 and '*l*' is the number of least reliable bit. Thus, error detection block checks all the possible bit sequence whether it is correct copy or not. Finally, "00000" bit sequence is found as correct copy. If this technique fails to find the correct copy then discards the whole erroneous copies and requests for next duplicate in order to repeat the same procedure.

Selection Combining Technique

Liang et al. assumed that from Tx to Rx, it is connected by a 3-branch and the copies are transmitted over three diversity branches and received by three different receivers. Each block is appended with a cyclic redundancy check (CRC) to aid in detection of errors. Three SCs in conjunction with ARQ in the block level are also considered. Later three modified techniques of SC have been modified and explained here under.

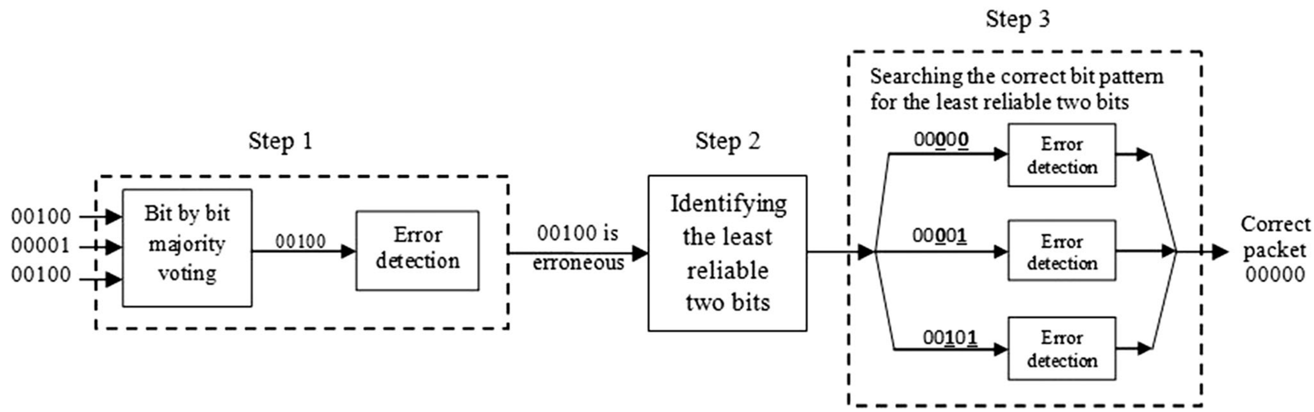

Fig. 2 Block diagram of conventional APC [7]

ARQ Based on SAH-SC(ARQ-SAH-SC)

The selection and hold (SAH-SC based on ARQ) has been studied and reported in the literature. In this scheme, the instantaneous SNR of the received signals with packets from the three branches is compared and selected the best one to the output. The received packet is checked for its correctness using CRC. If the packet is obtained as an erroneous, then duplicate copies will be retransmitted.

ARQ-POR-SC

The post-reception SC based on ARQ (ARQ-POR-SC) checks all the received copies and monitors the correctness of all the received copies. Selection is done based on the correct copies and if it fails to recover the original copy then discards the whole erroneous copies and requests for duplicate copies.

ELA-POR-SC

Liang et al., error location algorithm (ELA), the modified version of the SC based on ARQ has been studied. The scheme operates as follows: if any one of the received copies is correct, then it is accepted. However, if all the copies are erroneous then in order to get correct copy, it performed ELA-POR-SC. In this scheme, three copies are sent from transmitter to receiver. At least, one copy is found as correct then proceed for the next packet otherwise performing ELA-POR-SC. Let CP1, CP2 and CP3 are the three erroneous received copies of the same transmitted packet over the three diversity branches.

$$\mathrm{CP1CP1} = (\mathrm{CP1} \oplus \mathrm{CP3}).(\mathrm{CP1} \oplus \mathrm{CP2})$$
$$\mathrm{CP2CP2} = (\mathrm{CP1} \oplus \mathrm{CP2}).(\mathrm{CP2} \oplus \mathrm{CP3})$$
$$\mathrm{CP3CP3} = (\mathrm{CP1} \oplus \mathrm{CP3}).(\mathrm{CP2} \oplus \mathrm{CP3})$$

In CP1CP1, CP2CP2 and CP3CP3, every ‘1’ indicates an error in the copy of CP1, CP2 and CP3, respectively. In this case, the original packet can be retrieved by using

$$\begin{aligned}\mathrm{Original} &= \mathrm{CP1CP1} \oplus \mathrm{CP1}\ (= \mathrm{CP2CP2} \oplus \mathrm{CP2}\\ &= \mathrm{CP3CP3} \oplus \mathrm{CP3})\end{aligned}$$

However, the retrieval process fails when it is found as double, triple error and so on. In this time, erroneous copies are discarded and will request for next duplicate copies by sending NAK.

Packet Combining Scheme

Shyam Chakraborty suggested some modification based on SR-ARQ technique for enhancing the performance of BEC called extended ARQ (EARQ) also called packet combining scheme. This work is an extension technique of Sindhu [18]. Sindhu suggested the idea of locating the erroneous bit by XORed operation. However, in the conventional SRQ, the Rx normally discards the erroneous copies. But in the proposed scheme by Chakraborty, the Rx is used to buffer the erroneous copies and it requests for next copy by retransmission technique. If the requested copy is found correct, then buffered erroneous copy is discarded. If it is not found as correct copy, then XOR operation is performed to identify the erroneous bit location. If the output of the XOR is found as 1, then the erroneous bit is present. Thus, in order to obtain the correct copy the bit inversion of the bit (s) in error location (s) is done one after another followed by frame checking sequence (FCS). The throughput of the proposed protocol is given by the following Eq. (1)

$$v(\mathrm{Chakraborty}) = \frac{1}{1+P} \tag{1}$$

The protocol works only when there is single bit error (i.e., EARQ technique fails when double error occurs). The probability $P(i,\ j)$ that two copies with i, j errors, respectively, have a double error is given by Eq. (2)

Table 1 Modified packet combining scheme

Copies of erroneous pairs	Erroneous bits (y)	Erroneous detected position
[C-2 ⊕ C-1]	1 bit	6th position from MSB
[C-1 ⊕ C-3]	2 bits	5th and 7th positions from MSB
[C-3 ⊕ C-2]	3 bits	5,6 and 7th positions from MSB

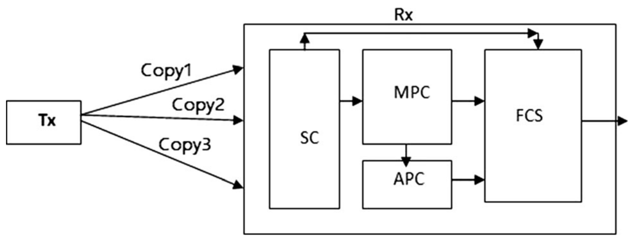

Fig. 3 Block diagram of proposed work

$$P(i,j) = 1 - \left[\frac{(n-i)!(n-j)!}{n!(n-i-j)!}\right] \quad (2)$$

The scheme is found suitable when the packet size is small and the limitation of the scheme is when the scheme is occurred at least same location of the erroneous copies.

The complexity of the bit inversion process to get correct copy is given by Eq. (3)

$$C = 2^{2n\alpha} - 2 \quad (3)$$

where α is the bit error rate and n is the packet size.

In order to avoid the complexity, it was suggested that when the number of 1's under XOR operation exceeds a certain number, Nmax, the pair is discarded and the retransmission is requested. In such cases,

$$P(i,j) = 1 - \left[\frac{(n-i)!(n-j)!}{n!(n-i-j)!}\right] \text{if } i+j \le N_{\max}$$
$$= 1 \text{ and if } i+j > N_{\max} \quad (4)$$

Modified Packet Combining Scheme

Further, modified packet combining scheme by Bhunia [20] has been carried out for performing higher error correction and also to enhance the error correction done by PC. In this technique, the Tx used to transmit i ($i > 1$) copies of the requested packet after getting NACK from Rx. The Rx on getting i duplicate copies can make a pair-wise XOR operation to locate the erroneous bit positions. Thus, if the Rx receives $i = 2$ copies then the Rx will have 3 copies. In this scheme, three erroneous copies are XORed in a pair. The identified bit error locations are put in ascending and then the first minimum erroneous bit is used to perform bit-by-bit inversion process followed by second and third; if failed then same technique will be repeated. The three erroneous copies are assumed as copy (C) C-1, C-2 and C-3 and then pair-wise XOR operation is carried out among (C-2 ⊕ C-1), (C-3 ⊕ C-2) and (C-1 ⊕ C-3) to locate the erroneous bit position.

Assume an original packet "11100111" and it is received as three erroneous copies as first erroneous copy, C-1 = 11101111, second erroneous copy, C-2 = 11101011 and third erroneous copy, C-3 = 11100101. The erroneous copies are performed XOR between C-2 ⊕ C-1 = 00000100, C-3 ⊕ C-2 = 00001110 and C-1 ⊕ C-3 = 00001010. The ascending orders based on common erroneous bit position are indicated by XOR operation which is clearly shown in Table 1. Thus, error correction will start from C-1 and if necessary then C-3 and followed by C-2. However, if the above process fails to recover the original copy then the same procedure will be repeated after discarding all the erroneous copies.

Proposed Work

The main objective of the proposed work is to achieve higher error correction capability and packet throughput over-conventional MPC and APC techniques. Thus, the proposed work derives the exact expressions for successful double or more error correction using the combined techniques of SC, MPC and APC techniques. The analysis is done with three erroneous copies and assuming that (a) frame synchronization is perfect (b) error are statistically independent and uniformly distributed and (c) frame checksum bits are transmitted without errors. The block diagram and flowchart of the proposed work is shown in Figs. 3, 4.

The combined SC + MPC + APC techniques using three paths are proposed in order to achieve higher error correction probability and packet throughput. In this case, the Tx sends the three copies of the same packet in three different paths where the paths are assumed as independent (i.e., disjoint paths). Using the concept of conventional SC, if the received copies check independently by frame checking sequence (FCS). If one of the copies is received correctly then the Rx will discard the other two copies and Rx will request for the next packet. If all the three copies are found as erroneous then MPC technique performs the following tasks to enhance the error correction after storing the received erroneous copies.

1. Let the three erroneous copies as CP_1^{err}, CP_2^{err}, and CP_3^{err} are buffered and pair-wised XOR operations are performed to find the bit error locations, i.e., $CP_1^{err} \oplus CP_2^{err} = X_1$ operation, $CP_2^{err} \oplus CP_3^{err} = Y_1$ operation, and $CP_3^{err} \oplus CP_1^{err} = Z_1$ operation. Thus, from the X_1,

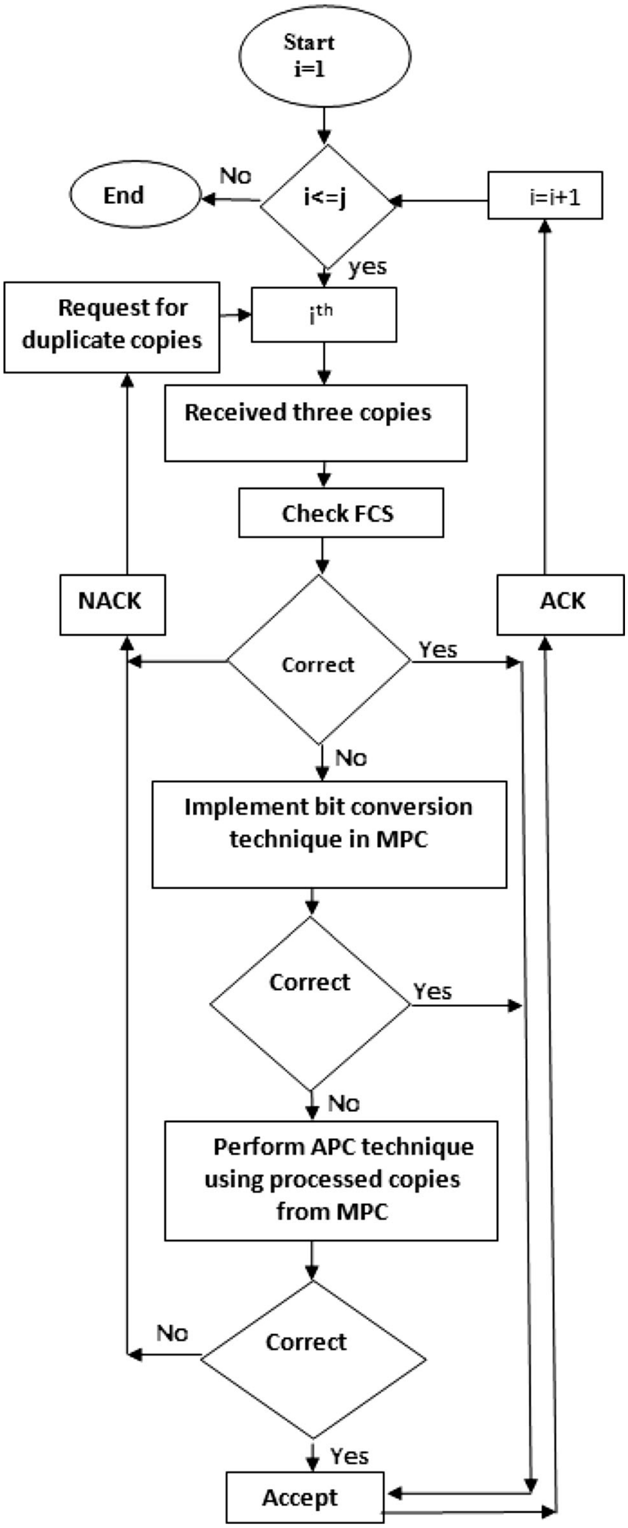

Fig. 4 Flowchart of the proposed work

Y_1, and Z_1 operations, the first, second, and third minimum erroneous bit locations are identified.

2. Let X_1, Y_1, and Z_1 be the first, second, and third minimum erroneous bit locations.

   (a) Firstly, from the X_1 operation the identified erroneous bit locations in CP_1^{err} are performed bit conversion technique (let X_2 operation) in such a way that if 0 then 1 or 1 then 0 but not both, i.e., if $1 \rightarrow 0 \text{but} 0 \rightarrow 0 \text{or if} 0 \rightarrow 1 \text{but} 1 \rightarrow 1$ and then paired-wise XOR will be performed with CP_2^{err} to identify the erroneous bit location and also to reduce the erroneous bit location as well. If all the resultant bits are found sequence of zeros and if it fails to recover the original copy after FCS then the X_3 operation will be performed. In X_3 operation, it also converts the identified erroneous bit location in CP_2^{err} in such a manner that if 0 then 1 or 1 then 0 but not both, i.e., if $1 \rightarrow 0 \text{but} 0 \rightarrow 0 \text{or if} 0 \rightarrow 1 \text{but} 1 \rightarrow 1$ and then pair-wise XOR will be performed between two processed or half-corrected erroneous copies from X_2 and X_3 operation. Similarly, if all the resultant copies are not found correct copy after FCS then the Y_2 and Y_3 operations will be performed.

   (b) Likewise in X operations, Y_2 operation is carried out from Y_1 operation but the bit conversion technique is applied to CP_2^{err} and then XOR operation will be performed with CP_3^{err}. Similarly, Y_3 operation will be performed but the bit conversion technique applies to CP_3^{err} and then XOR operation performs with half-corrected copy from Y_2 operation if the Y_2 operation fails to draw the original copy. If Y operations fail to recover the original copy then Z_2 and Z_3 operations will be performed with the same techniques of X and Y operations.

3. If the MPC block fails to obtain the original copy, then the half-corrected (erroneous copies) from X_2 or X_3, Y_2 or Y_3 and Z_2 or Z_3 operations will be performed the APC technique instead of CP_1^{err}, CP_2^{err}, and CP_3^{err} in conventional APC. The examples of the proposed scheme are shown below:

Examples of the Proposed Scheme

Example 1 Original copy, $O^r = 11111$

Let the three received erroneous copies are $CP_1^{err\text{-}} = \mathbf{0}1\mathbf{0}11$, $CP_2^{err} = \mathbf{0}11\mathbf{0}1$ and $CP_3^{err} = 1\mathbf{0}111$. Thus, the MPC technique is performed the pair-wised XOR operation to find the minimum erroneous bits location, i.e., X_1, Y_1 and Z_1 operations.

From X_1 operation:

$CP_1^{err} = 01011$
$CP_2^{err} = 01101$
. . ..$\oplus$
00110

From Y_1 operation:

$CP_2^{err} = 01101$
$CP_3^{err} = 10111$
. . ..$\oplus$
11010

Z_1 operation:

$CP_3^{err} = 10111$
$CP_1^{err} = 01011$
. . ..$\oplus$
11100

Firstly, the bit conversion technique of the proposed protocol is converted the erroneous bit location from the pair-wised XOR operation, i.e., starting from CP_1^{err} and then XOR operation is performed with CP_2^{err}.

01111
01101
. . ..$\oplus$
00010

Again, the bit conversion technique is implemented to CP_2^{err} and then pair-wise XOR operation is performed with the converted bit stream from CP_1^{err}.

01111
01111
. . ..$\oplus$

00000, the result is checked by FCS but failed to get original copy. Thus, it will continue the bit conversion technique from Y_1 operation, i.e., second minimum erroneous bit location

Secondly, the bit conversion technique is converted to CP_2^{err} and then XOR is performed with CP_3^{err}.

11111
10111
. . ..$\oplus$
01000

Again, the bit conversion technique is applied to CP_3^{err} and then pair-wised XOR is performed with the converted bits stream from CP_2^{err}, i.e.,

11111
11111
. . ..$\oplus$

00000, now it checks the FCS and it is obtained the original copy.

Example 2 **Original Copy, O^r = 10011**

Let the three received erroneous copies are CP_1^{err} = 11011, CP_2^{err} = 11001 and CP_3^{err} = 00000. Thus, X_1, Y_1 and Z_1 operations are performed to identify the first, second and third minimum erroneous bit locations.

From X_1 operation:

11011
11001
. . ..$\oplus$
00010

From Y_1 operation:

11001
00000
. . ..$\oplus$
11001

From Z_1 operation:

00000
11011
. . ..$\oplus$
11011

The minimum erroneous bit locations are identified, and therefore, the bit conversion method is applied to X_1 operation, i.e., CP_1^{err} and then CP_2^{err}.

11001
11001
. . ..$\oplus$

00000, no error is detected, and therefore, it checks for FCS and the output is failed to obtain the original copy. Thus, Y_1 operation will continue.

From Y_1 operation, the erroneous bit locations are identified, and therefore, the bit conversion method applies to CP_2^{err}.

00000
00000
. . ..$\oplus$

00000, no error is found. Thus after checking FCS, the output fails to obtain the original copy, and therefore, Z_1 operation will be continued.

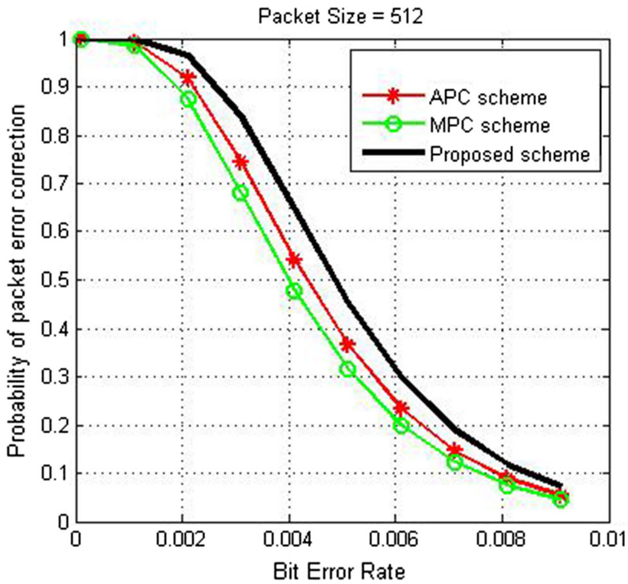

Fig. 5 Packet error correction probability with 512 bits packet size

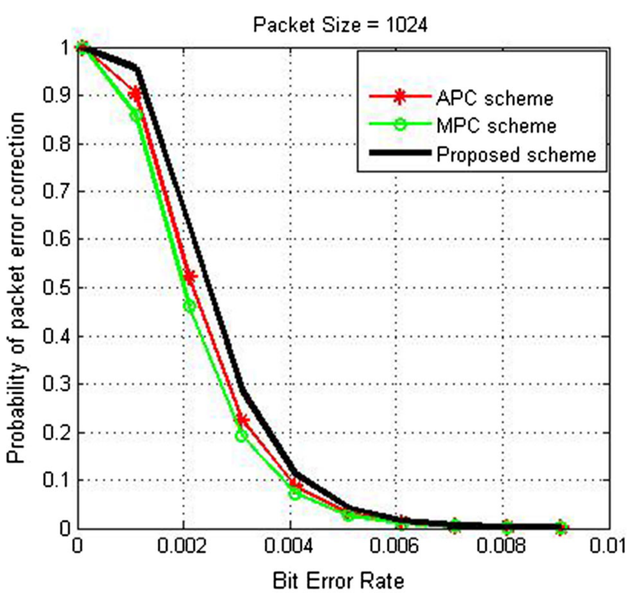

Fig. 6 Packet error correction probability with 1024 bits packet size

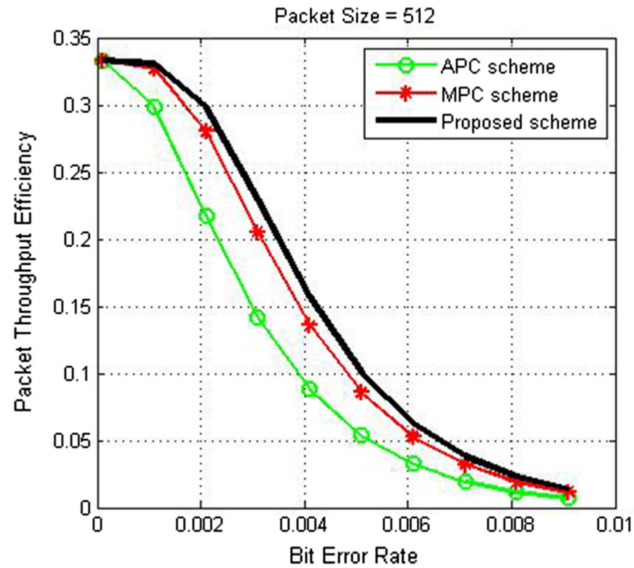

Fig. 7 Packet throughput efficiency with 512 bits packet size

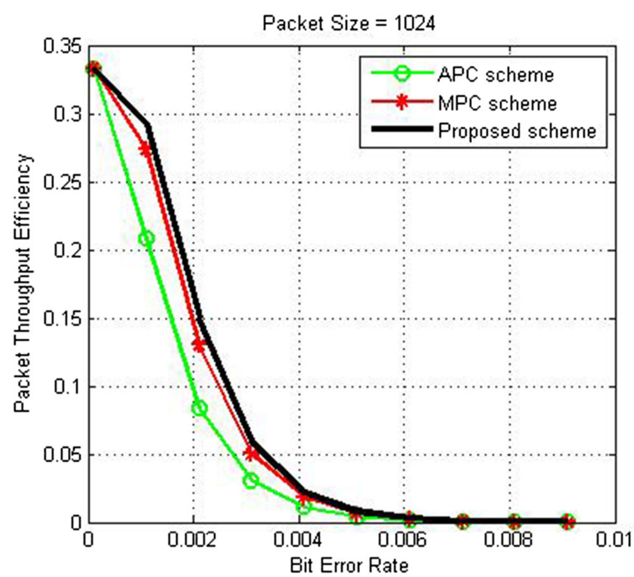

Fig. 8 Throughput efficiency with 1024 bits packet size

Similarly, from Z_1 operation, the erroneous bit locations are identified. Thus, bit conversion method will be applied to CP_3^{err} and then to CP_1^{err}.

10011

11011

$\ldots\ldots\ldots\oplus$

01000, still erroneous bit location is found, and therefore, bit conversion method applies to CP_1^{err}.

10011
10011
……..⊕

00000 no error is detected and thus it is checked for FCS. The output obtains original copy, i.e., 1011.

Numerical and Simulation Analysis

Let α be the probability of bit error rate and n is the size of the packet. If at least one of the copies is found correct from three branches using SC then the probability of obtaining the correct copy is given by Eq. (5)

$$\mathrm{PEC_{SC}} = 1 - [1 - (1 - \alpha)^n]^3 \quad (5)$$

The proposed work combines the three techniques, i.e., SC + MPC + APC techniques and if the proposed work performs error correction independently then the probability of getting at least one correct copy from the three techniques can be given by Eq. (6)

$$\mathrm{PEC_{SC+MPC+APC}} = \left[\frac{[(1-\mathrm{PE_{SC}}).\mathrm{PE_{MPC}}.\mathrm{PE_{APC}}].[(1-\mathrm{PE_{MPC}}).\mathrm{PE_{SC}}.\mathrm{PE_{APC}}].[(1-\mathrm{PE_{APC}}).\mathrm{PE_{SC}}.\mathrm{PE_{MPC}}]}{\mathrm{PE_{SC}}.\mathrm{PE_{MPC}}.\mathrm{PE_{APC}}}\right] \quad (6)$$

where $\mathrm{PE_{SC}}$ = Probability of packet error in SC technique, $\mathrm{PE_{MPC}}$ = Probability of packet error in MPC technique, $\mathrm{PE_{APC}}$ = Probability of packet error in APC technique.

The proposed protocol performs r number of pair-wise XOR operation from the received erroneous copies after SC technique failed to correct the original copy. Thus, Eq. (7) gives the probability of two corrupted copies which consist of k_i and k_j error bits $(i<j)$, where the erroneous bits are random and independent events [19].

$$p_{i,j}(h) = \left[1 - \frac{\sum_{k_i=1}^{n}\sum_{k_j=k_i}^{n-k_i}\binom{n}{k_i}\binom{n-k_i}{k_j}}{\sum_{k_i=1}^{n}\sum_{k_j=k_i}^{n}\binom{n}{k_i}\binom{n}{k_j}}\right] \quad (7)$$

Since, the occurrences of error bits in the corrupted packets are independent events. Thus, the proposed work provides the conditional probability h_r when the $\mathrm{CP_i^{err}}$, i = 1,2, and 3 arrives and performs 'r' pair-wise XOR operation at the receiver. Thus, h_r can be obtained by Eq. (8)

$$h_r = \left[\frac{\left[\sum_{k_1=1}^{n}\sum_{k_2=1}^{n}\cdots\sum_{k_r=1}^{n}p(k_1)p(k_2)\ldots p(k_r)\prod_{1\le i,j\le r}p_{i,j}(h)\right]}{[1-(1-\alpha)^n]^r\prod_{l=2}^{r-1}h_l}\right] \quad (8)$$

Again, the proposed protocol also performs an APC technique from the processed or half-corrected copies after MPC technique failed to obtain the original copy. Equation (9) gives the probability of packet error correction of the proposed protocol.

$$\mathrm{PEC_{prop}} = \left[1 - \sum_{i=1}^{r-1}p_i^{\mathrm{prop}}\right][(1-\alpha)^n + (1-(1-\alpha))^n.(1-h_r)].\left[1-[1-(1-\alpha)^n]^3.(1-h_r)\right].\mathrm{PEC_{SC}} \quad (9)$$

Thus, in order to compare the overall packet error probability of the proposed scheme and the conventional APC, the total packet error probability of the proposed scheme is given by the difference of the packet error probability of the conventional APC and the probability of the packet error correction of the proposed protocol.

$$\mathrm{PE_{pro}} = \mathrm{PE_{APC}} - \mathrm{PEC_{prop}} \quad (10)$$

where $\mathrm{PE_{APC}} = [1-(1-\alpha)^n] \times [1-(1-\alpha)^n] \times [1-(1-\alpha)^n] = [1-(1-\alpha)^n]^3$

The packet throughput efficiency [20–23] of the proposed protocol can be given by Eq. (11)

$$\lambda_{\mathrm{pro}} = \frac{1-\mathrm{PE_{pro}}}{3+\mathrm{PE_{pro}}} \quad (11)$$

The energy consumption is higher if the probability of packet error is higher. Therefore, the energy consumption (E) of the proposed scheme can be determined by Eq. (12)

$$E = \frac{1}{[1-\mathrm{PE_{pro}}]} \quad (12)$$

Conclusion

Several modifications of SC, PC, MPC and APC have been studied and reported in the literature, but the techniques were used to discard the erroneous copies without observing the processed erroneous copies. Thus, retransmission of duplicate copies is not encouraged in the data network as the retransmission of duplicate copies consumes extra communication energy. Therefore, the combined techniques of SC + MPC + APC are studied and then simulated in MATLAB in order to get lower retransmission of duplicate copies by getting higher error correction probability and packet throughput in the three branches diversity over conventional MPC and APC techniques. The proposed protocol can be obtained the original copy from the received erroneous copies by correcting two or more random errors using bit conversion technique with 'r' number of pair-wised XOR operation. Figures 5, 6 show the probability of packet error correction of the proposed scheme with the conventional MPC and APC techniques at 512 and 1024 bits packet size. Figures 7 and 8 obtain the packet throughput of the proposed scheme and

Table 2 The example of proposed scheme under APC technique with original copy, **O^r = 11111**

APC technique that uses the resultant copies, i.e., converted bit stream from MPC technique			
Majority voting of X_1, Y_1 and Z_1	Number of least reliable bits (l)	Number of searching correct bit patterns (2^l-1)	Output
01111	3	000	11111(correct copy)
11111		001	
00011		010	
……..		100	
01111(Not correct copy)		101	
		110	
		111	

Table 3 The example of conventional APC with original copy, **O^r = 11111**

Conventional APC scheme			
Majority voting of CP_1^{err} = 01011, CP_2^{err} = 01101, CP_3^{err} = 10111	Number of least reliable bits (l)	Number of searching correct bit pattern (2^l-1)	Output
01011	4	0000 1001	11111 (correct copy)
01101		0001 1010	
10111		0010 1011	
……..		0100 1100	
01111(Not correct copy)		0101 1101	
		0110 1110	
		0111 **1111**	
		1000	

Table 4 Proposed example of APC technique with original copy, **O^r = 10011**

APC technique that uses resultant copies of MPC, i.e., converted bit stream			
Majority voting of X_1, Y_1 and Z_1	Number of least reliable bits (l)	Number of searching correct bit patterns(2^l-1)	Output
11001	4	0000 1000	10011(correct copy)
00000		0001 1010	
10011		0010 **1011**	
……..		0110 1100	
10001		0101 1101	
		0110 1110	
		0111 1111	

Table 5 Example of conventional APC with original copy, **O^r = 10011**

Conventional APC scheme			
Majority voting of CP_1^{err} = 11011 CP_2^{err} = 11001 CP_3^{err} = 00000	Number of least reliable bits (l)	Number of searching correct bit patterns (2^l-1)	Output
11011	4	0000 0101 **1011**	10011(correct copy)
11001		0001 0110 1100	
00000		0010 0111 1110	
……..		0011 1000 1111	
11001		0100 1001	
		1010	

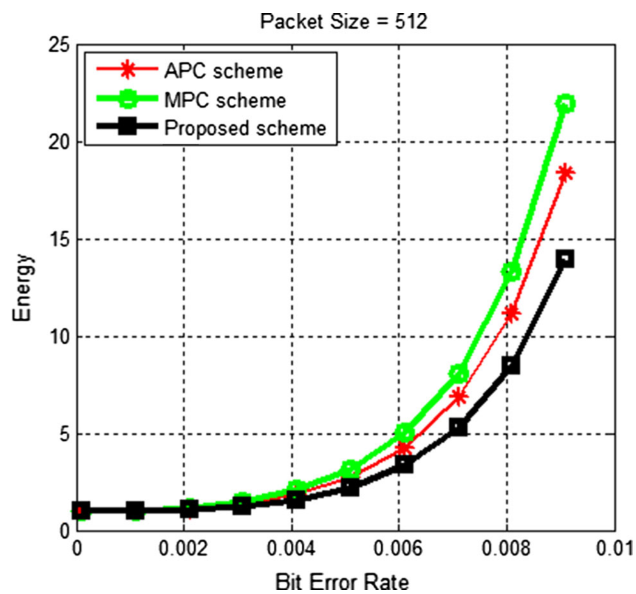

Fig. 9 Energy consumption with 512 bits packet size

show that the proposed scheme provides better result over the MPC and APC techniques at 512 and 1024 bits packet size. Tables 2, 3 and Tables 4, 5 show the comparative examples of the proposed scheme and conventional APC technique. The proposed technique can reduce the minimum average searching of correct bits pattern from 2^l-1 to $2^{l-i}-1$, where $i = 1,2,\ldots l$, it implies that at most l value can be reduced. Figures 9, 10 portray that energy consumption of the proposed work is lower than the conventional techniques of MPC and APC. Hence, the proposed scheme enhances the performance of conventional MPC and APC and consumes relatively less power as well.

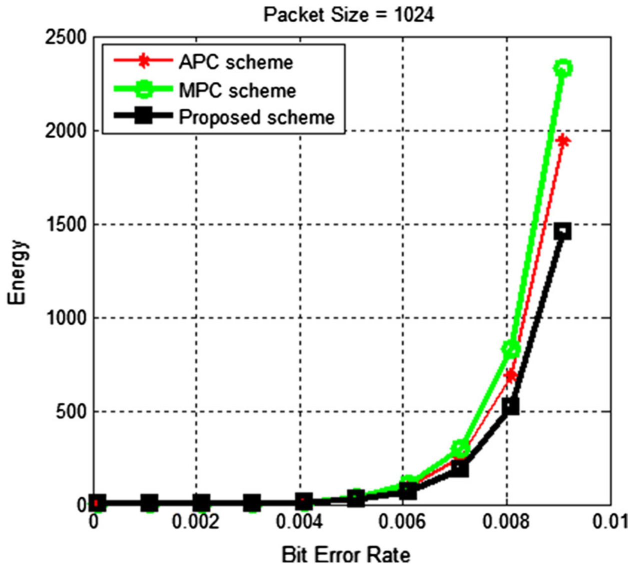

Fig. 10 Energy consumption with 1024 bits packet size

Acknowledgements I would like to thank “Visvesvaraya Ph. D Scheme”, Govt. of India to give us an opportunity to complete this paper with their financial support.

References

1. S.B. Wicker, Adaptive rate error control through the use of diverse combining and majority logic decoding in hybrid ARQ protocol. IEEE Trans. Commun. **39**(3), 380–385 (1991)
2. S.S. Chakraborty et al., An ARQ scheme with packet combining. IEEE Commun. Lett. **2**(7), 200–202 (1995)
3. S.S. Chakraborty et al., An exact analysis of an adaptive GBN scheme with sliding observation interval mechanism. IEEE Commun. Lett. **3**(5), 151–153 (1999)
4. S.S. Chakraborty et al., An adaptive ARQ scheme with packet combining for time varying channels. IEEE Commun. Lett. **3**(2), 52–54 (1999)
5. C.T. Bhunia, Modified packet combining scheme using error forecasting decoding to combat error in network. Proc IEEE Comput Soc **2**, 641–646 (2005)
6. Y. Liang, S.S. Chakraborty, ARQ and packet combining with post-reception selection diversity, in Proceedings of IEEE VTC’04, Los Angeles, CA (2004)
7. Y.-W. Leung, Aggressive packet combining for error control in wireless networks. IEICE Trans Commun **83**(2), 380–385 (2000)
8. C.T. Bhunia, A. Chowdhury, ARQ technique with variable number of copies in retransmission, in Proceedings of Conference on Computer Networking and Multimedia (COMNAM-2000), 21–22 December, Jadavpur University, Calcutta, India,16–21 (2000)
9. C.T. Bhunia, Packet reversed packet combining scheme, in Proceedings of IEEE Computer Society, CIT’07, Aizu University, Japan, pp 447–451 (2007)
10. C.T. Bhunia, Error forecasting schemes of error correction at receiver, in Proceedings of ITNG’2008, IEEE Computer Society, USA, pp. 332–336 (2008)
11. S. Ningthoujam, S.K. Chakraborty, C.T. Bhunia, New investigation of aggressive packet combining scheme to reduce transmission delay and three states markov model using multiple routes to Increase throughput. Int J Future Gener Commun Netw **8**(5), 157–166 (2015)
12. S.K. Chakraborty, R.S. Goswami, A. Bhunia, C.T. Bhunia, Investigation of two new protocols of aggressive packet combining in achieving Better throughput. J Inst Eng (India): Ser B **96**(2), 141–145 (2014)
13. S.K. Chakraborty, R.S. Goswami, A. Bhunia, C.T. Bhunia, Studies of several new modifications of aggressive packet combining to achieve higher throughput, based on error correction capability of disjoint error vectors. J Inst Eng (India) Ser B **97**(2), 269–272 (2015)
14. S. Ningthoujam, M.P. Dutta, S. Banerjee, C.T. Bhunia, S.K. Chakraborty, PC-APC schemes in multipath diversity system to get higher throughput. Int J Electr Comput Eng **7**(1), 337–343 (2017)
15. Y. Bulo, Y. Saring, C.T. Bhunia, APC-PC combined scheme in gilbert two state model: proposal and study. J Inst Eng (India): Ser B **98**(2), 239–243 (2016)
16. Y. Saring, Y. Bulo, C.T. Bhunia, Adaptive packet combining scheme in three state channel model. J Inst Eng (India): Ser B **99**(1), 1–6 (2018)
17. Y. Saring, S.V. Singh, Aggressive packet combining scheme with packet reversed and packet shifted copies for improved performance. IETE J Res **65**, 141–147 (2018)
18. P.S. Sindhu, Retransmission error control with memory. IEEE Trans. Commun. **COM-25**, 473–479 (1977)
19. S.-S. Wang, P.-C. Lee, K.-Y. Lin, T.-C. Yeh, A comparative study of packet combining based error recovery schemes for wireless network. Int. J. Ad Hoc Ubiquitous Comput. **16**, 183–191 (2014)
20. C.T. Bhunia, *Information Technology, Networks and Internet* (New Age International Publishers, New Delhi, 2005)
21. Y. Saring, S.V. Singh, Aggressive packet combining scheme with packet reversed and packet shifted copies for improved performance. IETE J Res **65**(2), 141–147 (2019)
22. S. Ningthoujam, S.K. Chakraborty, A Combined techniques of PC+ MPC+ APC to achieve higher error correction probability and throughput over APC and MPC techniques. Wirel Pers Communs **109**(3), 1–17 (2019)
23. S. Ningthoujam, S.K. Chakraborty, Analysis of the adaptive three-modes for PC+ MPC+ APC techniques using retransmission cyclemechanism. J High Speed Netw **25**(2), 205–220 (2019)