

Modified Aggressive Packet Combining Scheme with Repetition Code for Throughput Enhancement in High Error Rate Channel



Mancharla Ravi and Yaka Bulu

Abstract Aggressive packet combining (APC) scheme is a well-established scheme which reduces the number of retransmissions for receiving correct packet in error prone wireless link. It is a well-known fact that the retransmissions consume extra bandwidth and battery energy of the portable computer. Therefore, APC is an efficient technique which reduces number of retransmissions for a packet, thus reducing latency of the wireless system. In APC, three copies of a packet are transmitted, and receiver does bit-wise majority decision to get the combined copy. Least reliable bits identification is done in the combined packet if majority logic fails. Search the correct bit pattern for least reliable bits so obtained. APC provides higher reliability but at expense of throughput of the system. Therefore, major issue in APC is the lower throughput which at maximum is 33.33% ($\frac{1}{3} \times 100$). In this paper, modified APC with repetition code is proposed which addresses lower throughput issue of conventional APC. Simulation results show significant performance improvement in terms of throughput when packet combining scheme with repetition code is used in APC scheme.

Keywords Bit-by-bit majority logic · Bit error rate · Conventional aggressive packet combining scheme · Repetition code · Throughput

1 Introduction

The wireless networks suffer from high bit error rate 10^{-2} [1] to 10^{-3} [2]. In an automatic repeat request (ARQ) scheme, a packet is retransmitted if it gets corrupted due to transmission errors caused by the channel. Each retransmissions consume communication bandwidth and transmission energy. The bandwidth is a scarce resource

M. Ravi (✉) · Y. Bulu
Department of Electronics and Communication Engineering, National Institute of Technology
Arunachal Pradesh, Arunachal Pradesh, India
e-mail: Mancharla.phd@nitap.ac.in

Y. Bulu
e-mail: yaka@nitap.ac.in

because many portable computers may be sharing a limited free space spectrum. The energy is also a scarce resource because the portable computer is usually powered by battery.

Therefore, it is desirable to reduce the number of retransmissions in order to utilize the bandwidth and battery energy efficiently. In many error control protocols, the receiver discards the erroneous packet and requests the transmitter for a retransmission. However, an erroneous packet may contain both erroneous bits and correct bits, and hence, it may still contain useful information. The receiver may be able to combine this information from multiple erroneous copies to recover the correct packet. In order to achieve the desirable quality in high bit error rate wireless channels, several modifications for applying basic ARQ are found in literature where erroneous packets are combined and by applying logic, the error location is identified. Once error location is identified, bit inversion is done to error so identified (Brute method). The technique is variably applied in packet combining scheme [3], multiple route packet combining scheme [4], and aggressive packet combining scheme [5]. In packet combining scheme [3, 6, 7], two copies of a packet are transmitted, and if at least one of the received copies are error free, it is accepted as a correct transmission. However, if both copies are received erroneous, bit-wise modulo-2 sum of the copies is computed to locate the errors in the combined copy. Thereafter, the packet is corrected by brute force bit-by-bit inversion of bit located as erroneous and checking for correctness using frame check sequence (FCS). However, PC scheme fails if there is at least one-bit position where both copies have an error (termed as double error in [3]), and the computational complexity increases when the number of errors in the combined copy exceeds a predefined value N_{\max} [3]. To deal with the latency issue in wireless network, Leung [5] proposed an efficient technique called aggressive packet combining scheme. In aggressive packet combining scheme, transmitter sends three copies of packet to the receiver. Receiver on receiving three copies of the packet will apply bit-by-bit majority voting on three received copies to obtain a combined packet. Receiver checks error on the combined packet, and if the packet is not corrected by majority logic, receiver will identify least reliable bits and search the correct bit pattern for the identified least reliable bits. If still correct copy is not obtained, it will request for retransmission of the packet. APC gives better error correction capability [8–14] with reduced latency, but suffers from low throughput. APC scheme requires at least three copies of a packet to successfully retrieve the correct copy of the packet, thus the best packet throughput of APC scheme is $T_{\text{APC}} = \frac{1}{3} \times 100\% = 33.33\%$ only.

In this article, we propose a modified technique of APC which increase the throughput of the conventional APC using the idea of packet combining and three-bit repetition code. We use the concept of packet combining scheme for incorrectly received copies to identify the error locations and then use three-bit repetition code when the retransmission call is received at the receiver side. We assume that the round-trip delay is negligible, the feedback channel is error free, and CRC provides perfect error detection capability.

2 Proposed Scheme

In proposed technique, instead of transmitting three copies of the original packet as in conventional APC, two copies are sent initially. If the received two copies are erroneous, then XORing of both the copies are done to locate the error positions as that of the conventional packet combining scheme. Bit-by-bit inversion of the error positions which is done in conventional PC is avoided because this step involves computational complexity which is equal to $C = 2^{2n\alpha} - 2$ [3] where n is packet size in bits and α is bit error rate. Thus, even for medium-sized packets and at moderate BER, random fluctuations of the channel may make the bit inversion procedure extremely complex. It also leads to battery energy consumption and delay of the system (as delay is not acceptable in real-time traffic). Conventional APC is an efficient technique with low latency, but it suffers from low throughput. Therefore, this proposal is an attempt to increase the throughput of conventional APC. It is observed that current wireless mesh network protocols retransmit whole of the packet when a retransmission call is received at the sender side [8]. These retransmissions end up sending bits that have already received correctly, wasting network capacity. Retransmitting entire packets work well over wired networks where bit-level corruption is rare and packet loss implies that all the bits of the packet were lost. However, in case of wireless network, all the bits in a packet do not share the same fate. Thus, it is wasteful to resend the entire packet. Therefore, in the proposed technique, instead of retransmitting entire packet when negative acknowledgement (NACK) is received, sender sends only that bits which are erroneous by using basic three-bit repetition code. After XORing, receiver sends NACK along with errored bit positions information to the sender and keeping the errored copies at its buffer. At the sender side, instead of retransmitting the whole packet, it sends only those bits which are detected to be error by repeating each bit three times. Receiver applies bit-by-bit majority logic in the third erroneous copy, and again error detection is done on the code obtained after majority logic. Incorrect positions are rectified by comparing the bits obtained after majority logic with those erroneous bit locations in any of the first two received copies. Flow diagram of the proposed scheme assuming return channel to be error free, the round-trip delay is negligible, and CRC used at the receiver provides perfect error detection with example is shown in Fig. 1. In Fig. 1, $P1_C1$ is the copy 1 of packet 1, and $P1_C2$ stands for copy 2 of packet 1. $P1_Repetition_code$ stands for retransmitted packet with three-bit repetition code.

In the proposed scheme, aggregate number of bits transmitted is lesser than the conventional APC, so the throughput improvement is very high as compared to the conventional APC. It gives satisfactory results when the packet is medium and large sized.

Majority logic applied in the transmitted packet is successful if no two bits out of three repetition code is error. Generally, codeword to have two bits flipped out of three bits, the medium would have to be extremely noisy of the order of 10^{-3} to 10^{-2} [1, 2]. And practically, channel does not happen to be extremely noisy all the

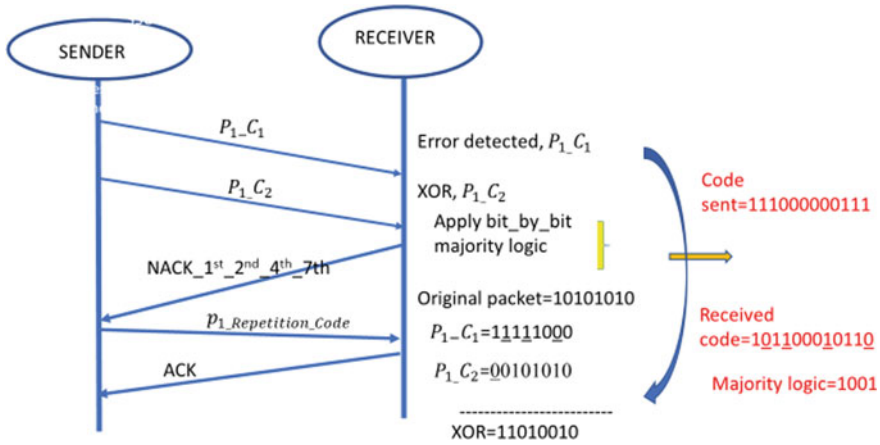


Fig. 1 Flow diagram of the proposed APC scheme with the bit repetition code

time. To understand the proposed scheme clearly, let us take an example showing proposed scheme.

An example showing proposed scheme for the packet $b_7b_6b_5b_4b_3b_2b_1b_0 = 11001100$

$$\text{Received copy, } b_7b_6b_5\bar{b}_4b_3b_2b_1b_0 = 110\bar{1}1100$$

$$\text{Received copy, } b_7\bar{b}_6b_4b_5b_3b_2\bar{b}_6b_0 = 1\bar{0}0011\bar{1}0$$

$$\text{XOR} = 01010010$$

The incorrect positions are identified as second, fourth, and seventh bit locations from the left. Receiver now sends NACK along with this errored bit positions information to the sender. Sender sends three-bit repetition code of this errored positions as 111 000 000. In receiver side, if the received code is $1\bar{0}1\bar{1}00\bar{0}00$. Apply majority logic, we get code as 100, and this code is sent for error detection. If found correct, receiver checks correct packet using this code in one of the erroneous copies stored in buffer of the receiver.

Error detection is done to check the packet.

3 Analysis and Simulation Results

In conventional APC scheme, three copies ($i = 3$) of a packet is transmitted at a time to get reliable packet at the receiver and the actual bit error rate, ϵ (as then only double or triple bits in error cannot be detected leading to actual bit error rate) for APC is given by ζ [9]:

$$\zeta = \binom{3}{2}\alpha^2(1 - \alpha) + \binom{3}{3}\alpha^3 \quad (1)$$

Therefore, probability of erroneous transmission (P_{APC}) or packet error rate (PER) in conventional APC for packet size “ n ” is given by [9]:

$$P_{APC} = (1 - (1 - \zeta)^n) \quad (2)$$

where “ α ” is bit error rate and ζ is the actual bit error rate. Throughput of the conventional APC is given by η_{APC} [15]:

$$\begin{aligned} \eta_{APC} &= \frac{(1 - P_{APC})}{(i + P_{APC})} \\ \eta_{APC} &= \frac{(1 - P_{APC})}{(3 + P_{APC})} \end{aligned} \quad (3)$$

where “ i ” is the number of copies transmitted.

In the proposed scheme, initially two copies are transmitted. At the receiver side, error detection is performed. If both the copies found erroneous, bit-wise modulo-2 sum is applied to find the error locations. Once error locations are identified, NACK is sent along with error location information. Therefore, probability of erroneous transmission P_{PC} for the first two copies assuming no double error occurs is given by [16]:

$$\begin{aligned} P_{PC} &= (1 - (1 - \alpha)^{ni}) \\ P_{PC} &= (1 - (1 - \alpha)^{2n}) \end{aligned} \quad (4)$$

Since two copies are transmitted in the first go therefore, $i = 2$.

For the third copy with three-bit repetition code, if any of the retransmitted bits cannot be recovered that is the case when two or all the three bits are erroneous. Therefore, bit(s) which cannot be recovered is written as β :

$$\beta = \alpha^3 + {}^3C_2\alpha^2(1 - \alpha) = \alpha^3 + 3\alpha^2 - 3\alpha^3 = 3\alpha^2 - 2\alpha^3 \quad (5)$$

Therefore, packet which is recoverable is given as ϕ :

$$\phi = 1 - \beta = 1 - (3\alpha^2 - 2\alpha^3) = 1 - 3\alpha^2 + 2\alpha^3 \quad (6)$$

Therefore, packet of k bits in error which are recoverable

$$= (1 - 3\alpha^2 + 2\alpha^3)^k \quad (7)$$

Probability of erroneous transmission for the proposed scheme P_{New} is given by:

$$P_{New} = P_{PC} \times [(1 - 3\alpha^2 + 2\alpha^3)^k] \quad (8)$$

Therefore, throughput of the proposed scheme is given by η_{New} :

$$\eta_{\text{New}} = \frac{(1 - P_{\text{New}})}{(i + P_{\text{New}})}$$

$$\eta_{\text{New}} = \frac{(1 - P_{\text{New}})}{[(2 + 3k) + P_{\text{New}}]} \quad (9)$$

Performance evaluation is done in terms of packet error rate (PER) and packet throughput, as determined by the computer simulation using MATLAB R2012b tool. Bit error rate (α) in the range 10^{-5} to 10^{-3} (low error rate) and 10^{-3} to 10^{-2} (high error rate) is taken for different values of bits in error (k) for comparison. Simulation results show the effectiveness of the proposed scheme in terms of throughput improvement for large-sized packet ($n = 1000$). But PER is almost same as that of the conventional APC as observed from simulation results in Fig. 4.

Figures 2 and 3 show that the throughput of the proposed scheme increases with change of bit error rate from low-to-high bit error rate, and this increment is more for large-sized packet. Throughput of the conventional APC decreases with increase in bit error rate. Not much improvement can be observed in terms of packet error rate (P) in the proposed scheme as shown in Figs. 4 and 5. It becomes worst when the packet size and bit error rate increase as chances of more number of bits getting corrupted increase in wireless links.

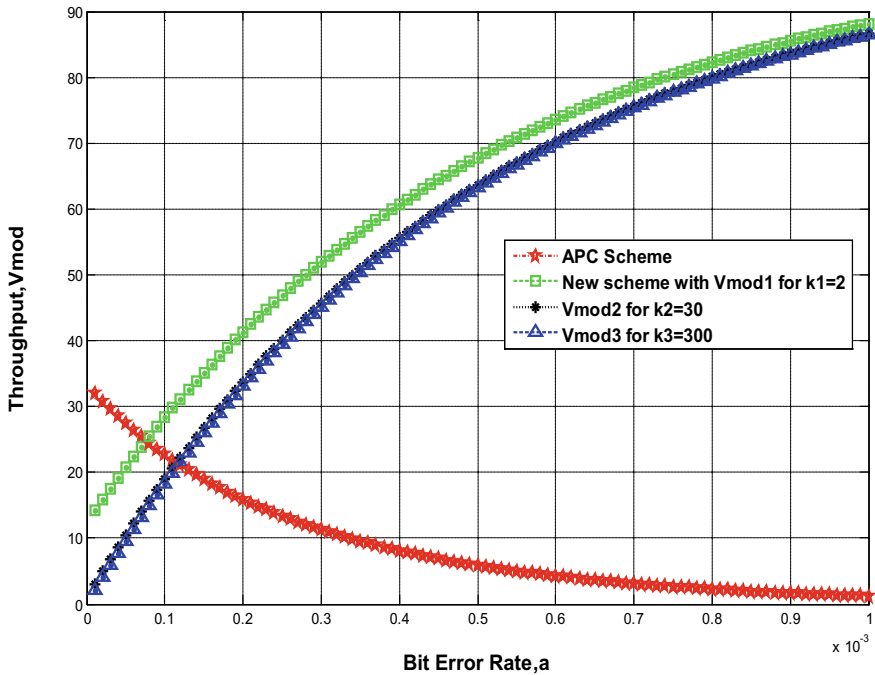


Fig. 2 Throughput plot of the proposed scheme for different values of k and APC scheme for $n = 1000$

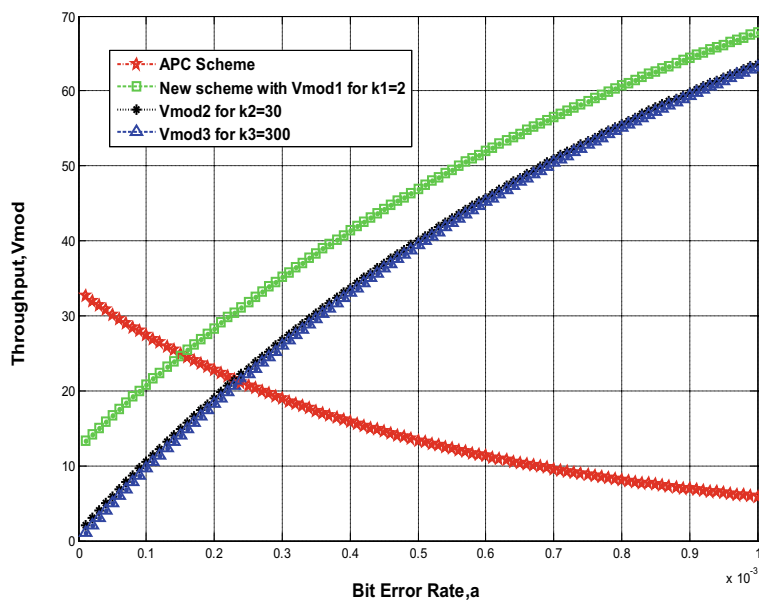


Fig. 3 Throughput plot of the proposed scheme for different values of k and APC scheme for $n = 500$

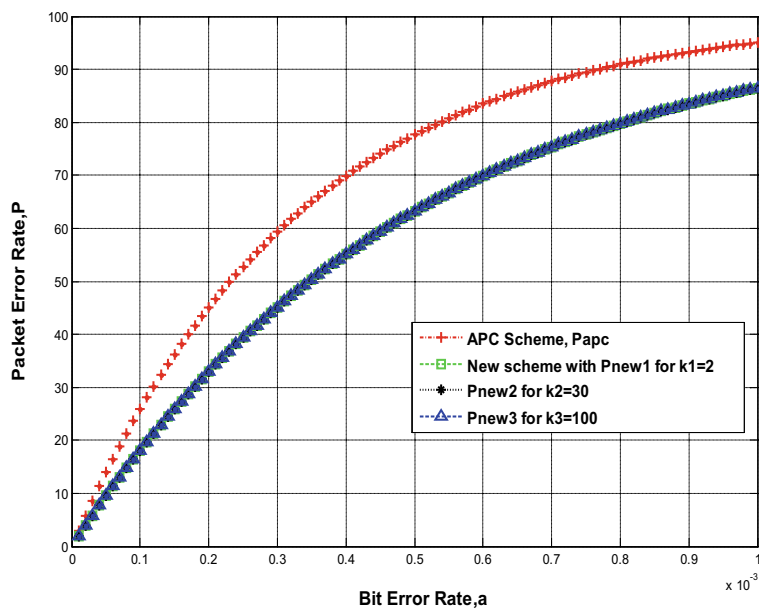


Fig. 4 Packet error rate plot for proposed scheme for different values of k and APC scheme for $n = 1000$

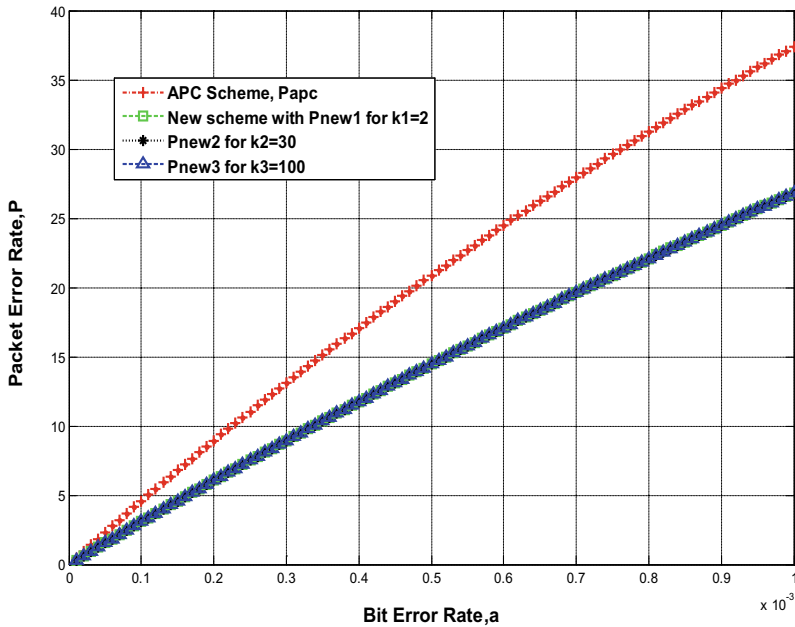


Fig. 5 Packet error rate plot for proposed scheme for different values of k and APC scheme for $n = 156$

4 Conclusion

The proposed scheme of bit repetition yields higher throughput as compared to APC scheme. Increment in throughput is prominent when the packet size and bit error rate increases as seen from Figs. 1 and 2. Not much improvement can be observed in terms of packet error rate (P) in the proposed scheme as shown in Figs. 3 and 4. It becomes worst when the packet size and bit error rate increase as chances of more number of bits getting corrupted increase in wireless links. The proposed scheme fails when double error occurs in the first two transmitted copies and two bits out of three transmitted repeated code get corrupted. Generally, codeword to have two bits flipped out of three bits, the medium would have to be extremely noisy of the order of 10^{-3} to 10^{-2} [1, 2]. And practically, channel does not happen to be extremely noisy all the time.

References

1. Liu H, Ma H, Zarki ME, Gupta S (1997) Error control schemes for networks: an overview. *Mob Netw Appl* 2:167–182
2. Yuen O (1996) Design trade-offs in cellular/PCS systems. *IEEE Comm Mag* 34(9):146–152

3. Chakraborty SS, et al (1995) An ARQ scheme with packet combining. *IEEE Comm Lett* 2(7):200–202
4. Hirayama Y, Okada H, Yamazato T, Katayama M (2005) Time-dependent analysis of the multiple-route packet combining scheme in wireless multihop network. *Int J Wirel Inf Netw* 42(1):35–44
5. Leung YW (2000) Aggressive packet combining for error control in wireless networks. *Trans Comm E83(2)*:380–385
6. Chakraborty SS, et al (1999) An exact analysis of an adaptive GBN scheme with sliding observation interval mechanism. *IEEE Comm Lett* 3(5):151–153
7. Chakraborty SS, et al (1999) An adaptive ARQ scheme with packet combining for time varying channels. *IEEE Comm Lett* 3(2):52–54
8. Jamieson K, Balakrishnan H (2007) PPR: partial packet recovery for wireless networks. *SIGCOMM'07*, Kyoto, Japan
9. Bhunia CT (2012) Several modifications of aggressive packet combining scheme for wireless network. In: *Proceedings of the IEEE computer, information and telecommunication systems (CITS)*, pp 1–5
10. Saring Y, Bulo Y, Bhunia CT (2015) New modifications of aggressive packet combining scheme with improved performance. *Int J Appl Eng Res* 10(17):37610–37615
11. Khumukcham R, Goswami A, Saring Y (2015) Four new protocols for achieving better correction capability of APC scheme. In: *Proceeding IEEE international conference of communication and signal processing*, Melmaruvathur, Tamil Nadu, pp 741–745
12. Khumukcham R, Saring Y, Goswami A (2015) Combined APC-PC scheme for random and time varying channels. In: *Proceeding IEEE international conference of communication and signal processing*, Melmaruvathur, Tamil Nadu, pp 358–360
13. Bulo Y, Sharma P, Bhunia CT (2016) Improving error correction capability of aggressive packet combining scheme by using half-byte packet reverse technique and even–odd selection method. *Int J Comput Appl* 137(2):32–36
14. Saring Y, Singh SV (2019) Aggressive packet combining scheme with packet reversed and packet shifted copies for improved performance. *IETE J Res*
15. Bhunia CT (2005) *IT, network and internet*. New Age International Publishers India, New Delhi
16. Chakraborty SS, Liinaharja M, Ruttik K (2002) Selection diversity based ARQ schemes and their enhancements using packet combining in a slow rayleigh fading channel. *IEEE ICPWC* 192–195