

## Lab 8: MOSFET Transistor Current-Voltage Characteristics

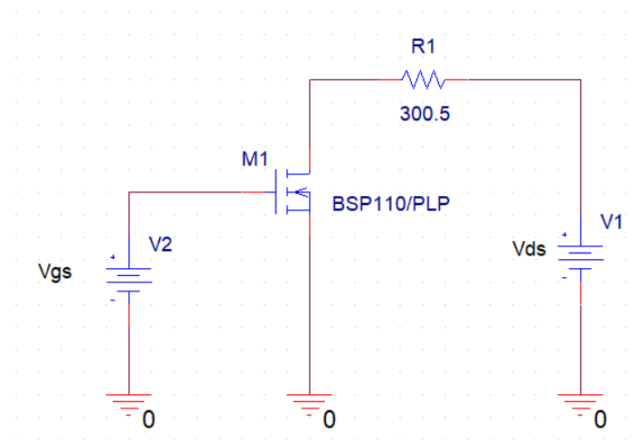
### Executive Summary:

The single MOSFET transistor circuit shown in the schematic below was constructed using the PSpice software. The circuit has the source of the transistor connected to ground, the gate connected to a voltage source, and the drain connected to a resistor in series with another voltage source. Two separate simulations were performed on the circuit. First, the voltage source at the gate was swept from 0.0V to 3.0V in .1V increments. The voltage source at the drain was kept at a constant 10V. The drain current ( $I_D$ ) was measured and plotted against the gate-source voltage ( $V_{GS}$ ). From this data, the threshold voltage of the MOSFET transistor ( $V_{TH}$ ) was determined to be 1.8V. In a second simulation, the voltage source at the gate was held constant at a value equal to  $V_{TH} + .01\text{ V}$  (1.9V). Meanwhile, the voltage source at the drain was swept from 0V to 10V in .1V increments. The drain current,  $I_D$ , was measured and plotted against the drain-source voltage ( $V_{DS}$ ).

### Objective:

To study the multiple modes of operations for a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and the relationship between measurements in each mode.

### Schematic:



MOSFET Analysis Schematic

Data:

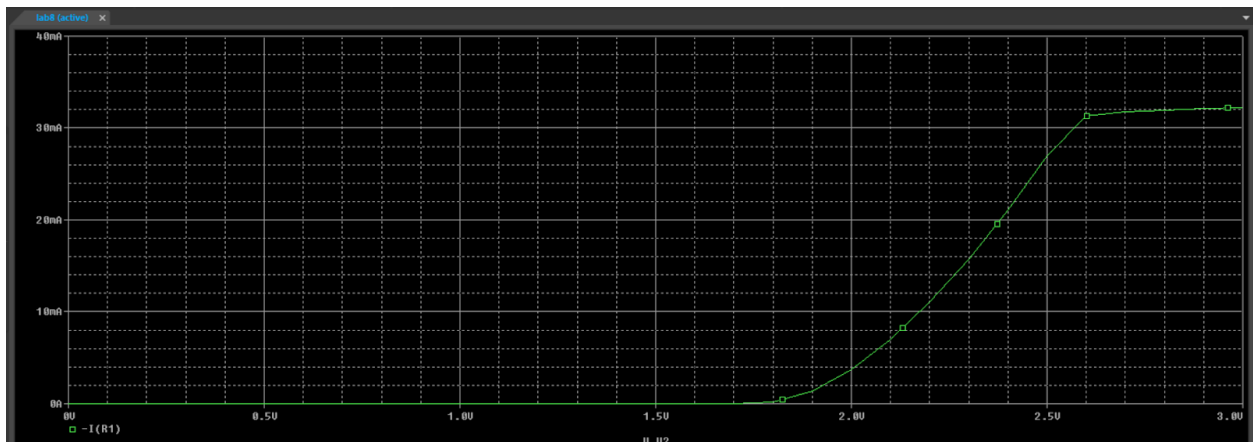


Figure 1 -  $I_D$  vs. Voltage Source at Gate =  $V_{GS}$  (Simulation 1)

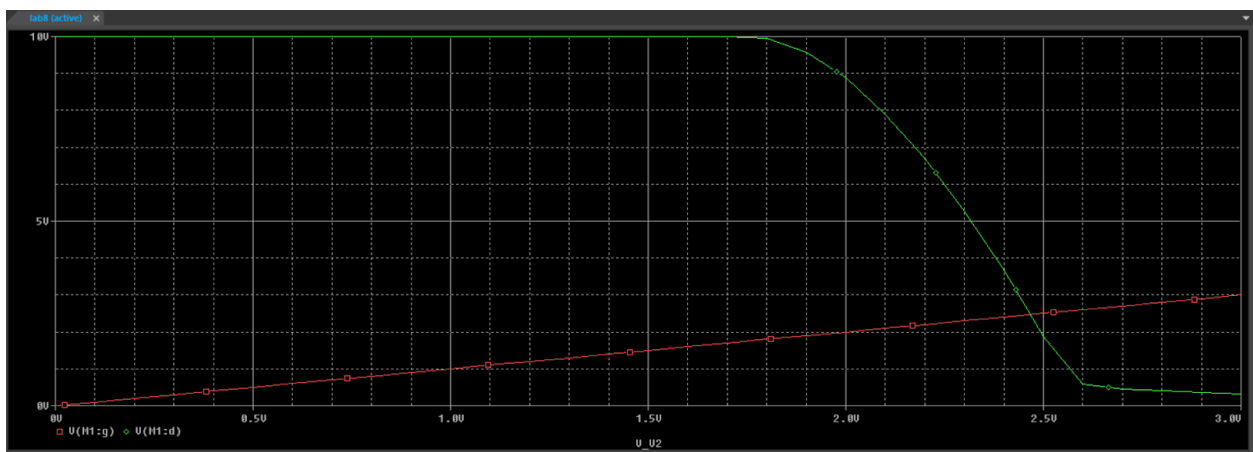


Figure 2 -  $V_{DS}$  (Green) and  $V_{GS}$  (Red) vs. Voltage Source at Gate =  $V_{GS}$  (Simulation 1)

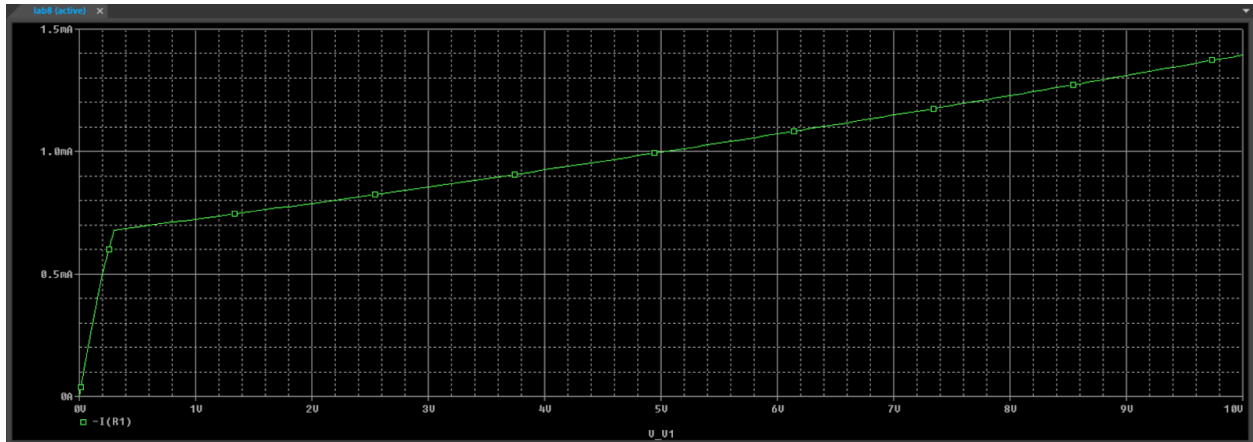


Figure 3 -  $I_D$  vs. Voltage Source at Drain (Simulation 2)

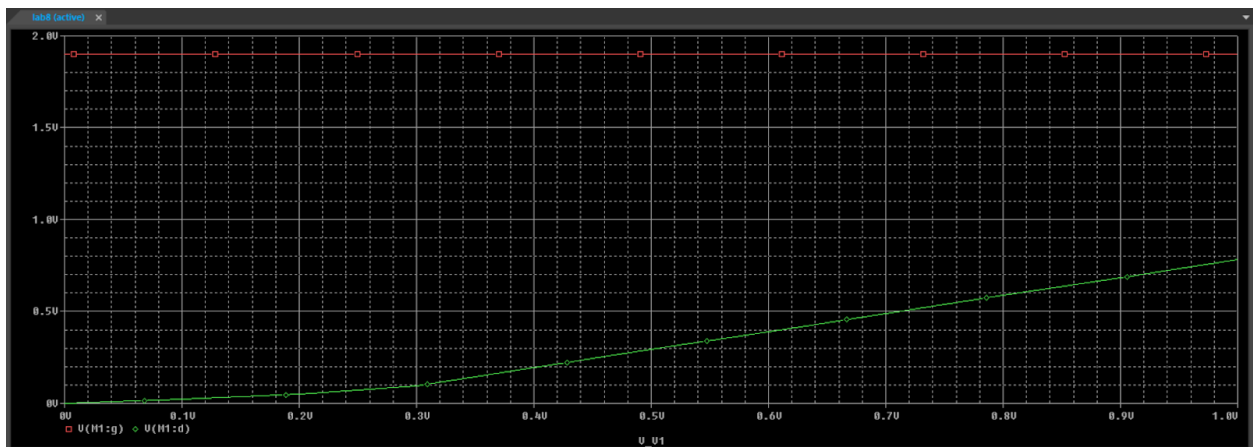


Figure 4 -  $V_{DS}$  (Green) and  $V_{GS}$  (Red) vs. Voltage Source at Drain (Simulation 2)

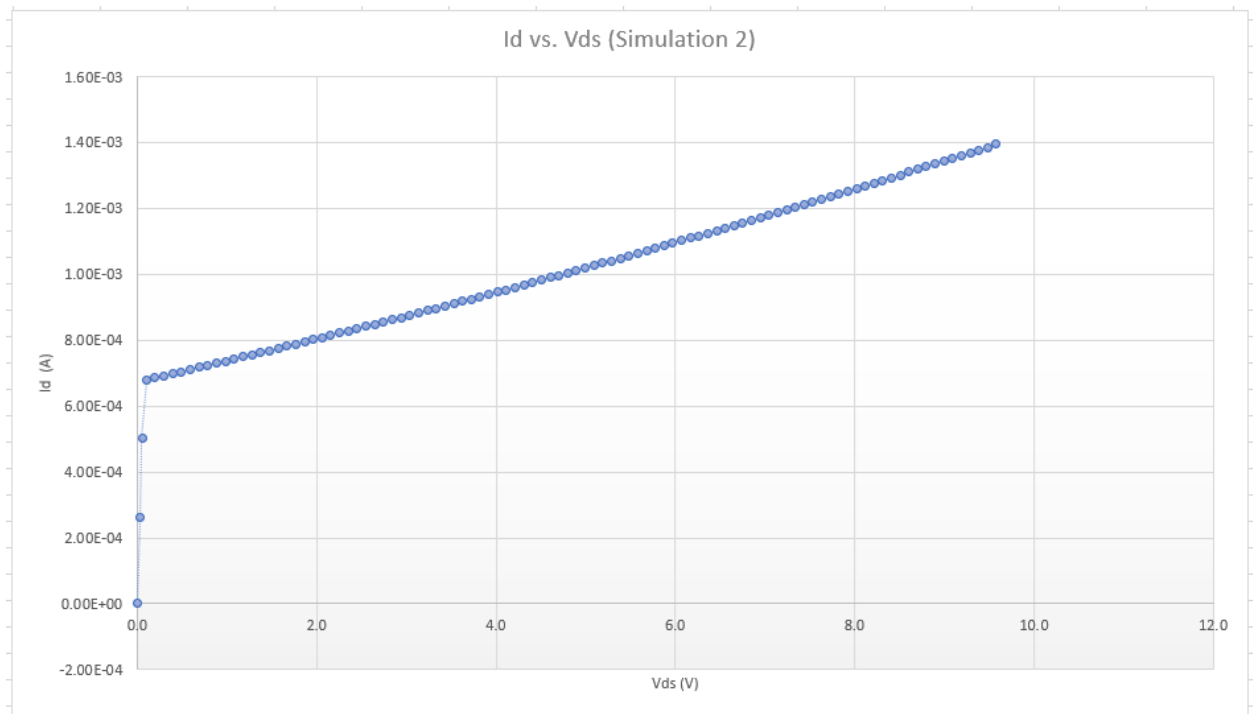


Figure 5 -  $I_D$  vs.  $V_{DS}$  (Simulation 2)

**Analysis:**

A MOSFET can operate in one of three modes. These modes are linear triode, saturation, and cutoff. The mode of the MOSFET is dependent on  $V_{GS}$ ,  $V_{DS}$  and  $V_{TH}$  following these expressions:

$$\text{Cutoff: } V_{GS} \leq V_{TH}$$

$$\text{Linear: } V_{GS} > V_{TH}, V_{DS} \leq V_{GS} - V_{TH}$$

$$\text{Saturation: } V_{GS} > V_{TH}, V_{DS} > V_{GS} - V_{TH}$$

In each of these modes, the  $I_{DS}$  is calculated as follows

$$\text{Cutoff: } I_{DS} = 0$$

$$\text{Linear: } I_{DS} = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}](1 + \lambda V_{DS})$$

$$\text{Saturation: } I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

In the first simulation of the circuit,  $V_{GS}$  was increased from 0V to 3V. When  $V_{GS}$  was in the range of 0V - 1.8V, the simulation results show that  $I_{DS}$  is equal to 0. This indicates the MOSFET was in cutoff.

Once  $V_{GS}$  becomes greater than 1.8V,  $I_{DS}$  exhibits quadratic growth (Figure 1). Saturation is the only mode for which there is a  $V_{GS}$  component squared in its  $I_{DS}$  equation. Since  $V_{GS}$  is the only variable in this simulation, we can conclude that the quadratic growth indicates saturation mode.  $V_{GS} > V_{TH}$  is the defining inequality in saturation so we can also conclude that  $V_{TH}$  is equal to 1.8V. This is a characteristic value of the transistor.

While  $I_{DS}$  increases quadratically,  $V_{DS}$  decreases due to Ohm's Law.  $V_{GS}$  is increasing in the simulation so there will be a point where  $V_{GS}$  will be greater than  $V_{DS}$  by a value of  $1.8V = V_{TH}$ . This would cause the MOSFET to go into linear mode. According to the data, this happens at around  $V_{GS} = 2.6V$  (Figure 2). In linear mode,  $V_{GS}$  and  $I_{DS}$  have a linear relationship which is why after 2.6V,  $I_{DS}$  increase at a linear rate rather than a quadratic rate (Figure 1).

In the second simulation,  $V_{GS}$  was set to  $V_{TH} + .1V = 1.9V$ . This is to assure that the MOSFET will not be in cutoff mode. In this second simulation, the voltage source at the drain is being increased from 0V to 10V. Since,  $V_{DS}$  starts at 0V and  $V_{GS}$  is at a constant 1.9V, the MOSFET starts off in linear mode ( $V_{GS} > V_{TH}$ ,  $V_{DS} \leq V_{GS} - V_{TH}$  is satisfied). The voltage increase of the source causes  $V_{DS}$  to increase as well. It will not take long for  $V_{DS}$  to increase to a point where it satisfies the inequality  $V_{DS} > V_{GS} - V_{TH} = .1V$ , causing it to go into saturation mode. Figure 4 shows that this will happen when the voltage source is at around .3V. This is when the MOSFET goes from linear to saturation mode. Figure 3 reflects this change in mode as well. After .3V,  $I_{DS}$  increases linearly with respect to the voltage increase. Before .3V  $I_{DS}$  increased at a much faster rate, which is in fact cubic growth. This again is due to the  $I_{DS}$  equations above. Since  $V_{DS}$  is the only variable in the second simulation,  $I_{DS}$  is directly influenced by it. When in linear mode, the equation for  $I_{DS}$  has a  $V_{DS}^3$  term (factored in equation above). When in saturation mode, the equation has only a single  $V_{DS}$  term. This is why Figure 3 exhibits the behavior it does. Figure 5 shows the same behavior as Figure 3 because  $V_{DS}$  is only slightly offset from the drain voltage source. The shape of the Figure is the same but the change from one mode to another is at a different x-value voltage (around  $V_{DS} = .1V$ ).