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ECE3200L-01

Lab 11:
NMOS Logic Inverter Amplifier with Enhancement Transistor Load

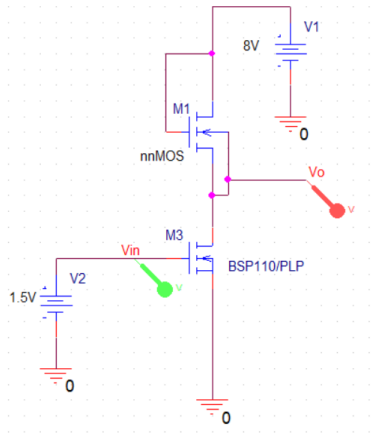
Executive Summary:

The NMOS logic inverter amplifier consists of two NMOS transistors. One of the transistors performs as the driver and the other as the load. For this lab, a VN0106 transistor is used as the driver and a CD4007 transistor as the enhancement load. The gate of the driver transistor is connected to the voltage source, its source to ground and its drain to the output. The load transistor has its source connected to the output and both its drain and gate connected to an 8V voltage supply. A coupling capacitor and resistor are added at the output when performing AC analysis. The input voltage was increased incrementally to find the bias point at which the change in output voltage was maximized. This voltage gain was then verified using AC analysis at that particular bias point. The peak voltage gain found from the DC analysis was -13.045 at a 2.0V input voltage. Using AC analysis, the gain at a 2.0V bias and .05V amplitude sinusoidal signal at 1000 Hz was -14.3 with a 1kΩ load and -19.7 without a load. The output impedance of the circuit was measured to be around 377Ω .

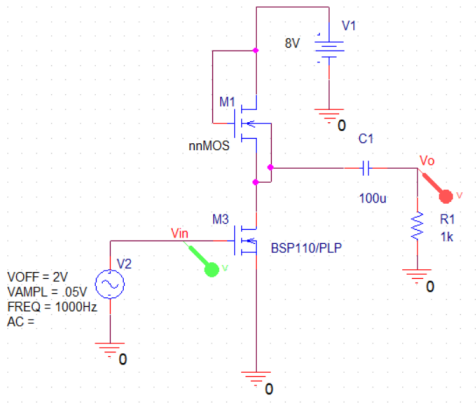
Objective:

The objectives of this experiment are: (a) to study the NMOS logic inverter circuit with enhancement mode NMOS transistor as its load (instead of a resistor); (b) and to show that this same circuit can be operated as an amplifier if it is biased to operate in the linear region of the input-output voltage transfer characteristic curve.

Schematics:

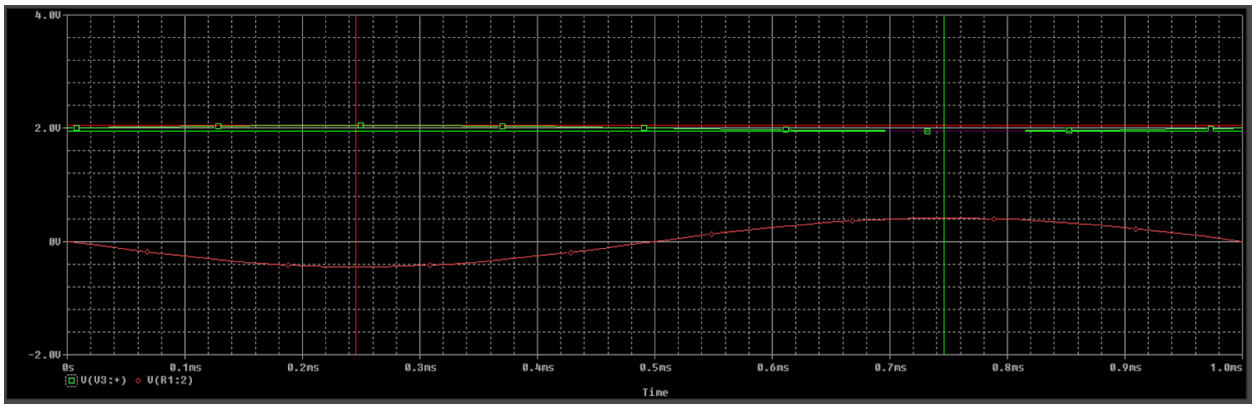


DC Analysis Schematic of NMOS Inverter



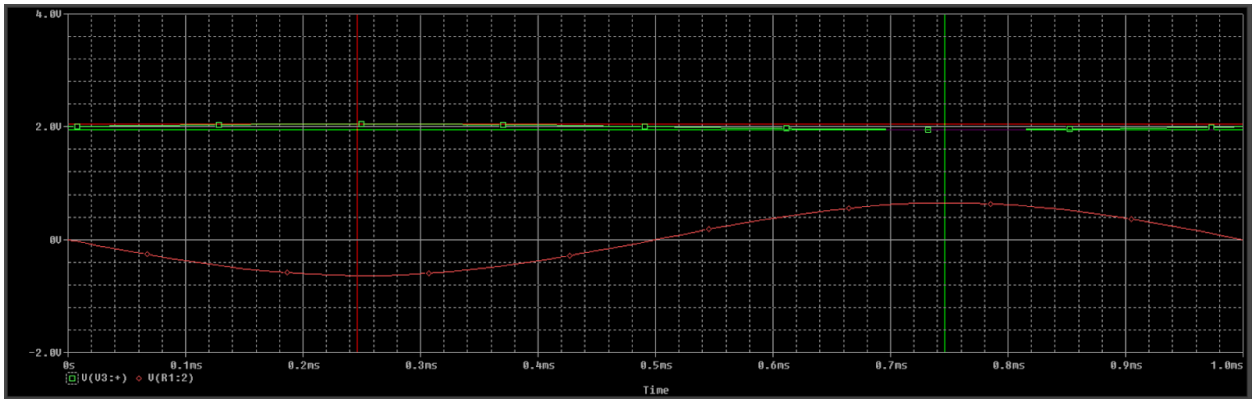
AC Analysis Schematic of NMOS Inverter

Data:



Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		99.951m		
	X Values	245.390u	746.099u	-500.709u	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(V3:+)	2.0500	1.9500	99.951m	0.000	0.000	2.0500	1.9500	2.0000
	V(R1:2)	-451.284m	410.417m	-861.701m	-2.5013	-1.5396	410.417m	-451.284m	-20.434m

Figure 1 - AC Analysis Vout with Load



Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		99.952m		
	X Values	246.099u	746.099u	-500.000u	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(V3:+)	2.0500	1.9500	99.952m	0.000	0.000	2.0500	1.9500	2.0000
	V(R1:2)	-637.284m	650.239m	-1.2875	-2.6873	-1.2998	650.239m	-637.284m	6.4774m

Figure 2 - AC Analysis Vout without Load

DC Voltage Measurements for NMOS Logic Inverter		
Vin (V)	PSPICE Vout (V)	Lab Measured Vout (V)
0	6.5979	6.747
1	6.5979	6.742
1.1	6.5979	6.73
1.2	6.5979	6.7
1.3	6.5979	6.653
1.4	6.5979	6.546
1.5	6.5979	6.418
1.6	6.5979	6.162
1.7	6.5979	5.743
1.8	6.1593	4.983
1.9	4.7858	3.8925
2	3.4701	2.3741
2.1	2.207	0.37656
2.2	0.991678	0.15473
2.3	0.304164	0.10188
2.4	0.230342	0.08035
2.5	0.192981	0.06772
2.6	0.168959	0.05856
2.7	0.151812	0.05137
2.8	0.13832	0.04632
2.9	0.12864	0.04279
3	0.120418	0.03956

Figure 3 - DC Voltage Measurements for NMOS Logic Inverter

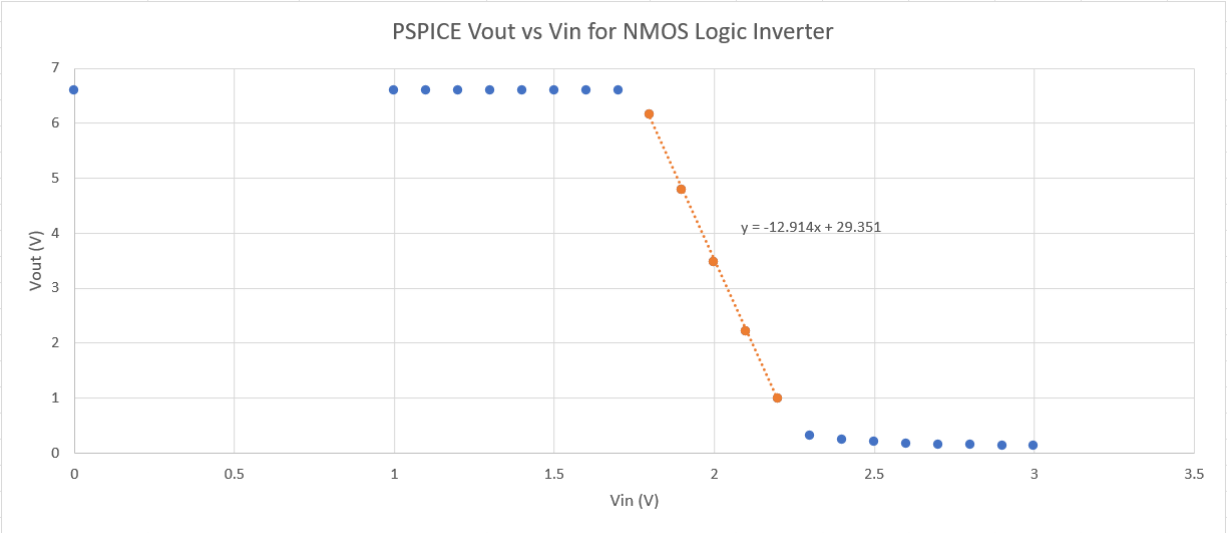


Figure 4 - PSPICE Vout vs Vin

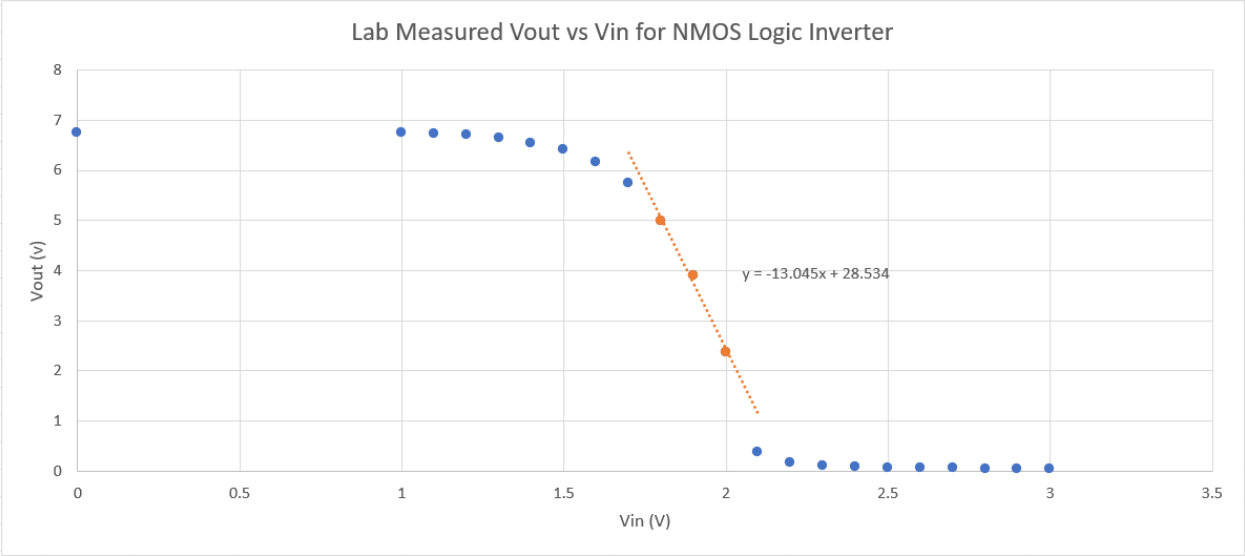


Figure 5 - Lab Vout vs Vin

PSPICE vs Lab Measured Data and Percent Errors			
	PSPICE	Lab Measured	Percent Error (%)
Gain from Slope	-12.914	-13.045	-1.004216175
Vout with No Load (V)	1.286	1.97	34.72081218
Vout with Load (V)	0.859649	1.43	39.88468531
Gain at Vbias with Load	-8.59649	-14.3	-39.88468531
Gain at Vbias without Load	-12.86	-19.7	-34.72081218
Ro (Ω)	495.9593974	377.6223776	31.33739597

Figure 6 - PSPICE vs Lab Percent Errors

Analysis:

Since the load transistor has its drain and gate connected, $V_{GS} = V_{DS}$. This means that the transistor could only operate in either cutoff or saturation as V_{DS} could never be more than $V_{GS} - V_{TN}$. This is important because in saturation, there is a linear relationship between the voltage across the transistor (V_{DS}) and the current through the transistor (I_D), allowing it to act as a load. The driver transistor of the logic inverter is connected as a common source amplifier with the drain resistor replaced by the enhancement load transistor. The output impedance of a common source amplifier would be equivalent to R_D. This corresponds to the impedance of the load transistor as seen from its source.The output impedance measured for the circuit was around 377Ω.

The DC analysis results shown in Figure 4 and Figure 5 demonstrate the change in modes of operation for the driver MOSFET. When the input voltage (V_{GS}) begins to increase from 0, it is initially less than V_{TN}. This corresponds to the cutoff region of the MOSFET and the current flowing through the drain will be 0. Modeling the load transistor as a resistor, the output voltage will then be given as $V_o = V_{DD} - I_D R_L$. For the case of cutoff the output voltage will be $V_o = V_{DD} - (0)R_L = V_{DD}$. As the input voltage continues to increase, V_{GS} will surpass V_{TN} slightly which will transition the transistor into saturation mode. The equation for drain current in saturation mode is given as $I_D = K_n(V_{GS} - V_{TN})^2$. Now the output voltage will be given as $V_o = V_{DD} - K_n(V_{in} - V_{TN})^2 R_L$. While in this region, the output voltage (V_{DS}) will decrease as a function of ${V_{in}}^2$. It does not take a large increase in input voltage for $V_{in} - V_{TN}$ to then surpass V_{DS}. When this happens, the MOSFET will now be in its non-saturation region where drain current is given as $I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$. The corresponding output voltage will be

$V_o = V_{DD} - K_n R_D[2(V_{in} - V_{TN})V_o - V_o^2]$. Out of these three modes of operation, the magnitude of V_o/V_{in} (slope) is maximized in saturation. Saturation corresponds to the transition region in Figures 4 & 5.

This DC behavior of the NMOS logic inverter is well represented by the PSPICE simulation. The input voltage which produced the steepest slope on the V_o vs. V_{in} graph was around 2V in the PSPICE simulation and around 1.8V in the lab. The slopes at these voltages representing the gain, were -12.914 in the PSPICE simulation and -13.045 in the lab. This corresponds to a percent error of -1%. DC voltages are more simple to model and there is less room for real world errors in the DC domain.

The AC behavior of the NMOS logic inverter however, varied more from the PSPICE simulation. When a 1kHz, 50mV AC signal was applied to the circuit at a 1.8V offset, the measured corresponding gain in the lab was -19.7. With a 1kΩ output load resistor, the gain dropped to around -14.3. In PSPICE, the gain was -12.86 with the load and -8.59 without one. The amplifier provides an inverted signal because as voltage across the gate-source terminals increases, the drain current increases as well. The increase in drain current will increase the voltage drop across the load resistor which will lower the output voltage. This is the underlying behavior behind a typical common source amplifier circuit.

The percent errors between the simulation and lab results are more present in the AC analysis. Some possible reasons for this could be the noise in the signal which affects AC signals more significantly, more variables for error sources (frequency, phase, etc.), and the introduction of outside coupling capacitors which are not present in DC analysis. The percent error for the AC analysis were all around the 30-40% indicating a systematic error, perhaps coming from the real world transistor/PSPICE model distinctions.