Chapter 3 :: Sequential Logic Design (1)

***Digital Design and Computer Architecture*, 2nd Edition**

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참고도서 : 개정판 논리회로 설계(김종현저) , 홍릉과학출판사.

- 제7장 순차회로의 분석과 설계

Chapter 3 :: Topics

- Introduction
- Latches and Flip-Flops

- Synchronous Logic Design
- Finite State Machines
- Shifter
- Timing of Sequential Logic
- Parallelism

3.1 Introduction

- Outputs of sequential logic depend on current *and* prior input values.
- Sequential logic thus has memory.

- Some definitions:
  - State(상태): contains all the information about a circuit necessary to explain its future behavior
  - Latches and flip-flops: state elements that store one bit of state
  - Synchronous sequential circuits(동기순자회로): combinational logic followed by a bank of flip-flops

Sequential Circuits

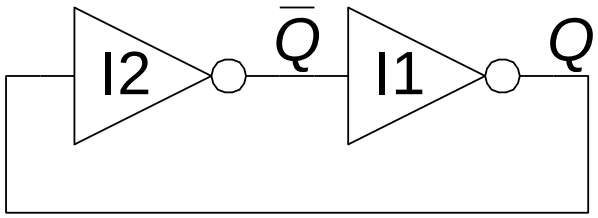
- give sequence to events
- have memory (short-term)
- use feedback from output to input to store information

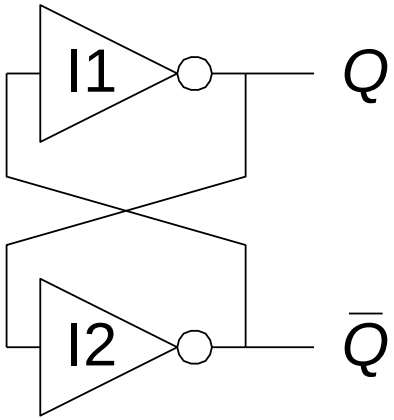
State Elements

- The state of a circuit determines its future behavior
- State elements store state
  - Bistable circuit
  - SR Latch
  - D Latch
  - D Flip-flop

3.2 Bistable Circuit

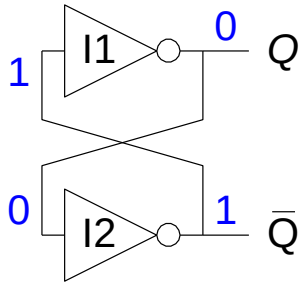
- Fundamental building block of other state elements
- Two outputs: Q, $\overline{Q}$
- No inputs



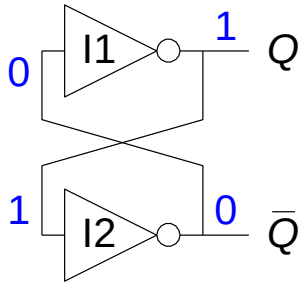


Bistable Circuit Analysis

- Consider the two possible cases:
  - $Q = 0$: then $\overline{Q} = 1$ and $Q = 0$ (consistent)



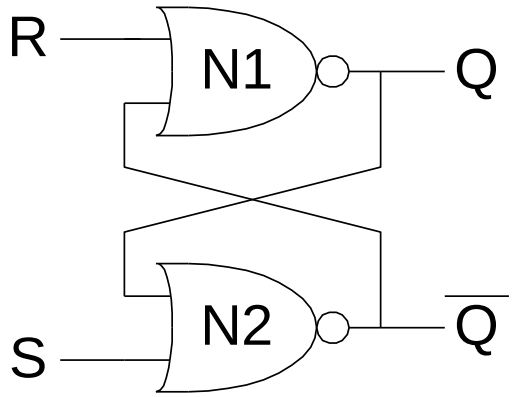
  - $Q = 1$: then $\overline{Q} = 0$ and $Q = 1$ (consistent)

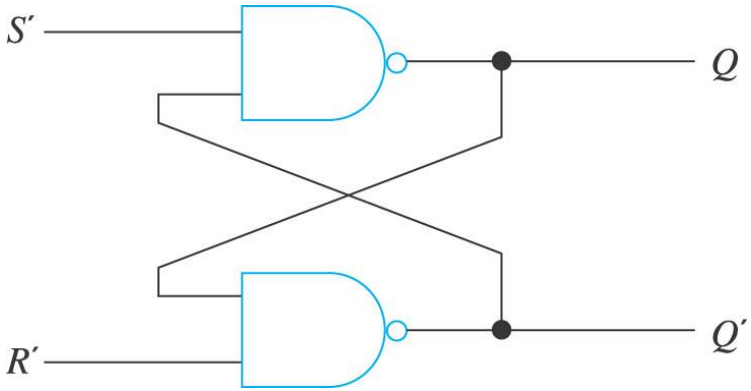


- Bistable circuit stores 1 bit of state in the state variable, Q (or $\overline{Q}$)
- But there are no inputs to control the state

3.2.1 SR Latch

- 두 개의 안정된 상태 값들(0과 1) 중의 하나를 기억(저장)하는 회로
  - 입력 단자: *S* (set), *R* (reset)
  - 출력 단자: *Q* (정상 출력), *Q′* (반전된 출력)
    <유의 사항: *Q* 와 *Q′* 은 보수 관계>

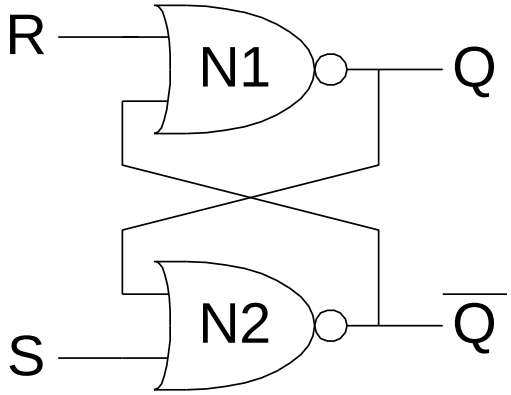




3.2.1 SR Latch

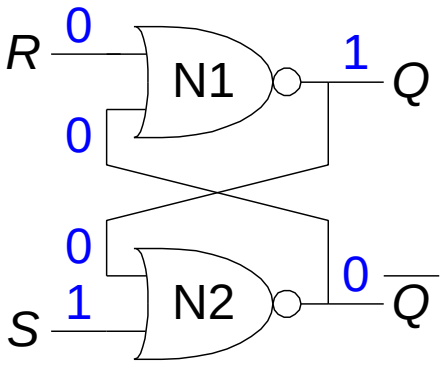
- Set/Reset Latch (SR Latch)
- Definitions
  - Set: Make the output 1
  - Reset: Make the output 0
- When the set input, *S*, is 1 (and *R* = 0), *Q* is set to 1
- When the reset input, *R*, is 1 (and *S* = 0), *Q* is reset to 0

- Consider the four possible cases:
  - ***S* = 1, *R* = 0**
  - ***S* = 0, *R* = 1**
  - ***S* = 0, *R* = 0**
  - ***S* = 1, *R* = 1**

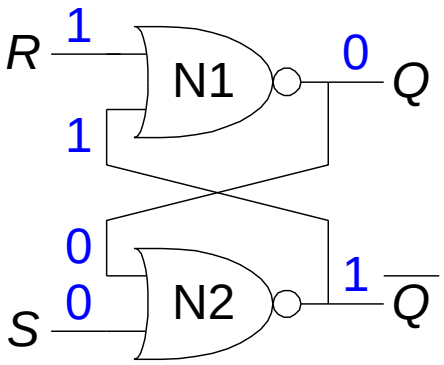


SR Latch Analysis

– $S = 1, R = 0$: then $Q = 1$ and $\overline{Q} = 0$



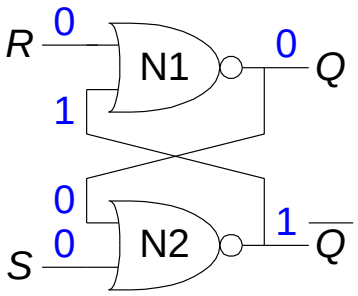
– $S = 0, R = 1$: then $Q = 0$ and $\overline{Q} = 1$



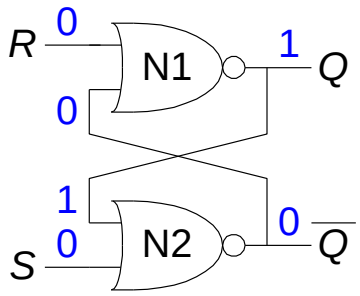
SR Latch Analysis

– $S = 0, R = 0$: then $Q = Q_{prev}$ and $\overline{Q} = \overline{Q_{prev}}$ (memory!)

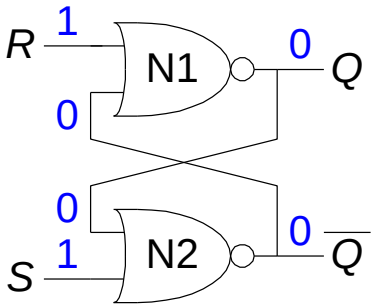
$Q_{prev} = 0$



$Q_{prev} = 1$

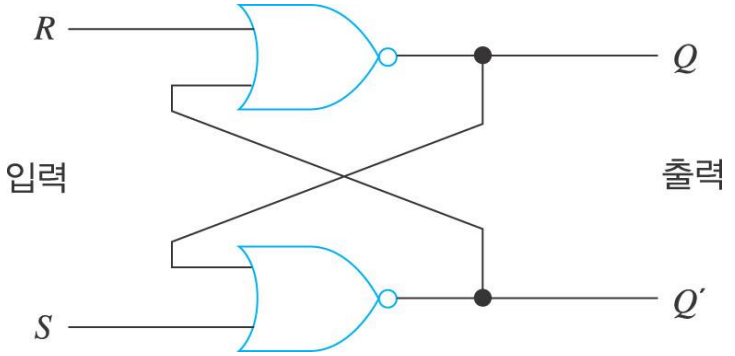


– $S = 1, R = 1$: then $Q = 0$ and $\overline{Q} = 0$ (invalid state: $\overline{Q} \neq$ NOT Q)

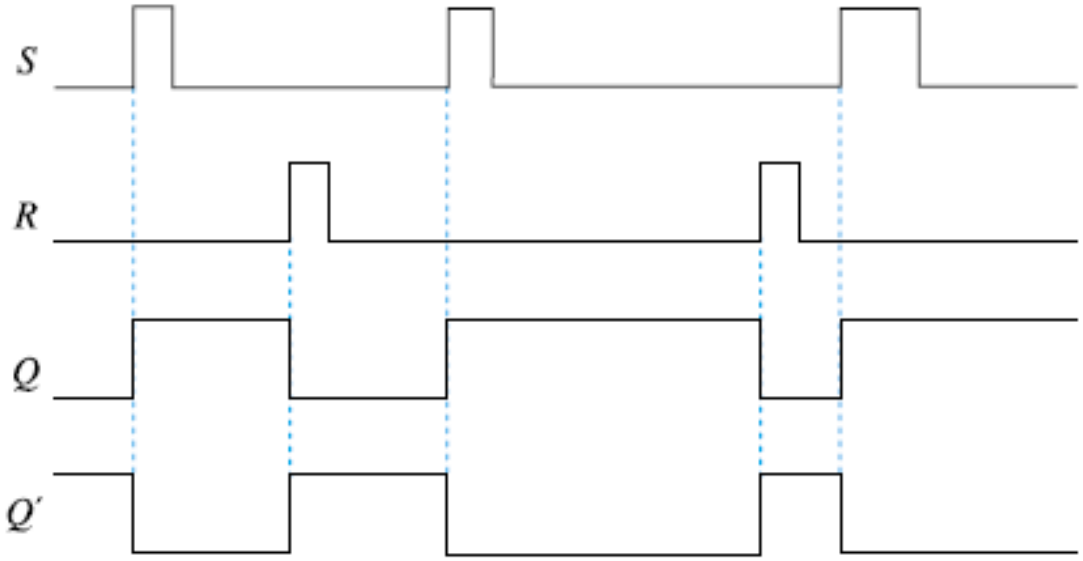


SR Latch Analysis

S	R	Q	Q'	
0	0	0	1	(초기값)
1	0	1	0	(세트 상태)
0	0	1	0	(불변)
0	1	0	1	(리셋 상태)
0	0	0	1	(불변)
1	1	0	0	(비정상)



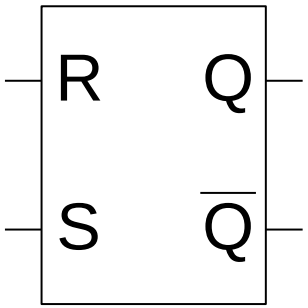
(b) 진리표



SR Latch Symbol

- Stores one bit of state (Q)
- Can control what value is being stored with S, R inputs
  - Invalid state when $S = R = 1$
  - Set: Make the output 1
    ($S = 1, R = 0, Q = 1$)
  - Reset: Make the output 0
    ($S = 0, R = 1, Q = 0$)

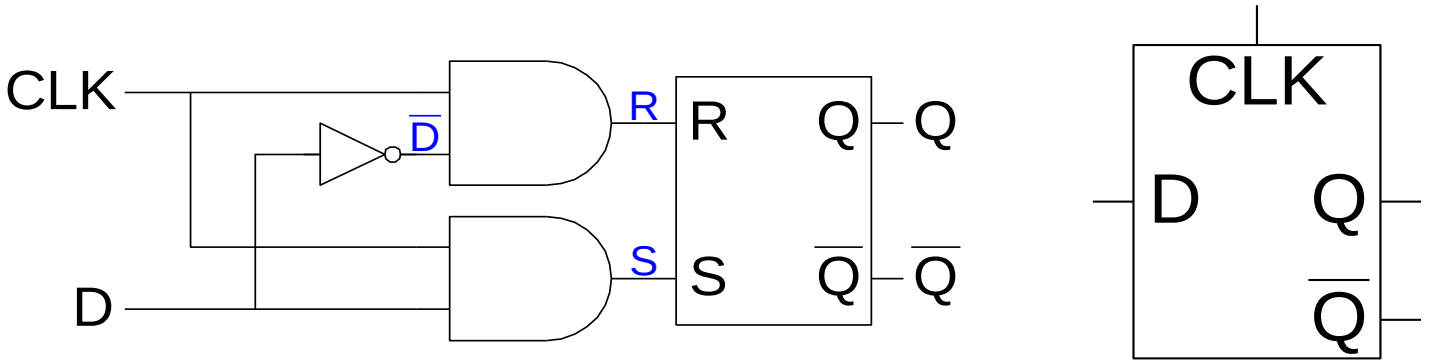
SR Latch Symbol



3.2.2 D Latch Internal Circuit

- *SR* 래치의 '금지된 입력'을 방지하기 위한 래치

- *SR* 래치의 두 입력 단자를 인버터를 통하여 접속함으로써, 두 입력이 서로 반대 값을 가짐, 입력 단자 수 = 1 (D)



3.2.2 D Latch

- Two inputs: *CLK*, *D*
  - *CLK*: controls *when* the output changes
  - *D* (the data input): controls *what* the output changes to

- Function
  - When *CLK* = 1, *D* passes through to *Q* (the latch is *transparent*)
  - When *CLK* = 0, *Q* holds its previous value (the latch is *opaque*)

CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

- Avoids invalid case when $Q \neq$ NOT Q'

3.2.2 D Latch

예제 7-2

D 래치의 *D* 입력 단자와 *En* 단자로 그림 7-9와 같은 파형이 들어올 때 발생하게 될 출력 파형을 구하라. 단, *D* 래치의 출력(*Q*)이 초기에는 리셋 상태에 있다고 가정한다.

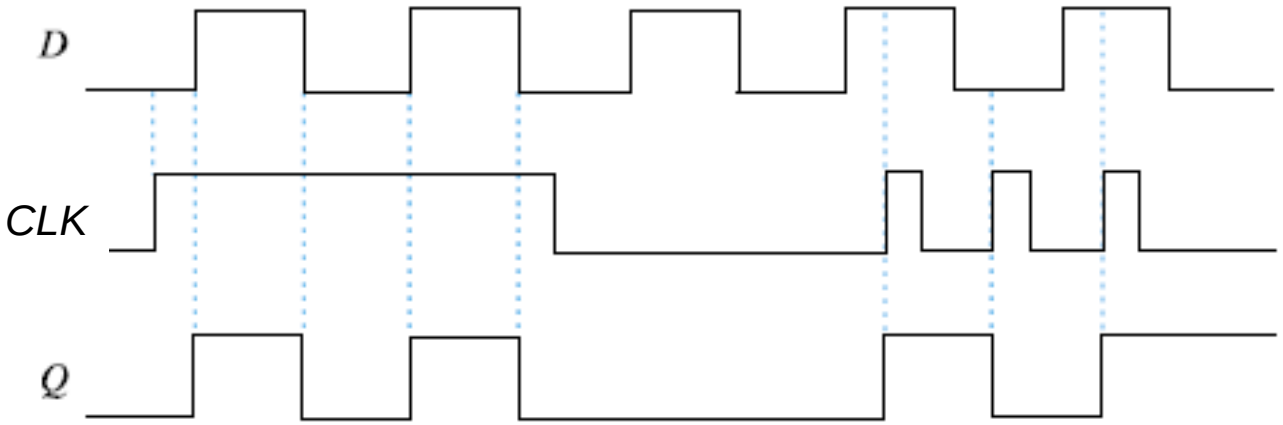


그림 7-9 [예제 7-2]에 대한 그림

3.2.3 Flip-Flop

- 래치의 문제점
  - 래치CLK 신호가 '*high*' 상태를 유지하고 있는 동안에는,
  - 입력 값이 바뀌면 출력도 그에 따라 계속 바뀜

    ➔ 순차회로의 출력이 계속 변경되는 불안정한 상태 발생

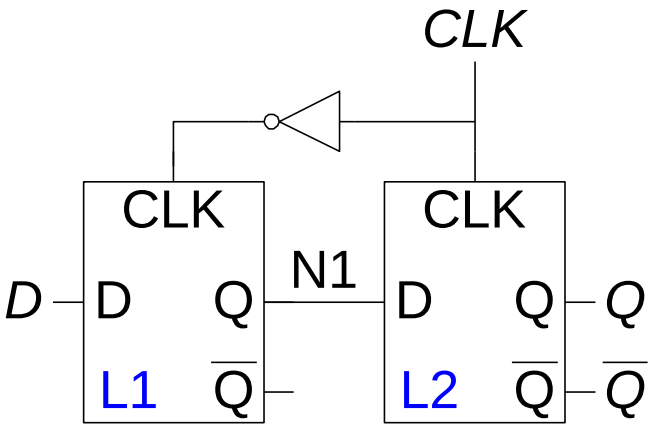
- 해결책
  - 래치CLK 신호가 0→1 혹은 1→0으로 전이(transit) 되는 순간에만 상태(state)가 변경되도록 함

- 플립-플롭
  - 래치CLK 신호의 상태 전이(state transition)가 발생하는 순간의 입력 신호에 따라 상태가 결정되도록 설계된 기억 소자

D Flip-Flop Internal Circuit

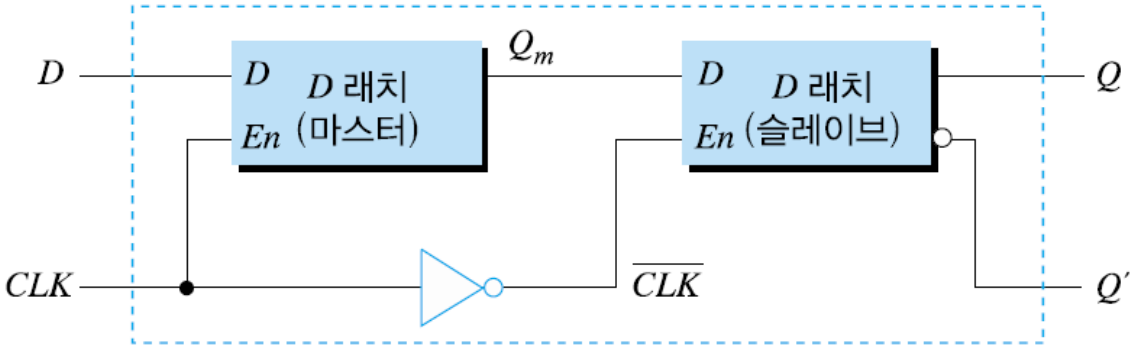
- Two back-to-back latches (L1 and L2) controlled by complementary clocks

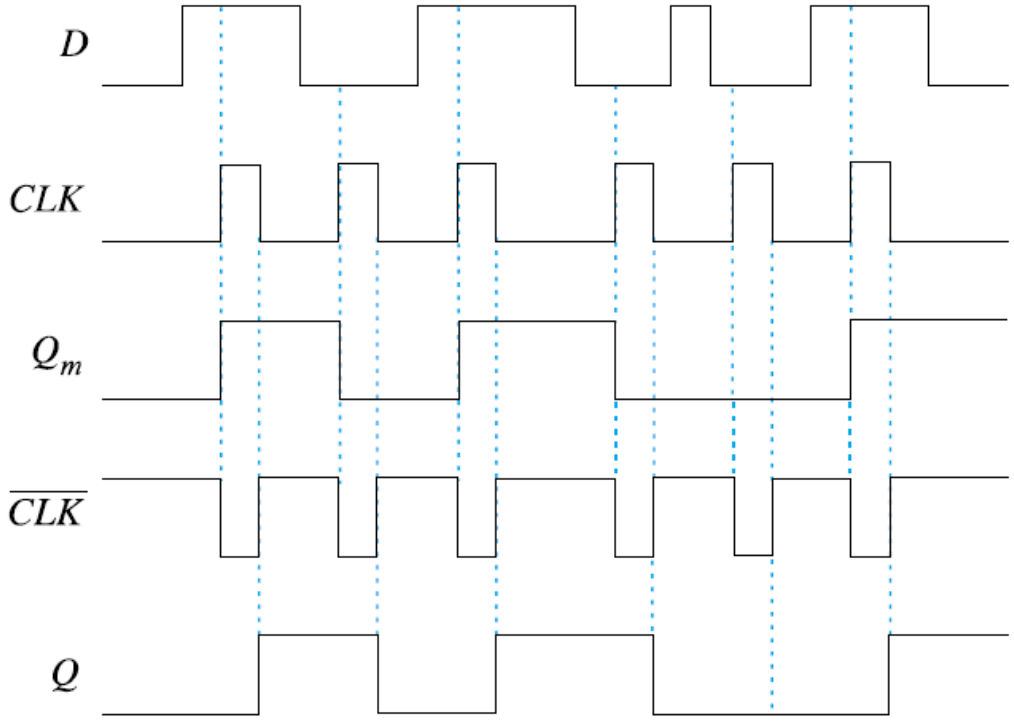
- When *CLK* = 0
  - L1 is transparent
  - L2 is opaque
  - *D* passes through to N1
- When *CLK* = 1
  - L2 is transparent
  - L1 is opaque
  - N1 passes through to *Q*



- Thus, on the edge of the clock (when *CLK* rises from 0→1)
  - *D* effectively passes through to *Q*

D Flip-Flop Internal Circuit



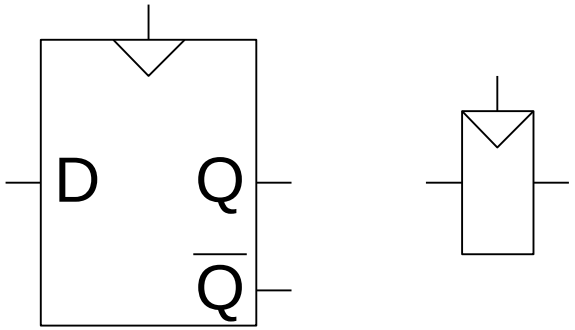


CLK 신호의 1→0 전이
순간의 *D* 입력 값이
상태 값으로 저장됨

3.2.3 D Flip-Flop

- Two inputs: *CLK*, *D*
- *Q* changes only on the rising edge of *CLK*
  - called an *edge-triggered* device
  - it is activated on the clock edge

D Flip-Flop Symbols



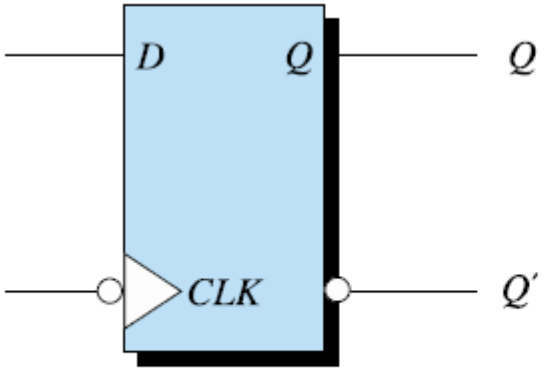
- The flip-flop "samples" *D* on the rising edge of *CLK*
  - When *CLK* rises from 0 to 1, *D* passes through to *Q*
  - Otherwise, *Q* holds its previous value

Clock edge trigger

- 하강 에지 트리거(falling-edge trigger)
  - clock 신호가 1 → 0으로 전이되는 순간의 입력 값에 따라 플립-플롭의 상태가 결정되는 방식.
  - 그래픽 기호에서 clock 입력 단에 버블(o) 및 > 로 표시.
  - negative edge trigger 라고도 함

- 상승 에지 트리거(rising-edge trigger)
  - clock 신호가 0 → 1로 전이되는 순간의 입력 값에 따라 플립-플롭의 상태가 결정되는 방식.
  - 그래픽 기호에서 clock 입력 단에 > 만 표시.
  - positive edge trigger 라고도 함

Negative edge trigger



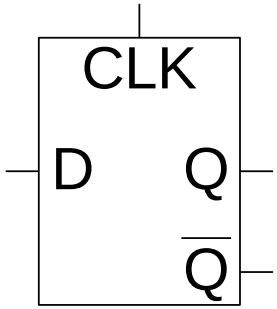
(a) 그래픽 기호

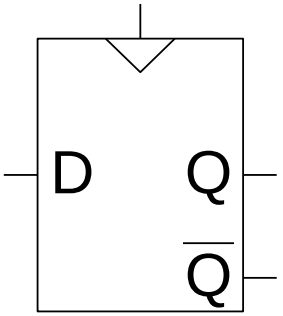
D	CLK	$Q(t+1)$	
0	↓	0	(리셋 상태)
1	↓	1	(세트 상태)
X	0/1	$Q(t)$	(불변)

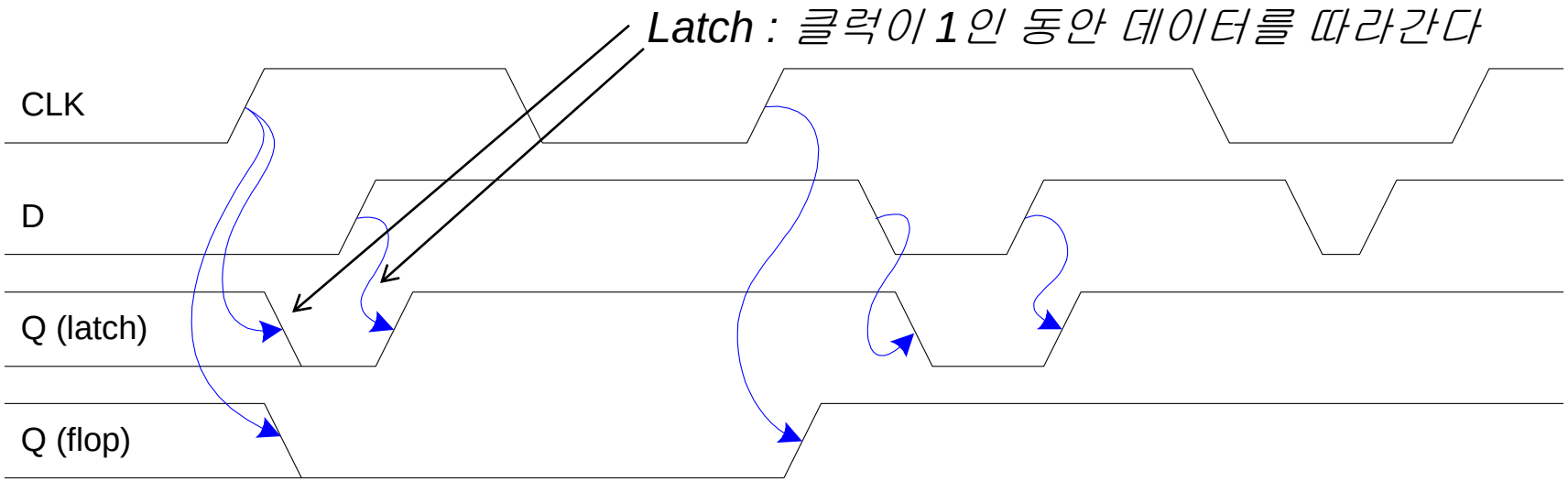
(b) 특성표

입력함수 : $Q(t+1) = D$

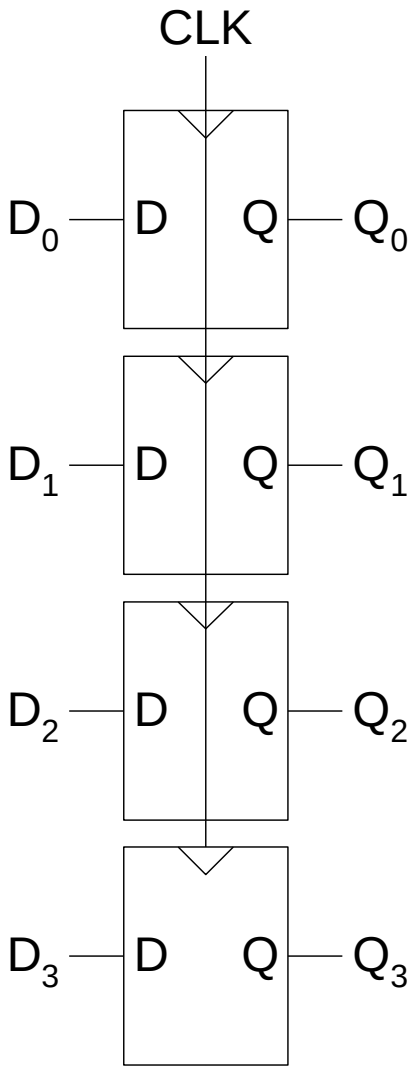
D Flip-Flop vs. D Latch

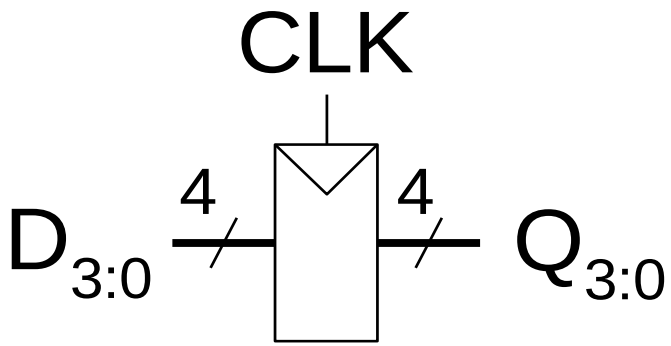






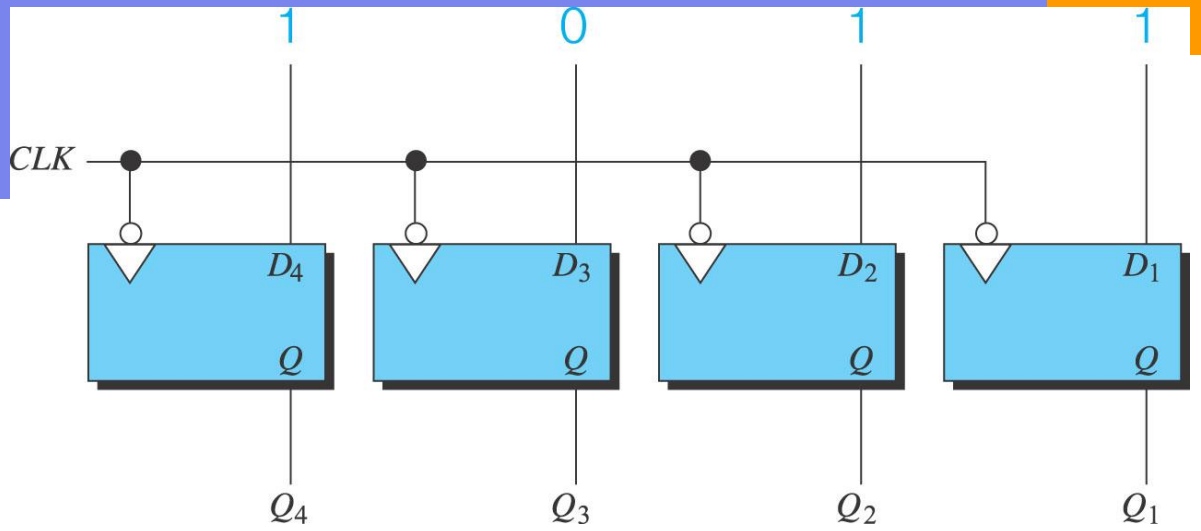
3.2.4 Registers

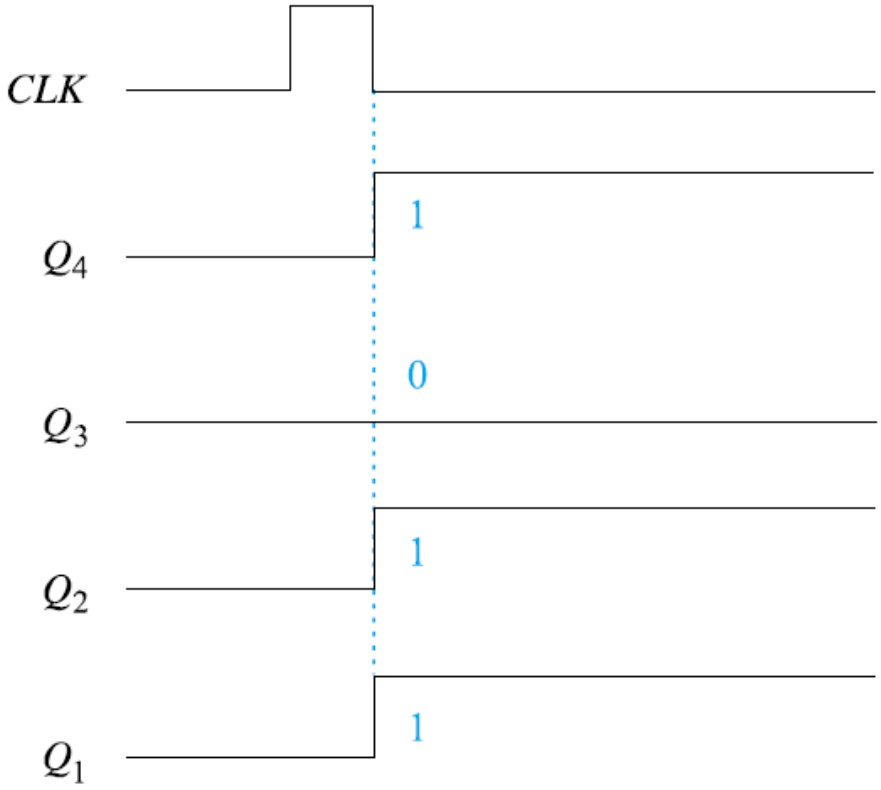




4-bit register

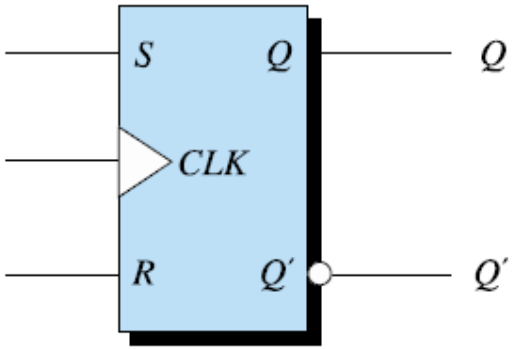
4 개의 입력 비트들을 동시에 저장하는 기능을 수행하는 장치





SR Flip-Flop

- 입력 : *S*(set: 세트), *R*(reset: 리셋)
- 상승-에지 트리거 SR 플립-플롭의 그래픽 기호와 특성



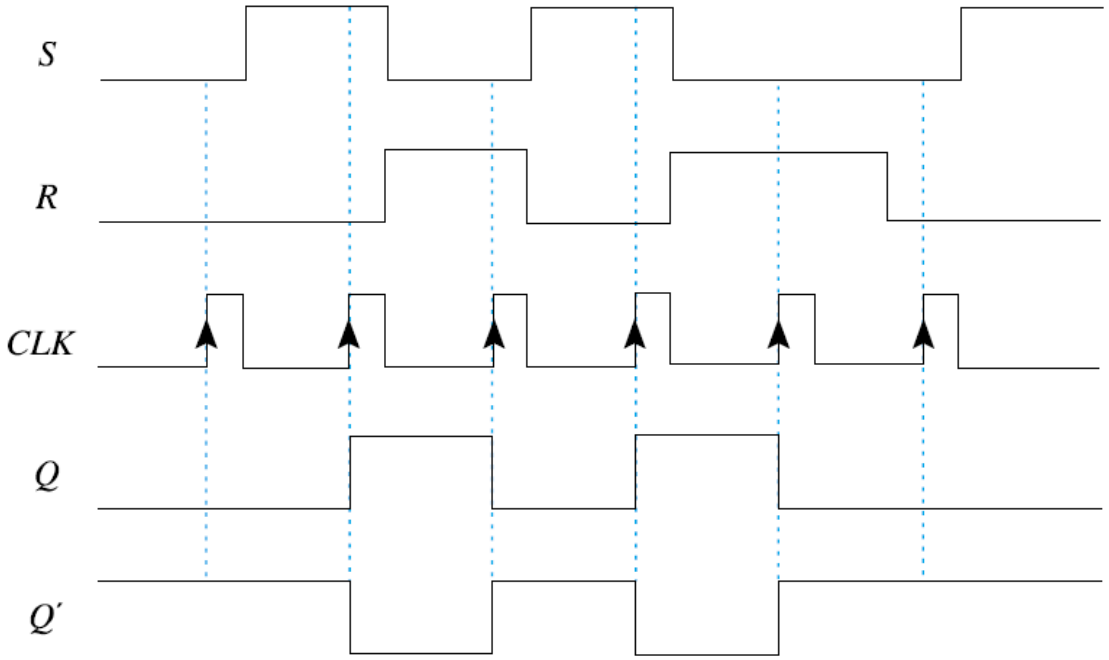
(a) 그래픽 기호

S	R	CLK	$Q(t+1)$	
0	0	↑	$Q(t)$	(불변)
0	1	↑	0	(리셋 상태)
1	0	↑	1	(세트 상태)
1	1	↑	?	(불확실)
X	X	0/1	$Q(t)$	(불변)

(b) 특성표

- 클록 신호의 특정 순간(에지)에 동작(상태 결정)
  ➔ 동기식 회로(synchronous circuit)

SR Flip-Flop



- *SR* 플립-플롭의 문제점:
  - *S* = *R* = 1일 때, *Q(t+1)* = ? (불확실)

JK Flip-Flop

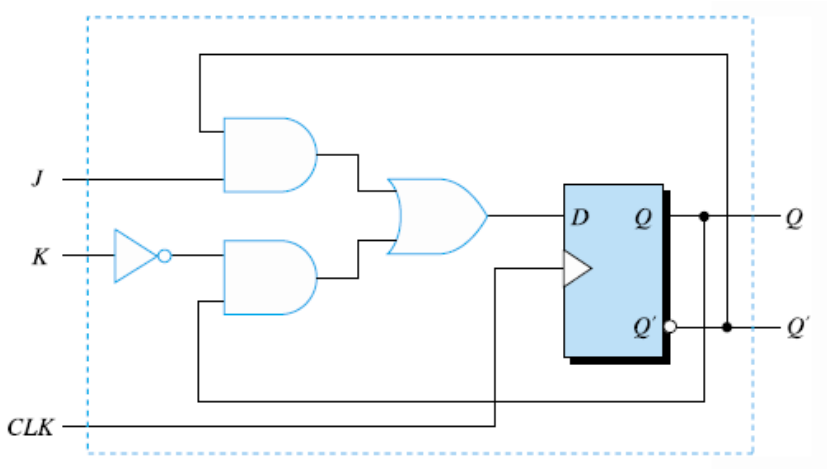
- *SR* 플립-플롭의 문제점을 보완
  - 두 입력들이 모두 1인 경우를 위한 새로운 동작 모드 추가

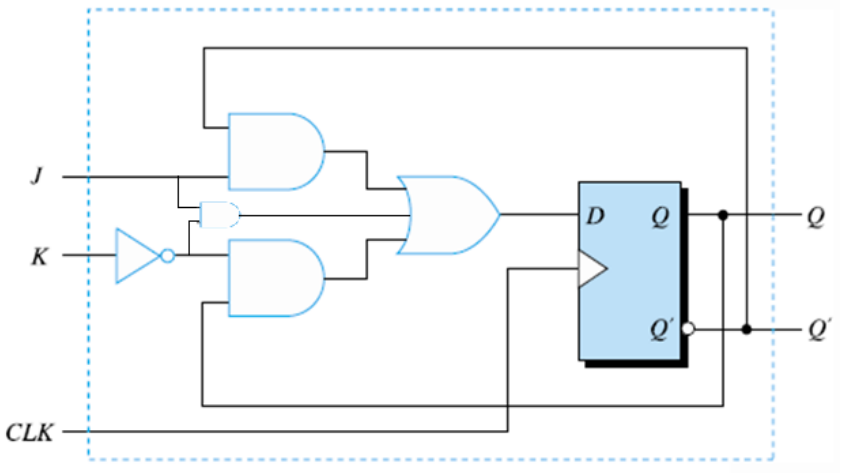
- 입력: *J*, *K*

- 세 가지 동작 모드:
  - 세트(set) : $Q \rightarrow 1$ (입력 조건: J=1, K=0)
  - 리셋(reset) : $Q \rightarrow 0$ (입력 조건: J=0, K=1)
  - 토글(toggle) : 상태 값이 현재 상태의 반대 값으로 변경되는 동작 (입력 조건: J=1, K=1)

JK Flip-Flop Internal Circuit

- *D* 플립-플롭에 외부 회로를 추가하여 구성



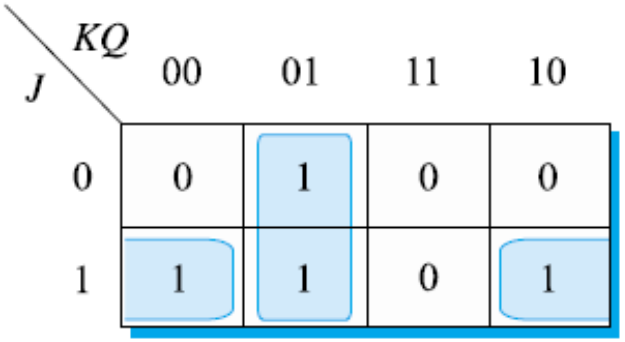


입력 함수(input function) : $D = JQ' + K'Q\ (+ K'J)$

JK Flip-Flop 특성함수

J	K	$Q(t)$	$Q(t+1)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a) 상태 전이표



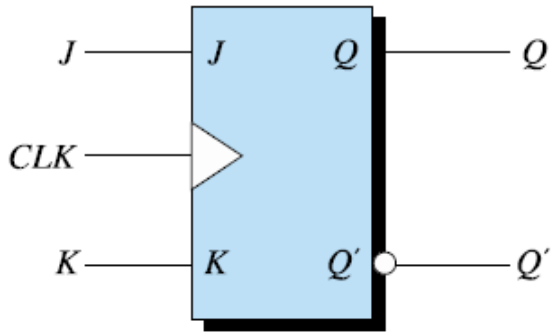
(b) 카노프 맵

입력 함수 : $Q(t+1) = JQ(t)' + K'Q(t) + K'J$

JK Flip-Flop 그래픽 기호와 특성

- 입력 함수(input function) : $D = JQ' + K'Q$
  - $J=1, K=0$ 이라면, $D = Q'+Q = 1$ → $Q(t+1) = 1$
  - $J=0, K=1$ 이라면, $D = 0+0 = 0$ → $Q(t+1) = 0$
  - $J=0, K=0$ 이라면, $D = 0+Q = Q$ → $Q(t+1) = Q(t)$
  - $J=1, K=1$ 이라면, $D = Q'$ → $Q(t+1) = Q(t)'$ <toggle>

- *JK* 플립-플롭의 그래픽 기호와 특성

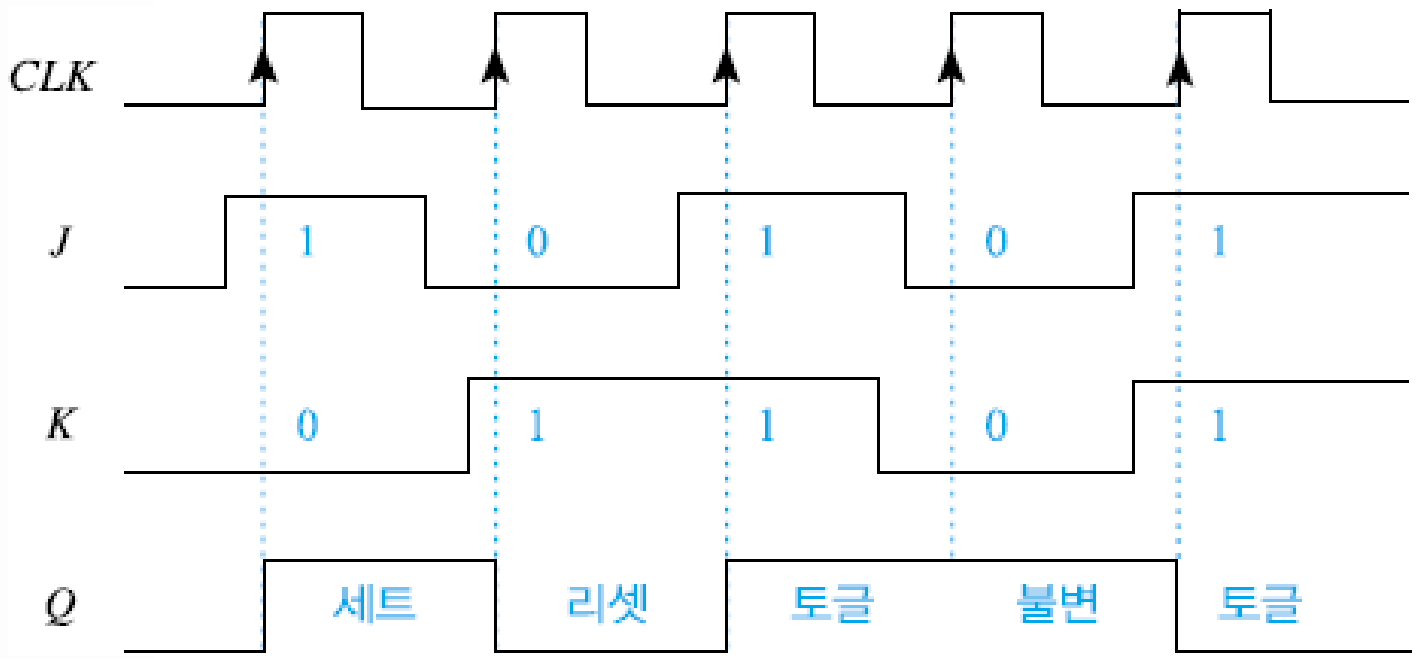


(a) 그래픽 기호

J	K	$Q(t+1)$	
0	0	$Q(t)$	(불변)
0	1	0	(리셋)
1	0	1	(세트)
1	1	$Q'(t)$	(토글)

(b) 특성표

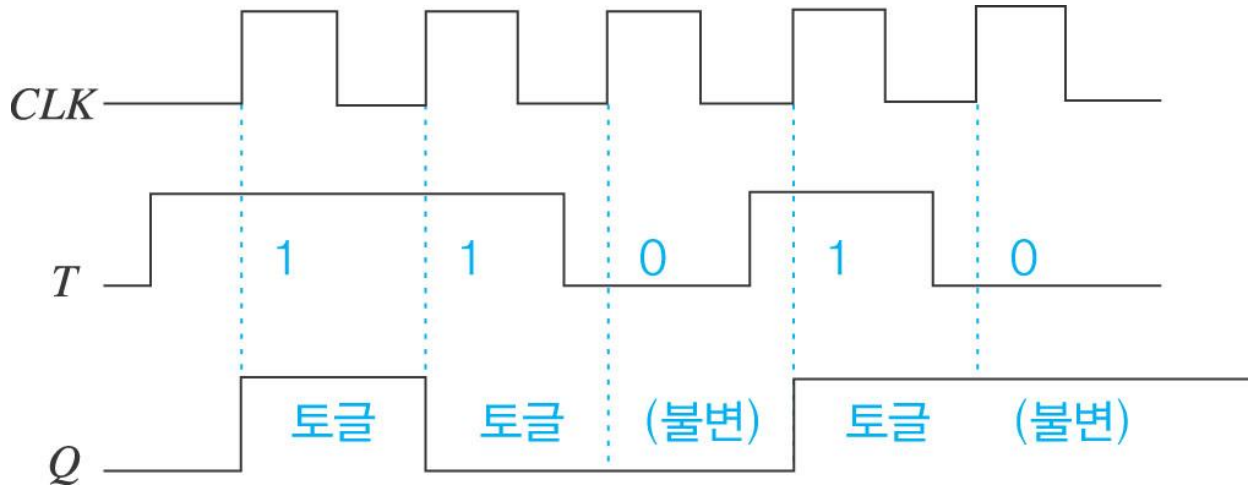
JK Flip-Flop 입출력 동작 특성



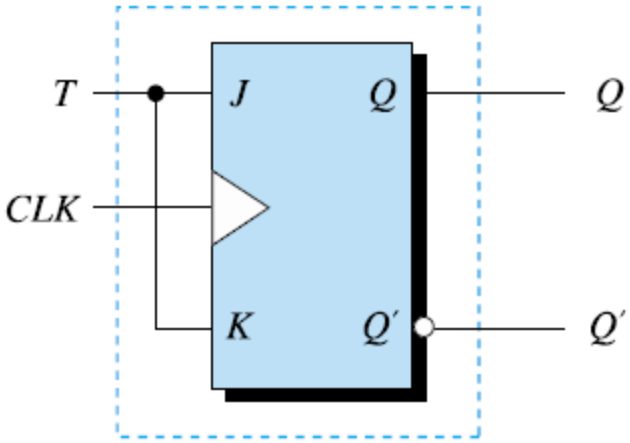
T Flip-Flop

- 구성 방법
  - *JK* 플립-플롭의 두 입력을 접속하여, 하나의 입력 *T* 만 사용

- 동작 특성 : *T* = 0 → 상태 불변(no change)
  T = 1 → 토글 (toggle)



T Flip-Flop 그래픽 기호와 입력 함수



(a) *JK* 플립-플롭을 이용한 구성

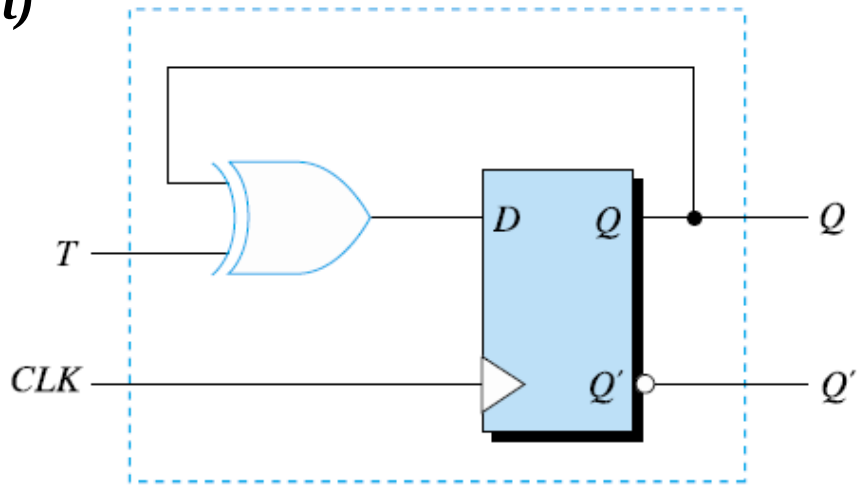
T	$Q(t+1)$	
0	$Q(t)$	(불변)
1	$Q'(t)$	(토글)

(b) 특성표

$$Q(t+1) = T'Q(t) + TQ(t)' = T \oplus Q(t)$$

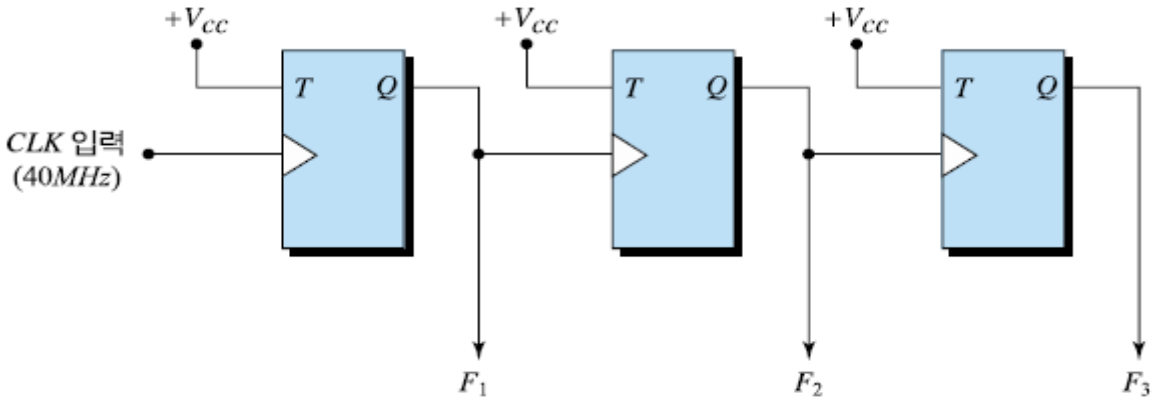
T	$Q(t)$	$Q(t+1)$	
0	0	0	(불변)
0	1	1	(불변)
1	0	1	(토글)
1	1	0	(토글)

(a) 상태 전이표

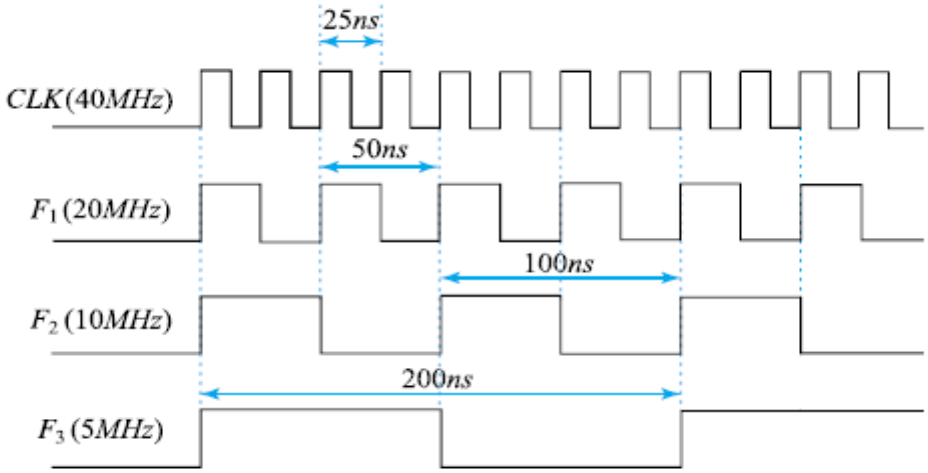


(b) *T* 플립-플롭의 다른 구성

주파수 감소기(frequency divider)



(a) T 플립-플롭들을 이용하여 구성한 주파수 감소기

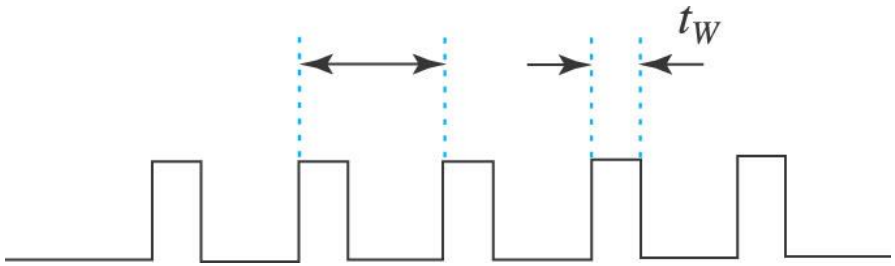


(b) CLK 신호 및 출력 파형들

Clock Signal

- 클록 신호(clock signal)
  - 동기식 순차회로의 동작 기준 시간을 정해주는 신호

  - 주기(duration) : 클록 신호에서 어떤 한 펄스의 상승 에지부터 다음 펄스의 상승 에지까지의 시간으로서, 기호는 τ



  - 클록 주파수(clock frequency: f) : 초당 발생되는 펄스의 수로서, $1/\tau$ 로 계산하며, 단위는 *Hz* (헤르츠)

  [예] $\tau = 0.01s$ → $f = 1/0.01 = 100Hz$
  $f = 20\ MHz$ → $\tau = 1/(20 \times 10^6) = 50 \times 10^{-9} = 50ns$

Clock Signal

- 펄스 폭(pulse width: t_W)
  - 각 펄스에서 '*high(1)*' 레벨이 유지되고 있는 시간

- 의무 사이클(duty cycle: D_t)
  - 클록 신호의 한 주기 동안 '*high(1)*' 레벨에 있는 시간의 전체 주기에 대한 비율

$$D_t = (t_W / \tau) \times 100\ [\%]$$

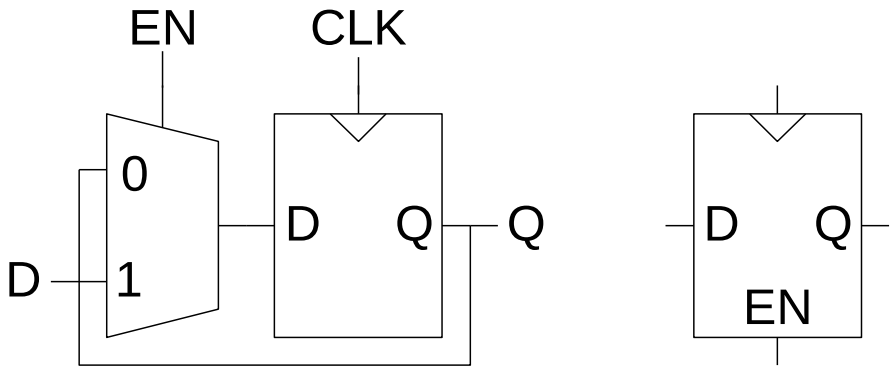
- 최대 클록 주파수(maximum clock frequency)
  - 플립-플롭에 인가될 수 있는 클록의 최대 주파수로서, 내부 회로의 동작 속도에 의해 결정

3.2.5 Enabled Flip-Flops

- Function
  - The enable input (*EN*) controls when new data (*D*) is stored
  - Inputs: *CLK*, *D*, *EN*
  - When *EN* = 1, *D* passes through to *Q* on the clock edge
  - When *EN* = 0, the flip-flop retains its previous state

Internal Circuit

Symbol



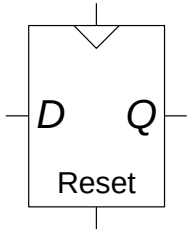
3.2.6 Resettable Flip-Flops

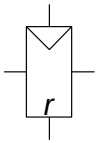
- Function
  - Inputs: *CLK*, *D*, *Reset*(*reset* 상태(*Q*=0)로 변경하는 입력)
  - 시스템 초기화 및 오류 발생 시 사용
  - 주로 '*active-low*' 신호 사용 (*Reset*=0:활성화)

  - When *Reset* = 1, *Q* is reset to 0
  - When *Reset* = 0, the flip-flop behaves like an ordinary D flip-flop

- Two types:
  - ***Synchronous***: resets at the clock edge only
  - ***Asynchronous***: resets immediately when *Reset* = 1

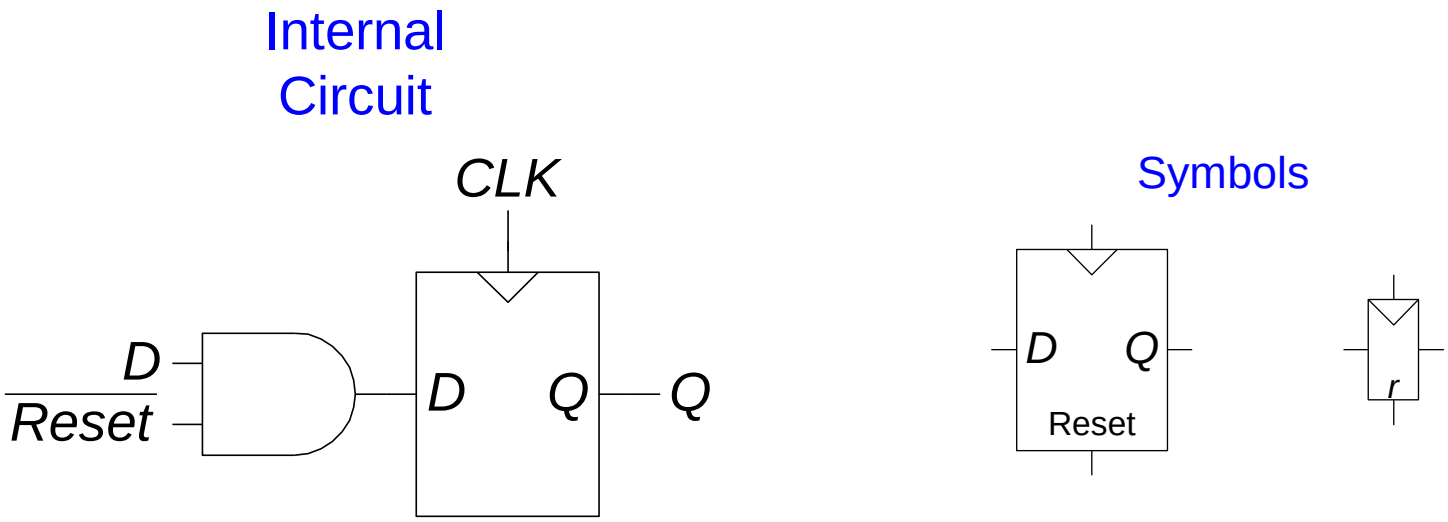
Symbols





Resettable Flip-Flops

- *Synchronously* resettable flip-flop
  - requires changing the internal circuitry of the flip-flop



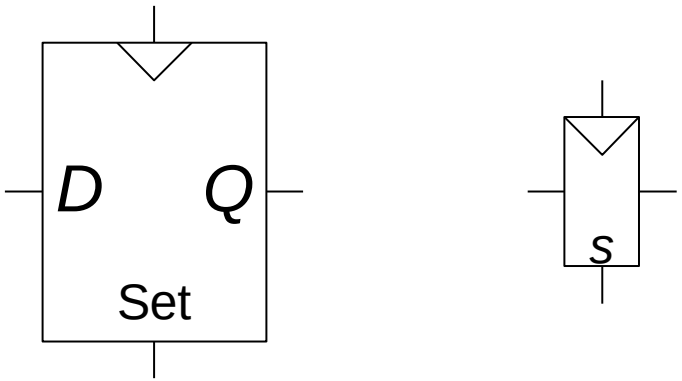
- Asynchronously resettable flip-flop: (see Exercise 3.12)

Settable Flip-Flops

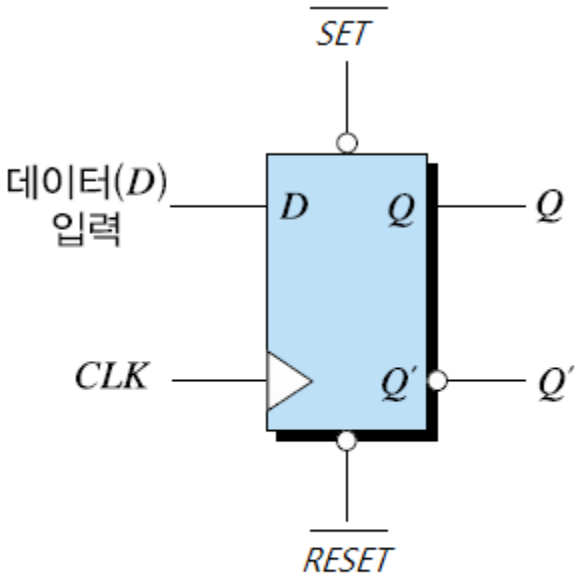
- Function
  - Inputs: *CLK*, *D*, *Set*(set 상태(*Q*=1)로 변경하는 입력)
  - 플립-플롭의 초기값 설정에 사용

  - When *Set* = 1, *Q* is set to 1
  - When *Set* = 0, the flip-flop behaves like an ordinary D flip-flop

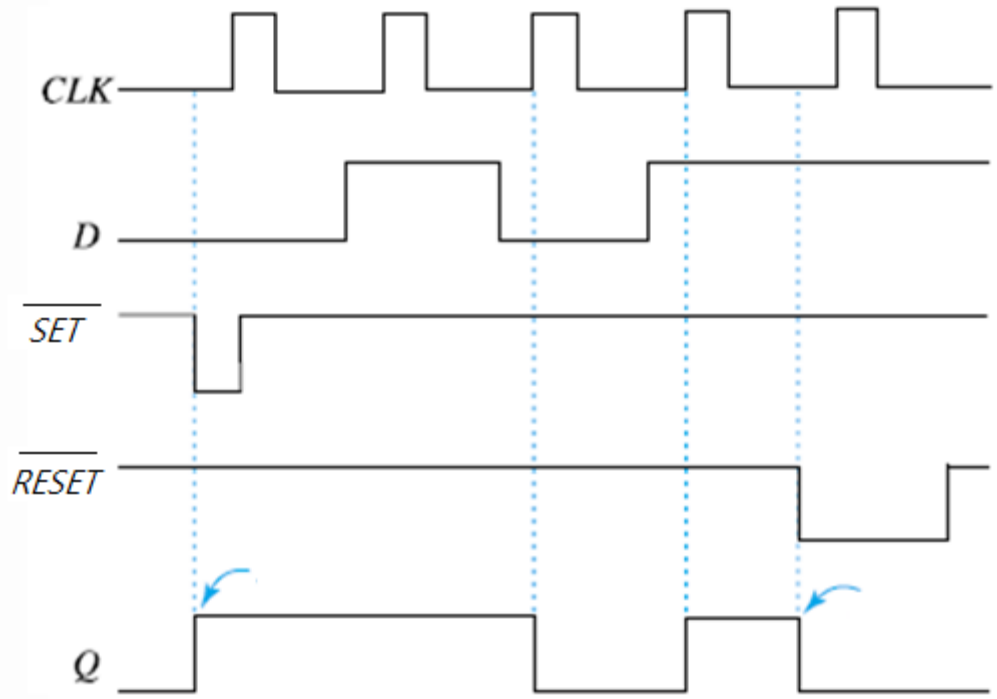
Symbols



Settable / Resettable



(a) 그래픽 기호



(b) 비동기식 입력 신호에 의한 D 플립-플롭의 동작

Q & A