Chapter 3 :: Sequential Logic Design (4)

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참고도서 : 개정판 논리회로 설계(김종현저) , 홍릉과학출판사.

- 제7장 순차회로의 분석과 설계

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Chapter 3 :: Topics

- Introduction
- Latches and Flip-Flops
- Synchronous Logic Design
- Finite State Machines

- Shifter

- Timing of Sequential Logic
- Parallelism

Shift Register의 설계

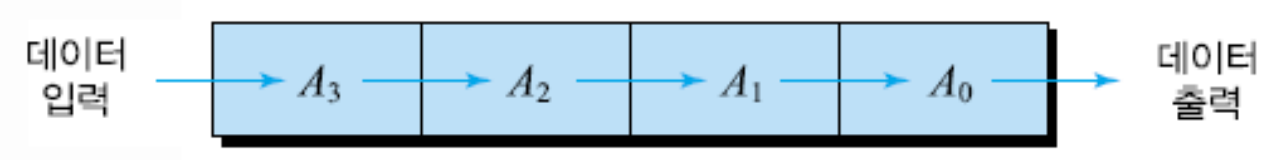
Register

- 레지스터(register)
  - 여러 개의 데이터 비트들을 저장하기 위한 장치로서, 비트 수만큼의 플립-플롭으로 구성.
  - *D* 플립-플롭들이 사용되며, 각 플립-플롭 당 한 비트씩 저장
  - 길이: 4-비트, 8-비트, 16-비트, 32-비트, 64-비트
  - 주요 용도: 컴퓨터 중앙처리장치(CPU)의 내부 기억장치

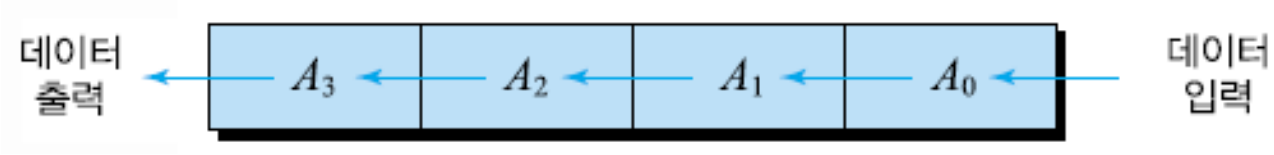
- 시프트 레지스터(shift register)
  - 저장 기능 외에, 비트들을 좌측 혹은 우측으로 이동시키는 기능도 가진 레지스터

Shifters

- **Logical shifter**
  - shifts value to left or right and fills empty spaces with 0's
  - Ex: 11001 >> 2 = 00110
  - Ex: 11001 << 2 = 00100
  - Right shift (LSB 방향)



  - Left shift (MSB(most significant bit) 방향)



Shifters

- **Arithmetic shifter**

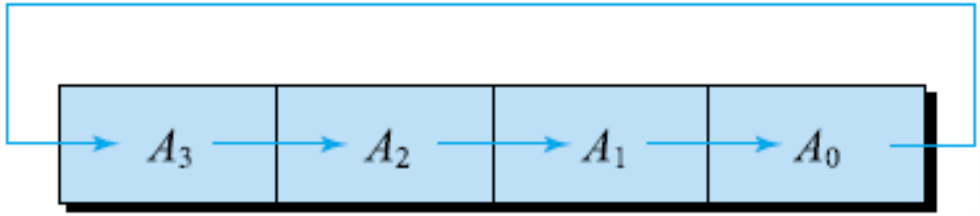
  same as logical shifter, but on right shift, fills empty spaces with the old most significant bit (MSB).

  –Ex: 11001 >>> 2 = **11**110

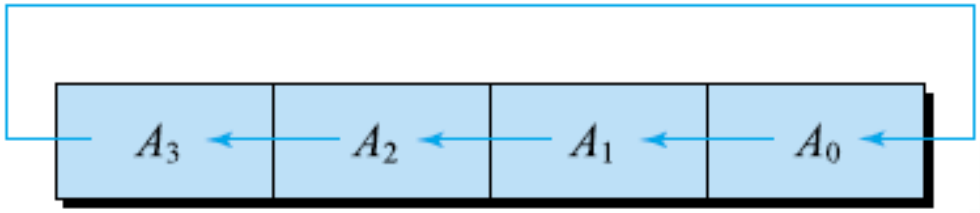
  –Ex: 11001 <<< 2 = 00100

Shifters

- **Rotator (circular shift, 순환 시프트)**
  - rotates bits in a circle, such that bits shifted off one end are shifted into the other end
  - Ex: 11001 ROR 2 = 01110
  - Ex: 11001 ROL 2 = 00111

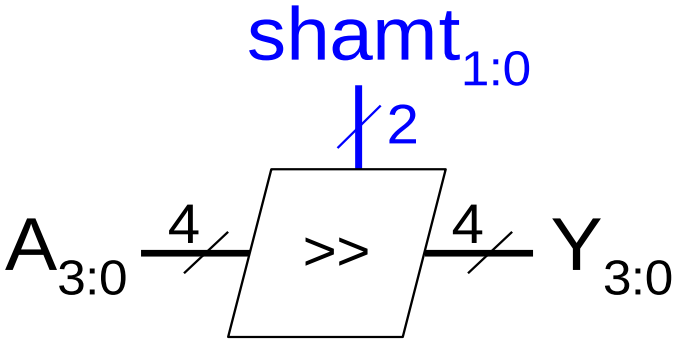


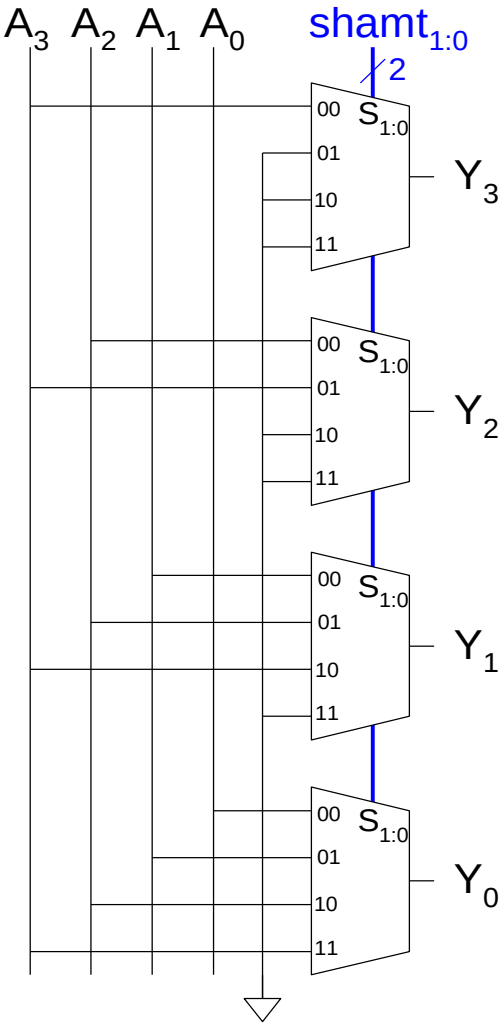
(a) 우측 회전



(b) 좌측 회전

Shifter Design

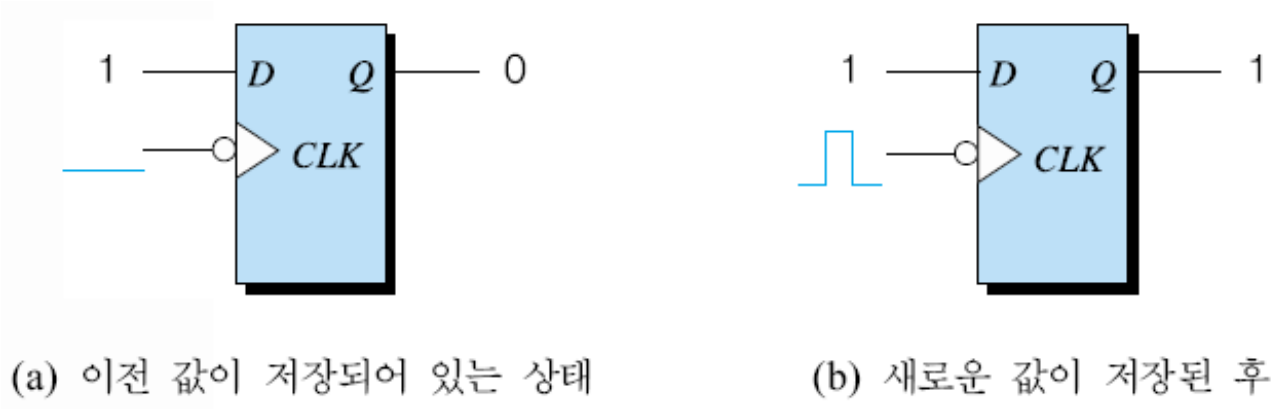




Parallel register(병렬 레지스터)

- 데이터 비트가 *D* 플립-플롭에 저장되는 원리
  - *D* 플립-플롭의 *D* 입력에 데이터 비트 값이 인가되면, CLK 신호의 트리거 에지에서 저장됨

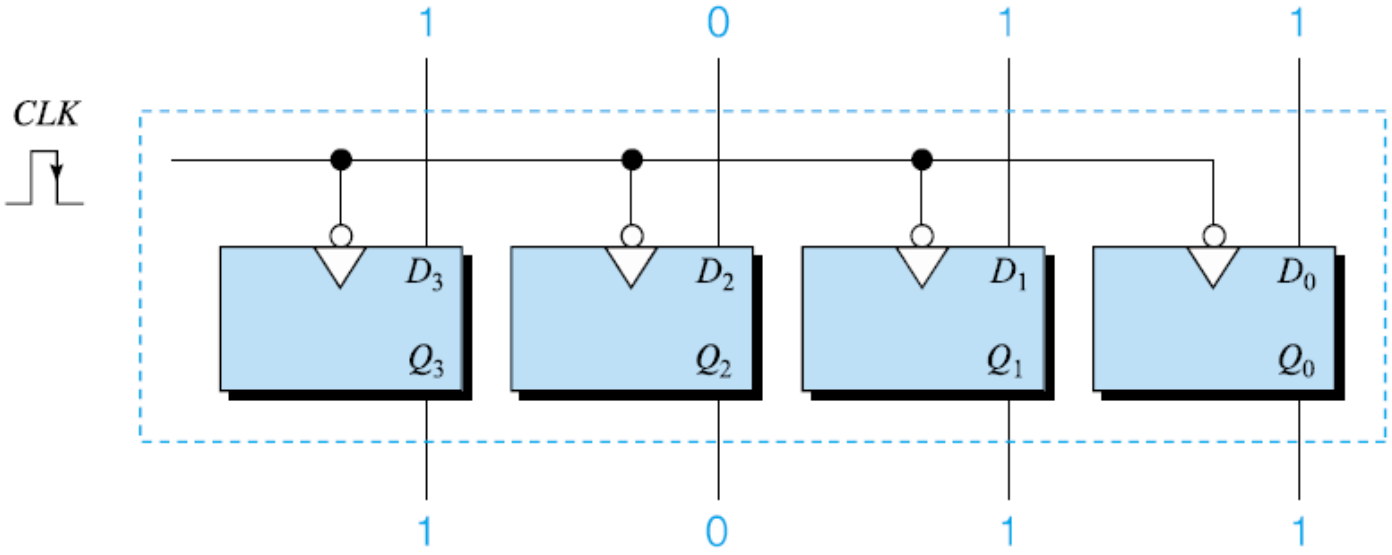
[예] *D* 입력에 '1'이 인가되었을 때, CLK의 하강 에지에서 데이터가 저장되는 동작



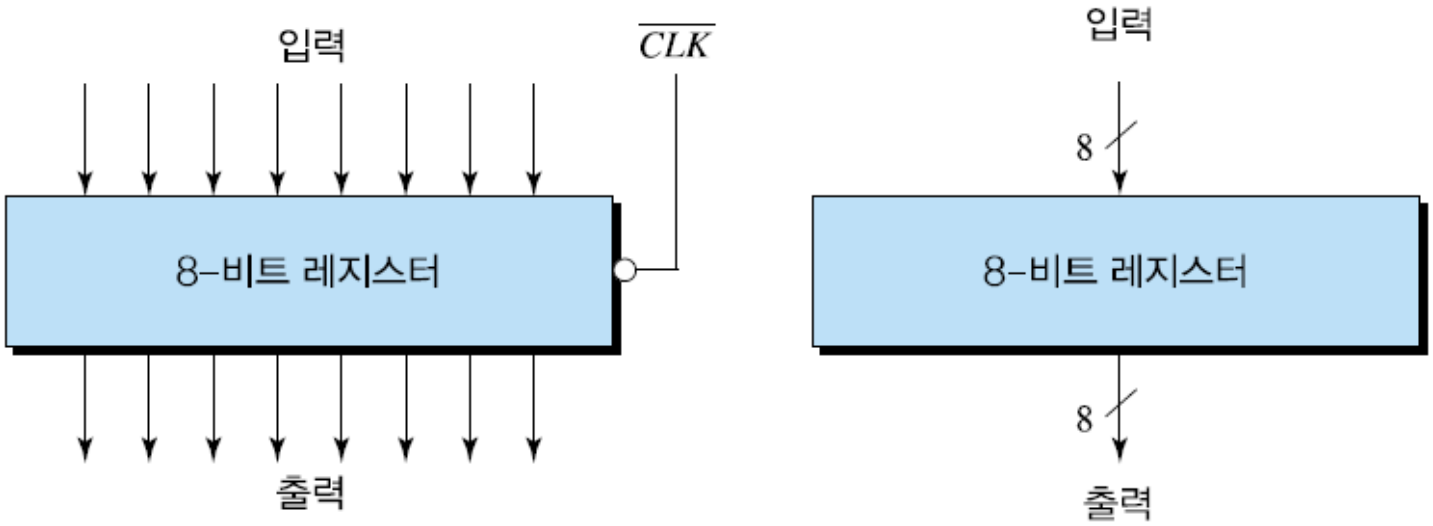
(a) 이전 값이 저장되어 있는 상태 (b) 새로운 값이 저장된 후

레지스터에서의 병렬 적재 동작

- 4-비트 병렬 레지스터에서의 병렬 적재(Load) 동작
  - 네 개의 입력 비트들이 동시에 각 D 플립-플롭들의 입력으로 인가
  - CLK 신호의 트리거 에지에서 동시에 저장



8-비트 병렬 레지스터의 블록도

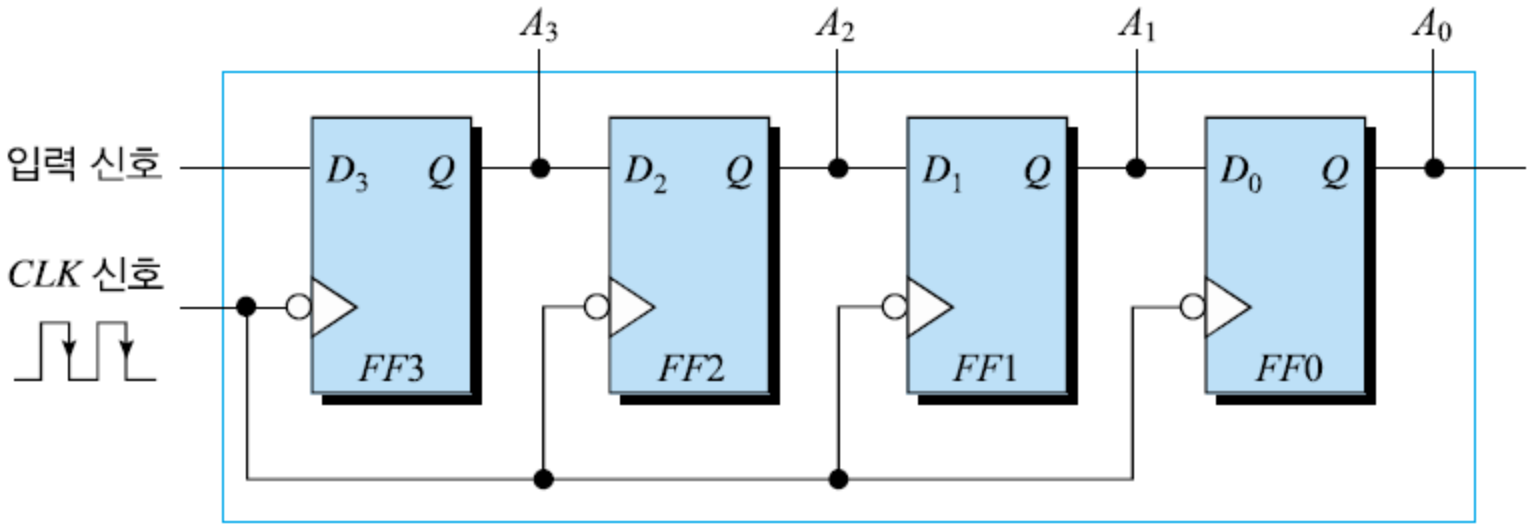


(a) 블록도 (b) 간략화 된 블록도

Serial register(직렬 레지스터)

- *D* 플립-플롭들을 직렬로 접속
- 저장할 데이터를 한 비트씩 입력

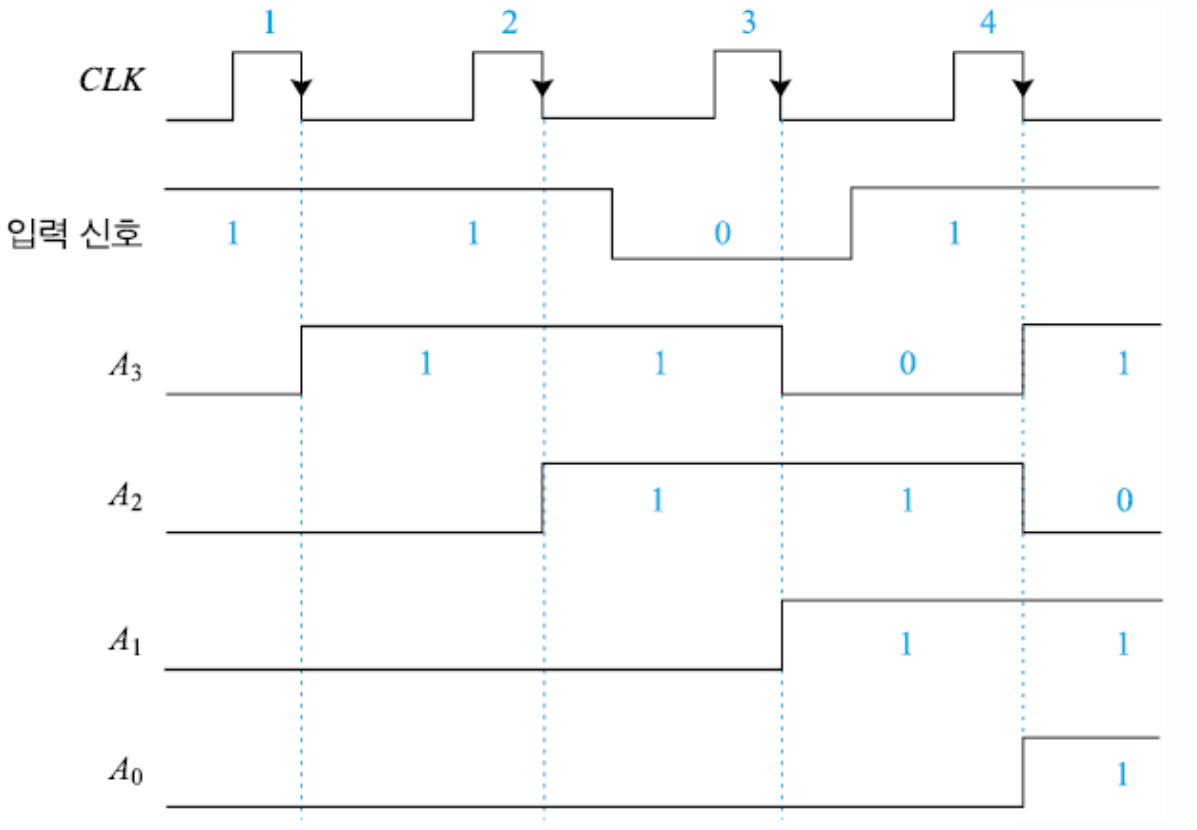
[예]4-비트 직렬 레지스터



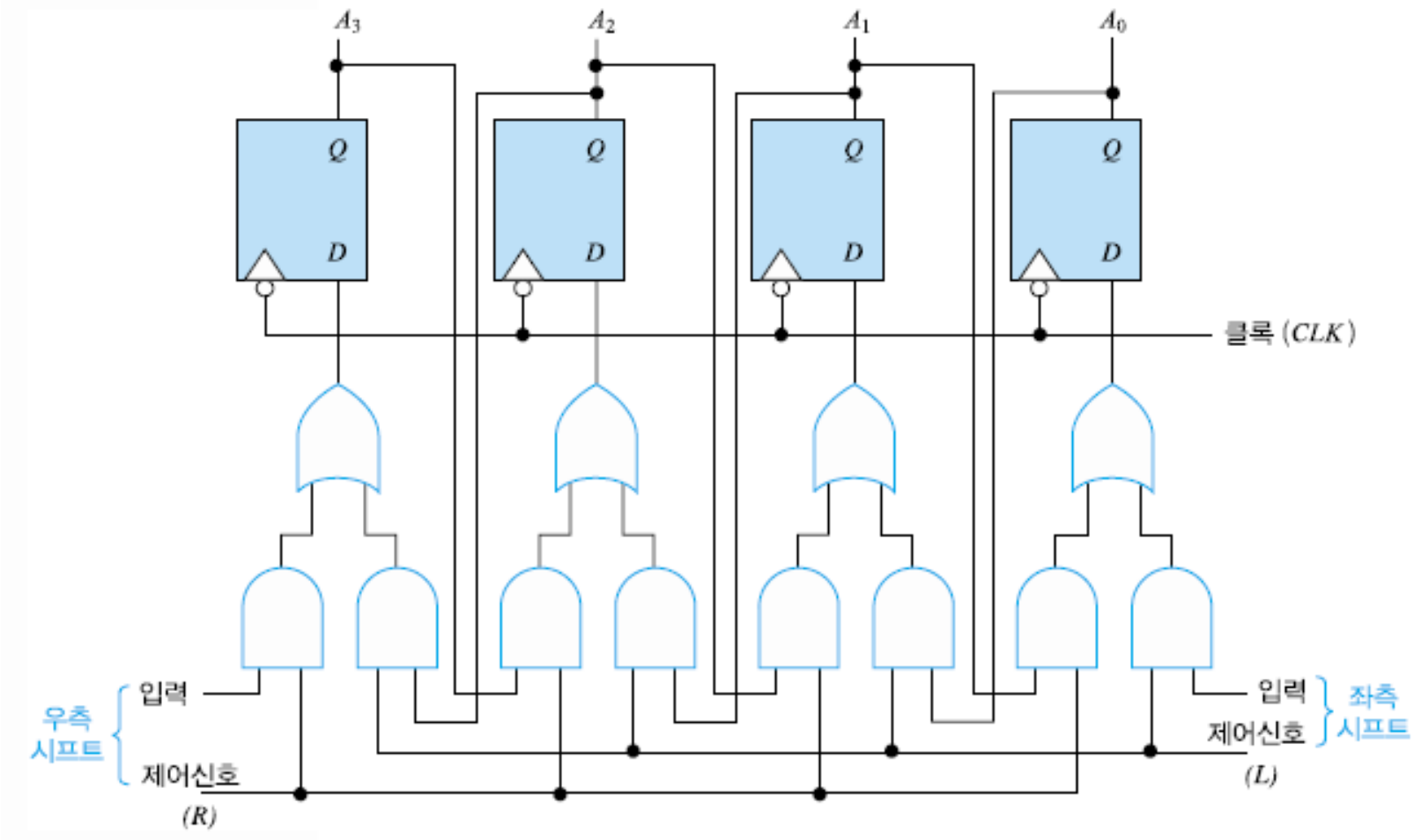
레지스터 데이터 저장 방법

- 데이터 저장 방법: LSB부터 MSB로 한 비트씩 입력

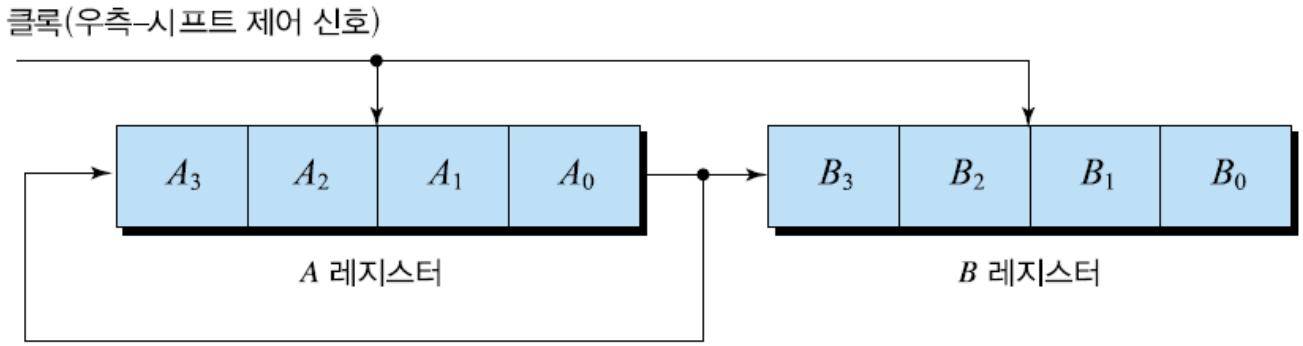
  [예] 데이터 '1011' 저장: 1, 1, 0, 1의 순서로 입력



양방향 **Shift register**의 내부 구성도



Shift 동작을 이용한 serial data 전송



	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
초기상태	1	0	1	1	0	0	0	0
t_1	1	1	0	1	1	0	0	0
t_2	1	1	1	0	1	1	0	0
t_3	0	1	1	1	0	1	1	0
t_4	1	0	1	1	1	0	1	1

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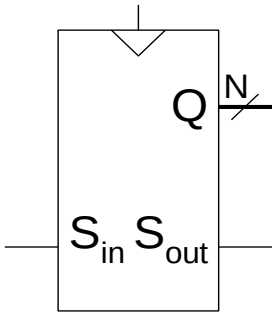
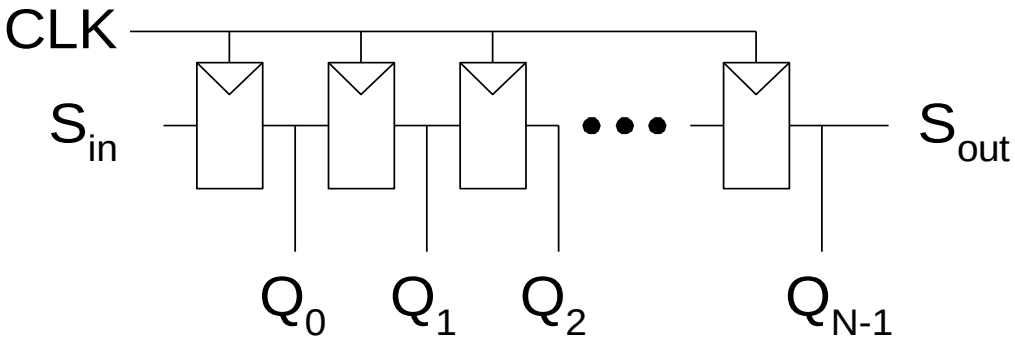
- Shift a new value in on each clock edge
- Shift a value out on each clock edge
- *Serial-to-parallel converter*: converts serial input (S_{in}) to parallel output ($Q_{0:N-1}$)

Symbol:

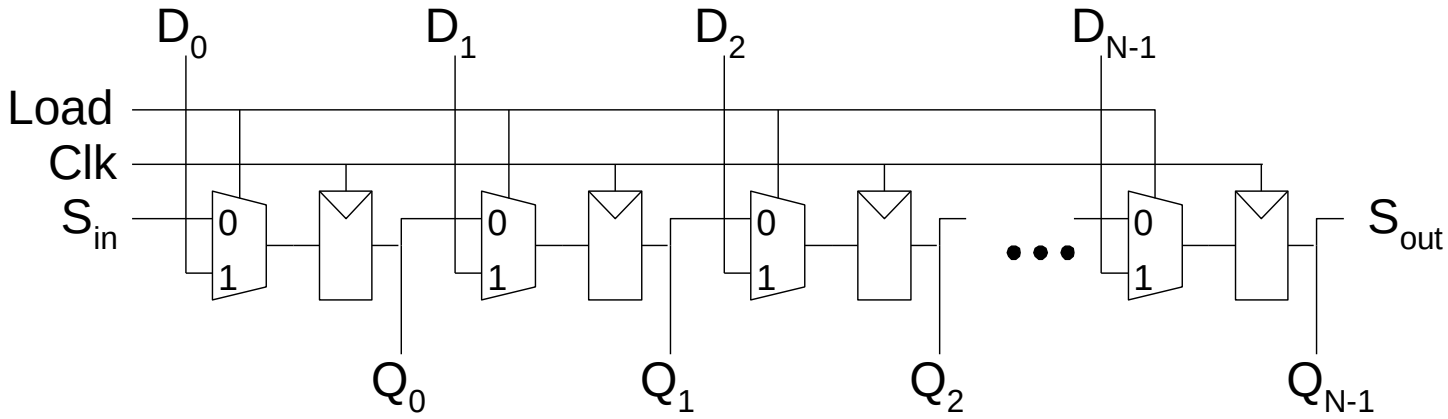


Implementation:



Shift Register with Parallel Load

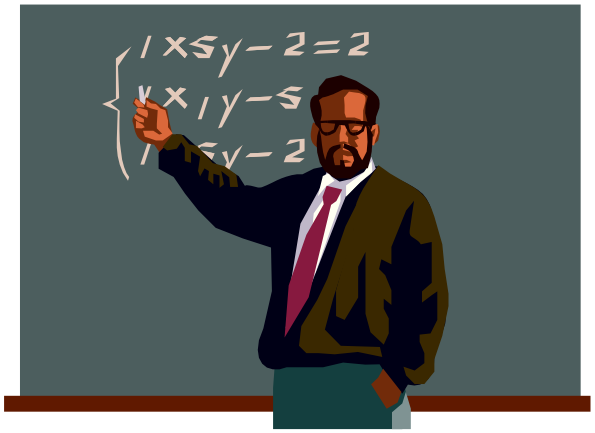
- When *Load* = 1, acts as a normal *N*-bit register
- When *Load* = 0, acts as a shift register
- Now can act as a *serial-to-parallel converter* (S_{in} to $Q_{0:N-1}$) or a *parallel-to-serial converter* ($D_{0:N-1}$ to S_{out})



3.4.6 FSM Design Procedure

- Identify the inputs and outputs (입출력을 고려하여)
- Sketch a state transition diagram (상태다이어그램을 그리고)
- Write a state transition table (상태표를 작성)
- Select state encodings (상태코드를 binary 또는 one-hot으로 결정)

- For a Moore machine:
  - Rewrite the state transition table with the selected state encodings
  - Write the output table
- For a Mealy machine:
  - Rewrite the combined state transition and output table with the selected state encodings

- Write Boolean equations for the next state and output logic(부울식 작성)
- Sketch the circuit schematic (회로도 스케치)

Q & A