Cadence Full-Custom IC Design

Contents

Introduction

Course & Tool

- Course
  Nineplus IT - Cadence® Full-Custom IC Designer
- Tools
  1. Cadence Virtuoso Schematic Editor / Layout Editor
  2. Cadence Virtuoso Spectre / ADE
  3. Assura DRC / LVS
  4. GPDK090

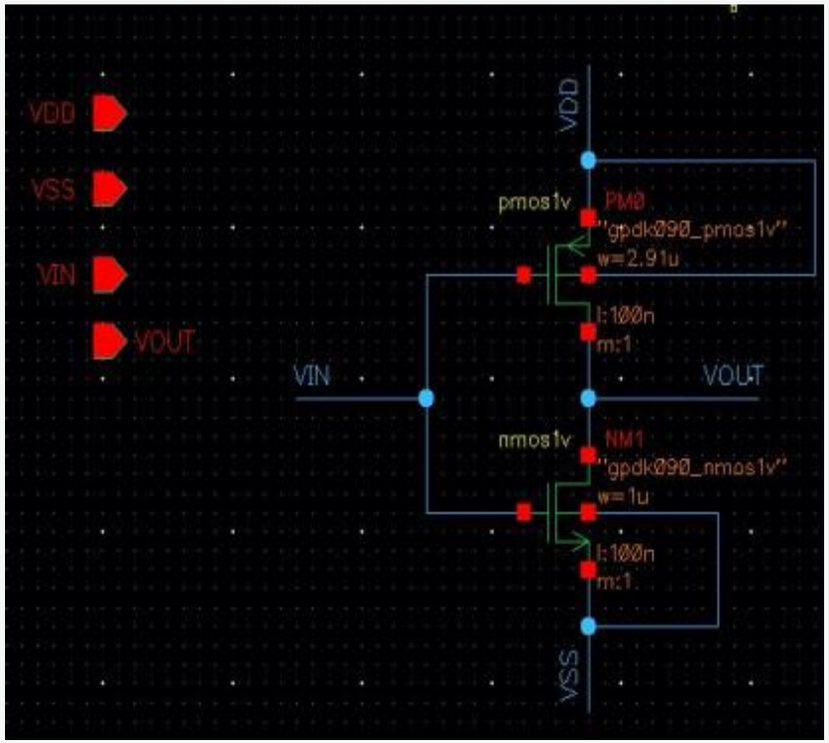
Digital Circuit

What do I make?

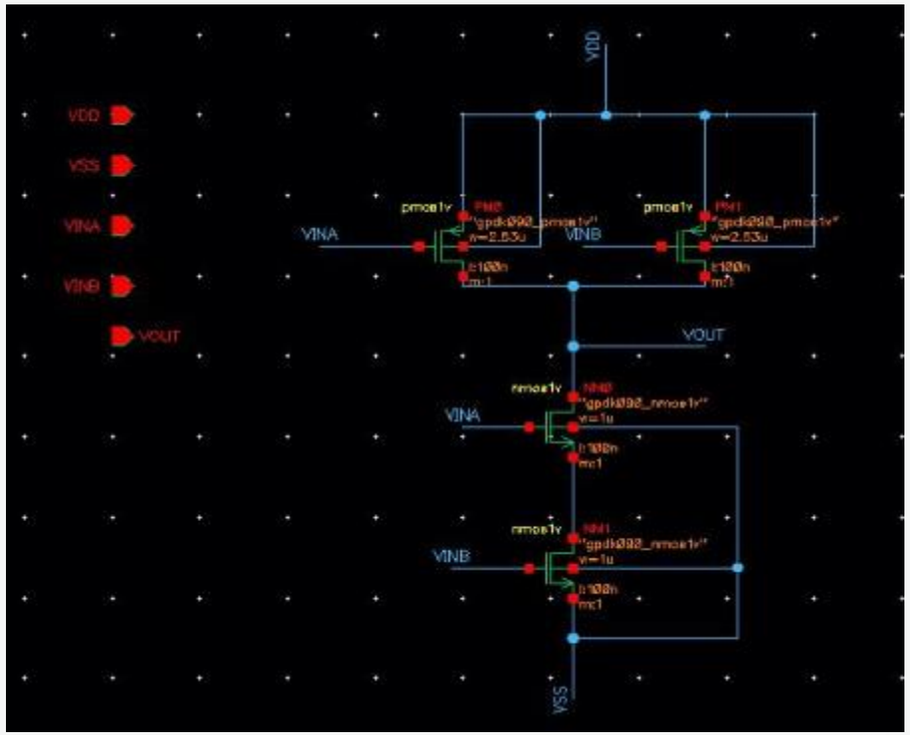
Logic Gate	Multiplexer	Adder
NOT Gate	2X1 MUX	Half Adder
2~4 NAND/NOR	4X1 MUX	Full Adder
Switch (for transmission gate)		4_bit Adder & Substracter

Logic Gate

Schematic



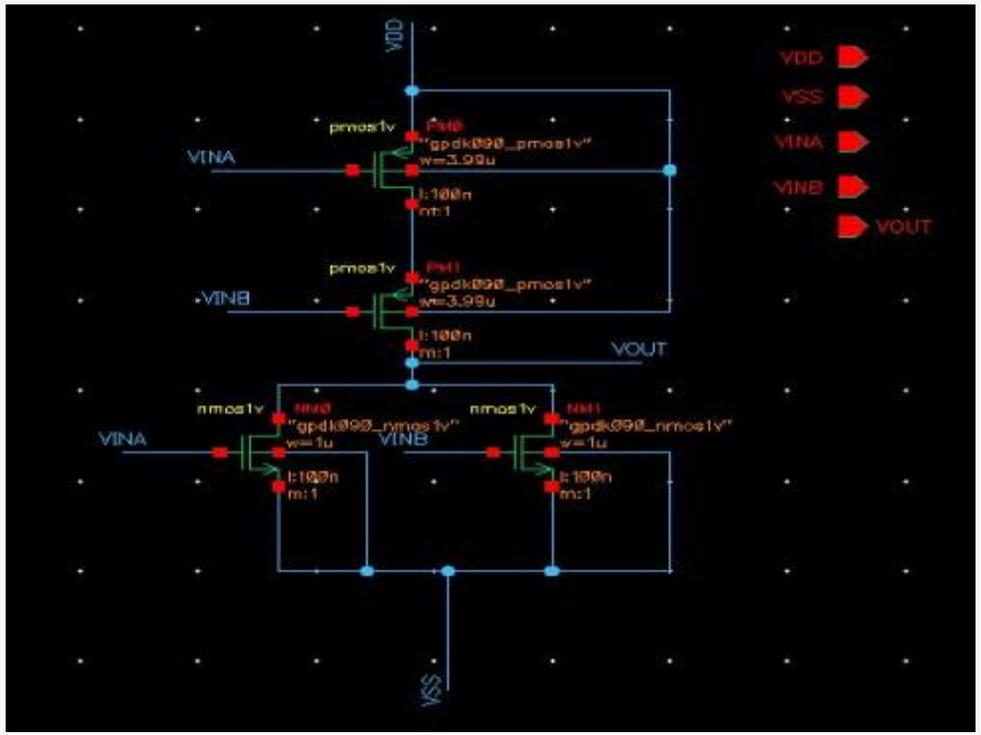
NOT GATE



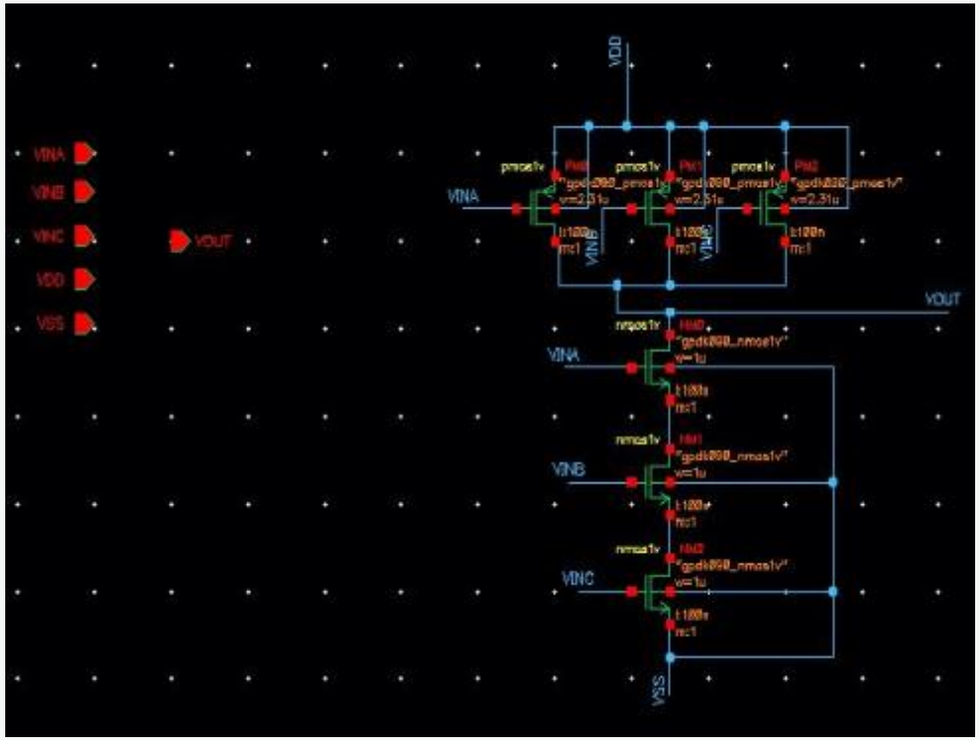
2-NAND GATE

Logic Gate

Schematic



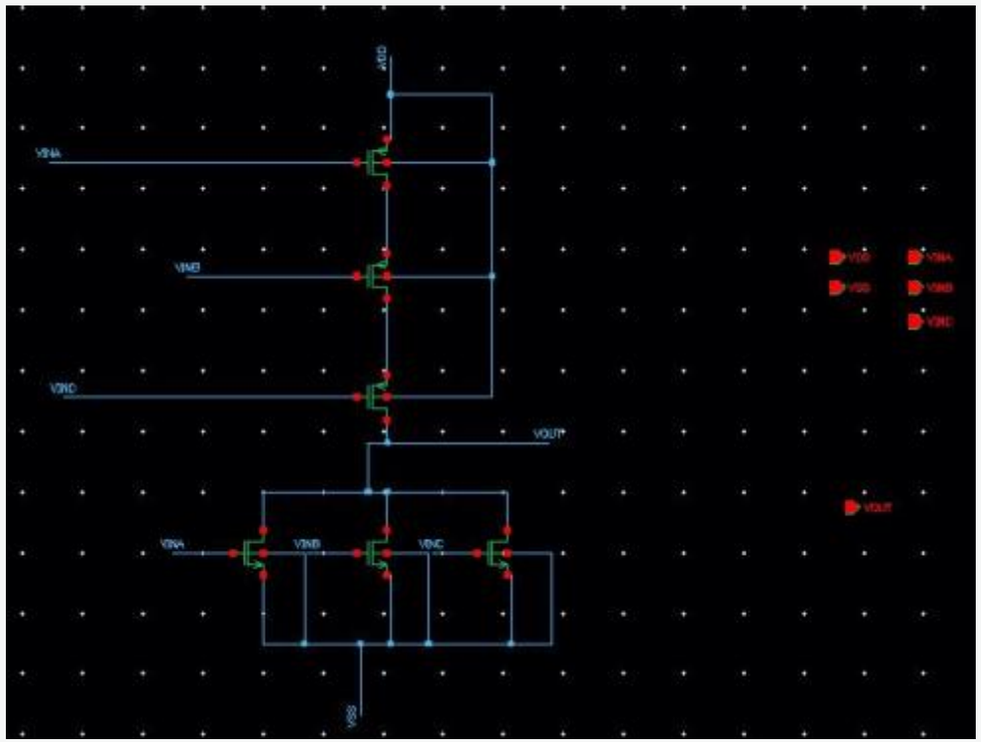
2-NOR GATE



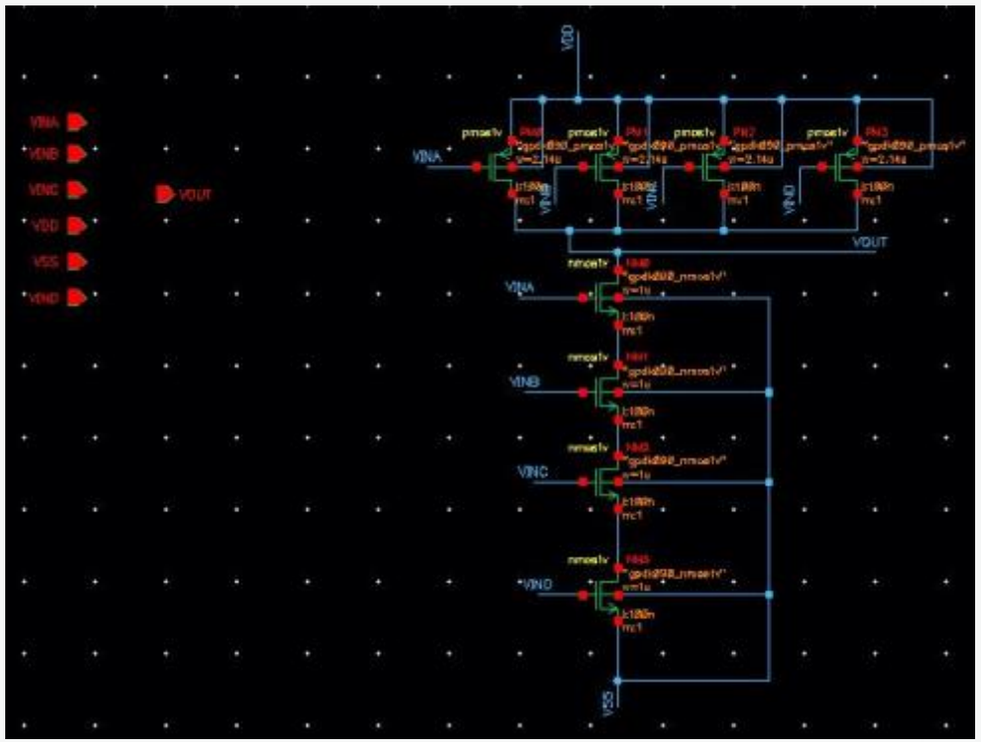
3-NAND GATE

Logic Gate

Schematic



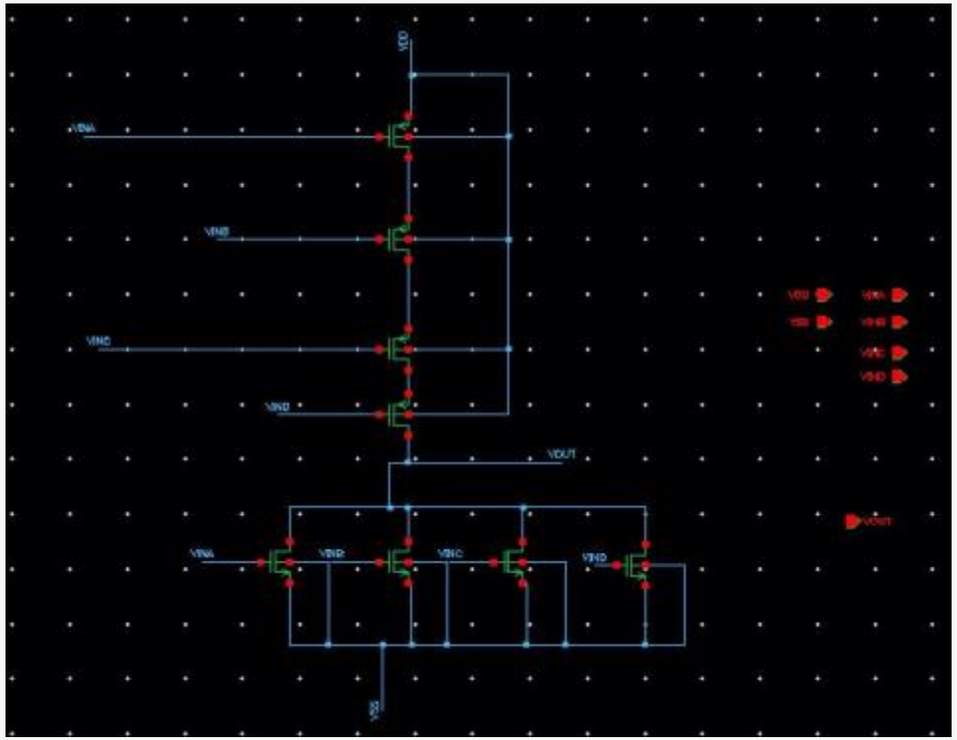
3-NOR GATE



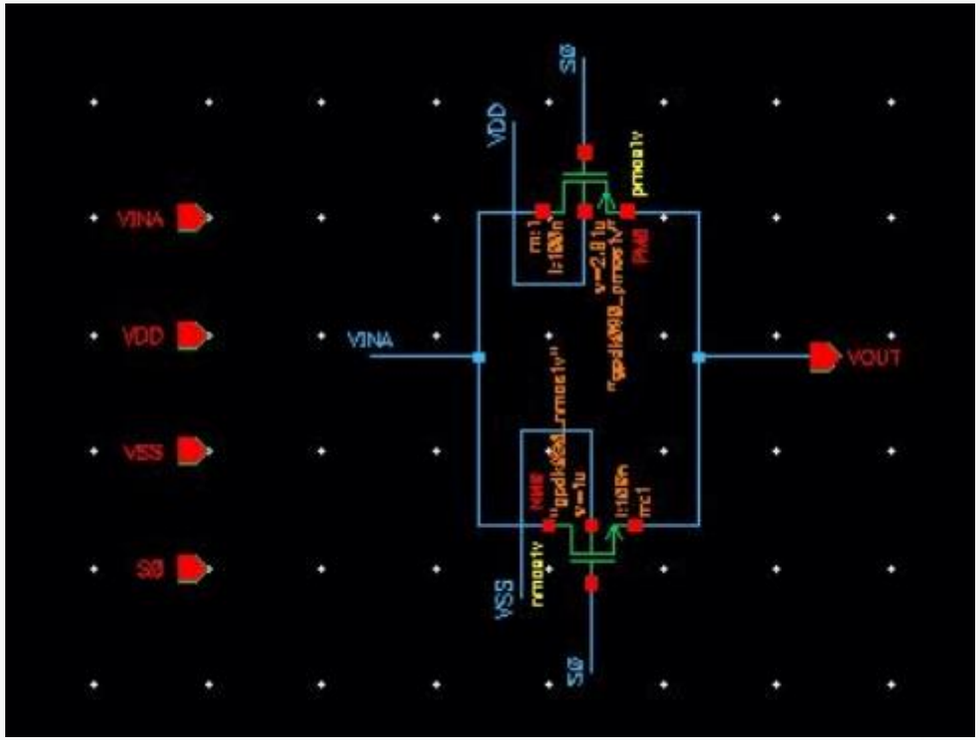
4-NAND GATE

Logic Gate

Schematic



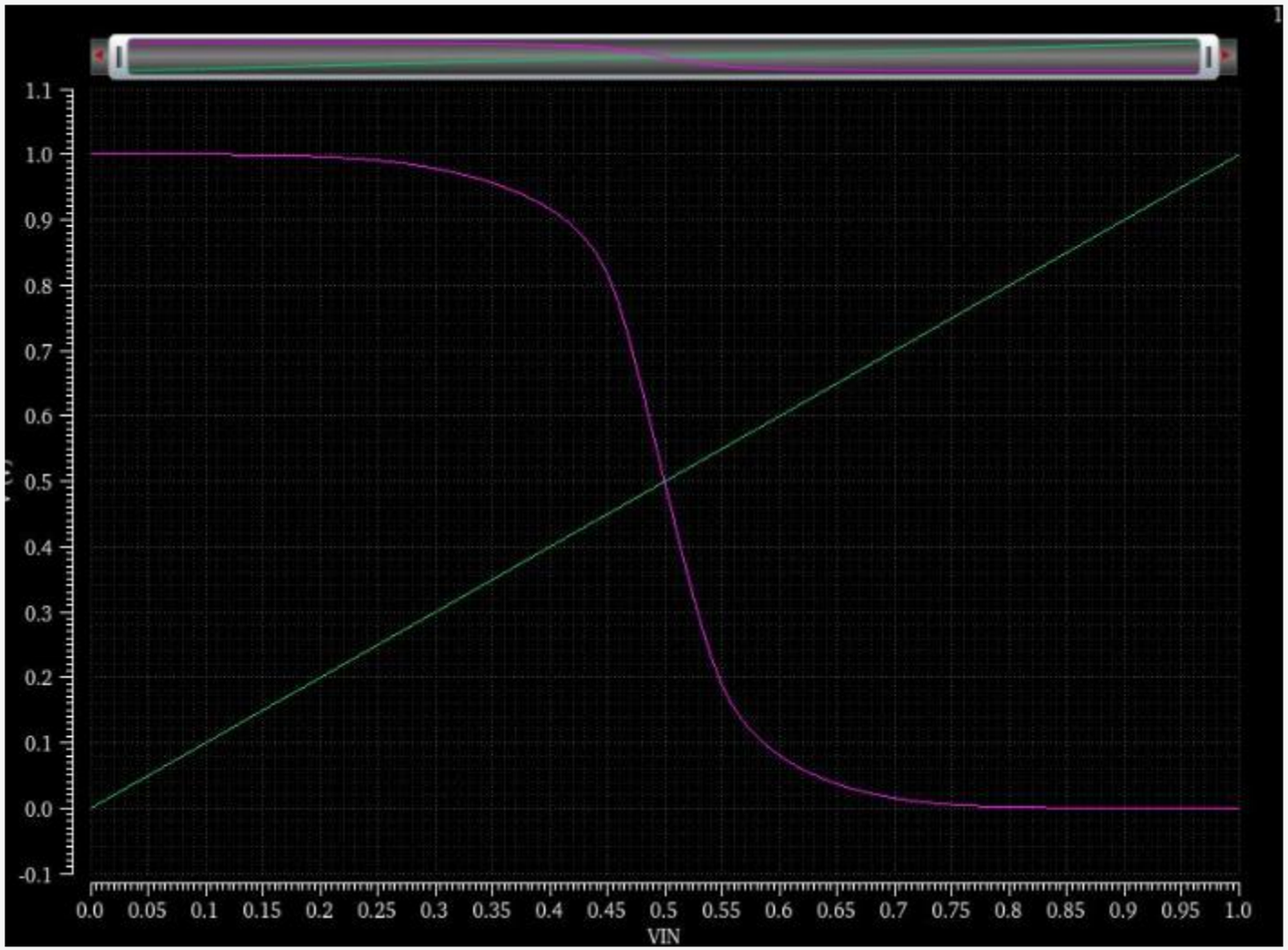
4-NOR GATE



SWITCH GATE

Logic Gate

Simulation & parameter(pmos width) correction



Simulaton

Logic gate

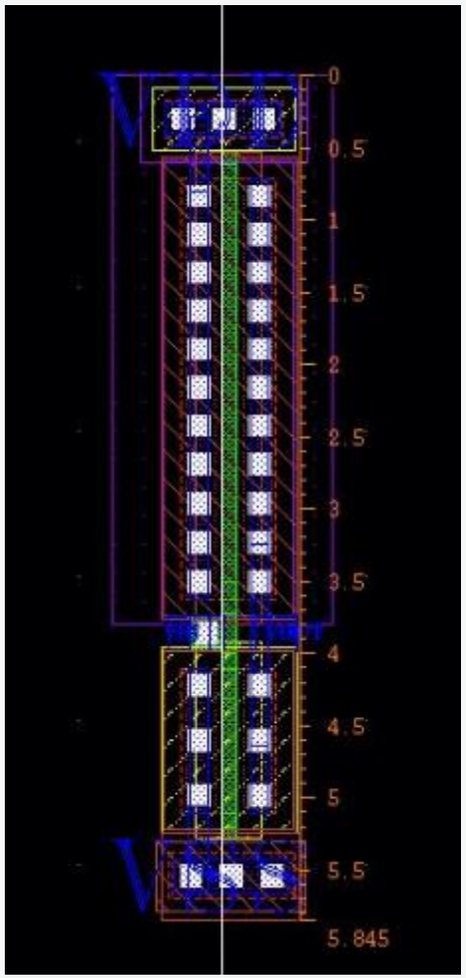
Simulation & parameter(pmos width) correction

	NOT	2NAND	2NOR	3NAND	3NOR	4NAND	4NOR
NMOS	1um	1um	1um	1um	1um	1um	1um
PMOS	2.91um	2.53um	3.99um	2.31um	5um	2.14um	5.96um

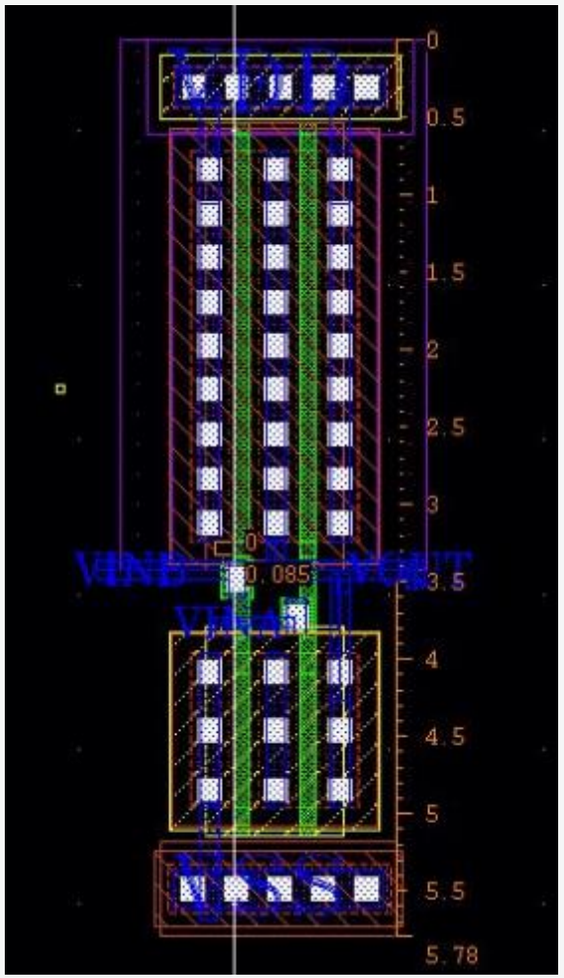
Corrected Width

Logic Gate

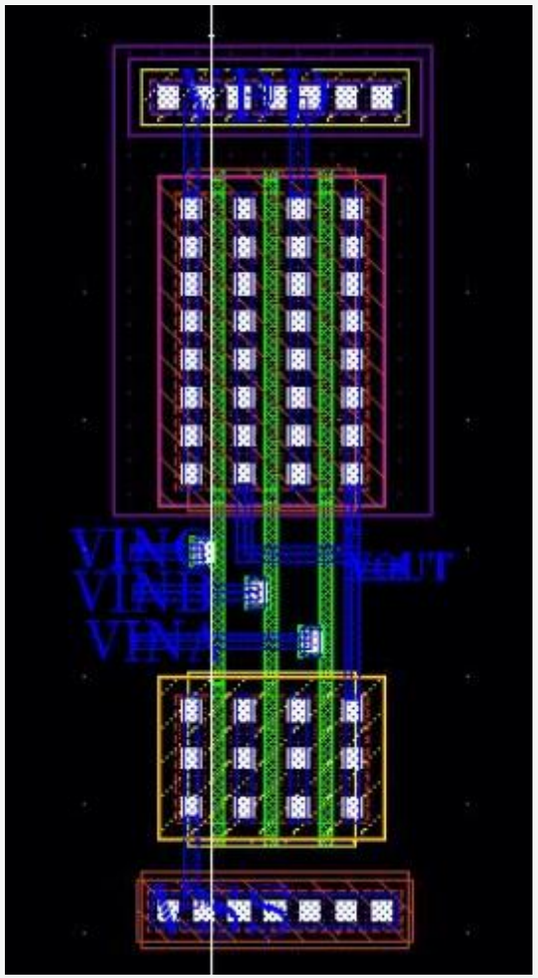
Layout



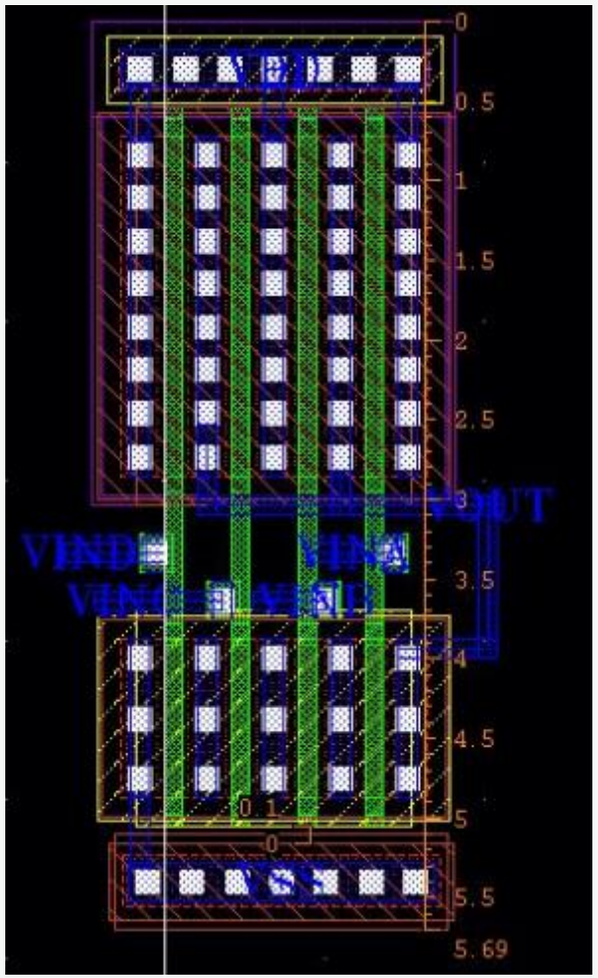
NOT



2NAND



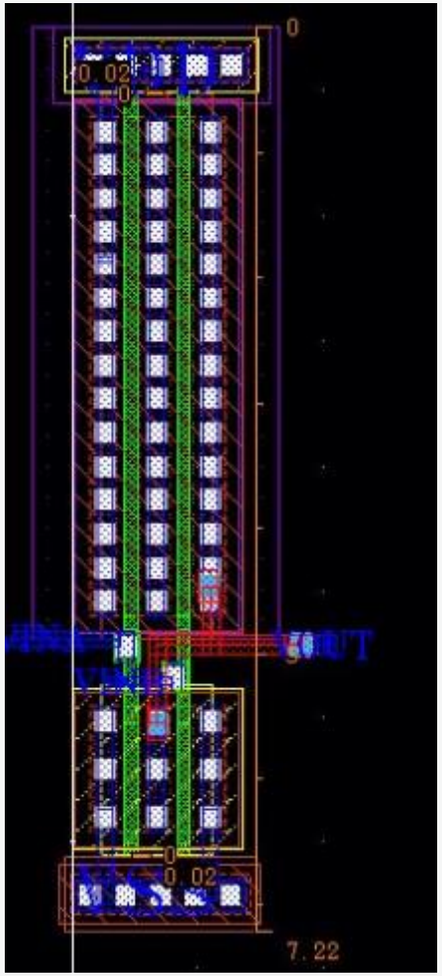
3NAND



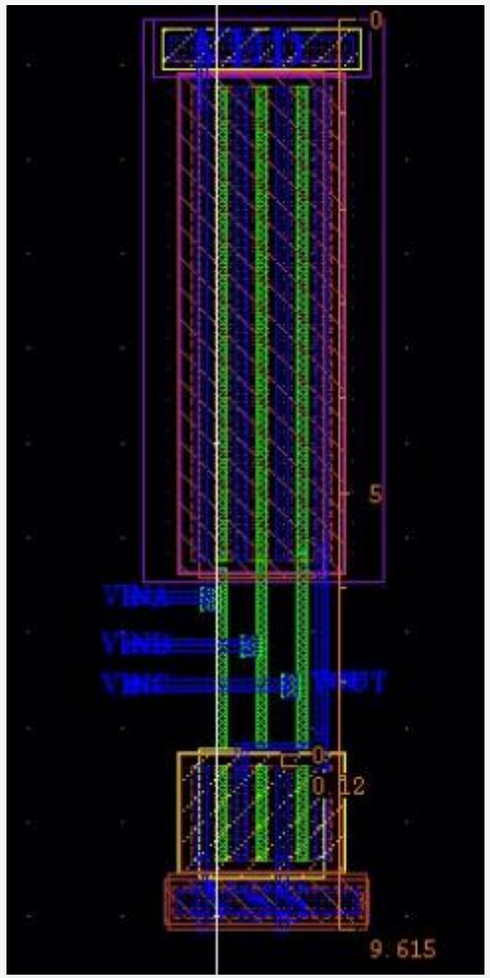
4NAND

Logic Gate

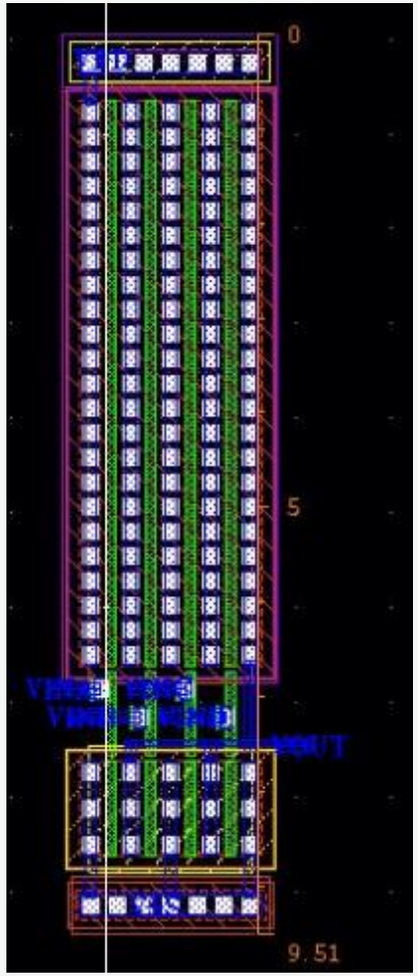
Layout



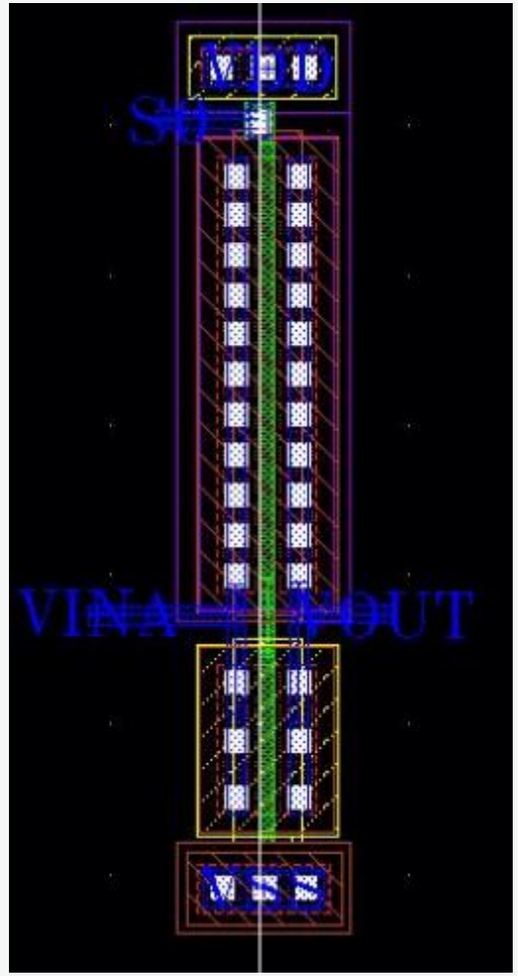
2NOR



3NOR



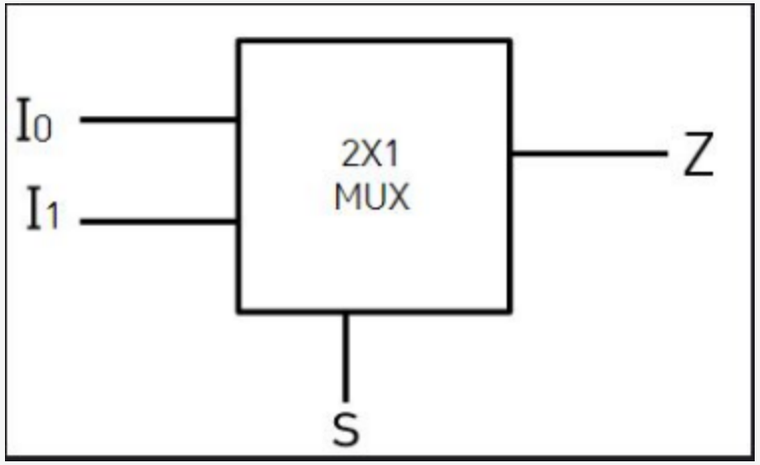
4NOR

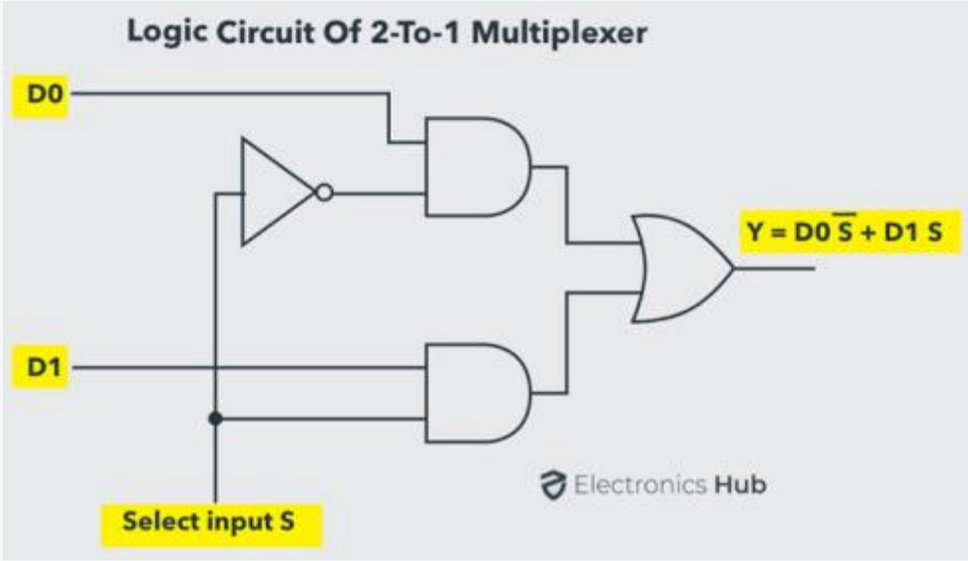


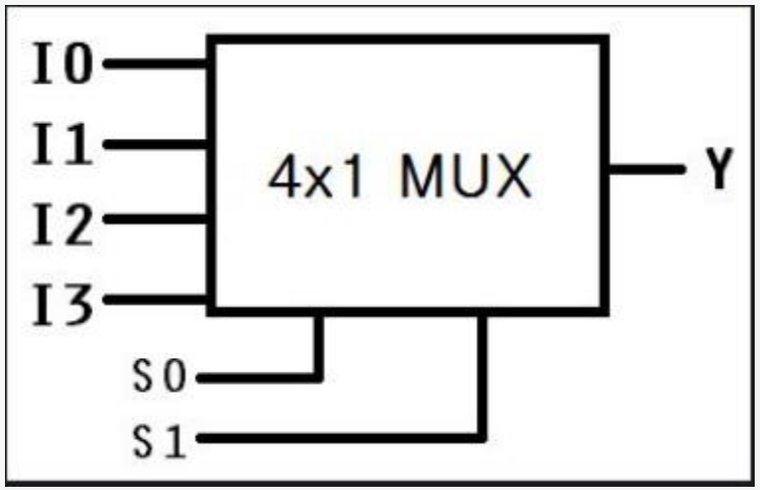
SWITCH

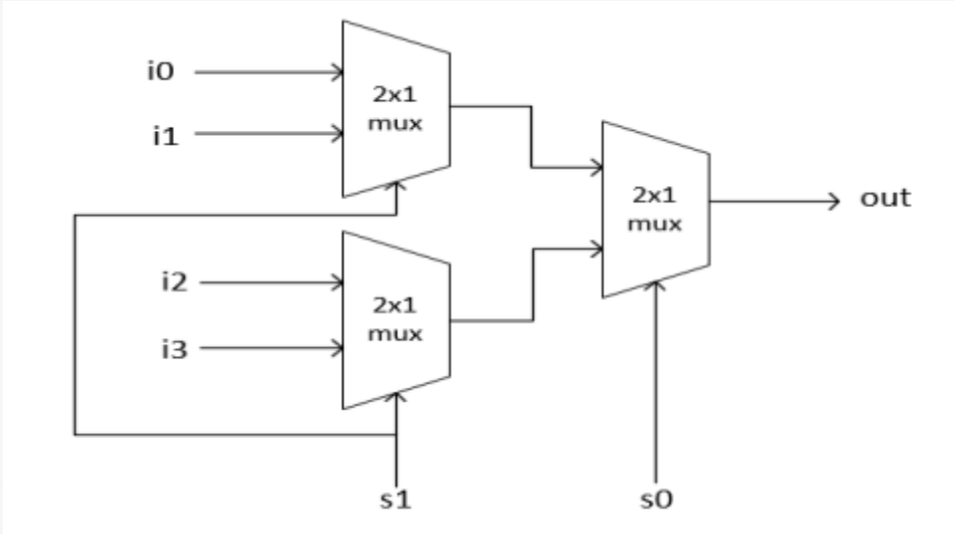
Multiplexer

What is multiplexer?



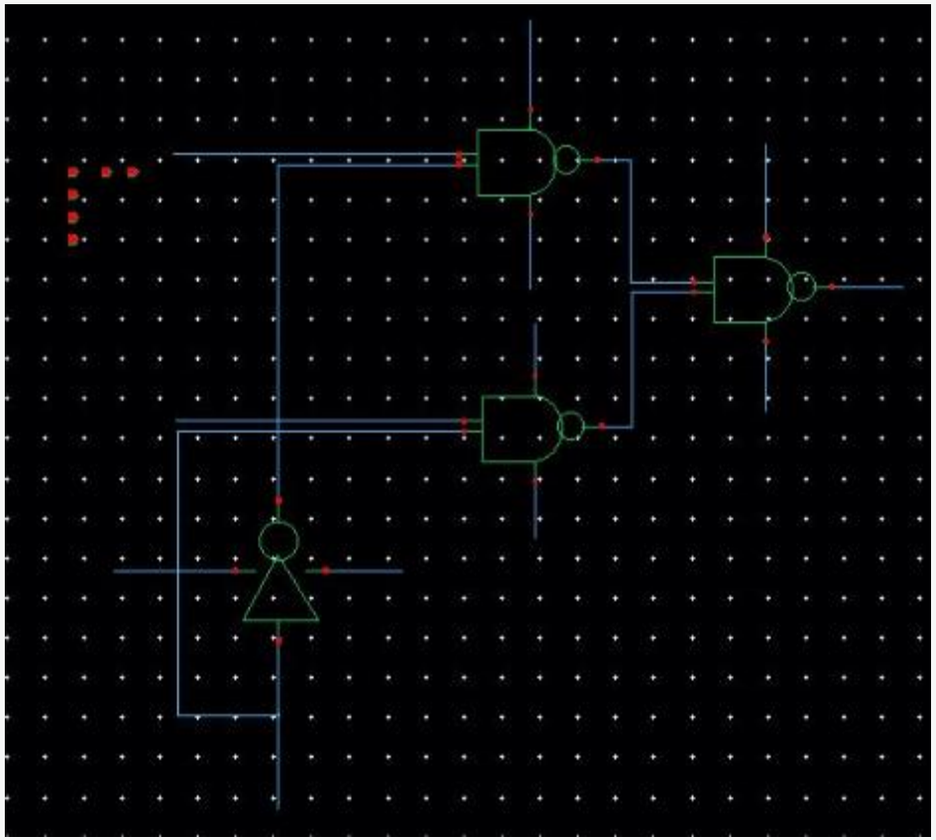




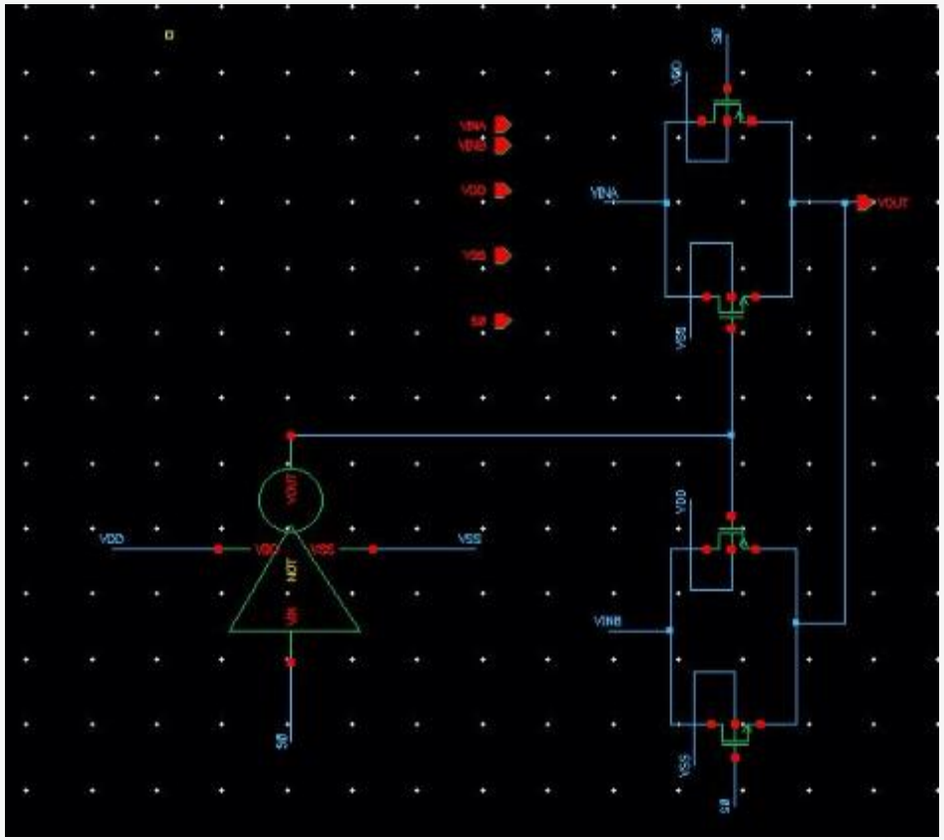


2X1 Multiplexer (vs transmission gate)

Schematic & Simulation



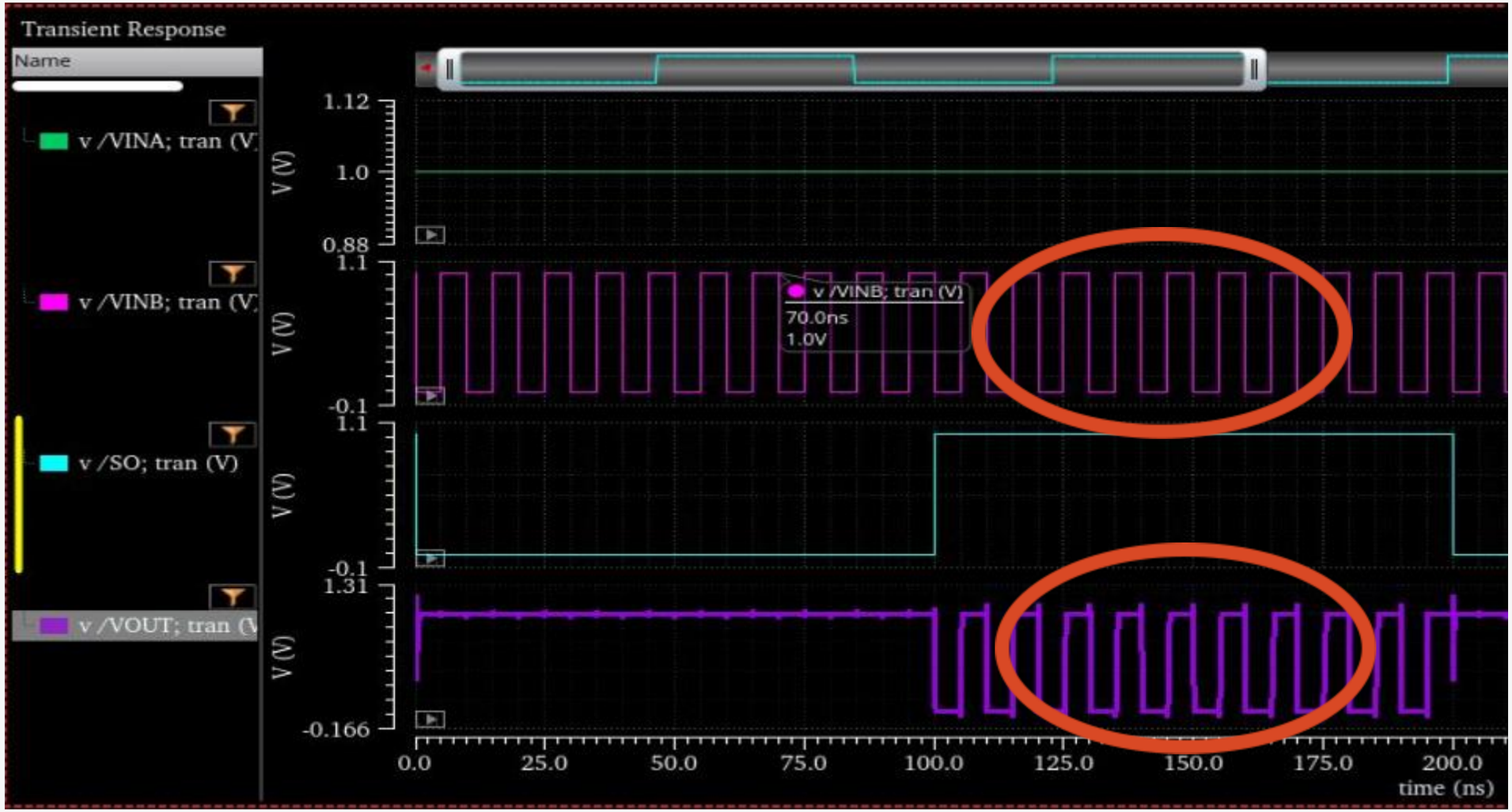
2X1 MUX



2X1 MUX(transmission gate)

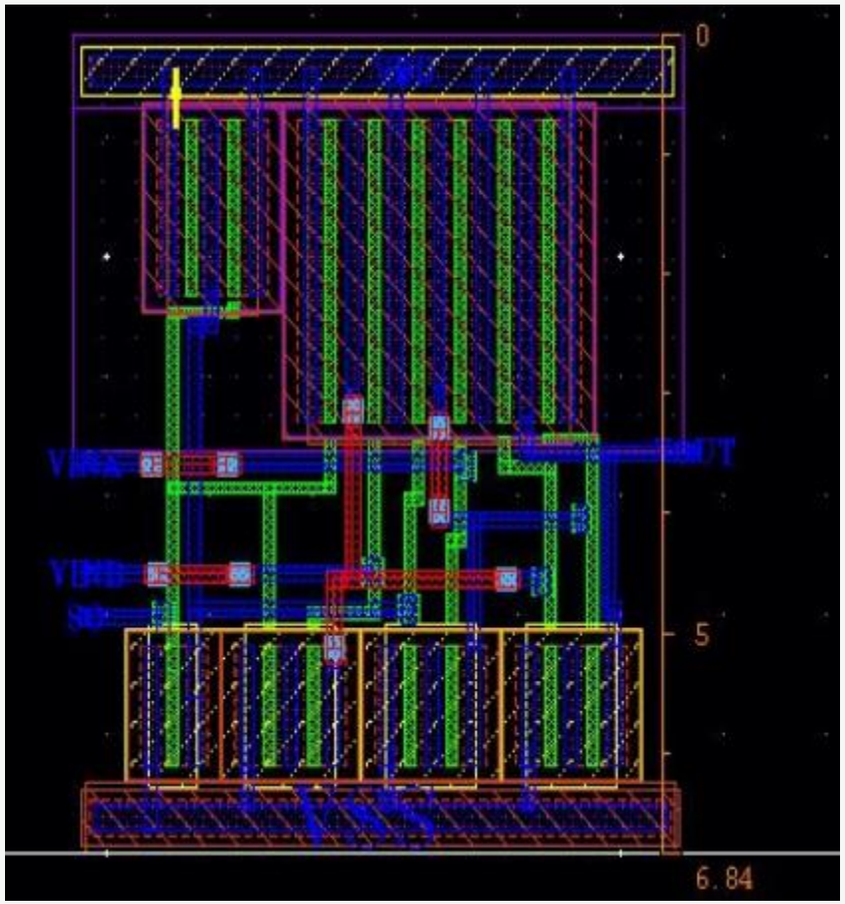
2X1 Multiplexer (vs transmission gate)

Simulation

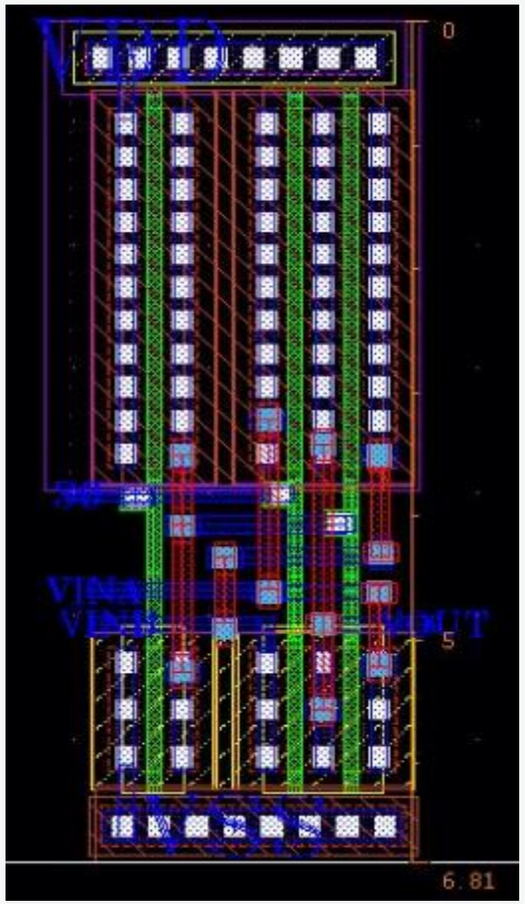


2X1 Multiplexer (vs transmission gate)

Layout



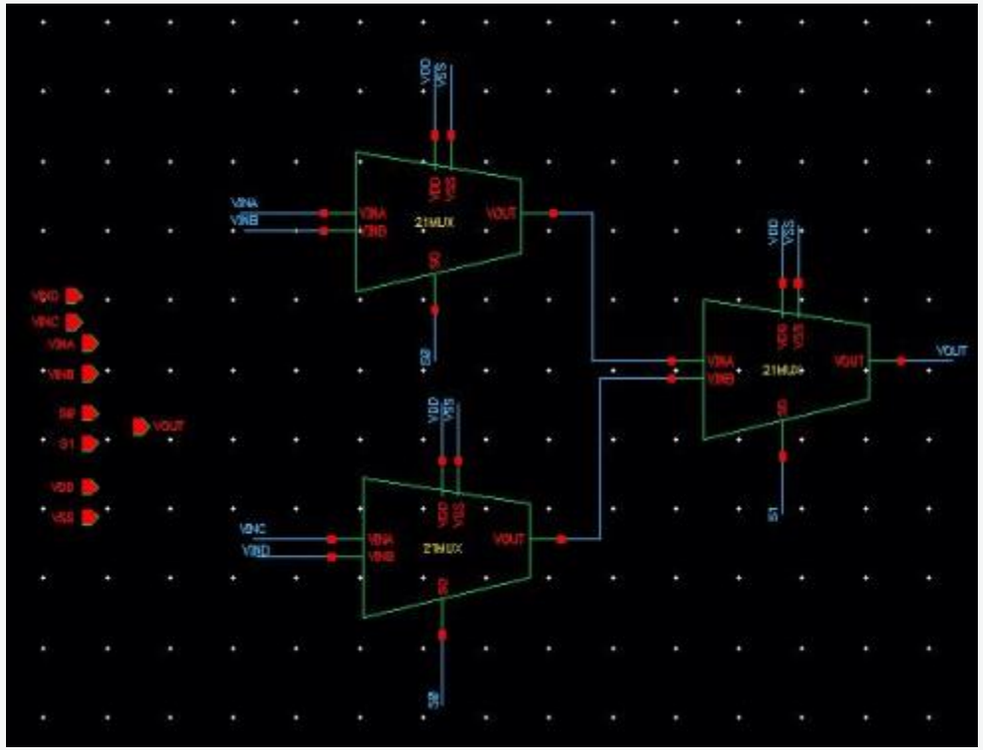
2X1 MUX



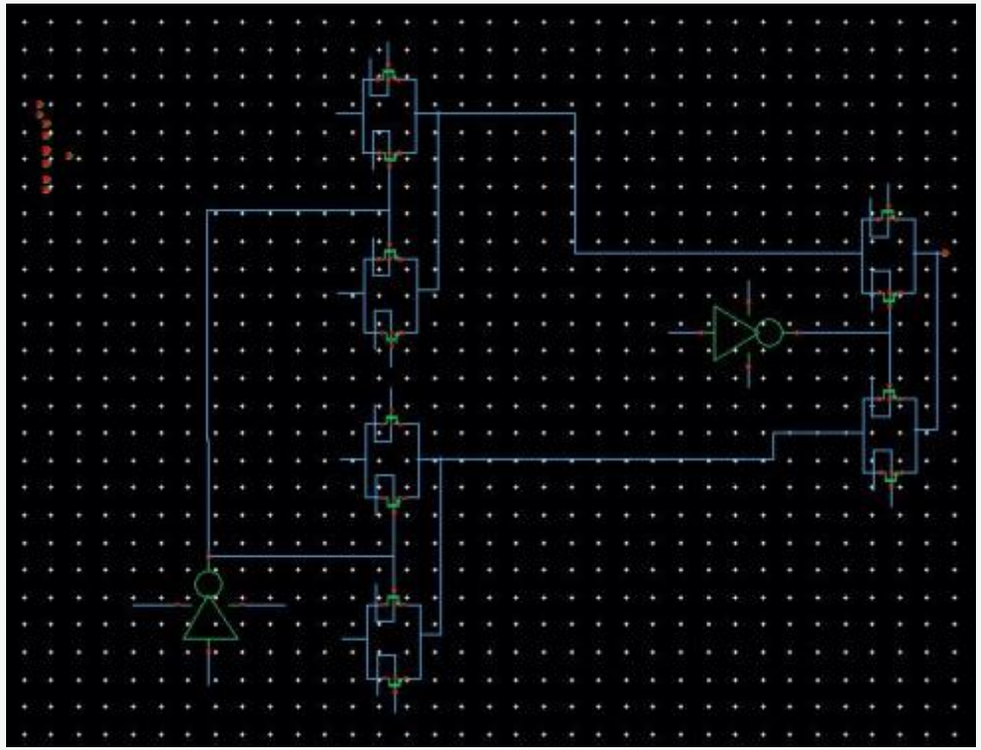
2X1 MUX(transmission gate)

4X1 Multiplexer (vs transmission gate)

Schematic & Simulation



4X1 MUX



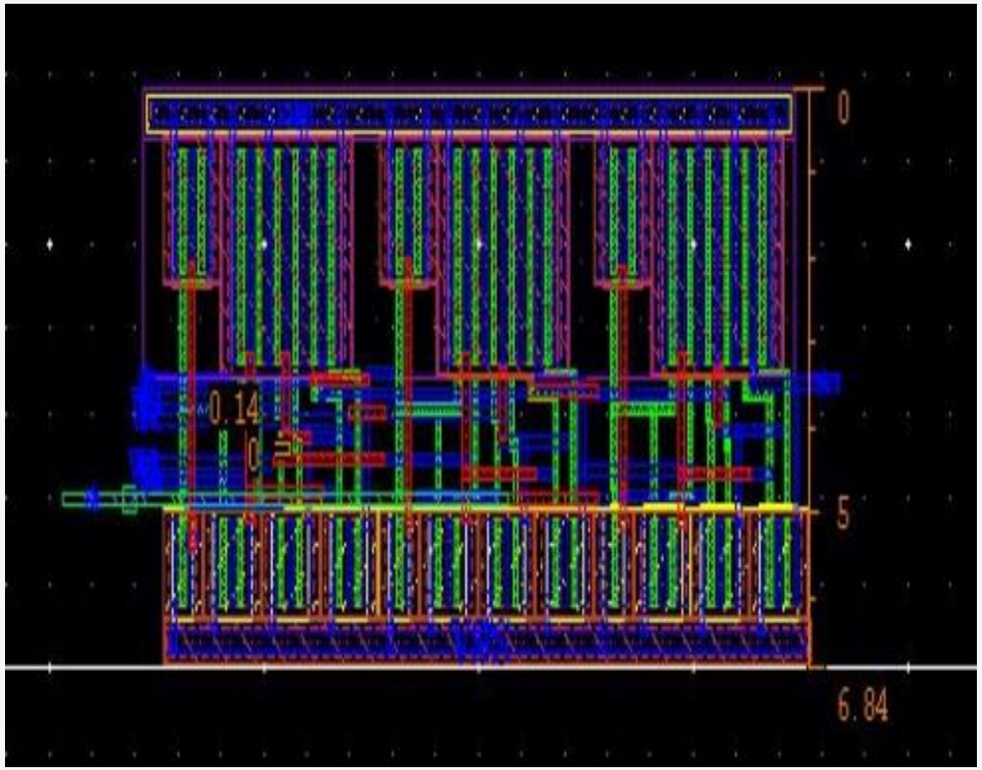
4X1 MUX(transmission gate)

4X1 Multiplexer (vs transmission gate)

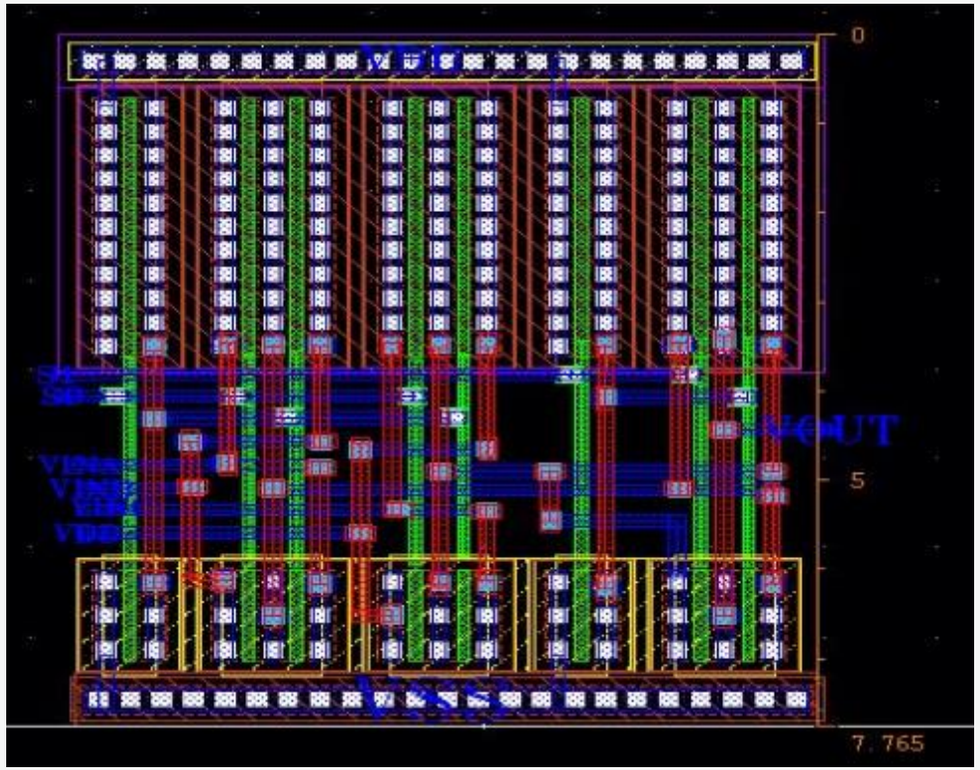
Simulation

4X1 Multiplexer (vs transmission gate)

Layout



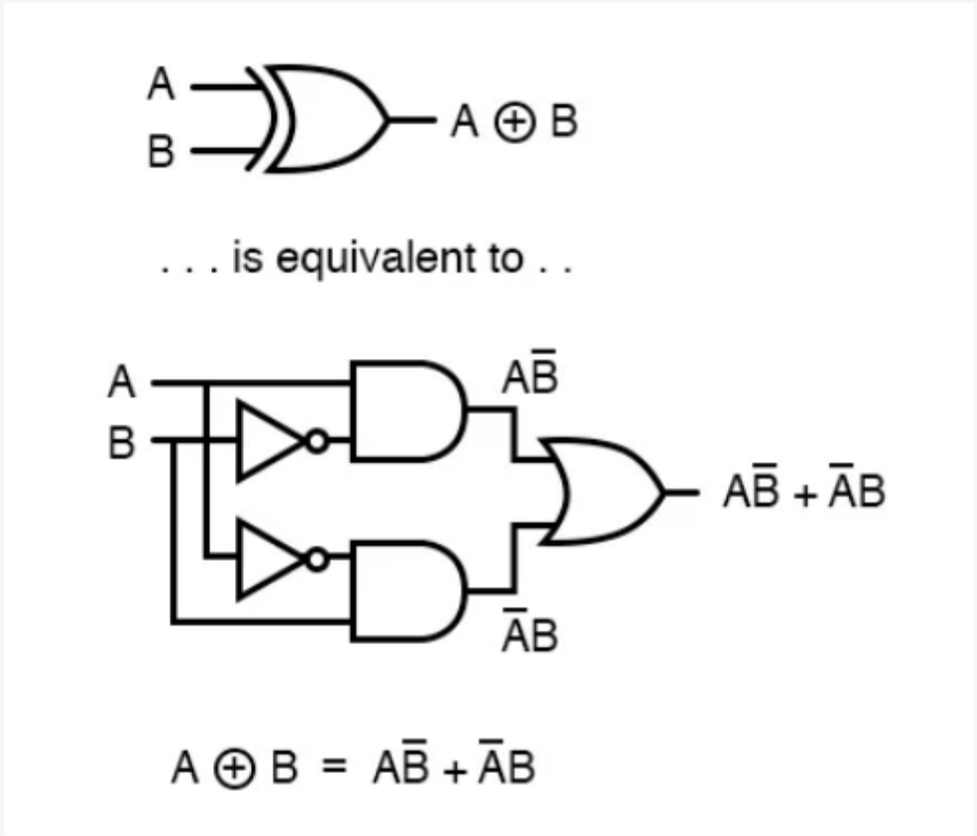
4X1 MUX

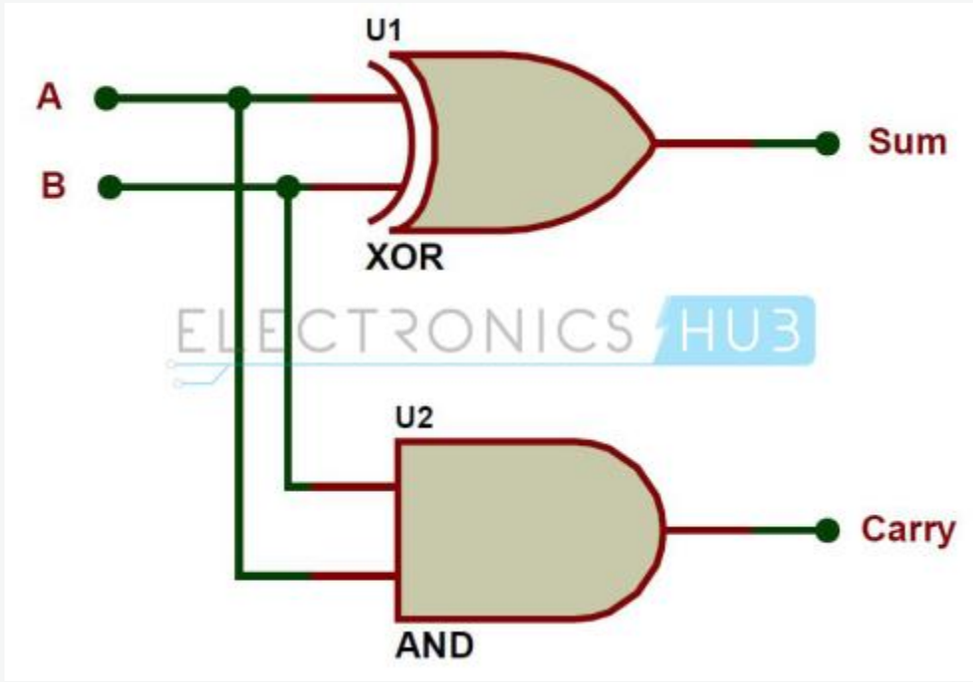


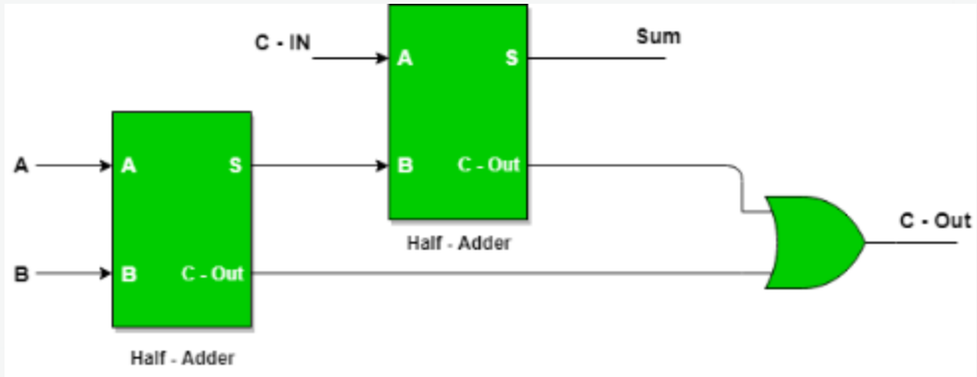
4X1 MUX(transmission gate)

Adder

What is adder?

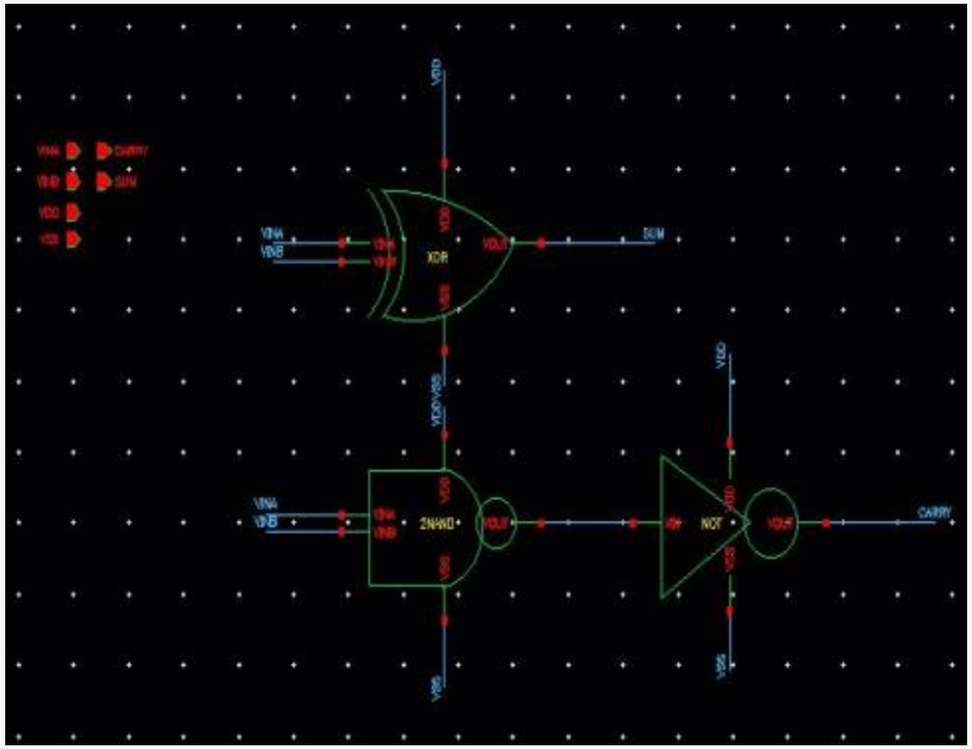




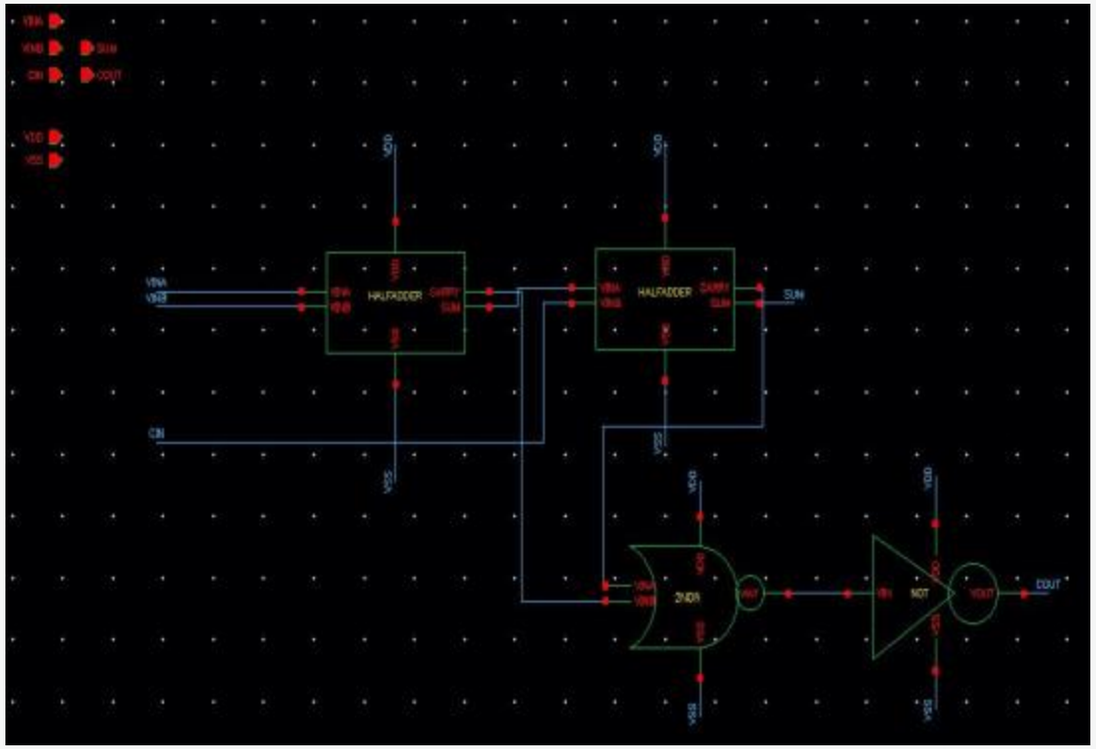


Adder(HA, FA)

Schematic & Simulation



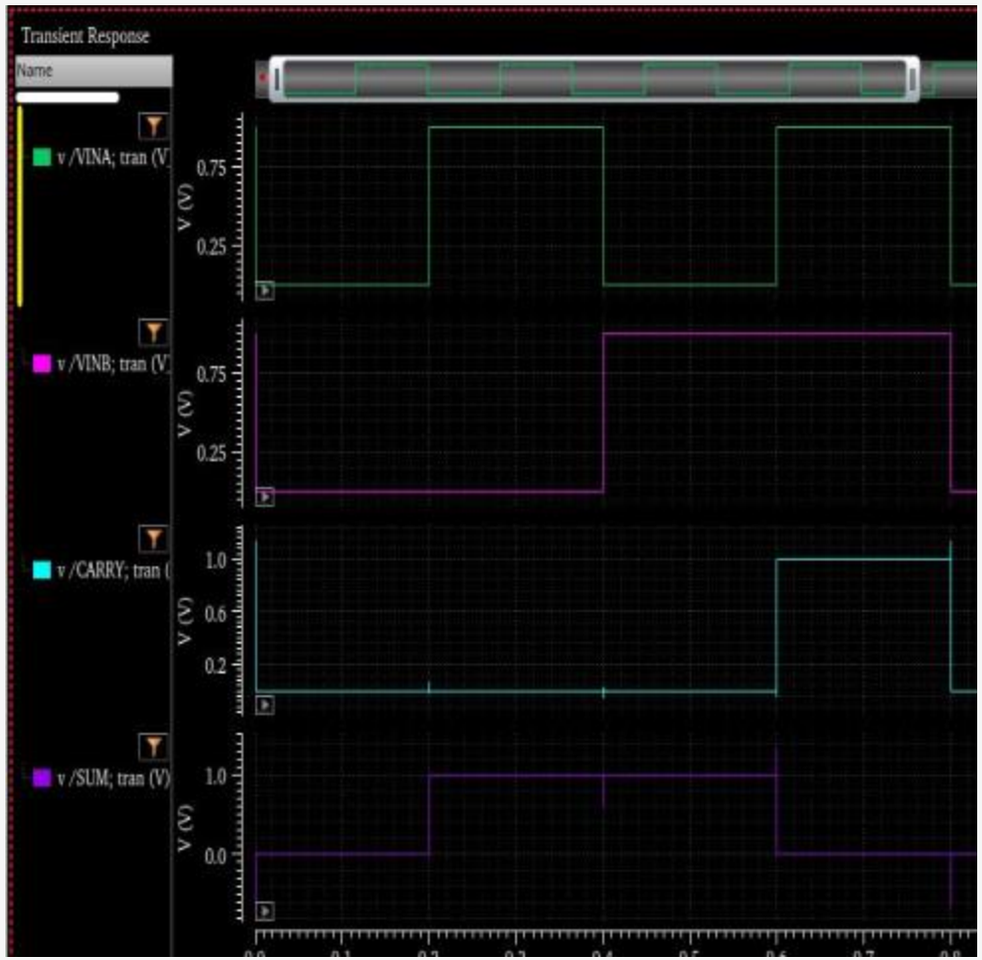
HALF ADDER



FULL ADDER

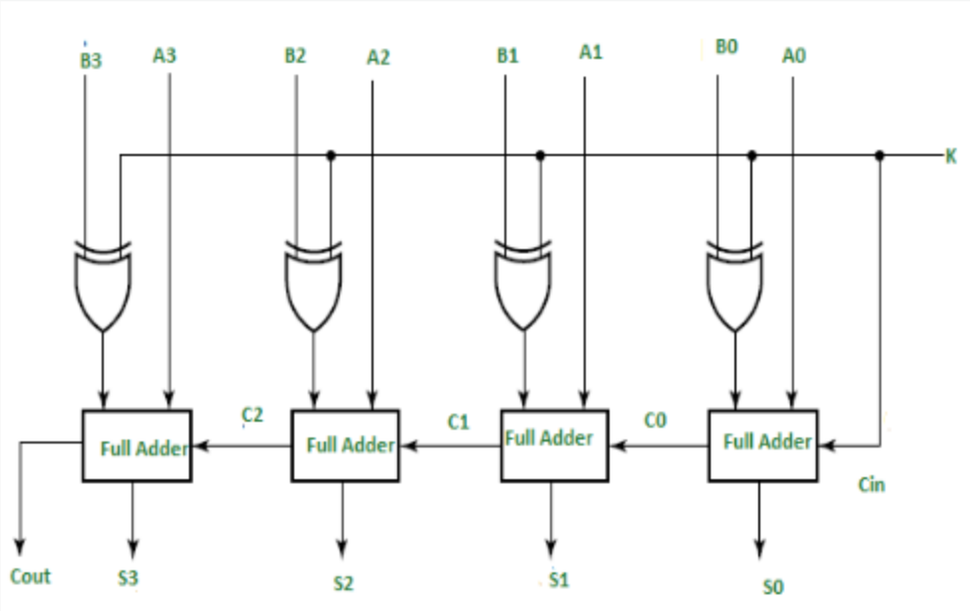
Adder(HA, FA)

Schematic & Simulation

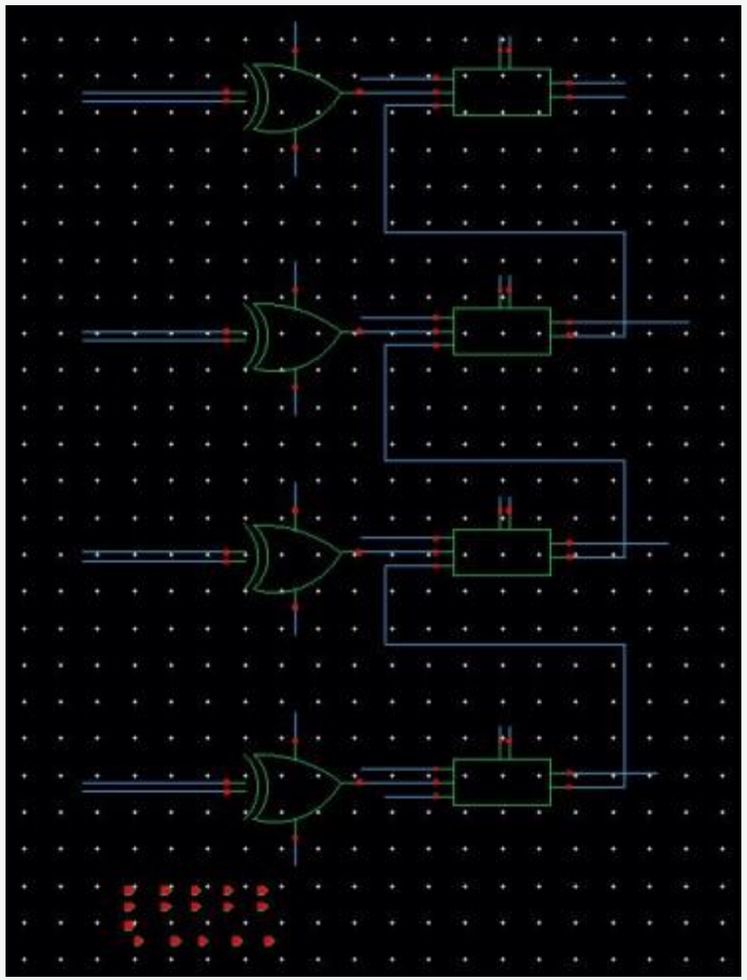


Adder(4_bit adder & substractor)

gate Circuit & Schematic



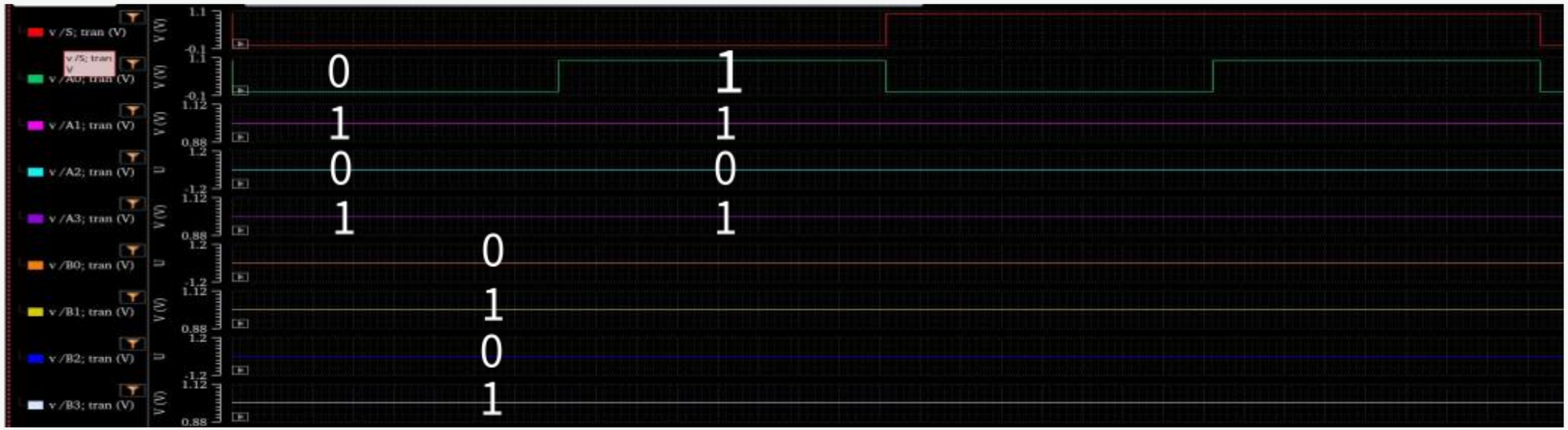
Circuit

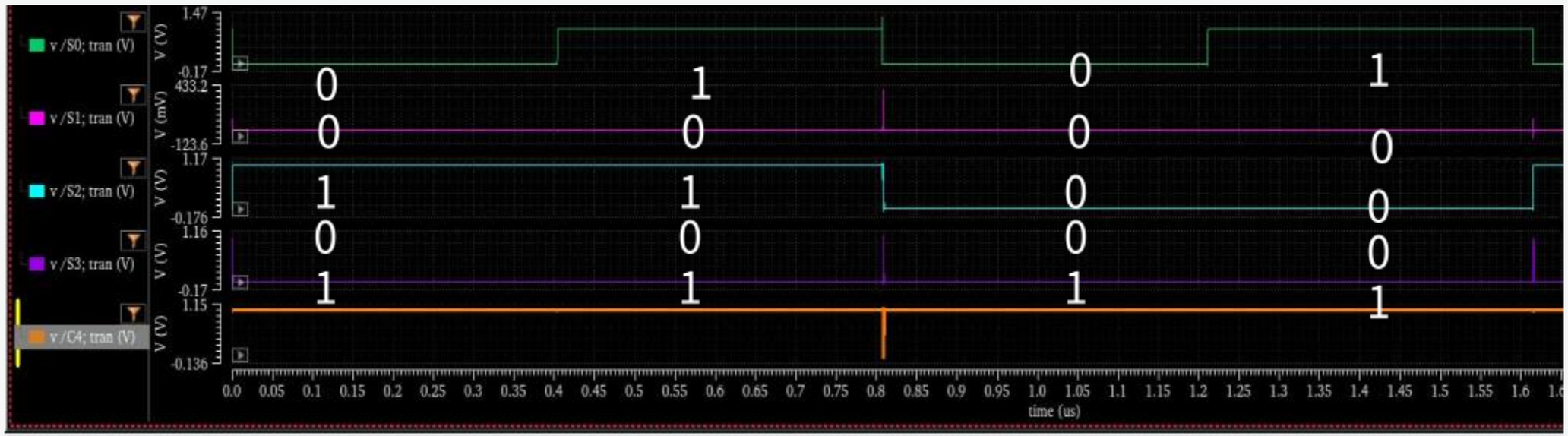


Schematic

Adder(4_bit adder & substractor)

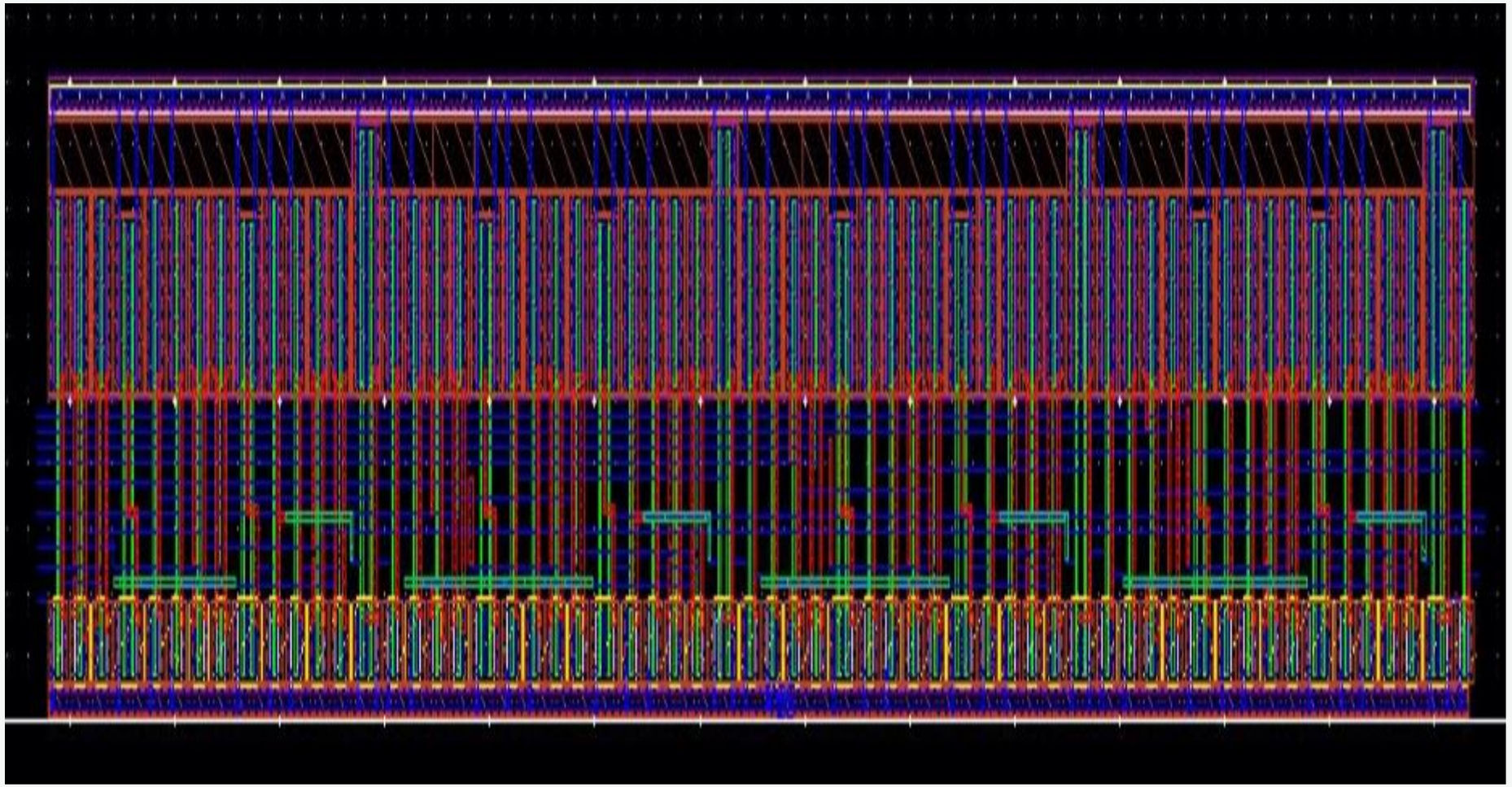
Simulation





Adder(4_bit adder & substractor)

Layout



Summary

Contact

Email

Phone

SNS