PCB 교육 정리

여름방학 단기 교육

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- PadStack 실습
- Constraint
- Routing
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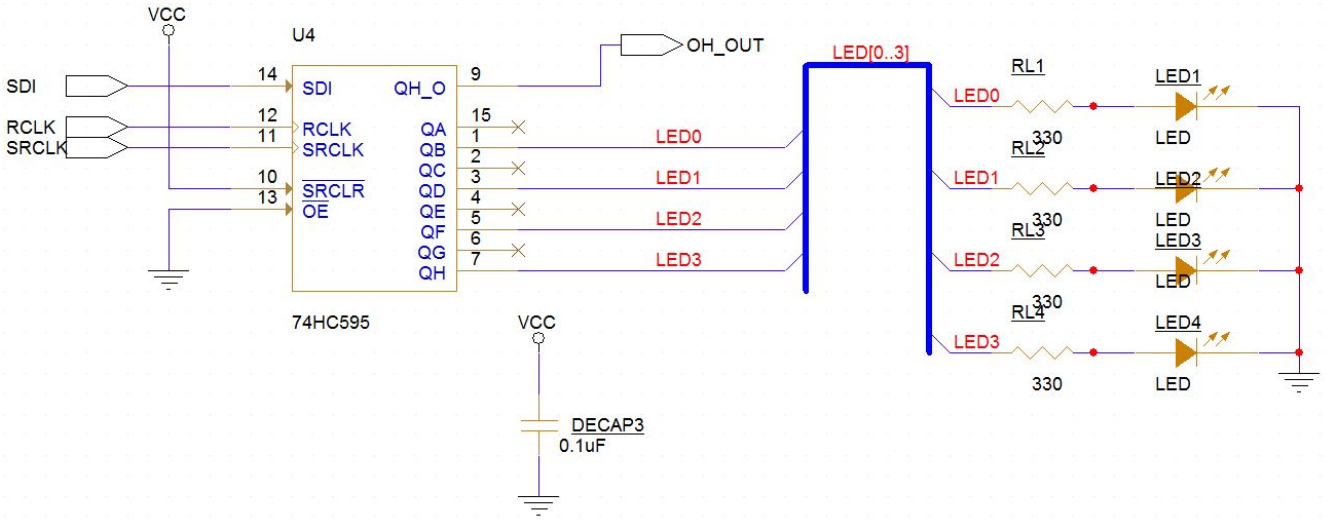
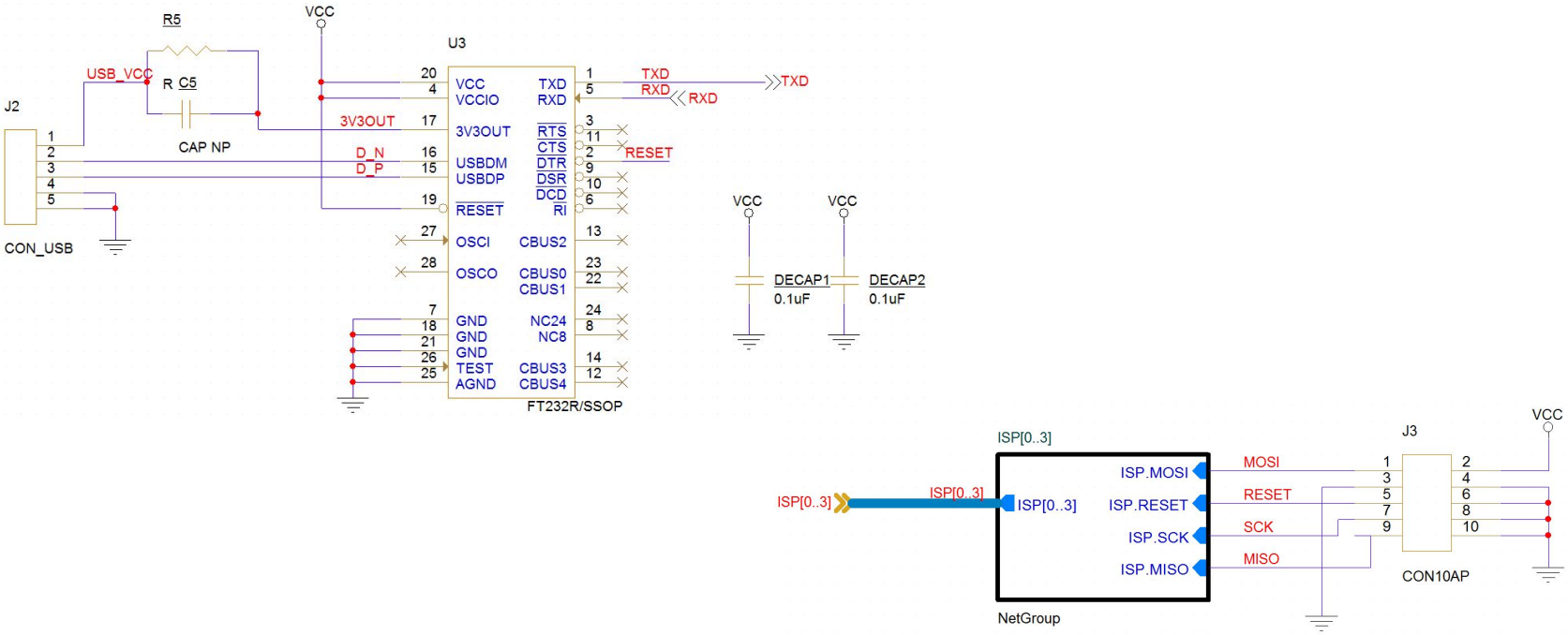
최종 기초 회로

LED_MODULE



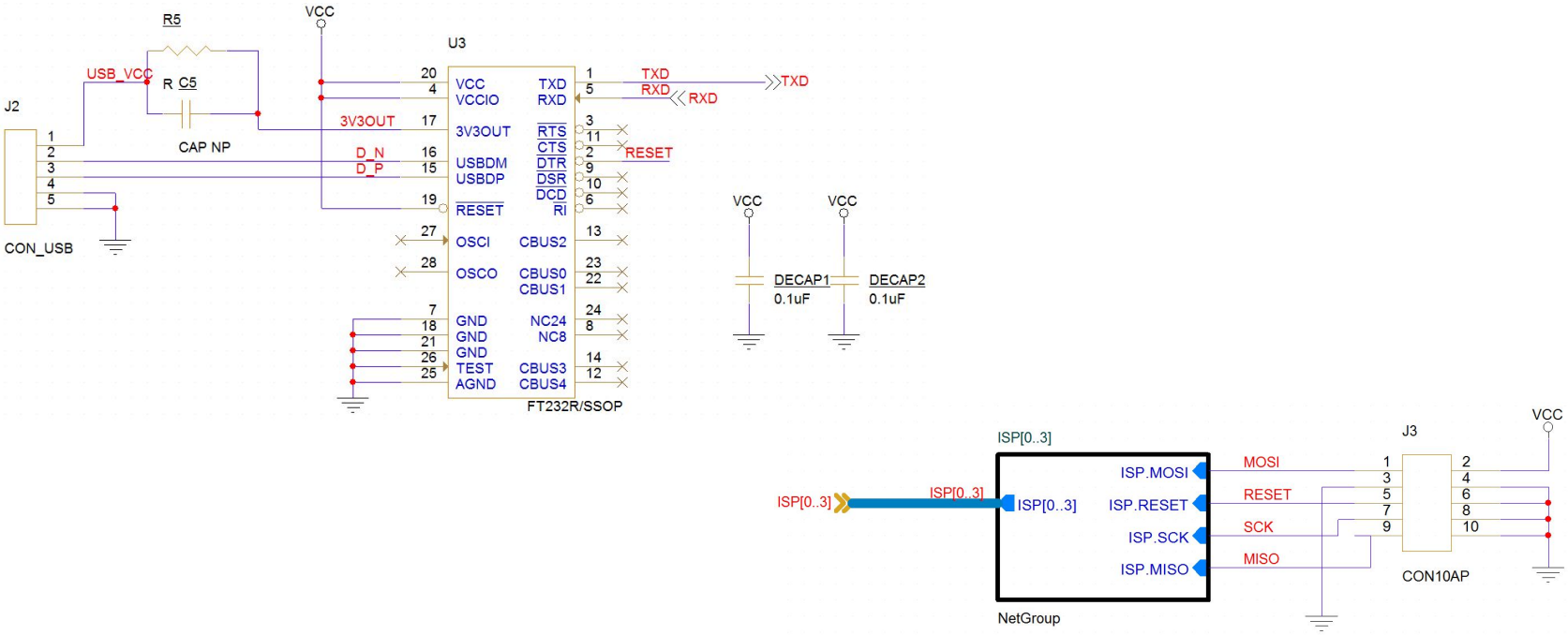
최종 기초 회로

MAIN_CONNECT



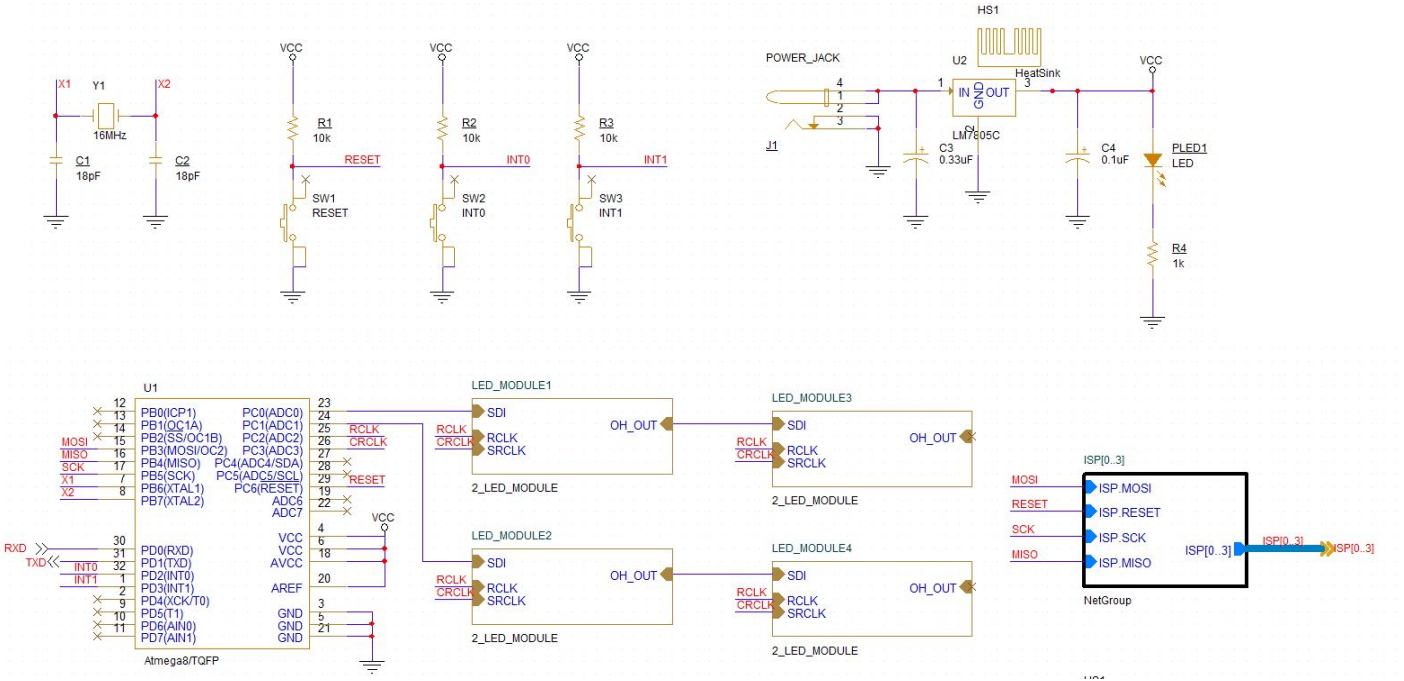
최종 기초 회로

MAIN_CONNECT



최종 기초 회로

MAIN TOP

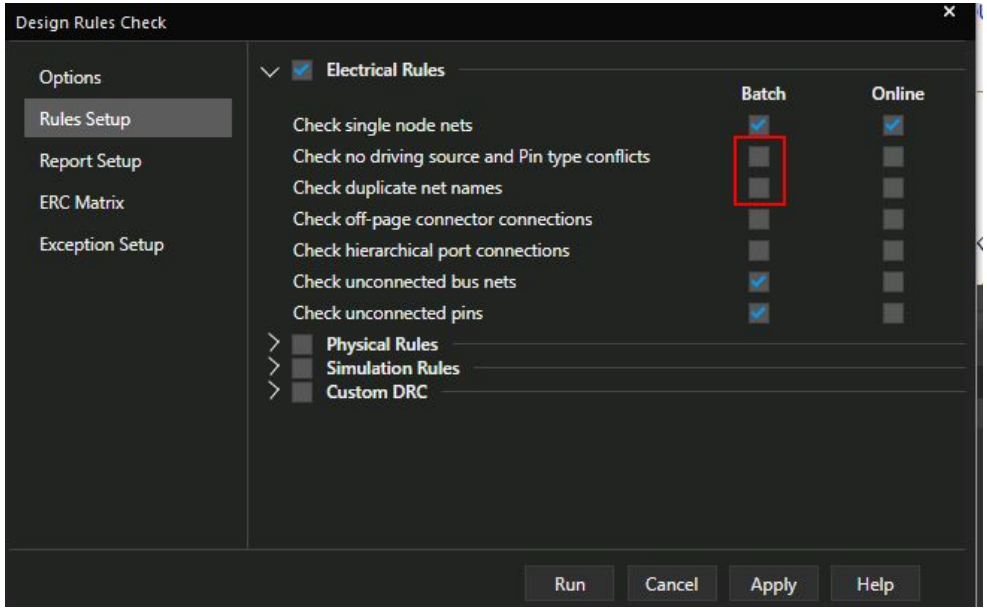


ERC CHECK

Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	U7,QH_O Output Connected to Input Port	2_LED_MODULE, MODULE (109.22, 50.80)	MODULE	1_MAIN₩LED_MODULE4	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	OH_OUT Input Port Connected to Output	2_LED_MODULE, MODULE (121.92, 45.72)	MODULE	1_MAIN₩LED_MODULE4	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	U6,QH_O Output Connected to Input Port	2_LED_MODULE, MODULE (109.22, 50.80)	MODULE	1_MAIN₩LED_MODULE3	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	OH_OUT Input Port Connected to Output	2_LED_MODULE, MODULE (121.92, 45.72)	MODULE	1_MAIN₩LED_MODULE4	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	U5,QH_O Output Connected to Input Port	2_LED_MODULE, MODULE (109.22, 50.80)	MODULE	1_MAIN₩LED_MODULE2	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	OH_OUT Input Port Connected to Output	2_LED_MODULE, MODULE (121.92, 45.72)	MODULE	1_MAIN₩LED_MODULE4	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	U4,QH_O Output Connected to Input Port	2_LED_MODULE, MODULE (109.22, 50.80)	MODULE	1_MAIN₩LED_MODULE1	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	OH_OUT Input Port Connected to Output	2_LED_MODULE, MODULE (121.92, 45.72)	MODULE	1_MAIN₩LED_MODULE4	No
Warning	Electrical	WARNING(ORCAP-1608): Net has no driving source	N12885	1_MAIN, 1_MAIN (160.02, 78.74)	1_MAIN	1_MAIN₩	No
Warning	Electrical	WARNING(ORCAP-1608): Net has no driving source	N04627	1_MAIN, 1_MAIN (160.02, 48.26)	1_MAIN	1_MAIN₩	No
Error	Electrical	ERROR(ORCAP-1628): Possible pin type conflict	U3,D₩T₩R₩ Output Connected to Output	1_MAIN, 2_CONNECT (157.48, 66.04)	2_CONNECT	1_MAIN₩	No

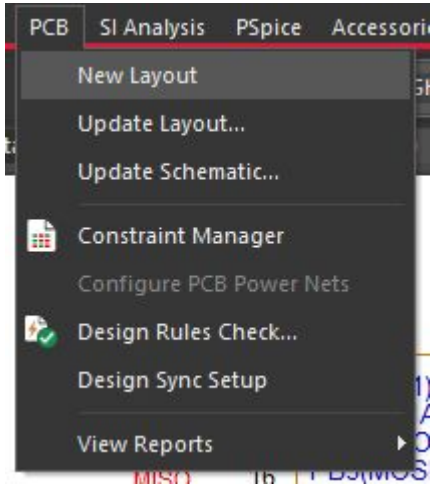
다양한 warning 및 error 발생

ERC CHECK



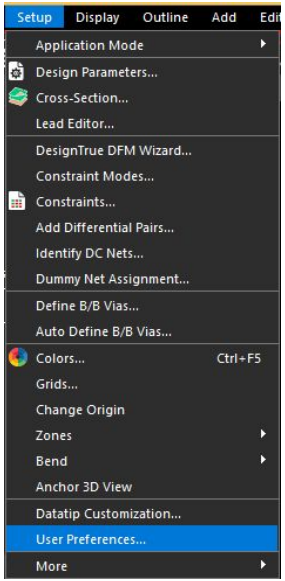
PCB layout 작업을 위해 DRC를 통과 해야한다. duplicate net names와 conflict checking은 비활성화 하였다.

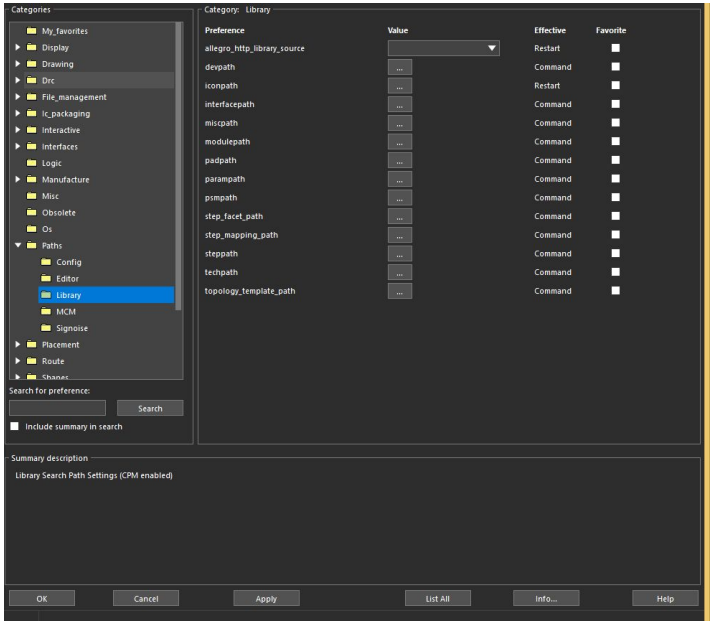
NET LIST 추출



New Layout을 통해 PCB 작업을 시작한다. 이 작업에서 오류가 있거나 버전이 낮은 툴의 경우는 netlist를 추출하여 import 하는 방식으로 수행하여야 한다.

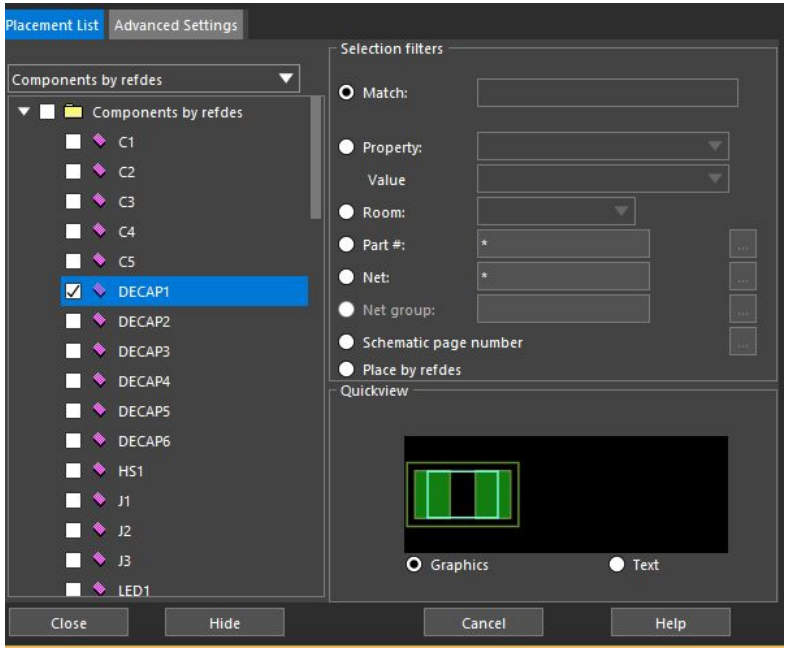
NET LIST 추출





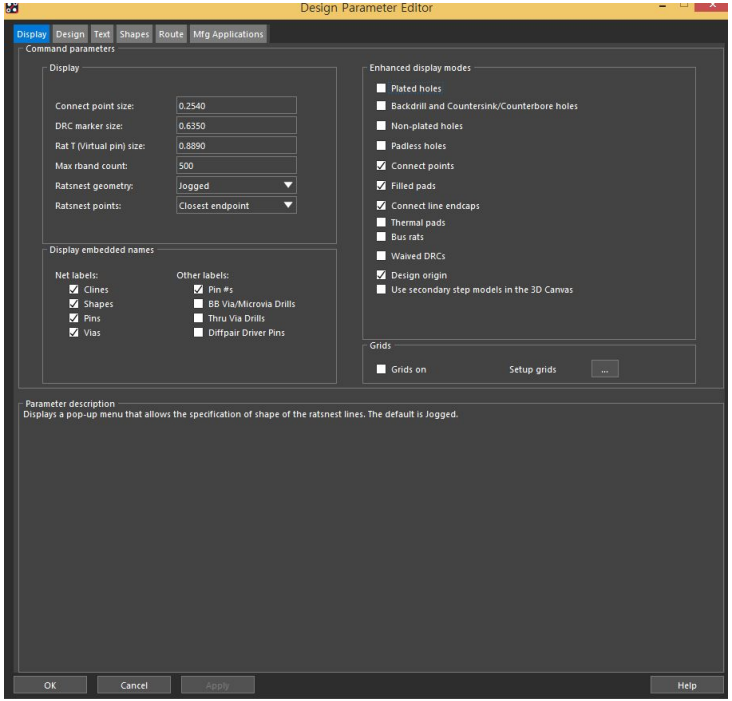
초기 단계에서는 각 부품의 이미지가 보이지 않는다. 따라서 library를 넣어줘야한다.
components의 symbol의 경로를 지정한다.

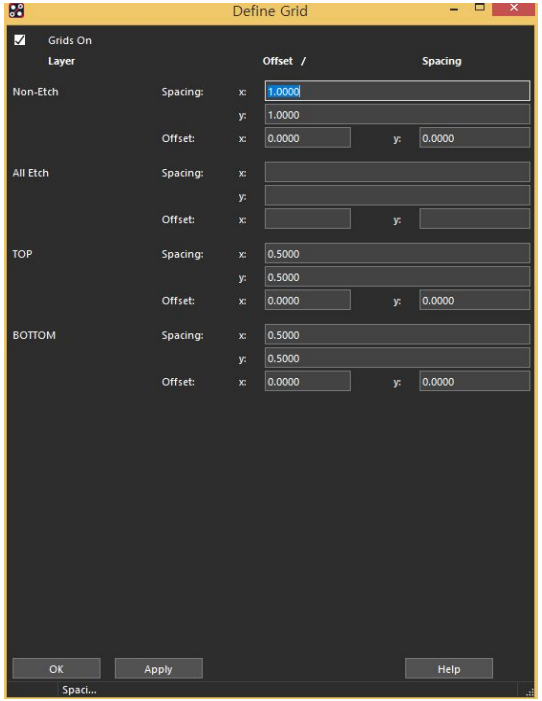
NET LIST 추출



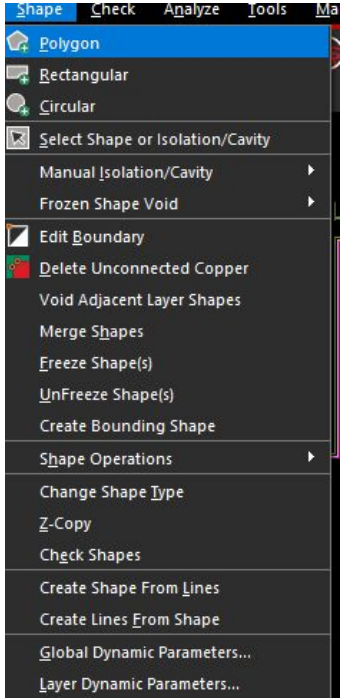
components manually에서 하나씩 확인 가능하다.

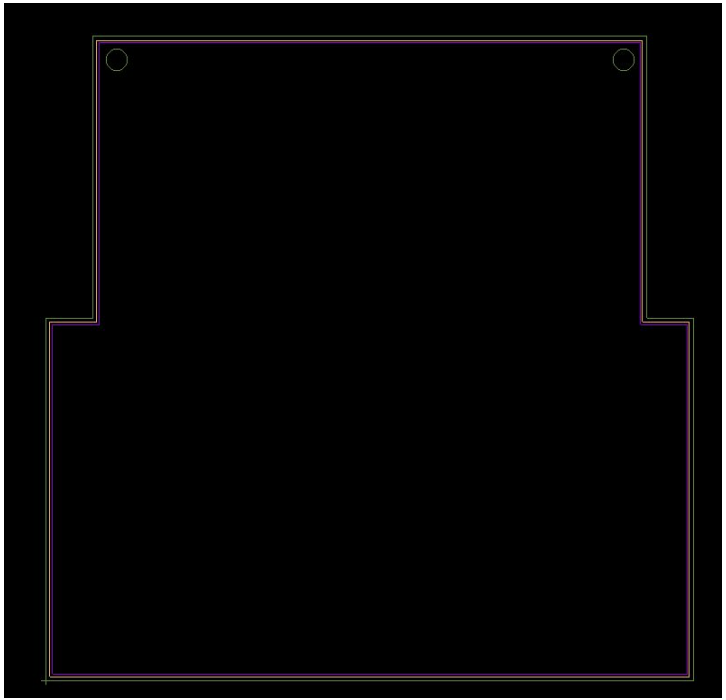
pcb 기초 setup


Design Parameter Editor
Display
Design
Text
Shapes
Route
Mfg Applications
Command parameters
Display
Connect point size:
0.2540
DRC marker size:
0.6350
Rat T (Virtual pin) size:
0.8890
Max rband count:
500
Ratsnest geometry:
Jogged
Ratsnest points:
Closest endpoint
Display embedded names
Net labels:
Clines
Shapes
Pins
Vias
Other labels:
Pin #s
BB Via/Microvia Drills
Thru Via Drills
Diffpair Driver Pins
Enhanced display modes
Plated holes
Backdrill and Countersink/Counterbore holes
Non-plated holes
Padless holes
Connect points
Filled pads
Connect line endcaps
Thermal pads
Bus rats
Waived DRCs
Design origin
Use secondary step models in the 3D Canvas
Grids
Grids on
Setup grids
...
Parameter description
Displays a pop-up menu that allows the specification of shape of the ratsnest lines. The default is Jogged.
OK
Cancel
Apply
Help


Define Grid
Grids On
Layer
Offset /
Spacing
Non-Etch
Spacing:
x:
1.0000
y:
1.0000
Offset:
x:
0.0000
y:
0.0000
All Etch
Spacing:
x:
y:
Offset:
x:
y:
TOP
Spacing:
x:
0.5000
y:
0.5000
Offset:
x:
0.0000
y:
0.0000
BOTTOM
Spacing:
x:
0.5000
y:
0.5000
Offset:
x:
0.0000
y:
0.0000
OK
Apply
Help
Spaci...

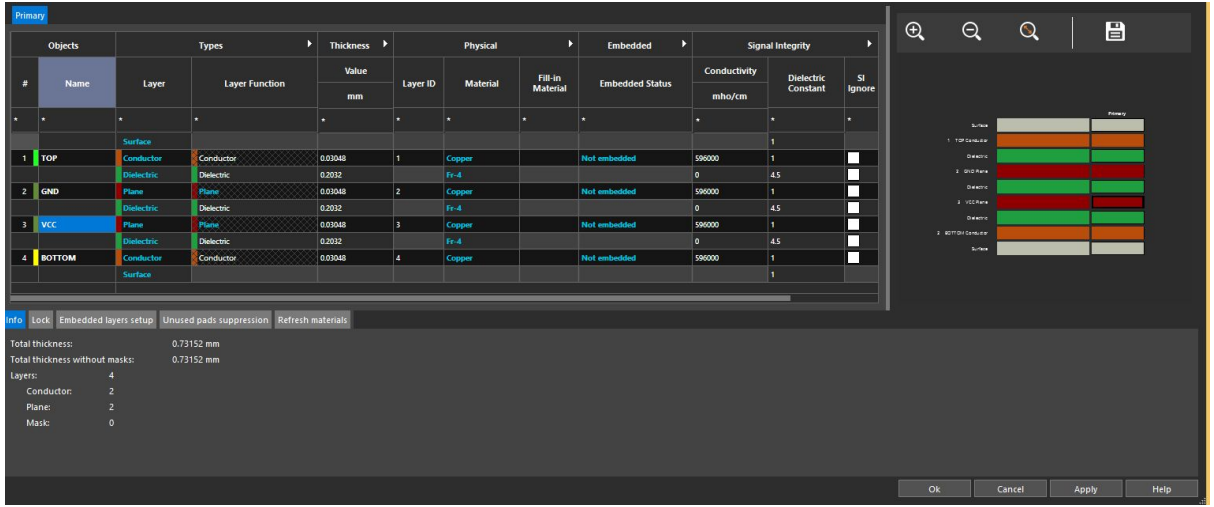
pcb 실습

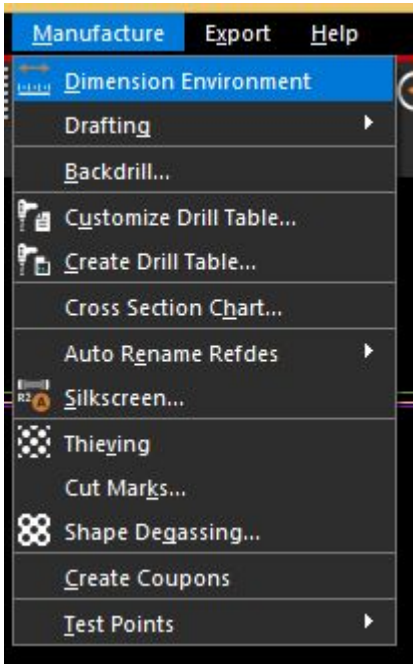




polygon toolbar를 사용하여 좌표 입력후 다음과 같은 outline을 그린다. z-copy를 통해 package keepin과 route keepin을 진행한다

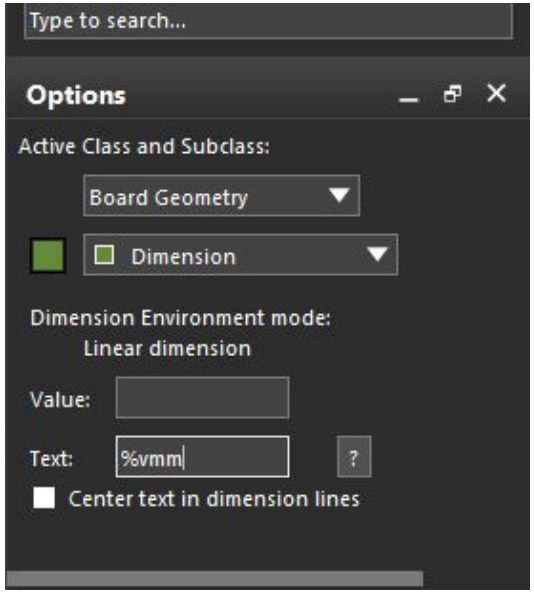
pcb 실습

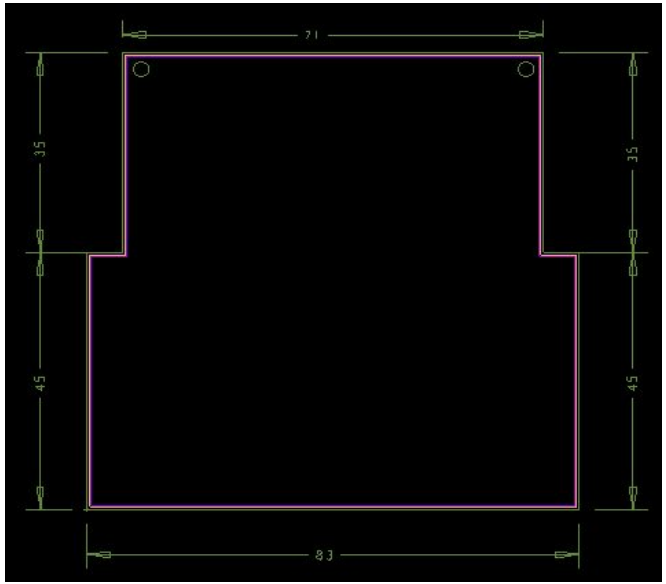




cross section 층 추가
TOP, GND, VCC, BOTTOM 총 4개의 층으로 작업한다.
Via를 통해 배선하게 된다.

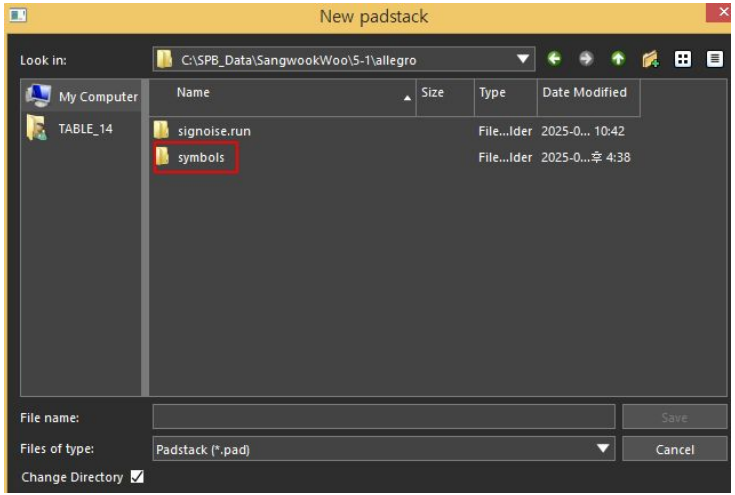
pcb 실습

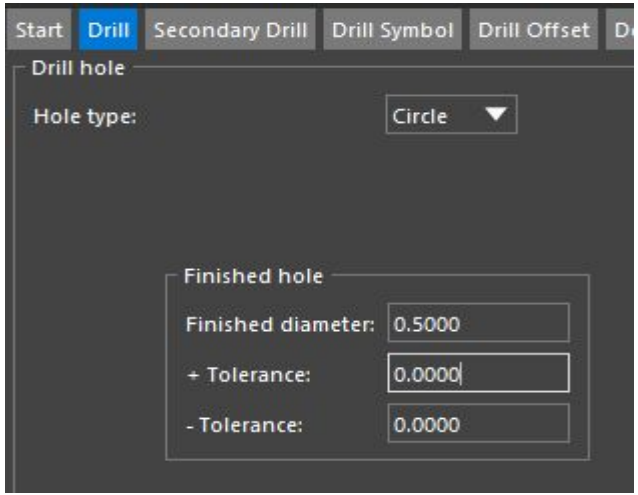




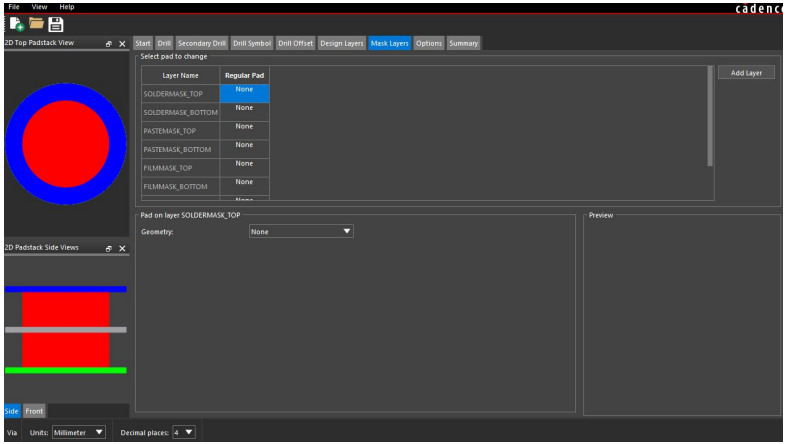
dimension enviroment 활성화 후 paramteter 설정 후 양 끝점 설정

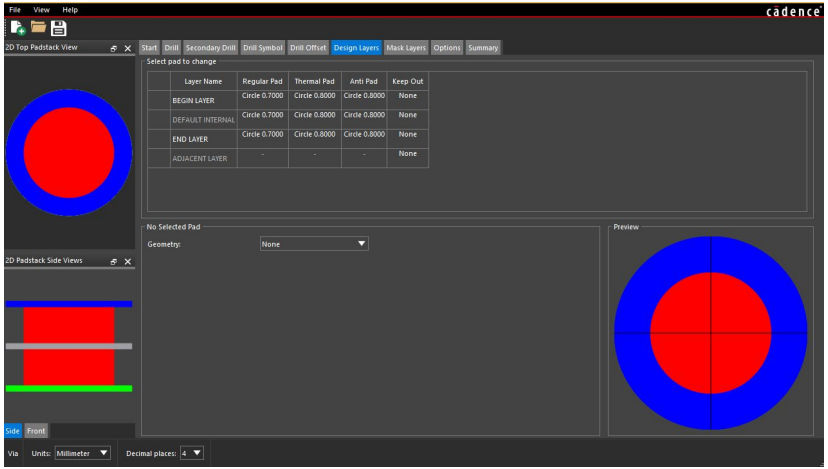
PadStack


New padstack
Look in:
C:\SPB_Data\SangwookWoo\5-1\allegro
My Computer
TABLE_14
Name
Size
Type
Date Modified
signoise.run
File...lder
2025-0... 10:42
symbols
File...lder
2025-0...후 4:38
File name:
Save
Files of type:
Padstack (*.pad)
Cancel
Change Directory

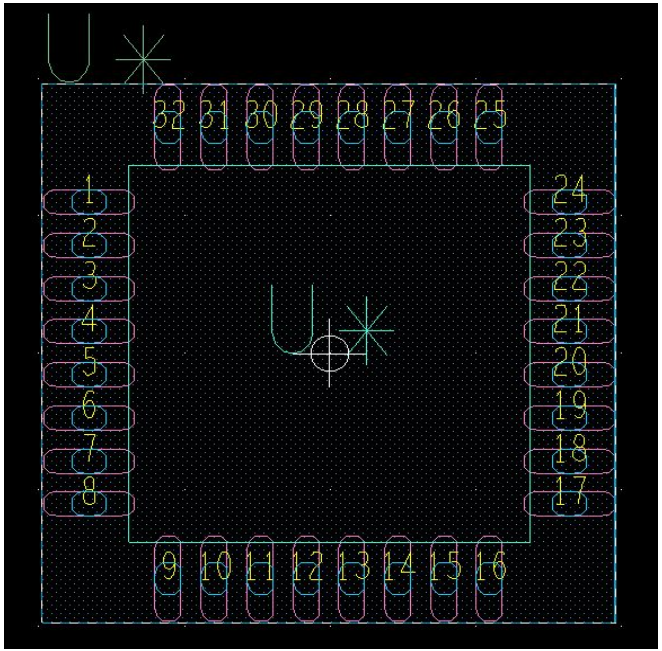

Start
Drill
Secondary Drill
Drill Symbol
Drill Offset
Drill hole
Hole type:
Circle
Finished hole
Finished diameter:
0.5000
+ Tolerance:
0.0000
- Tolerance:
0.0000

PadStack


File View Help
cadence
2D Top Padstack View
Start Drill Secondary Drill Drill Symbol Drill Offset Design Layers Mask Layers Options Summary
Select pad to change
Layer Name Regular Pad
SOLDERMASK_TOP None
SOLDERMASK_BOTTOM None
PASTEMASK_TOP None
PASTEMASK_BOTTOM None
FILMMASK_TOP None
FILMMASK_BOTTOM None
Add Layer
Pad on layer SOLDERMASK_TOP
Geometry: None
Preview
2D Padstack Side Views
Side Front
Via Units: Millimeter Decimal places: 4

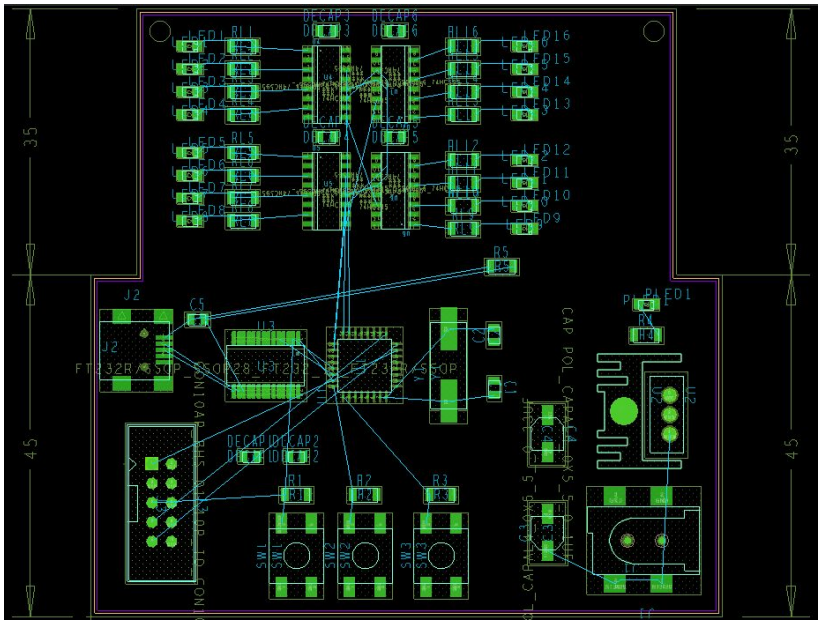

File View Help
cadence
2D Top Padstack View
Start Drill Secondary Drill Drill Symbol Drill Offset Design Layers Mask Layers Options Summary
Select pad to change
Layer Name Regular Pad Thermal Pad Anti Pad Keep Out
BEGIN LAYER Circle 0.7000 Circle 0.8000 Circle 0.8000 None
DEFAULT INTERNAL Circle 0.7000 Circle 0.8000 Circle 0.8000 None
END LAYER Circle 0.7000 Circle 0.8000 Circle 0.8000 None
ADJACENT LAYER - - - None
No Selected Pad
Geometry: None
Preview
2D Padstack Side Views
Side Front
Via Units: Millimeter Decimal places: 4

PadStack



PadStack을 활용하여 U1 symbol 제작

PCB 실습

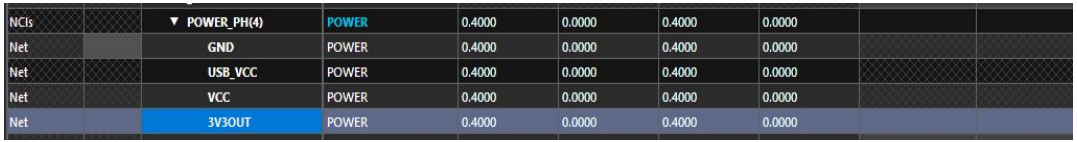


components manually를 활용하여 부품을 배치한다.

Constraint

Objects	Referenced Physical CSet
Name	
*	*
▼ hier_test	DEFAULT
▼ POWER_PH(4)	POWER
GND	POWER
USB_VCC	POWER
VCC	POWER
3V3OUT	POWER

Power line 규칙은 다르게 좀 더 굵게 적용한다.



NCIs		▼ POWER_PH(4)	POWER	0.4000	0.0000	0.4000	0.0000		
Net		GND	POWER	0.4000	0.0000	0.4000	0.0000		
Net		USB_VCC	POWER	0.4000	0.0000	0.4000	0.0000		
Net		VCC	POWER	0.4000	0.0000	0.4000	0.0000		
Net		3V3OUT	POWER	0.4000	0.0000	0.4000	0.0000		

Power line Class 적용

Constraint

hier_test

Objects			Referenced Physical CSet	Line Width		Neck		Referen
Type	S	Name		Min	Max	Min Width	Max Length	
				mm	mm	mm	mm	
*	*	*	*	*	*	*	*	*
Dsn		▼ hier_test	DEFAULT	0.3000	0.0000	0.3000	0.0000	
Rgn		SMD		0.2000				

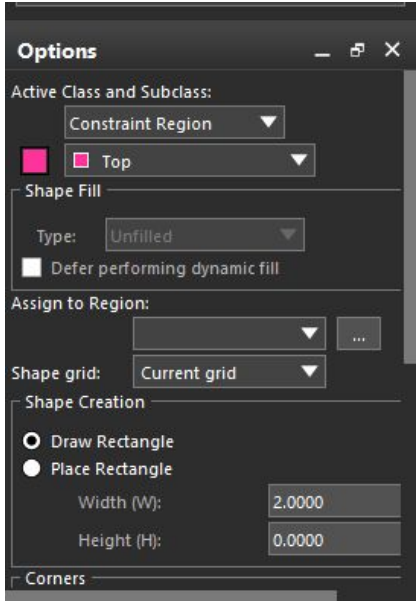
SMD Rule

hier_test

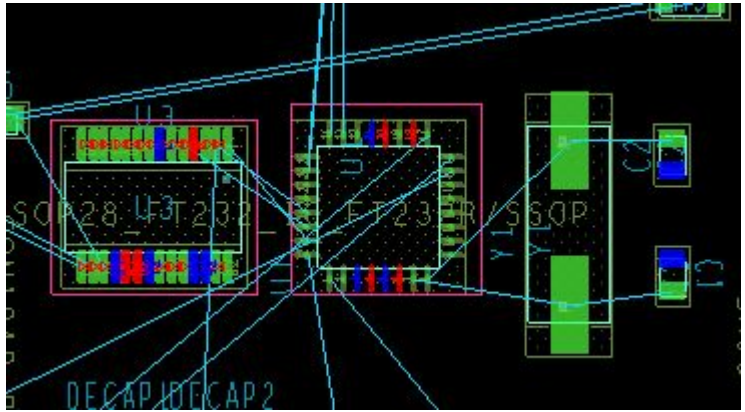
Objects			Referenced Spacing CSet	Line To	Thru Pin To	SMD Pin To	Test Pin To	Thru Via To	BB Via To	Test Via To	Shape To	Bond Finger To	Hole To	Min BB Via Gap
Type	S	Name		All	All	All	All	All	All	All	All	All	All	
				mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		▼ hier_test	DEFAULT	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.1270
SCS		▸ DEFAULT		0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.2000	0.1270

Spacing작업은 U1, U3의 pin spacing rule을 다른 배선과 다르게 더 좁은 간격을 허용한다.

Constraint

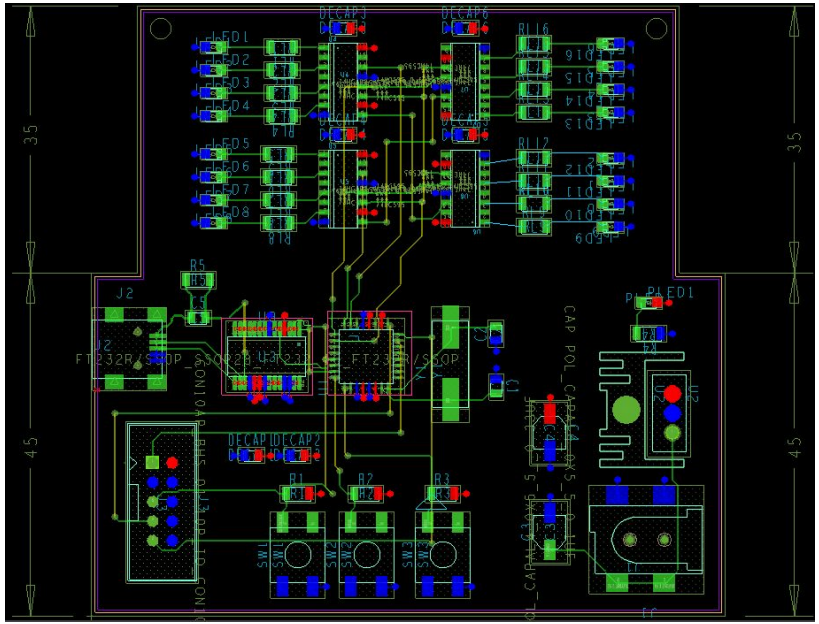


SMD Spacing 관련 rule 적용



Rectangular를 활용하여 적용한다.

Routing



DRC check 전 1차 배선 완료 모습
FAN OUT과 TOP, BOTTOM 배선이 되어 있는 것을 확인 할 수 있다.

Routing

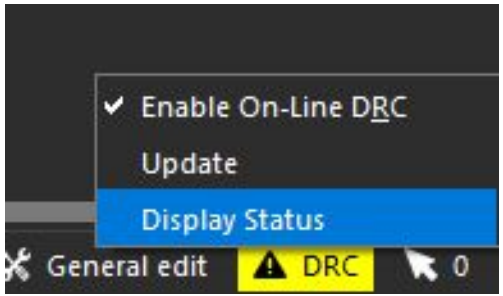
DRC Error Count Summary

DRC Error Type	DRC Error Count
Physical Constraint	2
Total DRC Errors	2

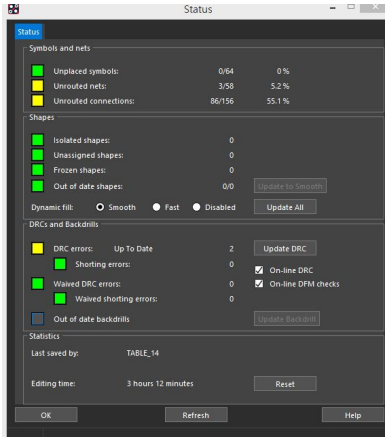
Detailed DRC Errors

Constraint Name	DRC Marker Location	DRC Subclass	Required Value	Actual Value	Constraint Source	Constraint Source Type	Element 1	Element 2
Minimum Neck Width	(21.5377 28.9985)	TOP	0.4 MM	0.2 MM	POWER	PHYSICAL CONSTRAINTS	Odd-angle Line Segment "Vcc Etch/Top"	
Minimum Neck Width	(23.1583 28.9999)	TOP	0.4 MM	0.2 MM	POWER	PHYSICAL CONSTRAINTS	Odd-angle Line Segment "Gnd Etch/Top"	

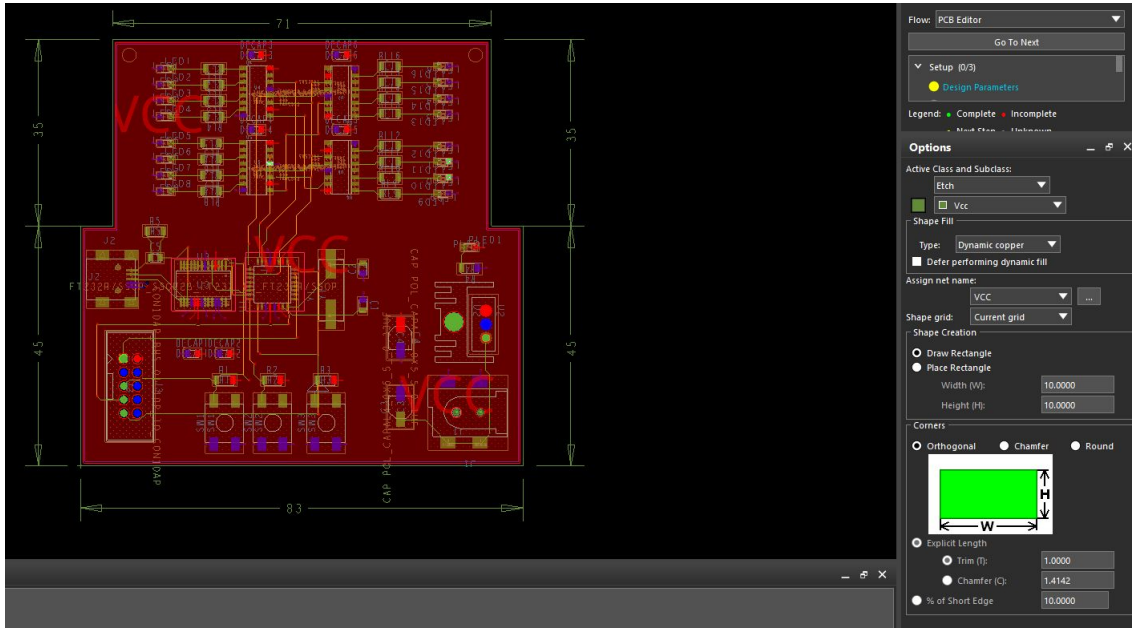
DRC Check Report.



DRC-> Display Status로 DRC 확인 가능

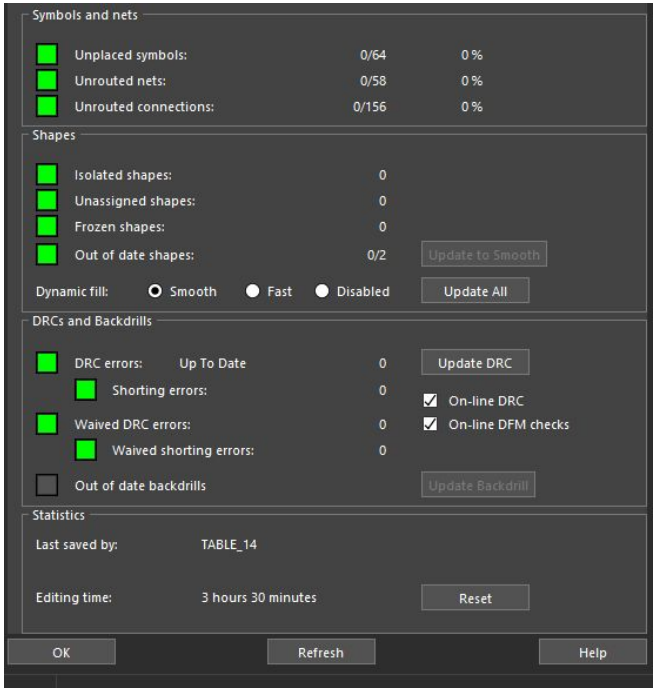


Routing



내부 **plane** 설정

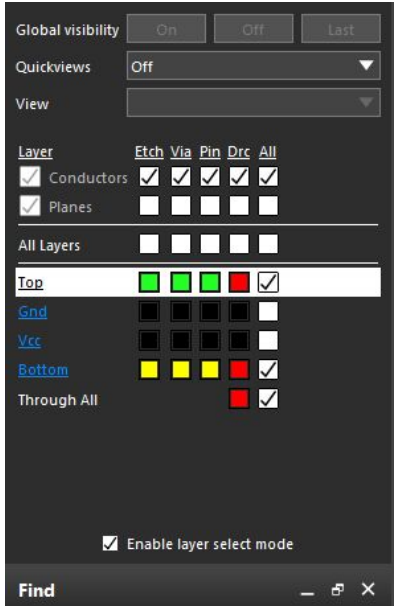
Routing



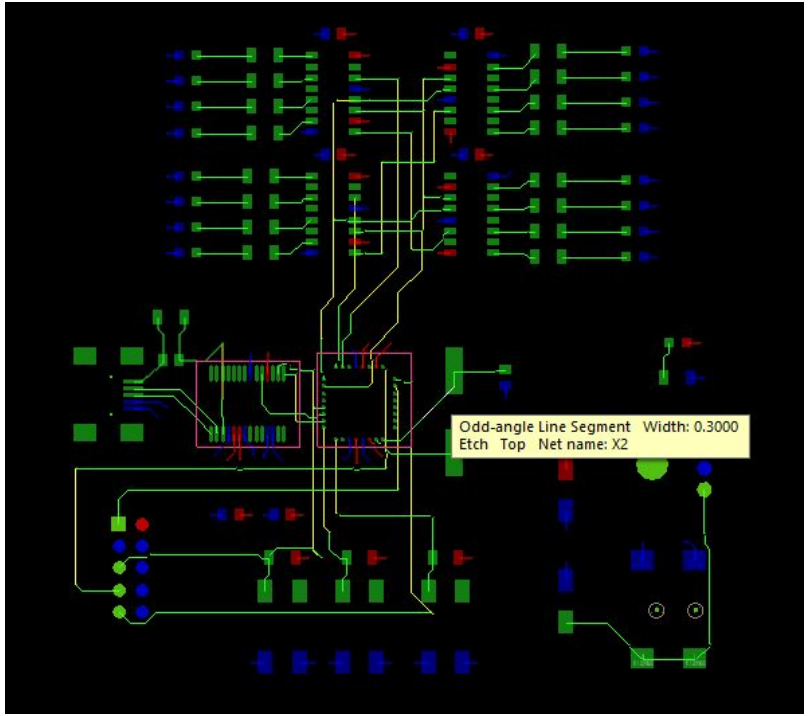
DRC Check 완료.

모두 0이 될 때까지 수정해야한다.

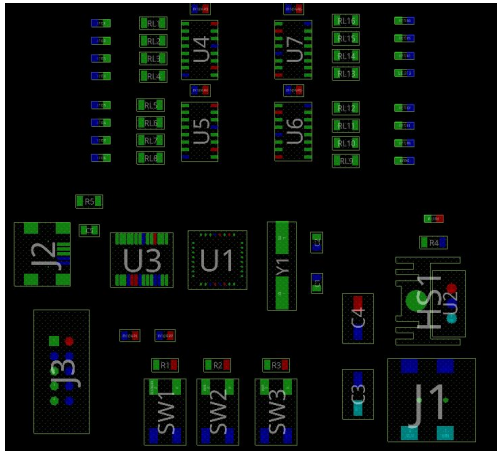
Routing

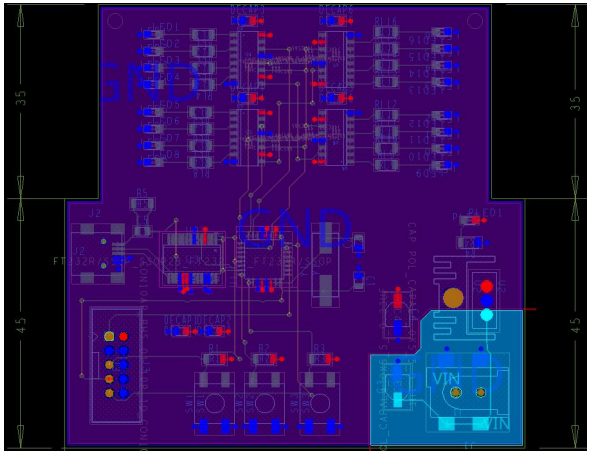


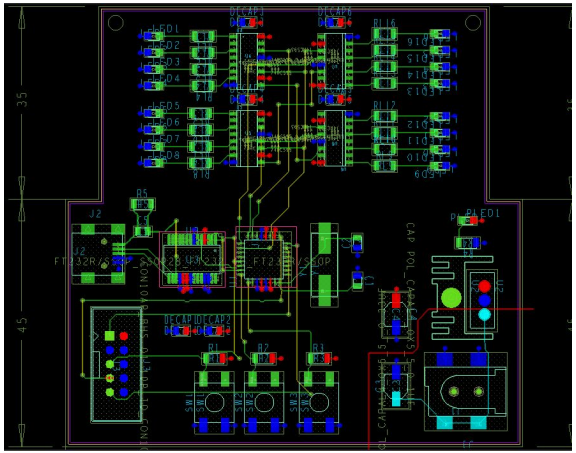
Visuality를 활용해 다양한 Layer 확인 가능



Routing

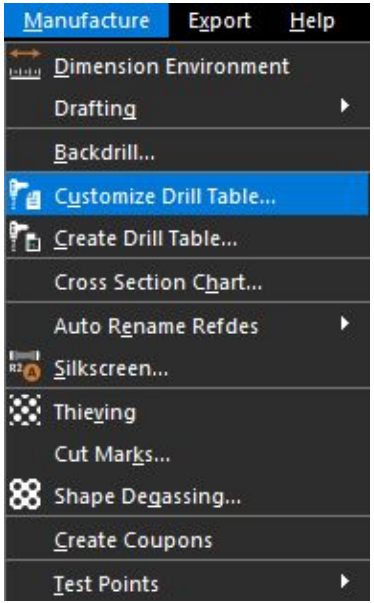


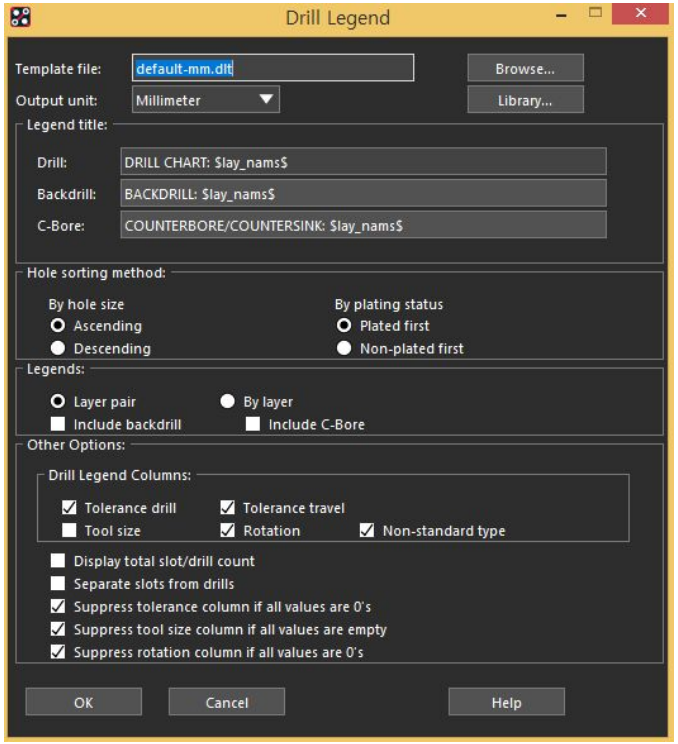


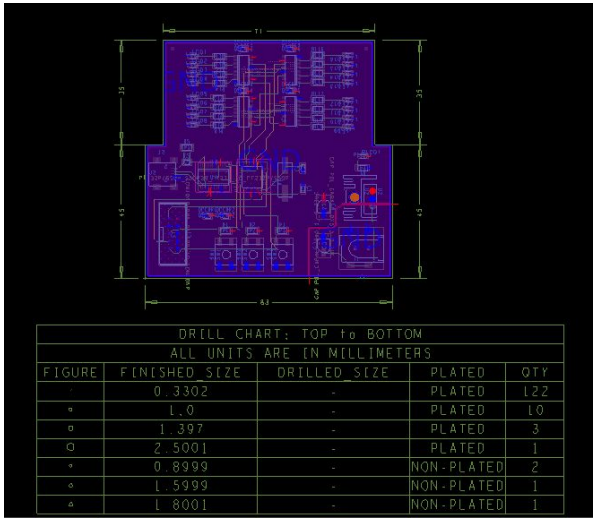


배선을 완료한 후 Artwork 추출을 시작한다.

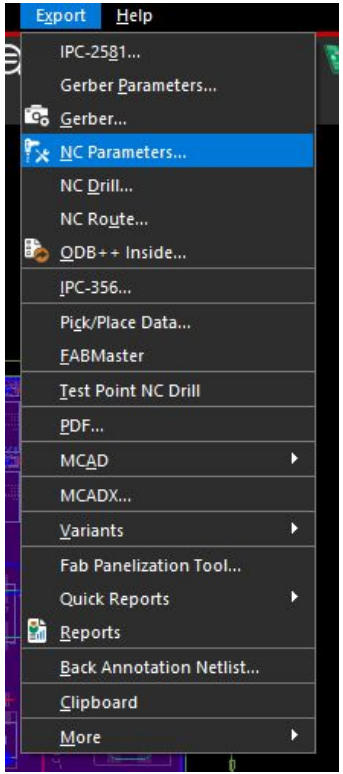
ArtWork 추출

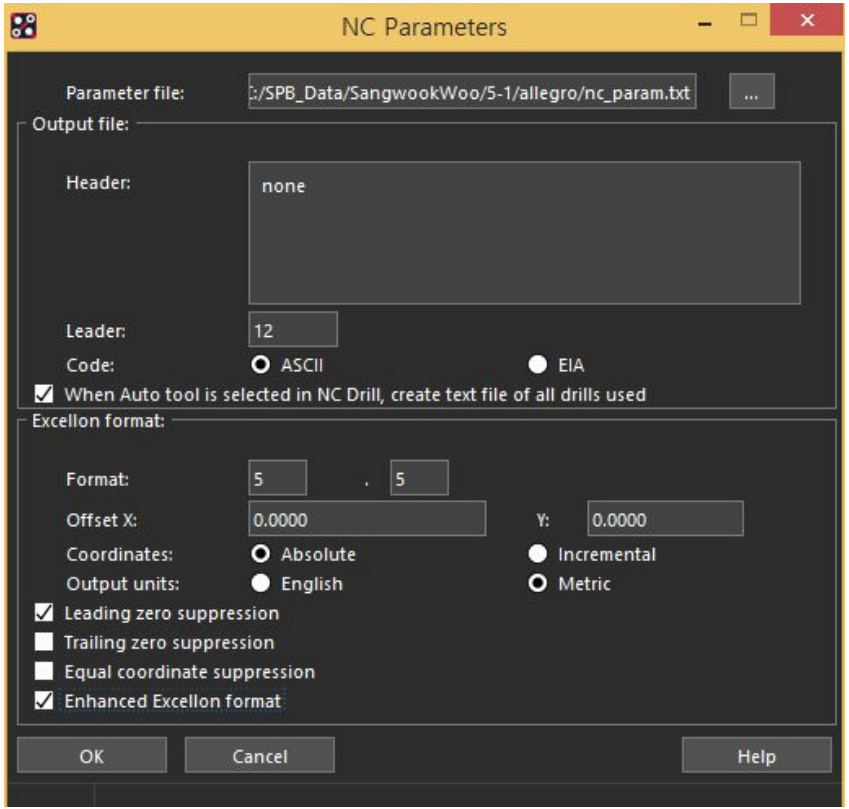

Manufacture
Export
Help
Dimension Environment
Drafting
Backdrill...
Customize Drill Table...
Create Drill Table...
Cross Section Chart...
Auto Rename Refdes
Silkscreen...
Thieving
Cut Marks...
Shape Degassing...
Create Coupons
Test Points

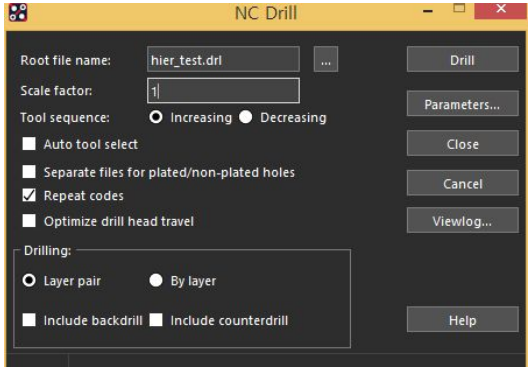

Drill Legend
Template file:
default-mm.dlt
Browse...
Output unit:
Millimeter
Library...
Legend title:
Drill:
DRILL CHART: lay_nams
Backdrill:
BACKDRILL: lay_nams
C-Bore:
COUNTERBORE/COUNTERSINK: lay_nams
Hole sorting method:
By hole size
Ascending
Descending
By plating status
Plated first
Non-plated first
Legends:
Layer pair
By layer
Include backdrill
Include C-Bore
Other Options:
Drill Legend Columns:
Tolerance drill
Tolerance travel
Tool size
Rotation
Non-standard type
Display total slot/drill count
Separate slots from drills
Suppress tolerance column if all values are 0's
Suppress tool size column if all values are empty
Suppress rotation column if all values are 0's
OK
Cancel
Help


DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILLIMETERS
FIGURE
FINISHED SIZE
DRILLED SIZE
PLATED
QTY
0.3302
PLATED
122
1.0
PLATED
10
1.397
PLATED
3
2.5001
PLATED
1
0.8999
NON-PLATED
2
1.5999
NON-PLATED
1
1.8001
NON-PLATED
1

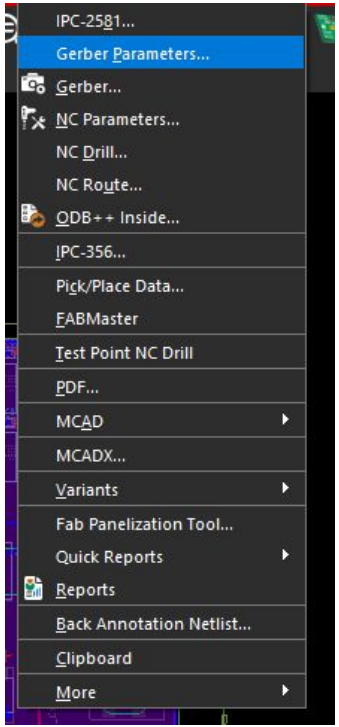
ArtWork 추출

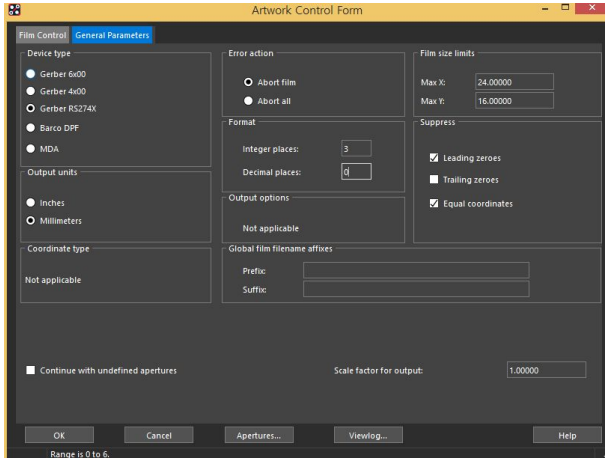

Export
Help
IPC-2581...
Gerber Parameters...
Gerber...
NC Parameters...
NC Drill...
NC Route...
ODB++ Inside...
IPC-356...
Pick/Place Data...
FABMaster
Test Point NC Drill
PDF...
MCAD
MCADX...
Variants
Fab Panelization Tool...
Quick Reports
Reports
Back Annotation Netlist...
Clipboard
More

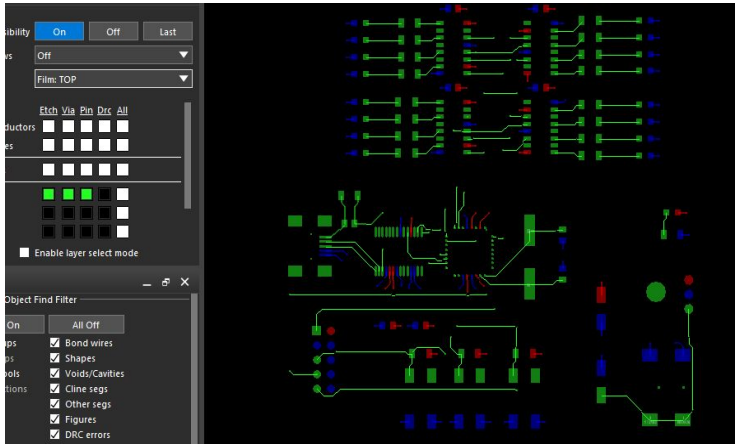

NC Parameters
Parameter file:
:/SPB_Data/SangwookWoo/5-1/allegro/nc_param.txt
...
Output file:
Header:
none
Leader:
12
Code:
ASCII
EIA
When Auto tool is selected in NC Drill, create text file of all drills used
Excellon format:
Format:
5
5
Offset X:
0.0000
Y:
0.0000
Coordinates:
Absolute
Incremental
Output units:
English
Metric
Leading zero suppression
Trailing zero suppression
Equal coordinate suppression
Enhanced Excellon format
OK
Cancel
Help


NC Drill
Root file name:
hier_test.drl
...
Drill
Scale factor:
1
Parameters...
Tool sequence:
Increasing
Decreasing
Close
Auto tool select
Separate files for plated/non-plated holes
Cancel
Repeat codes
Optimize drill head travel
Viewlog...
Drilling:
Layer pair
By layer
Include backdrill
Include counterdrill
Help

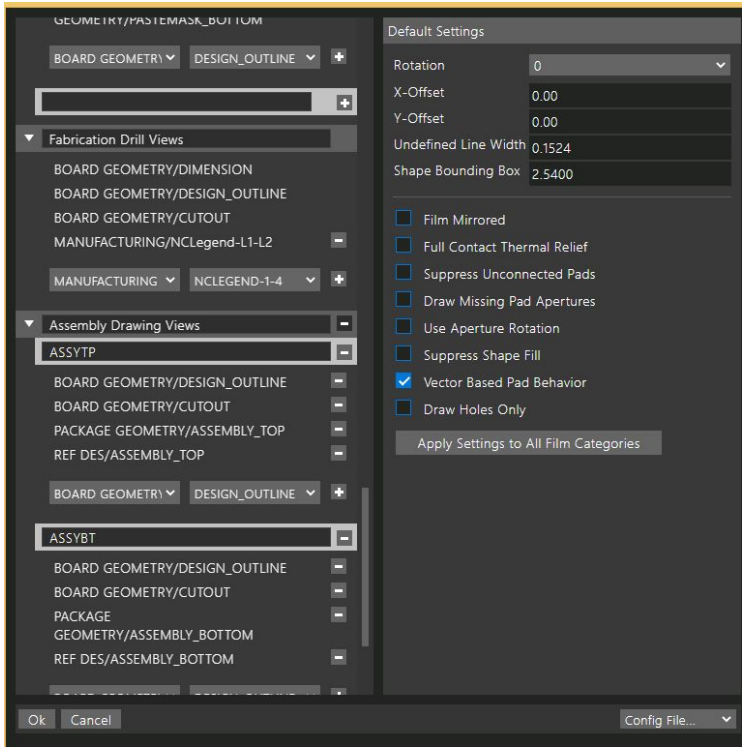
ArtWork 추출

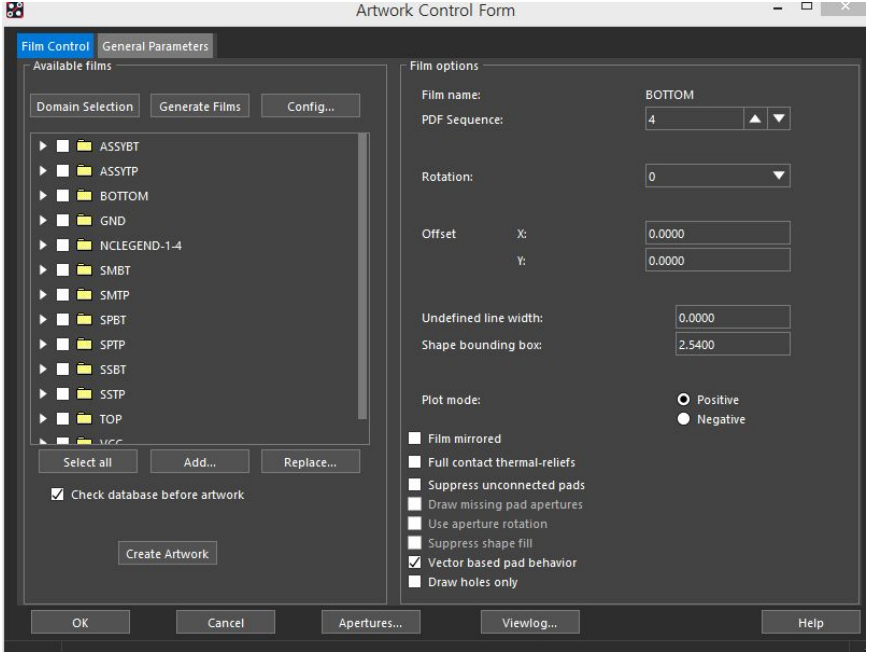

IPC-2581...
Gerber Parameters...
Gerber...
NC Parameters...
NC Drill...
NC Route...
ODB++ Inside...
IPC-356...
Pick/Place Data...
FABMaster
Test Point NC Drill
PDF...
MCAD
MCADX...
Variants
Fab Panelization Tool...
Quick Reports
Reports
Back Annotation Netlist...
Clipboard
More


Artwork Control Form
Film Control
General Parameters
Device type
Gerber 6x00
Gerber 4x00
Gerber RS274X
Barco DPF
MDA
Output units
Inches
Millimeters
Coordinate type
Not applicable
Error action
Abort film
Abort all
Format
Integer places:
Decimal places:
Output options
Not applicable
Film size limits
Max X:
Max Y:
24.00000
16.00000
Suppress
Leading zeroes
Trailing zeroes
Equal coordinates
Global film filename affixes
Prefix:
Suffix:
Continue with undefined apertures
Scale factor for output:
1.00000
OK
Cancel
Apertures...
Viewlog...
Help

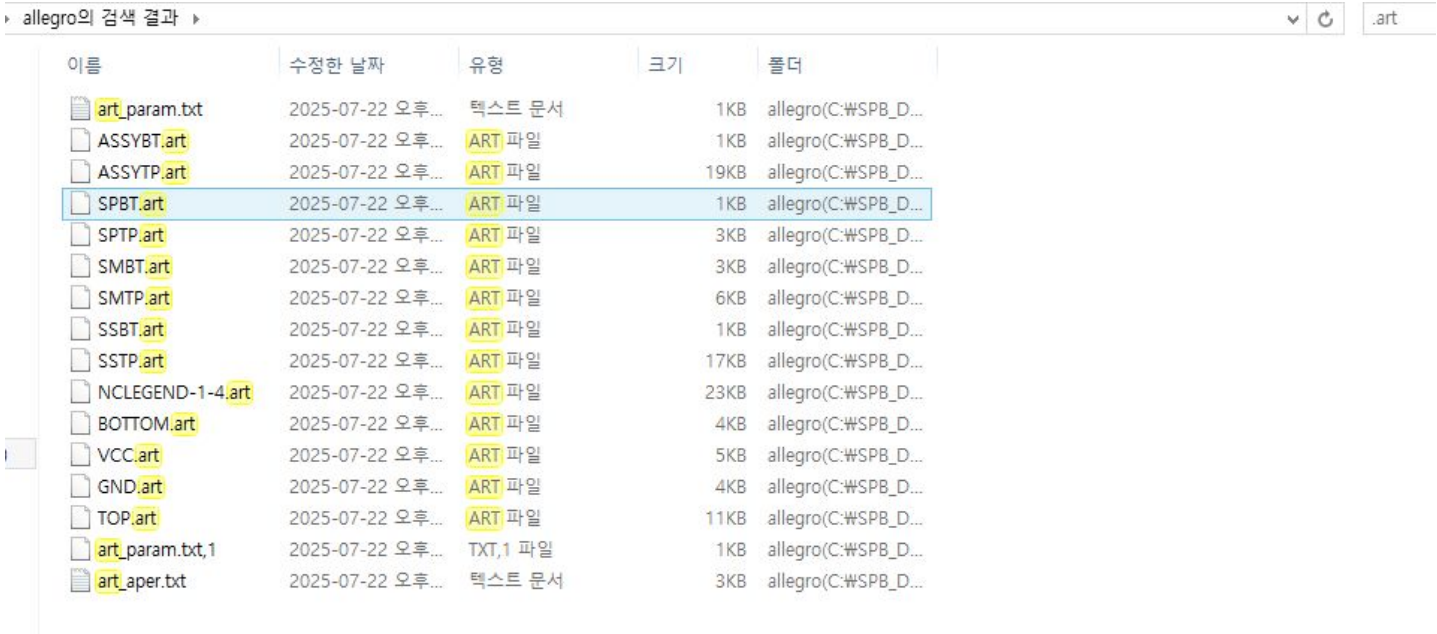

On
Off
Last
Off
Film: TOP
Etch Via Pin Drc All
Enable layer select mode
Object Find Filter
On
All Off
Bond wires
Shapes
Voids/Cavities
Cline segs
Other segs
Figures
DRC errors

ArtWork 추출


GEOMETRY/PASTEMASK_BOTTOM
BOARD GEOMETRY
DESIGN_OUTLINE
Fabrication Drill Views
BOARD GEOMETRY/DIMENSION
BOARD GEOMETRY/DESIGN_OUTLINE
BOARD GEOMETRY/CUTOUT
MANUFACTURING/NCLegend-L1-L2
MANUFACTURING
NCLEGEND-1-4
Assembly Drawing Views
ASSYTP
BOARD GEOMETRY/DESIGN_OUTLINE
BOARD GEOMETRY/CUTOUT
PACKAGE GEOMETRY/ASSEMBLY_TOP
REF DES/ASSEMBLY_TOP
BOARD GEOMETRY
DESIGN_OUTLINE
ASSYBT
BOARD GEOMETRY/DESIGN_OUTLINE
BOARD GEOMETRY/CUTOUT
PACKAGE GEOMETRY/ASSEMBLY_BOTTOM
REF DES/ASSEMBLY_BOTTOM
Default Settings
Rotation
0
X-Offset
0.00
Y-Offset
0.00
Undefined Line Width
0.1524
Shape Bounding Box
2.5400
Film Mirrored
Full Contact Thermal Relief
Suppress Unconnected Pads
Draw Missing Pad Apertures
Use Aperture Rotation
Suppress Shape Fill
Vector Based Pad Behavior
Draw Holes Only
Apply Settings to All Film Categories
Ok
Cancel
Config File...


Artwork Control Form
Film Control
General Parameters
Available films
Domain Selection
Generate Films
Config...
ASSYBT
ASSYTP
BOTTOM
GND
NCLEGEND-1-4
SMBT
SMTP
SPBT
SPTP
SSBT
SSTP
TOP
Select all
Add...
Replace...
Check database before artwork
Create Artwork
Film options
Film name:
BOTTOM
PDF Sequence:
4
Rotation:
0
Offset
X:
0.0000
Y:
0.0000
Undefined line width:
0.0000
Shape bounding box:
2.5400
Plot mode:
Positive
Negative
Film mirrored
Full contact thermal-reliefs
Suppress unconnected pads
Draw missing pad apertures
Use aperture rotation
Suppress shape fill
Vector based pad behavior
Draw holes only
OK
Cancel
Apertures...
Viewlog...
Help

ArtWork 추출



manual을 따라 작업을 수행한 결과 최종적으로 .art file을 생성할 수 있다.