LED Display Driver IC

IK2102

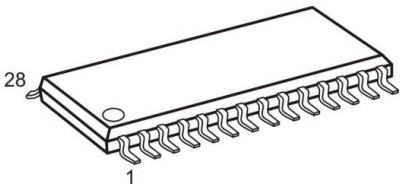
GENERAL DESCRIPTION

The IK2102 is a common cathode type LED panel display driver with output size - 4 digits x13 segments or 7 digits x 10 segments and addition key scan function.

Serial interface provide connection with microprocessor.

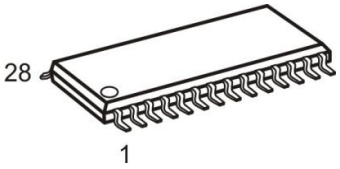
IK2102DW

SOP-28



IK2102TSD

TSSOP-28



Ta = -40 to 85°C
for all package

FEATURES

- Wide operation Voltage: 3.0V to 5.5V
- Serial Interface
- 8-Step Dimming Circuitry
- Built in OSC generator (with external resistor regulation)
- Pulse Segment Current: 10 mA type (8 mA to 12 mA) @ V_{DD}= 3.3V to 5.5V
- Pulse Segment Current: 15 mA type (12 mA to 18 mA) @ V_{DD}= 5.0V
- Key scanning: 10 × 2 matrix
- Operation Temperature: -40 to 85°C
- PKG option

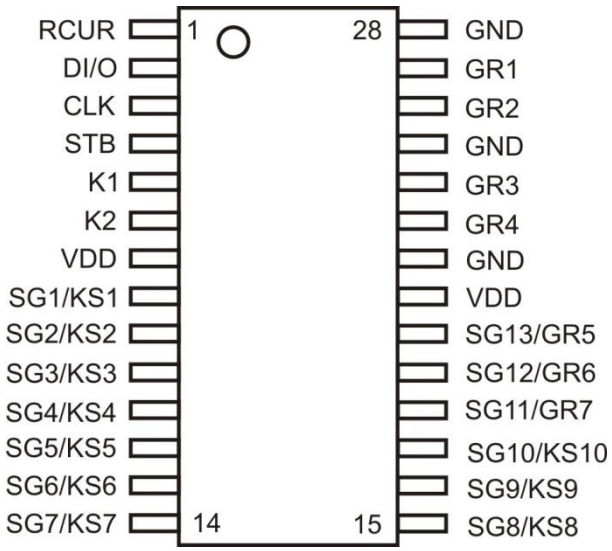
APPLICATIONS

- Micro-computer Peripheral Device
- VCR set
- DVD Combo set
- DMB Player

ORDERING INFORMATION

Device	Package	Packing
IK2102DW	SOP 28	Tube
IK2102DWT	SOP 28	Tape & Reel
IK2102TSD	TSSOP 28	Tube
IK2102TSDT	TSSOP 28	Tape & Reel

PIN ASSIGNMENT



PIN LIST AND DESCRIPTIONS

Pin Name	I/O	Description	Pin №
RCUR	I	A resistor is connected to this pin to determine the SG1-SG13 output current and internal oscillation frequency.	1
DI/O	I/O	Data Input - Output Pin This pin inputs serial data at the rising edge of the clock (starting from the bit). Data Output Pin - N-Channel, Open-Drain This pin outputs serial data at the falling edge of the clock.	2
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and output data at the falling edge.	3
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed. When this pin is HIGH, CLK is ignored.	4
K1, K2	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor).	5, 6
VDD	-	Power Supply	7, 21
SG1/KS1 to SG10/KS10	O	Segment Output Pins (P-Channel, Open Drain) Also acts as the Key Source.	8 - 17
SG11/GR7 to SG13/GR5	O	Segment / Grid Output Pins	18 - 20
GND	-	Ground Pins	22, 25, 28
GR4 to GR1	O	Grid Output Pins	23, 24, 26, 27

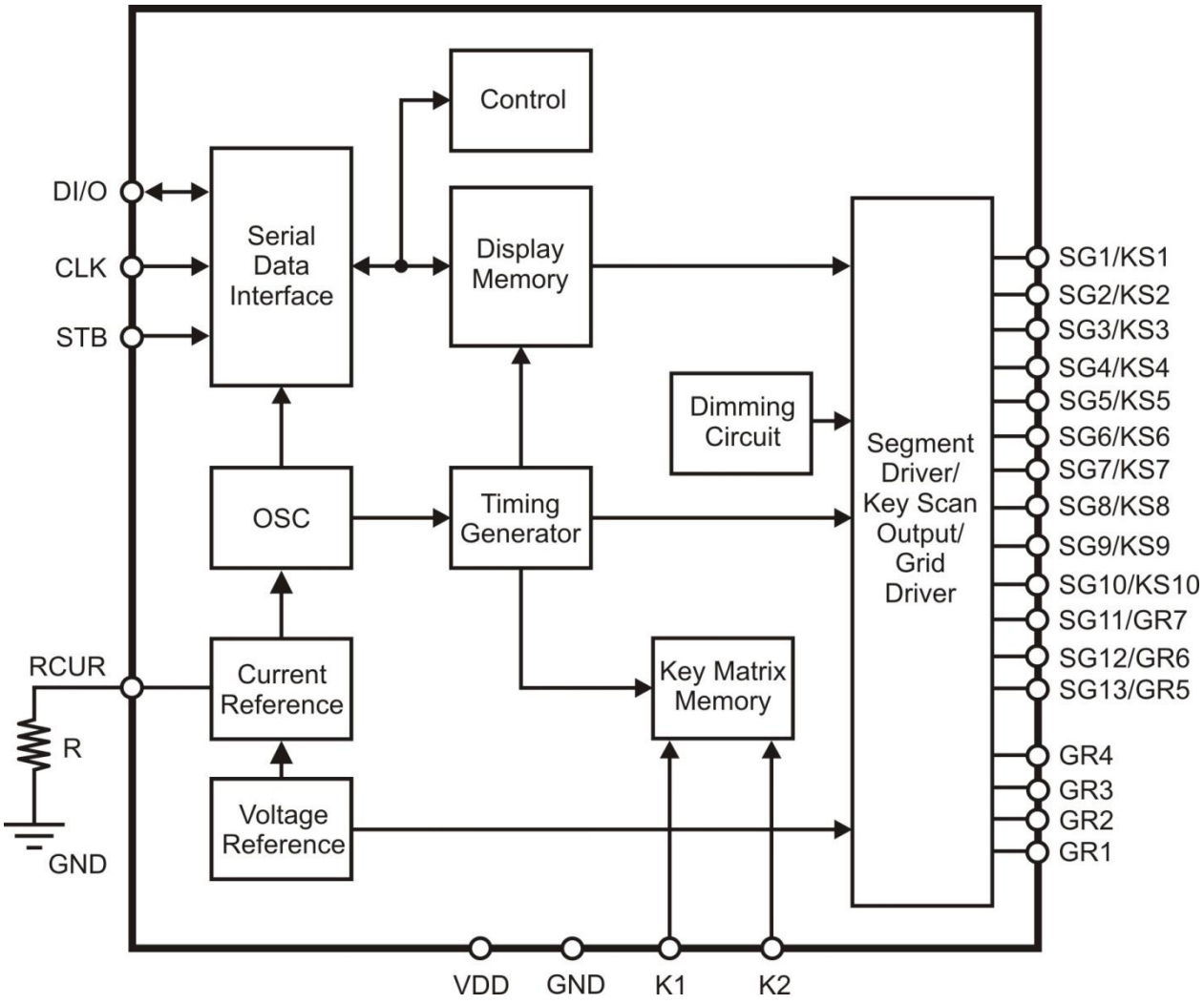
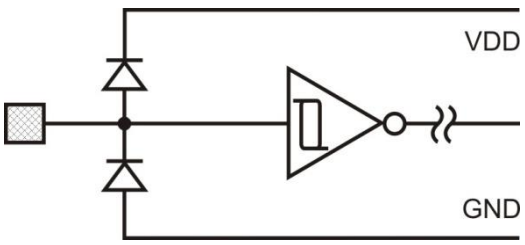


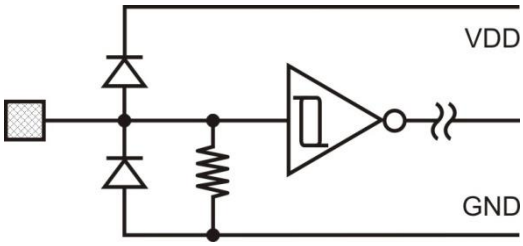
Figure. Block Diagram

The schematic diagrams of the input and output circuits are shown below.

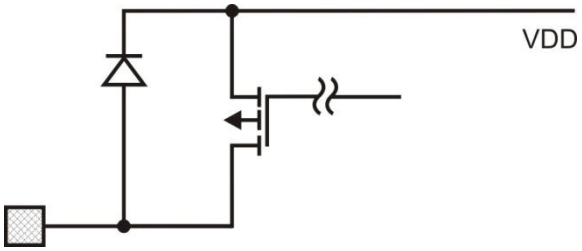
Input Pins: CLK, STB & DIN(DI/O)



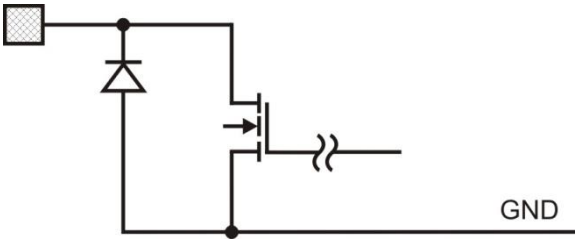
Input Pins: K1, K2



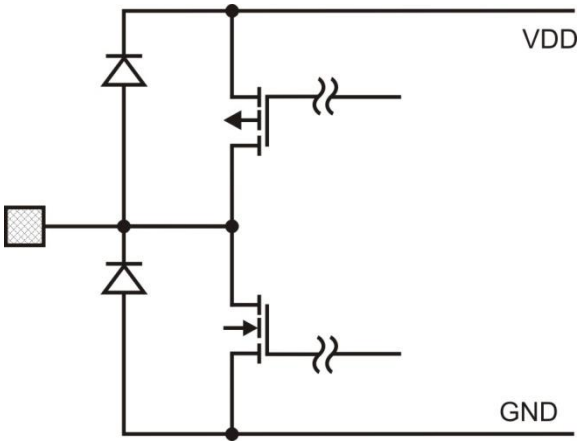
Input Pins: RCUR, SG1 to SG10



Output Pins: DOUT(DI/O), GR1 to GR4



Output Pins: SG11/GR7, SG12/GR6 & SG13/GR5



FUNCTIONAL DESCRIPTION

Commands

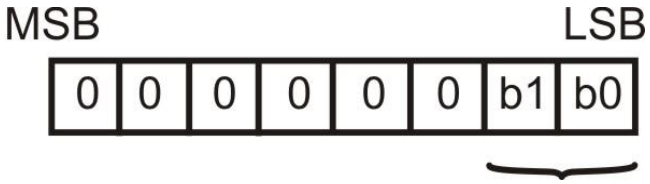
A command is the first byte (b0 to b7) inputted to IK2102 via DI/O Pin after STB pin has changed from ”HIGH” to “LOW” state. If for some reason the STB Pin is set “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

IK2102 provides 4 display modes setting as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to IK2102 via the DIN, DI/O Pin when STB is “LOW”. However, for these commands, Bit 3 & Bit 8 (b2 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids be used (4 grids to13 segments, 7 grids to 10 segments). A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

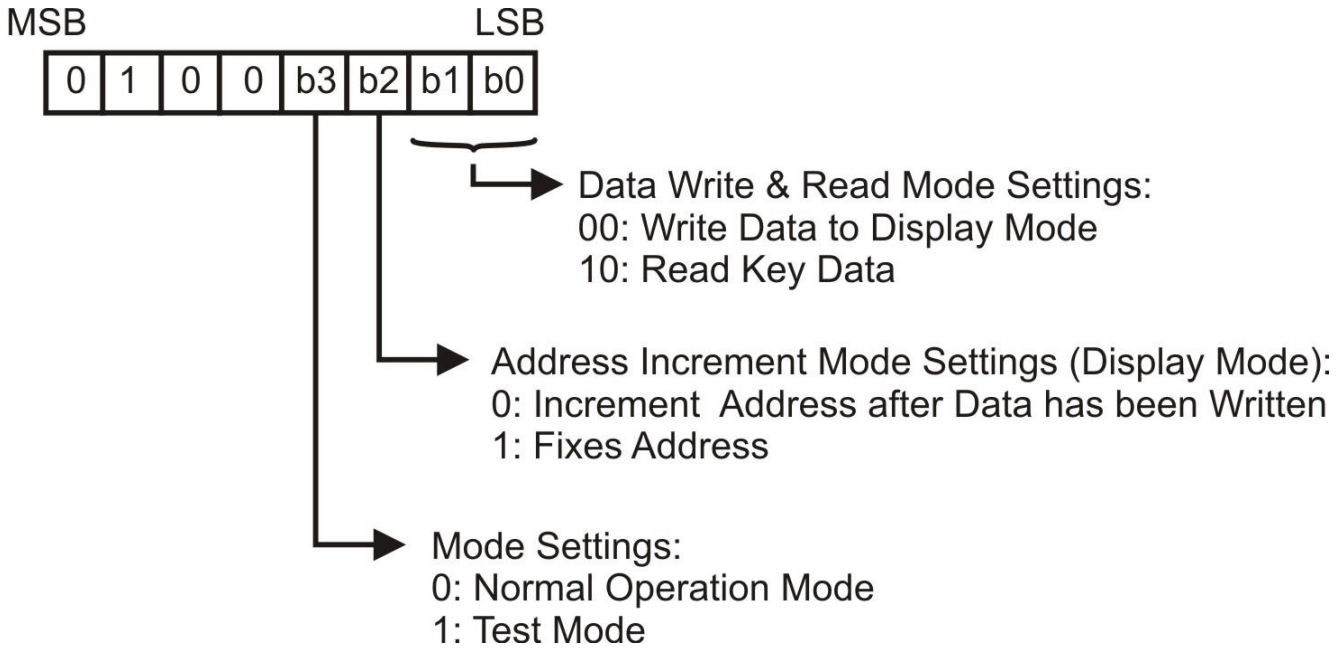
When Power is turned “ON”, the mode 11 is selected.



Display Mode Settings:
00: 4 Grids, (13 Segments)
01: 5 Grids, (12 Segments)
10: 6 Grids, (11 Segments)
11: 7 Grids, (10 Segments)

COMMAND 2: DATA SETTING COMMANDS

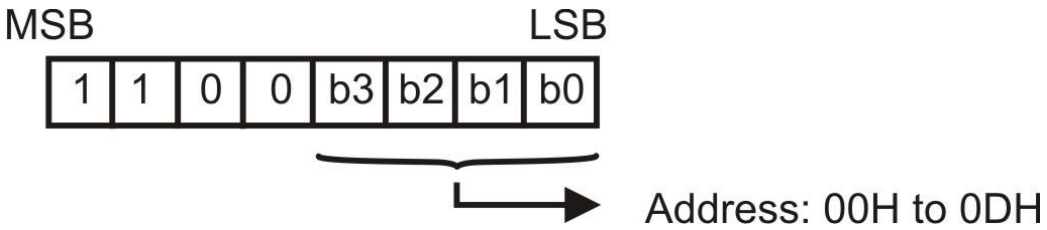
The Data Setting Commands executes the Data Write Mode for IK2102. The Data Setting Command, the bits5 and 6 (b4, b5) are given the value of “0”. , bit7 (b6) is given the value of “1” while bit8 (b7) is given the value of “0”. Please refer to the diagram below.
When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of “0”.



COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to 0DH”. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



Display Mode and RAM Address

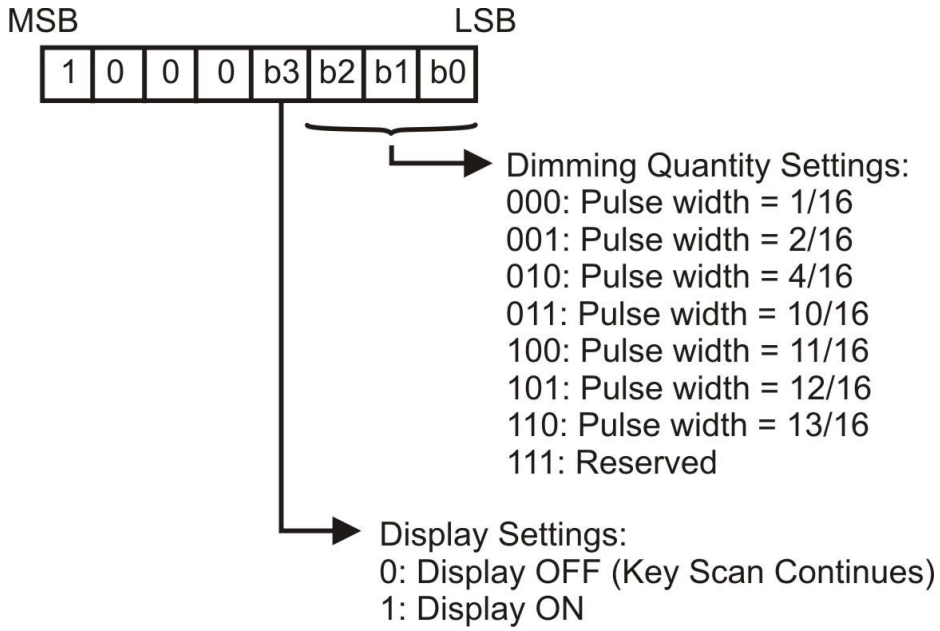
Data transmitted from an external device to IK2102 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of IK2102 are given below in 8 bit unit.

SG1	SG4	SG5	SG8	SG9	SG12	SG13	
00HL		00HU		01HL		01HU	DIG1
02HL		02HU		03HL		03HU	DIG2
04HL		04HU		05HL		05HU	DIG3
06HL		06HU		07HL		07HU	DIG4
08HL		07HU		09HL		09HU	DIG5
0AHL		0AHU		0BHL		0BHU	DIG6
0CHL		0CHU		0DHL		0DHU	DIG7

b0	b3	b4	b7
xxHL		xxHU	
Lower 4 bits		Higher 4 bits	

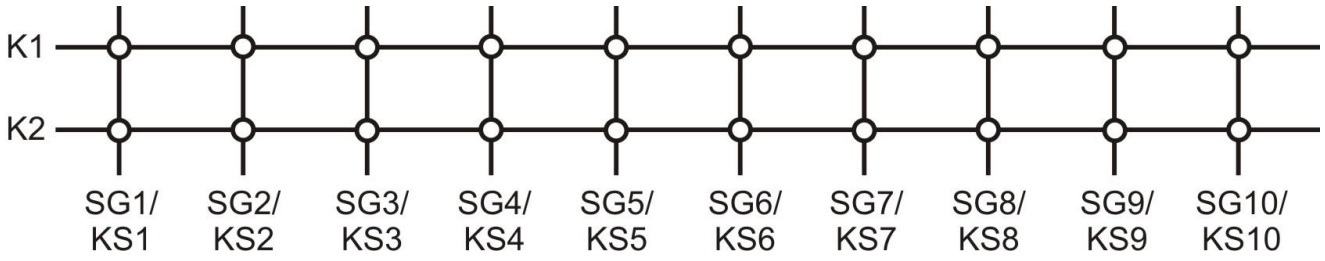
COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.

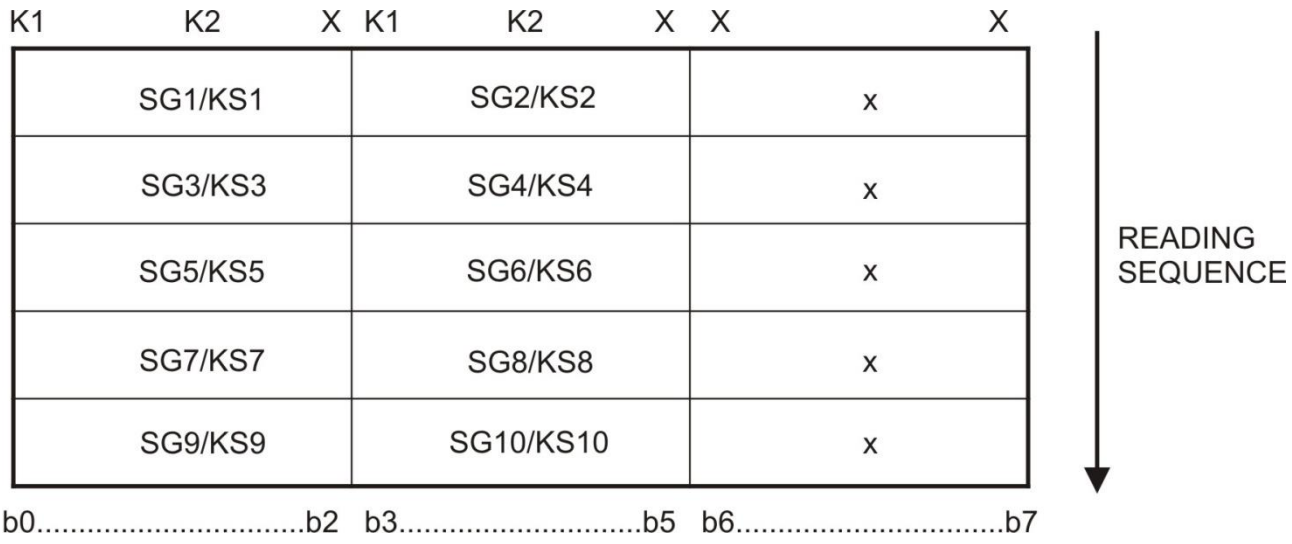


KEY MATRIX & KEY INPUT DATA STOREGE RAM

Key Matrix consists of 10 x 2 arrays as shown below:

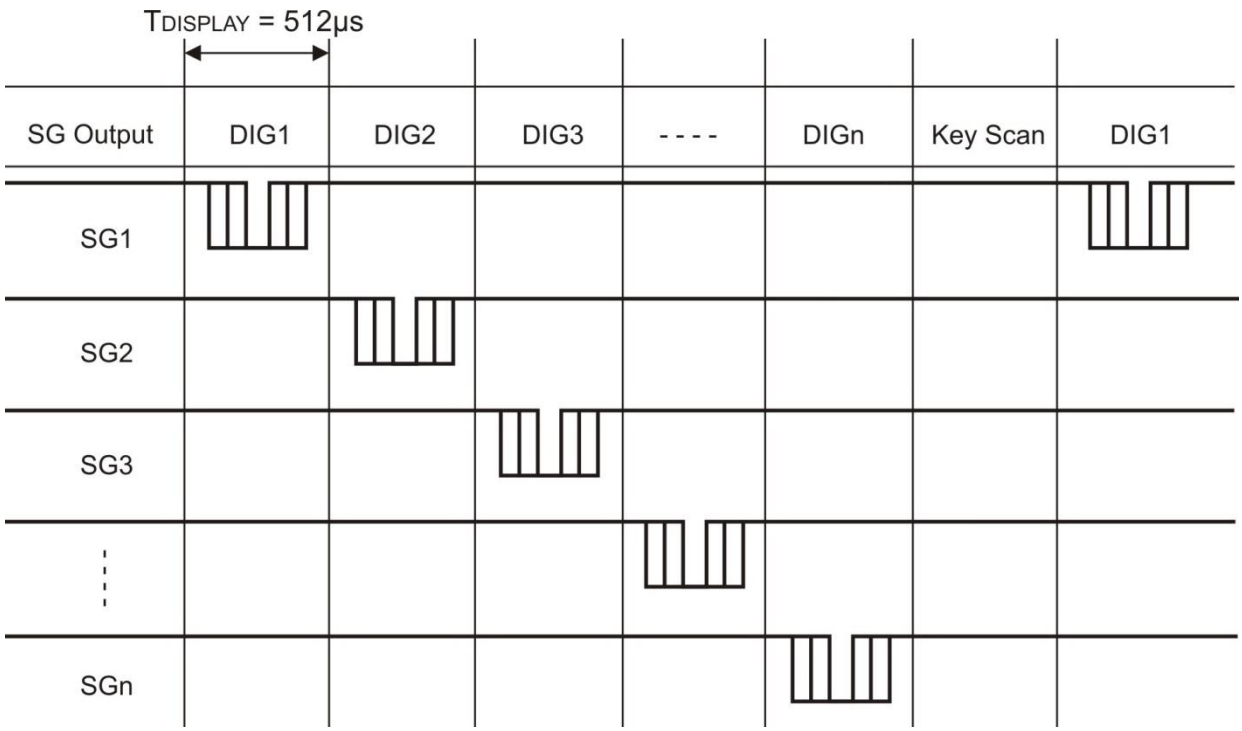


Each data entered by each key (or any combination of keys) is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.



Note: b2, b5, b6 and b7 do not care.

SCANNING AND DISPLAY TIMING

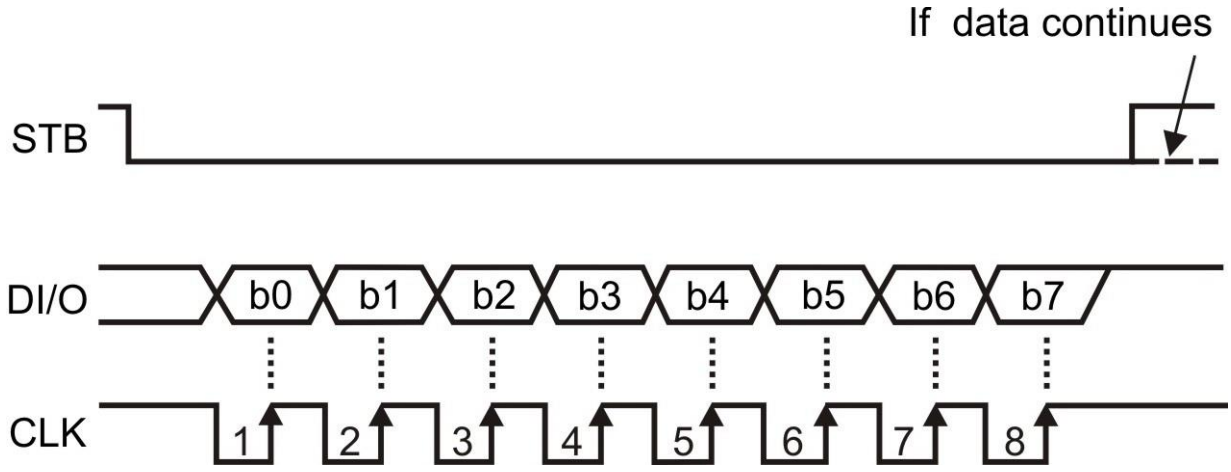


1 Frame = Tdisplay x (n+1)

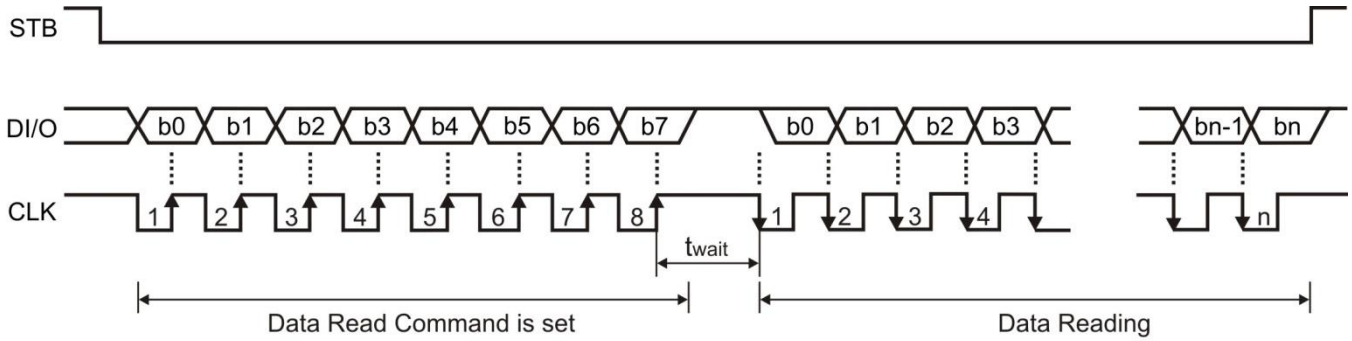
SERIAL COMMUMICATION FORMAT

The following diagram shows the serial communication format.

Reception (Data/Command Write)



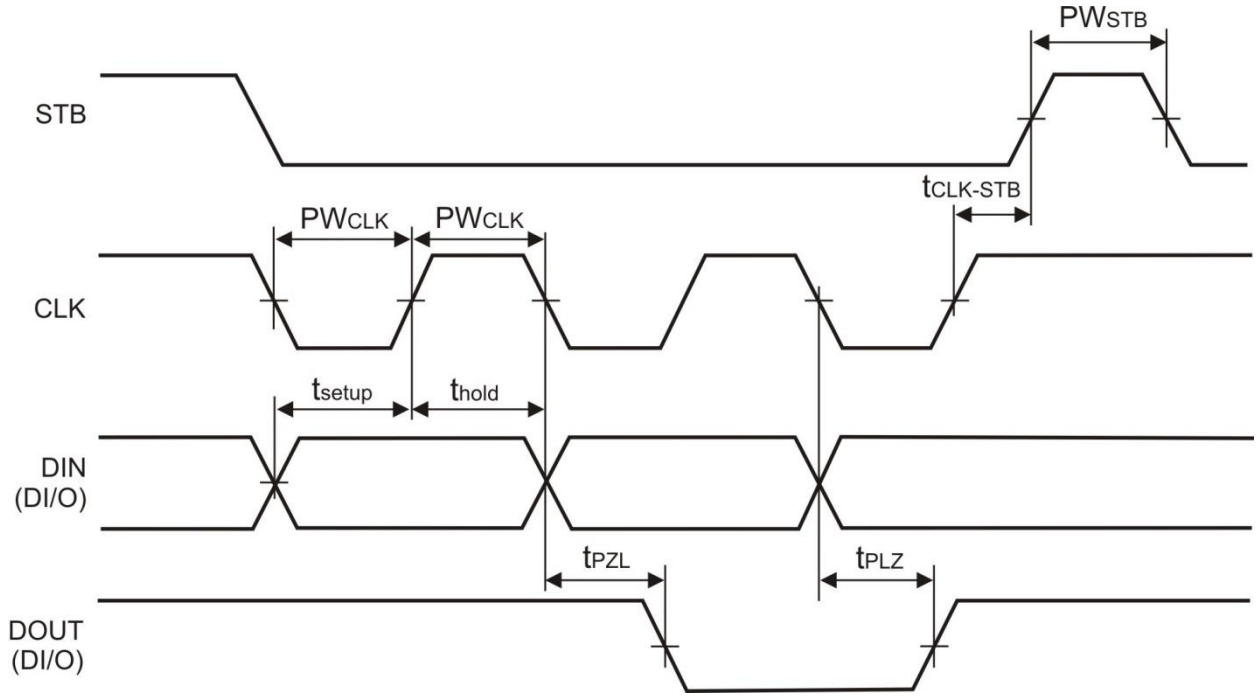
Transmission (Data Read)



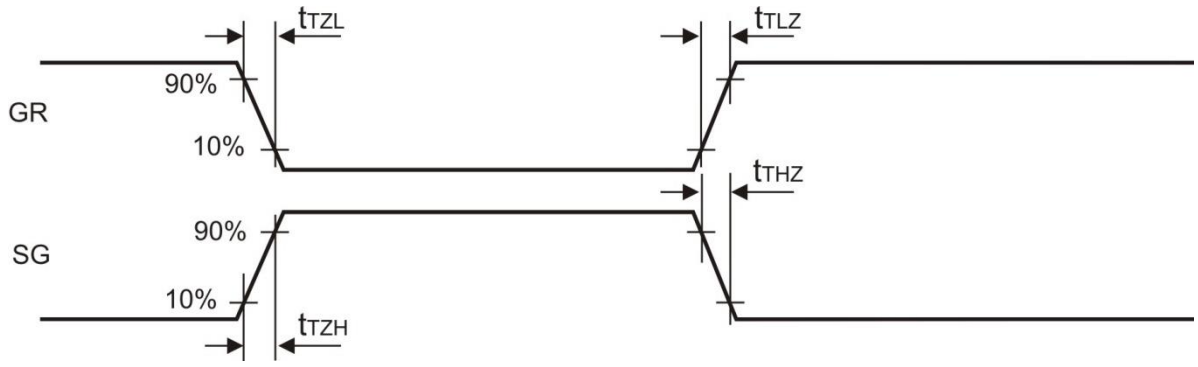
Where: t_{wait} (waiting time) ≥ 1μs

SWITCHING CHARACTERISTIC WAVEFORM

Switching Characteristics Waveform is given below.



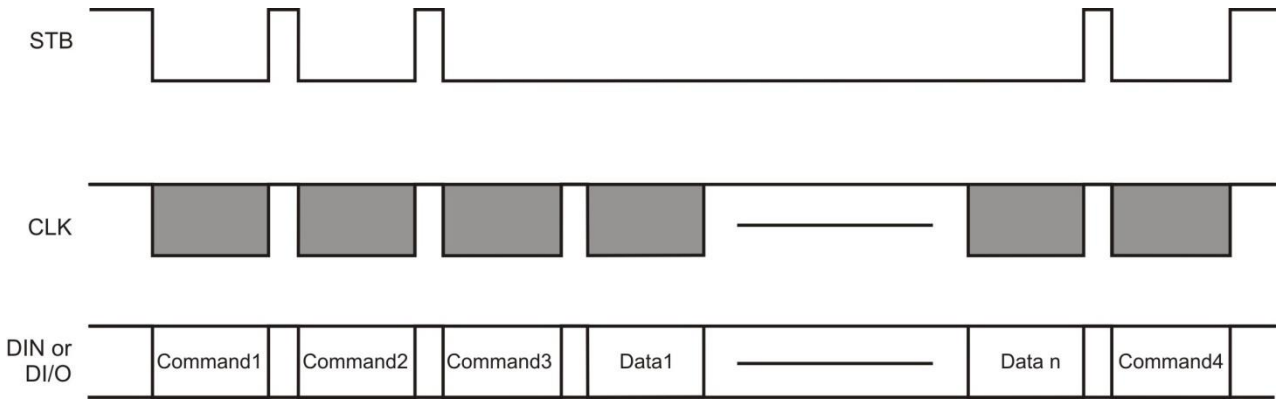
PW_{STB} (Strobe Pulse Width) ≥ 1μs
$t_{CLK-STB}$ (Clock - Strobe Time) ≥ 1μs
PW_{CLK} (Clock Pulse Width) ≥ 400ns
t_{setup} (Data Setup Time) ≥ 100ns
t_{hold} (Data Hold Time) ≥ 100ns
t_{PZL}
t_{PLZ}



t_{TZL} < 1μs
t_{TLZ} < 10μs
t_{TZH} (Rise Time) ≤ 1μs
t_{THZ} (Fall Time) ≤ 10μs

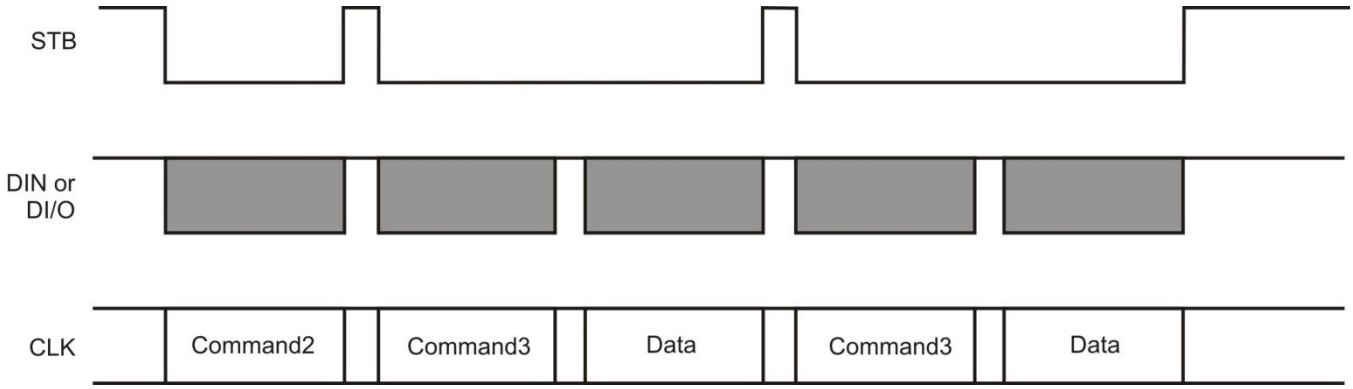
APLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



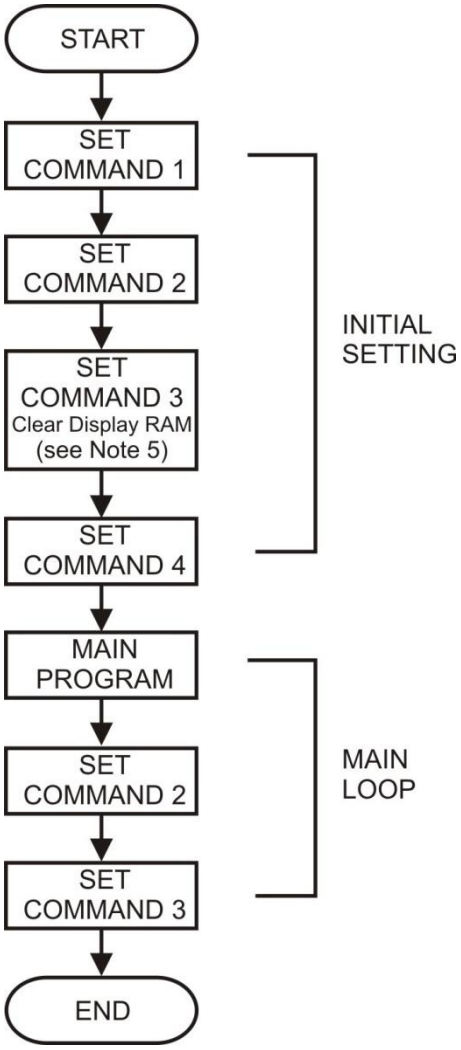
Where: Command 1: Display Mode Setting
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to Data n: Transfer Display Data (14 Bytes max)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.



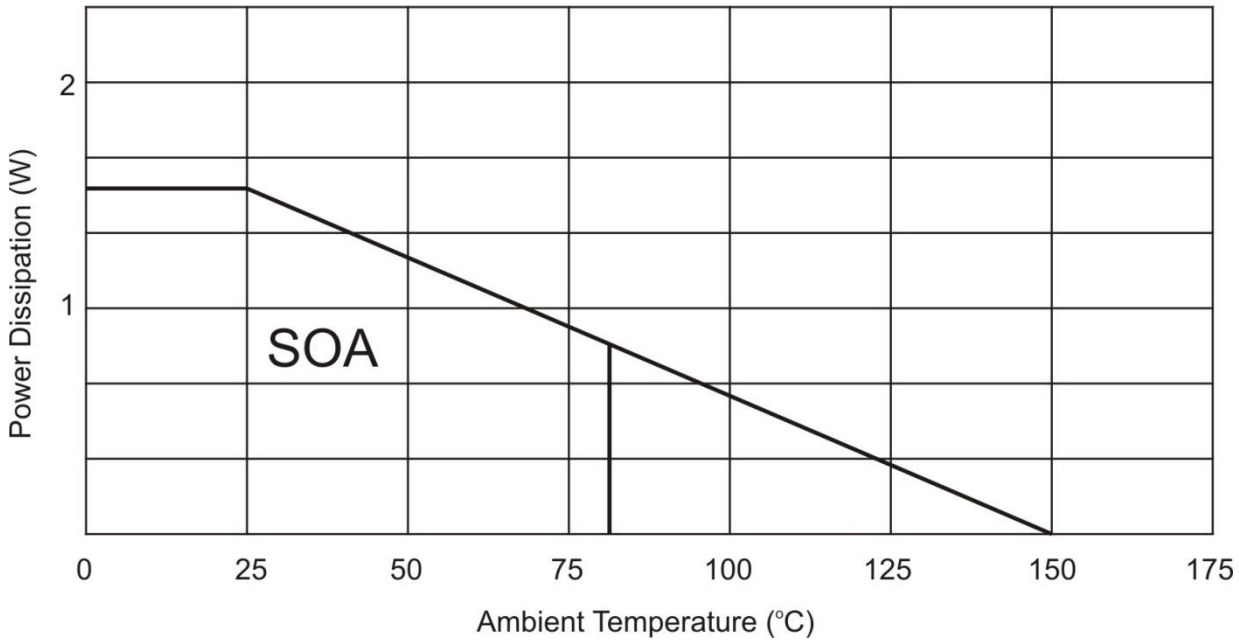
Where: Command 2 -- Data Setting Command
Command 3 -- Address Setting Command
Data -- Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART



Notes: 1. Command 1: Display Mode Setting
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined: thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

POWER DISSIPATION CURVE



ABSOLUTE MAXIMUM RATINGS*

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Rating	Units
Supply Voltage	VCC	-0.5 to +6.0	V
Logic Input Voltage	V_I	-0.5 to V_{DD}+0.5	V
Driver Output Current/Pin	I_{OLGR}	250	mA
	I_{OHSG}	-18	mA
Maximum Driver Output Current/Total	I_{TOTAL}	250	mA
Operation Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-65 to +150	°C

**Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

RECOMMENDED OPERATION RANGE

(Unless otherwise stated, Ta= -40 to +85°C, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Logic Supply Voltage	V_{DD}	3.0	3.3	5.5	V
Dynamic Current (see Note)	I_{DDdyn}	.	.	1	mA
High-Level Input Voltage	V_{IH}	$0.7V_{DD}$	.	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	.	$0.3V_{DD}$	V

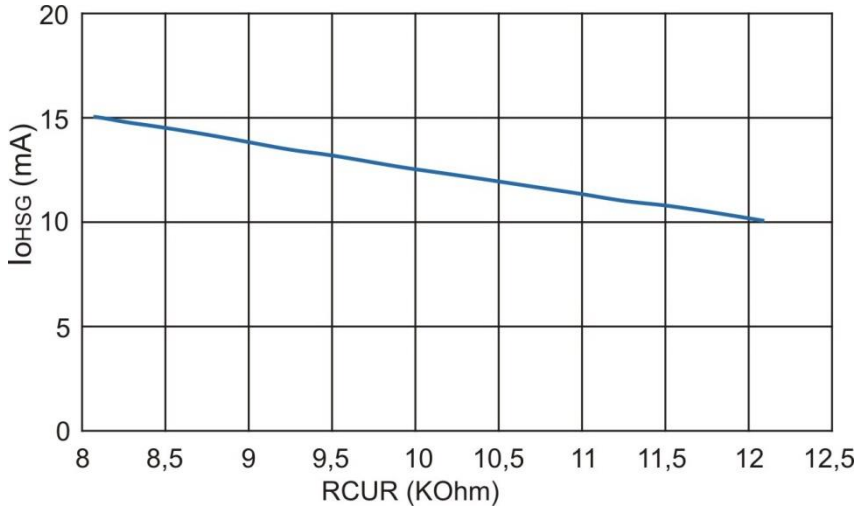
Note: Test Condition: Set Display Control Commands = 80H (Display Turn OFF State)

ELECTRICAL CHARACTERISTICS

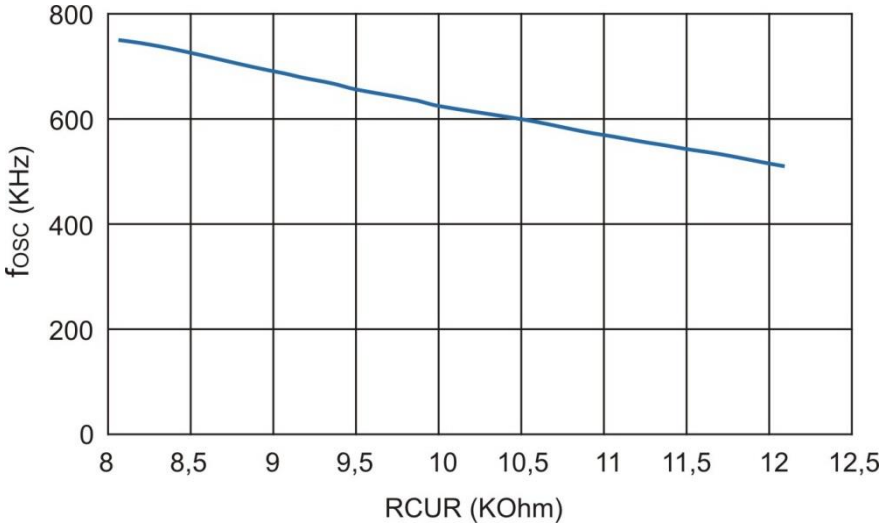
(Unless otherwise stated, V_{DD} = 3.3 to 5.5V, GND = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-Level Output Current	I_{OHSG1}	V_{DD} = 3.3 to 5.5V, V_{LED} =2.3V R = 12.1KOhm SG1 to SG10 SG11/GR7 to SG13/GR5	8	10	12	mA
	I_{OHSG2}	V_{DD} = 5V, V_{LED} =2.3V R = 8.07KOhm SG1 to SG10 SG11/GR7 to SG13/GR5	12	15	18	mA
Digital Input Current	I_{DG}	-	-0.2	-	+0.2	uA
Low-Level Digital Output Current	I_{OLDG}	V_O = 0.4V	4	-	-	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	V_O = V_{DD} =2.3V R = 12.1KOhm SG1 TO SG10 SG11/GR7 to SG13/GR5	-	-	±5	%
High-Level Input Voltage	V_{IH}	-	$0.7V_{DD}$	-	$0.3V_{DD}$	V
Low-Level Input Voltage	V_{IL}	-	-	-	$0.3V_{DD}$	V
Oscillation Frequency	f_{OSC1}	V_{DD}=3.3 to 5.5V R = 12.1kOhm	400	500	600	kHz
	f_{OSC2}	V_{DD} = 5V, R = 8.07KOhm	500	750	900	
K1, K2 Pull Down Resistor	R_{PD}	V_{DD} =5.0V	40	-	100	KΩ

High-Level Output Current

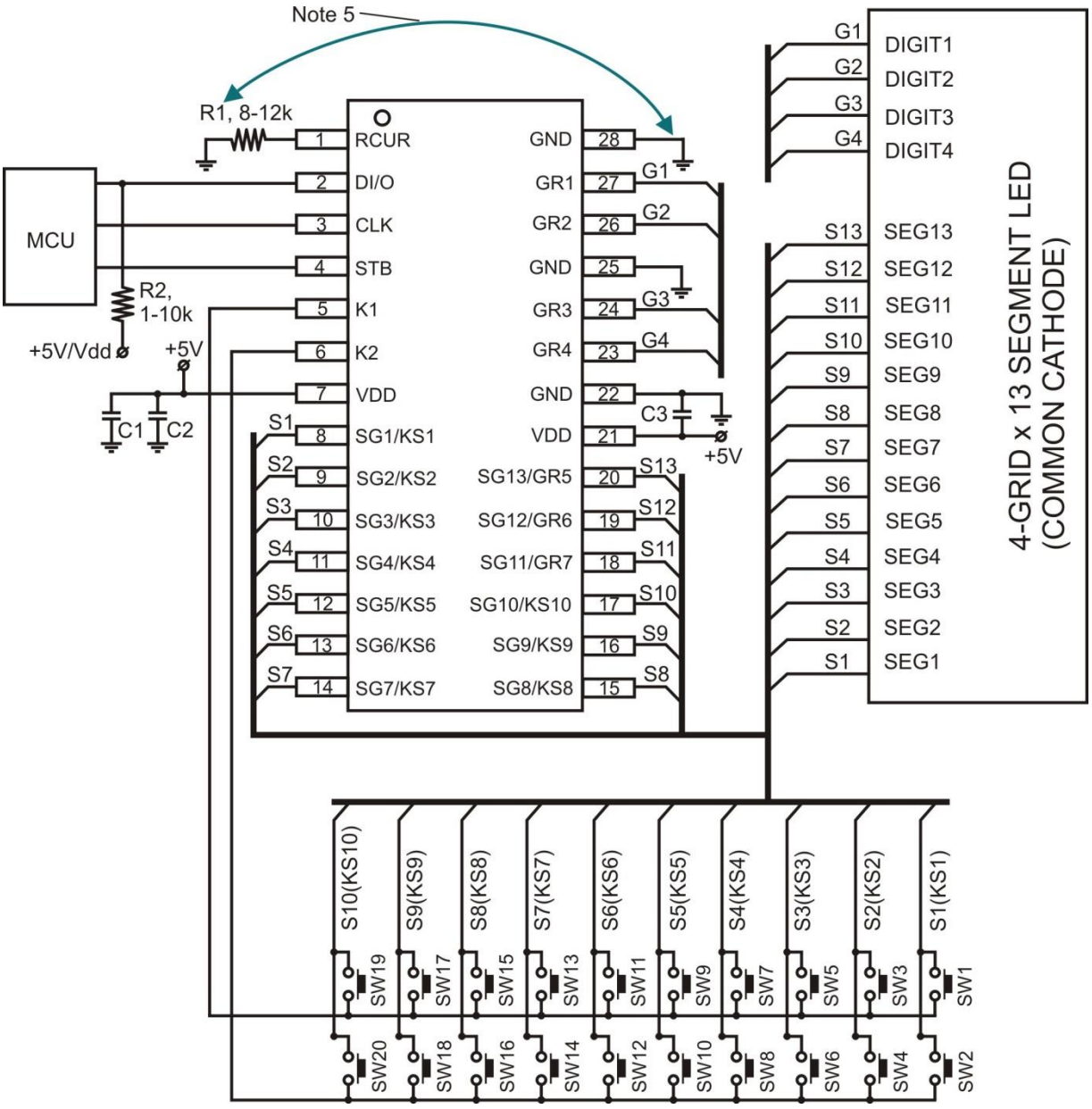


Oscillation Frequency



Remark: graphs are only V_{DD} = 5V

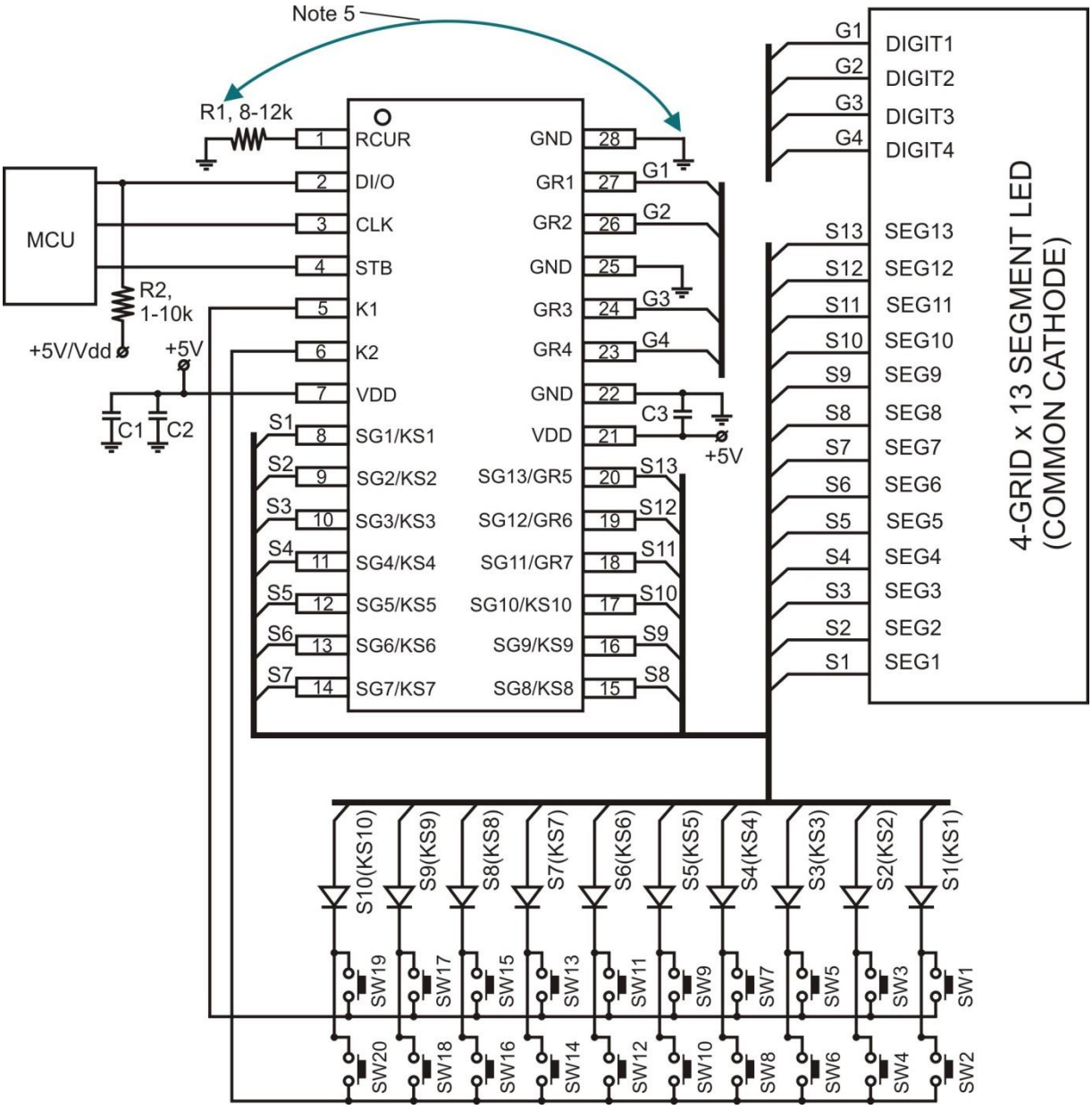
APPLICATION CIRCUIT



Note:
1. Circuit is for V_{DD} =5V
   When V_{DD} =3.3V, Recommend R1 = 12.1kOhm.
2. The capacitors (0.1uF) connected between the GND and V_{DD} Pins must be located as near as possible to the IK2102 chip.
3. IK2102 power supply is separate from the application system power supply.
4. For increase stability of IC and reduce noise, C1 & C2 should be placed closer to 7 pin and C3 should be placed closer to 21pin.
5. Ground of R1 should be routed directly to pin (28), not though common GND.

Recommend value
C1&C3 0.1uF-ceramics
C2 470uF ~ 1000uF

APPLICATION CIRCUIT (IK2102, key scan with diodes)

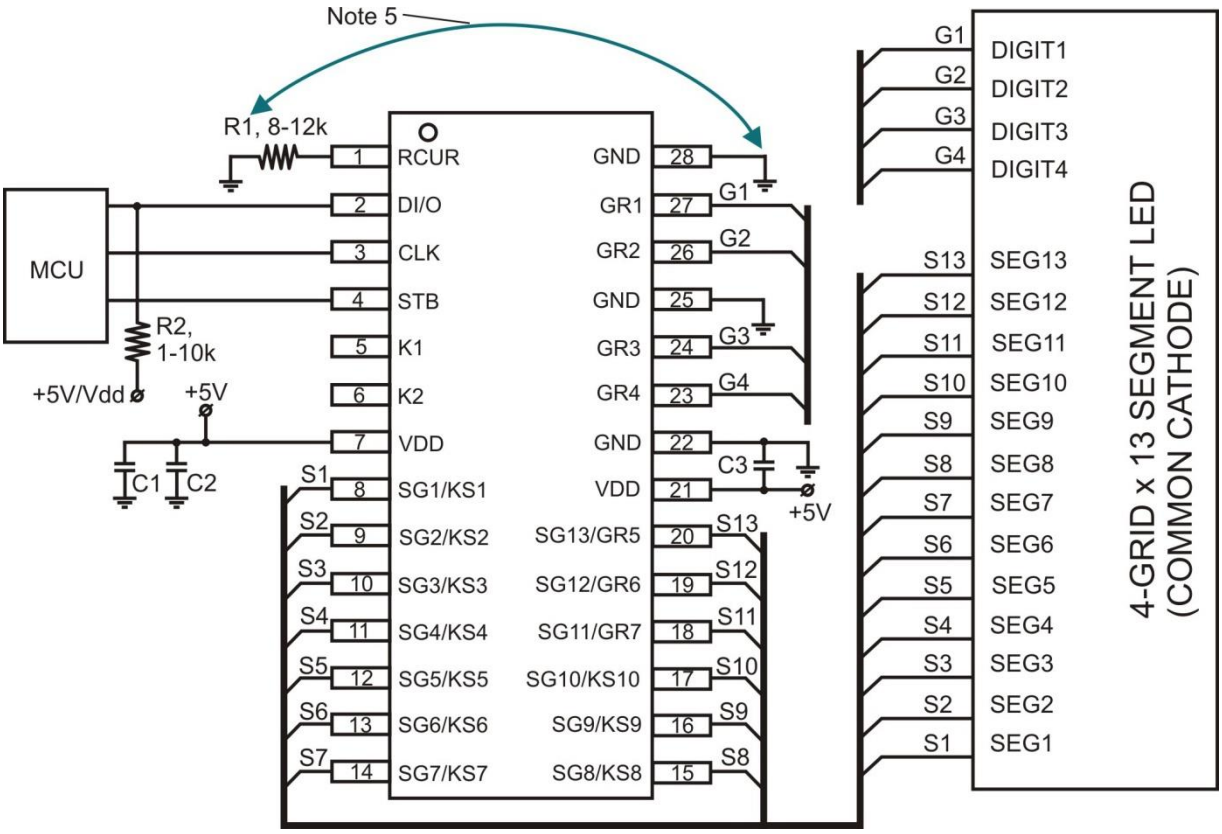


Note:

1. Circuit is for V_{DD} =5V
   When V_{DD} =3.3V, Recommend R1 = 12.1kOhm
2. The capacitors (0.1uF) connected between the GND and V_{DD} Pins must be located as near as possible to the IK2102 chip.
3. IK2102 power supply is separate from the application system power supply
4. For increase stability of IC and reduce noise, C1 & C2 should be placed closer to 7 pin and C3 should be placed closer to 21pin.
5. Ground of R1 should be routed directly to pin (28), not though common GND.

Recommend value
C1&C3 0.1uF - ceramics
C2 470uF ~ 1000uF

APPLICATION CIRCUIT (IK2102 without key scan)

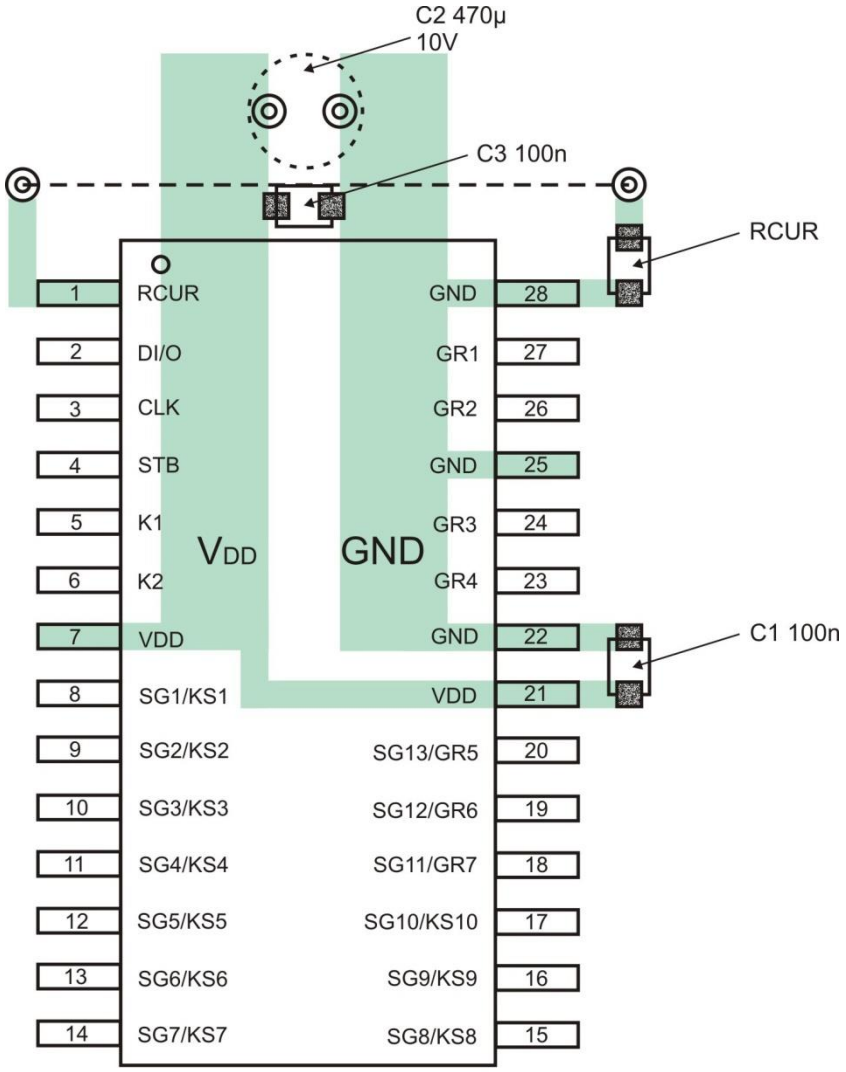


Note:

1. Circuit is for V_{DD} =5V
   When V_{DD} =3.3V, Recommend R1 = 12.1kOhm
2. The capacitors (0.1uF) connected between the GND and V_{DD} Pins must be located as near as possible to the IK2102 chip.
3. IK2102 power supply is separate from the application system power supply
4. For increase stability of IC and reduce noise, C1 & C2 should be placed closer to 7 pin and C3 should be placed closer to 21pin.
5. Ground of R1 should be routed directly to pin (28), not though common GND.

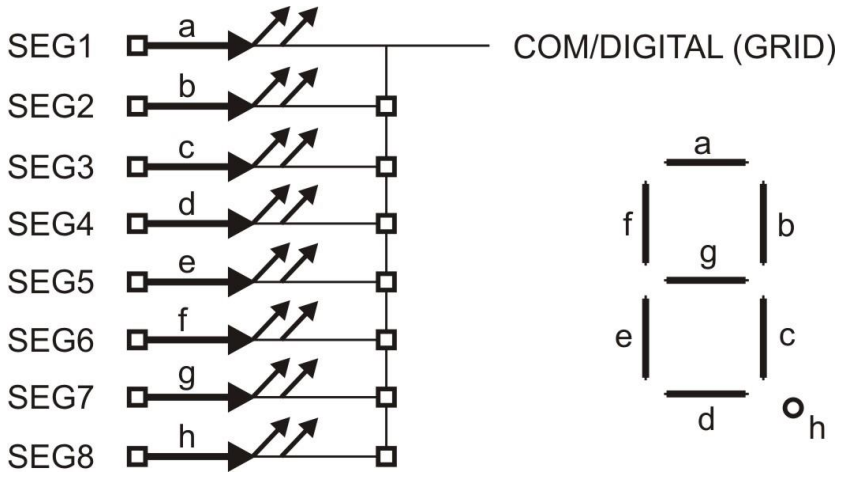
Recommend value
C1&C3 0.1uF-ceramics
C2 470uF ~ 1000uF

Recommended Layout for GND and Vcc buses



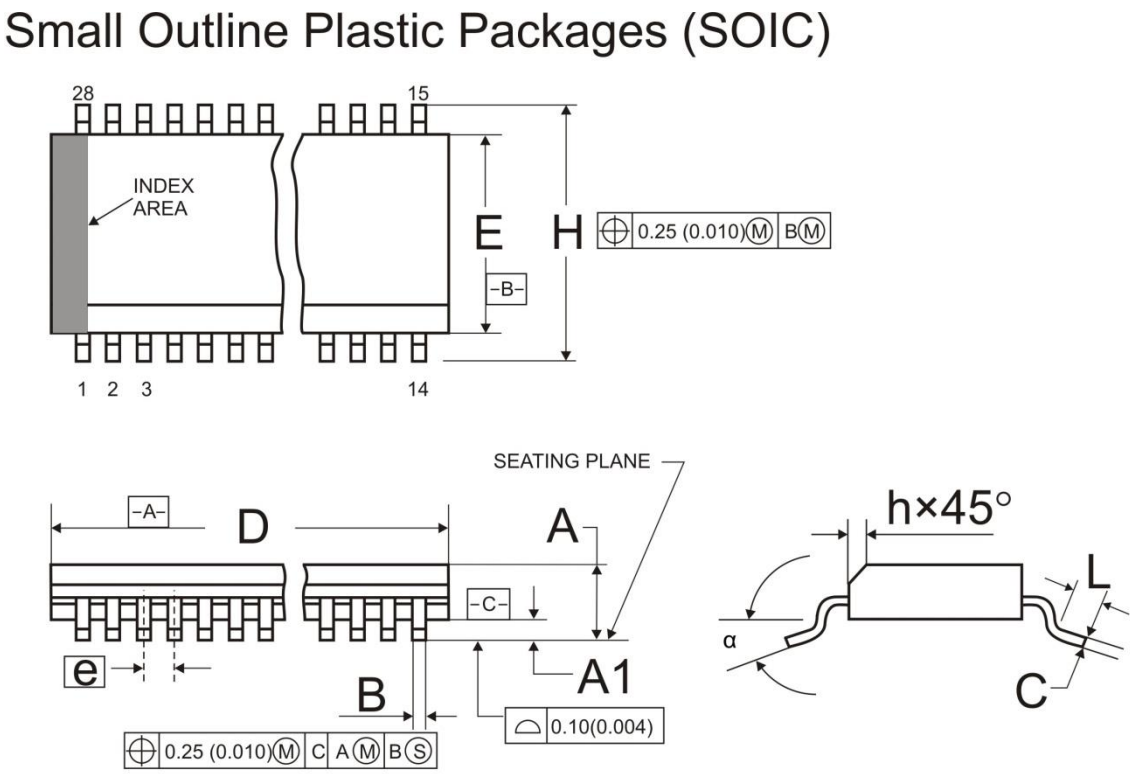
Layout consideratuions

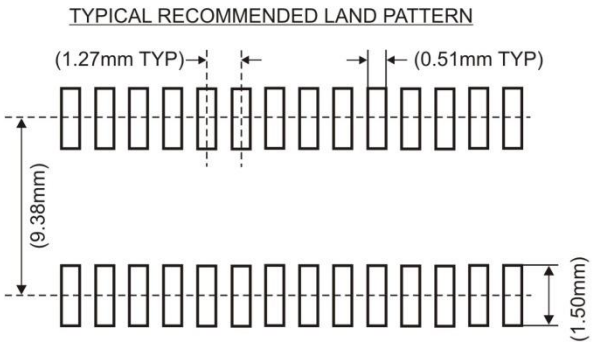
COMMON CATHODE TYPE LED PANEL



PACKAGE DIMENSIONS

28SOP

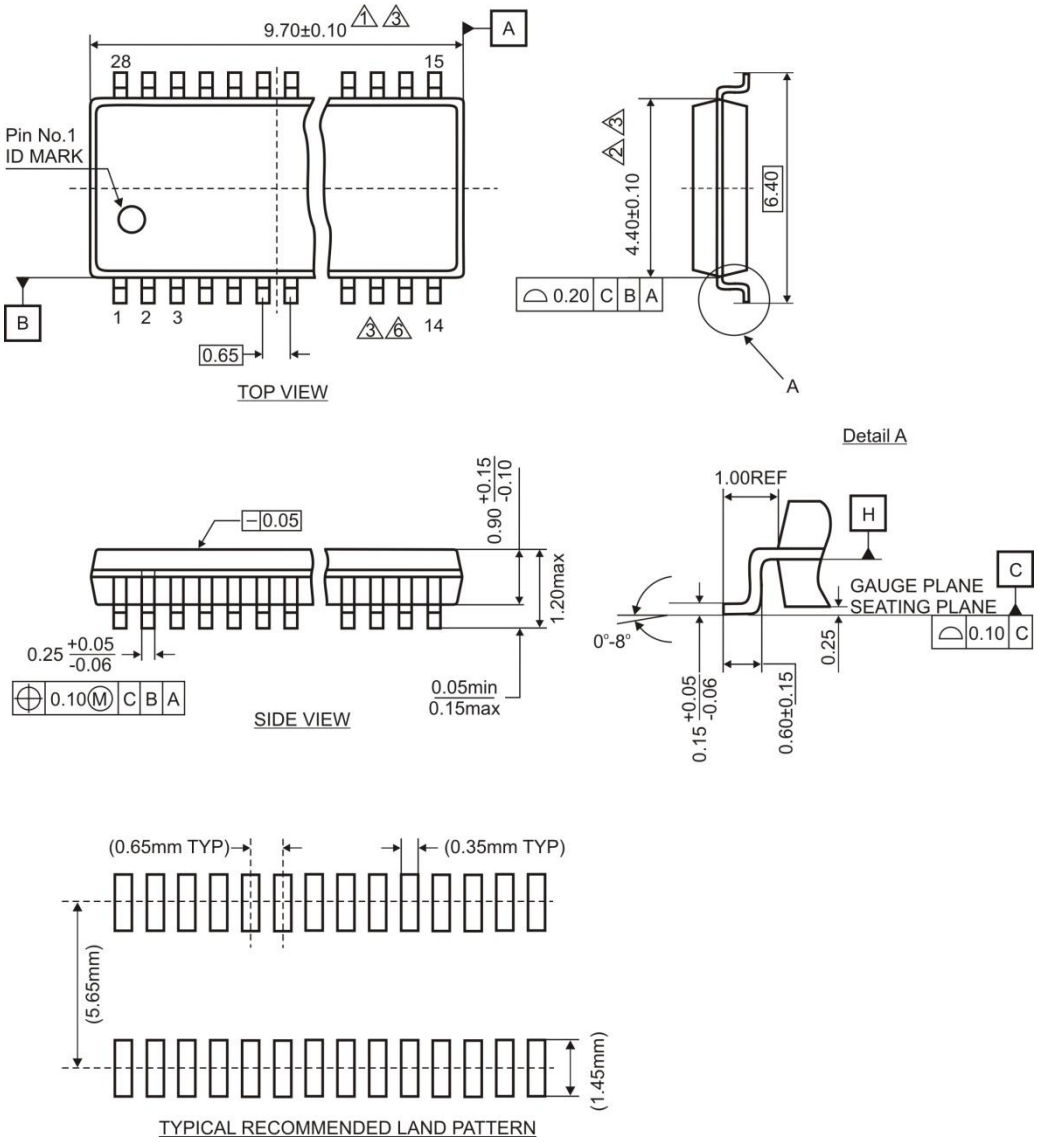




Symbol	Min	Max	Notes
A	2.35	2.65	-
A1	0.10	0.30	-
B	0.33	0.51	9
C	0.23	0.32	-
D	17.70	18.10	3
E	7.40	7.60	4
e	1.27 BSC		-
H	10.00	10.65	-
h	0.25	0.75	5
L	0.40	1.27	6
N	28		7
α	0^o	8^o	-

NOTES:
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)



NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.

2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.

3. Dimensions are measured at datum plane H.

4 Dimensioning and tolerancing per ASME Y14.5M-1994.

5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.

6 Dimension in ( ) are for reference only.

7 Conforms to JEDEC MO-153.