Chapter Six: Synchronous Sequential Logic Circuit

1. **True or False.** A modulo-28 counter requires (4) flip flops at least.

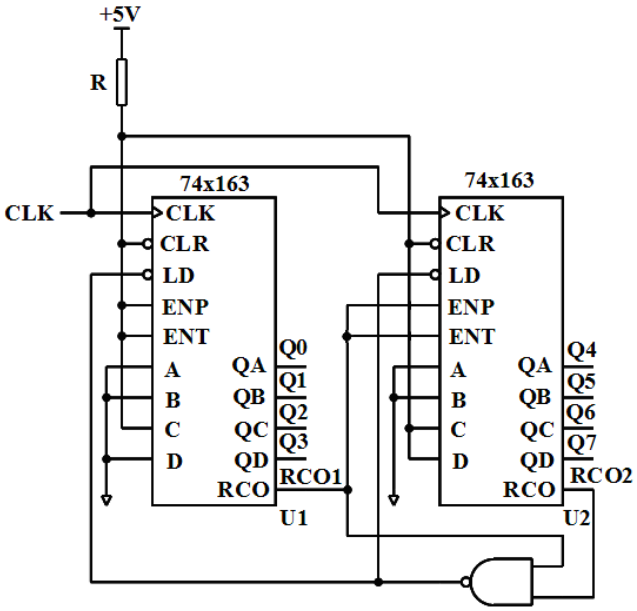
2. **True or False.** A circuit is called (Moore) when the output depends not only on its states but also on the input.

3. **True or False.** The number of valid states is (7) for an 8-bit ring counter.

4. **True or False.** A modulo-264 counter requires (4) 74x163 binary counters at least.

5. **True or False.** To generate a sequence signal 11010111 using shift register, (4) bits are required at least.

6. Analyze the sequential-circuit as shown below, which contains two 74x163 4-bit binary counter.
(1) **True or False.** The logic expression of LD_L(RCO1, RCO2) for U_1 and U_2 is **LD_L (RCO1, RCO2) = (RCO1·RCO2)**.
(2) **True or False.** Assume the initial state is 196_{10}, the state sequence in a cycle for the circuit is **196, 197, 198…253, 254, 255, 256, 196**.
(3) **True or False.** The modulus for the circuit is **59**.



7. Analyze the clocked synchronous state machine in Figure VI.
(1) **True or False.** The out excitation equations and the output equation are:

$$D_1 = X' \qquad D_2 = (Y+Q_1)Q_3 \qquad D_3 = Y\,Q_2 + Q_1'$$

$$Z = Q_1'\,Q_2\,Q_3$$

(2) List out the transition/output table (Table VI).

(3) Assume the initial state $Q_3Q_2Q_1$=000, draw the timing diagram for Q_3, Q_2, Q_1 and Z.

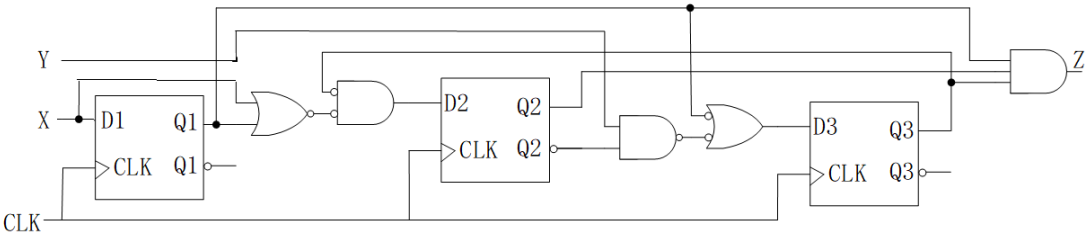
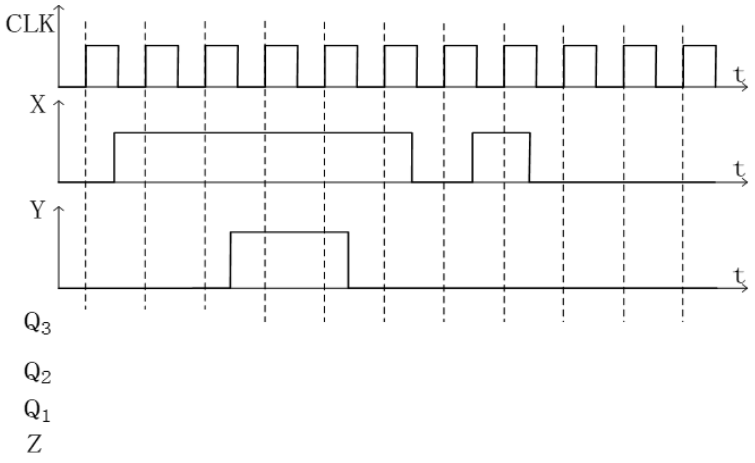


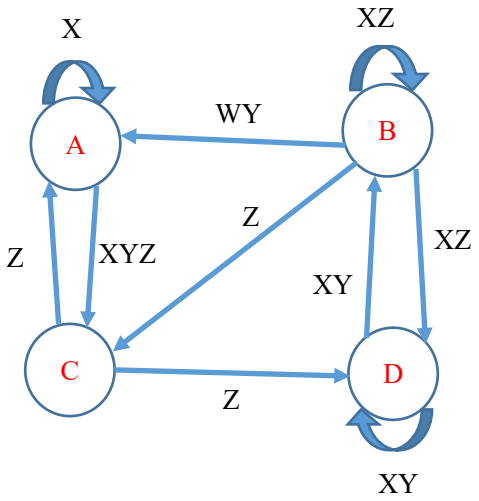
Figure VI

Table VI Transition/output Table

S	XY				Z
	00	01	10	11	
000					
001					
010					
011					
100					
101					
110					
111					
$Q_3Q_2Q_1$	$Q_3^*\ Q_2^*\ Q_1^*$				



8. **True or False.** States (**A and C**) in the figure are ambiguous.

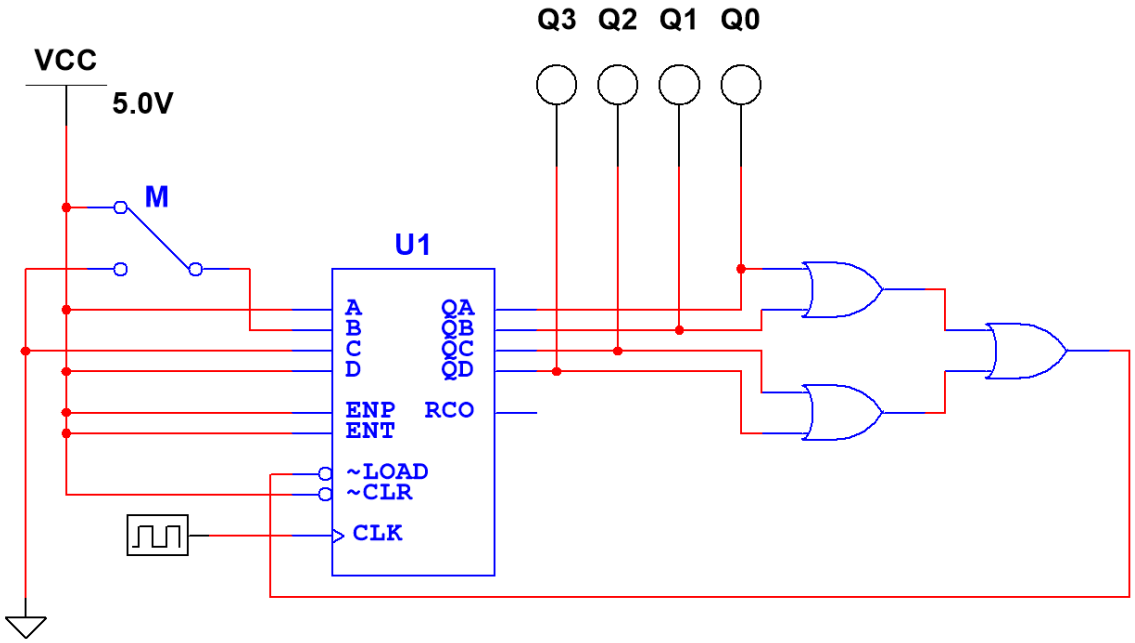


9. **True or False.** To implement a module 29 counter，we need at least （ **4** ） flip-flops.

10. **True or False.** For a five bit binary adder counter, suppose the initial state is 00000, then after 74 clocks, its state should be (_____**01011**_____).

11. Synchronous Logic Analysis.

Analyze the synchronous sequential logic circuit shown in the following figure which contains a 74x163 counter and some OR gates.



The function table for the 74X163 counter

Input					Current States	Next States
CLK	CLR	LOAD	ENT	ENP	QD QC QB QA	QD* QC* QB* QA*
0	X	X	X	X	QD QC QB QA	QD QC QB QA
1	X	X	X	X	QD QC QB QA	QD QC QB QA
↑	0	X	X	X	X X X X	0 0 0 0
↑	1	0	X	X	X X X X	D C B A
↑	1	1	0	X	QD QC QB QA	QD QC QB QA
↑	1	1	X	0	QD QC QB QA	QD QC QB QA
↑	1	1	1	1	0 0 0 0	0 0 0 1
↑	1	1	1	1	0 0 0 1	0 0 1 0
↑	1	1	1	1	…….	……..
↑	1	1	1	1	1 1 1 1	0 0 0 0

(1) **True or False.** The function for the LOAD signal in the figure is LOAD = QA+QB+QC.

(2) **True or False.** When M=1, the state sequence is 1011->1100->1101->1110->1111->1011.

(3) **True or False.** The function of the circuit is a 16-number addition counter.

12. Synchronous Logic Design.

(1) Design a clocked synchronous state machine with one input X, and a single Moore type output Z that is 1 if X had the same value at **every two** or **more than** two positive edges. Otherwise, the

output should be 0. Please fill in the blanks in the following state table.

State	The meaning of each state	Input		Output
		X=0	X=1	Z

(2) Suppose there is a synchronous state machine with the input X, state Q2Q1, output Z， and the transition table is shown in the following table. Please implement it by JK flip-flops and other Small Scale Integration gates, write out the excitation and output function.

Input X	Current State		Next State		Output Z
	Q_2^n	Q_1^n	Q_2^{n+1}	Q_1^{n+1}	
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	1	1	0