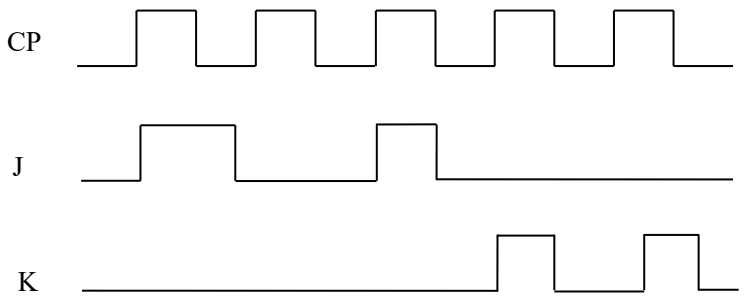
1. Please draw the waveform of the output Q of the negative edge J-K flip-flop. The clock signal CP, excitation signals J and K are drawn in the following figure. Assume that the initial value of Q is “0”.

1. 请根据下面的时钟信号 CP，激励信号 J 和 K，画出下降沿 J-K 触发器的输出 Q 的波形。假设触发器的初始状态值 Q 为“0”。



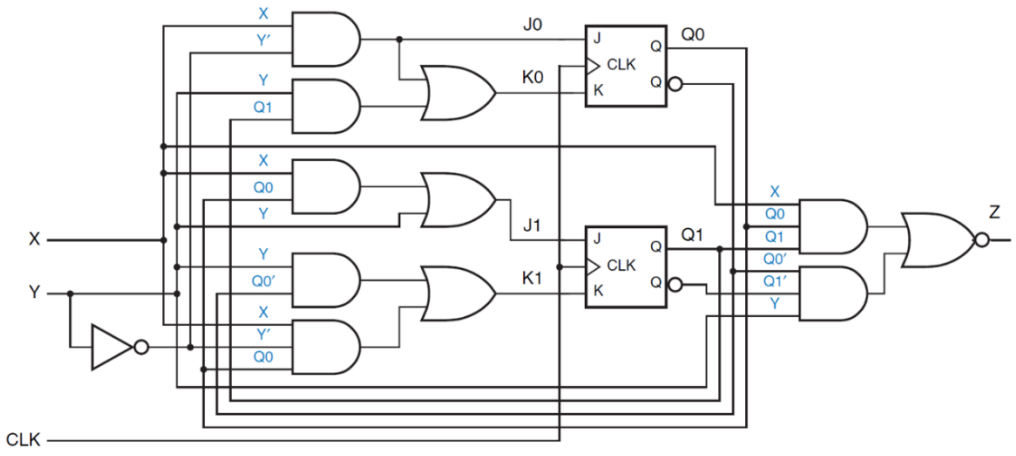
2. Please use the Verilog structural style or dataflow style to describe the following logic functions.

2. 请使用 Verilog 代码的“门级”描述或“数据流级”描述，编程实现下列逻辑函数。

$$G = (W + \overline{Z}) \bullet (X + Y + Z)$$

3. Analyze the synchronous sequential logic circuit shown in the following figure, write the output and excitation functions, write the state table, and draw the corresponding state diagram. The state A, B, C, D is Q1Q0=00，01，10，11 respectively.

3. 分析下列同步时序逻辑电路，写出输出方程和激励方程，写出状态表，画出状态图，状态 A，B，C，D 分别对应 Q1Q0=00，01，10，11。



4. Design a counter with J-K flip-flops. The cycle is “000→100→011→111→010→000”. When the state is “010”, the output value is “1”; Otherwise, the output value is “0”. Please write the state table, Karnaugh map, state equation, output equation and excitation equation. Check whether it can be started automatically, if it can't start automatically, describe the solution.

4. 请使用 J-K 触发器设计循环为“000→100→011→111→010→000”的计数器。当计数到“010”时，输出值为“1”；否则，输出值为“0”。包括：写出状态表，画出卡诺图，写出状态方程、输出方程和激励方程。检查是否能够自启动，若不能自启动，请说出解决办法。