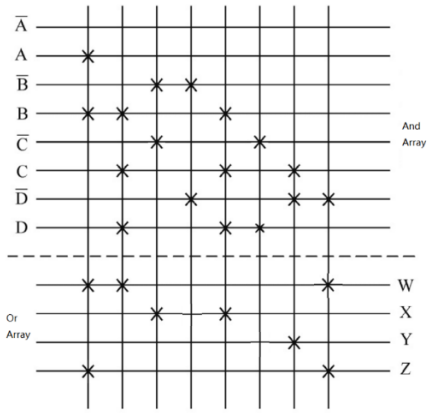
1. The following circuit is composed of programmable logic array (PLA) device. Write the function of W, X, Y and Z. Describe this circuit with Verilog.

1. 分析下列采用可编程逻辑阵列（PLA）器件组成的电路图。写出 W、X、Y、Z 的表达式，采用 Verilog 进行描述。

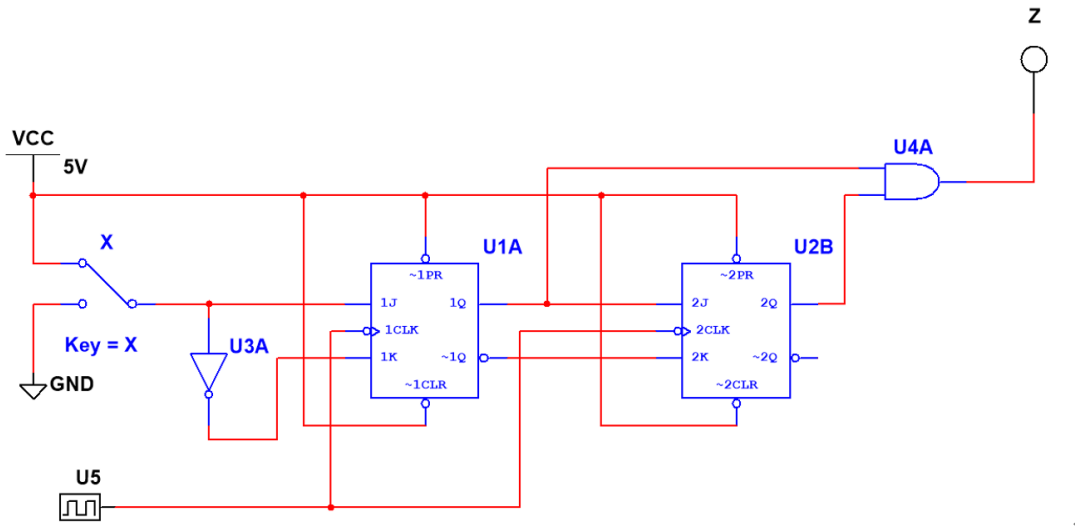


2. Analyze the synchronous sequential logic circuit shown in the following figure.

(1) Write the Boolean functions of output, excitations and state variables.

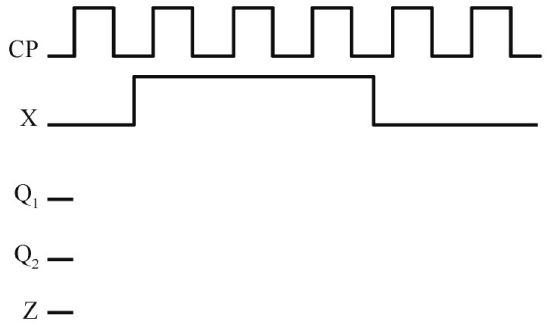
2. 分析下图所示同步时序逻辑电路。

（1）写出输出函数、激励函数和次态函数表达式。



(2) Let the initial state of the flip-flops be 00, and draw the output waveforms of Q1, Q2 and Z.

（2）设触发器的初态为 00，画出 Q1、Q2 和 Z 的输出波形。



3. Try to implement a synchronous sequential circuit that recognizes the input sequence consisting of “0010” with JK flip-flop and other small-scale logic gates (The input can be overlapped; the output is Mealy type). Assign the states according to the binary number 00, 01, 10 and 11.

3. 试用 JK 触发器和其它小规模逻辑门电路实现一个识别“0010”串行序列检测器（输入可重叠，输出为 Mealy 型），状态编码按照二进制 00，01，10，和 11 编码。