

# LOW-IMPEDANCE SHIELDED TIP PIEZORESISTIVE PROBE ENABLES PORTABLE MICROWAVE IMPEDANCE MICROSCOPY

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## ABSTRACT

We present new scanning probes suitable for Microwave Impedance Microscopy measurements on any scanning platform using a piezoactuator. We microfabricated piezoresistive cantilevers integrated with low-impedance, electrically-shielded transmission lines to enable simultaneous topographical and electrical scanning probe microscopy. The probes provide topography feedback with nanometer vertical resolution for samples or setups where laser detection is not feasible or desirable. MIM is a scanning probe technique that utilizes the interaction of a GHz electrical signal with a sample and yields a conductivity map of the sample at the nanoscale. Our new design exhibits vertical displacement resolution of 3.5 nm in a measurement bandwidth from 1 Hz to 10 kHz. The capacitance between shield and inner conductors measured with an impedance analyzer is 9.5 pF and the trace resistance is 32 Ω. We have demonstrated sample location and topographic scanning capabilities using the self-sensing piezoresistor.

## INTRODUCTION

### Paper Length

Since the development of Atomic Force Microscopy (AFM) by Binning and Quate in 1986 [1], Scanning Probe Microscopy (SPM) is gaining increasing interest in various fields such as electronics [2], material science [3] and biology [4]. In particular, applications using microwave signals have emerged to study local electronic properties of materials. Microwave Impedance Microscopy (MIM) has demonstrated great promise for mapping local electronic properties [5,6]. MIM enables the study of local complex dielectric constants in novel electronic materials. MIM uses radio frequency (RF) signals (~1 GHz) to measure the local tip-sample impedance. The RF signal is guided to the tip and is reflected at the tip-sample interface. The near-field interaction at the tip-sample interface yields information about the complex dielectric constants of the sample. As the tip scans across the sample, the reflected signal changes, providing the map of electrical properties. Because the dimension of the tip-sample interaction is much smaller than the wavelength at 1 GHz, the spatial resolution is determined by the size of the tip apex. While recent probes have capacitance and resistance as low as 1 pF and 5 Ω respectively [7], they rely on optical beam bounce for topography feedback. This technique is effective at room temperature, but when photosensitive materials are studied at cryogenic temperature, stray photons from the laser can produce excitations in the

sample that decay over long time scales. This creates a challenge for aligning the tip and the sample.

Piezoresistivity is the change in resistivity in a material in response to a mechanical stress. This effect is widely used as a transduction mechanism in MEMS/NEMS devices, such as pressure sensors [8], force sensors [9] and accelerometers [10]. Although laser detection for AFM still gives the best resolution, the latest research in single crystal silicon piezoresistive cantilevers has demonstrated sub-nanometer resolution at room temperature [11].

In this paper we present the design and fabrication of a low-impedance shielded tip piezoresistive probe. The self-sensing cantilever allows topography feedback where laser beam bounce technique is not available or hard to implement. Furthermore, the low parasitic impedance of the tip enables MIM measurements.

## DESIGN AND FABRICATION

### Design

To leverage the repeatable mechanical properties of single crystal silicon [12], we used it as the main material for our cantilever and tip. Single crystal silicon also exhibits significant piezoresistivity [13], which we used to develop a self-sensing probe.

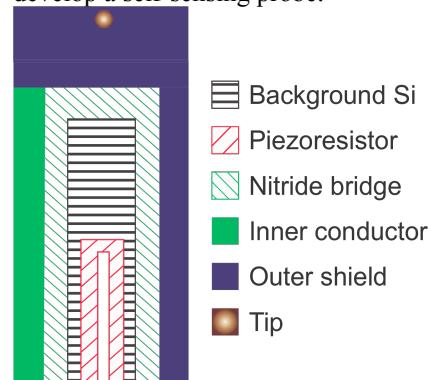


Figure 1: Sketch of the probe designed with all the features and materials. The background silicon between the piezoresistor legs is etched to minimize leakage current. The inner conductor and outer shield are both made with aluminum and are deposited on the nitride before connecting the tip.

Since heavily-doped silicon has a higher parasitic capacitance and resistance compared to metal conductors such as aluminum or gold, we used a 0.5 μm thick aluminum layer as the inner conductor to the tip. To further reduce the parasitic impedance, we separated the tip and the main cantilever structure with a strip of silicon nitride to electrically isolate both parts. The nitride strip is

also used to support the metal lines connected to the tip (Figure 1) and isolate them from the background silicon. We designed probes with three different lengths, corresponding to three different stiffnesses to accommodate for contact and tapping mode as well as soft samples. The targeted spring constant of the cantilevers were 1, 10 and 15 N/m.

The piezoresistor geometry and doping profile were designed using a Matlab optimization code previously reported by J.C. Doll et al. [14]. Indeed, the minimum detectable force  $F_{\min}$  was optimized according to the design bounds such as stiffness, bandwidth and power dissipation. We calculated  $F_{\min}$  by dividing the total integrated voltage noise  $V_{noise}$  by the force sensitivity  $S_{FV}$ . The two dominant noise sources considered were Johnson and Hooge noise [15].

$$F_{\min} = \frac{V_{noise}}{S_{FV}} \quad (1)$$

The force sensitivity is defined by geometrical parameters and process parameters:

$$S_{FV} = \frac{3(l_c - 0.5l_p)\pi_{l,max}}{8w_p t_c^2} \gamma V_{bridge} \beta^* \quad (2)$$

where  $l_c$  is the cantilever length,  $l_p$  is the piezoresistor length,  $w_p$  is the piezoresistor width,  $t_c$  is the cantilever thickness,  $\pi_{l,max}$  the longitudinal piezoresistive coefficient,  $\gamma$  is the contact resistance ratio  $V_{bridge}$  is the Wheatstone bridge bias voltage and  $\beta^*$  is the doping correction factor [14]. Although we need to optimize the minimum detectable displacement  $d_{\min}$  for an AFM probe design, we can easily reformalize this using Hooke's law as previously reported [15]

$$F_{\min} = k \cdot d_{\min}, \quad (3)$$

where  $k$  is the cantilever stiffness. Therefore the displacement sensitivity  $S_{dV}$  and  $d_{\min}$  can be experimentally measured using equation (4) and (5).

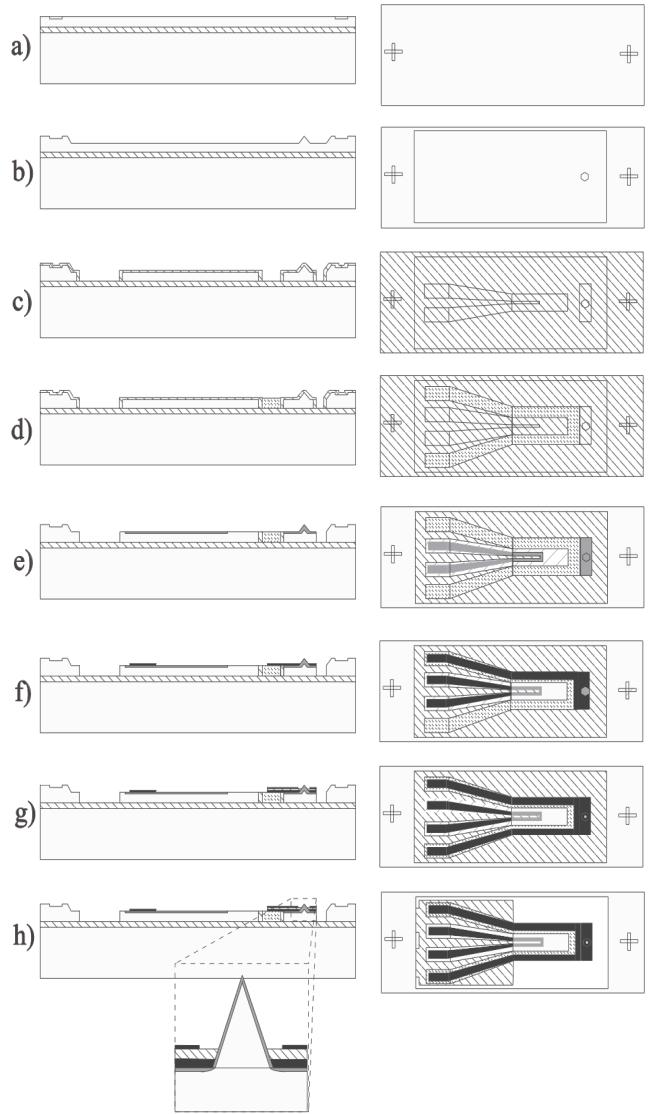
$$S_{dV} = \frac{\Delta V}{d} \quad (4)$$

$$d_{\min} = \frac{V_{noise}}{S_{dV}} \quad (5)$$

### Fabrication process

We started with (100) single crystal silicon on insulator (SOI) wafers with an 8.5  $\mu\text{m}$  thick device layer, a 0.5  $\mu\text{m}$  buried silicon oxide (BOX), and a 400  $\mu\text{m}$  handle layer. The device layer and handle wafer were p-type silicon with a resistivity of 1-5 and 0.05-0.1  $\Omega\cdot\text{cm}$ , respectively. Throughout the process, the wafers were singed and primed at 150°C in hexamethyldisilazane (HMDS) before spinning resist. The photoresist was exposed using an ASML PAS5000/60 5:1 reducing stepper. In addition, because we designed the piezoresistor with n-type doping, the wafers were rotated 45° to maximize the piezoresistive coefficient [13].

As illustrated in Figure 2, the fabrication process consisted of eight photolithography steps. After cleaning the wafer in Piranha (20 min in 9:1  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  at 120°C), we patterned alignment marks in 1  $\mu\text{m}$  SPR 3612 photoresist, etched them 1200 Å deep with a  $\text{CHF}_3/\text{O}_2$  plasma and stripped the resist in Piranha.



□ p-type Silicon □ Silicon dioxide □ Silicon nitride

■ n-type Silicon ■ Aluminum

Figure 2: Process flow. a) Alignment marks were etched in silicon using Reactive Ion Etching (RIE) b) silicon tips were created by KOH anisotropic etch c) cantilever and die were patterned in silicon with Magnetic Enhanced Reactive Ion Etching (MERIE) d) tips were sharpened by thermal oxidation and nitride was deposited and etched with MERIE e) piezoresistor and tip were doped by phosphorus diffusion f) metal inner conductor and piezoresistor contact pads were deposited and wet etched g) passivation LTO and shield metal were deposited and patterned using wet etching h) devices were backside etched using Deep Reactive Ion Etching (DRIE) and released with RIE.

Next, we RCA cleaned (10 min 4:1  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  at 90°C, 10 min in 5:1:1  $\text{H}_2\text{O}:\text{HCl}:\text{H}_2\text{O}_2$  at 70°C and 30 s in 50:1 HF) then oxidized the wafer for 39 minutes at 1000°C in a wet atmosphere to grow a 5000 Å thick oxide mask. We spin coated 1.6  $\mu\text{m}$  thick SPR 3612 photoresist film and patterned circles with 4.5  $\mu\text{m}$  radius. We etched the oxide mask in a  $\text{CHF}_3/\text{O}_2$  plasma and removed the resist in piranha. We created the 6  $\mu\text{m}$  tall tips by undercutting the oxide mask in 45% KOH at 70°C for 22

min. Then we cleared the oxide in 6:1 BOE ( $H_2O_2$ : $NH_4F$ /HF).

Then, the cantilever structure was defined in 7  $\mu m$  thick SPR 220-7 photoresist and etched in a HBr/Cl<sub>2</sub>/O<sub>2</sub> plasma. We stripped the resist in piranha and sharpened the tips by growing a 200 nm thick oxide at 900°C in a wet atmosphere [16].

We then deposited a 2  $\mu m$  thick silicon rich LPCVD silicon nitride film at 600 °C, followed by a 200 nm thick low temperature oxide (LTO) film at 400 °C. We defined the nitride isolation structure into 7  $\mu m$  thick photoresist, etched the LTO mask in 6 : 1 BOE and cleaned the resist in Piranha. We finally etched the silicon nitride for 15h in 85%  $H_3PO_4$  at 155 °C.

Next, we patterned 7  $\mu m$  of resist and etched the remaining oxide from the tip sharpening step in 6 : 1 BOE to define the piezoresistor and inner conductor to the tip. We stripped the resist in Piranha and doped the wafer by phosphorus diffusion with POCL<sub>3</sub> for 15 minutes at 900°C. We cleared the oxide in 6:1 BOE.

To create the tip inner conductor and piezoresistor's contacts, we sputtered 0.5  $\mu m$  of aluminum and wet etched in AL-11 aluminum etchant (25:8:1:1  $H_3PO_4$ : $H_2O_2$ : $CH_3COOH$ : $HNO_3$ ) at 40°C with a 7  $\mu m$  resist mask. We cleaned the photoresist in PRX-127.

We deposited a 500 nm thick LTO layer as an isolator layer followed by 200 nm of sputtered aluminum as a shield layer. The aluminum and oxide were patterned with a 7  $\mu m$  thick photoresist in aluminum etch and pad etch, respectively, to define the shield metal layer and open contacts to the inner conductor and piezoresistors.

Finally, to define the backside of the wafer, we spun and patterned 7  $\mu m$  of resist. We then protected the frontside of the wafer with 10  $\mu m$  resist. We etched the handle layer silicon with deep reactive ion etching (DRIE) and the BOX with a CHF<sub>3</sub>/O<sub>2</sub> plasma. The photoresist was cleared in PRX-127 followed by a final clean in PRS-1000. A finished device image is shown in Figure 3.

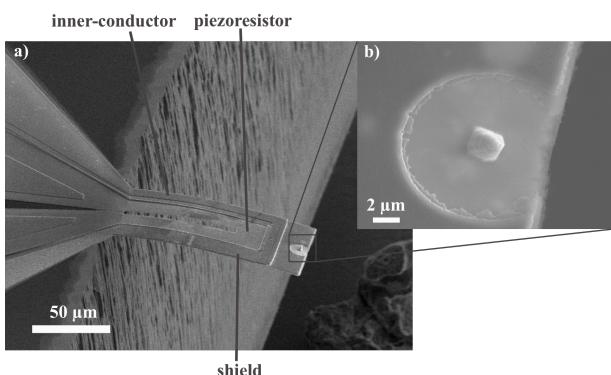


Figure 3: a) SEM image with 52° of tilt of a finished device showing piezoresistor, tip inner conductor and shield metal. b) Top view and close up of the tip. The circle around the tip is where the shielding is opened.

## RESULTS

The cantilever piezoresistor was connected to three metal film resistors to form a Wheatstone bridge configuration. Then, the bridge output was amplified with a low-noise instrumentation amplifier, TI INA103. The signal conditioning circuit displayed a lower noise floor than our piezoresistor (Figure 4). The noise was measured utilizing a signal analyzer HP8568a.

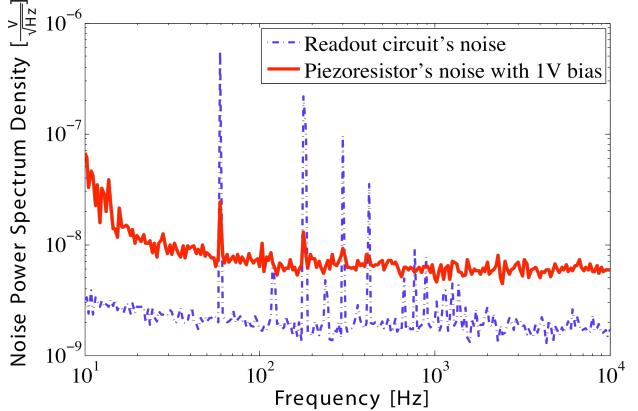


Figure 4: Piezoresistor and read-out circuit noise spectra. Both curves are showing a 1/f noise regime at low frequency and a Johnson noise regime at high frequency. As expected the piezoresistor noise is much larger than the read-out circuit noise. The latter does not alter the probe resolution.

To measure the probe displacement sensitivity, we mounted a probe on a Witec α300 AFM system. Next, we engaged the tip with a glass slide and used the amplified piezoresistor's output as the feedback signal. We then performed a force displacement curve and recorded the piezoelectric stage position and piezoresistor output to obtain the sensitivity of the device. The resolution was calculated as the integrated the noise spectrum in a given bandwidth divided by the sensitivity (Figure 5). The resolution in a bandwidth from 1 Hz to 10 kHz was found to be 3.5 nm.

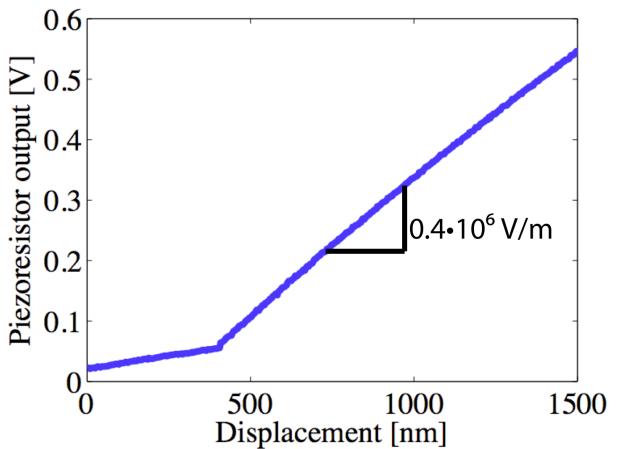
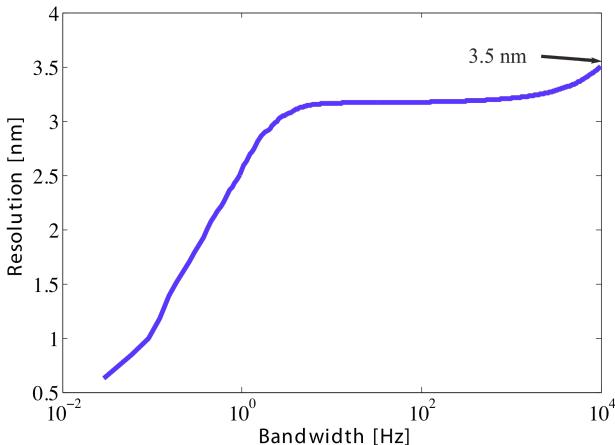
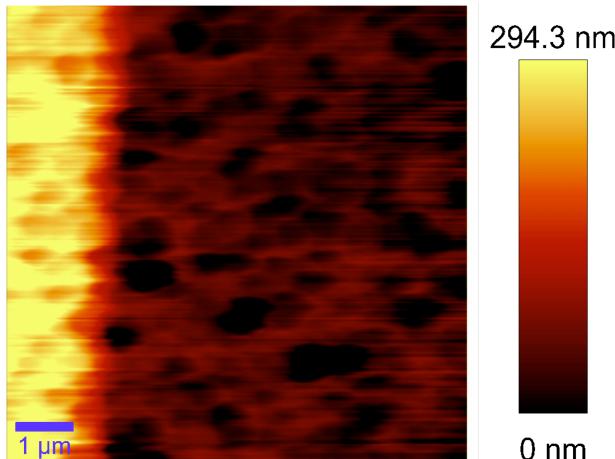


Figure 5: Plot of the piezoresistor output versus AFM stage position while doing a force displacement curve. The slope shows a sensitivity of  $0.4 \times 10^6$  V/m with an amplifier gain of 1000.



*Figure 6: Displacement resolution versus bandwidth. The resolution degrades with larger bandwidth increases due to increased noise. This probe shows a 3.5 nm resolution when used in the designed bandwidth of 1 Hz - 10 kHz.*

We performed contact mode AFM scans on 300 nm thick patterned aluminum electrodes deposited on silicon dioxide. Our probe clearly resolved the electrode and thus was capable of locating the sample of interest for further MIM studies.



*Figure 7: Topography of an aluminum electrode on silicon dioxide using piezoresistive feedback. Z-axis is given by the piezoelectric stage output. The measurement was made at room temperature. The image clearly show the aluminum electrode location.*

## CONCLUSION

We report the design and fabrication of a piezoresistive cantilever with a low-impedance conduction line to our electrically-shielded tip. The self-sensing piezoresistive probe has a displacement resolution of 3.5 nm. We demonstrate topography scans using piezoresistive feedback. This probe will enable coupled topography scans with MIM images. Although the capacitance and resistance of the tip is not as low as previously reported probes, the measured impedance suggests MIM measurements can be obtained in a self-sensing mode, though with decreased MIM sensitivity and thus contrast.

## ACKNOWLEDGEMENTS

Fabrication work was performed in part at the Stanford Nanofabrication Facility (a member of the National Nanotechnology Infrastructure Network) supported by the NSF under Grant ECS-9731293, its lab members, and the industrial members of the Stanford Center for Integrated Systems. This work was supported by the National Science Foundation (NSF) under Grant No. ECCS-0708031, NSF NSEC Center for Probing the Nanoscale (CPN) Grant No. PHY-0425897 and a CPN fellowship to AJH. The authors would like to thank J.C. Doll, A.J. Rastegar, S. Sadeghipour as well as the Stanford Nanofabrication Facility staff for their advice and help.

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