Code No: **RT41041** **R13** **Set No. 1**

IV B.Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2018

VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) Compare CMOS, Bipolor, BiCMOS technologies? [4]
   b) Write a note on the general observation about design rules. [3]
   c) Explain the criteria for choice of layers. [4]
   d) Draw the typical architecture of PLA. [3]
   e) Write a short note on SoC Design. [4]
   f) List the applications of FPGA. [4]

PART–B *(3x16 = 48 Marks)*

2. a) What are the steps involved in the nMOS fabrication? Explain with neat sketches. [8]
   b) Derive the relationship between drain to source current I_{ds} verses drain to source voltage V_{ds} in non-saturated and saturated region. [8]

3. a) What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter. [8]
   b) Explain about double poly CMOS rules. [8]

4. a) Explain the concept of sheet resistance and apply it to compute the ON resistance (VDD to GND) of an NMOS inverter having pull up to pull down ratio of 4:1, If n channel resistance is Rsn =104 Ω per square. [8]
   b) What is inverter delay? How delay is calculated to for multiple stages? [8]

5. a) Explain switch logic and its arrangements? And also explain properties of transmission gate. [8]
   b) Discuss the general arrangement of a 4-bit arithmetic process. [8]

6. a) Explain the importance of package selection. [8]
   b) Explain the importance of design for testability. [8]

7. a) Explain about building block architecture of FPGA. [8]
   b) Explain the design flow using FPGA. [8]

Code No: **RT41041** **R13** **Set No. 2**

IV B.Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2018

VLSI DESIGN

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1.	a)	Define threshold voltage of a MOS device and explain its significance.	[4]
	b)	Explain how stick diagrams can be used for layout diagrams.	[3]
	c)	Write short notes on area capacitances of layers.	[4]
	d)	Explain a four line Gray code to Binary code converter.	[4]
	e)	Write a short note on mixed signal design.	[3]
	f)	List out the steps in FPGA design flow.	[4]

PART–B *(3x16 = 48 Marks)*

2.	a)	Explain the processing steps used in IC fabrication process.	[8]
	b)	Derive the expression for the ratio between Zp.u and Zp.d if an nMOS inverter is to be driven from another nMOS inverter.	[8]
3.	a)	Design a stick diagram for inverter using CMOS.	[8]
	b)	Design a layout diagram for CMOS 3-input NAND gate.	[8]
4.	a)	Explain scaling of MOS circuits. Give merits and demerits of scaling.	[8]
	b)	Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.	[8]
5.	a)	Discuss about Two-phase clocking in detail.	[8]
	b)	With an example, Explain about system design.	[8]
6.	a)	Discuss the VLSI design issues and design trends.	[8]
	b)	Explain the ASIC design flow.	[8]
7.	a)	Write the VHDL code to implement stack.	[8]
	b)	Explain the architectural features of FPGA.	[8]

Code No: **RT41041** **R13** **Set No. 3**

IV B.Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2018

VLSI DESIGN

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Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) Define the terms SSI, MSI, LSI and VLSI. [4]
   b) Define stick diagram and layout diagram. [3]
   c) Draw and explain fan-in and fan-out characteristics of CMOS design. [3]
   d) Write short notes on switch logic and its arrangements. [4]
   e) Draw the ASIC design flow. [4]
   f) Explain the functions of LUT based logic block. [4]

PART–B *(3x16 = 48 Marks)*

2. a) With neat sketches explain BICMOS fabrication in an n-well process. [8]
   b) Explain and derive the expressions for MOS transistor parameters g_m, g_{ds} and ω_0. [8]

3. a) Design a layout for CMOS 2-input NOR gate. [8]
   b) Write a short note on 2μm Double Metal, Double Poly, CMOS/BiCMOS rules. [8]

4. a) Explain constituents of wiring capacitance. [8]
   b) What are the limits on logic levels and supply voltage due to noise in scaling? [8]

5. a) Explain bus arbitration logic for n-line bus structured design approach. [8]
   b) Realize the 2-i/p NOR gate using NMOS, PMOS and CMOS technologies. [8]

6. a) Discuss about design for testability in VLSI design. [8]
   b) Draw and explain the FPGA design flow. [8]

7. a) Explain implementation of queue using VHDL [8]
   b) Write the VHDL code to implement four bit shift register. [8]

Code No: **RT41041** **R13** **Set No. 4**

IV B.Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2018

VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) Explain the Latch-up effect in CMOS circuits with suitable diagrams. [4]
   b) Draw the circuit diagram for CMOS two-input NOR gate. [3]
   c) Write short notes on realization of gates using CMOS technology. [4]
   d) Explain a four-bit dynamic shift register. [4]
   e) List out the steps in FPGA design flow. [3]
   f) Write about configuration modes. [4]

PART–B *(3x16 = 48 Marks)*

2. a) Explain the structures of n MOS enhancement mode, depletion mode and p-MOS enhancement mode transistors. [8]
   b) Draw and explain the operation of BiCMOS inverter. [8]

3. a) What is a stick diagram and explain about different symbols used for components in stick diagram. [8]
   b) Design a stick diagram and layout for the CMOS logic shown below.
   Y = $\overline{(AB) + (CD)}$ [8]

4. a) Realize basic gates using NMOS. [8]
   b) Explain scaling factors for device parameters. [8]

5. a) Explain the structured design approach of parity generator. [8]
   b) Explain the design of a 4-bit shifter. [8]

6. a) Explain the stuck at fault model with example. [8]
   b) Explain about the clocking mechanism. [8]

7. a) Explain the FPGA design process. [8]
   b) Explain the concept of sheet resistance. [8]