Code No: R1622023 **R16** SET - 1

II B. Tech II Semester Supplementary Examinations, November - 2018
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	Write first 20 numbers in base-6 system?	(3M)
	b)	What is duality?	(2M)
	c)	Define combinational circuit?	(2M)
	d)	What is PAL?	(2M)
	e)	List out the application of counters?	(3M)
	f)	What is Mealy model?	(2M)

PART -B

2.	a)	convert the following decimal numbers to the indicated base: i) 7562.45 to Octal ii) 1938.257 to hexadecimal iii)175.175 to binary	(7M)
	b)	Construct Hamming code for BCD 0110. Use even parity.	(7M)
3.	a)	Minimization of function f using K-map $f(A,B,C,D) = \sum(0,2,3,4,6,7,8,10) + d(12,13,14,15$	(7M)
	b)	Minimize the given 5 variable function using QM Tabular Method $f = \Sigma (2, 4, 9, 10, 11, 12, 19, 20, 21, 22, 23, 24, 25, 26, 29, 31)$.	(7M)
4.	a)	Draw and explain about BCD adder circuit Excess3 adder circuit	(7M)
	b)	Explain in detail about4-bit digital comparator	(7M)
5.	a)	Implement $f (A,B,C,D) = \sum(0,1,3,5,6,8,9,11,12,13)$ using PROM and explain its procedure	(7M)
	b)	Design and implement Full adder with PLA	(7M)
6.	a)	With the aid of external logic, convert D type flip-flop to a T flip-flop	(7M)
	b)	Explain about decade ripple counter	(7M)
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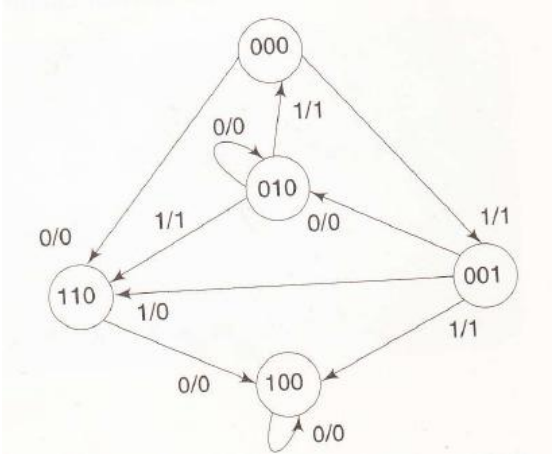
7. a) For the state diagram shown in below fig, design using J-K Flip-flop (7M)



b) Design a sequence detector circuit to detect a serial input sequence of 1010.it should produce an output 1 when the input pattern has been detected. (7M)