Code No: **RT42044C** **R13** **Set No. 1**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2018

LOW POWER VLSI DESIGN

(Electronics and Communications Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1.	a)	Write a note on estimation of glitching power.	[4]
	b)	Explain the power minimization at algorithm level.	[4]
	c)	Explain about static state power estimation.	[4]
	d)	Explain carry save adder and its advantages.	[4]
	e)	What are types of Multiplier architecture?	[3]
	f)	Explain the basics of DRAM.	[3]

PART–B *(3x16 = 48 Marks)*

2.	a)	Explain about switching power dissipation and short circuit power dissipation	[10]
	b)	Briefly explain about velocity saturation.	[6]
3.	a)	List out the comparisons between VTCMOS and MTCMOS circuits.	[8]
	b)	Compare pipelining and parallel processing approaches.	[8]
4.		Explain the significance of the following terms (i) Spice Basics (ii) Spice power analysis	[16]
5.	a)	Explain the trends of technology and power supply voltage.	[8]
	b)	Discuss about low – voltage, low -power logic style.	[8]
6.	a)	Discuss the types of multiplier architectures.	[8]
	b)	Explain about Booth multiplier.	[8]
7.	a)	Compare SRAM and DRAM.	[4]
	b)	Give a note on future trend and development of ROM.	[8]
	c)	Write down differences between 6T and 4T static RAM cells.	[4]

Code No: **RT42044C** **R13** **Set No. 2**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2018

LOW POWER VLSI DESIGN

(Electronics and Communications Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1. a) Explain about impact ionization. [3]
   b) What are Mask Level measures? [3]
   c) Explain capacitive power estimation. [4]
   d) What are the standard adder cells? [4]
   e) Explain about the multiplication operation. [4]
   f) Draw a 6 transistor SRAM cell. [4]

PART–B *(3x16 = 48 Marks)*

2. a) What are the sources of power dissipation in digital IC? With usual notation derive the equation for short circuit power dissipation in a CMOS inverter, Discuss the technique to minimize this power dissipation. [8]
   b) Write the explanatory notes on physics of power dissipation in MOSFET devices. [8]

3. a) Explain the various problems encountered in cell based design at circuit level. [8]
   b) Explain about switch capacitance minimization approach. [8]

4. a) List the advantages and limitations of SPICE power analysis method. [8]
   b) Explain about static power and gate level capacitance estimation. [8]

5. a) Explain the basic theory, operation and performance evaluation of carry look-ahead adders. [8]
   b) Discuss about Carry select adder and its operations. [8]

6. Draw the basic building blocks of the Baugh-Wooley multiplier architecture and explain its operation. [16]

7. a) With a neat diagram, explain the block diagram of DRAM architecture. [8]
   b) Discuss low power SRAM technologies with neat diagrams. [8]

Code No: **RT42044C** **R13** **Set No. 3**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2018

LOW POWER VLSI DESIGN

(Electronics and Communications Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) Derive the expression for dynamic power dissipation in a CMOS inverter. [4]
   b) Explain about Circuit level measures. [4]
   c) Explain about gate level logic simulation [4]
   d) What are the types of CMOS adders? [3]
   e) What is Booth multiplier? [4]
   f) What is the self refresh circuit? [3]

PART–B *(3x16 = 48 Marks)*

2. a) What are Glitches? Explain how glitches affect the power dissipation. How can they be avoided? [8]
   b) Discuss gate level analysis to estimate power in a CMOS circuit. [8]

3. a) Explain about VTCMOS circuit. [8]
   b) Explain about architecture level approach of low power design. [8]

4. Explain about the modeling and analysis of transistor using SPICE. [16]

5. a) Draw the logic circuit of the conventional CMOS full adder and explain about it. [8]
   b) Explain the basic theory, operation and performance evaluation of standard cell adders. [8]

6. a) Write down the algorithm of Baugh-Wooley multiplier. [8]
   b) Explain about Wallace tree multiplier. [8]

7. With a neat diagram, explain the block diagram of SRAM architecture and its memory cells. [16]

Code No: **RT42044C** **R13** **Set No. 4**

IV B.Tech II Semester Regular/Supplementary Examinations, April - 2018

LOW POWER VLSI DESIGN

(Electronics and Communications Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
*****

PART–A *(22 Marks)*

1. a) Explain the technology and device innovations for novel high speed low power VLSI devices. [4]
   b) Explain about system level measures. [4]
   c) Explain about gate level capacitive estimations. [4]
   d) Explain the function of Ripple carry adder. [3]
   e) What is Wallace tree multiplier? [3]
   f) Explain pre-charge and Equalization Circuit. [4]

PART–B *(3x16 = 48 Marks)*

2. a) Explain the effect of V_{dd} and V_t on CMOS power analysis where V_{dd} is supply and V_t is threshold voltage. [8]
   b) With the help of neat diagrams, explain the impact of transistor sizing gate oxide thickness and technology scaling on low power electronics. [8]

3. a) Explain the basic theory, operation and performance evaluation of MTCMOS circuit. [10]
   b) Differentiate MTCMOS from DTCMOS. [6]

4. What are the SPICE circuit simulators available for circuit design? Among them what are free ware and what are the commercial software? Explain it. [16]

5. a) Write down the differences between carry select adders and carry save adders. [8]
   b) Discuss any two types of low voltage low power logic styles. [8]

6. a) Explain low voltage low power multiplier and its architecture. [8]
   b) Differentiate Braun multiplier and Baugh Wooley multiplier. [8]

7. a) How the power consumption can be reduced in SRAM to achieve performance. [8]
   b) Distinguish between SRAM and DRAM and its technologies. [8]