Code No: R1632044 **R16** SET - 1

III B. Tech II Semester Supplementary Examinations, November -2019

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

~~~~~~

PART –A (14 Marks)

1. a) What is BIBO stability? What are the conditions for BIBO stability? [2M]
   b) How FFT is more efficient to determine DFT of sequence? [2M]
   c) Why IIR filters do not have linear phase? [2M]
   d) What conditions are to be satisfied by the impulse response of an FIR system in order to have a linear phase? [3M]
   e) What is the significance of Multirate Signal processing? [3M]
   f) What are the advantages of VLIW architecture? [2M]

PART –B (56 Marks)

2. a) Determine the Inverse Z-Transform of: $X(Z)=1/(1-Z^{-1})(1-Z^{-1})^2$. [7M]
   b) Determine the stability for the following systems: [7M]
   i) $h(n) = 2^n u(n)$ ii) $h(n) = 5^n u(3-n)$ iii) $h(n) = e^{-6|n|}$.

3. a) Find the DFT of a sequence x(n)={1, 1, 0, 0} and find the IDFT of Y(k)={1, 0, 1, 0}. [7M]
   b) Establish the relation between DFT and Z-transform. [7M]

4. a) Determine direct form I and cascade realization of the following system: [7M]
   $$H[z]=\frac{2\left(1-z^{-1}\right)\left(1+\sqrt{2}z^{-1}+z^{-2}\right)}{\left(1+0.5z^{-1}\right)\left(1-0.9z^{-1}+0.81z^{-2}\right)}$$
   b) Design a Chebyshev filter with a maximum pass band attenuation of 2.5 dB at a frequency of 20 rad/sec and the stop band attenuation of 30 dB at a frequency 50 rad/sec. [7M]

5. a) List out the characteristics of FIR digital filters. [7M]
   b) Explain the need for the use of window sequence in the design of FIR filter. Describe the window sequence generally used and compare the properties. [7M]

6. a) Explain the decimation and interpolation processes with an example. [7M]
   b) Explain any two applications of Multirate digital signal processing. [7M]

7. a) Explain the following in detail: [7M]
   i) Index Register ii) On-chip memory.
   b) With neat block diagram, explain about the pipelining. [7M]

*****
~~~~~~