

II B. Tech I Semester Supplementary Examinations, May - 2019
DIGITAL LOGIC DESIGN
 (Com to CSE & IT)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answer **ALL** the question in **Part-A**
 3. Answer any **FOUR** Questions from **Part-B**

PART -A

1. a) Convert the following (i) $(AB)_{16} = (\quad)_{10}$ (ii) $(1234)_8 = (\quad)_{10}$ (3M)
- b) Find the 2's complement and 1's complement of 101101 (2M)
- c) Convert the following expression SOP into POS $(AB + C)(B + C^1D)$. (3M)
- d) What are the Universal gates? Why they called as universal gates. (2M)
- e) Define Toggle condition. (2M)
- f) Classify the register with respect to serial and parallel input-output. (2M)

PART -B

2. a) The binary numbers listed have a sign bit in the leftmost position and if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. (7M)
 (i) $101011 + 111000$ (ii) $001110 + 110010$ (iii) $111001 - 001010$
 (iv) $101011 - 100110$
- b) Convert the following to Decimal and then to octal. (7M)
 (i) $(125F)_{16}$ (ii) $(10111111)_2$ (iii) $(4234)_{10}$
3. a) Find the complement and duality of given function below and then reduce minimum number of literals in each case $F = [(\overline{ab}).a][(\overline{ab}).b]$ (7M)
- b) Simplify the following to minimum number of literals. (7M)
 (i) $\overline{A}B(\overline{D} + \overline{C}D) + B(A + \overline{A}CD)$ (ii) $\overline{x}\overline{y} + xy + \overline{x}y$
4. a) Design a full adder by using two half adders. (7M)
- b) Explain about decoder circuit and implement the 4×16 decoder by using two 3×8 decoders. (7M)
5. a) What is a flip-flop? Design the basic flip-flop using NOR gates and explain. (7M)
- b) What is an excitation table? Write the excitation tables for JK and T flip-flops. (7M)
6. a) Write the differences between synchronous and Asynchronous Counters. (7M)
- b) Explain the operation of the 4-bit asynchronous counter. (7M)
7. a) Write the difference between mealy and moore machines. (6M)
- b) Convert the given mealy machine to moore machine by using translation diagram. (8M)

State	Input		Out put
	a	b	
A	B	A	0
B	B	C	0
C	B	D	0
D	B	A	1