Code No: R1632043 **R16** SET - 1

III B. Tech II Semester Supplementary Examinations, November - 2019

VLSI DESIGN

(**Common to** Electronics and Communication Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A (14 Marks)

1. a) Why is VLSI design process presented in NMOS only? Justify with an example. [2M]
   b) Give the different scaling models and scaling factors. [2M]
   c) Explain about Inverter Delays. [2M]
   d) Explain about chip output circuit. [3M]
   e) What information from the targeted FPGA device is required in RTL synthesis? [3M]
   f) Explain about Clock Design. [2M]

PART –B (56 Marks)

2. a) Derive an equation for I_{ds} of an n-channel Enhancement MOSFET operating in Saturation region. [7M]
   b) An nMOS transistor is operating in saturation region with the following parameters. V_{GS} = 5V; V_{tn} = 1.2V; W/L = 110; $\mu_n C_{ox}$ = 110 $\mu A/V^2$. Find transconductance of the device. [7M]

3. a) Explain about double poly CMOS rules. [7M]
   b) Design a layout diagram for CMOS 3-input NAND gate. [7M]

4. a) What is meant by sheet resistance R_s? Explain the concept of R_s applied to MOS transistors. [7M]
   b) Calculate on resistance of an inverter from VDD to GND. If n- channel sheet resistance R_{sn}=104 Ω per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4$ Ω per square. (Z_{pu}=4:4 and Z_{pd}=2:2). [7M]

5. Discuss in detail about Fault types and Models. [14M]

6. a) Write down the step by step approach of FPGA design process on XILINX environment. [7M]
   b) Design a queue and write the dataflow style VHDL program for the same. [7M]

7. Discuss in detail about Low Power CMOS Logic Circuits. [14M]

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