Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, October/November - 2018

DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS

(Common to Electronics Computer Engineering and Electronics Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Explain about data objects in VHDL.	[3M]
	b)	Discuss about Technology Libraries.	[4M]
	c)	Explain briefly Static RAM Internal structure.	[4M]
	d)	Explain about CMOS steady state electrical behavior.	[4M]
	e)	Explain the significance of Dual Priority encoder.	[4M]
	f)	Compare latches and flip flops.	[3M]

PART -B

2	a)	Explain the Packages and Libraries of VHDL?	[8M]
	b)	Compare and contrast between VHDL and Verilog HDL.	[8M]
3	a)	Explain why place and route tools are used in VHDL with the help of data flow diagram.	[8M]
	b)	Explain in detail about Post Layout Timing Simulation.	[8M]
4	a)	Explain the internal structure of PROM and list its advantages.	[8M]
	b)	Describe DRAM with an appropriate diagram and explain about its timings.	[8M]
5	a)	Explain dynamic electrical behavior of a CMOS.	[8M]
	b)	What are the salient features of ECL? and explain its internal structure	[8M]
6	a)	Write the VHDL code for 16 bit barrel shifter.	[8M]
	b)	Design a 4 bit carry look ahead adder using gates and write the VHDL code for it.	[8M]
7	a)	Write a VHDL program to design a modulo-8 counter.	[8M]
	b)	Explain in detail about the working of Johnson Counter using 74 LS194.	[8M]

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