Code No: R1622023 **R16** SET - 1

II B. Tech II Semester Supplementary Examinations, November - 2019
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

~~~~~~

PART –A

1. a) Design OR gate using NAND gate. (2M)
   b) Write the statement for De-morgan's Law? (2M)
   c) Compare decode with a demultiplex. (3M)
   d) What are the basic blocks of a PLA? (3M)
   e) List out the application of Register? (2M)
   f) What is Moore model? (2M)

PART -B

2. a) Perform the following using 6's complement: (8M)
      i. $(126)_7 + (42)_7$
      ii. $(126)_7 - (42)_7$
   b) Explain about weighted codes. (6M)

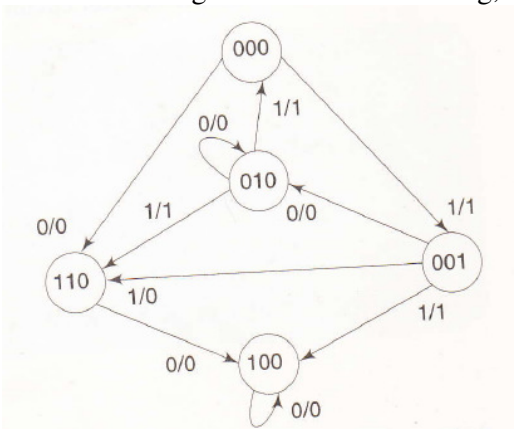
3. a) Simplify the given function using tabular method. (7M)
      F (A, B, C, D) = Σ (0, 2, 3, 6, 7, 8, 10, 12, 13)
   b) Minimize below expression using EX-OR function (7M)
      $$f = \bar{A}B\bar{C} + \bar{A}\bar{B}C + A\bar{C}D + AC\bar{D}$$

4. a) Design Full adders from half adder and write the applications of full adder. (7M)
   b) Define Multiplexer and explain the procedure to implement 32 X 1 MUX by Using 4 X 1 Multiplexers. (7M)

5. Design an Excess-3 to BCD code converter using a (a) PROM (b) PAL. (7+7M)

6. a) With the aid of external logic, convert D type flip-flop to a J-K flip-flop. (7M)
   b) Explain different types of shift registers. (7M)
~~~~~~

7. a) For the state diagram shown in below fig, design using T Flip-flop. (7M)



b) Design a serial adder to add two binary numbers. (7M)