Code No: R1622054 **R16** SET - 1

II B. Tech II Semester Supplementary Examinations, November - 2019
COMPUTER ORGANIZATION
(Com to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

~~~~~~

PART –A

1. a) Explain different types of data representation? (2M)
   b) Differentiate multi computers and multi processors. (2M)
   c) Explain with example the implementation of register transfer? (2M)
   d) List out addressing modes. (2M)
   e) What are memory reference instructions? (2M)
   f) Explain about memory interleaving. (4M)

PART -B

2. a) What are the differences between CISC and RISC processors?-Compare. (7M)
   b) Represent the number $(+46.5)_{10}$ as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and exponent has 8 bits. (7M)

3. a) With the help of the example, explain in detail various types of memory reference instructions. (7M)
   b) Explain 4-bit binary incremented with a circuit diagram to increment 0110. (7M)

4. a) Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating (3+4) [10(2+6) +8]. (7M)
   b) Illustrate different classes of interrupts. (7M)

5. a) Define addressing mode. Explain different types of Addressing modes. (7M)
   b) A two word instruction is stored in memory at an address designated by the symbol 'W'. The address field of the instruction (stored at W+1) is designated by the symbol 'Y'. The operand used during the execution of the instruction stored at an address symbolized by 'Z'. An index register contains the value 'X'. State how 'Z' is calculated from the other addresses if the addressing mode of the instruction is 1.Direct 2.Indirect 3.Relative 4.Indexed (7M)

6. a) Define Virtual Memory. Explain the process of converting virtual addresses to physical addresses with a neat diagram. (7M)
   b) Differentiate the following (i) Pipeline conflict (ii) Network interlock (7M)

7. a) How the logical address is translated into physical address in paging?-Give details. (7M)
   b) Explain about asynchronous data transfer and asynchronous communication interface. (7M)
~~~~~~