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Fully-vertical GaN-on-Si power MOSFETs

Riyaz Abdul Khadar, Chao Liu, Reza Soleimanzadeh and Elison Matioli, *Member, IEEE*

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***Abstract*— We report the first demonstration of fully-vertical power MOSFETs on 6.6-µm-thick GaN grown on a 6-inch Si substrate by metal-organic chemical vapor deposition (MOCVD). A robust fabrication method was developed based on a selective and local removal of the Si substrate as well as the resistive GaN buffer layers, followed by a conformal deposition of a 35-µm-thick copper layer on the backside by electroplating, which provides excellent mechanical stability and electrical contact to the drain terminal. The fabrication process of the gate trench was optimized, improving considerably the effective mobility at the p-GaN channel and the output current of the devices. High performance fully-vertical GaN-on-Si MOSFETs are presented, with low specific on-resistance ($R_{on,sp}$) of 5 mΩcm^2 and high off-state breakdown voltage (BV) of 520 V. Our results reveal a major step towards the realization of high performance GaN vertical power devices on cost-effective Si substrates.**

***Index Terms* – GaN, vertical, power devices, GaN-on-Si, high breakdown, fully-vertical, MOSFETs, low $R_{on,sp}$.**

I. Introduction

GaN-based devices are excellent candidates for power electronics due to their superior material properties, such as large critical electric field, high electron mobility and saturation velocity, and capability of high temperature operation. High performance lateral GaN power devices with large breakdown voltage and low on-resistance have been demonstrated [1]–[4]. The main drawback of lateral devices is that the breakdown voltage (BV) scales proportionally with the gate-to-drain spacing and thus requiring large device area for high voltage operation. Nevertheless, beyond a specific gate-to-drain separation, the BV is dictated by the thickness and quality of the buffer layers which increases the overall complexity and cost of epitaxial growth for high voltage devices. Lateral devices are also severely affected by trap states and high electric fields present at the surface, which lead to current collapse and other reliability problems [5], [6].

These issues do not plague GaN vertical devices as the electric field peaks far away from the surface, and the breakdown voltage depends on the thickness of the drift layer, independently of the device area [7]. Vertical p-i-n diodes and transistors on bulk GaN substrates have already been reported with nearly ideal ON- and OFF-state performances, which was possible due to the low defect density and the ability to homo-epitaxially grow thick layers on these substrates [8]–[19]. Yet, bulk GaN substrates are still prohibitively expensive and only available in small diameters. The recent progress on the hetero-epitaxial growth of thick GaN layers on large area Si substrates [20]–[22] offers a cost-effective platform to develop vertical GaN-on-Si power devices, taking advantage of the low cost, large scale, and mature fabrication technology of Si substrates.

The authors are with the Power and Wide-band-gap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, CH-1015 Lausanne, Switzerland (e-mail: riyazmohammed.abdul@epfl.ch; elison.matioli@epfl.ch).

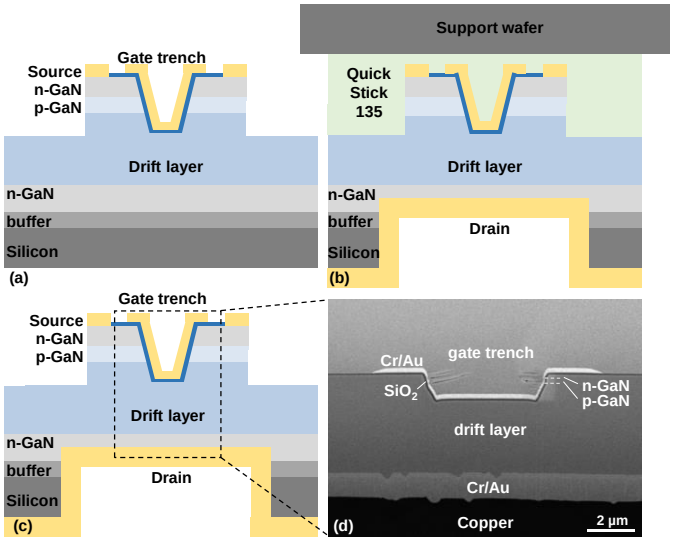

Fig. 1. Fabrication process of fully-vertical GaN-on-Si MOSFETs. (a) Schematic of the device structure after definition of source and gate pads. (b) The drain contact is defined at the backside via a support wafer attached to the device using QuickStick 135. (c) Schematic of the completed device after removing the support wafer. (d) Cross-sectional SEM image of the fabricated fully-vertical GaN-on-Si MOSFET.

Recently, high-voltage GaN-on-Si quasi-vertical transistors [23], [24] and high-performance quasi- and fully-vertical p-i-n diodes [20], [21] have been demonstrated, but their performance (quasi-vertical) is severely limited by current crowding in the bottom n-GaN layer [25], which significantly increases the $R_{on,sp,}$ especially in large area devices. While the $R_{on,sp}$ can be improved by increasing the doping and thickness of the bottom n-GaN layer, this restricts the remainder thickness of the drift layer which can be grown without wafer cracking, thus limiting the effective BV. In addition, quasi-vertical designs require a larger device area since all pads occupy the top surface of the wafer.

These challenges can be addressed by a fully-vertical design, since it is not affected by current crowding due to the vertical nature of the current flow, offering therefore a much larger current capability and significantly smaller $R_{on,sp}$. In addition, a fully-vertical design would provide a larger number of devices per unit area of the wafer compared to quasi-vertical designs, since the drain contact is made at the bottom of the wafer.

In this work, we demonstrate the first fully-vertical GaN-on-Si power MOSFET based on a robust fabrication process to selectively remove the Si substrate and resistive buffer layers under the devices, followed by a conformal deposition of a 35-µm-thick copper layer on the backside by electroplating, which provided excellent mechanical stability and electrical contact to the bottom n-GaN layer. The devices

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were fabricated on a 6.6 µm-thick n-p-i-n GaN epitaxial structure grown on 6-inch Si substrate. The fabrication process of the gate trenches, including alignment, etching mask and surface treatment was optimized to increase the channel field effect mobility and device output current. Fully-vertical GaN-on-Si power MOSFETs are demonstrated presenting large forward current density up to 1.6 kA/cm^2 and small $R_{on,sp,}$ down to 5 mΩcm^2, along with high *BV* of 520 V. These results open a promising pathway for the development of GaN-on-Silicon vertical devices for future power applications.

II. Device Structure and Fabrication

The n-p-i-n epitaxial structure consisted, from bottom to top, of 1.07 µm-thick buffer, 1 µm-thick n-GaN ([Si] ~ 1 × 10^{19}cm^{-3}), 4 µm-thick i-GaN ([Si] ~ 2 × 10^{16} cm^{-3}), 350 nm-thick p-GaN ([Mg] ~ 2 × 10^{19} cm^{-3}), a 180 nm-thick n-GaN layer ([Si] ~ 5 × 10^{18} cm^{-3}), and 20 nm-thick n$^+$-GaN ([Si] ~ 1 × 10^{19} cm^{-3}). All the GaN layers were grown by MOCVD on a 6-inch Si (111) substrate. The full width at half maximum (FWHM) of the X-ray omega rocking curves for (002) and (102) orientations were 237 and 330 arcsec.

The fabrication process started with a 1.27 µm deep dry-etching of the gate trench using two different types of hard masks - metal (Ni) and oxide (SiO_2) – fabricated on separate chips for comparison. A subsequent treatment by 25% Tetra

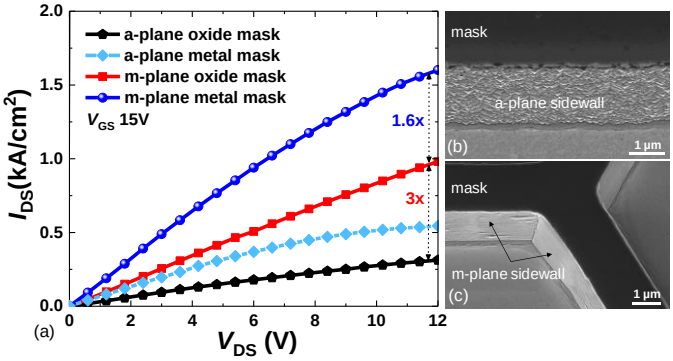

Fig. 2. (a) Comparison of the I_{DS}-V_{DS} of the fabricated vertical MOSFETs with gate trench aligned along m- and a-plane, using metal and oxide hard masks. SEM images of the trench sidewall aligned along the (b) a-plane and (c) m-plane, after TMAH wet treatment. Notice the much smoother m-plane sidewalls compared to the a-plane.

Methyl Ammonium Hydroxide (TMAH) was performed at 85°C for 1 hour to smoothen the etched surface and remove dry-etching damages at the gate trench sidewalls [26], [27]. A rapid thermal anneal (RTA) was then carried out at 750°C for 20 min in N_2 ambient to activate the buried p-GaN layer through the sidewalls. The devices were isolated by 1.35 µm-deep Cl_2-based mesa etch, followed by 100 nm-thick SiO_2 gate oxide deposited by atomic layer deposition (ALD) at 300°C using Bis(tertiary-butylamino)silane and ozone as precursors. The thick oxide layer protects the gate terminal against the high electric field regions at the bottom of the gate trench during reverse bias operation. After opening the source contact by dry etching of SiO_2, Cr/Au (50/250 nm) were deposited as gate and source contacts. For the remainder of the fully-vertical device fabrication, the Si substrate was first thinned by grinding from 1000 µm to 500 µm (Fig. 1(a)). The chip was then attached to a Si support wafer by a temporary mounting wax (QuickStick 135) for the backside processing.

After patterning the regions of the backside under each device, the Si substrate was completely dry-etched by bosch deep-reactive-ion-etch process, followed by a Cl_2-based dry-etching of the resistive GaN buffer. Cr/Au (50/250nm) metal stack was deposited as ohmic contact for the drain by e-beam evaporation, followed by a 35-µm-thick electroplated Cu layer, which offered excellent mechanical stability to the thin GaN membrane (Fig. 1(b)). The chips were then released from the Si support wafer by immersion in hot acetone to dissolve the QuickStick 135 mounting wax (Fig. 1(c)). Fig. 1(d) shows the cross-sectional SEM image of the fabricated device.

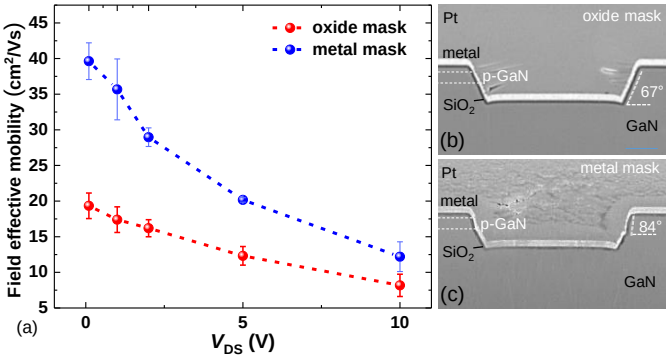

Fig. 3. (a) Field effect mobility extracted from devices with metal mask and oxide mask etched gate trench (b) Cross-sectional SEM of oxide mask etched gate trench presenting slanted side walls (67°) and (c) metal mask etched gate trench showing near-vertical (84°) sidewalls at the channel (p-GaN) region.

III. Results And Discussion

To optimize the device performance, we investigated the effect of orientation and etch mask used to define the gate trench, on the electrical characteristics of the devices. Gate trenches were aligned along the m- and a-planes of GaN followed by a TMAH surface treatment. The width and length of the gate trench were 32 µm and 6 µm respectively. The Cl_2-based dry-etching process was performed using metal and oxide hard masks. As shown in Fig. 2(a), vertical MOSFETs with gate trench aligned along the m-plane presented 3x-higher drain current and 3x-lower $R_{on,sp}$ as compared to those aligned along the a-plane. Such a significant enhancement is due to the

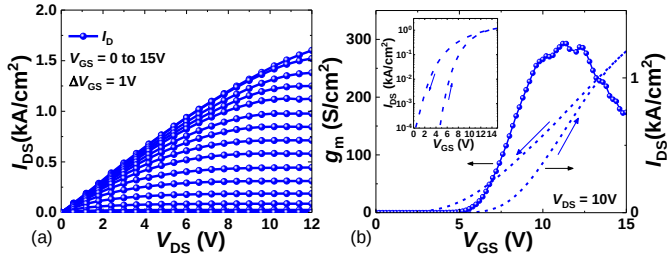

Fig. 4. (a) I_{DS}-V_{DS} characteristics of metal mask vertical MOSFET for V_{GS} varying from 15 V to 0 V in steps of 1 V. (b) Transfer and transconductance (g_m) characteristics. Inset figure shows the transfer curve in semi-log scale.

much smoother m-plane sidewall after TMAH treatment compared to the a-plane, as evident from Fig. 2(b) and (c), which resulted in a much improved electron mobility in the MOSFET channel (similar observation was reported in [28]). An additional 1.6x-fold improvement in output current was achieved by utilizing a metal (Ni) hard mask to etch the gate trenches, instead of SiO_2 hard mask.

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Fig. 3(a) shows the extracted field-effect mobility from the transconductance of vertical MOSFETs fabricated with metal and oxide hard masks, at V_{DS} of 0.1, 1, 2, 5 and 10 V using the relation $g_m = (Z/L)\times\mu\times C_o\times V_{DS}$ with an average g_m obtained from double-sweep measurement [29]. A much higher field average effective mobility was observed for the device processed with metal hard mask of 41 cm^2/Vs as compared to 21 cm^2/Vs for the oxide mask. To the best of our knowledge, this is the highest mobility reported on GaN trench gate MOSFETs grown on foreign substrates.

This is possibly due to fact that the angled trench sidewall (67°) created by the oxide mask is oriented mostly at a semi-polar GaN plane [30], [31] very close to the $10\bar{1}1$ plane [32], which is not charge neutral, leading to more scattering and reduced electron mobility in the inversion channel. On the other hand, the metal mask offers a near-vertical (84°) and smooth sidewall for the p-GaN channel [27]. However, further studies are needed to accurately understand this improvement in mobility. Fig. 4 (a) shows the output characteristics of the fabricated vertical MOSFETs with metal mask, revealing a very high current density of 1.6 kA/cm^2 and a $R_{on,sp}$ of 5 mΩcm^2. These values were normalized by the device active area, defined by the gate trench area of 10 µm × 36 µm [23], [33], after accounting for a lateral current spreading of 2 µm from all the sides of the gate trench (which was confirmed by TCAD simulations). These devices exhibited 2.8x-better current density and 3x-lower $R_{on,sp}$ as compared to quasi-vertical MOSFETs on a similar GaN epitaxial structure on Si substrate described in [23]. This improvement in electrical performance is mainly due to the fully-vertical design of the device [34] and the improved mobility in the p-GaN inversion channel. The p-GaN inversion channel is the major limiting factor to the $R_{on,sp}$, as the resistance of the i-GaN layer was 0.33 mΩcm^2 and of the bottom n-GaN layer was 6.2 × 10^{-4} mΩcm^2. The lateral spreading resistance from the source contact to the p-GaN inversion channel was 2.62 × 10^{-7} mΩcm^2 and the source and drain contact resistances were 5 × 10^{-5} mΩcm^2. These values are much smaller than the measured 5 mΩcm^2, indicating that the $R_{on,sp}$ is mainly determined by the resistance of the p-GaN inversion layer.

Fig. 4(b) shows the the I_{DS} - V_{GS} and the g_m - V_{GS} characteristics of the metal mask device. The device presented a V_{th} of 7.9 V (from extrapolation in linear scale) along with a 125%-higher g_m, up to 300 S/cm^2 as compared to the quasi-vertical device [23]. The V_{th}, defined at I_{DS} of 20 A/cm^2, was 6.4 V. Such a relatively small V_{th} value is mainly due to donor-type N-vacancies present in the trench sidewall as a result of defects from the dry-etching process [13], [17], [18]. The negative hysteresis of ~ 2 V (at a current density of 0.2 kA/cm^2) observed in the I_{DS}-V_{GS} curves is likely due to bulk oxide traps [35], which can be addressed with a better quality gate oxide deposition and post-deposition annealing.

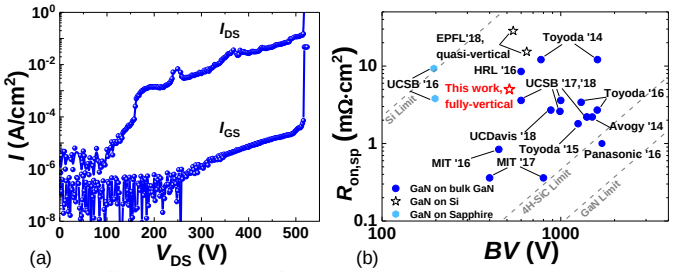

Fig. 5. (a) Off-state blocking performance of the metal mask vertical MOSFET measured at a V_{GS} of 0 V. (b) $R_{on,sp}$ vs BV benchmarking of the metal mask device against other reported GaN vertical transistors on bulk GaN and Si substrates.

The GaN-on-Si vertical MOSFETs exhibited an excellent off-state behavior, with BV of 520 V, which was achieved without deploying any particular field plate or edge termination techniques (Fig. 5(a)), along with a small drain to source leakage current (I_{DS}) lower than 10^{-1} A/cm^2 (normalized by the mesa area of 110 µm × 197 µm as in [11], [12], [23]). The nearly-linear dependence in log-scale of the drain-to-source leakage current (I_{DS}) with applied electric field at high bias is an indication of variable range hopping mechanism [26]. The gate leakage current remained below 10^{-4} A/cm^2 until the breakdown happened at the gate edge. Fig. 5(b) presents the benchmarking of our fully-vertical GaN-on-Si MOSFETs against other GaN vertical transistors demonstrated on bulk GaN and Si substrates [12-21], [24], [25], [36], [37]. Compared to other GaN-on-Si transistors, our device presented a much lower $R_{on,sp}$ of 5 mΩcm^2 and BV similar to previous reports on GaN-on-Si MOSFETs [23], [24] with a similar epitaxial structure and without field plates. The gate-edge breakdown can be improved with a smoother and rounded corner at the sidewall base [27], and by improving the quality of the gate oxide [37]. Further enhancement in breakdown voltage is envisaged by employing properly designed field plates at the source and gate contacts together with thick passivation layers, as demonstrated in bulk GaN MOSFETs [12], [15], [17].

IV. Conclusions

Fully-vertical GaN-on-Si MOSFETs were demonstrated for the first time using a robust fabrication method to locally remove the Si substrate, relying on a conformally electroplated thick Cu layer, which provides excellent electrical contact and mechanical stability. The device exhibited low $R_{on,sp}$ of 5 mΩcm^2, high current density greater than 1.6 kA/cm^2, excellent transconductance of 300 S/cm^2, and high BV of 520 V despite the absence of field plates. These results offer an important step towards the future adoption of vertical GaN-on-Si for cost-effective high-voltage and high-current applications.

V. Acknowledgement

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VI. References

[1] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 367–370, Mar. 2017, doi: 10.1109/LED.2017.2661755.

[2] J. Ma and E. Matioli, "Slanted Tri-gates for High-Voltage GaN Power Devices," *IEEE Electron Device Lett.*, vol. PP, no. 99, pp. 1–1, 2017, doi: 10.1109/LED.2017.2731799.

[3] O. S. Koksaldi, J. Haller, H. Li, B. Romanczyk, M. Guidry, S. Wienecke, S. Keller, and U. K. Mishra, "N-Polar GaN HEMTs Exhibiting Record Breakdown Voltage Over 2000 V and Low Dynamic On-Resistance," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1014–1017, Jul. 2018, doi: 10.1109/LED.2018.2834939.

[4] M. Wang, Y. Wang, C. Zhang, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, K. J. Chen, and B. Shen, "900 V/1.6 mΩ.cm^2 Normally Off Al_2O_3/GaN MOSFET on Silicon Substrate," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2035–2040, Jun. 2014, doi: 10.1109/TED.2014.2315994.

[5] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2015–2020, Oct. 2003, doi: 10.1109/TED.2003.816549.

[6] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives," *IEEE Trans. Device Mater. Reliab.*, vol. 8, no. 2, pp. 332–343, Jun. 2008, doi: 10.1109/TDMR.2008.923743.

[7] B. J. Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1717–1731, Oct. 1996, doi: 10.1109/16.536818.

[8] Z. Hu, K. Nomoto, B. Song, M. Zhu, M. Qi, M. Pan, X. Gao, V. Protasenko, D. Jena, and H. G. Xing, "Near unity ideality factor and Shockley-Read-Hall lifetime in GaN-on-GaN p-n diodes with avalanche breakdown," *Appl. Phys. Lett.*, vol. 107, no. 24, p. 243501, Dec. 2015, doi: 10.1063/1.4937436.

[9] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV Vertical GaN PN Diodes," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 247–249, Feb. 2014, doi: 10.1109/LED.2013.2294175.

[10] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, "1200 V GaN vertical fin power field-effect transistors," in *2017 IEEE Int. Electron Devices Meet. IEDM*, San Francisco, CA, USA, Dec. 2017, pp. 9.2.1-9.2.4, doi: 10.1109/IEDM.2017.8268357.

[11] C. Gupta, C. Lund, S. H. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, and U. K. Mishra, "In SituOxide,GaN Interlayer-Based Vertical Trench MOSFET(OG-FET) on Bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 353–355, Mar. 2017, doi: 10.1109/LED.2017.2649599.

[12] C. Gupta, S. H. Chan, Y. Enatsu, A. Agarwal, S. Keller, and U. K. Mishra, "OG-FET: An In-Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1601–1604, Dec. 2016, doi: 10.1109/LED.2016.2616508.

[13] C. Gupta, A. Agarwal, S. H. Chan, O. S. Koksaldi, S. Keller, and U. K. Mishra, "1 kV field plated in-situ oxide, GaN interlayer based vertical trench MOSFET (OG-FET)," in *2017 75th Annu. Device Res. Conf. DRC*, Jun. 2017, pp. 1–2, doi: 10.1109/DRC.2017.7999410.

[14] M. Sun, Y. Zhang, X. Gao, and T. Palacios, "High-Performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 509–512, Apr. 2017, doi: 10.1109/LED.2017.2670925.

[15] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Appl. Phys. Express*, vol. 7, no. 2, p. 021002, Jan. 2014, doi: 10.7567/APEX.7.021002.

[16] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8 mΩ·cm^2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Appl. Phys. Express*, vol. 8, no. 5, p. 054101, May 2015, doi: 10.7567/APEX.8.054101.

[17] R. Li, Y. Cao, M. Chen, and R. Chu, "600 V/ 1.7 Ω Normally-Off GaN Vertical Trench Metal-Oxide-Semiconductor Field-Effect Transistor," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1466–1469, Nov. 2016, doi: 10.1109/LED.2016.2614515.

[18] H. Nie, Q. Diduck, B. Alvarez, A. P. Edwards, B. M. Kayes, M. Zhang, G. Ye, T. Prunty, D. Bour, and I. C. Kizilyalli, "1.5-kV and 2.2-mΩ-cm^2 Vertical GaN Transistors on Bulk-GaN Substrates," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 939–941, Sep. 2014, doi: 10.1109/LED.2014.2339197.

[19] D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda, "1.7 kV/1.0 mΩcm^2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *2016 IEEE Int. Electron Devices Meet. IEDM*, Dec. 2016, pp. 10.1.1-10.1.4, doi: 10.1109/IEDM.2016.7838385.

[20] R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si Quasi-Vertical p-i-n Diodes With BFOM of 2.0 GW/cm^2," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.

[21] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, "720-V/0.35-mΩ.cm^2 Fully Vertical GaN-on-Si Power Diodes by Selective Removal of Si Substrates and Buffer Layers," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 715–718, May 2018, doi: 10.1109/LED.2018.2819642.

[22] A. Tanaka, W. Choi, R. Chen, and S. A. Dayeh, "Si Complies with GaN to Overcome Thermal Mismatches for the Heteroepitaxy of Thick GaN on Si," *Adv. Mater.*, vol. 29, no. 38, p. 1702557, Oct. 2017, doi: 10.1002/adma.201702557.

[23] C. Liu, R. A. Khadar, and E. Matioli, "GaN-on-Si Quasi-Vertical Power MOSFETs," *IEEE Electron Device Lett.*, vol. PP, no. 99, pp. 1–1, 2017, doi: 10.1109/LED.2017.2779445.

[24] C. Liu, R. A. Khadar, and E. Matioli, "Vertical GaN-on-Si MOSFETs With Monolithically Integrated Freewheeling Schottky Barrier Diodes," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1034–1037, Jul. 2018, doi: 10.1109/LED.2018.2841959.

[25] X. Zhang, X. Zou, X. Lu, C. W. Tang, and K. M. Lau, "Fully- and Quasi-Vertical GaN-on-Si p-i-n Diodes: High Performance and Comprehensive Comparison," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 809–815, Mar. 2017, doi: 10.1109/TED.2017.2647990.

[26] Y. Zhang, M. Sun, H. Y. Wong, Y. Lin, P. Srivastava, C. Hatem, M. Azize, D. Piedra, L. Yu, T. Sumitomo, N. A. de Braga, R. V. Mickevicius, and T. Palacios, "Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015, doi: 10.1109/TED.2015.2426711.

[27] Y. Zhang, M. Sun, Z. Liu, D. Piedra, J. Hu, X. Gao, and T. Palacios, "Trench formation and corner rounding in vertical GaN power devices," *Appl. Phys. Lett.*, vol. 110, no. 19, p. 193506, May 2017, doi: 10.1063/1.4983558.

[28] C. Gupta, S. H. Chan, C. Lund, A. Agarwal, O. S. Koksaldi, J. Liu, Y. Enatsu, S. Keller, and U. K. Mishra, "Comparing electrical performance of GaN trench-gate MOSFETs with a-plane and m-plane sidewall channels," *Appl. Phys. Express*, vol. 9, no. 12, p. 121001, Nov. 2016, doi: 10.7567/APEX.9.121001.

[29] H. Otake, S. Egami, H. Ohta, Y. Nanishi, and H. Takasu, "GaN-Based Trench Gate Metal Oxide Semiconductor Field Effect Transistors with Over 100 cm^2/(V s) Channel Mobility," *Jpn. J. Appl. Phys.*, vol. 46, no. 7L, p. L599, Jun. 2007, doi: 10.1143/JJAP.46.L599.

[30] V. N. Bessolov, E. V. Konenkova, S. A. Kukushkin, A. V. Osipov, and S. N. Rodin, "SEMIPOLAR GALLIUM NITRIDE ON SILICON: TECHNOLOGY AND PROPERTIES," p. 19.

[31] M. T. Hardy, D. F. Feezell, S. P. DenBaars, and S. Nakamura, "Group III-nitride lasers: a materials perspective," *Mater. Today*, vol. 14, no. 9, pp. 408–415, Sep. 2011, doi: 10.1016/S1369-7021(11)70185-7.

[32] M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, "GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistor Fabricated with Novel Wet Etching," *Appl. Phys. Express*, vol. 1, p. 021104, Feb. 2008, doi: 10.1143/APEX.1.021104.

[33] W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, and H. G. Xing, "600 V GaN vertical V-trench MOSFET with MBE regrown channel," in *2017 75th Annu. Device Res. Conf. DRC*, Jun. 2017, pp. 1–2, doi: 10.1109/DRC.2017.7999414.

[34] Y. Zhang, M. Sun, D. Piedra, J. Hennig, A. Dadgar, and T. Palacios, "Reduction of on-resistance and current crowding in quasi-vertical GaN power diodes," *Appl. Phys. Lett.*, vol. 111, no. 16, p. 163506, Oct. 2017, doi: 10.1063/1.4989599.

[35] M. Ťapajna, M. Jurkovič, L. Válik, Š. Haščík, D. Gregušová, F. Brunner, E.-M. Cho, and J. Kuzmík, "Bulk and interface trapping in the gate dielectric of GaN based metal-oxide-semiconductor high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 102, no. 24, p. 243509, Jun. 2013, doi: 10.1063/1.4811754.

[36] D. Ji, C. Gupta, S. H. Chan, A. Agarwal, W. Li, S. Keller, U. K. Mishra, and S. Chowdhury, "Demonstrating gt;1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices," in *2017 IEEE Int. Electron Devices Meet. IEDM*, Dec. 2017, pp. 9.4.1-9.4.4, doi: 10.1109/IEDM.2017.8268359.

[37] D. Ji, A. Agarwal, H. Li, W. Li, S. Keller, and S. Chowdhury, "880 V/2.7 mΩ.cm^2 MIS Gate Trench CAVET on Bulk GaN Substrates," *IEEE Electron Device Lett.*, vol. 39, no. 6, pp. 863–865, Jun. 2018, doi: 10.1109/LED.2018.2828844.