# Optimised Vedic Multiplier for Multiplication of 8bit Binary Numbers

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## Introduction

FPGA based technology, allows easy reconfigurability, less development time with respect to full custom VLSI design. Areas such as Image processing, digital signal processing (DSP), Coding, Graphics, Robotics and different control algorithms like adaptive control, model predictive control (MPC), use multipliacation operations extensively.So our aim was to build a multiplier that has minimal delay and very low power consumption.Our aim was to build an optimised version of the already known Vedic Multiplier.

## Logic Of Simple Vedic Multiplier

Let us consider two numbers a= a0 a1 and b= a0 b1 as shown in line diagram. First the final product is obtained by taking the productof 2 LSB's i.e. a0 and b0 ,in second step the product of the LSB of x with the higher bit of y is taken in crosswise manner, the output carry generated is added to the result of the next step. Next step is to take product of 2 MSB's.

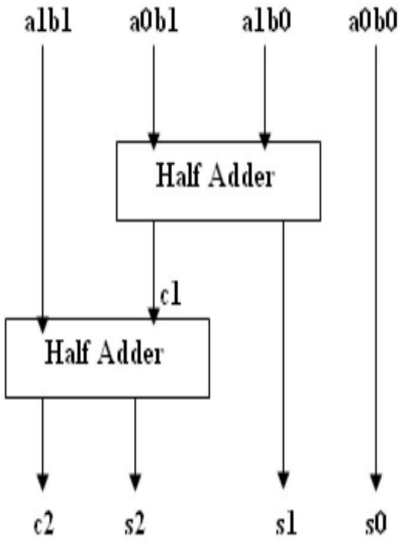
S 0 = a0 b0 . . . . . (1)

C 1 S 1 = a1 b0 +a0 b1 .....(2)

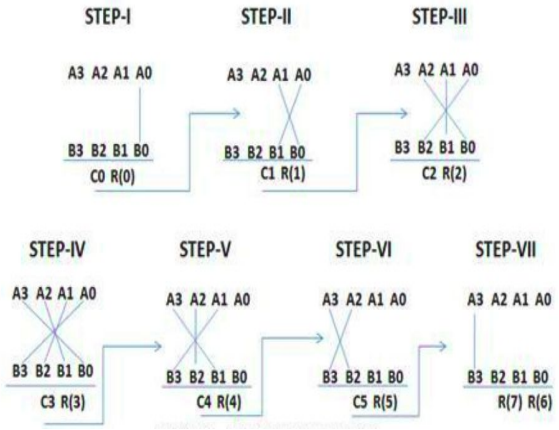
C 2 S 2 = C 1 +a1 b1 ..... (3)

The final result obtained is C 2 S 2 C 1 S 1 S 0. The 2x2 Vedic multiplier consists of four AND gate and two half adder. The advantage of this multiplier is that as the bit increases the area and delay increases very slowly, hence it is faster when compared with other multipliers. Hence total delay is the sum of delay of 2 half adders after partial product generation.The 4x4 and 8x8 Vedics operate similarly by recursively using

the 2x2 Vedic.Their working is shown in the following block diagrams.




A 4-bit Vedic Multiplication is explained below.

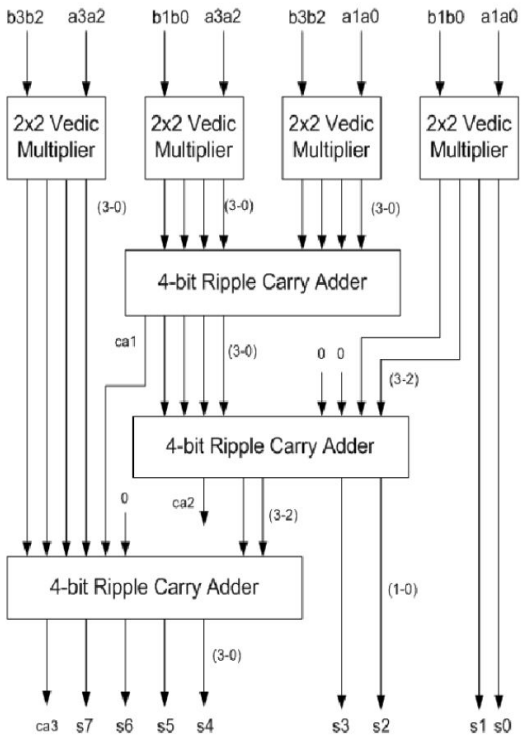



# Design

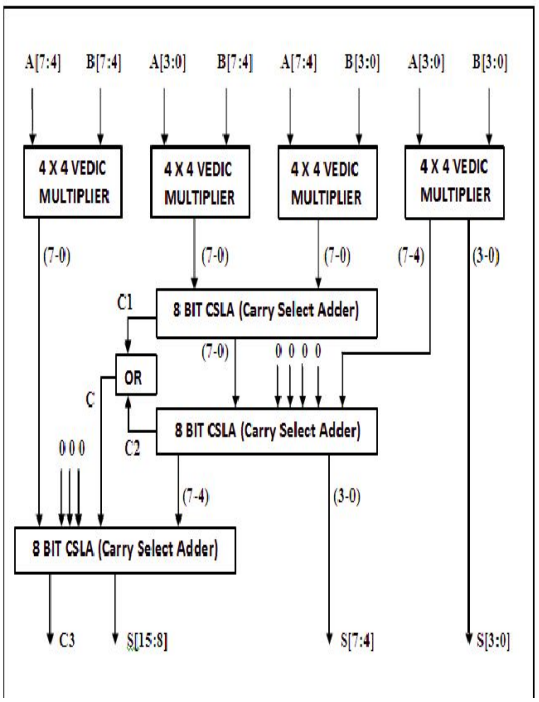
The IEEE journals we used for referring used RCA and CSLA for adders but to minimise delay we used CLA.

The fig below shows block diag of a 2x2 Vedic

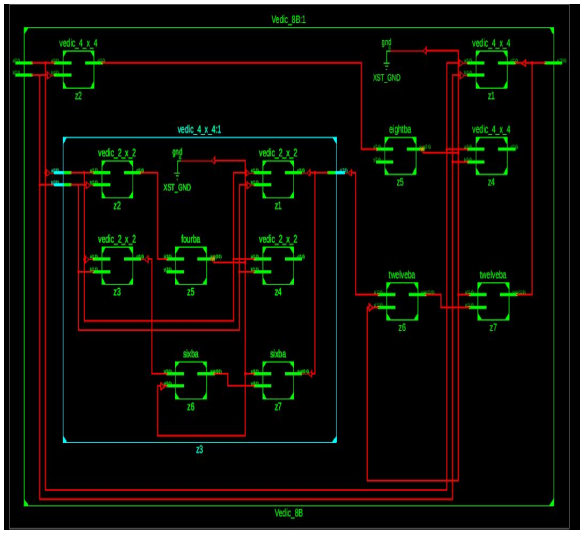
The fig below shows block diag of a 4x4 Vedic

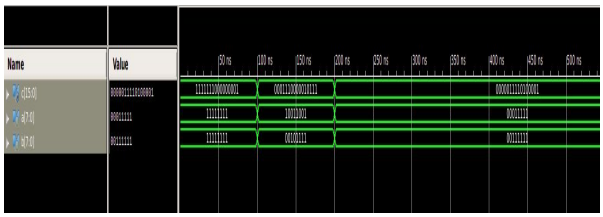



The fig below shows block diag of a 8x8 Vedic

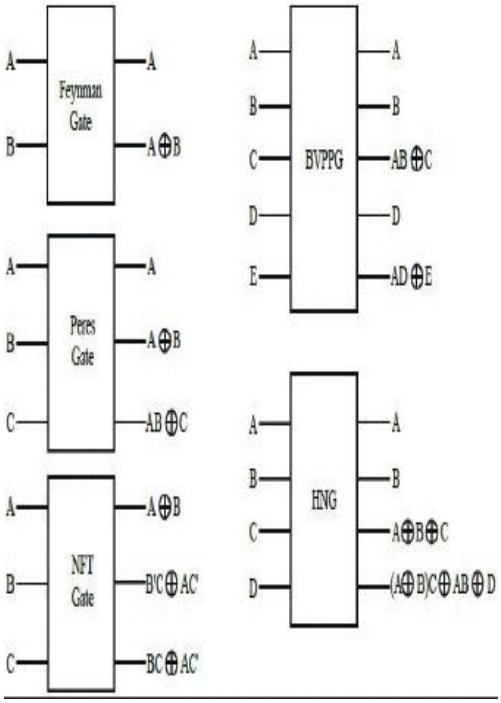



This are the RTL schematic and timing diagram of our design

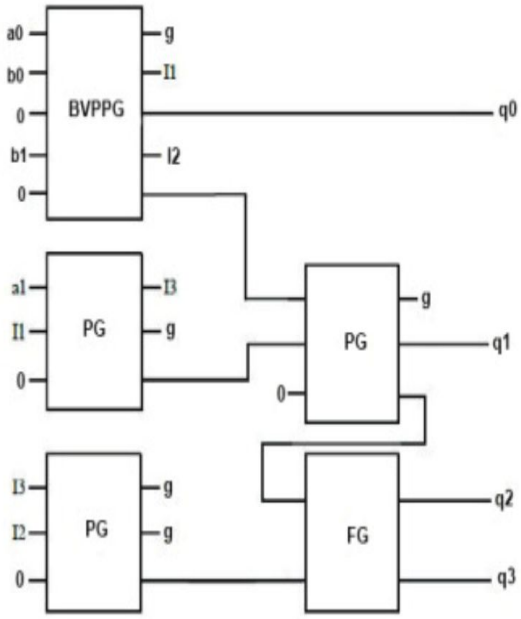




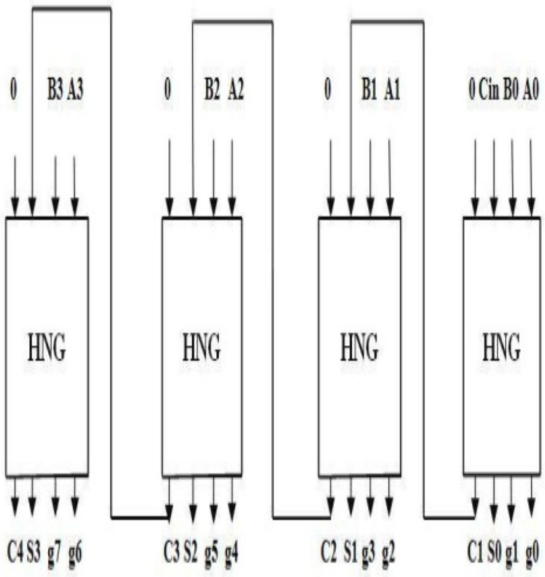
But now to optimise the Power further we used Reversible Logic Gates.



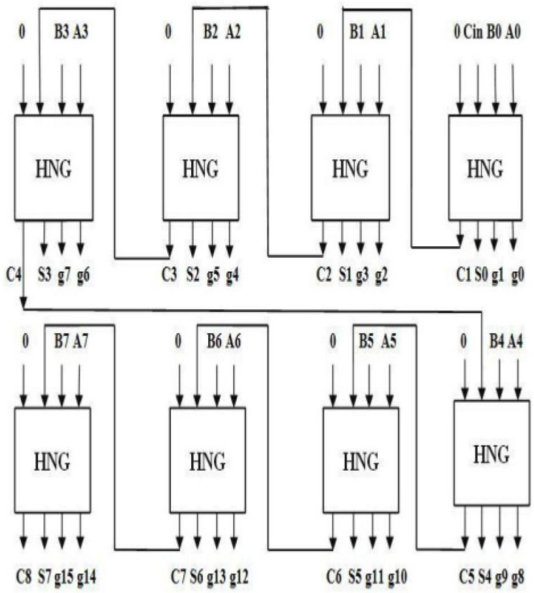

The fig given below shows block diag of a 2x2 Vedic Using reversible gates



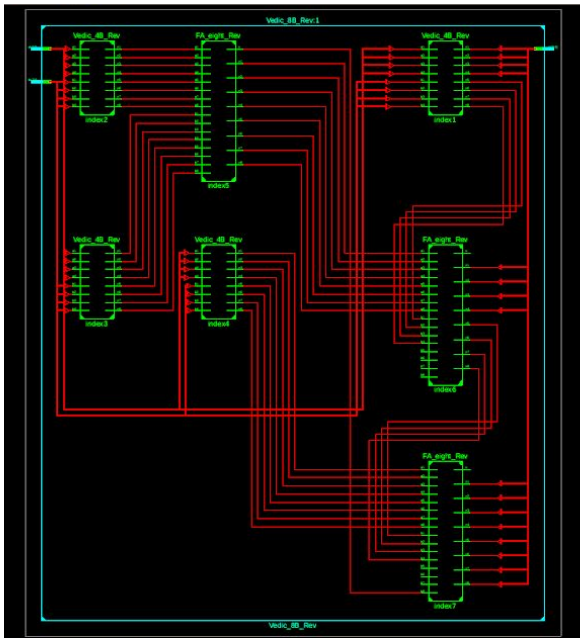
The fig given below is the block diag of a 4bit adder.We use this adder in place of the CLA in 4bit Vedic block for optimisation.

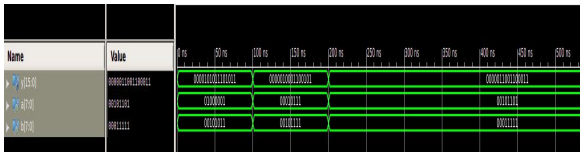



The fig given below is the block diag of a 8bit adder.We use this adder in place of the CLA in 8bit Vedic block for optimisation.




This are the RTL schematic and timing diagram of our design






# Results

We could not get hold of data for Power of a normal Vedic Multiplier.We calculated the power of our Unoptimised Vedic and compared the results with our Optimised Vedic.
Then we used Cadence tools,namely Genus and Innovus , to further optimise the Area and Power.We made a comparison between powers of our two designs based on the reports of the above mentioned Cadence tools.

| | Delay(ns) | No. of Slices | No. Of LUTs |
|---|---|---|---|
| Standard Paper's | 27.65 | 96 | 167 |
| Our Vedic | 21.917 | 125 | 219 |

| | Delay(ns) | Area(um2) | Power(nWatt) |
|---|---|---|---|
| Vedic Multiplier | 21.917 | 1965.669 | 80663.937 |
| Optimised Vedic | 21.618 | 1739.356 | 68043.714 |

| Tool | Genus | | Innovus | |
|---|---|---|---|---|
| Type Of Multiplier | Area (um2) | Power(nWatt) | Area(um2) | Power(nWatt) |
| Non-Optimised | 1965.669 | 80663.937 | 1965.6693 | 80374.69 |
| Optimised | 1739.356 | 68043.714 | 1739.3562 | 64621.77 |

# Conclusion

1. We conclude that by using CLA instead of RCA and CSA we have obtained a lesser Delay however we traded-off in Area and Power.
2. The Optimised Vedic Multiplier (using reversible logic) has significantly lower Area,Power and Delay .
3. Innovus gave lesser Power for both the Non-Optimised(Simple) Vedic and the Optimised Vedic Multiplier.

# Acknowledgement

The notable contributions of Prof.Azeemuddin Syed and the TA's namely Mayank Awasthi and Kunal wadhwani was very valuable. They helped us complete the project fully and on time with full understanding of the basic concepts to complex implementation of the project.
We also used several online resources,the signifacant ones are mentioned below.

# References

1. https://www.ijert.org/research/design-optimization-of-vedic-multiplier-using-reversible-logic-IJERTV3IS031946.pdf
2. https://ieeexplore.ieee.org/document/7475262(IEEE reference)