Yuchao Qin

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Education

Peking University — Beijing, China
B.S. in Applied Physics, Department of EECS, CGPA: 89/100 (WES-calculated: 3.81/4.00) — Sep 2022–Jul 2026

Research Experience

Stanford UGVR Program — Stanford University
Research Assistant to: Prof. Thierry Tambe — Jun 2025-Current

- **Toolchain Proficiency**: Learn how to use ASIP Design Tools and gain fluency in the nML language to construct custom ASIP architectures.
- **Functional Extension**: Extend ASIP design tool capabilities by integrating memory-aware profiling and logging mechanisms.
- **System-Level Implementation**: Implement a DMA-based DRAM subsystem on the FlexAcc core using nML to enable realistic memory modeling.
- **Cross-Design Profiling**: Collect and analyze memory access logs across multiple ASIP designs and algorithmic models to evaluate architectural trade-offs.

Lossless Compression Accelerator Architecture Design — Peking University
Research Assistant to: Prof. Bonan Yan — Sep 2024-Current

- Designed the workflow for a lossless compression accelerator using Probabilistic Circuits
- Developed and implemented Python-based rANS algorithm for compression
- Proposed a novel parallelized architecture to enhance computational efficiency
- Reproduced multiple neural-compression methods, including IVPF and Integer Discrete Flows

Quantization Research and Deployment of LLMs — HOUMO.AI
Research Assistant to: Senior Engineer Fan Wang — Jun 2024-Aug 2024

- Developed an efficient quantization algorithm for the BERT model
- Deployed the optimized BERT quantization model on XinHan1, an AI-specific chip developed by HOUMO.AI
- Conducted research on RAG architecture and inference overhead optimization

Process-in-Memory (PIM) Chip Design — Peking University
Research Assistant to: Prof. Yuchao Yang — Mar 2024-May 2024

- Reviewed over 30 academic papers and authored a comprehensive review on PIM research
- Presented four paper reviews at research group meetings

Publications

- **Author:** Anjunyi Fan, Xuejie Liu, Anji Liu, Qiuping Wu, **Yuchao Qin**, Guy Van den Broeck, Yitao Liang, Bonan Yan
- **Title:** Scaling Up Tractable Probabilistic Models Through Software-Hardware Codesign
- **Status:** Submitted to Nature Machine Intelligence (NMI)

Course Projects

- **5-stage RISC-V CPU Core:** In the course "Computer architecture and intelligent chip design", My team and I construct a 5-stage RISC-V CPU Core with branch prediction and win the first prize in the China College IC Competition. See the project at DeepSleep.
- **Matrix multiplication accelerator:** In the course "Principles and Design of Digital Systems(Honor Track)", I succesfully design an accelerator using systolic array. See the project at My_sysAcc.
- **Sparse Matrix-Dense Matrix Multiplication accelerator:** In the course "Chip Design using High-level Programming Language", I develop a hardware accelerator for SpMM. See the project at My_SpMM.
- **Detailed Placement for FPGA wirelength optimization:** In the course "Optimization and Machine Learning in VLSI Design Automation", My team and I develop EDA tools to solve the DP problems for FPGA. See the project at FPGA_r_op.

Relevant Courses

- **Circuit Design**: Principles and Design of Digital Systems(Honor Track); Principles of Analog Circuits(Honor Track); Advanced Analog Integrated Circuits Design; Advanced Digital Integrated Circuits Design
- **Chip Design**: Computer architecture and intelligent chip design; Optimization and Machine Learning in VLSI Design Automation; Chip Design using High-level Programming Language
- **Device & Physics**: Physics of Semiconductor; Integrated Circuit Devices; Integrated Circuit Manufacturing Technology; Quantum Mechanics
- **Artificial Intelligence**: Machine Learning for Electronics Information Engineering(Honor Track)
- **Signal Processing**: Signals and Systems (Honor Track)
- **Computing**: Introduction to Computation; Data Structure and Algorithm; Optimization for Computing System

Skill Summary

- **Languages:** Mandarin (Native); English
- **Programming:** C++, Python, MATLAB, Julia, ASIP design language
- **Circuit Design and Simulation:** Verilog, Cadence Virtuoso, HSpice, ASIP Design Tools, Chisel

Scholarships and Awards

- Silver Medal in the 38th Chinese Physics Olympiad Finals 2021
- Jiukun Scholarship 2022–2023
- Merit Student at Peking University 2023
- Most Valuable Player in "Peking Soccer Cup" 2023
- Tiktok Scholarship for EE Student 2023–2024
- Having been selected as a member of the inaugural Experimental Class in Electronic Information Science 2023–2026

Extra-curriculum Outreach

- Captain of EECS soccer team at Peking University — Oct, 2022–Current
  Led the team to the semifinals three years in a row, achieved one runner-up and two third-place finishes.
- Propaganda Principal of Experimental Class of Electronic Information Science (E Class) — Sep, 2023–Current
  Set up a WeChat public account
- Member of PKU AI Innovation and Entrepreneurship Club — Jun, 2024–Current
- Member of PKU Blockchain — Jun, 2024–Current

Appendix

If you would like to learn more about my background and research, feel free to explore my personal website at https://worldline22.github.io/