

請勿攜去  
Not to be taken away

第 1 頁(共 8 頁) Page 1 of 8

版權所有 不得翻印  
Copyright Reserved

香港中文大學  
The Chinese University of Hong Kong

二零二一至二二年度上學期科目考試  
Course Examination 1<sup>st</sup> Term, 2021-22

科目編號及名稱 IERG2060/ESTR2304 — Basic Analog and Digital Circuits  
Course Code & Title : .....

時間 2 小時 0 分鐘  
Time allowed : ..... hours ..... minutes

學號 座號  
Student I.D. No. : ..... Seat No. : .....

**Notes:**

1. Correct the final answers to 4 significant figures when necessary.
2. Answer ALL five (5) questions.
3. Each question carries 20%.
4. Put your answers on the answer book.

✓ Q1 — Sinusoidal Signals (20%):

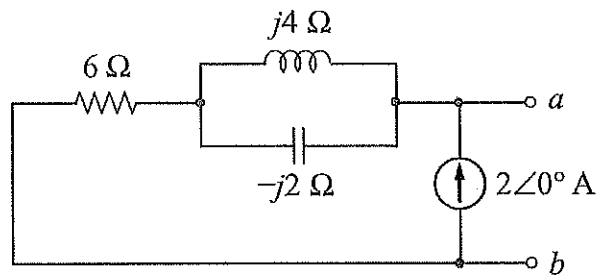


Fig. 1

Refer to the circuit in Fig. 1 for parts (a) to (c).

- (a) Determine the Thevenin and Norton equivalents ( $V_{Th}$ ,  $I_N$  and  $Z_{Th}$ ) at terminals  $a$ - $b$  in polar form ( $R\angle\theta$ ). (12%)
- (b) If a load  $Z_L$  is connected to the terminals  $a$ - $b$ , determine the value of  $Z_L$  in polar form ( $R\angle\theta$ ) for maximum average power transfer. (2%)
- (c) Find that maximum average power  $P_{max}$ . (2%)

Consider the following for parts (d) to (f).

The voltage across a load and the current through it are given by

$$v(t) = 339.4 \cos(60t + 90^\circ)\text{ V}$$

$$i(t) = 5.657 \cos(60t + 45^\circ)\text{ A}$$

- (d) Determine the complex power,  $S$ . (2%)
- (e) Determine apparent power,  $S$ . (1%)
- (f) Determine the power factor, pf. (1%)

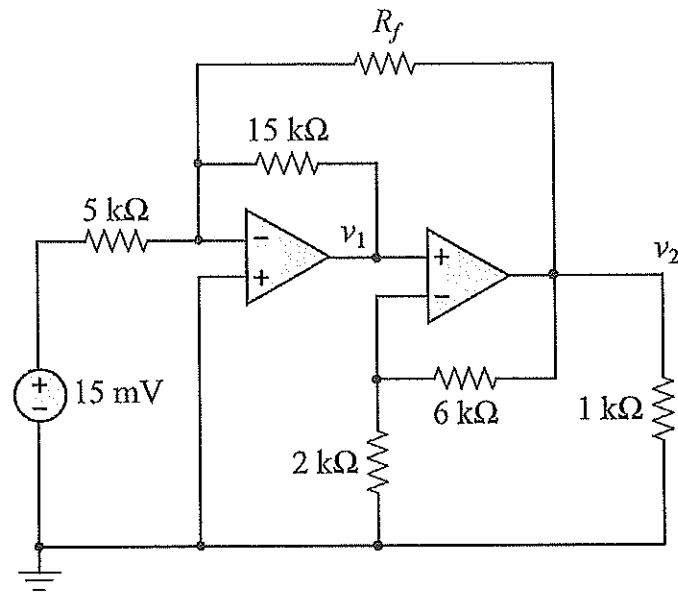
**Q2 — Operational Amplifier (20%):**

Fig. 2

Assuming that  $R_f = \infty$  for parts (a) and (b).

- (a) Determine the value of  $v_1$ . (5%)
- (b) Determine the value of  $v_2$ . (5%)

Consider  $R_f = 10 \text{ k}\Omega$  for part (c).

- (c) Determine the value of  $v_1$  and  $v_2$ . (10%)

**Q3 — Boolean Algebra (20%):**

- (a) Simplify the following expression by applying only one of the theorems. State the theorem used. (4%)

$$(V' + U + W)[(W + X) + Y + UZ'] + [(W + X) + UZ' + Y]$$

- (b) Factor the following expression to obtain a product-of-sums (POS). (4%)

$$A'B'C + B'CD' + EF'$$

- (c) Simplify the following expression to obtain a sum-of-products (SOP). (4%)

$$\{X + [Y'(Z + W)']'\}'$$

- (d) (i) Simplify the following function so that it can be realized using two OR gates and two AND gates. (4%)

$$F = (V + W + X)(V + X + Y)(V + Z)$$

- (ii) Draw that circuit (using two OR gates and two AND gates). (4%)

**Q4 — Combinational Logic (20%):**

Consider a logic function  $F$  that has four inputs  $A, B, C$  and  $D$ , which are binary representation of the number 0 to 15.  $A$  is the most significant bit and  $D$  is the least significant bit. Therefore,

$$ABCD = 0111 \quad \text{represents 7 (0111}_2\text{), and}$$

$$ABCD = 1100 \quad \text{represents 12 (1100}_2\text{).}$$

The function  $F = 1$  if the input number is a prime number, and  $F = 0$  if not. For this question, 1 is consider to be a prime while 0 is not. In other words,

$$F = \Sigma m(1, 2, 3, 5, 7, 11, 13)$$

- (a) Draw a 4-input Karnaugh map for output  $F$ . (8%)  
(b) Find the minimum sum-of-products (SOP) for  $F$  using the Karnaugh map. (4%)  
(c) Find the minimum sum-of-products (SOP) for  $F'$  using the Karnaugh map. (4%)  
(d) Find the minimum product-of-sums (POS) for  $F'$  using answer in (c). (4%)

**Q5 — Sequential Logic (20%):**

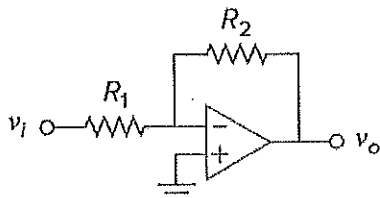
Using  $D$  flip-flops, design a 3-bit counter ( $ABC$ ) which counts in the sequence:

000, 010, 111, 101, 011, 110, (repeat) 000, ...

- (a) Complete the following transition table. (8%)

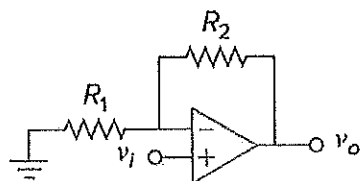
$ABC$	$A^+B^+C^+$
000	
001	
...	

- (b) Draw the Karnaugh maps for  $D_A$ ,  $D_B$  and  $D_C$ . (3%)
- (c) Using the Karnaugh maps, find the minimum sum-of-products for  $D_A$ ,  $D_B$  and  $D_C$ . (3%)
- (d) Draw the designed circuit using  $D$  flip-flops, AND gates and OR gates. Note that each  $D$  flip-flop is capable of producing both  $Q$  and  $Q'$ , and is negative-edge-triggered. (6%)

**APPENDIX****Op amp circuit****Name/output-input relationship**

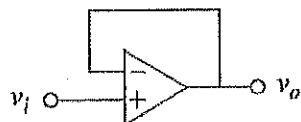
Inverting amplifier

$$v_o = -\frac{R_2}{R_1} v_i$$



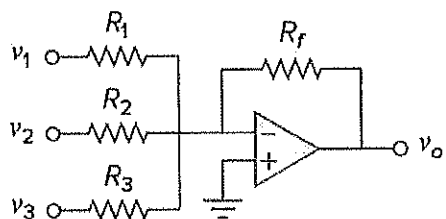
Noninverting amplifier

$$v_o = \left(1 + \frac{R_2}{R_1}\right) v_i$$



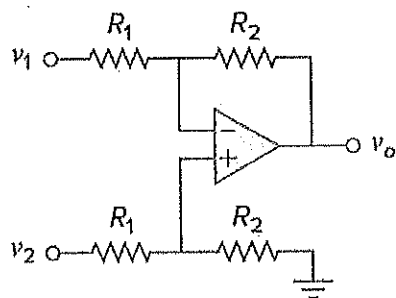
Voltage follower

$$v_o = v_i$$



Summer

$$v_o = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$$



Difference amplifier

$$v_o = \frac{R_2}{R_1} (v_2 - v_1)$$

## Operations with 0 and 1:

1.  $X + 0 = X$

1D.  $X \cdot 1 = X$

2.  $X + 1 = 1$

2D.  $X \cdot 0 = 0$

## Idempotent laws:

3.  $X + X = X$

3D.  $X \cdot X = X$

## Involution law:

4.  $(X')' = X$

## Laws of complementarity:

5.  $X + X' = 1$

5D.  $X \cdot X' = 0$

## Commutative laws:

6.  $X + Y = Y + X$

6D.  $XY = YX$

## Associative laws:

7.  $(X + Y) + Z = X + (Y + Z)$   
 $= X + Y + Z$

7D.  $(XY)Z = X(YZ) = XYZ$

## Distributive laws:

8.  $X(Y + Z) = XY + XZ$

8D.  $X + YZ = (X + Y)(X + Z)$

## DeMorgan's laws:

9.  $(X + Y)' = X'Y'$

9D.  $(XY)' = X' + Y'$

## Uniting theorems:

1.  $XY + XY' = X$

1D.  $(X + Y)(X + Y') = X$

## Absorption theorems:

2.  $X + XY = X$

2D.  $X(X + Y) = X$

## Elimination theorems:

3.  $X + X'Y = X + Y$

3D.  $X(X' + Y) = XY$

## Duality:

4.  $(X + Y + Z + \dots)' = XYZ \dots$

4D.  $(XYZ \dots)' = X + Y + Z + \dots$

## Theorems for multiplying out and factoring:

5.  $(X + Y)(X' + Z) = XZ + X'Y$

5D.  $XY + X'Z = (X + Z)(X' + Y)$

## Consensus theorems:

6.  $XY + YZ + X'Z = XY + X'Z$

6D.  $(X + Y)(Y + Z)(X' + Z) = (X + Y)(X' + Z)$

<b>D Flip-Flop</b>		
<b>D</b>	<b><math>Q^+</math></b>	<b>Operation</b>
0	0	Reset
1	1	Set

<b>SR Flip-Flop</b>			
<b>S</b>	<b>R</b>	<b><math>Q^+</math></b>	<b>Operation</b>
0	0	$Q$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

$$Q^+ = JQ' + K'Q$$

<b>JK Flip-Flop</b>			
<b>J</b>	<b>K</b>	<b><math>Q^+</math></b>	<b>Operation</b>
0	0	$Q$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'$	Complement

$$Q^+ = T \oplus Q = TQ' + T'Q$$

<b>T Flip-Flop</b>		
<b>T</b>	<b><math>Q^+</math></b>	<b>Operation</b>
0	$Q$	No change
1	$Q'$	Complement

— END —