香 港 中 文 大 學

The Chinese University of Hong Kong

二零二二至二三年度上學期科目考試

Course Examination 1st Term, 2022-23

科目編號及名稱
Course Code & Title : **IERG 2060 Basic Analog and Digital Circuits**

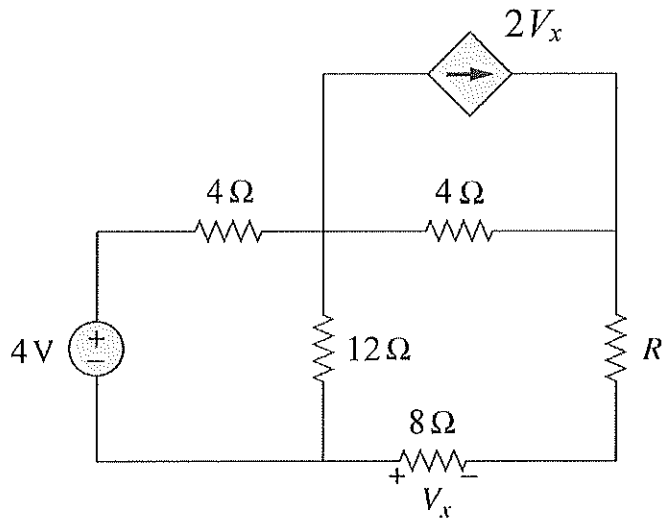
時間　　小時　　分鐘
Time allowed : 2 hours 0 minutes

學號　　座號
Student I.D. No. : ..... Seat No. : .....

- **This paper comprises EIGHT questions.**
- **Answer ANY FOUR questions from Questions 1 to 5 AND answer ALL from Questions 6 to 8.**
- **Each question carries 20 points**
- **Total score of this paper is 140 points.**

Question 1

In the following circuit, determine the maximum power transferred to the resister R.

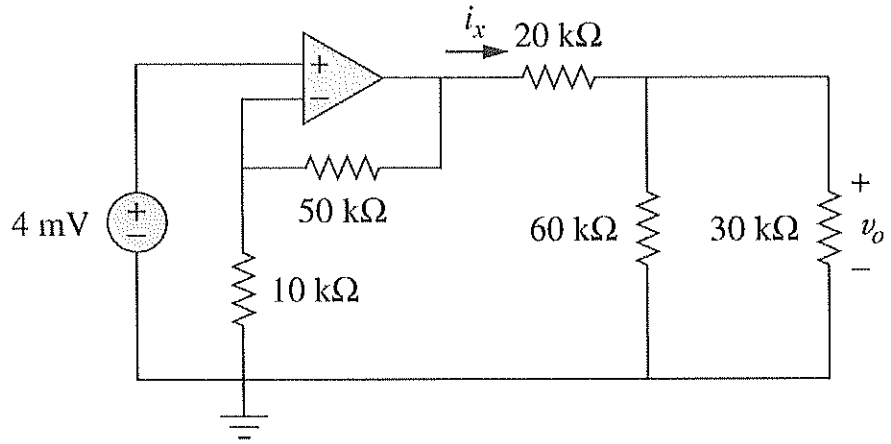


Question 2

In the following circuit,

(a) determine the current i_x, and voltage v_o.

(b) determine the power dissipated by the 60kΩ resistor.

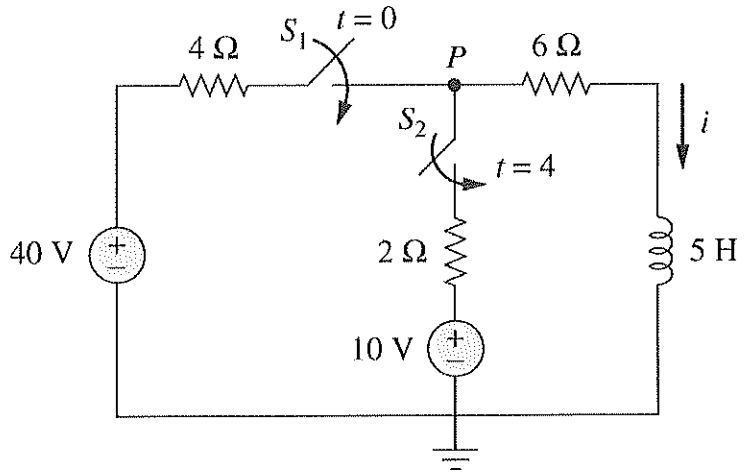


Question 3

In the following circuit, initially, both switches S_1 and S_2 are opened for a long time. Switch S_1 is closed at t=0, while switch S_2 is closed at t=4. Determine the current i passing through the inductor,

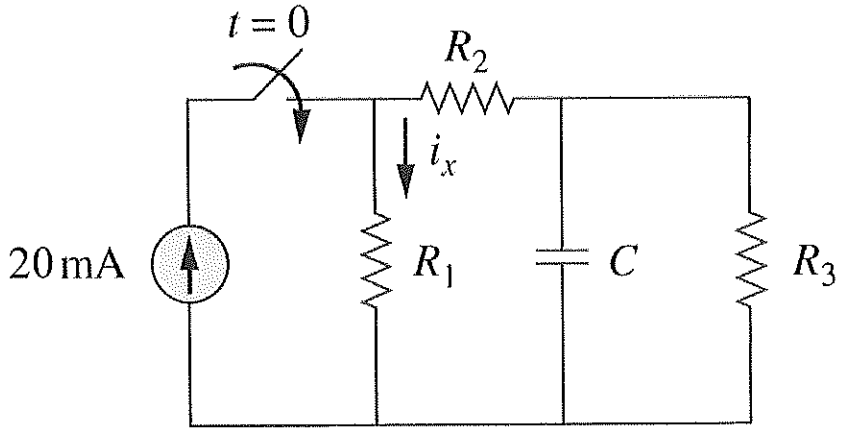
(a) for $t > 0$ (and before switch S_2 is closed), and

(b) for $t > 4$, (after switch S_2 is closed)



Question 4

In the following circuit, the switch is closed at t=0. Find i_x for $t>0$, *assuming* R_1=R_2=2kΩ, R_3=4kΩ, and C=0.25mF.



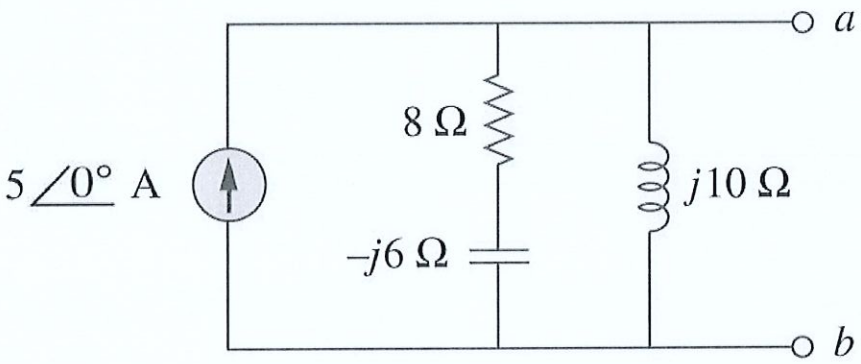
Question 5

In the following AC circuit, using phasor method,

(a) determine the Thévenin equivalent impedance across ports *a*-*b*.

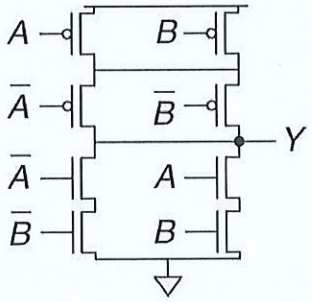
(b) determine the Thévenin equivalent voltage across ports *a*-*b*.

*Express your answers in rationalized complex number form, that is, $x+jy$.



Question 6

(a) The following figure shows a logic gate circuit using CMOS gates. Write a truth table with two inputs, *A* and *B*. and output *Y*. Determine the name of this logic function.



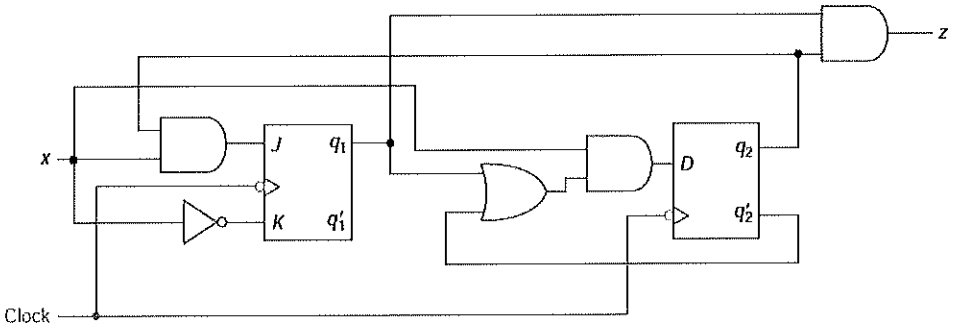
(b) For each of the following Boolean expressions, ***simplify*** the expression and ***sketch*** the simple combinational circuit to realize your answer. Label the inputs and output clearly.

(i) $Y = ABCD + \bar{A}B\bar{C}D + \overline{(\bar{B} + D)}E$

(ii) $Y = \bar{A}\bar{B} + \bar{A}B\bar{C} + \overline{(\bar{A} + C)}$

Question 7

Consider the following logic circuit with one J-K flip-flop and one D flip-flop. x is the input variable and z is the output variable. Clock is the clock input.



(a) Express the boolean expressions for the inputs of the J-K flip-flop and the D flip-flop, namely J, K, and D, in terms of the input variable x, and their current state variables, q_1, q_1', q_2 and q_2'.

(b) Express the boolean expression for the output variable z, in terms of the input variable x, and their current state variables, q_1, q_1', q_2 and q_2'.

(c) Write down the state transition table, in terms of present states, input, next states, output and the flip-flop inputs.

(d) Construct the state diagram, labelled with states in circles, and input/output on each arrow.

Question 8

Design a synchronous counter that goes through the following sequence:

1→ 3→ 5→ 7 →4 →2→ 0→ 6→ and repeat

using D flip flops. Please perform the following procedures:

(1) define the input variables,

(2) determine the required number of flip flops,

(3) show a state-transition table,

(4) derive the Boolean expressions for the inputs of the flip flops and output, and

(5) construct a labelled logic circuit diagram.

**** END ****

APPENDIX

	Axiom		Dual	Name
A1	$B = 0$ if $B \neq 1$	A1′	$B = 1$ if $B \neq 0$	Binary field
A2	$\overline{0} = 1$	A2′	$\overline{1} = 0$	NOT
A3	$0 \bullet 0 = 0$	A3′	$1 + 1 = 1$	AND/OR
A4	$1 \bullet 1 = 1$	A4′	$0 + 0 = 0$	AND/OR
A5	$0 \bullet 1 = 1 \bullet 0 = 0$	A5′	$1 + 0 = 0 + 1 = 1$	AND/OR

	Theorem		Dual	Name
T1	$B \bullet 1 = B$	T1′	$B + 0 = B$	Identity
T2	$B \bullet 0 = 0$	T2′	$B + 1 = 1$	Null Element
T3	$B \bullet B = B$	T3′	$B + B = B$	Idempotency
T4		$\overline{\overline{B}} = B$		Involution
T5	$B \bullet \overline{B} = 0$	T5′	$B + \overline{B} = 1$	Complements

	Theorem		Dual	Name
T6	$B \bullet C = C \bullet B$	T6′	$B + C = C + B$	Commutativity
T7	$(B \bullet C) \bullet D = B \bullet (C \bullet D)$	T7′	$(B + C) + D = B + (C + D)$	Associativity
T8	$(B \bullet C) + B \bullet D = B \bullet (C + D)$	T8′	$(B + C) \bullet (B + D) = B + (C \bullet D)$	Distributivity
T9	$B \bullet (B + C) = B$	T9′	$B + (B \bullet C) = B$	Covering
T10	$(B \bullet C) + (B \bullet \overline{C}) = B$	T10′	$(B + C) \bullet (B + \overline{C}) = B$	Combining
T11	$(B \bullet C) + (\overline{B} \bullet D) + (C \bullet D)$ $= B \bullet C + \overline{B} \bullet D$	T11′	$(B + C) \bullet (\overline{B} + D) \bullet (C + D)$ $= (B + C) \bullet (\overline{B} + D)$	Consensus
T12	$\overline{B_0 \bullet B_1 \bullet B_2 \ldots}$ $= (\overline{B_0} + \overline{B_1} + \overline{B_2} \ldots)$	T12′	$\overline{B_0 + B_1 + B_2 \ldots}$ $= (\overline{B_0} \bullet \overline{B_1} \bullet \overline{B_2})$	De Morgan's Theorem

De Morgan's Theorem $\overline{A \cdot B} = \overline{A} + \overline{B}$; $\overline{A + B} = \overline{A} \cdot \overline{B}$

(a) *JK* Flip-Flop

J	K	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}(t)$	Complement

(b) *SR* Flip-Flop

S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

(c) *D* Flip-Flop

D	$Q(t+1)$	Operation
0	0	Reset
1	1	Set

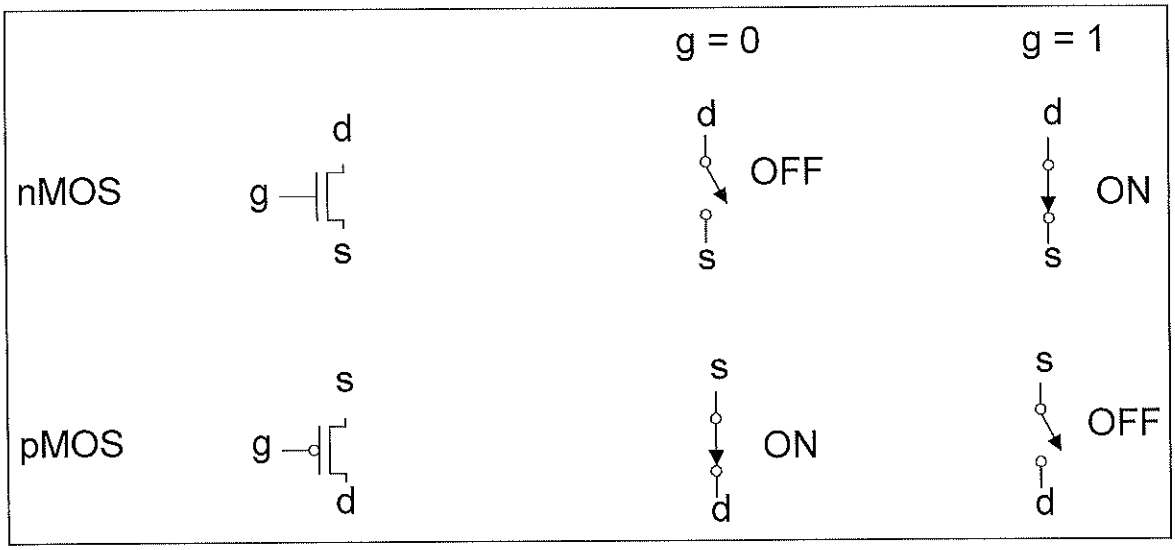
(d) *T* Flip-Flop

T	$Q(t+1)$	Operation
0	$Q(t)$	No change
1	$\overline{Q}(t)$	Complement

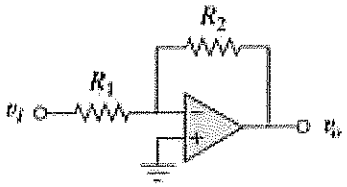
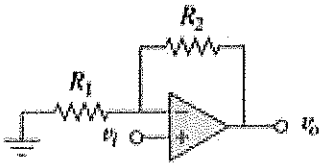
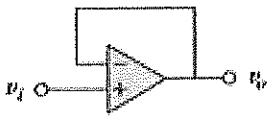
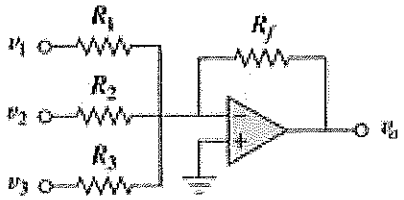
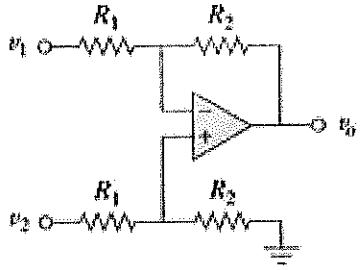
J-K flip flop: $Q^+ = J \cdot \overline{Q} + \overline{K} \cdot Q$

T flip flop: $Q^+ = T \cdot \overline{Q} + \overline{T} \cdot Q$

CMOS Logic



Summary of basic op amp circuits.

Op amp circuit	Name/output-input relationship
	Inverting amplifier $v_o = -\frac{R_2}{R_1} v_i$
	Noninverting amplifier $v_o = \left(1 + \frac{R_2}{R_1}\right) v_i$
	Voltage follower $v_o = v_i$
	Summer $v_o = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$
	Difference amplifier $v_o = \frac{R_2}{R_1}(v_2 - v_1)$

- End -