Computer Architecture

Course Administrative Details

Course Title	*Computer Architecture*		
Instructor(s)	*Nikolaos Mavridis*	**Instructor's e-mail**	*nmavrid@gmail.com*
Course #	*???*	**Course Type**	*Core*
Faculty	*Computer Science and Engineering*	**Major**	*Computer science*
Academic year	*2016-2017*	**Semester Offered**	*Fall*
No. of Credits	*6 ECTS*	**Total workload on average**	*12 hrs. per week inc. 8 hrs. of self-study*
Lecture Hours	*2 per week*	**Lab Hours**	*2 per week*
Language	*English*	**Frequency**	*Weekly*
Target Audience	*Bachelors*	**Anticipated Enrollment**	*129 students*
Studying year	*1*		
Grading Mode	*A, B, C, D*	**Keywords**	*Architecture, Microprocessor, Assembly Language, Digital Systems, Cache Memory etc..*

Course outline

[Short description of the course. Example: This is an introductory course in computer architecture. After a general introduction, we adopt a bottom-up approach, starting from fundamentals of digital systems, moving from combinatorial to sequential to higher-level components, all the describing the building blocks of a modern CPU. We also quickly cover an introduction to VHDL for hardware description. Then, we move to the assembly-language level, and we consider the basic concepts of it as well as its relation to higher-level languages, and quickly introduce fundamentals of parallelism, pipelines, and cache memories.

Course Delivery

In general, almost every Wednesday, there will be one 2-hour lecture (all students) together with one 2-hour lab (in sections of 33 students)

Prerequisite courses

This is a First year's bachelors course, without pre-requisite courses

Required background knowledge

[Example: Basic understanding of iuniversity-entrance-level mathematics, physics, as well as programming

Course structure

[Example: IA – Individual Assignment, RQ – reading questions, GA – group assignment etc.]

Week# / Date	***Topic***	***Assignments***
Week1/Aug24	*Introduction to DS*	
Week2/Aug31	*Binary Arithmetic and Logic Gates*	
Week3/Sep7	*Combinatorial 1 and 2 (No Glitches) (Ch2)*	
Week4/Sep14	*Combin + Sequential (Basic FSM, no timing) (Ch3)*	
Week5/Sep21	*Basic Intro to VERILOG (Ch4)*	*Lab on Verilog*
Week6/Sep28	*Building Blocks + FP Arithmetic (Ch5)*	
Week7/Oct5	*MidTerm*	
Week8/Oct12	*Intro to MIPS Assembly (Ch6) PartA*	*Lab on MIPS Assembly 1*
Week9/Oct19	*Intro to MIPS Assembly (Ch6) PartB*	*Lab on MIPS Assembly 1*
Week10/Oct 26	*Data Paths & Pipelines (Ch7) PartA*	
Week11/Nov 2	*Data Paths & Pipelines (Ch7) PartB*	
Week12/Nov 9	*Caches & Memory (Ch8) PartA*	
Week13/Nov 16	*Caches & Memory (Ch8) PartB*	
Week14/Nov 26	*Review + Projects*	
Finals Dec1-12	*Finals*	

Textbook(s)

B1) Digital Design and Computer Architecture, Second Edition, D. Harris and S. Harris (2012) [Primary TextBook!]
B2) Computer Organization and Design, Revised Fourth Edtion: The Hardware/Software Interface (The Morgan Kaufmann Series in Computer Architecture and Design), 2012

Reference Materials

As extra reading, you might want to visit the ARM processors versions of the books, as well as:
Computer Architecture, Fifth Edition: A Quantitative Approach (The Morgan Kaufmann Series in Computer Architecture and Design)

Computer Resources

Students should have Laptops with installed the MIPS and Verilog Simulators

Laboratory Exercises

1. Verilog Exercises
2. MIPS Assembly Part 1
3. MPIS Assembly Part2

Laboratory Resources

MIPS + Verilog Simulators (TBD)

Grading criteria

Assignments/Projects (30%), Midterm (30%), and Final Exam (40%)

Late Submission Policy

This policy will be strictly applied in this course. If a personal emergency should arise that affects your ability to turn in an assignment in a timely fashion, you must contact the course instructor BEFORE the deadline to get a "Special Late Submission Approval" from the course instructor. Without the "Special Late Submission Approval" submissions will be still accepted up to 48 hours late, but with a 50% penalty. No "Special Late Submission Approval" will be granted after the deadline. All late submissions should be submitted by email directly to the instructors

Cooperation Policy and Quotations

We encourage vigorous discussion and cooperation in this class. You should feel free to discuss any aspects of the class with any classmates. However, we insist that any written material that is not specifically designated as a Team Deliverable be done by you alone. This includes answers to reading questions, individual reports associated with assignments, and labs. We also insist that if you include verbatim text from any source, you clearly indicate it using standard conventions of quotation or indentation and a note to indicate the source.

Additional information