Computer Architecture (BS-1)
Innopolis University
Autumn, 2016

Homework 1. Memory and performance

Due: 29/11/2016 15:30

Submission:

Each task file should be named exactly as asked in the assignment. File name should be the same as module name. Please format your submission as a PDF file and name it as following:

hw2_{yoursurname}_{yourname}.pdf

Please note that no braces are needed. Example file name: hw2_ivanov_ivan.pdf
Upload the file into the moodle and be aware, that no submissions are accepted after the deadline.

Grading criterias:

- corresponding to the naming convention, correctness of submission – 10%
- exercises – 90%

Exercise 1

You are provided with an initial page table, where LRU (Least Recently Used) column works the following way: the older an entry is, the lower its LRU will be. Each moment an entry is used, its LRU number is set to 4 (because it's now the most recently used). LRU's of other entries' are decreased by one.

Initial Page table:

Index	Valid	PPN or On disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

Additionally, you are given a TLB:

Initial TLB:

Valid	VPN	PPN	LRU
1	11	12	2
1	7	4	3
1	3	6	4
0	4	9	1

Consider the stream of virtual addresses provided below:
0x0FFF
0x7A28
0x3DAD
0x3A98
0x1C19
0x1000
0x22D0

Addresses from the stream are used (read/write) sequentially.
Task: evaluate the final page table and TLB values after using all the addresses from the list.

Exercise 2
What are some advantages and disadvantages of using a larger virtual/physical page size? Give detailed answer.

Exercise 3
Fill into the blanks of the following table. Comment your decisions.

Virtual address bits	Physical address bits	Page Size	VPN bits	PPN bits
32	32	16KB		
32	26			13
	32		21	
		32KB	25	
64			48	

Exercise 4
Consider that your system bus supports 36 bit addresses and your 2Gb RAM is broken into pages of 2KB size. How many bits are there in PPN and VPN? If all the flags (valid, dirty, etc) take up 12 per entry, how many bits does an entire page table consume?

Exercise 5
Assuming 32 bits of physical memory, how many total bits of storage are required for an 8-way set associative 4KB cache, if blocks are 16B and it uses write back and LRU replacement?

Exercise 6
You are provided with a combined memory (cache + RAM) structured the following way:
- Cache block size 512 Byte
- Cache size 512 KB (Byte addressed)
- Memory size 2 GB (Byte addressed)

How many number of cache blocks are needed? What is the structure of the addresses for the following cache structures:

- direct mapped cache
- fully associative cache
- 4-way set-associative cache;

Exercise 7
Consider the following MIPS program:

```
      addi  $s0, $0, 0 # i = 0
      add   $s1, $0, $0 # sum = 0
      addi  $t0, $0, 10 # $t0 - 10
loop:
      slt   $t1, $s0, $t0 # if (i < 10), $t1 == 1, else $t1 = 0
      beq   $t1, $0, done # if (i >= 10), branch to done
      add   $s1, $s1, $s0 # sum += i
      addi  $s0, $s0, 1 # i++
      j     loop
done:
```

(a) How many cycles does it take to execute the following program on the multicycle MIPS processor?
(b) What is the CPI of this program?

Exercise 8
You are given the following delay times for particular elements of MIPS processor:

Element	**Delay**
ALU	3 ns
CPU Registers	2 ns
Instruction Memory	5 ns
Data Memory	5 ns
Adder	1 ns
Other components	0 ns

What will be the execution time of the following MIPS program on different CPU implementations (single-cycle, multi-cycle)?

```
start:
        addi    $1, $zero, 4
        add     $2, $zero, $zero
        add     $3, $zero, $zero

sum:
        slt     $5, $1, $2
        beq     $5, $zero, endsum

        lw      $6, 0($3)
        addi    $6, $6, 10
        sw      $6, 0($3)
        addi    $1, $1, 1

        addi    $3, $3, 4

        j sum

endsum:
```

State your assumptions and give an explained answer.