Computer Architecture (BS-1)
Innopolis University
Autumn, 2016

# Homework 1. Verilog

**Comments**: in this homework you are asked to implement the following exercises using Hardware Definition Language (HDL). Particularly Verilog. This is an individual assignment.

**Due: 28/09/2016 15:30**

**Submission:**

Each task file should be named exactly as asked in the assignment. File name should be the same as module name. Please zip all three .v files together into one archive and name it as following:

*hw1_{yoursurname}_{yourname}.zip*

Please note that no braces are needed. Example file name: hw1_ivanov_ivan.zip
Upload the file into the moodle and be aware, that no submissions are accepted after the deadline.

**Grading criterias:**

- corresponding to the naming convention, correctness of submission – 10%
- exercises – 90%

Please check, that you code is compilable, otherwise we will not be able to check it. The code will be checked via Altera Modelsim.

**Tasks:**

1. Write an HDL module called "**minority**". It receives three inputs, a, b, and c. It produces one output, y, that is TRUE if at least two of the inputs are FALSE.
2. Write an HDL module for a hexadecimal seven-segment display decoder. The decoder should handle the digits A, B, C, D, E, and F as well as 0-9. Name the module "**segmentdisplay**".
3. Write an HDL module for an eight-input priority circuit. Name the module "**priority**".

Eight-input priority circuit can be described as an analog to the solution of the following problem (but in this case it will have 8 inputs, unlike 4 described in problem):

*Problem:*
*The dean, the department chair, the teaching assistant, and the dorm social chair each use the auditorium from time to time. Unfortunately, they occasionally conflict, leading to disasters such as the one that occurred when the dean's fundraising meeting with crusty trustees happened at the same time as the dorm' s BTB1 party. Alyssa P. Hacker has been called in to design a room reservation system.*
*The system has four inputs, A3, . . . , A0, and four outputs, Y3, . . . , Y0. These signals can also be written as A3:0 and Y3:0. Each user asserts her input when she requests the auditorium for the next day. The system asserts at most one output, granting the auditorium to the highest priority user. The dean, who is paying for the system, demands highest priority (3). The department chair, teaching assistant, and dorm social chair have decreasing priority.*