A CMOS Programmable Analog Standard Cell Library in Skywater 130nm Open-Source Process

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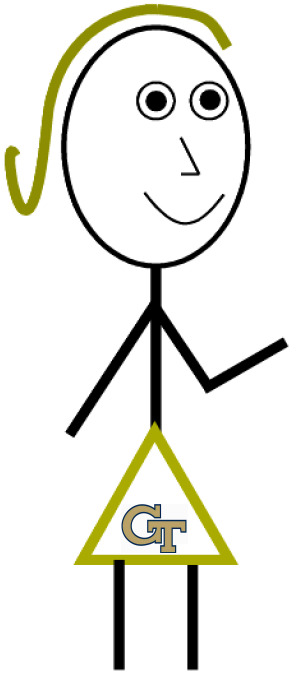
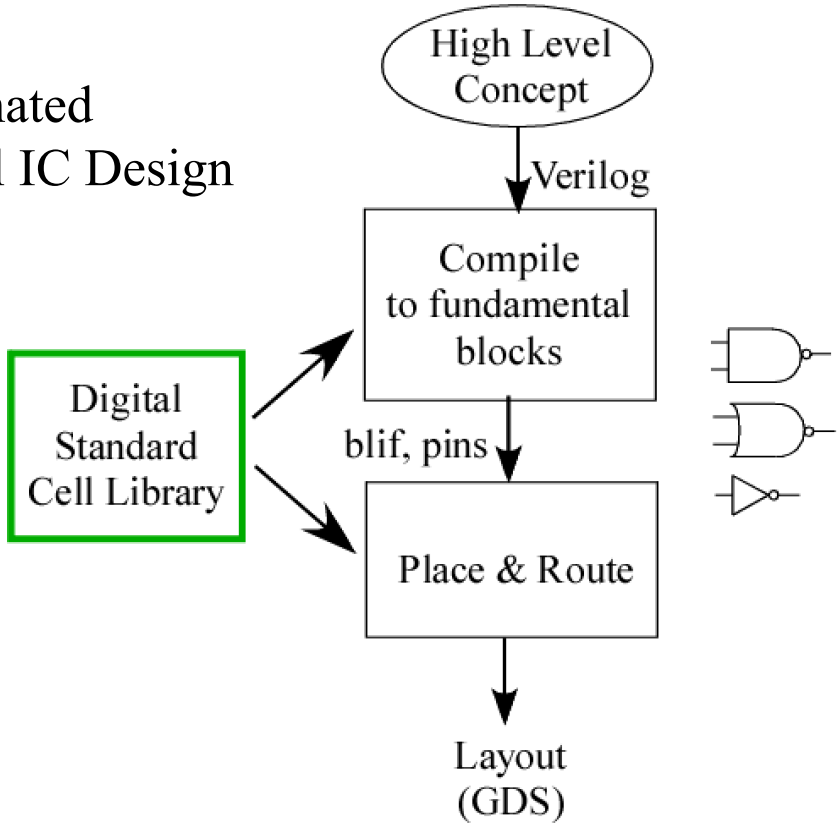
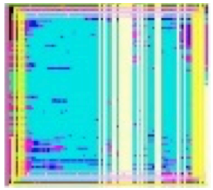
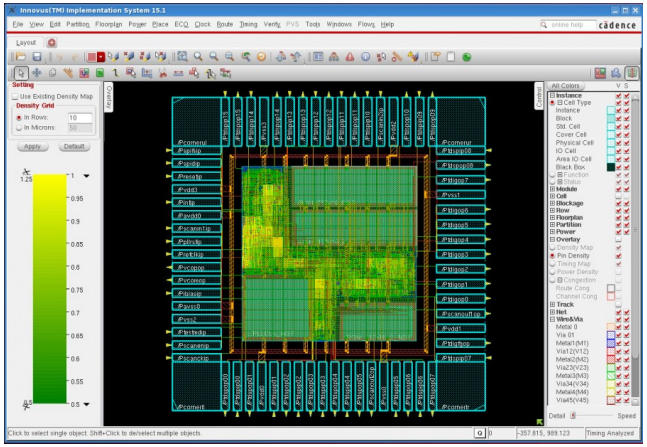
University of Mississippi

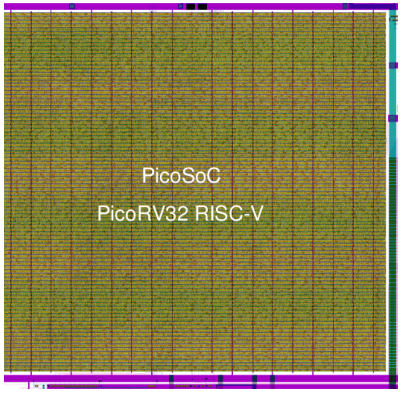


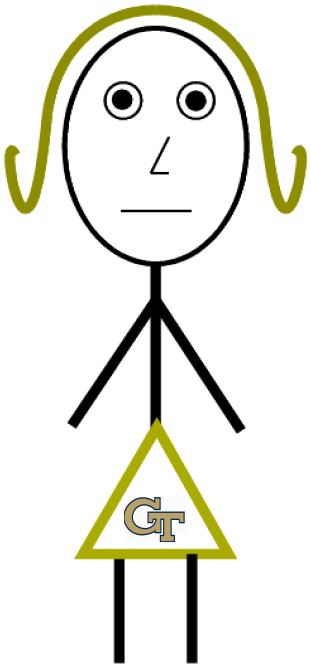
Automated Digital IC Design





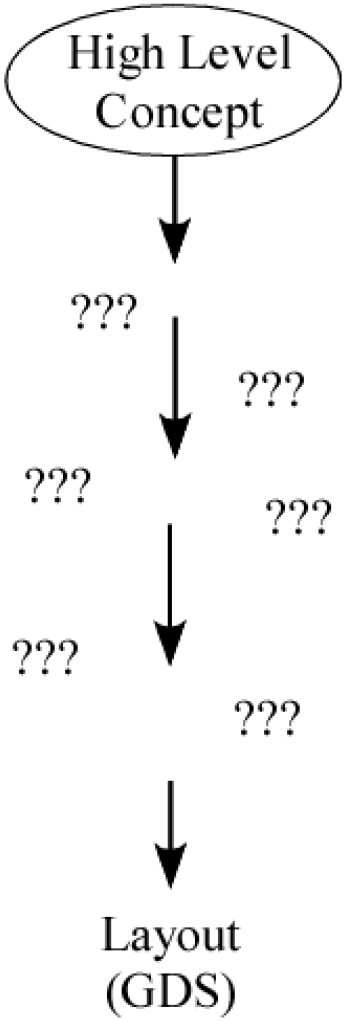


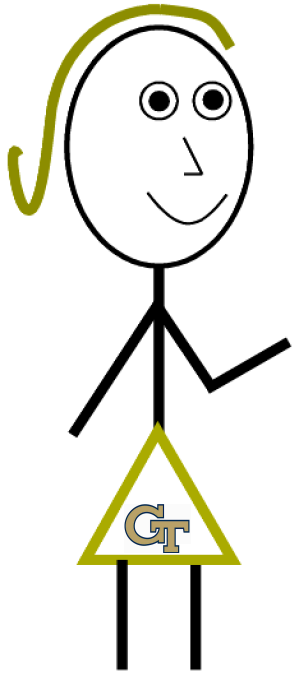




Automated
Analog IC Design

What if we had an
Analog Standard
Cell Library?





Automated
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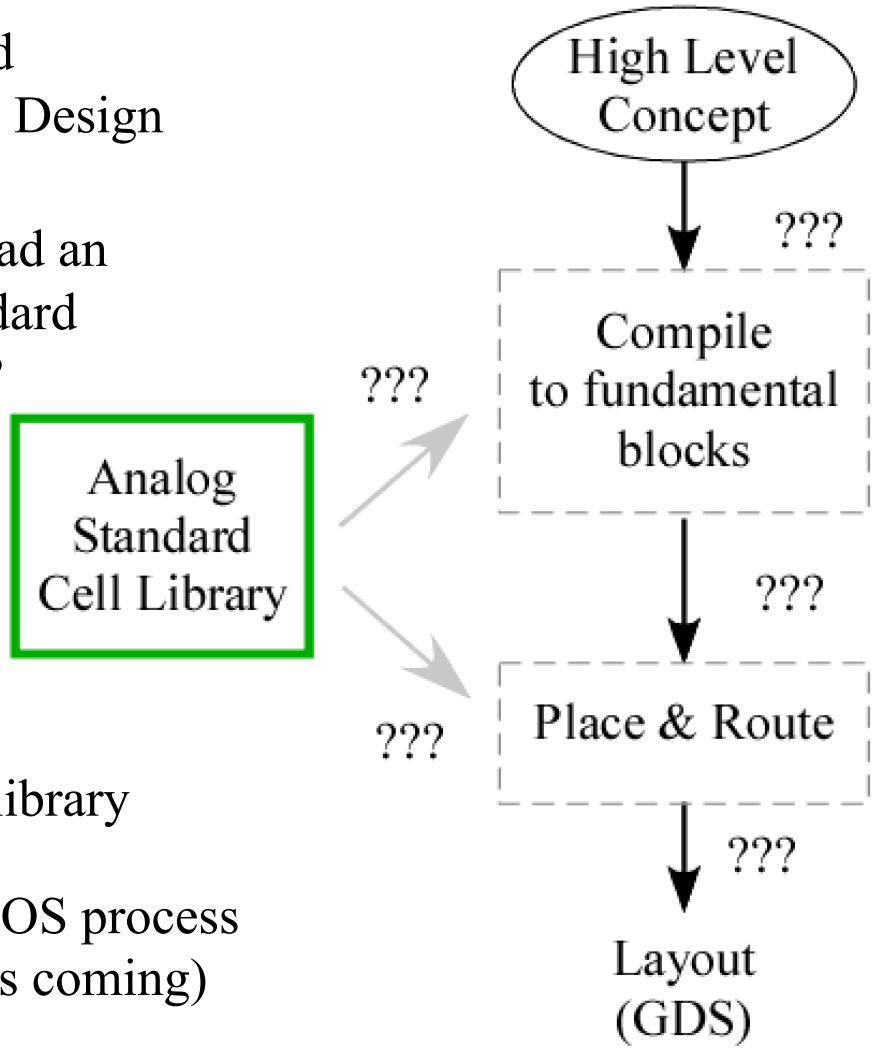


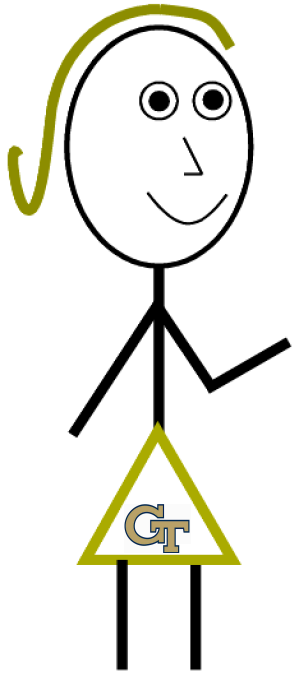
Talk discusses the first standard cell library

Open-Source, Skywater 130nm CMOS process
(in fab, measurement results coming)

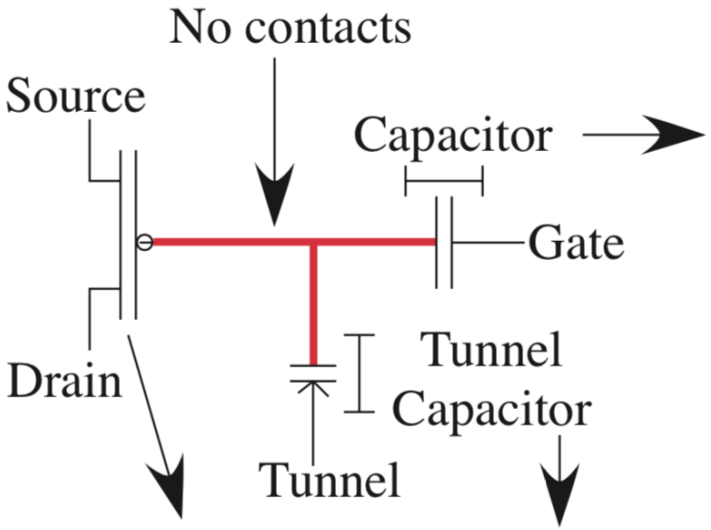
Barry Muldrey
U. Of Mississippi

Parker Hardy
U. Of Mississippi

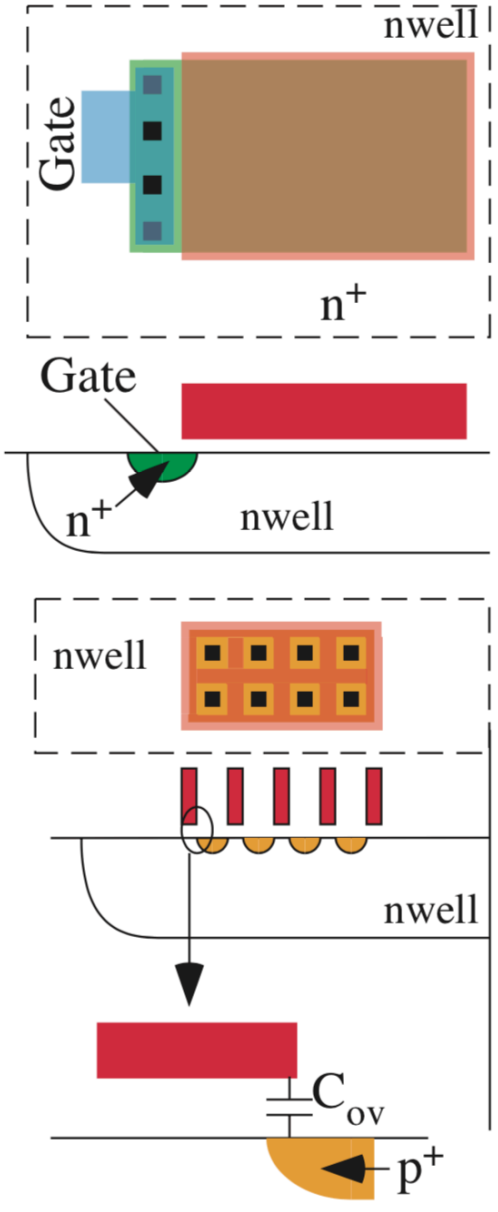
Floating-Gate Devices in Standard CMOS



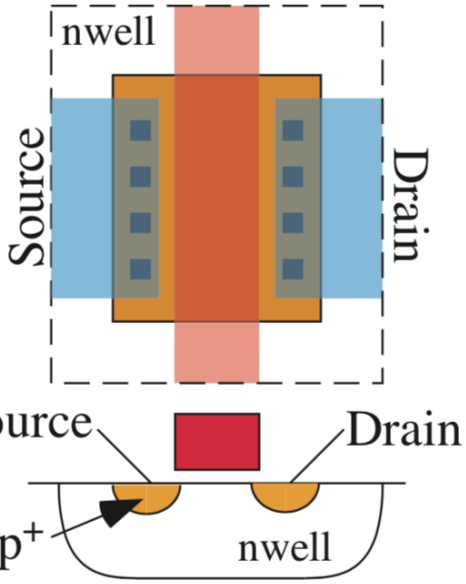
Floating Gate Circuit



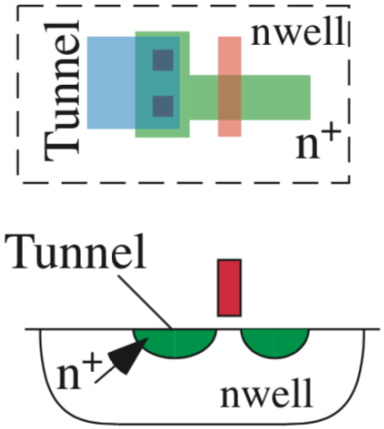
Capacitor Options

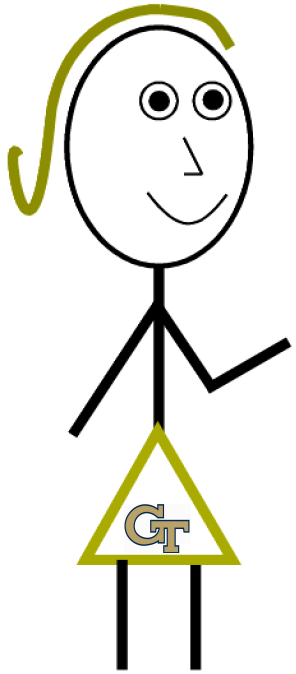


Thicker Insulator pFET



Tunneling Junction

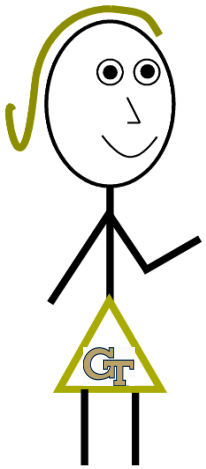




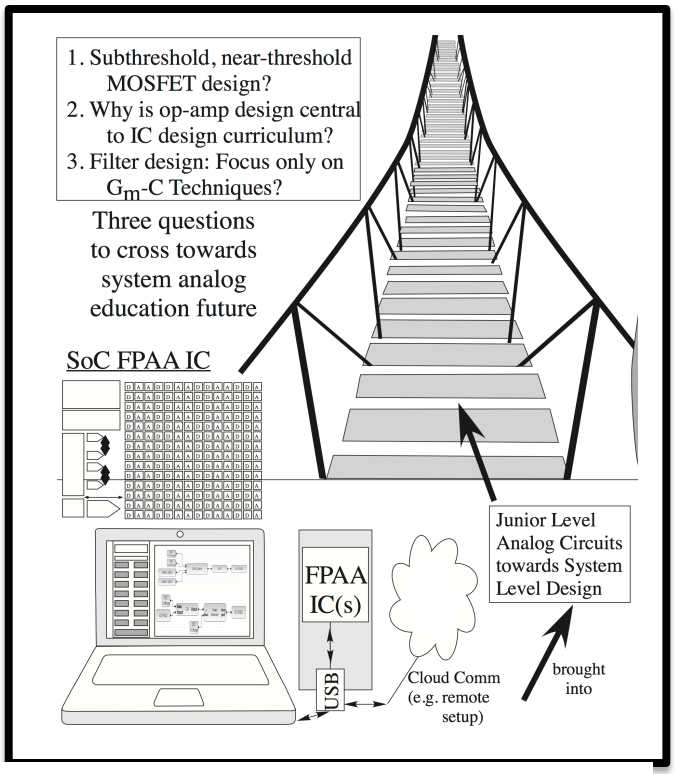
Without analog programmability, the challenge is huge

Floating-Gate Devices enables the opportunity

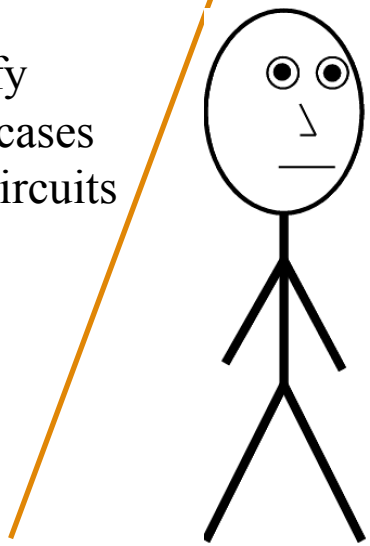
- Analog Programmability
- Standard CMOS

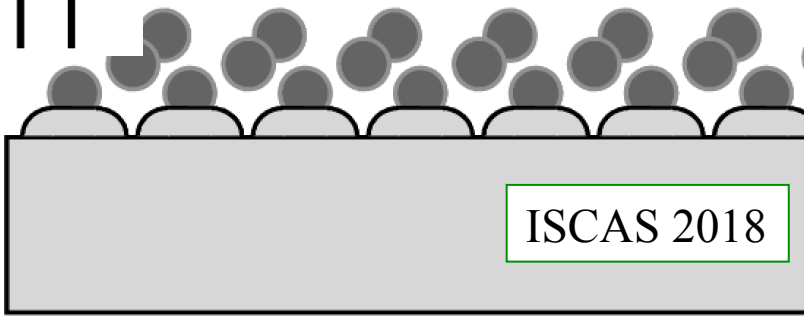


Yes.
For 25+ years
Almost every
CMOS process



No library could satisfy a small percentage of cases with all the different circuits & device sizes.



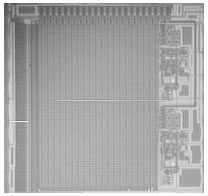


IC design transformed by programmability →

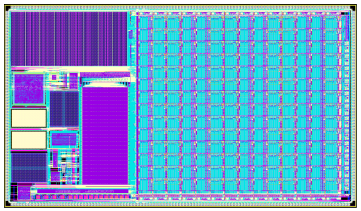
- Prog. FG biasing
- FG TA inputs
- GmC, SubV_T Design (**no bank of passives**)
- Configurable Design

20 years of FG-based FPAA innovation

RASP 1.5 (2001-2005)



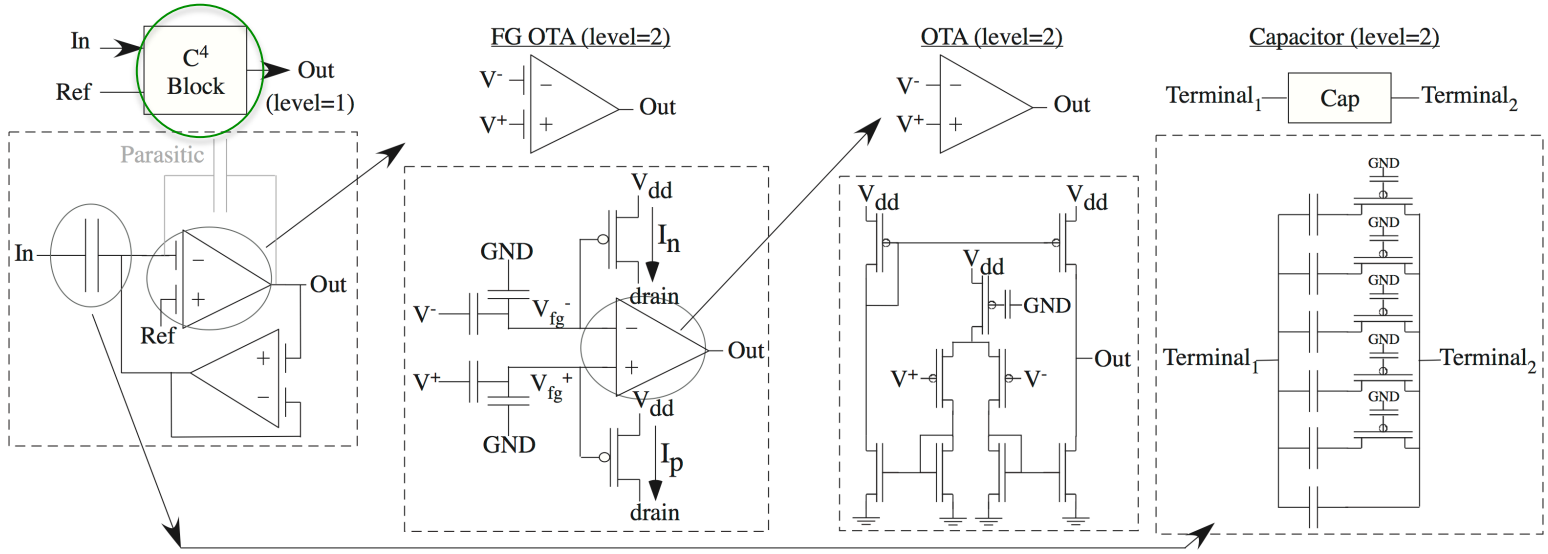
RASP 3.0 (2013-15)

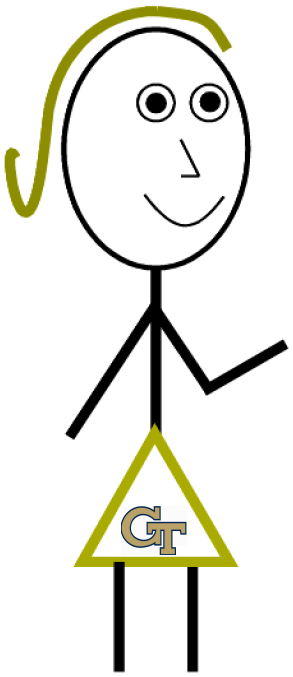


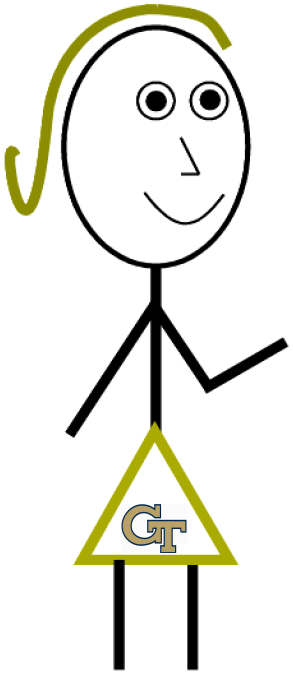
- Core blocks ~ converged
- Computing in routing (FG enabled)

Initial Standard Cells inspired from FPAA design exploration & successes

Abstraction in Analog Design from FPAA design







What IC process
to implement a
Std Cell Library?

350nm

40nm

65nm

Skywater
130nm

90nm

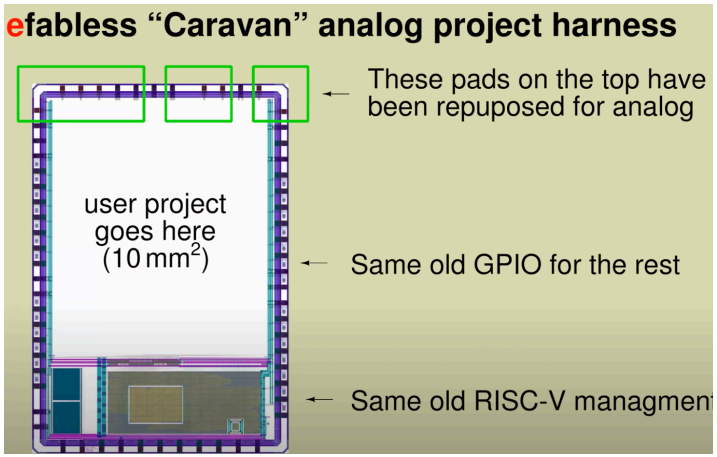
14nm

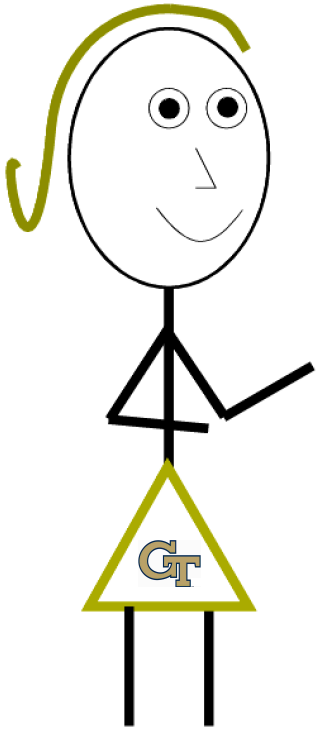
Open-Source
(design files,
tools)

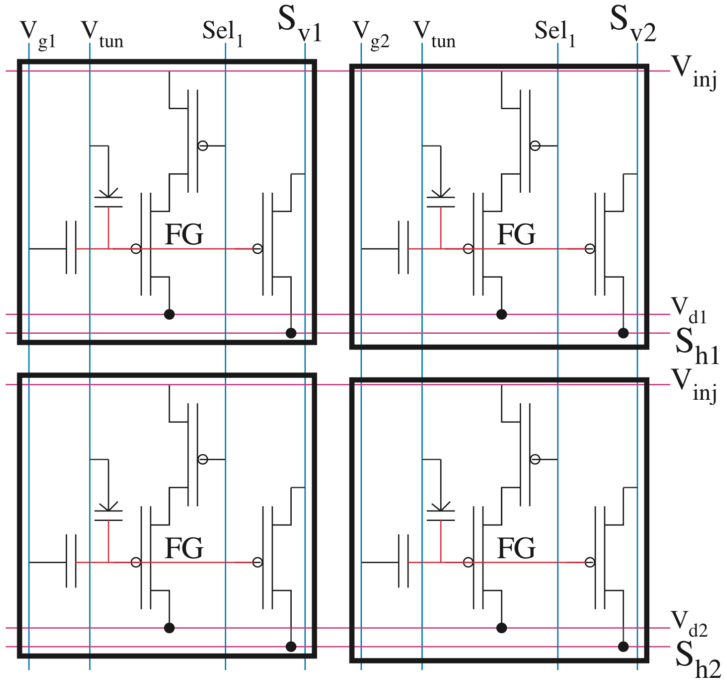
Enables wide use
of Std Cell Library

General Fabrication
Platform

(reminds me of
SoC FPAA structure)



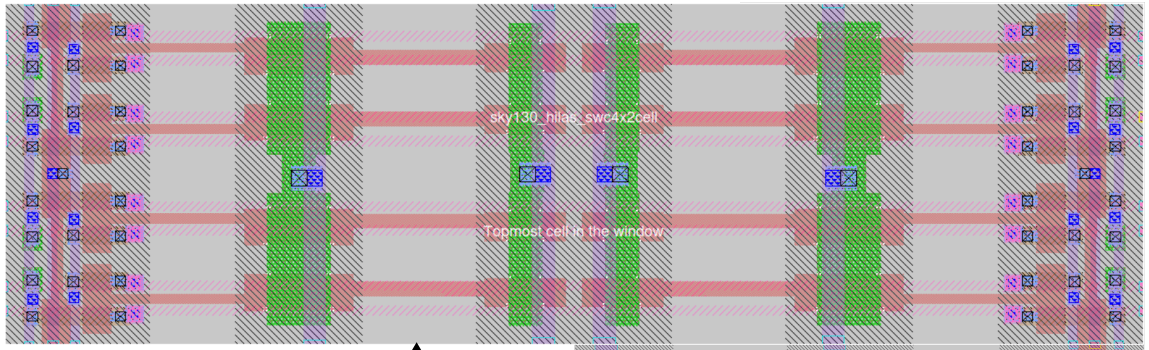




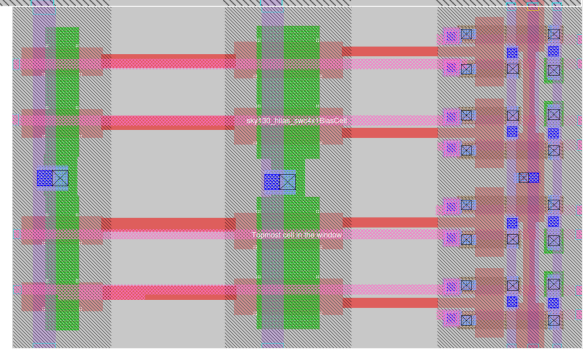
FG Crossbar Cells

~ Perfect isolation

- Indirect Programming
- supply lines in both directions
- Signal lines in both directions



swc4x2cell

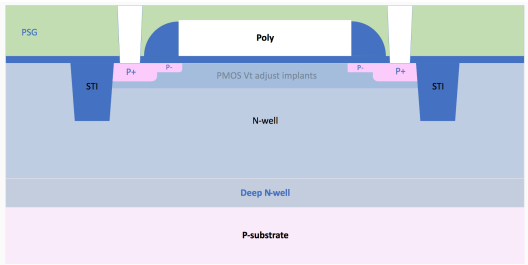


SWC4x1BiasCell

Well spacing for tunneling junction

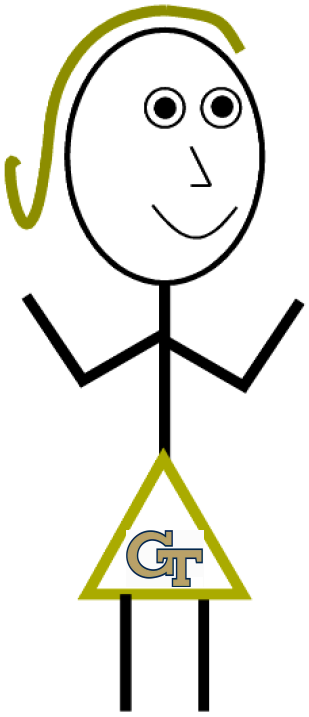
Skywater 130nm Device Details

5/10.5V NFET



(sky130_fd_pr__pfet_g5v0d10v5)

Thick Insulator for FG retention



Analog Std Cell Summary

Analog Cells:

Cell Type	Variations	Name	Width
Transconductance Amplifiers (TA)	2 TA, FG bias, no FG inputs	TA2Cell_NoFG	17.92μm
	2 TA, FG bias, FG inputs (V_L large)	TA2Cell_1FG	28.09μm
	2 TA, FG bias, FG inputs (V_L small)	TA2Cell_1FG_Strong	28.10μm
	2 TA, signal bias, no FG inputs	TA2SignalBiasCell	8.45μm
Capacitors	Selectable 16 unit cap	capacitorArray01	36.70μm
	Two separate unit caps	capacitorSize04	5.78μm
	2 unit cap	capacitorSize03	5.79μm
	4 unit cap	capacitorSize01	10.42μm
	8 unit cap	capacitorSize02	7.97μm
Winner-Take-All (WTA)	4 WTA stages	WTA4Stage01	14.07um
Ratioed Transistor DAC Modules	5 bit transistor module	DAC5bit01	16.58μm
Transmission Gates	4 Single Throw T-gates	Tgate4Single01	4.76μm
	4 Double Throw T-gates	Tgate4Double01	7.08μm
	4 T-gate for prog select (V_{inj})	drainSelect01	5.42μm
Transistors (nFET + pFET)	3 nFETs + 3 pFETs (W/L$\approx$1)	Trans4small	2.80 μm
	2 nFETs + 2 pFETs (W/L$\approx$10)	Trans2med	3.53μm
	1 nFETs (W/L$\approx$100)	nFETLarge	4.37μm
	1 pFETs (W/L$\approx$100)	pFETLarge	4.64μm

Pitch = 6.5µm

FG Cells:

Cell Type	Variations	Name	Width	V / O
Crossbar Cell (Same C_T)	4×2 Cell	swc4x2cell	20.12μm	V
		swc4x2cellOverlap	17.97μ	O
	4×1 Bias	swc4x1BiasCell	10.11μm	V
	4×1 cell	cellAttempt01	10.08μm	V
FG Gate cell (Same C_T)	2 x 1 FG Biases	FGBias2x1cell	11.53μm	V
	2 x1 FG Transistors	FGtrans2x1cell	11.52μm	V
FG Characterization cell	Tun, pFET (inj), Capacitors	FGcharacterization01	29.95μm	V+O

Varactor (V) and Overlap (O) capacitors

FG components

4x1 SWC

4x2 SWC

2x1 Transistor

2x2 Transistor

Many complex blocks with FG and non-FG components In the Island interface

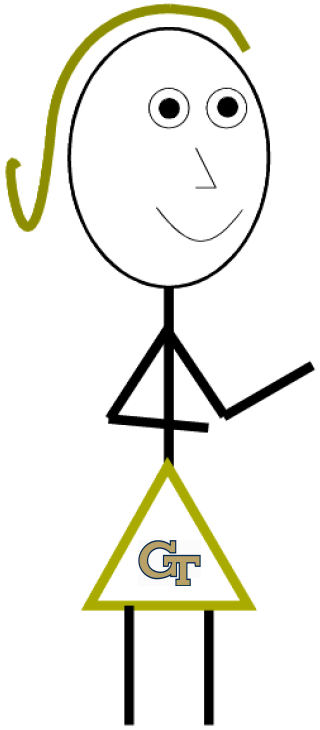
+ Block Parts

1 TA Term Part

2 TA Term Part

pFET Trans Pair Part

4 WTA Part



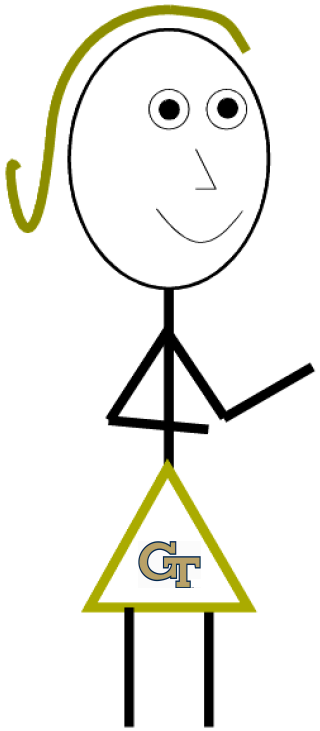
2 non-FG TA

2x1 Transistor | pFET Trans Pair Part | pFET Trans Pair Part | 2 TA Term Part → Output, Output

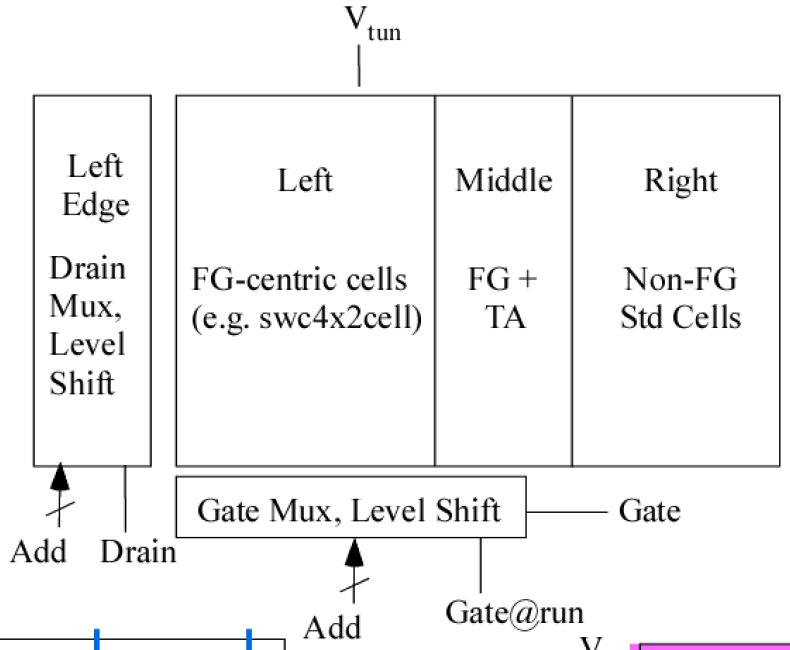
1 FG & 1 non-FG TA

2x2 Transistor | pFET Trans Pair Part | 2 TA Term Part → Output, Output

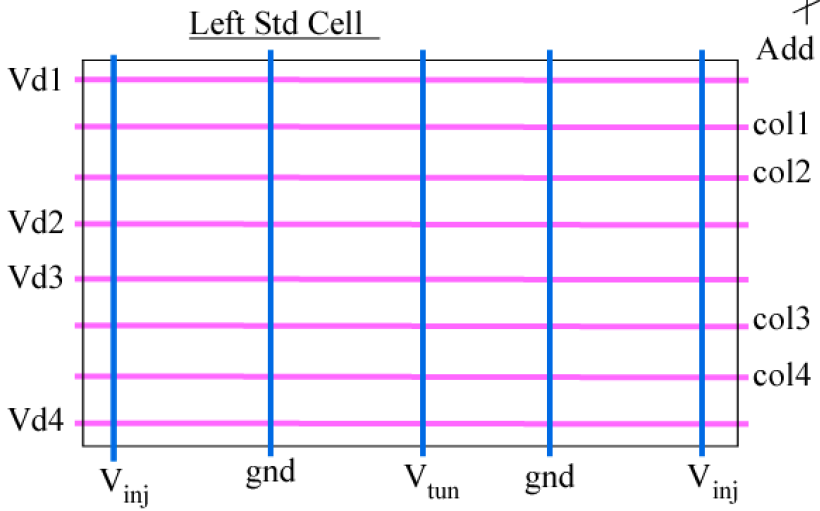
Multiple 4x2 SWC cells as input → 4x1 SWC | 4 WTA Part → 4 Output

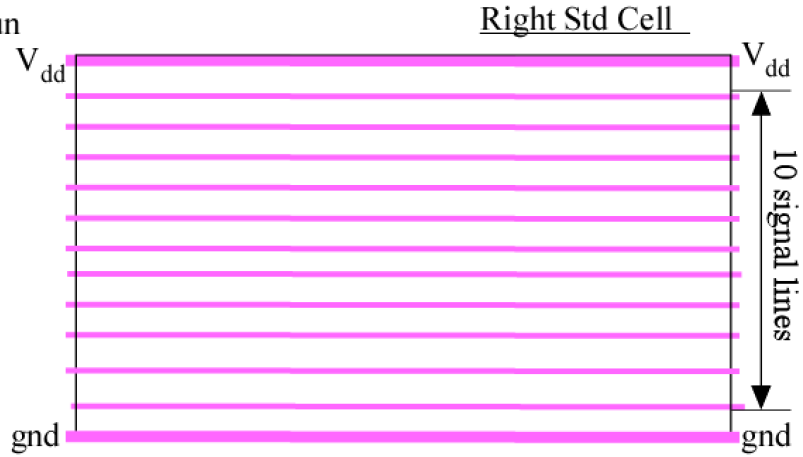


Std. Cell Island Approach



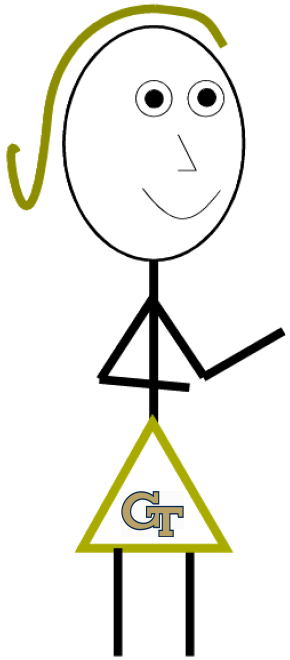
Approach for these elements, might be occasional exceptions





Middle has potentially both cases.

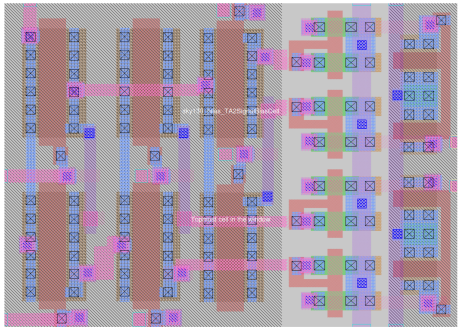
Programmable FG Cells requires different routing (vertical V_{tun}, V_{inj}, V_{dd})



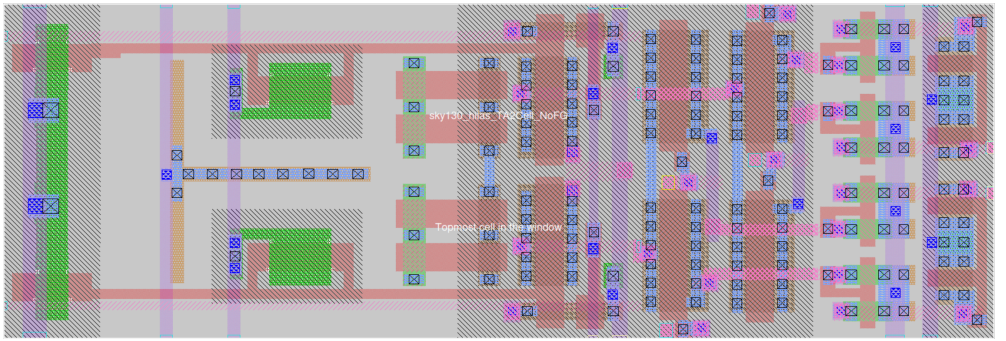
Transconductance Amplifiers (TA)

Pitch and Width Matched to swc4x2cell

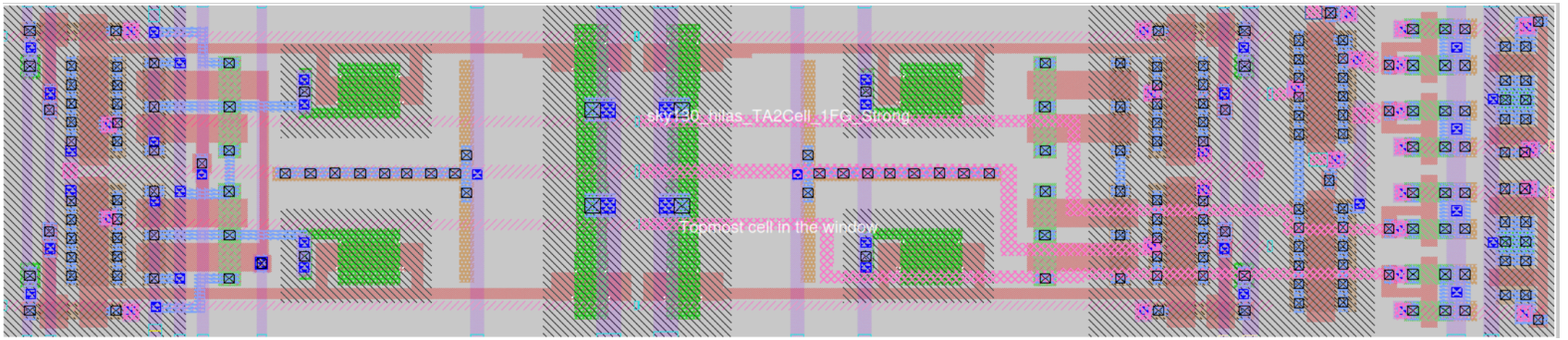
TA2SignalBiasCell



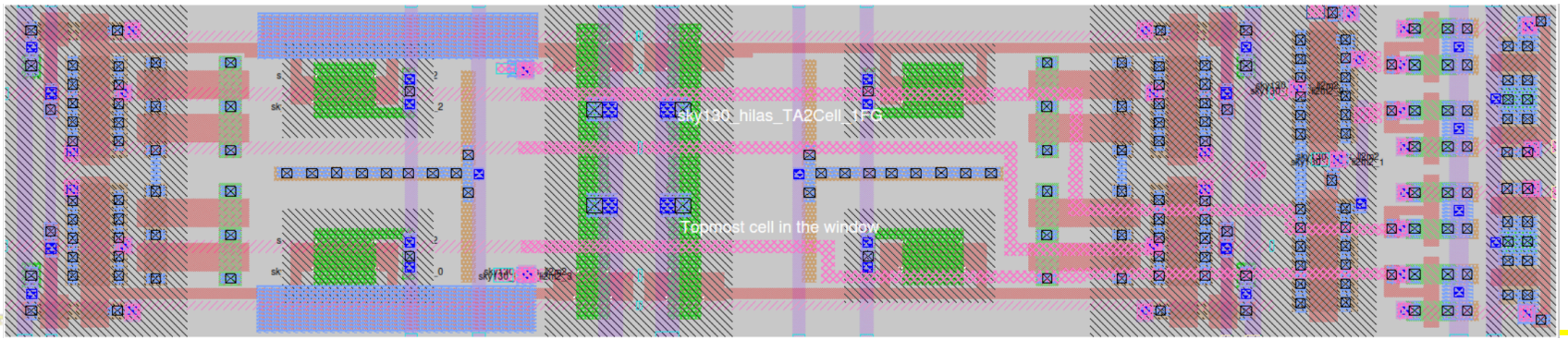
TA2Cell_NoFG



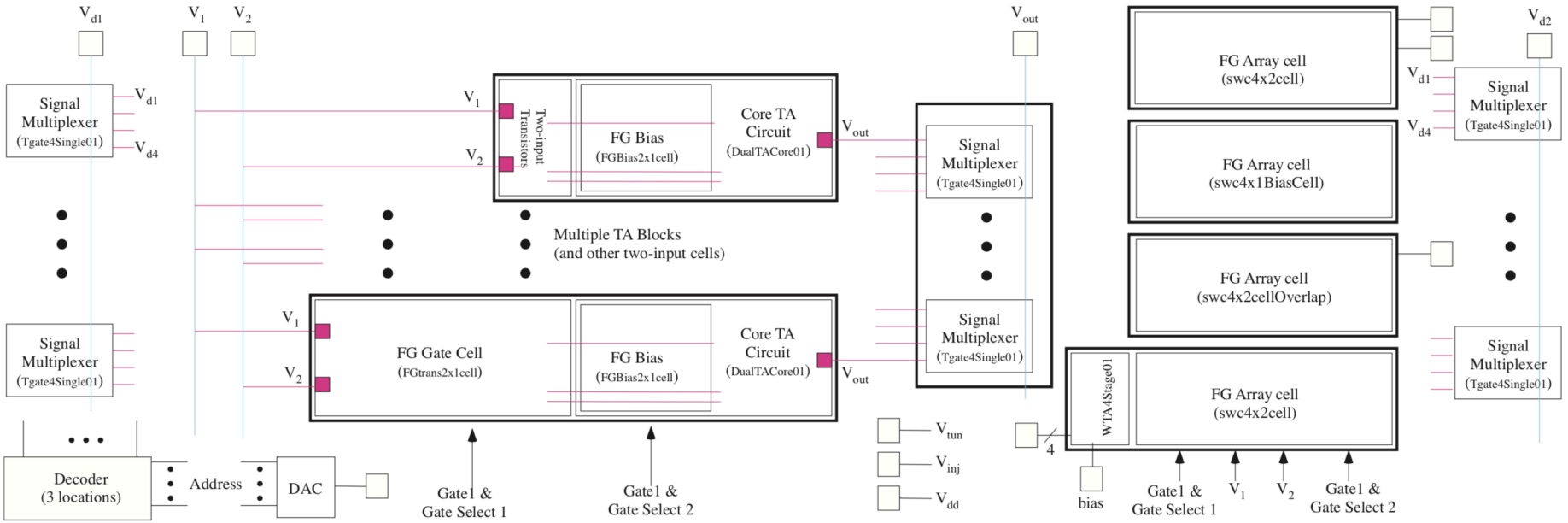
TA2Cell_1FG_Stror

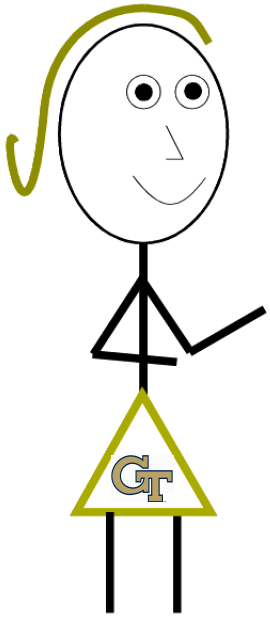


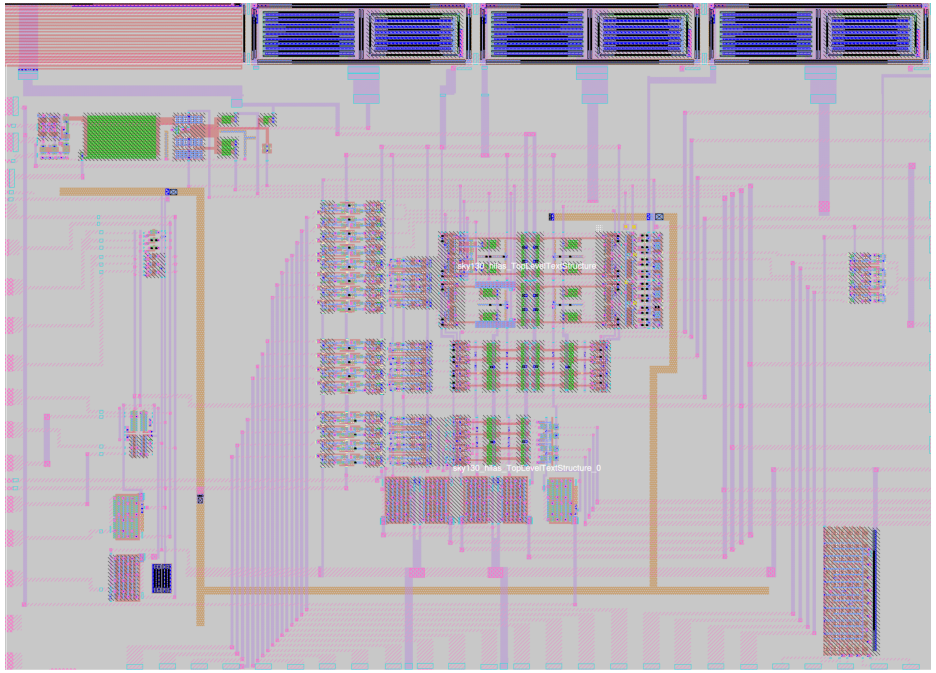
TA2Cell_1FG

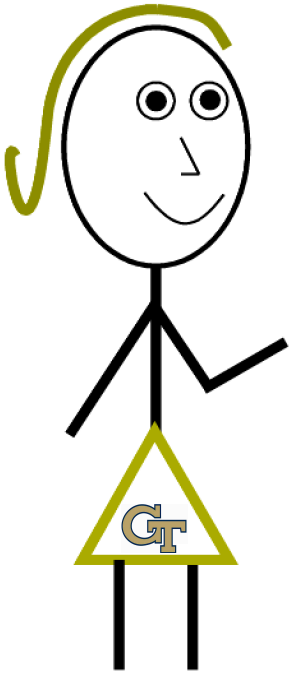


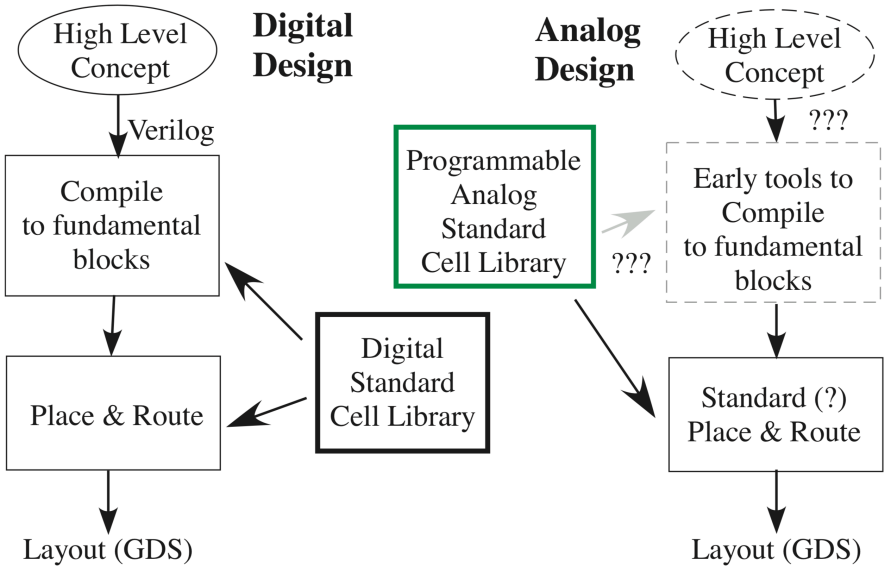
130nm Standard Cell Test Structure











First Analog Standard Cell library → a start of the library

Excited to see the experimental results of this library

Already expanding to a complete set:

- SSCS: a few additional variations (Nov run): direct & indirect FG structures
- Analog IC core elements (class development): More TA, Amplifiers, Comparitors, ADCs)

All open source in Skywater 130nm CMOS

The hope is that analog standard cells increases the impact of every Analog IC designer, and increases the awareness of their artistry.