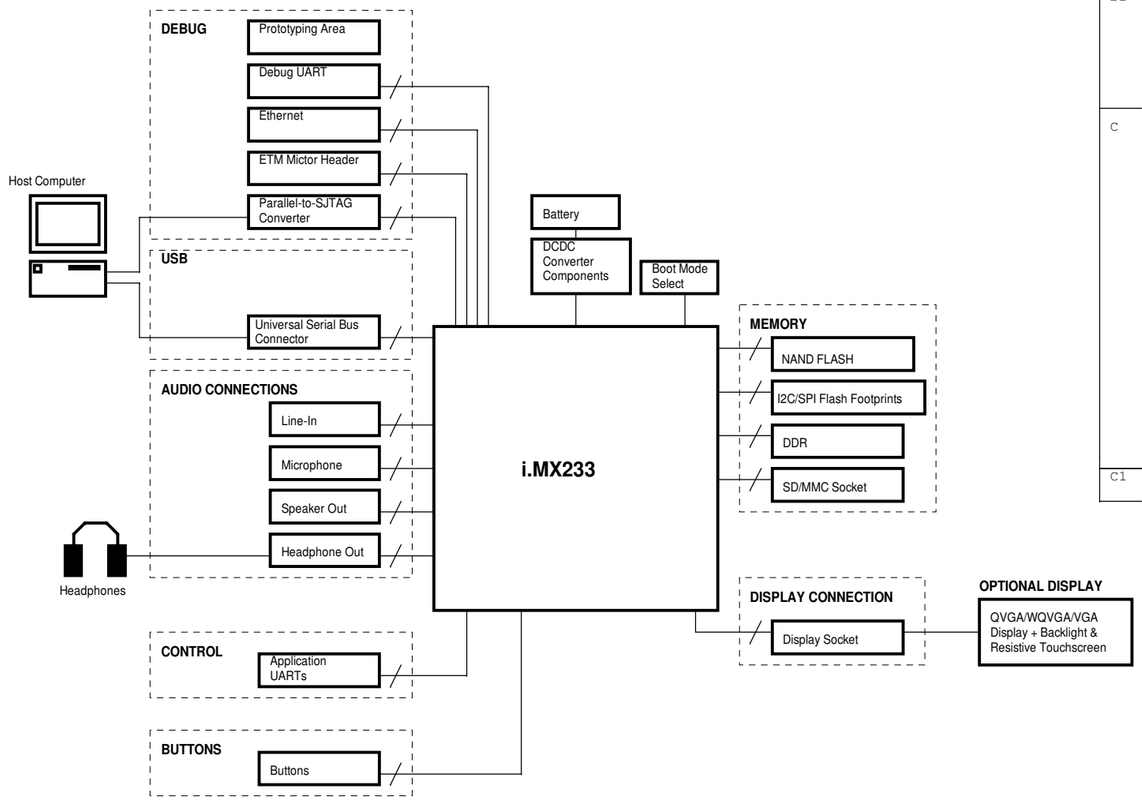
Table of Contents

2	Notes
3	i.MX233
4	AUDIO CONNECTIONS
5	SPI, I2C, & UART
6	DDR1
7	NAND
8	LCD
9	UI & SJTAG
10	USB & ETHERNET
11	JTAG
12	POWER SUPPLY

Block Diagram



Revisions

Rev	Description	Date	Approved
X1	Original Release	06/04/09	Mark Midddleton
A	Release to Production	06/10/09	Mark Midddleton
A1	Change U1 Part number to i.MX233	06/29/09	Mark Midddleton
B	Changed U16 to REG104 Removed SSP1 traces to LCD. Changed default NAND. Changed R183 to 10K. Added Pull Up to Ethernet CS. Modified UART Enable circuit. Added isolation jumpers to SSP1 traces to expansion port. Added USB 5V to External 5V jumper opt. Modified OTG Host power circuitry. Changed U48 to MMA7455L and POP. Switched I2C_SDA/SCL on J38.	08/05/09	Mark Midddleton
B1	Change U1 to ITC compliant part.	08/21/09	Mark Midddleton
B2	Modified UART Enable Circuit to DNP incorrect components. Populated Video Out circuit. Changed D20 to different Diode. Changed U13 to different LVT244 buffer. Populating EEPROM U49 by default.	10/26/09	Mark Midddleton
C	Modified UART Enable circuit. Enable signal now from VDDA. Added posts to DUART IC inputs. Added posts to CPLD SJTAG outputs. Reversed poles on Debug switch (S22). Added 4PDT switch to disconnect DUART circuit from i.MX233 chip. Removed Rotary A/B traces from DUART. Added Rotary A trace to USB_ID sense. Changed R185 to 10K. Populating USB Host circuit by default. Changed Q9, Q10 to lower cost FETs. Added 5V cutout circuit to reset button. Added alternate OE option for U13 to fix SPI NOR Flash boot conflict. Changed R93 to 10K. Changed netname on JTAG reset to show they are active low. Added LCD reset to J37.79. Change U45 NAND to single CE K9LBG08U0D	12/02/09	Mark Midddleton
C1	Corrected Off Board UART Enable signal to GND (S23.6).	12/02/09	Mark Midddleton

Designer: Mark Middleton	Drawing Title: i.MX233 EVK	
Drawn by: DRAWN_BY	Page Title: TITLE PAGE	
Approved: <Approver>	Size: Custom	Document Number: SOURCE:SCH-77066 PDF:SPF-77066 — Rev: C1
	Date: Monday, March 15, 2010	Sheet 1 of 12

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

USAGE GUIDE

TO ENTER BATTERY-POWERED MODE

Set HOLD SWITCH (S1) = OFF

Set BOOT MODE SELECT DIPSWITCH (S36) = 0100 to selects boot from NAND.

Set USB5V SWITCH (S14) = OFF

Set DEBUG SWITCH (S22) = OFF

Set BATTERY SOURCE SWITCH (S22) according to power source. If an actual battery or external power supply is used, it should be connected at J21 or J13 and the BATTERY SOURCE SWITCH should be set to BATTERY. If the internal regulators are used, an AC Adapter should be connected to the J6 power jack and the BATTERY SOURCE SWITCH should be set to REGULATOR.

Then press POWER BUTTON (S2) to power on the player.

TO ENTER USB / 5V POWERED MODE

Set HOLD SWITCH (S1) = OFF

Set BOOT MODE SELECT DIPSWITCH (S36) = 0100 to selects boot from NAND.

Set DEBUG SWITCH (S22) = OFF

Set BATTERY SOURCE SWITCH (S22) according to power source. If an actual battery or external power supply is used, it should be connected at J21 or J13 and the BATTERY SOURCE SWITCH should be set to BATTERY. If no battery power supply is available or needed in USB mode the BATTERY SOURCE SWITCH should be set to BATTERY. If the internal regulators are used, an AC Adapter should be connected to J6 and the BATTERY SOURCE SWITCH should be set to REGULATOR.

USB5V SWITCH (S14) = ON

Connect a USB cable to the J4 USB jack and the device should power on and enumerate.

TO ENTER RECOVERY MODE

METHOD 1:

With USB disconnected, set the BOOT MODE SELECT DIPSWITCH (S36) to 0000 (Boot from USB). Connect USB cable (or flip USB5V switch to ON). Once the EVK enumerates in Device Manager as Player Recovery Device, set the BOOT MODE SELECT DIPSWITCH (S36) back to 0100.

METHOD 2:

Ensure DEBUG SWITCH (S22) is set to OFF. With USB disconnected, press and hold the RECOVERY BUTTON (S25), and then connect USB cable (or flip USB5V switch to ON). Continue to hold the RECOVERY BUTTON for 5 seconds or until the Player Recovery Device appears in the Device Manager.

TO ENTER DEBUG MODE

Set HOLD SWITCH (S1) = OFF

Set BOOT MODE SELECT DIPSWITCH (S36) = 0100 to selects boot from NAND.

Set USB5V SWITCH (S14) depending on which mode you wish to debug.

Connect the Slingshot JTAG cable to the J2 JTAG Port.

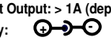
Set BATTERY SOURCE SWITCH (S22) according to power source. If an actual battery or external power supply is used, it should be connected at J21 or J13 and the BATTERY SOURCE SWITCH should be set to BATTERY. If the internal regulators are used, an AC Adapter should be connected to J6 and the BATTERY SOURCE SWITCH should be set to REGULATOR.

Set DEBUG SWITCH (S22) = ON

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC

Current Output: > 1A (depending on application)

Polarity: 

Inner Diameter: 2.1mm

Outer Diameter: 5.5mm

SWITCH OPERATION

BATTERY SOURCE SWITCH (S12)

BATTERY:

Allows the board to be powered from either the J21 header or the J13 connector. Note that J21 and J13 are wire in parallel, so power should only be applied to one of the two inputs at any time. Allowable input voltage ranges:
3.0V to 4.2V (nominal 3.7V)

REGULATOR:

Uses the onboard regulator as the power source for the DC-DC converters. The regulators are adjustable through external resistors or a potentiometer, but the default value is 4.20V

USB5V SWITCH (S14)

ON:

Connects USB5V to the VDD5V pin on the i.MX233. If a USB cable is attached, this should allow the device to power up and enumerate.

OFF:

Disconnects USB5V from the EVK. Can be used to force a USB disconnect and re-enumeration without unplugging the USB cable.

DEBUG SWITCH (S22)

ON:

Allows use of the Serial JTAG port for development or debug.

OFF:

Normal (non-debug) operation.

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Drawing Title: **i.MX233 EVK**

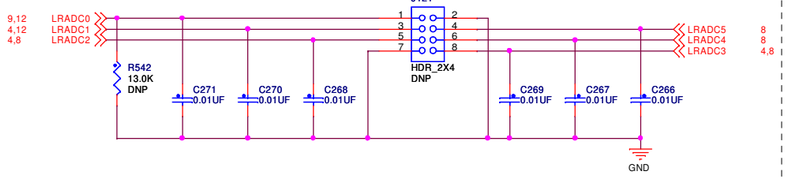
Page Title: **NOTES**

Size	Document Number	Rev
C	SCH-77066 PDF: SPF-77066	C1

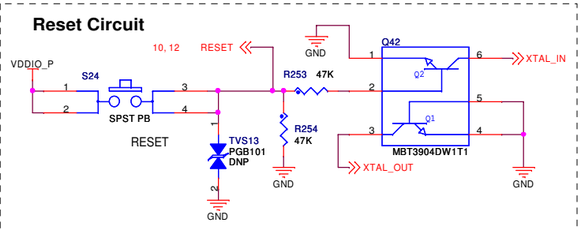
Date: Monday, March 15, 2010 Sheet 2 of 12

i.MX233 169-Pin BGA

Resistive Touchscreens Capacitors

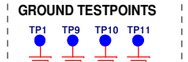


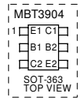
Reset Circuit



POWER TESTPOINTS

GROUND TESTPOINTS





NOTE: The VAG capacitor ground must route to star ground at VSSA2.

Note: Route SHORTING TRACE for R577 between pads on same layer as pads.

Note: Route SHORTING TRACE for R571, R572, R573, and R574 between pads on same layer as pads.

The i.MX233 should use low-ESR (~300mOhms) tantalums or ceramics for both the VDD4P2 and the LI-ION BATTERY supplies to prevent a battery charger oscillation issue.

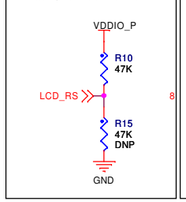
C1, C8, C50 should be a low-ESR tantalum or ceramic (<400mOhms) to reduce power supply noise. Ceramic capacitors are recommended. Do not use Y5R.

IMPORTANT: Place C150, C70, and C31 very close to DCDC_BATT Pin

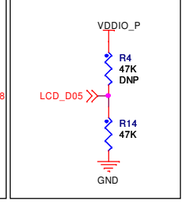
i.MX233 BOOT MODE SELECT

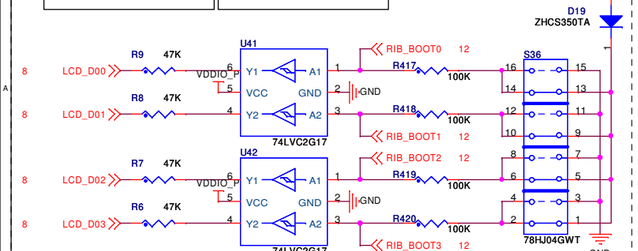
	LCD DATA			
BOOT MODE	**03**	**02**	**01**	**00**
USB	0	0	0	0
3.3V I2C Master	0	0	0	1
3.3V SPI Flash 1 Master	0	0	1	0
3.3V NAND	0	1	0	0
DEBUG	0	1	1	0
3.3V SD/MMC 1	1	0	0	1

LCD_RS needs to be pulled HIGH to enable Resistor Boot Mode. If LCD_RS is pulled low, the i.MX233 will attempt to boot from OTP.



LCD_D05 = ETM Enable Bit:
Low = ETM disabled
High = ETM enabled





IMPORTANT CRYSTAL DESIGN NOTES

The 24 MHz crystal should be located close to the i.MX233. Consult crystal manufacturer datasheet for recommended load capacitor values (typically 10-18pF).

Cload = [(C26*C27) / (C26+C27)] + Cstray

where Cstray = stray PCB capacitance, typically 4 - 6 pF

Note: For Microsoft DRM applications use a 30 ppm crystal.

i.MX233
169-BGA

U1 i.MX233

9,12 LRADC0	A8	LRADC0/BUTTON1/TEMP/MICBIAS	
4,12 LRADC1	B9	LRADC1/BUTTON2/TEMP/MICBIAS	
4,8 LRADC2	C9	LRADC2/TOUCHSCREEN0	
4,8 LRADC3	D9	LRADC3/TOUCHSCREEN1	
8 LRADC4	A10	LRADC4/TOUCHSCREEN2	
8 LRADC5	B10	LRADC5/TOUCHSCREEN3	
LI-ION_BATTERY	A11	BATT	
	C7	VDDA1	
	C2	VDDXTAL	
	C8, A2, D4	VSSA1, VSSA2, VSSA5	
	B4	RTC_XTALI	
	C4	RTC_XTALO	
	A4	XTALI	
	A5	XTALO	
9 PSWITCH	B3	PSWITCH	
	E13	VDD5V	
10 USB_D+	A1	USB_DP	
10 USB_D-	B2	USB_DM	
VDDS	B1	VDDS	
4 SPKR+	C1	SPEAKERP	
4 SPKR-	D1	SPEAKERN	
VAG	A3	VAG	
4 HP_OUT_R	B8	HPR	
4 HP_OUT_L	B7	HPL	
4 HP_VGND	A7	HP_VGND	
4 LINE1_INR	A6	LINE1_INR	
4 LINE1_INL	B5	LINE1_INL	
4 MIC	B6	MIC	
4 VDAC1	C11	VDAC1	
9 SERIAL_JTAG	E12	DEBUG	
5 UART1_RX	H8	AUART1_RX	
5 UART1_TX	J8	AUART1_TX	
5 UART1_CTS	G7	AUART1_CTS	
5 UART1_RTS	H7	AUART1_RTS	
	B11	DCDC_BATTERY	
	A9	VDD4P2	
	A13	DCDC_GND	
	B13	DCDC_LN1	
	A12	DCDC_LP	
	C13	DCDC_VDDIO	
	D13	DCDC_VDDD	
	B12	DCDC_VDDA	
	C10	VDDM	
	L6	VDDIO_EMIO	
	L8	VDDIO_EMI1	
	L10	VDDIO_EMI2	
	E11	VDDIO33_1	
	G3	VDDIO33_3	
	D5	VDDD1	
	D8	VDDD3	
	E9	VSSD1	
	J7	VSSD5	
	J9	VSSIO_EMI1	
	L7	VSSIO_EMI2	
	K10	EMI_D00	
	M10	EMI_D01	
	N10	EMI_D02	
	M11	EMI_D03	
	K9	EMI_D04	
	L11	EMI_D05	
	L9	EMI_D06	
	N9	EMI_D07	
	N8	EMI_D08	
	M8	EMI_D09	
	K7	EMI_D10	
	L7	EMI_D11	
	K6	EMI_D12	
	N7	EMI_D13	
	M7	EMI_D14	
	K13	EMI_D15	
	K12	EMI_A00	
	J13	EMI_A01	
	K11	EMI_A02	
	G10	EMI_A03	
	G12	EMI_A04	
	F12	EMI_A05	
	G11	EMI_A06	
	F13	EMI_A07	
	J12	EMI_A08	
	H10	EMI_A09	
	H13	EMI_A10	
	J10	EMI_A11	
	H12	EMI_A12	
	M12	EMI_CE0	
	M9	EMI_CE1	
	N12	EMI_DQM0	
	K8	EMI_DQM1	
	M6	EMI_DQS0	
	L13	EMI_DQS1	
	L12	EMI_CLK	
	N13	EMI_BA0	
	M13	EMI_BA1	
	L11	EMI_RAS	
	F11	EMI_CAS	
	D7	EMI_WE	
	E8	EMI_CKE	
	C5	ROTARYA	
	C6	ROTARYB	
	H6	I2C_SCL	
	H5	I2C_SDA	
	K2	GPMI_D00	7
	L1	GPMI_D01	7
	L2	GPMI_D02	7
	L3	GPMI_D03	7
	L5	GPMI_D04	7
	L4	GPMI_D05	7
	M2	GPMI_D06	7
	M1	GPMI_D07	7
	M3	GPMI_D08	5,8
	M4	GPMI_D09	5,8
	M5	GPMI_D10	5,8
	N1	GPMI_D11	5,8
	N2	GPMI_D12	8
	N3	GPMI_D13	8
	N4	GPMI_D14	5,9
	N5	GPMI_D15	5,9
	G8	GPMI_CE0	7
	F8	GPMI_CE1	7
	K5	GPMI_CE2	7,10
	G6	GPMI_RDY0	7
	J6	GPMI_RDY1	7
	F6	GPMI_RDY2	7
	E6	GPMI_RDY3	7
	E7	GPMI_WR	7
	H6	GPMI_RD	7
	F7	GPMI_WP	7
	K3	GPMI_CLE	7
	K4	GPMI_ALE	7
SSP1_DATA0/SPI_MISO	G9	SSP1_DATA0:SPI1_MISO	5,8,10
SSP1_DATA1	F9	SSP1_DATA1	5,10
SSP1_DATA2	F10	SSP1_DATA2	5,10
SSP1_DATA3/SPI_SS0	E10	SSP1_DATA3:SPI1_SS#	5,8,10
SSP1_CMD/SPI_MOSI	H9	SSP1_CMD:SPI1_MOSI	5,8,10
SSP1_SCK	D12	SSP1_SCK:SPI1_SCK	5,8,10
SSP1_DETECT	D10	SSP1_DETECT	5,10
LCD_D00	D3	LCD_D00	8
LCD_D01	E2	LCD_D01	8
LCD_D02	E4	LCD_D02	8
LCD_D03	F1	LCD_D03	8
LCD_D04	F3	LCD_D04	8
LCD_D05	F5	LCD_D05	8
LCD_D06	G2	LCD_D06	8
LCD_D07	G5	LCD_D07	8
LCD_D08	H2	LCD_D08	5,8
LCD_D09	H3	LCD_D09	5,8
LCD_D10	H1	LCD_D10	5,8
LCD_D11	G4	LCD_D11	5,8
LCD_D12	G1	LCD_D12	8
LCD_D13	F4	LCD_D13	8
LCD_D14	F2	LCD_D14	8
LCD_D15	E5	LCD_D15	8
LCD_D16	E3	LCD_D16	8
LCD_D17	E1	LCD_D17	8
LCD_CS	H4	LCD_CS	8
LCD_RS/LCD_CCIRCLK	J3	LCD_RS	8
LCD_RESET	J5	LCD_RESET	8
LCD_WR	J4	LCD_WR	8
LCD_ENABLE	H5	LCD_EN	8
LCD_HSYNC	J2	LCD_HSYNC	8
LCD_VSYNC	J1	LCD_BUSY:LCD_VSYNC	8
LCD_DOTCK	K1	LCD_DOTCLK	8
PWM0	C3	PWM0	5,9
PWM1	D2	PWM1	5,9
PWM2	H11	PWM2	5,8
PWM3	D11	PWM3	5,8
PWM4	C12	PWM4	5,8
I2C_SDA	C5	I2C_SDA	5,8,9,12
I2C_SCL	C6	I2C_SCL	5,8,9,12
ROTARYB	C5	ROTARYB	5,6,7
ROTARYA	C6	ROTARYA	5,10
EMI_CKE	E8	EMI_CKE	6
EMI_WEn	D7	EMI_WEn	6
EMI_CASn	F11	EMI_CASn	6
EMI_RASn	L11	EMI_RASn	6
EMI_BA1	M13	EMI_BA1	6
EMI_BA0	N13	EMI_BA0	6
EMI_CLKN	L12	EMI_CLKN	6
EMI_CLK	L13	EMI_CLK	6
EMI_DQS1	M6	EMI_DQS1	6
EMI_DQS0	N12	EMI_DQS0	6
EMI_DQM1	K8	EMI_DQM1	6
EMI_DQM0	M9	EMI_DQM0	6
EMI_CE1n	M12	EMI_CE1n	6
EMI_CE0n	J10	EMI_CE0n	6
EMI_A12	H12	EMI_A12	6
EMI_A11	J10	EMI_A11	6
EMI_A10	H13	EMI_A10	6
EMI_A09	H10	EMI_A09	6
EMI_A08	J12	EMI_A08	6
EMI_A07	F13	EMI_A07	6
EMI_A06	G11	EMI_A06	6
EMI_A05	F12	EMI_A05	6
EMI_A04	G12	EMI_A04	6
EMI_A03	G10	EMI_A03	6
EMI_A02	K11	EMI_A02	6
EMI_A01	J13	EMI_A01	6
EMI_A00	K12	EMI_A00	6

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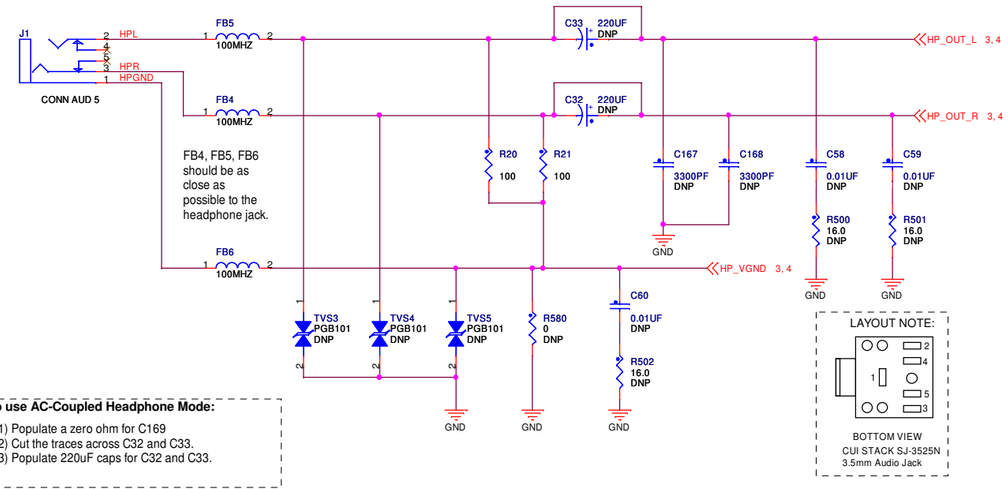
Drawing Title:	i.MX233 EVK		
Page Title:	i.MX233		
Size: C	Document Number: SCH-77066 PDF: SPF-77066		Rev: C1
Date: Monday, March 15, 2010	Sheet 3 of 12		

Headphone

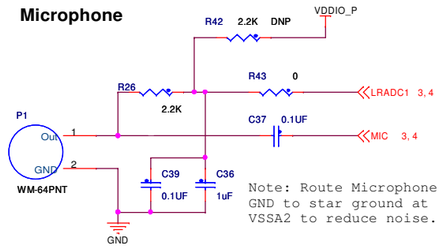
Note: Route SHORTING TRACE for C32 and C33 between pads on same layer as pads.



To use AC-Coupled Headphone Mode:

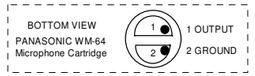
1) Populate a zero ohm for C169
2) Cut the traces across C32 and C33.
3) Populate 220uF caps for C32 and C33.

Microphone

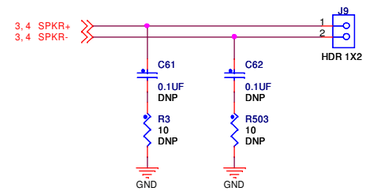


Note: Route Microphone GND to star ground at VSSA2 to reduce noise.

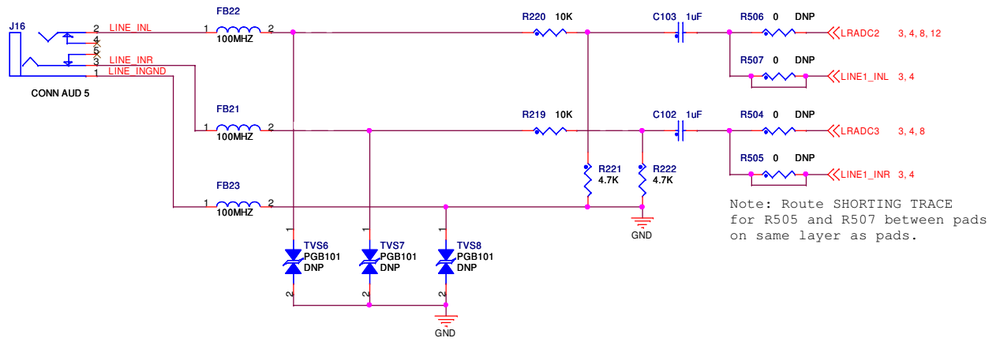
The microphone is configured for LRADC1 bias by default. If LRADC1 is not available, VDDIO bias can be used by cutting the trace between R43 pads and populating R42.



External Speaker

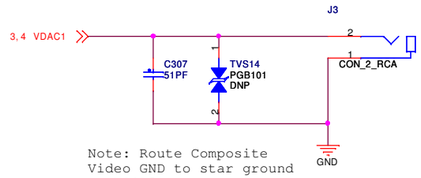


Line-In Circuit



Note: Route SHORTING TRACE for R505 and R507 between pads on same layer as pads.

Optional Composite Video



Note: Route Composite Video GND to star ground at VSSA2.

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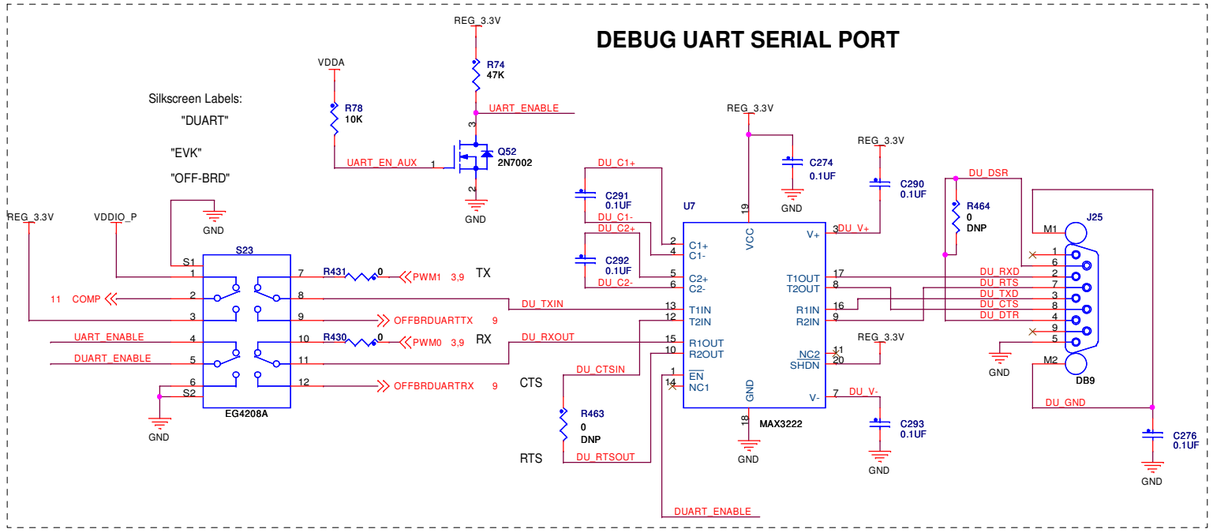
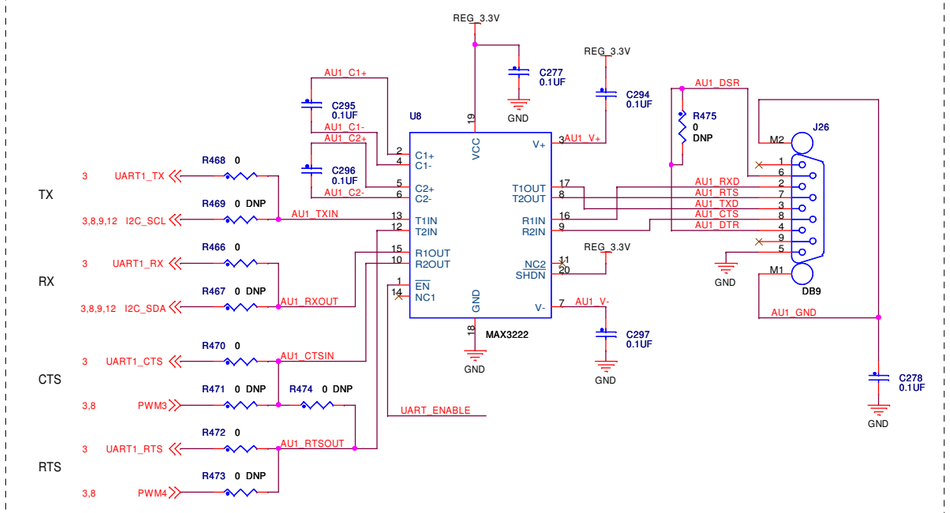
Drawing Title:	i.MX233 EVK
Page Title:	AUDIO CONNECTIONS
Size: C	Document Number: SCH-77066 PDF: SPF-77066 Rev: C1
Date: Monday, March 15, 2010	Sheet 4 of 12

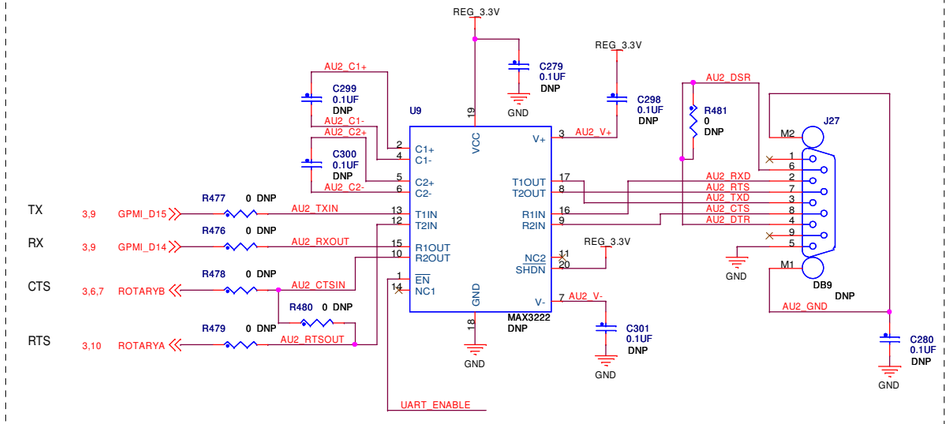
DEBUG UART SERIAL PORT



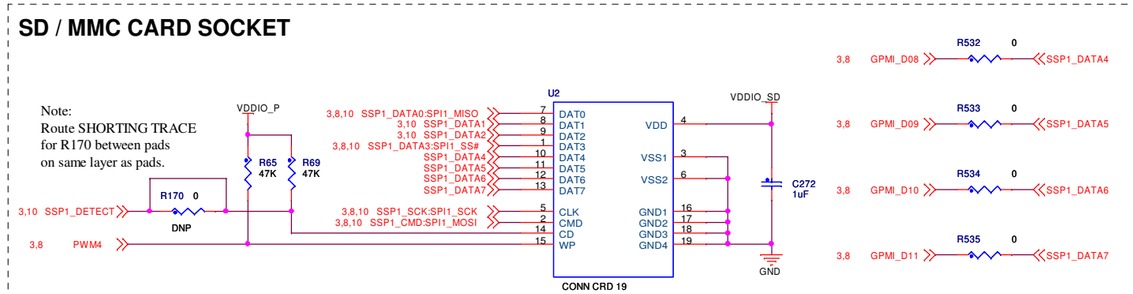
APPLICATION UART1 SERIAL PORT



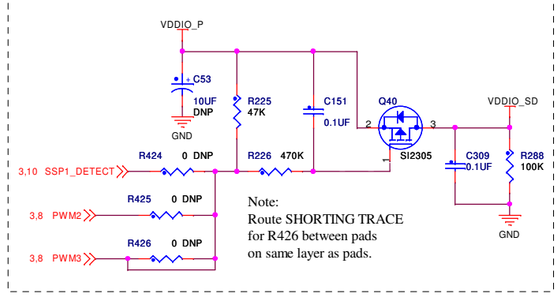
OPTIONAL APPLICATION UART2 SERIAL PORT



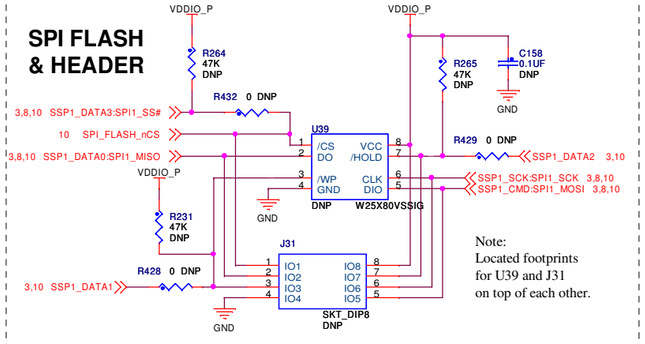
SD / MMC CARD SOCKET



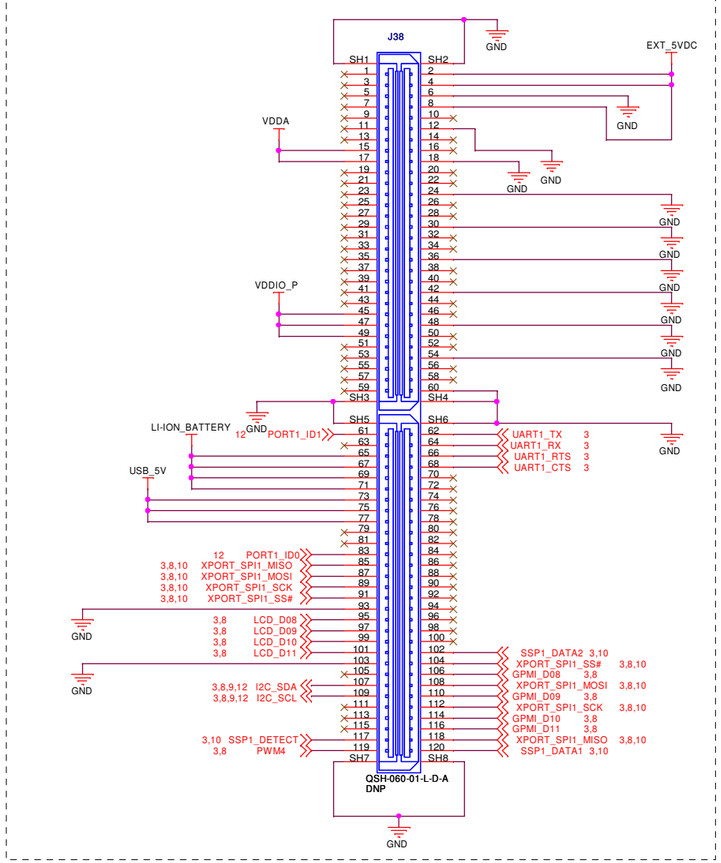
SD / MMC POWER CONTROL



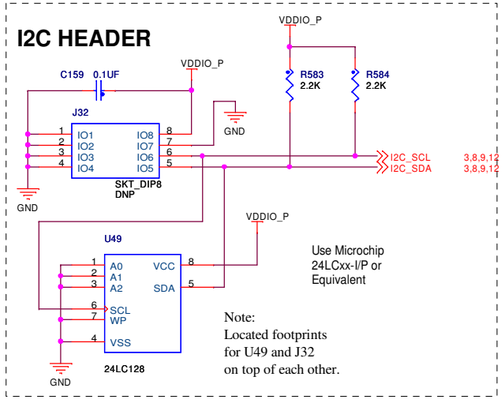
SPI FLASH & HEADER

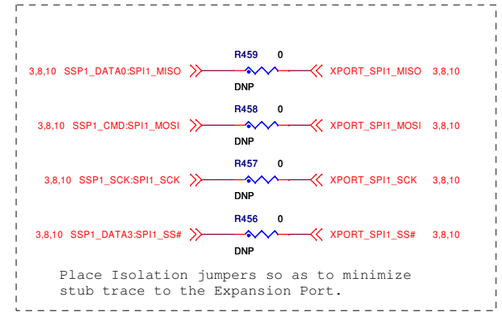


EXPANSION PORT



I2C HEADER





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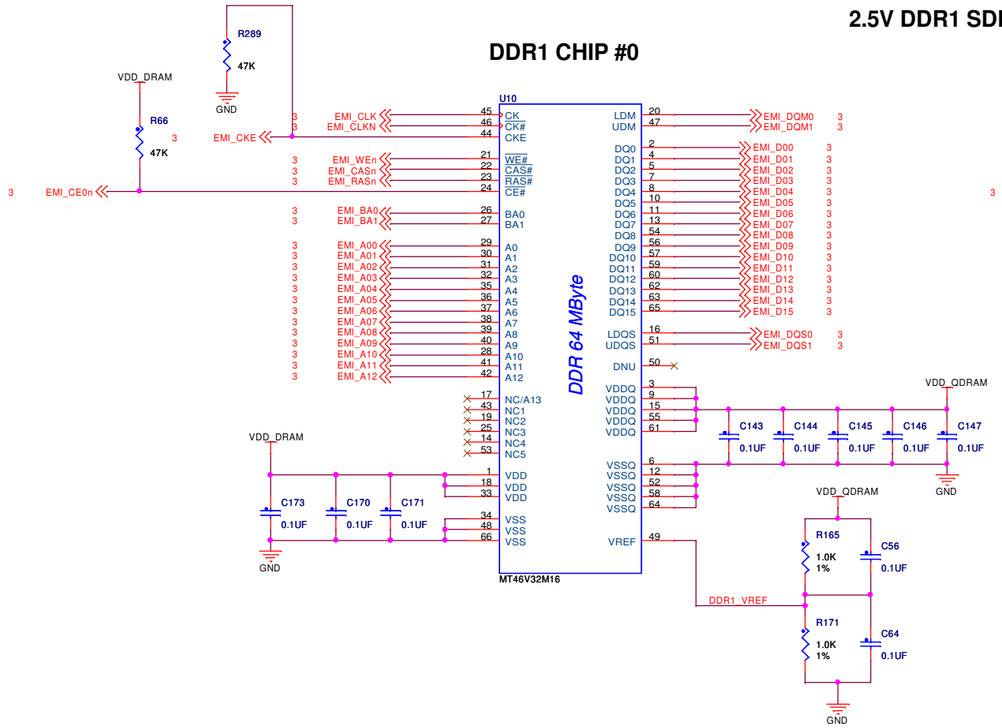
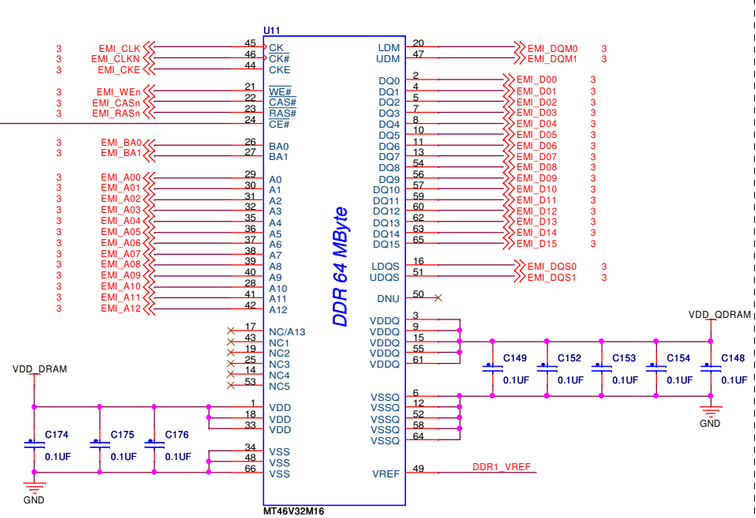
ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	i.MX233 EVK		
Page Title:	SPI, I2C, &UART		
Size: Custom	Document Number: SCH-77066 PDF: SPF-77066		Rev: C1
Date: Monday, March 15, 2010	Sheet 5 of 12		

2.5V DDR1 SDRAM

DDR1 CHIP #0



DDR1 CHIP #1



2.5V Power Connection

Note:
Route SHORTING TRACE for R385 and R386 between pads on same layer as pads.

Note:
To remove power to DDR DRAM signal functions (leavind DRAM in static power state), populate Q41, R227 and R581, and cut trace across R386. This will power down signal functions when VDDIO is powered down.

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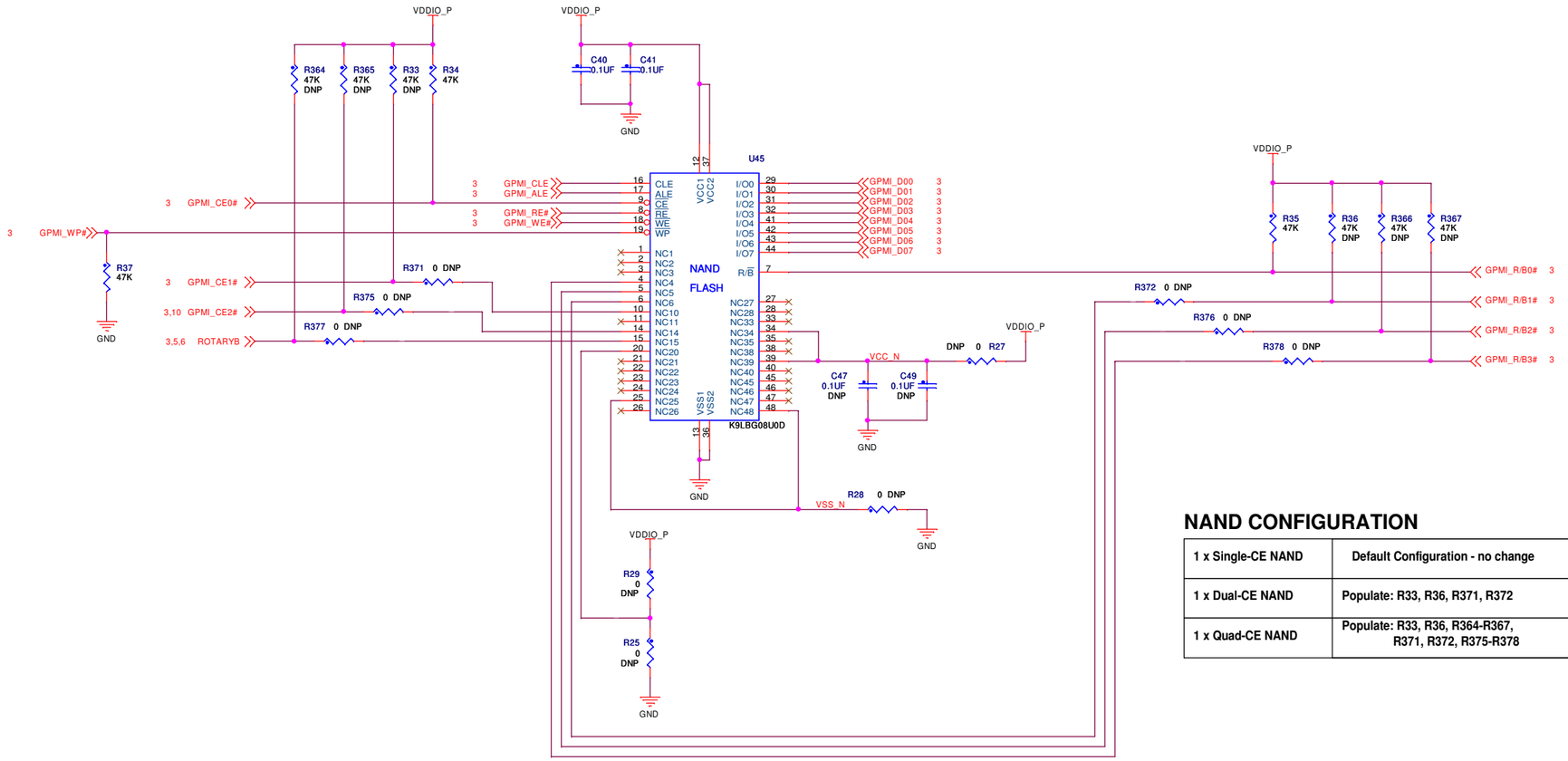
ICAP Classification:	FCP: ___ FIUO: X	PUBI: ___
Drawing Title:	i.MX233 EVK	
Page Title:	DDR1	
Size C	Document Number SCH-77066 PDF: SPF-77066	Rev C1
Date: Monday, March 15, 2010	Sheet 6 of 12	

8-BIT NAND FLASH

NOTE: To support ONFI standard NAND Flash, populate R27,R28, C47, C49.
Depending on the NAND, it may also be necessary to populate either R29 or R25.



NAND CONFIGURATION

1 x Single-CE NAND	Default Configuration - no change
1 x Dual-CE NAND	Populate: R33, R36, R371, R372
1 x Quad-CE NAND	Populate: R33, R36, R364-R367, R371, R372, R375-R378

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

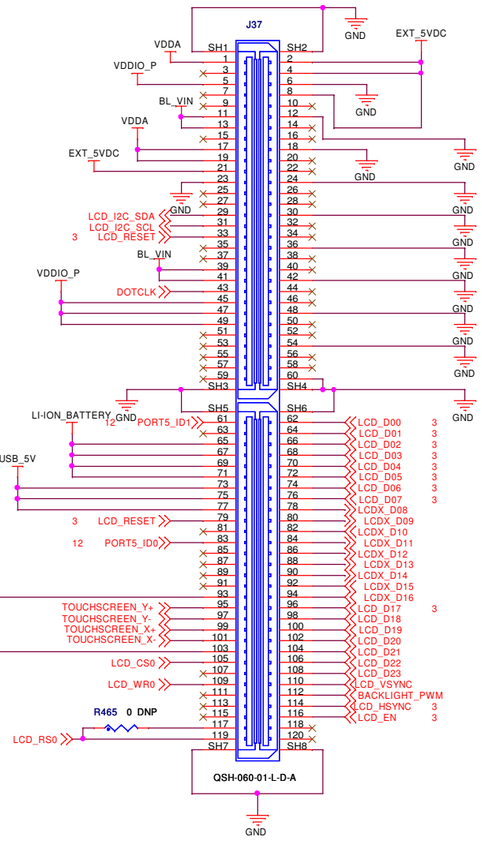
Drawing Title: i.MX233 EVK

Page Title: NAND

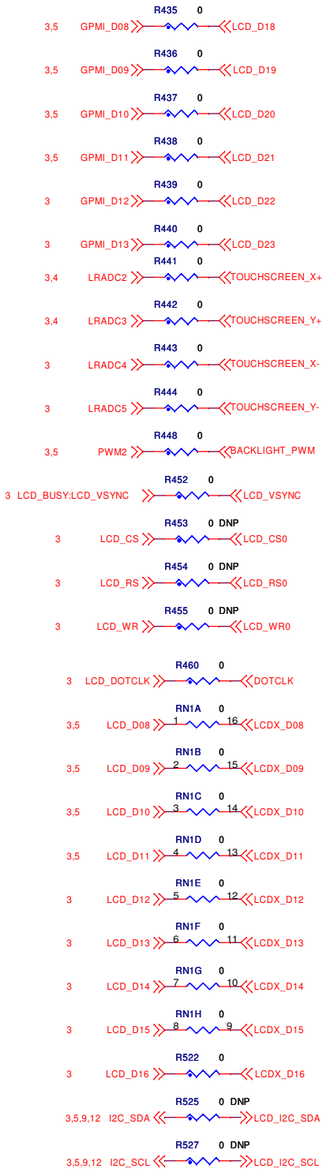
Size	Document Number	Rev
C	SCH-77066 PDF: SPF-77066	C1

Date: Monday, March 15, 2010 Sheet 7 of 12

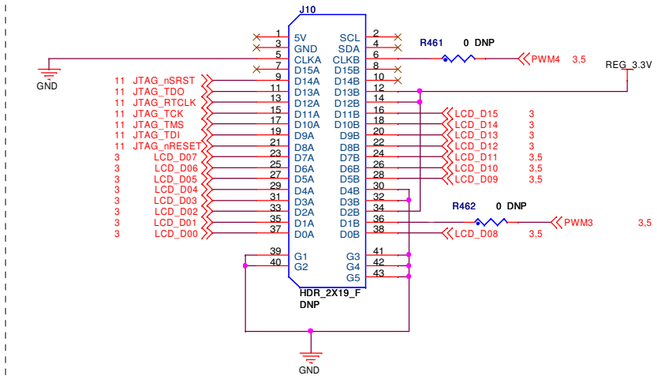
LCD Connector



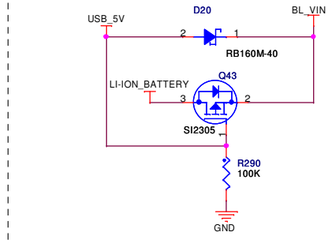
LCD Expansion Header Connections



Optional Mictor Connection Header



LCD Backlight Boost Converter Input Power Selection



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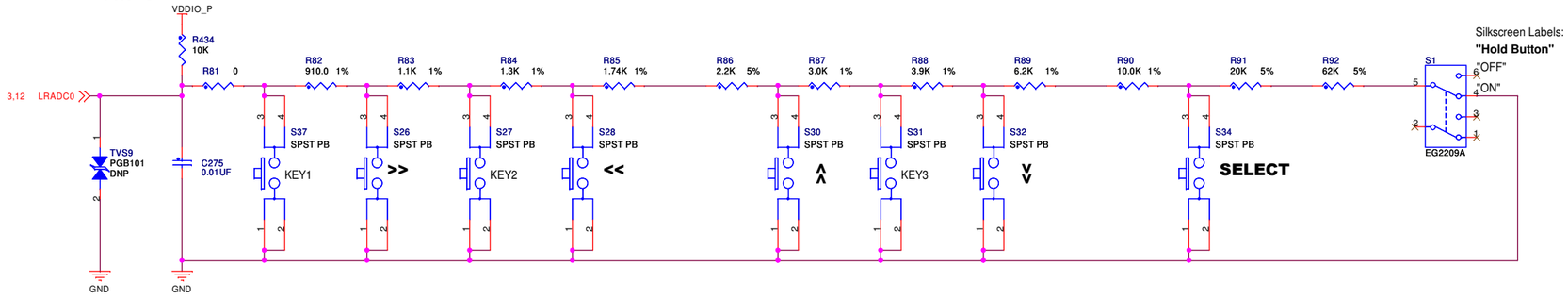
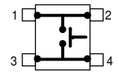
ICAP Classification: FCP: ___ FIUO: X PUBI: ___			
Drawing Title: i.MX233 EVK			
Page Title: LCD			
Size C	Document Number SCH-77066 PDF: SPF-77066		Rev C1
Date: Monday, March 15, 2010		Sheet 8 of 12	

Buttons

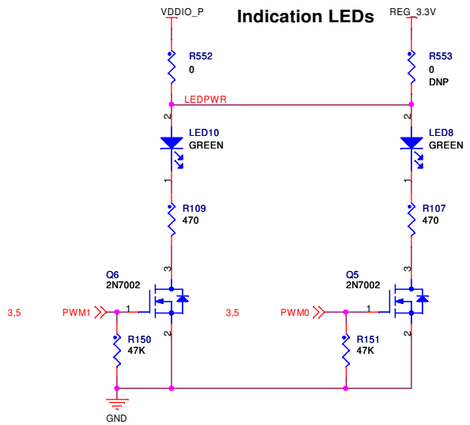


LAYOUT NOTE:

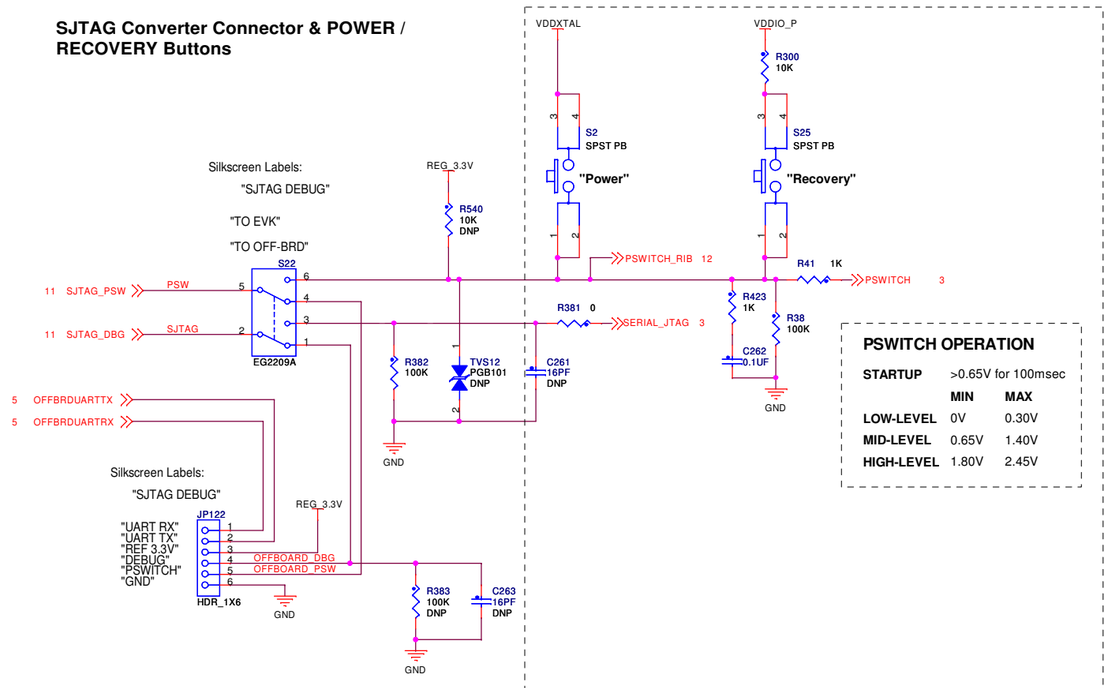


TOP VIEW
EG2526CT-ND
TACT SWITCH

Indication LEDs



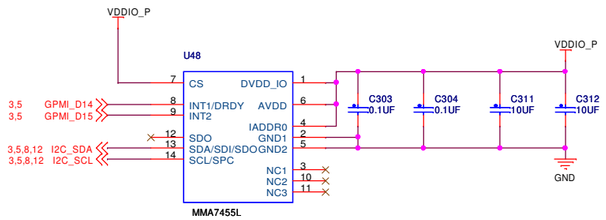
SJTAG Converter Connector & POWER / RECOVERY Buttons



PSWITCH OPERATION

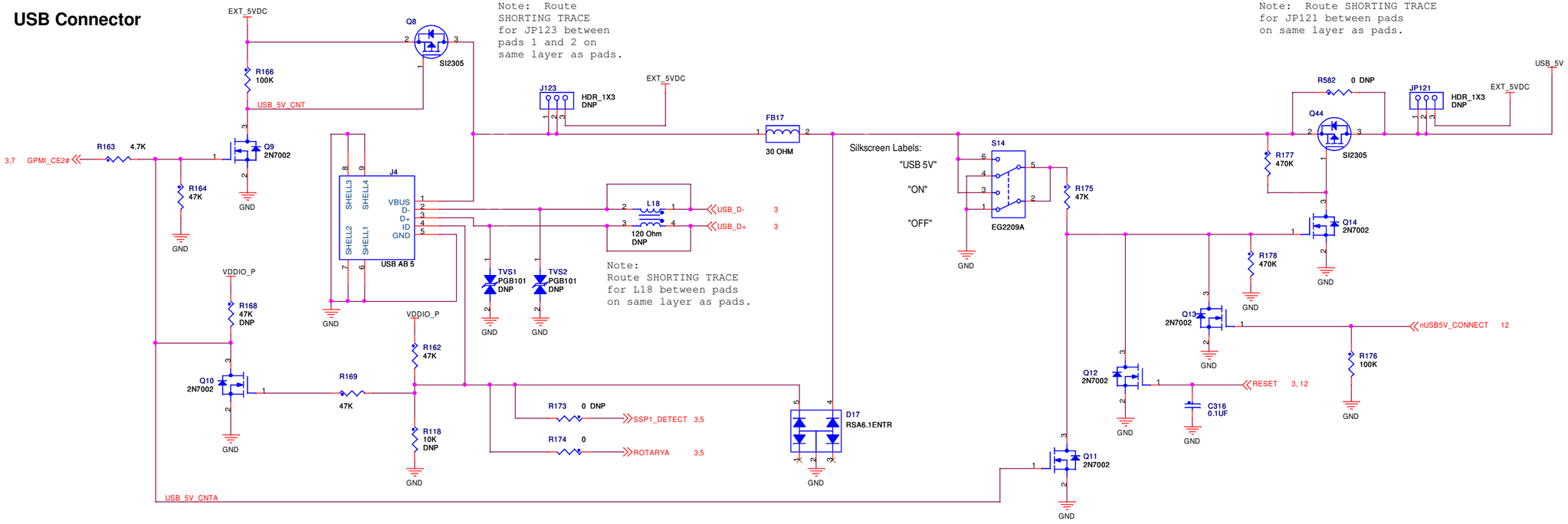
STARTUP	>0.65V for 100msec	
	MIN	**MAX**
LOW-LEVEL	0V	0.30V
MID-LEVEL	0.65V	1.40V
HIGH-LEVEL	1.80V	2.45V

ACCELEROMETER

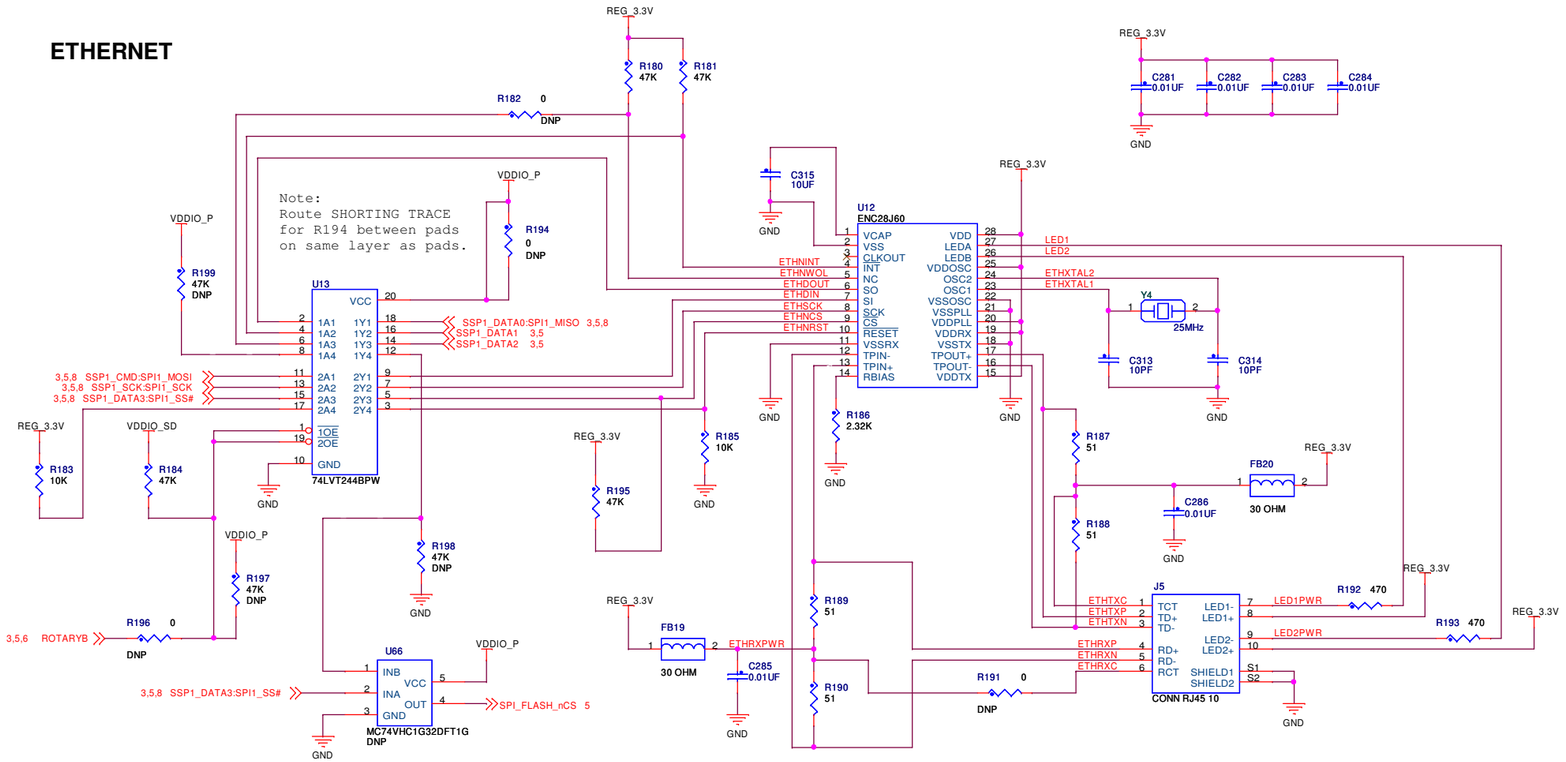


ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	i.MX233 EVK		
Page Title:	UI & SJTAG		
Size: C	Document Number: SCH-77066 PDF: SPF-77066		Rev: C1
Date: Monday, March 15, 2010	Sheet 9 of 12		

USB Connector

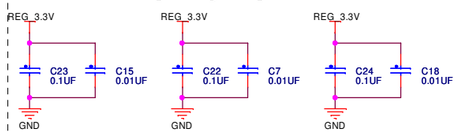


ETHERNET

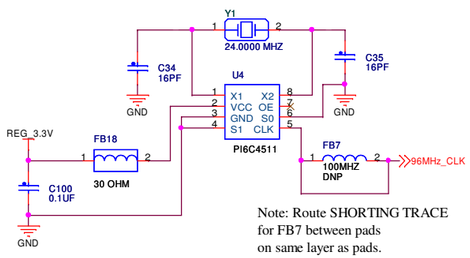


ICAP Classification:	FCP:	FIUO: X	PUBI:
Drawing Title:	i.MX233 EVK		
Page Title:	USB		
Size: C	Document Number: SCH-77066 PDF: SPF-77066		Rev: C1
Date: Monday, March 15, 2010	Sheet 10 of 12		

CPLD Decoupling Caps

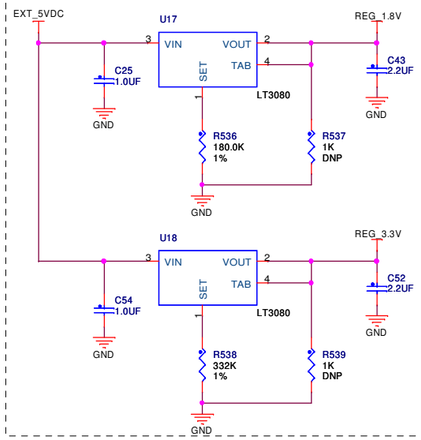


96MHz Clock Generator

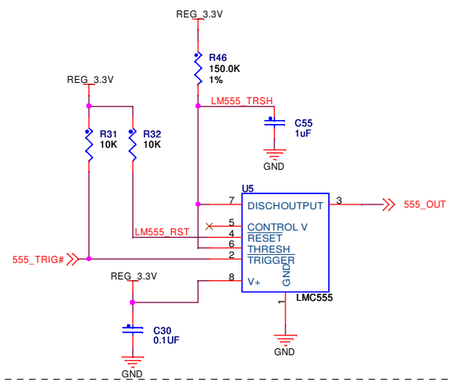


Note: Route SHORTING TRACE for FB7 between pads on same layer as pads.

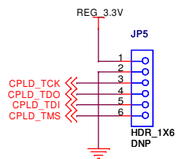
JTAG POWER



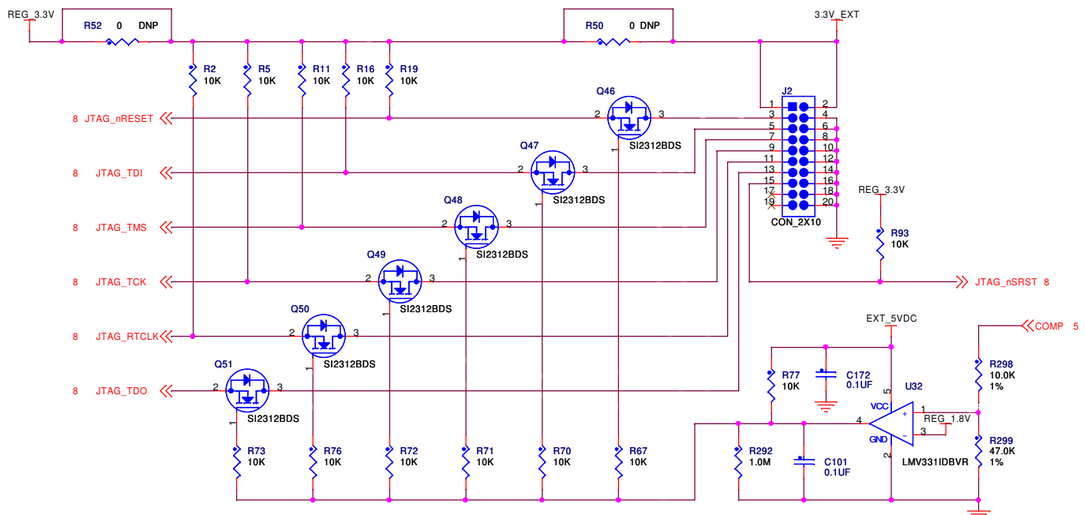
100msec Pulse Generator



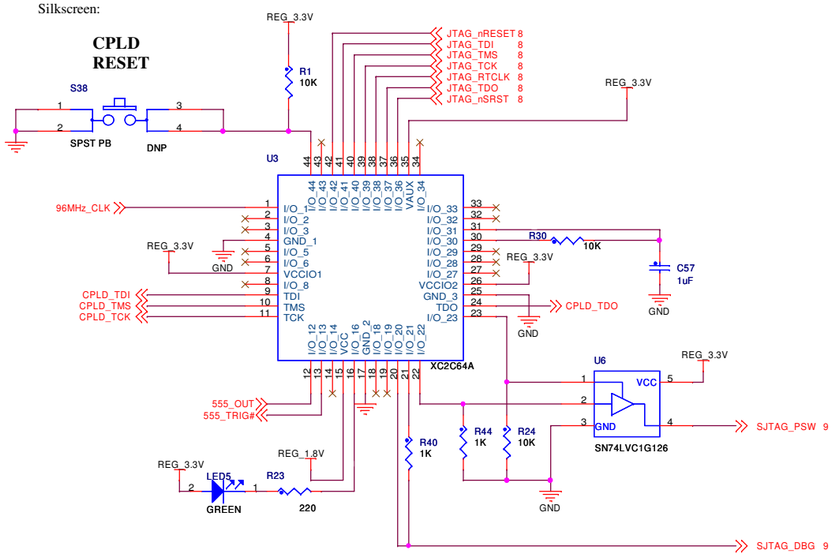
CPLD Program Header



Note: Route SHORTING TRACE for R52 and R50 between pads on same layer as pads.



Silkscreen:



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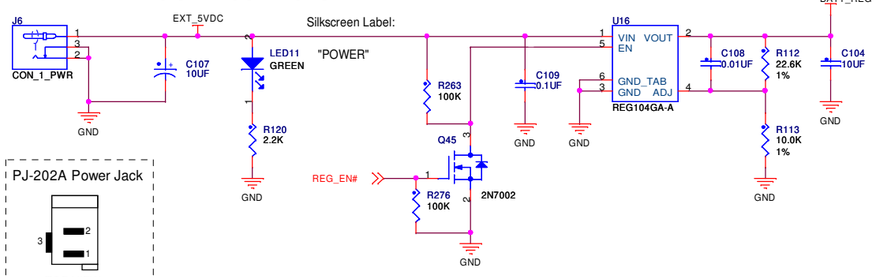
Drawing Title: **i.MX233 EVK**

Page Title: **JTAG**

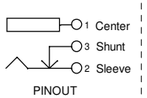
Size	Document Number	Rev
C	SCH-77066 PDF: SPF-77066	C1

Date: Monday, March 15, 2010 Sheet 11 of 12

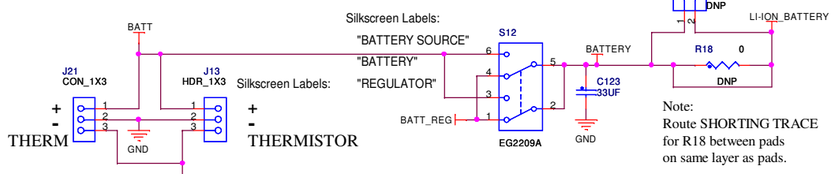
BATTERY & 5V REGULATORS



PJ-202A Power Jack



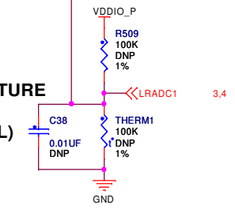
BATTERY & SOURCE SELECT SWITCH



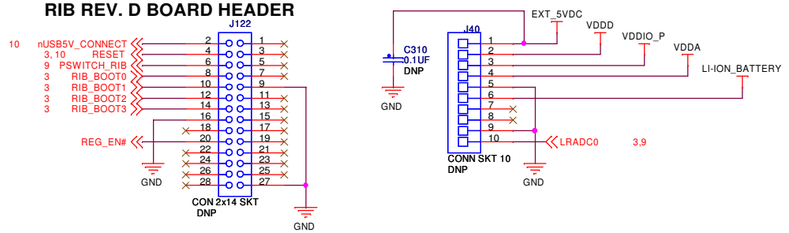
Note:
Route SHORTING TRACE
for R18 between pads
on same layer as pads.

Note:
3-pin connector J21 allows the use of
aftermarket Li-ION batteries. Recommended
battery capacity is 500 - 1000 mAh.

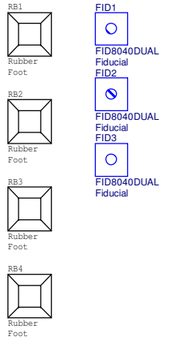
BATTERY CHARGE TEMPERATURE SENSE (OPTIONAL)



RIB REV. D BOARD HEADER

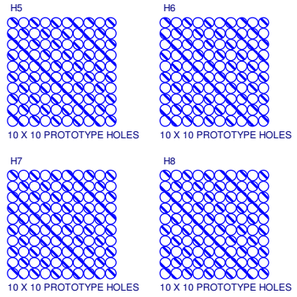


FIDUCIALS & MOUNTING HOLES



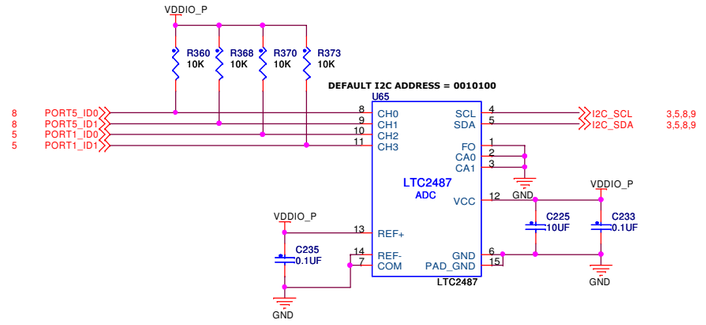
Board Mounting Holes for 4-40 screws

PROTOTYPING AREA 20 X 20 THROUGH HOLES



HARDWARE IDENTIFICATION (4-Channels)

This reduced functionality board ID circuit supports detection of one LCD port (Port 5) and one accessory port (Port 1).



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___		
Drawing Title: i.MX233 EVK		
Page Title: POWER SUPPLY		
Size C	Document Number SCH-77066 PDF: SPF-77066	Rev C1
Date: Monday, March 15, 2010	Sheet 12 of 12	