

# **Programming Paradigms Final Project: Test Report**

GROUP 26  
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# Chapter 1

## Syntax Tests

### Syntax 1

#### Source

```
1 int number;  
2  
3 procedure p() {}
```

#### Output

```
1 Main: tokenList not fully parsed
```

### Syntax 2

#### Source

```
1 procedure(j, int i) {};
```

#### Output

```
1 Main: tokenList not fully parsed
```

### Syntax 3

#### Source

```
1 int 5num = 5;
```

#### Output

```
1 Main: tokenList not fully parsed
```

## Syntax 4

### Source

```
1 if (true) else {// do nothing}
```

### Output

```
1 Main: tokenList not fully parsed
```

## Syntax 5

### Source

```
1 print(5*(3-1));
```

### Output

```
1 Main: tokenList not fully parsed
```

## Chapter 2

# Contextual Tests

### Wrong Type

#### Source

```
1 int i = 1;
2 if (i) {
3     print(i);
4 }
```

#### Output

```
1 Main: Condition in if statement should be of type: bool, but isnt, in: ASTVar "i" ([],[],[])
```

### Not Declared

#### Source

```
1 if (i) {
2     print(1);
3 }
```

#### Output

```
1 Main: Variable: i not declared in Checker.getExprType.iterVar
```

## Chapter 3

# Semantic Tests

### Banking

#### Source

```
1  global int john = 10000;
2  global int jane = 2000;
3  global int martijn = 99999;
4
5  procedure deposit(int account, int amount) {
6      account = (account + amount);
7  }
8
9  procedure withdraw(int account, int amount) {
10     if ((account >= amount)) {
11         account = (account - amount);
12     }
13 }
14
15 procedure transfer(int sender, int target, int amount) {
16     if ((sender >= amount)) {
17         sender = (sender - amount);
18         target = (target + amount);
19     }
20 }
21
22 procedure test1() {
23     print(john, jane, martijn);
24     fork deposit(jane, 100);
25     fork deposit(john, 100);
26     fork deposit(martijn, 1);
27     join;
28     print(john, jane, martijn);
29
30     fork deposit(jane, 200);
```



```
31     fork withdraw(john, 200);
32     fork deposit(martijn, 2000);
33     join;
34     print(john, jane, martijn);
35     fork withdraw(jane, 10);
36     fork withdraw(john, 20);
37     fork deposit(martijn, 100);
38     join;
39     print(john, jane, martijn);
40     fork withdraw(jane, 300);
41     fork withdraw(john, 30000);
42     fork withdraw(martijn, 50);
43     join;
44     print(john, jane, martijn);
45     fork withdraw(jane, 35);
46     fork transfer(martijn, john, 1000);
47     join;
48     print(john, jane, martijn);
49     fork transfer(martijn, jane, 100);
50     join;
51     print(john, jane, martijn);
52
53 }
54
55 test1();
```

## Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 1470)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
```

```
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 7) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 2 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
```

```
68 Compute Add 7 0 4
69 ComputeI Add 4 3 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Compute Add 7 0 6
73 Load (IndAddr 6) 6
74 ComputeI Add 6 1 6
75 Load (IndAddr 6) 5
76 Push 5
77 Compute Add 7 0 6
78 Load (IndAddr 6) 6
79 ComputeI Add 6 2 6
80 Load (IndAddr 6) 5
81 Push 5
82 Pop 3
83 Pop 2
84 Compute Add 2 3 4
85 Push 4
86 Compute Add 7 0 6
87 Load (IndAddr 6) 6
88 ComputeI Add 6 1 6
89 Pop 2
90 Store 2 (IndAddr 6)
91 Push 2
92 Pop 0
93 Load (IndAddr 7) 7
94 Load (ImmValue 6) 2
95 Compute Sub 7 2 2
96 ComputeI Add 0 1 5
97 ComputeI Gt 5 2 6
98 Branch 6 (Rel 23)
99 Compute Add 7 5 6
100 Load (IndAddr 6) 4
101 Load (IndAddr 2) 3
102 Compute Lt 3 0 6
103 Branch 6 (Rel 2)
104 Store 4 (IndAddr 3)
105 Compute Incr 2 0 2
106 Load (IndAddr 2) 3
107 Compute Lt 3 0 6
108 Branch 6 (Rel 10)
109 Compute Add 3 0 6
110 TestAndSet (IndAddr 6)
111 Receive 6
112 Branch 6 (Rel 2)
113 Jump (Rel (-4))
114 ComputeI Add 3 1 3
115 WriteInstr 4 (IndAddr 3)
```

```
116 ComputeI Sub 3 1 3
117 WriteInstr 0 (IndAddr 3)
118 Compute Incr 5 0 5
119 ComputeI Add 2 2 2
120 Jump (Rel (-23))
121 Compute Decr 7 0 2
122 Load (IndAddr 2) 6
123 Load (IndAddr 7) 7
124 Jump (Ind 6)
125 Load (ImmValue 7) 2
126 Compute Sub 7 2 2
127 Load (ImmValue 1) 5
128 ComputeI Gt 5 2 6
129 Branch 6 (Rel 7)
130 Load (IndAddr 2) 3
131 Compute Add 7 5 6
132 Store 3 (IndAddr 6)
133 Compute Incr 5 0 5
134 ComputeI Add 2 3 2
135 Jump (Rel (-7))
136 Compute Add 7 0 4
137 ComputeI Add 4 3 4
138 Store 7 (IndAddr 4)
139 Compute Add 4 0 7
140 Compute Add 7 0 6
141 Load (IndAddr 6) 6
142 ComputeI Add 6 1 6
143 Load (IndAddr 6) 5
144 Push 5
145 Compute Add 7 0 6
146 Load (IndAddr 6) 6
147 ComputeI Add 6 2 6
148 Load (IndAddr 6) 5
149 Push 5
150 Pop 3
151 Pop 2
152 Compute GtE 2 3 4
153 Push 4
154 Pop 6
155 ComputeI Xor 6 1 6
156 Branch 6 (Rel 30)
157 Compute Add 7 0 4
158 ComputeI Add 4 1 4
159 Store 7 (IndAddr 4)
160 Compute Add 4 0 7
161 Compute Add 7 0 6
162 Load (IndAddr 6) 6
163 Load (IndAddr 6) 6
```

```
164 ComputeI Add 6 1 6
165 Load (IndAddr 6) 5
166 Push 5
167 Compute Add 7 0 6
168 Load (IndAddr 6) 6
169 Load (IndAddr 6) 6
170 ComputeI Add 6 2 6
171 Load (IndAddr 6) 5
172 Push 5
173 Pop 3
174 Pop 2
175 Compute Sub 2 3 4
176 Push 4
177 Compute Add 7 0 6
178 Load (IndAddr 6) 6
179 Load (IndAddr 6) 6
180 ComputeI Add 6 1 6
181 Pop 2
182 Store 2 (IndAddr 6)
183 Push 2
184 Pop 0
185 Load (IndAddr 7) 7
186 Load (IndAddr 7) 7
187 Load (ImmValue 6) 2
188 Compute Sub 7 2 2
189 ComputeI Add 0 1 5
190 ComputeI Gt 5 2 6
191 Branch 6 (Rel 23)
192 Compute Add 7 5 6
193 Load (IndAddr 6) 4
194 Load (IndAddr 2) 3
195 Compute Lt 3 0 6
196 Branch 6 (Rel 2)
197 Store 4 (IndAddr 3)
198 Compute Incr 2 0 2
199 Load (IndAddr 2) 3
200 Compute Lt 3 0 6
201 Branch 6 (Rel 10)
202 Compute Add 3 0 6
203 TestAndSet (IndAddr 6)
204 Receive 6
205 Branch 6 (Rel 2)
206 Jump (Rel (-4))
207 ComputeI Add 3 1 3
208 WriteInstr 4 (IndAddr 3)
209 ComputeI Sub 3 1 3
210 WriteInstr 0 (IndAddr 3)
211 Compute Incr 5 0 5
```

```
212 ComputeI Add 2 2 2
213 Jump (Rel (-23))
214 Compute Decr 7 0 2
215 Load (IndAddr 2) 6
216 Load (IndAddr 7) 7
217 Jump (Ind 6)
218 Load (ImmValue 10) 2
219 Compute Sub 7 2 2
220 Load (ImmValue 1) 5
221 ComputeI Gt 5 3 6
222 Branch 6 (Rel 7)
223 Load (IndAddr 2) 3
224 Compute Add 7 5 6
225 Store 3 (IndAddr 6)
226 Compute Incr 5 0 5
227 ComputeI Add 2 3 2
228 Jump (Rel (-7))
229 Compute Add 7 0 4
230 ComputeI Add 4 4 4
231 Store 7 (IndAddr 4)
232 Compute Add 4 0 7
233 Compute Add 7 0 6
234 Load (IndAddr 6) 6
235 ComputeI Add 6 1 6
236 Load (IndAddr 6) 5
237 Push 5
238 Compute Add 7 0 6
239 Load (IndAddr 6) 6
240 ComputeI Add 6 3 6
241 Load (IndAddr 6) 5
242 Push 5
243 Pop 3
244 Pop 2
245 Compute GtE 2 3 4
246 Push 4
247 Pop 6
248 ComputeI Xor 6 1 6
249 Branch 6 (Rel 54)
250 Compute Add 7 0 4
251 ComputeI Add 4 1 4
252 Store 7 (IndAddr 4)
253 Compute Add 4 0 7
254 Compute Add 7 0 6
255 Load (IndAddr 6) 6
256 Load (IndAddr 6) 6
257 ComputeI Add 6 1 6
258 Load (IndAddr 6) 5
259 Push 5
```

```
260 Compute Add 7 0 6
261 Load (IndAddr 6) 6
262 Load (IndAddr 6) 6
263 ComputeI Add 6 3 6
264 Load (IndAddr 6) 5
265 Push 5
266 Pop 3
267 Pop 2
268 Compute Sub 2 3 4
269 Push 4
270 Compute Add 7 0 6
271 Load (IndAddr 6) 6
272 Load (IndAddr 6) 6
273 ComputeI Add 6 1 6
274 Pop 2
275 Store 2 (IndAddr 6)
276 Push 2
277 Pop 0
278 Compute Add 7 0 6
279 Load (IndAddr 6) 6
280 Load (IndAddr 6) 6
281 ComputeI Add 6 2 6
282 Load (IndAddr 6) 5
283 Push 5
284 Compute Add 7 0 6
285 Load (IndAddr 6) 6
286 Load (IndAddr 6) 6
287 ComputeI Add 6 3 6
288 Load (IndAddr 6) 5
289 Push 5
290 Pop 3
291 Pop 2
292 Compute Add 2 3 4
293 Push 4
294 Compute Add 7 0 6
295 Load (IndAddr 6) 6
296 Load (IndAddr 6) 6
297 ComputeI Add 6 2 6
298 Pop 2
299 Store 2 (IndAddr 6)
300 Push 2
301 Pop 0
302 Load (IndAddr 7) 7
303 Load (IndAddr 7) 7
304 Load (ImmValue 9) 2
305 Compute Sub 7 2 2
306 ComputeI Add 0 1 5
307 ComputeI Gt 5 3 6
```

```
308 Branch 6 (Rel 23)
309 Compute Add 7 5 6
310 Load (IndAddr 6) 4
311 Load (IndAddr 2) 3
312 Compute Lt 3 0 6
313 Branch 6 (Rel 2)
314 Store 4 (IndAddr 3)
315 Compute Incr 2 0 2
316 Load (IndAddr 2) 3
317 Compute Lt 3 0 6
318 Branch 6 (Rel 10)
319 Compute Add 3 0 6
320 TestAndSet (IndAddr 6)
321 Receive 6
322 Branch 6 (Rel 2)
323 Jump (Rel (-4))
324 ComputeI Add 3 1 3
325 WriteInstr 4 (IndAddr 3)
326 ComputeI Sub 3 1 3
327 WriteInstr 0 (IndAddr 3)
328 Compute Incr 5 0 5
329 ComputeI Add 2 2 2
330 Jump (Rel (-23))
331 Compute Decr 7 0 2
332 Load (IndAddr 2) 6
333 Load (IndAddr 7) 7
334 Jump (Ind 6)
335 Load (ImmValue 1) 2
336 Compute Sub 7 2 2
337 Load (ImmValue 1) 5
338 ComputeI Gt 5 0 6
339 Branch 6 (Rel 7)
340 Load (IndAddr 2) 3
341 Compute Add 7 5 6
342 Store 3 (IndAddr 6)
343 Compute Incr 5 0 5
344 ComputeI Add 2 3 2
345 Jump (Rel (-7))
346 Compute Add 7 0 4
347 ComputeI Add 4 1 4
348 Store 7 (IndAddr 4)
349 Compute Add 4 0 7
350 Load (ImmValue 37) 2
351 TestAndSet (IndAddr 2)
352 Receive 3
353 Branch 3 (Rel 2)
354 Jump (Rel (-4))
355 Load (ImmValue 38) 4
```



```
356 ReadInstr (IndAddr 4)
357 Receive 5
358 Push 5
359 WriteInstr 0 (IndAddr 2)
360 Load (ImmValue 33) 2
361 TestAndSet (IndAddr 2)
362 Receive 3
363 Branch 3 (Rel 2)
364 Jump (Rel (-4))
365 Load (ImmValue 34) 4
366 ReadInstr (IndAddr 4)
367 Receive 5
368 Push 5
369 WriteInstr 0 (IndAddr 2)
370 Load (ImmValue 35) 2
371 TestAndSet (IndAddr 2)
372 Receive 3
373 Branch 3 (Rel 2)
374 Jump (Rel (-4))
375 Load (ImmValue 36) 4
376 ReadInstr (IndAddr 4)
377 Receive 5
378 Push 5
379 WriteInstr 0 (IndAddr 2)
380 Pop 6
381 PrintOut 6
382 Pop 6
383 PrintOut 6
384 Pop 6
385 PrintOut 6
386 TestAndSet (DirAddr 1)
387 Receive 6
388 Branch 6 (Rel 2)
389 Jump (Rel (-3))
390 Load (ImmValue 100) 6
391 Push 6
392 Load (ImmValue 33) 2
393 TestAndSet (IndAddr 2)
394 Receive 3
395 Branch 3 (Rel 2)
396 Jump (Rel (-4))
397 Load (ImmValue 34) 4
398 ReadInstr (IndAddr 4)
399 Receive 5
400 Push 5
401 WriteInstr 0 (IndAddr 2)
402 Load (ImmValue 5) 4
403 Pop 3
```

```
404 WriteInstr 3 (IndAddr 4)
405 Compute Incr 4 0 4
406 Load (ImmValue (-1)) 3
407 WriteInstr 3 (IndAddr 4)
408 Compute Incr 4 0 4
409 Load (ImmValue 33) 3
410 WriteInstr 3 (IndAddr 4)
411 Compute Incr 4 0 4
412 Pop 3
413 WriteInstr 3 (IndAddr 4)
414 Compute Incr 4 0 4
415 Load (ImmValue (-1)) 3
416 WriteInstr 3 (IndAddr 4)
417 Compute Incr 4 0 4
418 Load (ImmValue (-1)) 3
419 WriteInstr 3 (IndAddr 4)
420 Compute Incr 4 0 4
421 Load (ImmValue 2) 5
422 WriteInstr 5 (DirAddr 4)
423 Load (ImmValue 57) 6
424 Push 6
425 Pop 5
426 WriteInstr 5 (DirAddr 3)
427 WriteInstr 0 (DirAddr 2)
428 Load (ImmValue 1) 3
429 ReadInstr (IndAddr 3)
430 Receive 6
431 Branch 6 (Rel 2)
432 Jump (Rel (-3))
433 TestAndSet (DirAddr 1)
434 Receive 6
435 Branch 6 (Rel 2)
436 Jump (Rel (-3))
437 Load (ImmValue 100) 6
438 Push 6
439 Load (ImmValue 35) 2
440 TestAndSet (IndAddr 2)
441 Receive 3
442 Branch 3 (Rel 2)
443 Jump (Rel (-4))
444 Load (ImmValue 36) 4
445 ReadInstr (IndAddr 4)
446 Receive 5
447 Push 5
448 WriteInstr 0 (IndAddr 2)
449 Load (ImmValue 5) 4
450 Pop 3
451 WriteInstr 3 (IndAddr 4)
```

```
452 Compute Incr 4 0 4
453 Load (ImmValue (-1)) 3
454 WriteInstr 3 (IndAddr 4)
455 Compute Incr 4 0 4
456 Load (ImmValue 35) 3
457 WriteInstr 3 (IndAddr 4)
458 Compute Incr 4 0 4
459 Pop 3
460 WriteInstr 3 (IndAddr 4)
461 Compute Incr 4 0 4
462 Load (ImmValue (-1)) 3
463 WriteInstr 3 (IndAddr 4)
464 Compute Incr 4 0 4
465 Load (ImmValue (-1)) 3
466 WriteInstr 3 (IndAddr 4)
467 Compute Incr 4 0 4
468 Load (ImmValue 2) 5
469 WriteInstr 5 (DirAddr 4)
470 Load (ImmValue 57) 6
471 Push 6
472 Pop 5
473 WriteInstr 5 (DirAddr 3)
474 WriteInstr 0 (DirAddr 2)
475 Load (ImmValue 1) 3
476 ReadInstr (IndAddr 3)
477 Receive 6
478 Branch 6 (Rel 2)
479 Jump (Rel (-3))
480 TestAndSet (DirAddr 1)
481 Receive 6
482 Branch 6 (Rel 2)
483 Jump (Rel (-3))
484 Load (ImmValue 1) 6
485 Push 6
486 Load (ImmValue 37) 2
487 TestAndSet (IndAddr 2)
488 Receive 3
489 Branch 3 (Rel 2)
490 Jump (Rel (-4))
491 Load (ImmValue 38) 4
492 ReadInstr (IndAddr 4)
493 Receive 5
494 Push 5
495 WriteInstr 0 (IndAddr 2)
496 Load (ImmValue 5) 4
497 Pop 3
498 WriteInstr 3 (IndAddr 4)
499 Compute Incr 4 0 4
```

```
500 Load (ImmValue (-1)) 3
501 WriteInstr 3 (IndAddr 4)
502 Compute Incr 4 0 4
503 Load (ImmValue 37) 3
504 WriteInstr 3 (IndAddr 4)
505 Compute Incr 4 0 4
506 Pop 3
507 WriteInstr 3 (IndAddr 4)
508 Compute Incr 4 0 4
509 Load (ImmValue (-1)) 3
510 WriteInstr 3 (IndAddr 4)
511 Compute Incr 4 0 4
512 Load (ImmValue (-1)) 3
513 WriteInstr 3 (IndAddr 4)
514 Compute Incr 4 0 4
515 Load (ImmValue 2) 5
516 WriteInstr 5 (DirAddr 4)
517 Load (ImmValue 57) 6
518 Push 6
519 Pop 5
520 WriteInstr 5 (DirAddr 3)
521 WriteInstr 0 (DirAddr 2)
522 Load (ImmValue 1) 3
523 ReadInstr (IndAddr 3)
524 Receive 6
525 Branch 6 (Rel 2)
526 Jump (Rel (-3))
527 Compute Equal 0 1 6
528 Branch 6 (Rel 4)
529 Load (ImmValue 2) 2
530 PrintOut 2
531 EndProg
532 Load (ImmValue 30) 3
533 Load (ImmValue 0) 2
534 ReadInstr (IndAddr 3)
535 Receive 4
536 Compute Add 2 4 2
537 ComputeI NEq 3 33 6
538 Compute Incr 3 0 3
539 Branch 6 (Rel (-5))
540 Compute Equal 2 0 6
541 Branch 6 (Rel 2)
542 Jump (Rel (-10))
543 Load (ImmValue 37) 2
544 TestAndSet (IndAddr 2)
545 Receive 3
546 Branch 3 (Rel 2)
547 Jump (Rel (-4))
```

```
548 Load (ImmValue 38) 4
549 ReadInstr (IndAddr 4)
550 Receive 5
551 Push 5
552 WriteInstr 0 (IndAddr 2)
553 Load (ImmValue 33) 2
554 TestAndSet (IndAddr 2)
555 Receive 3
556 Branch 3 (Rel 2)
557 Jump (Rel (-4))
558 Load (ImmValue 34) 4
559 ReadInstr (IndAddr 4)
560 Receive 5
561 Push 5
562 WriteInstr 0 (IndAddr 2)
563 Load (ImmValue 35) 2
564 TestAndSet (IndAddr 2)
565 Receive 3
566 Branch 3 (Rel 2)
567 Jump (Rel (-4))
568 Load (ImmValue 36) 4
569 ReadInstr (IndAddr 4)
570 Receive 5
571 Push 5
572 WriteInstr 0 (IndAddr 2)
573 Pop 6
574 PrintOut 6
575 Pop 6
576 PrintOut 6
577 Pop 6
578 PrintOut 6
579 TestAndSet (DirAddr 1)
580 Receive 6
581 Branch 6 (Rel 2)
582 Jump (Rel (-3))
583 Load (ImmValue 200) 6
584 Push 6
585 Load (ImmValue 33) 2
586 TestAndSet (IndAddr 2)
587 Receive 3
588 Branch 3 (Rel 2)
589 Jump (Rel (-4))
590 Load (ImmValue 34) 4
591 ReadInstr (IndAddr 4)
592 Receive 5
593 Push 5
594 WriteInstr 0 (IndAddr 2)
595 Load (ImmValue 5) 4
```

```
596 Pop 3
597 WriteInstr 3 (IndAddr 4)
598 Compute Incr 4 0 4
599 Load (ImmValue (-1)) 3
600 WriteInstr 3 (IndAddr 4)
601 Compute Incr 4 0 4
602 Load (ImmValue 33) 3
603 WriteInstr 3 (IndAddr 4)
604 Compute Incr 4 0 4
605 Pop 3
606 WriteInstr 3 (IndAddr 4)
607 Compute Incr 4 0 4
608 Load (ImmValue (-1)) 3
609 WriteInstr 3 (IndAddr 4)
610 Compute Incr 4 0 4
611 Load (ImmValue (-1)) 3
612 WriteInstr 3 (IndAddr 4)
613 Compute Incr 4 0 4
614 Load (ImmValue 2) 5
615 WriteInstr 5 (DirAddr 4)
616 Load (ImmValue 57) 6
617 Push 6
618 Pop 5
619 WriteInstr 5 (DirAddr 3)
620 WriteInstr 0 (DirAddr 2)
621 Load (ImmValue 1) 3
622 ReadInstr (IndAddr 3)
623 Receive 6
624 Branch 6 (Rel 2)
625 Jump (Rel (-3))
626 TestAndSet (DirAddr 1)
627 Receive 6
628 Branch 6 (Rel 2)
629 Jump (Rel (-3))
630 Load (ImmValue 200) 6
631 Push 6
632 Load (ImmValue 35) 2
633 TestAndSet (IndAddr 2)
634 Receive 3
635 Branch 3 (Rel 2)
636 Jump (Rel (-4))
637 Load (ImmValue 36) 4
638 ReadInstr (IndAddr 4)
639 Receive 5
640 Push 5
641 WriteInstr 0 (IndAddr 2)
642 Load (ImmValue 5) 4
643 Pop 3
```

```
644 WriteInstr 3 (IndAddr 4)
645 Compute Incr 4 0 4
646 Load (ImmValue (-1)) 3
647 WriteInstr 3 (IndAddr 4)
648 Compute Incr 4 0 4
649 Load (ImmValue 35) 3
650 WriteInstr 3 (IndAddr 4)
651 Compute Incr 4 0 4
652 Pop 3
653 WriteInstr 3 (IndAddr 4)
654 Compute Incr 4 0 4
655 Load (ImmValue (-1)) 3
656 WriteInstr 3 (IndAddr 4)
657 Compute Incr 4 0 4
658 Load (ImmValue (-1)) 3
659 WriteInstr 3 (IndAddr 4)
660 Compute Incr 4 0 4
661 Load (ImmValue 2) 5
662 WriteInstr 5 (DirAddr 4)
663 Load (ImmValue 125) 6
664 Push 6
665 Pop 5
666 WriteInstr 5 (DirAddr 3)
667 WriteInstr 0 (DirAddr 2)
668 Load (ImmValue 1) 3
669 ReadInstr (IndAddr 3)
670 Receive 6
671 Branch 6 (Rel 2)
672 Jump (Rel (-3))
673 TestAndSet (DirAddr 1)
674 Receive 6
675 Branch 6 (Rel 2)
676 Jump (Rel (-3))
677 Load (ImmValue 2000) 6
678 Push 6
679 Load (ImmValue 37) 2
680 TestAndSet (IndAddr 2)
681 Receive 3
682 Branch 3 (Rel 2)
683 Jump (Rel (-4))
684 Load (ImmValue 38) 4
685 ReadInstr (IndAddr 4)
686 Receive 5
687 Push 5
688 WriteInstr 0 (IndAddr 2)
689 Load (ImmValue 5) 4
690 Pop 3
691 WriteInstr 3 (IndAddr 4)
```

```
692 Compute Incr 4 0 4
693 Load (ImmValue (-1)) 3
694 WriteInstr 3 (IndAddr 4)
695 Compute Incr 4 0 4
696 Load (ImmValue 37) 3
697 WriteInstr 3 (IndAddr 4)
698 Compute Incr 4 0 4
699 Pop 3
700 WriteInstr 3 (IndAddr 4)
701 Compute Incr 4 0 4
702 Load (ImmValue (-1)) 3
703 WriteInstr 3 (IndAddr 4)
704 Compute Incr 4 0 4
705 Load (ImmValue (-1)) 3
706 WriteInstr 3 (IndAddr 4)
707 Compute Incr 4 0 4
708 Load (ImmValue 2) 5
709 WriteInstr 5 (DirAddr 4)
710 Load (ImmValue 57) 6
711 Push 6
712 Pop 5
713 WriteInstr 5 (DirAddr 3)
714 WriteInstr 0 (DirAddr 2)
715 Load (ImmValue 1) 3
716 ReadInstr (IndAddr 3)
717 Receive 6
718 Branch 6 (Rel 2)
719 Jump (Rel (-3))
720 Compute Equal 0 1 6
721 Branch 6 (Rel 4)
722 Load (ImmValue 2) 2
723 PrintOut 2
724 EndProg
725 Load (ImmValue 30) 3
726 Load (ImmValue 0) 2
727 ReadInstr (IndAddr 3)
728 Receive 4
729 Compute Add 2 4 2
730 ComputeI NEq 3 33 6
731 Compute Incr 3 0 3
732 Branch 6 (Rel (-5))
733 Compute Equal 2 0 6
734 Branch 6 (Rel 2)
735 Jump (Rel (-10))
736 Load (ImmValue 37) 2
737 TestAndSet (IndAddr 2)
738 Receive 3
739 Branch 3 (Rel 2)
```



```
740  Jump (Rel (-4))
741  Load (ImmValue 38) 4
742  ReadInstr (IndAddr 4)
743  Receive 5
744  Push 5
745  WriteInstr 0 (IndAddr 2)
746  Load (ImmValue 33) 2
747  TestAndSet (IndAddr 2)
748  Receive 3
749  Branch 3 (Rel 2)
750  Jump (Rel (-4))
751  Load (ImmValue 34) 4
752  ReadInstr (IndAddr 4)
753  Receive 5
754  Push 5
755  WriteInstr 0 (IndAddr 2)
756  Load (ImmValue 35) 2
757  TestAndSet (IndAddr 2)
758  Receive 3
759  Branch 3 (Rel 2)
760  Jump (Rel (-4))
761  Load (ImmValue 36) 4
762  ReadInstr (IndAddr 4)
763  Receive 5
764  Push 5
765  WriteInstr 0 (IndAddr 2)
766  Pop 6
767  PrintOut 6
768  Pop 6
769  PrintOut 6
770  Pop 6
771  PrintOut 6
772  TestAndSet (DirAddr 1)
773  Receive 6
774  Branch 6 (Rel 2)
775  Jump (Rel (-3))
776  Load (ImmValue 10) 6
777  Push 6
778  Load (ImmValue 33) 2
779  TestAndSet (IndAddr 2)
780  Receive 3
781  Branch 3 (Rel 2)
782  Jump (Rel (-4))
783  Load (ImmValue 34) 4
784  ReadInstr (IndAddr 4)
785  Receive 5
786  Push 5
787  WriteInstr 0 (IndAddr 2)
```

```
788 Load (ImmValue 5) 4
789 Pop 3
790 WriteInstr 3 (IndAddr 4)
791 Compute Incr 4 0 4
792 Load (ImmValue (-1)) 3
793 WriteInstr 3 (IndAddr 4)
794 Compute Incr 4 0 4
795 Load (ImmValue 33) 3
796 WriteInstr 3 (IndAddr 4)
797 Compute Incr 4 0 4
798 Pop 3
799 WriteInstr 3 (IndAddr 4)
800 Compute Incr 4 0 4
801 Load (ImmValue (-1)) 3
802 WriteInstr 3 (IndAddr 4)
803 Compute Incr 4 0 4
804 Load (ImmValue (-1)) 3
805 WriteInstr 3 (IndAddr 4)
806 Compute Incr 4 0 4
807 Load (ImmValue 2) 5
808 WriteInstr 5 (DirAddr 4)
809 Load (ImmValue 125) 6
810 Push 6
811 Pop 5
812 WriteInstr 5 (DirAddr 3)
813 WriteInstr 0 (DirAddr 2)
814 Load (ImmValue 1) 3
815 ReadInstr (IndAddr 3)
816 Receive 6
817 Branch 6 (Rel 2)
818 Jump (Rel (-3))
819 TestAndSet (DirAddr 1)
820 Receive 6
821 Branch 6 (Rel 2)
822 Jump (Rel (-3))
823 Load (ImmValue 20) 6
824 Push 6
825 Load (ImmValue 35) 2
826 TestAndSet (IndAddr 2)
827 Receive 3
828 Branch 3 (Rel 2)
829 Jump (Rel (-4))
830 Load (ImmValue 36) 4
831 ReadInstr (IndAddr 4)
832 Receive 5
833 Push 5
834 WriteInstr 0 (IndAddr 2)
835 Load (ImmValue 5) 4
```

```
836 Pop 3
837 WriteInstr 3 (IndAddr 4)
838 Compute Incr 4 0 4
839 Load (ImmValue (-1)) 3
840 WriteInstr 3 (IndAddr 4)
841 Compute Incr 4 0 4
842 Load (ImmValue 35) 3
843 WriteInstr 3 (IndAddr 4)
844 Compute Incr 4 0 4
845 Pop 3
846 WriteInstr 3 (IndAddr 4)
847 Compute Incr 4 0 4
848 Load (ImmValue (-1)) 3
849 WriteInstr 3 (IndAddr 4)
850 Compute Incr 4 0 4
851 Load (ImmValue (-1)) 3
852 WriteInstr 3 (IndAddr 4)
853 Compute Incr 4 0 4
854 Load (ImmValue 2) 5
855 WriteInstr 5 (DirAddr 4)
856 Load (ImmValue 125) 6
857 Push 6
858 Pop 5
859 WriteInstr 5 (DirAddr 3)
860 WriteInstr 0 (DirAddr 2)
861 Load (ImmValue 1) 3
862 ReadInstr (IndAddr 3)
863 Receive 6
864 Branch 6 (Rel 2)
865 Jump (Rel (-3))
866 TestAndSet (DirAddr 1)
867 Receive 6
868 Branch 6 (Rel 2)
869 Jump (Rel (-3))
870 Load (ImmValue 100) 6
871 Push 6
872 Load (ImmValue 37) 2
873 TestAndSet (IndAddr 2)
874 Receive 3
875 Branch 3 (Rel 2)
876 Jump (Rel (-4))
877 Load (ImmValue 38) 4
878 ReadInstr (IndAddr 4)
879 Receive 5
880 Push 5
881 WriteInstr 0 (IndAddr 2)
882 Load (ImmValue 5) 4
883 Pop 3
```

```
884 WriteInstr 3 (IndAddr 4)
885 Compute Incr 4 0 4
886 Load (ImmValue (-1)) 3
887 WriteInstr 3 (IndAddr 4)
888 Compute Incr 4 0 4
889 Load (ImmValue 37) 3
890 WriteInstr 3 (IndAddr 4)
891 Compute Incr 4 0 4
892 Pop 3
893 WriteInstr 3 (IndAddr 4)
894 Compute Incr 4 0 4
895 Load (ImmValue (-1)) 3
896 WriteInstr 3 (IndAddr 4)
897 Compute Incr 4 0 4
898 Load (ImmValue (-1)) 3
899 WriteInstr 3 (IndAddr 4)
900 Compute Incr 4 0 4
901 Load (ImmValue 2) 5
902 WriteInstr 5 (DirAddr 4)
903 Load (ImmValue 57) 6
904 Push 6
905 Pop 5
906 WriteInstr 5 (DirAddr 3)
907 WriteInstr 0 (DirAddr 2)
908 Load (ImmValue 1) 3
909 ReadInstr (IndAddr 3)
910 Receive 6
911 Branch 6 (Rel 2)
912 Jump (Rel (-3))
913 Compute Equal 0 1 6
914 Branch 6 (Rel 4)
915 Load (ImmValue 2) 2
916 PrintOut 2
917 EndProg
918 Load (ImmValue 30) 3
919 Load (ImmValue 0) 2
920 ReadInstr (IndAddr 3)
921 Receive 4
922 Compute Add 2 4 2
923 ComputeI NEq 3 33 6
924 Compute Incr 3 0 3
925 Branch 6 (Rel (-5))
926 Compute Equal 2 0 6
927 Branch 6 (Rel 2)
928 Jump (Rel (-10))
929 Load (ImmValue 37) 2
930 TestAndSet (IndAddr 2)
931 Receive 3
```

```
932 Branch 3 (Rel 2)
933 Jump (Rel (-4))
934 Load (ImmValue 38) 4
935 ReadInstr (IndAddr 4)
936 Receive 5
937 Push 5
938 WriteInstr 0 (IndAddr 2)
939 Load (ImmValue 33) 2
940 TestAndSet (IndAddr 2)
941 Receive 3
942 Branch 3 (Rel 2)
943 Jump (Rel (-4))
944 Load (ImmValue 34) 4
945 ReadInstr (IndAddr 4)
946 Receive 5
947 Push 5
948 WriteInstr 0 (IndAddr 2)
949 Load (ImmValue 35) 2
950 TestAndSet (IndAddr 2)
951 Receive 3
952 Branch 3 (Rel 2)
953 Jump (Rel (-4))
954 Load (ImmValue 36) 4
955 ReadInstr (IndAddr 4)
956 Receive 5
957 Push 5
958 WriteInstr 0 (IndAddr 2)
959 Pop 6
960 PrintOut 6
961 Pop 6
962 PrintOut 6
963 Pop 6
964 PrintOut 6
965 TestAndSet (DirAddr 1)
966 Receive 6
967 Branch 6 (Rel 2)
968 Jump (Rel (-3))
969 Load (ImmValue 300) 6
970 Push 6
971 Load (ImmValue 33) 2
972 TestAndSet (IndAddr 2)
973 Receive 3
974 Branch 3 (Rel 2)
975 Jump (Rel (-4))
976 Load (ImmValue 34) 4
977 ReadInstr (IndAddr 4)
978 Receive 5
979 Push 5
```

```
980 WriteInstr 0 (IndAddr 2)
981 Load (ImmValue 5) 4
982 Pop 3
983 WriteInstr 3 (IndAddr 4)
984 Compute Incr 4 0 4
985 Load (ImmValue (-1)) 3
986 WriteInstr 3 (IndAddr 4)
987 Compute Incr 4 0 4
988 Load (ImmValue 33) 3
989 WriteInstr 3 (IndAddr 4)
990 Compute Incr 4 0 4
991 Pop 3
992 WriteInstr 3 (IndAddr 4)
993 Compute Incr 4 0 4
994 Load (ImmValue (-1)) 3
995 WriteInstr 3 (IndAddr 4)
996 Compute Incr 4 0 4
997 Load (ImmValue (-1)) 3
998 WriteInstr 3 (IndAddr 4)
999 Compute Incr 4 0 4
1000 Load (ImmValue 2) 5
1001 WriteInstr 5 (DirAddr 4)
1002 Load (ImmValue 125) 6
1003 Push 6
1004 Pop 5
1005 WriteInstr 5 (DirAddr 3)
1006 WriteInstr 0 (DirAddr 2)
1007 Load (ImmValue 1) 3
1008 ReadInstr (IndAddr 3)
1009 Receive 6
1010 Branch 6 (Rel 2)
1011 Jump (Rel (-3))
1012 TestAndSet (DirAddr 1)
1013 Receive 6
1014 Branch 6 (Rel 2)
1015 Jump (Rel (-3))
1016 Load (ImmValue 30000) 6
1017 Push 6
1018 Load (ImmValue 35) 2
1019 TestAndSet (IndAddr 2)
1020 Receive 3
1021 Branch 3 (Rel 2)
1022 Jump (Rel (-4))
1023 Load (ImmValue 36) 4
1024 ReadInstr (IndAddr 4)
1025 Receive 5
1026 Push 5
1027 WriteInstr 0 (IndAddr 2)
```

```
1028 Load (ImmValue 5) 4
1029 Pop 3
1030 WriteInstr 3 (IndAddr 4)
1031 Compute Incr 4 0 4
1032 Load (ImmValue (-1)) 3
1033 WriteInstr 3 (IndAddr 4)
1034 Compute Incr 4 0 4
1035 Load (ImmValue 35) 3
1036 WriteInstr 3 (IndAddr 4)
1037 Compute Incr 4 0 4
1038 Pop 3
1039 WriteInstr 3 (IndAddr 4)
1040 Compute Incr 4 0 4
1041 Load (ImmValue (-1)) 3
1042 WriteInstr 3 (IndAddr 4)
1043 Compute Incr 4 0 4
1044 Load (ImmValue (-1)) 3
1045 WriteInstr 3 (IndAddr 4)
1046 Compute Incr 4 0 4
1047 Load (ImmValue 2) 5
1048 WriteInstr 5 (DirAddr 4)
1049 Load (ImmValue 125) 6
1050 Push 6
1051 Pop 5
1052 WriteInstr 5 (DirAddr 3)
1053 WriteInstr 0 (DirAddr 2)
1054 Load (ImmValue 1) 3
1055 ReadInstr (IndAddr 3)
1056 Receive 6
1057 Branch 6 (Rel 2)
1058 Jump (Rel (-3))
1059 TestAndSet (DirAddr 1)
1060 Receive 6
1061 Branch 6 (Rel 2)
1062 Jump (Rel (-3))
1063 Load (ImmValue 50) 6
1064 Push 6
1065 Load (ImmValue 37) 2
1066 TestAndSet (IndAddr 2)
1067 Receive 3
1068 Branch 3 (Rel 2)
1069 Jump (Rel (-4))
1070 Load (ImmValue 38) 4
1071 ReadInstr (IndAddr 4)
1072 Receive 5
1073 Push 5
1074 WriteInstr 0 (IndAddr 2)
1075 Load (ImmValue 5) 4
```

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1076 Pop 3
1077 WriteInstr 3 (IndAddr 4)
1078 Compute Incr 4 0 4
1079 Load (ImmValue (-1)) 3
1080 WriteInstr 3 (IndAddr 4)
1081 Compute Incr 4 0 4
1082 Load (ImmValue 37) 3
1083 WriteInstr 3 (IndAddr 4)
1084 Compute Incr 4 0 4
1085 Pop 3
1086 WriteInstr 3 (IndAddr 4)
1087 Compute Incr 4 0 4
1088 Load (ImmValue (-1)) 3
1089 WriteInstr 3 (IndAddr 4)
1090 Compute Incr 4 0 4
1091 Load (ImmValue (-1)) 3
1092 WriteInstr 3 (IndAddr 4)
1093 Compute Incr 4 0 4
1094 Load (ImmValue 2) 5
1095 WriteInstr 5 (DirAddr 4)
1096 Load (ImmValue 125) 6
1097 Push 6
1098 Pop 5
1099 WriteInstr 5 (DirAddr 3)
1100 WriteInstr 0 (DirAddr 2)
1101 Load (ImmValue 1) 3
1102 ReadInstr (IndAddr 3)
1103 Receive 6
1104 Branch 6 (Rel 2)
1105 Jump (Rel (-3))
1106 Compute Equal 0 1 6
1107 Branch 6 (Rel 4)
1108 Load (ImmValue 2) 2
1109 PrintOut 2
1110 EndProg
1111 Load (ImmValue 30) 3
1112 Load (ImmValue 0) 2
1113 ReadInstr (IndAddr 3)
1114 Receive 4
1115 Compute Add 2 4 2
1116 ComputeI NEq 3 33 6
1117 Compute Incr 3 0 3
1118 Branch 6 (Rel (-5))
1119 Compute Equal 2 0 6
1120 Branch 6 (Rel 2)
1121 Jump (Rel (-10))
1122 Load (ImmValue 37) 2
1123 TestAndSet (IndAddr 2)
```



```
1124 Receive 3
1125 Branch 3 (Rel 2)
1126 Jump (Rel (-4))
1127 Load (ImmValue 38) 4
1128 ReadInstr (IndAddr 4)
1129 Receive 5
1130 Push 5
1131 WriteInstr 0 (IndAddr 2)
1132 Load (ImmValue 33) 2
1133 TestAndSet (IndAddr 2)
1134 Receive 3
1135 Branch 3 (Rel 2)
1136 Jump (Rel (-4))
1137 Load (ImmValue 34) 4
1138 ReadInstr (IndAddr 4)
1139 Receive 5
1140 Push 5
1141 WriteInstr 0 (IndAddr 2)
1142 Load (ImmValue 35) 2
1143 TestAndSet (IndAddr 2)
1144 Receive 3
1145 Branch 3 (Rel 2)
1146 Jump (Rel (-4))
1147 Load (ImmValue 36) 4
1148 ReadInstr (IndAddr 4)
1149 Receive 5
1150 Push 5
1151 WriteInstr 0 (IndAddr 2)
1152 Pop 6
1153 PrintOut 6
1154 Pop 6
1155 PrintOut 6
1156 Pop 6
1157 PrintOut 6
1158 TestAndSet (DirAddr 1)
1159 Receive 6
1160 Branch 6 (Rel 2)
1161 Jump (Rel (-3))
1162 Load (ImmValue 35) 6
1163 Push 6
1164 Load (ImmValue 33) 2
1165 TestAndSet (IndAddr 2)
1166 Receive 3
1167 Branch 3 (Rel 2)
1168 Jump (Rel (-4))
1169 Load (ImmValue 34) 4
1170 ReadInstr (IndAddr 4)
1171 Receive 5
```

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1172 Push 5
1173 WriteInstr 0 (IndAddr 2)
1174 Load (ImmValue 5) 4
1175 Pop 3
1176 WriteInstr 3 (IndAddr 4)
1177 Compute Incr 4 0 4
1178 Load (ImmValue (-1)) 3
1179 WriteInstr 3 (IndAddr 4)
1180 Compute Incr 4 0 4
1181 Load (ImmValue 33) 3
1182 WriteInstr 3 (IndAddr 4)
1183 Compute Incr 4 0 4
1184 Pop 3
1185 WriteInstr 3 (IndAddr 4)
1186 Compute Incr 4 0 4
1187 Load (ImmValue (-1)) 3
1188 WriteInstr 3 (IndAddr 4)
1189 Compute Incr 4 0 4
1190 Load (ImmValue (-1)) 3
1191 WriteInstr 3 (IndAddr 4)
1192 Compute Incr 4 0 4
1193 Load (ImmValue 2) 5
1194 WriteInstr 5 (DirAddr 4)
1195 Load (ImmValue 125) 6
1196 Push 6
1197 Pop 5
1198 WriteInstr 5 (DirAddr 3)
1199 WriteInstr 0 (DirAddr 2)
1200 Load (ImmValue 1) 3
1201 ReadInstr (IndAddr 3)
1202 Receive 6
1203 Branch 6 (Rel 2)
1204 Jump (Rel (-3))
1205 TestAndSet (DirAddr 1)
1206 Receive 6
1207 Branch 6 (Rel 2)
1208 Jump (Rel (-3))
1209 Load (ImmValue 1000) 6
1210 Push 6
1211 Load (ImmValue 35) 2
1212 TestAndSet (IndAddr 2)
1213 Receive 3
1214 Branch 3 (Rel 2)
1215 Jump (Rel (-4))
1216 Load (ImmValue 36) 4
1217 ReadInstr (IndAddr 4)
1218 Receive 5
1219 Push 5
```

```
1220 WriteInstr 0 (IndAddr 2)
1221 Load (ImmValue 37) 2
1222 TestAndSet (IndAddr 2)
1223 Receive 3
1224 Branch 3 (Rel 2)
1225 Jump (Rel (-4))
1226 Load (ImmValue 38) 4
1227 ReadInstr (IndAddr 4)
1228 Receive 5
1229 Push 5
1230 WriteInstr 0 (IndAddr 2)
1231 Load (ImmValue 5) 4
1232 Pop 3
1233 WriteInstr 3 (IndAddr 4)
1234 Compute Incr 4 0 4
1235 Load (ImmValue (-1)) 3
1236 WriteInstr 3 (IndAddr 4)
1237 Compute Incr 4 0 4
1238 Load (ImmValue 37) 3
1239 WriteInstr 3 (IndAddr 4)
1240 Compute Incr 4 0 4
1241 Pop 3
1242 WriteInstr 3 (IndAddr 4)
1243 Compute Incr 4 0 4
1244 Load (ImmValue (-1)) 3
1245 WriteInstr 3 (IndAddr 4)
1246 Compute Incr 4 0 4
1247 Load (ImmValue 35) 3
1248 WriteInstr 3 (IndAddr 4)
1249 Compute Incr 4 0 4
1250 Pop 3
1251 WriteInstr 3 (IndAddr 4)
1252 Compute Incr 4 0 4
1253 Load (ImmValue (-1)) 3
1254 WriteInstr 3 (IndAddr 4)
1255 Compute Incr 4 0 4
1256 Load (ImmValue (-1)) 3
1257 WriteInstr 3 (IndAddr 4)
1258 Compute Incr 4 0 4
1259 Load (ImmValue 3) 5
1260 WriteInstr 5 (DirAddr 4)
1261 Load (ImmValue 218) 6
1262 Push 6
1263 Pop 5
1264 WriteInstr 5 (DirAddr 3)
1265 WriteInstr 0 (DirAddr 2)
1266 Load (ImmValue 1) 3
1267 ReadInstr (IndAddr 3)
```

```
1268 Receive 6
1269 Branch 6 (Rel 2)
1270 Jump (Rel (-3))
1271 Compute Equal 0 1 6
1272 Branch 6 (Rel 4)
1273 Load (ImmValue 2) 2
1274 PrintOut 2
1275 EndProg
1276 Load (ImmValue 30) 3
1277 Load (ImmValue 0) 2
1278 ReadInstr (IndAddr 3)
1279 Receive 4
1280 Compute Add 2 4 2
1281 ComputeI NEq 3 33 6
1282 Compute Incr 3 0 3
1283 Branch 6 (Rel (-5))
1284 Compute Equal 2 0 6
1285 Branch 6 (Rel 2)
1286 Jump (Rel (-10))
1287 Load (ImmValue 37) 2
1288 TestAndSet (IndAddr 2)
1289 Receive 3
1290 Branch 3 (Rel 2)
1291 Jump (Rel (-4))
1292 Load (ImmValue 38) 4
1293 ReadInstr (IndAddr 4)
1294 Receive 5
1295 Push 5
1296 WriteInstr 0 (IndAddr 2)
1297 Load (ImmValue 33) 2
1298 TestAndSet (IndAddr 2)
1299 Receive 3
1300 Branch 3 (Rel 2)
1301 Jump (Rel (-4))
1302 Load (ImmValue 34) 4
1303 ReadInstr (IndAddr 4)
1304 Receive 5
1305 Push 5
1306 WriteInstr 0 (IndAddr 2)
1307 Load (ImmValue 35) 2
1308 TestAndSet (IndAddr 2)
1309 Receive 3
1310 Branch 3 (Rel 2)
1311 Jump (Rel (-4))
1312 Load (ImmValue 36) 4
1313 ReadInstr (IndAddr 4)
1314 Receive 5
1315 Push 5
```

```
1316 WriteInstr 0 (IndAddr 2)
1317 Pop 6
1318 PrintOut 6
1319 Pop 6
1320 PrintOut 6
1321 Pop 6
1322 PrintOut 6
1323 TestAndSet (DirAddr 1)
1324 Receive 6
1325 Branch 6 (Rel 2)
1326 Jump (Rel (-3))
1327 Load (ImmValue 100) 6
1328 Push 6
1329 Load (ImmValue 33) 2
1330 TestAndSet (IndAddr 2)
1331 Receive 3
1332 Branch 3 (Rel 2)
1333 Jump (Rel (-4))
1334 Load (ImmValue 34) 4
1335 ReadInstr (IndAddr 4)
1336 Receive 5
1337 Push 5
1338 WriteInstr 0 (IndAddr 2)
1339 Load (ImmValue 37) 2
1340 TestAndSet (IndAddr 2)
1341 Receive 3
1342 Branch 3 (Rel 2)
1343 Jump (Rel (-4))
1344 Load (ImmValue 38) 4
1345 ReadInstr (IndAddr 4)
1346 Receive 5
1347 Push 5
1348 WriteInstr 0 (IndAddr 2)
1349 Load (ImmValue 5) 4
1350 Pop 3
1351 WriteInstr 3 (IndAddr 4)
1352 Compute Incr 4 0 4
1353 Load (ImmValue (-1)) 3
1354 WriteInstr 3 (IndAddr 4)
1355 Compute Incr 4 0 4
1356 Load (ImmValue 37) 3
1357 WriteInstr 3 (IndAddr 4)
1358 Compute Incr 4 0 4
1359 Pop 3
1360 WriteInstr 3 (IndAddr 4)
1361 Compute Incr 4 0 4
1362 Load (ImmValue (-1)) 3
1363 WriteInstr 3 (IndAddr 4)
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1364 Compute Incr 4 0 4
1365 Load (ImmValue 33) 3
1366 WriteInstr 3 (IndAddr 4)
1367 Compute Incr 4 0 4
1368 Pop 3
1369 WriteInstr 3 (IndAddr 4)
1370 Compute Incr 4 0 4
1371 Load (ImmValue (-1)) 3
1372 WriteInstr 3 (IndAddr 4)
1373 Compute Incr 4 0 4
1374 Load (ImmValue (-1)) 3
1375 WriteInstr 3 (IndAddr 4)
1376 Compute Incr 4 0 4
1377 Load (ImmValue 3) 5
1378 WriteInstr 5 (DirAddr 4)
1379 Load (ImmValue 218) 6
1380 Push 6
1381 Pop 5
1382 WriteInstr 5 (DirAddr 3)
1383 WriteInstr 0 (DirAddr 2)
1384 Load (ImmValue 1) 3
1385 ReadInstr (IndAddr 3)
1386 Receive 6
1387 Branch 6 (Rel 2)
1388 Jump (Rel (-3))
1389 Compute Equal 0 1 6
1390 Branch 6 (Rel 4)
1391 Load (ImmValue 2) 2
1392 PrintOut 2
1393 EndProg
1394 Load (ImmValue 30) 3
1395 Load (ImmValue 0) 2
1396 ReadInstr (IndAddr 3)
1397 Receive 4
1398 Compute Add 2 4 2
1399 ComputeI NEq 3 33 6
1400 Compute Incr 3 0 3
1401 Branch 6 (Rel (-5))
1402 Compute Equal 2 0 6
1403 Branch 6 (Rel 2)
1404 Jump (Rel (-10))
1405 Load (ImmValue 37) 2
1406 TestAndSet (IndAddr 2)
1407 Receive 3
1408 Branch 3 (Rel 2)
1409 Jump (Rel (-4))
1410 Load (ImmValue 38) 4
1411 ReadInstr (IndAddr 4)
```

```
1412 Receive 5
1413 Push 5
1414 WriteInstr 0 (IndAddr 2)
1415 Load (ImmValue 33) 2
1416 TestAndSet (IndAddr 2)
1417 Receive 3
1418 Branch 3 (Rel 2)
1419 Jump (Rel (-4))
1420 Load (ImmValue 34) 4
1421 ReadInstr (IndAddr 4)
1422 Receive 5
1423 Push 5
1424 WriteInstr 0 (IndAddr 2)
1425 Load (ImmValue 35) 2
1426 TestAndSet (IndAddr 2)
1427 Receive 3
1428 Branch 3 (Rel 2)
1429 Jump (Rel (-4))
1430 Load (ImmValue 36) 4
1431 ReadInstr (IndAddr 4)
1432 Receive 5
1433 Push 5
1434 WriteInstr 0 (IndAddr 2)
1435 Pop 6
1436 PrintOut 6
1437 Pop 6
1438 PrintOut 6
1439 Pop 6
1440 PrintOut 6
1441 Load (IndAddr 7) 7
1442 Load (ImmValue 0) 2
1443 Compute Sub 7 2 2
1444 ComputeI Add 0 1 5
1445 ComputeI Gt 5 0 6
1446 Branch 6 (Rel 23)
1447 Compute Add 7 5 6
1448 Load (IndAddr 6) 4
1449 Load (IndAddr 2) 3
1450 Compute Lt 3 0 6
1451 Branch 6 (Rel 2)
1452 Store 4 (IndAddr 3)
1453 Compute Incr 2 0 2
1454 Load (IndAddr 2) 3
1455 Compute Lt 3 0 6
1456 Branch 6 (Rel 10)
1457 Compute Add 3 0 6
1458 TestAndSet (IndAddr 6)
1459 Receive 6
```

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1460 Branch 6 (Rel 2)
1461 Jump (Rel (-4))
1462 ComputeI Add 3 1 3
1463 WriteInstr 4 (IndAddr 3)
1464 ComputeI Sub 3 1 3
1465 WriteInstr 0 (IndAddr 3)
1466 Compute Incr 5 0 5
1467 ComputeI Add 2 2 2
1468 Jump (Rel (-23))
1469 Compute Decr 7 0 2
1470 Load (IndAddr 2) 6
1471 Load (IndAddr 7) 7
1472 Jump (Ind 6)
1473 Nop
1474 Nop
1475 Load (ImmValue 10000) 6
1476 Push 6
1477 Pop 6
1478 Load (ImmValue 35) 2
1479 TestAndSet (IndAddr 2)
1480 Receive 3
1481 Branch 3 (Rel 2)
1482 Jump (Rel (-3))
1483 Load (ImmValue 36) 4
1484 WriteInstr 6 (IndAddr 4)
1485 WriteInstr 0 (IndAddr 2)
1486 Load (ImmValue 2000) 6
1487 Push 6
1488 Pop 6
1489 Load (ImmValue 33) 2
1490 TestAndSet (IndAddr 2)
1491 Receive 3
1492 Branch 3 (Rel 2)
1493 Jump (Rel (-3))
1494 Load (ImmValue 34) 4
1495 WriteInstr 6 (IndAddr 4)
1496 WriteInstr 0 (IndAddr 2)
1497 Load (ImmValue 99999) 6
1498 Push 6
1499 Pop 6
1500 Load (ImmValue 37) 2
1501 TestAndSet (IndAddr 2)
1502 Receive 3
1503 Branch 3 (Rel 2)
1504 Jump (Rel (-3))
1505 Load (ImmValue 38) 4
1506 WriteInstr 6 (IndAddr 4)
1507 WriteInstr 0 (IndAddr 2)
```



```
1508 Compute Add 7 0 4
1509 ComputeI Add 4 1 4
1510 Load (ImmValue 0) 5
1511 Load (ImmValue 1522) 6
1512 Push 6
1513 Pop 5
1514 Store 5 (IndAddr 4)
1515 Compute Incr 4 0 4
1516 Store 7 (IndAddr 4)
1517 Compute Add 4 0 7
1518 Load (ImmValue 335) 6
1519 Push 6
1520 Pop 2
1521 Jump (Ind 2)
1522 Load (ImmValue 1) 2
1523 WriteInstr 2 (DirAddr 0)
1524 EndProg
```

## Results

```
1 >>> 10000
2 >>> 2000
3 >>> 99999
4 >>> 10100
5 >>> 2100
6 >>> 100000
7 >>> 9900
8 >>> 2300
9 >>> 102000
10 >>> 9880
11 >>> 2290
12 >>> 102100
13 >>> 9880
14 >>> 1990
15 >>> 102050
16 >>> 10880
17 >>> 1955
18 >>> 101050
19 >>> 10880
20 >>> 2055
21 >>> 100950
```

## Blocks

### Source

```
1 int x = 1;
2 int y = 100;
```

```
3  bool a = false;
4  bool b = false;
5  print(x,y,a,b);
6  {
7      int x = 2;
8      int y = 120;
9      bool a = true;
10     bool b = false;
11     print(x,y,a,b);
12     { }
13     int x = 3;
14     int y = 123;
15     bool a = false;
16     bool b = true;
17     print(x,y,a,b);
18     {
19         int x = 4;
20         int y = 423;
21         bool a = true;
22         bool b = true;
23         print(x,y,a,b);
24     }
25     print(x,y,a,b);
26     {
27         int x = 5;
28         int y = 453;
29         bool a = true;
30         bool b = false;
31         print(x,y,a,b);
32         {
33             int x = 5;
34             int y = 453;
35             bool a = false;
36             bool b = true;
37             print(x,y,a,b);
38         }
39         print(x,y,a,b);
40         {
41             int x = 6;
42             int y = 456;
43             bool a = false;
44             bool b = false;
45             print(x,y,a,b);
46         }
47         print(x,y,a,b);
48     }
49     print(x,y,a,b);
50 }
```

```
51     print(x,y,a,b);
52     {
53         print(x,y,a,b);
54         {
55             print(x,y,a,b);
56         }
57     }
58     print(x,y,a,b);
59 }
60 print(x,y,a,b);
```

## Generated SprIL

```
0  Branch 1 (Rel 6)
1  TestAndSet (DirAddr 2)
2  Receive 6
3  Branch 6 (Rel 2)
4  Jump (Rel (-3))
5  Jump (Rel 54)
6  ReadInstr (DirAddr 0)
7  Receive 3
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
```

```
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Nop
58 Nop
59 Load (ImmValue 1) 6
60 Push 6
61 Compute Add 7 0 6
62 ComputeI Add 6 1 6
63 Pop 5
64 Store 5 (IndAddr 6)
65 Load (ImmValue 100) 6
66 Push 6
67 Compute Add 7 0 6
68 ComputeI Add 6 2 6
69 Pop 5
70 Store 5 (IndAddr 6)
71 Load (ImmValue 0) 6
72 Push 6
73 Compute Add 7 0 6
74 ComputeI Add 6 3 6
75 Pop 5
76 Store 5 (IndAddr 6)
77 Load (ImmValue 0) 6
78 Push 6
79 Compute Add 7 0 6
80 ComputeI Add 6 4 6
81 Pop 5
82 Store 5 (IndAddr 6)
```

```
83 Compute Add 7 0 6
84 ComputeI Add 6 4 6
85 Load (IndAddr 6) 5
86 Push 5
87 Compute Add 7 0 6
88 ComputeI Add 6 3 6
89 Load (IndAddr 6) 5
90 Push 5
91 Compute Add 7 0 6
92 ComputeI Add 6 2 6
93 Load (IndAddr 6) 5
94 Push 5
95 Compute Add 7 0 6
96 ComputeI Add 6 1 6
97 Load (IndAddr 6) 5
98 Push 5
99 Pop 6
100 PrintOut 6
101 Pop 6
102 PrintOut 6
103 Pop 6
104 PrintOut 6
105 Pop 6
106 PrintOut 6
107 Compute Add 7 0 4
108 ComputeI Add 4 5 4
109 Store 7 (IndAddr 4)
110 Compute Add 4 0 7
111 Load (ImmValue 2) 6
112 Push 6
113 Compute Add 7 0 6
114 ComputeI Add 6 1 6
115 Pop 5
116 Store 5 (IndAddr 6)
117 Load (ImmValue 120) 6
118 Push 6
119 Compute Add 7 0 6
120 ComputeI Add 6 2 6
121 Pop 5
122 Store 5 (IndAddr 6)
123 Load (ImmValue 1) 6
124 Push 6
125 Compute Add 7 0 6
126 ComputeI Add 6 3 6
127 Pop 5
128 Store 5 (IndAddr 6)
129 Load (ImmValue 0) 6
130 Push 6
```

```
131 Compute Add 7 0 6
132 ComputeI Add 6 4 6
133 Pop 5
134 Store 5 (IndAddr 6)
135 Compute Add 7 0 6
136 ComputeI Add 6 4 6
137 Load (IndAddr 6) 5
138 Push 5
139 Compute Add 7 0 6
140 ComputeI Add 6 3 6
141 Load (IndAddr 6) 5
142 Push 5
143 Compute Add 7 0 6
144 ComputeI Add 6 2 6
145 Load (IndAddr 6) 5
146 Push 5
147 Compute Add 7 0 6
148 ComputeI Add 6 1 6
149 Load (IndAddr 6) 5
150 Push 5
151 Pop 6
152 PrintOut 6
153 Pop 6
154 PrintOut 6
155 Pop 6
156 PrintOut 6
157 Pop 6
158 PrintOut 6
159 Compute Add 7 0 4
160 ComputeI Add 4 5 4
161 Store 7 (IndAddr 4)
162 Compute Add 4 0 7
163 Compute Add 7 0 4
164 ComputeI Add 4 1 4
165 Store 7 (IndAddr 4)
166 Compute Add 4 0 7
167 Load (IndAddr 7) 7
168 Load (ImmValue 3) 6
169 Push 6
170 Compute Add 7 0 6
171 ComputeI Add 6 1 6
172 Pop 5
173 Store 5 (IndAddr 6)
174 Load (ImmValue 123) 6
175 Push 6
176 Compute Add 7 0 6
177 ComputeI Add 6 2 6
178 Pop 5
```

```
179 Store 5 (IndAddr 6)
180 Load (ImmValue 0) 6
181 Push 6
182 Compute Add 7 0 6
183 ComputeI Add 6 3 6
184 Pop 5
185 Store 5 (IndAddr 6)
186 Load (ImmValue 1) 6
187 Push 6
188 Compute Add 7 0 6
189 ComputeI Add 6 4 6
190 Pop 5
191 Store 5 (IndAddr 6)
192 Compute Add 7 0 6
193 ComputeI Add 6 4 6
194 Load (IndAddr 6) 5
195 Push 5
196 Compute Add 7 0 6
197 ComputeI Add 6 3 6
198 Load (IndAddr 6) 5
199 Push 5
200 Compute Add 7 0 6
201 ComputeI Add 6 2 6
202 Load (IndAddr 6) 5
203 Push 5
204 Compute Add 7 0 6
205 ComputeI Add 6 1 6
206 Load (IndAddr 6) 5
207 Push 5
208 Pop 6
209 PrintOut 6
210 Pop 6
211 PrintOut 6
212 Pop 6
213 PrintOut 6
214 Pop 6
215 PrintOut 6
216 Compute Add 7 0 4
217 ComputeI Add 4 5 4
218 Store 7 (IndAddr 4)
219 Compute Add 4 0 7
220 Load (ImmValue 4) 6
221 Push 6
222 Compute Add 7 0 6
223 ComputeI Add 6 1 6
224 Pop 5
225 Store 5 (IndAddr 6)
226 Load (ImmValue 423) 6
```

```
227 Push 6
228 Compute Add 7 0 6
229 ComputeI Add 6 2 6
230 Pop 5
231 Store 5 (IndAddr 6)
232 Load (ImmValue 1) 6
233 Push 6
234 Compute Add 7 0 6
235 ComputeI Add 6 3 6
236 Pop 5
237 Store 5 (IndAddr 6)
238 Load (ImmValue 1) 6
239 Push 6
240 Compute Add 7 0 6
241 ComputeI Add 6 4 6
242 Pop 5
243 Store 5 (IndAddr 6)
244 Compute Add 7 0 6
245 ComputeI Add 6 4 6
246 Load (IndAddr 6) 5
247 Push 5
248 Compute Add 7 0 6
249 ComputeI Add 6 3 6
250 Load (IndAddr 6) 5
251 Push 5
252 Compute Add 7 0 6
253 ComputeI Add 6 2 6
254 Load (IndAddr 6) 5
255 Push 5
256 Compute Add 7 0 6
257 ComputeI Add 6 1 6
258 Load (IndAddr 6) 5
259 Push 5
260 Pop 6
261 PrintOut 6
262 Pop 6
263 PrintOut 6
264 Pop 6
265 PrintOut 6
266 Pop 6
267 PrintOut 6
268 Load (IndAddr 7) 7
269 Compute Add 7 0 6
270 ComputeI Add 6 4 6
271 Load (IndAddr 6) 5
272 Push 5
273 Compute Add 7 0 6
274 ComputeI Add 6 3 6
```



```
275 Load (IndAddr 6) 5
276 Push 5
277 Compute Add 7 0 6
278 ComputeI Add 6 2 6
279 Load (IndAddr 6) 5
280 Push 5
281 Compute Add 7 0 6
282 ComputeI Add 6 1 6
283 Load (IndAddr 6) 5
284 Push 5
285 Pop 6
286 PrintOut 6
287 Pop 6
288 PrintOut 6
289 Pop 6
290 PrintOut 6
291 Pop 6
292 PrintOut 6
293 Compute Add 7 0 4
294 ComputeI Add 4 5 4
295 Store 7 (IndAddr 4)
296 Compute Add 4 0 7
297 Load (ImmValue 5) 6
298 Push 6
299 Compute Add 7 0 6
300 ComputeI Add 6 1 6
301 Pop 5
302 Store 5 (IndAddr 6)
303 Load (ImmValue 453) 6
304 Push 6
305 Compute Add 7 0 6
306 ComputeI Add 6 2 6
307 Pop 5
308 Store 5 (IndAddr 6)
309 Load (ImmValue 1) 6
310 Push 6
311 Compute Add 7 0 6
312 ComputeI Add 6 3 6
313 Pop 5
314 Store 5 (IndAddr 6)
315 Load (ImmValue 0) 6
316 Push 6
317 Compute Add 7 0 6
318 ComputeI Add 6 4 6
319 Pop 5
320 Store 5 (IndAddr 6)
321 Compute Add 7 0 6
322 ComputeI Add 6 4 6
```

```
323 Load (IndAddr 6) 5
324 Push 5
325 Compute Add 7 0 6
326 ComputeI Add 6 3 6
327 Load (IndAddr 6) 5
328 Push 5
329 Compute Add 7 0 6
330 ComputeI Add 6 2 6
331 Load (IndAddr 6) 5
332 Push 5
333 Compute Add 7 0 6
334 ComputeI Add 6 1 6
335 Load (IndAddr 6) 5
336 Push 5
337 Pop 6
338 PrintOut 6
339 Pop 6
340 PrintOut 6
341 Pop 6
342 PrintOut 6
343 Pop 6
344 PrintOut 6
345 Compute Add 7 0 4
346 ComputeI Add 4 5 4
347 Store 7 (IndAddr 4)
348 Compute Add 4 0 7
349 Load (ImmValue 5) 6
350 Push 6
351 Compute Add 7 0 6
352 ComputeI Add 6 1 6
353 Pop 5
354 Store 5 (IndAddr 6)
355 Load (ImmValue 453) 6
356 Push 6
357 Compute Add 7 0 6
358 ComputeI Add 6 2 6
359 Pop 5
360 Store 5 (IndAddr 6)
361 Load (ImmValue 0) 6
362 Push 6
363 Compute Add 7 0 6
364 ComputeI Add 6 3 6
365 Pop 5
366 Store 5 (IndAddr 6)
367 Load (ImmValue 1) 6
368 Push 6
369 Compute Add 7 0 6
370 ComputeI Add 6 4 6
```

```
371 Pop 5
372 Store 5 (IndAddr 6)
373 Compute Add 7 0 6
374 ComputeI Add 6 4 6
375 Load (IndAddr 6) 5
376 Push 5
377 Compute Add 7 0 6
378 ComputeI Add 6 3 6
379 Load (IndAddr 6) 5
380 Push 5
381 Compute Add 7 0 6
382 ComputeI Add 6 2 6
383 Load (IndAddr 6) 5
384 Push 5
385 Compute Add 7 0 6
386 ComputeI Add 6 1 6
387 Load (IndAddr 6) 5
388 Push 5
389 Pop 6
390 PrintOut 6
391 Pop 6
392 PrintOut 6
393 Pop 6
394 PrintOut 6
395 Pop 6
396 PrintOut 6
397 Load (IndAddr 7) 7
398 Compute Add 7 0 6
399 ComputeI Add 6 4 6
400 Load (IndAddr 6) 5
401 Push 5
402 Compute Add 7 0 6
403 ComputeI Add 6 3 6
404 Load (IndAddr 6) 5
405 Push 5
406 Compute Add 7 0 6
407 ComputeI Add 6 2 6
408 Load (IndAddr 6) 5
409 Push 5
410 Compute Add 7 0 6
411 ComputeI Add 6 1 6
412 Load (IndAddr 6) 5
413 Push 5
414 Pop 6
415 PrintOut 6
416 Pop 6
417 PrintOut 6
418 Pop 6
```

```
419 PrintOut 6
420 Pop 6
421 PrintOut 6
422 Compute Add 7 0 4
423 ComputeI Add 4 5 4
424 Store 7 (IndAddr 4)
425 Compute Add 4 0 7
426 Load (ImmValue 6) 6
427 Push 6
428 Compute Add 7 0 6
429 ComputeI Add 6 1 6
430 Pop 5
431 Store 5 (IndAddr 6)
432 Load (ImmValue 456) 6
433 Push 6
434 Compute Add 7 0 6
435 ComputeI Add 6 2 6
436 Pop 5
437 Store 5 (IndAddr 6)
438 Load (ImmValue 0) 6
439 Push 6
440 Compute Add 7 0 6
441 ComputeI Add 6 3 6
442 Pop 5
443 Store 5 (IndAddr 6)
444 Load (ImmValue 0) 6
445 Push 6
446 Compute Add 7 0 6
447 ComputeI Add 6 4 6
448 Pop 5
449 Store 5 (IndAddr 6)
450 Compute Add 7 0 6
451 ComputeI Add 6 4 6
452 Load (IndAddr 6) 5
453 Push 5
454 Compute Add 7 0 6
455 ComputeI Add 6 3 6
456 Load (IndAddr 6) 5
457 Push 5
458 Compute Add 7 0 6
459 ComputeI Add 6 2 6
460 Load (IndAddr 6) 5
461 Push 5
462 Compute Add 7 0 6
463 ComputeI Add 6 1 6
464 Load (IndAddr 6) 5
465 Push 5
466 Pop 6
```

```
467 PrintOut 6
468 Pop 6
469 PrintOut 6
470 Pop 6
471 PrintOut 6
472 Pop 6
473 PrintOut 6
474 Load (IndAddr 7) 7
475 Compute Add 7 0 6
476 ComputeI Add 6 4 6
477 Load (IndAddr 6) 5
478 Push 5
479 Compute Add 7 0 6
480 ComputeI Add 6 3 6
481 Load (IndAddr 6) 5
482 Push 5
483 Compute Add 7 0 6
484 ComputeI Add 6 2 6
485 Load (IndAddr 6) 5
486 Push 5
487 Compute Add 7 0 6
488 ComputeI Add 6 1 6
489 Load (IndAddr 6) 5
490 Push 5
491 Pop 6
492 PrintOut 6
493 Pop 6
494 PrintOut 6
495 Pop 6
496 PrintOut 6
497 Pop 6
498 PrintOut 6
499 Load (IndAddr 7) 7
500 Compute Add 7 0 6
501 ComputeI Add 6 4 6
502 Load (IndAddr 6) 5
503 Push 5
504 Compute Add 7 0 6
505 ComputeI Add 6 3 6
506 Load (IndAddr 6) 5
507 Push 5
508 Compute Add 7 0 6
509 ComputeI Add 6 2 6
510 Load (IndAddr 6) 5
511 Push 5
512 Compute Add 7 0 6
513 ComputeI Add 6 1 6
514 Load (IndAddr 6) 5
```

```
515 Push 5
516 Pop 6
517 PrintOut 6
518 Pop 6
519 PrintOut 6
520 Pop 6
```

## Results

```
1 >>> 1
2 >>> 100
3 >>> 0
4 >>> 0
5 >>> 2
6 >>> 120
7 >>> 1
8 >>> 0
9 >>> 3
10 >>> 123
11 >>> 0
12 >>> 1
13 >>> 4
14 >>> 423
15 >>> 1
16 >>> 1
17 >>> 3
18 >>> 123
19 >>> 0
20 >>> 1
21 >>> 5
22 >>> 453
23 >>> 1
24 >>> 0
25 >>> 5
26 >>> 453
27 >>> 0
28 >>> 1
29 >>> 5
30 >>> 453
31 >>> 1
32 >>> 0
33 >>> 6
34 >>> 456
35 >>> 0
36 >>> 0
37 >>> 5
38 >>> 453
39 >>> 1
```

```
40 >>> 0
41 >>> 3
42 >>> 123
43 >>> 0
44 >>> 1
45 >>> 2
46 >>> 120
47 >>> 1
48 >>> 0
49 >>> 2
50 >>> 120
51 >>> 1
52 >>> 0
53 >>> 2
54 >>> 120
55 >>> 1
56 >>> 0
57 >>> 2
58 >>> 120
59 >>> 1
60 >>> 0
61 >>> 1
62 >>> 100
63 >>> 0
64 >>> 0
```

## Call-by-reference

### Source

```
1 global int var = 1337;
2 global int y = 42;
3
4 procedure write(int input, int output) {
5     output = input;
6 }
7
8 print (y);
9 fork write(var, y);
10 join;
11 print(y);
```

### Generated SprIL

```
0 Compute Equal 1 0 6
1 Branch 6 (Rel 2)
2 Jump (Rel 7)
3 TestAndSet (DirAddr 2)
```

```
4  Receive 6
5  Branch 6 (Rel 2)
6  Jump (Rel (-3))
7  Load (ImmValue 0) 7
8  Jump (Rel 111)
9  ReadInstr (DirAddr 0)
10 Receive 3
11 Compute Equal 3 0 6
12 Branch 6 (Rel 2)
13 EndProg
14 TestAndSet (DirAddr 2)
15 Receive 6
16 Branch 6 (Rel 2)
17 Jump (Rel (-8))
18 ComputeI Add 1 30 3
19 TestAndSet (IndAddr 3)
20 Receive 6
21 Branch 6 (Rel 2)
22 Jump (Rel (-3))
23 ReadInstr (DirAddr 3)
24 Receive 3
25 Push 3
26 ComputeI Add 7 1 4
27 ReadInstr (DirAddr 4)
28 Receive 5
29 Load (ImmValue 5) 2
30 Compute Equal 5 0 6
31 Branch 6 (Rel 18)
32 ReadInstr (IndAddr 2)
33 Receive 3
34 Store 3 (IndAddr 4)
35 Compute Incr 2 0 2
36 Compute Incr 4 0 4
37 ReadInstr (IndAddr 2)
38 Receive 3
39 Store 3 (IndAddr 4)
40 Compute Incr 2 0 2
41 Compute Incr 4 0 4
42 ReadInstr (IndAddr 2)
43 Receive 3
44 Store 3 (IndAddr 4)
45 Compute Incr 2 0 2
46 Compute Incr 4 0 4
47 Compute Decr 5 0 5
48 Jump (Rel (-18))
49 Load (ImmValue 57) 5
50 Store 5 (IndAddr 4)
51 Compute Incr 4 0 4
```



```
52 Store 7 (IndAddr 4)
53 Compute Add 4 0 7
54 Pop 2
55 WriteInstr 0 (DirAddr 1)
56 Jump (Ind 2)
57 ComputeI Add 1 30 3
58 WriteInstr 0 (IndAddr 3)
59 Jump (Abs 9)
60 Load (ImmValue 7) 2
61 Compute Sub 7 2 2
62 Load (ImmValue 1) 5
63 ComputeI Gt 5 2 6
64 Branch 6 (Rel 7)
65 Load (IndAddr 2) 3
66 Compute Add 7 5 6
67 Store 3 (IndAddr 6)
68 Compute Incr 5 0 5
69 ComputeI Add 2 3 2
70 Jump (Rel (-7))
71 Compute Add 7 0 4
72 ComputeI Add 4 3 4
73 Store 7 (IndAddr 4)
74 Compute Add 4 0 7
75 Compute Add 7 0 6
76 Load (IndAddr 6) 6
77 ComputeI Add 6 1 6
78 Load (IndAddr 6) 5
79 Push 5
80 Compute Add 7 0 6
81 Load (IndAddr 6) 6
82 ComputeI Add 6 2 6
83 Pop 2
84 Store 2 (IndAddr 6)
85 Push 2
86 Pop 0
87 Load (IndAddr 7) 7
88 Load (ImmValue 6) 2
89 Compute Sub 7 2 2
90 ComputeI Add 0 1 5
91 ComputeI Gt 5 2 6
92 Branch 6 (Rel 23)
93 Compute Add 7 5 6
94 Load (IndAddr 6) 4
95 Load (IndAddr 2) 3
96 Compute Lt 3 0 6
97 Branch 6 (Rel 2)
98 Store 4 (IndAddr 3)
99 Compute Incr 2 0 2
```

```
100 Load (IndAddr 2) 3
101 Compute Lt 3 0 6
102 Branch 6 (Rel 10)
103 Compute Add 3 0 6
104 TestAndSet (IndAddr 6)
105 Receive 6
106 Branch 6 (Rel 2)
107 Jump (Rel (-4))
108 ComputeI Add 3 1 3
109 WriteInstr 4 (IndAddr 3)
110 ComputeI Sub 3 1 3
111 WriteInstr 0 (IndAddr 3)
112 Compute Incr 5 0 5
113 ComputeI Add 2 2 2
114 Jump (Rel (-23))
115 Compute Decr 7 0 2
116 Load (IndAddr 2) 6
117 Load (IndAddr 7) 7
118 Jump (Ind 6)
119 Load (ImmValue 1337) 6
120 Push 6
121 Pop 6
122 Load (ImmValue 32) 2
123 TestAndSet (IndAddr 2)
124 Receive 3
125 Branch 3 (Rel 2)
126 Jump (Rel (-3))
127 Load (ImmValue 33) 4
128 WriteInstr 6 (IndAddr 4)
129 WriteInstr 0 (IndAddr 2)
130 Load (ImmValue 42) 6
131 Push 6
132 Pop 6
133 Load (ImmValue 34) 2
134 TestAndSet (IndAddr 2)
135 Receive 3
136 Branch 3 (Rel 2)
137 Jump (Rel (-3))
138 Load (ImmValue 35) 4
139 WriteInstr 6 (IndAddr 4)
140 WriteInstr 0 (IndAddr 2)
141 Load (ImmValue 34) 2
142 TestAndSet (IndAddr 2)
143 Receive 3
144 Branch 3 (Rel 2)
145 Jump (Rel (-4))
146 Load (ImmValue 35) 4
147 ReadInstr (IndAddr 4)
```

```
148 Receive 5
149 Push 5
150 WriteInstr 0 (IndAddr 2)
151 Pop 6
152 PrintOut 6
153 TestAndSet (DirAddr 1)
154 Receive 6
155 Branch 6 (Rel 2)
156 Jump (Rel (-3))
157 Load (ImmValue 34) 2
158 TestAndSet (IndAddr 2)
159 Receive 3
160 Branch 3 (Rel 2)
161 Jump (Rel (-4))
162 Load (ImmValue 35) 4
163 ReadInstr (IndAddr 4)
164 Receive 5
165 Push 5
166 WriteInstr 0 (IndAddr 2)
167 Load (ImmValue 32) 2
168 TestAndSet (IndAddr 2)
169 Receive 3
170 Branch 3 (Rel 2)
171 Jump (Rel (-4))
172 Load (ImmValue 33) 4
173 ReadInstr (IndAddr 4)
174 Receive 5
175 Push 5
176 WriteInstr 0 (IndAddr 2)
177 Load (ImmValue 5) 4
178 Pop 3
179 WriteInstr 3 (IndAddr 4)
180 Compute Incr 4 0 4
181 Load (ImmValue (-1)) 3
182 WriteInstr 3 (IndAddr 4)
183 Compute Incr 4 0 4
184 Load (ImmValue 32) 3
185 WriteInstr 3 (IndAddr 4)
186 Compute Incr 4 0 4
187 Pop 3
188 WriteInstr 3 (IndAddr 4)
189 Compute Incr 4 0 4
190 Load (ImmValue (-1)) 3
191 WriteInstr 3 (IndAddr 4)
192 Compute Incr 4 0 4
193 Load (ImmValue 34) 3
194 WriteInstr 3 (IndAddr 4)
195 Compute Incr 4 0 4
```

```
196 Load (ImmValue 2) 5
197 WriteInstr 5 (DirAddr 4)
198 Load (ImmValue 60) 6
199 Push 6
200 Pop 5
201 WriteInstr 5 (DirAddr 3)
202 WriteInstr 0 (DirAddr 2)
203 Load (ImmValue 1) 3
204 ReadInstr (IndAddr 3)
205 Receive 6
206 Branch 6 (Rel 2)
207 Jump (Rel (-3))
208 Compute Equal 0 1 6
209 Branch 6 (Rel 4)
210 Load (ImmValue 2) 2
211 PrintOut 2
212 EndProg
213 Load (ImmValue 30) 3
214 Load (ImmValue 0) 2
215 ReadInstr (IndAddr 3)
216 Receive 4
217 Compute Add 2 4 2
218 ComputeI NEq 3 32 6
219 Compute Incr 3 0 3
220 Branch 6 (Rel (-5))
221 Compute Equal 2 0 6
222 Branch 6 (Rel 2)
223 Jump (Rel (-10))
224 Load (ImmValue 34) 2
225 TestAndSet (IndAddr 2)
226 Receive 3
227 Branch 3 (Rel 2)
228 Jump (Rel (-4))
229 Load (ImmValue 35) 4
230 ReadInstr (IndAddr 4)
231 Receive 5
232 Push 5
233 WriteInstr 0 (IndAddr 2)
234 Pop 6
235 PrintOut 6
236 Load (ImmValue 1) 2
237 WriteInstr 2 (DirAddr 0)
238 EndProg
```

## Results

```
1 >>> 42
2 >>> 1337
```

## Cyclic Recursion

### Source

```
1 procedure prod(int i) {
2     i = (i + 1);
3     //print (i);
4     cons(i);
5 }
6
7 procedure cons(int i) {
8     if ((i > 1)) {
9         i = (i - 2);
10        print(i);
11        prod(i);
12    } else if ((i > 0)) {
13        i = (i - 1);
14        print(i);
15    }
16 }
17
18 prod(18);
```

### Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 323)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
```

```
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 4) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 1 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 2 4
70 Store 7 (IndAddr 4)
```

```
71 Compute Add 4 0 7
72 Compute Add 7 0 6
73 Load (IndAddr 6) 6
74 ComputeI Add 6 1 6
75 Load (IndAddr 6) 5
76 Push 5
77 Load (ImmValue 1) 6
78 Push 6
79 Pop 3
80 Pop 2
81 Compute Add 2 3 4
82 Push 4
83 Compute Add 7 0 6
84 Load (IndAddr 6) 6
85 ComputeI Add 6 1 6
86 Pop 2
87 Store 2 (IndAddr 6)
88 Push 2
89 Pop 0
90 Compute Add 7 0 6
91 Load (IndAddr 6) 6
92 ComputeI Add 6 1 6
93 Load (IndAddr 6) 5
94 Push 5
95 Compute Add 7 0 4
96 ComputeI Add 4 1 4
97 Load (ImmValue 1) 5
98 Pop 3
99 Store 3 (IndAddr 4)
100 Compute Incr 4 0 4
101 Compute Add 7 0 6
102 Load (IndAddr 6) 6
103 ComputeI Add 6 1 6
104 Store 6 (IndAddr 4)
105 Compute Incr 4 0 4
106 Load (ImmValue (-1)) 3
107 Store 3 (IndAddr 4)
108 Compute Incr 4 0 4
109 Load (ImmValue 120) 6
110 Push 6
111 Pop 5
112 Store 5 (IndAddr 4)
113 Compute Incr 4 0 4
114 Store 7 (IndAddr 4)
115 Compute Add 4 0 7
116 Load (ImmValue 152) 6
117 Push 6
118 Pop 2
```

```
119  Jump (Ind 2)
120  Load (IndAddr 7) 7
121  Load (ImmValue 3) 2
122  Compute Sub 7 2 2
123  ComputeI Add 0 1 5
124  ComputeI Gt 5 1 6
125  Branch 6 (Rel 23)
126  Compute Add 7 5 6
127  Load (IndAddr 6) 4
128  Load (IndAddr 2) 3
129  Compute Lt 3 0 6
130  Branch 6 (Rel 2)
131  Store 4 (IndAddr 3)
132  Compute Incr 2 0 2
133  Load (IndAddr 2) 3
134  Compute Lt 3 0 6
135  Branch 6 (Rel 10)
136  Compute Add 3 0 6
137  TestAndSet (IndAddr 6)
138  Receive 6
139  Branch 6 (Rel 2)
140  Jump (Rel (-4))
141  ComputeI Add 3 1 3
142  WriteInstr 4 (IndAddr 3)
143  ComputeI Sub 3 1 3
144  WriteInstr 0 (IndAddr 3)
145  Compute Incr 5 0 5
146  ComputeI Add 2 2 2
147  Jump (Rel (-23))
148  Compute Decr 7 0 2
149  Load (IndAddr 2) 6
150  Load (IndAddr 7) 7
151  Jump (Ind 6)
152  Load (ImmValue 4) 2
153  Compute Sub 7 2 2
154  Load (ImmValue 1) 5
155  ComputeI Gt 5 1 6
156  Branch 6 (Rel 7)
157  Load (IndAddr 2) 3
158  Compute Add 7 5 6
159  Store 3 (IndAddr 6)
160  Compute Incr 5 0 5
161  ComputeI Add 2 3 2
162  Jump (Rel (-7))
163  Compute Add 7 0 4
164  ComputeI Add 4 2 4
165  Store 7 (IndAddr 4)
166  Compute Add 4 0 7
```



```
167 Compute Add 7 0 6
168 Load (IndAddr 6) 6
169 ComputeI Add 6 1 6
170 Load (IndAddr 6) 5
171 Push 5
172 Load (ImmValue 1) 6
173 Push 6
174 Pop 3
175 Pop 2
176 Compute Gt 2 3 4
177 Push 4
178 Pop 6
179 ComputeI Xor 6 1 6
180 Branch 6 (Rel 67)
181 Compute Add 7 0 4
182 ComputeI Add 4 1 4
183 Store 7 (IndAddr 4)
184 Compute Add 4 0 7
185 Compute Add 7 0 6
186 Load (IndAddr 6) 6
187 Load (IndAddr 6) 6
188 ComputeI Add 6 1 6
189 Load (IndAddr 6) 5
190 Push 5
191 Load (ImmValue 2) 6
192 Push 6
193 Pop 3
194 Pop 2
195 Compute Sub 2 3 4
196 Push 4
197 Compute Add 7 0 6
198 Load (IndAddr 6) 6
199 Load (IndAddr 6) 6
200 ComputeI Add 6 1 6
201 Pop 2
202 Store 2 (IndAddr 6)
203 Push 2
204 Pop 0
205 Compute Add 7 0 6
206 Load (IndAddr 6) 6
207 Load (IndAddr 6) 6
208 ComputeI Add 6 1 6
209 Load (IndAddr 6) 5
210 Push 5
211 Pop 6
212 PrintOut 6
213 Compute Add 7 0 6
214 Load (IndAddr 6) 6
```

```
215 Load (IndAddr 6) 6
216 ComputeI Add 6 1 6
217 Load (IndAddr 6) 5
218 Push 5
219 Compute Add 7 0 4
220 ComputeI Add 4 1 4
221 Load (ImmValue 1) 5
222 Pop 3
223 Store 3 (IndAddr 4)
224 Compute Incr 4 0 4
225 Compute Add 7 0 6
226 Load (IndAddr 6) 6
227 Load (IndAddr 6) 6
228 ComputeI Add 6 1 6
229 Store 6 (IndAddr 4)
230 Compute Incr 4 0 4
231 Load (ImmValue (-1)) 3
232 Store 3 (IndAddr 4)
233 Compute Incr 4 0 4
234 Load (ImmValue 245) 6
235 Push 6
236 Pop 5
237 Store 5 (IndAddr 4)
238 Compute Incr 4 0 4
239 Store 7 (IndAddr 4)
240 Compute Add 4 0 7
241 Load (ImmValue 57) 6
242 Push 6
243 Pop 2
244 Jump (Ind 2)
245 Load (IndAddr 7) 7
246 Jump (Rel 48)
247 Compute Add 7 0 6
248 Load (IndAddr 6) 6
249 ComputeI Add 6 1 6
250 Load (IndAddr 6) 5
251 Push 5
252 Load (ImmValue 0) 6
253 Push 6
254 Pop 3
255 Pop 2
256 Compute Gt 2 3 4
257 Push 4
258 Pop 6
259 ComputeI Xor 6 1 6
260 Branch 6 (Rel 34)
261 Compute Add 7 0 4
262 ComputeI Add 4 1 4
```

```
263 Store 7 (IndAddr 4)
264 Compute Add 4 0 7
265 Compute Add 7 0 6
266 Load (IndAddr 6) 6
267 Load (IndAddr 6) 6
268 ComputeI Add 6 1 6
269 Load (IndAddr 6) 5
270 Push 5
271 Load (ImmValue 1) 6
272 Push 6
273 Pop 3
274 Pop 2
275 Compute Sub 2 3 4
276 Push 4
277 Compute Add 7 0 6
278 Load (IndAddr 6) 6
279 Load (IndAddr 6) 6
280 ComputeI Add 6 1 6
281 Pop 2
282 Store 2 (IndAddr 6)
283 Push 2
284 Pop 0
285 Compute Add 7 0 6
286 Load (IndAddr 6) 6
287 Load (IndAddr 6) 6
288 ComputeI Add 6 1 6
289 Load (IndAddr 6) 5
290 Push 5
291 Pop 6
292 PrintOut 6
293 Load (IndAddr 7) 7
294 Load (IndAddr 7) 7
295 Load (ImmValue 3) 2
296 Compute Sub 7 2 2
297 ComputeI Add 0 1 5
298 ComputeI Gt 5 1 6
299 Branch 6 (Rel 23)
300 Compute Add 7 5 6
301 Load (IndAddr 6) 4
302 Load (IndAddr 2) 3
303 Compute Lt 3 0 6
304 Branch 6 (Rel 2)
305 Store 4 (IndAddr 3)
306 Compute Incr 2 0 2
307 Load (IndAddr 2) 3
308 Compute Lt 3 0 6
309 Branch 6 (Rel 10)
310 Compute Add 3 0 6
```

```
311 TestAndSet (IndAddr 6)
312 Receive 6
313 Branch 6 (Rel 2)
314 Jump (Rel (-4))
315 ComputeI Add 3 1 3
316 WriteInstr 4 (IndAddr 3)
317 ComputeI Sub 3 1 3
318 WriteInstr 0 (IndAddr 3)
319 Compute Incr 5 0 5
320 ComputeI Add 2 2 2
321 Jump (Rel (-23))
322 Compute Decr 7 0 2
323 Load (IndAddr 2) 6
324 Load (IndAddr 7) 7
325 Jump (Ind 6)
326 Nop
327 Nop
328 Load (ImmValue 18) 6
329 Push 6
330 Compute Add 7 0 4
331 ComputeI Add 4 1 4
332 Load (ImmValue 1) 5
333 Pop 3
334 Store 3 (IndAddr 4)
335 Compute Incr 4 0 4
336 Load (ImmValue (-1)) 3
337 Store 3 (IndAddr 4)
338 Compute Incr 4 0 4
339 Load (ImmValue (-1)) 3
340 Store 3 (IndAddr 4)
341 Compute Incr 4 0 4
342 Load (ImmValue 353) 6
343 Push 6
344 Pop 5
345 Store 5 (IndAddr 4)
346 Compute Incr 4 0 4
347 Store 7 (IndAddr 4)
348 Compute Add 4 0 7
349 Load (ImmValue 57) 6
350 Push 6
351 Pop 2
352 Jump (Ind 2)
353 Load (ImmValue 1) 2
354 WriteInstr 2 (DirAddr 0)
355 EndProg
```

## Results

```
1  >>> 17
2  >>> 16
3  >>> 15
4  >>> 14
5  >>> 13
6  >>> 12
7  >>> 11
8  >>> 10
9  >>> 9
10 >>> 8
11 >>> 7
12 >>> 6
13 >>> 5
14 >>> 4
15 >>> 3
16 >>> 2
17 >>> 1
18 >>> 0
19 >>> 0
```

## Deep Expression

### Source

```
1  int a = 100;
2  100000;
3  200000;
4  300000;
5  400000;
6  a = ((a + (((10 * (-15)) * 42) * (3 + 2))) * (2 * ((7 + 11) - 98))); // actual approximate answer fo
7  print(a);
```

### Generated SprIL

```
0  Branch 1 (Rel 6)
1  TestAndSet (DirAddr 2)
2  Receive 6
3  Branch 6 (Rel 2)
4  Jump (Rel (-3))
5  Jump (Rel 54)
6  ReadInstr (DirAddr 0)
7  Receive 3
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
```

```
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Nop
58 Nop
59 Load (ImmValue 100) 6
```

```
60 Push 6
61 Compute Add 7 0 6
62 ComputeI Add 6 1 6
63 Pop 5
64 Store 5 (IndAddr 6)
65 Load (ImmValue 100000) 6
66 Push 6
67 Pop 0
68 Load (ImmValue 200000) 6
69 Push 6
70 Pop 0
71 Load (ImmValue 300000) 6
72 Push 6
73 Pop 0
74 Load (ImmValue 400000) 6
75 Push 6
76 Pop 0
77 Compute Add 7 0 6
78 ComputeI Add 6 1 6
79 Load (IndAddr 6) 5
80 Push 5
81 Load (ImmValue 10) 6
82 Push 6
83 Load (ImmValue 15) 6
84 Push 6
85 Pop 2
86 Compute Sub 2 2 4
87 Compute Sub 4 2 4
88 Push 4
89 Pop 3
90 Pop 2
91 Compute Mul 2 3 4
92 Push 4
93 Load (ImmValue 42) 6
94 Push 6
95 Pop 3
96 Pop 2
97 Compute Mul 2 3 4
98 Push 4
99 Load (ImmValue 3) 6
100 Push 6
101 Load (ImmValue 2) 6
102 Push 6
103 Pop 3
104 Pop 2
105 Compute Add 2 3 4
106 Push 4
107 Pop 3
```

```
108 Pop 2
109 Compute Mul 2 3 4
110 Push 4
111 Pop 3
112 Pop 2
113 Compute Add 2 3 4
114 Push 4
115 Load (ImmValue 2) 6
116 Push 6
117 Load (ImmValue 7) 6
118 Push 6
119 Load (ImmValue 11) 6
120 Push 6
121 Pop 3
122 Pop 2
123 Compute Add 2 3 4
124 Push 4
125 Load (ImmValue 98) 6
126 Push 6
127 Pop 3
128 Pop 2
129 Compute Sub 2 3 4
130 Push 4
131 Pop 3
132 Pop 2
133 Compute Mul 2 3 4
134 Push 4
135 Pop 3
136 Pop 2
137 Compute Mul 2 3 4
138 Push 4
139 Compute Add 7 0 6
140 ComputeI Add 6 1 6
141 Pop 2
142 Store 2 (IndAddr 6)
143 Push 2
144 Pop 0
145 Compute Add 7 0 6
146 ComputeI Add 6 1 6
147 Load (IndAddr 6) 5
148 Push 5
149 Pop 6
150 PrintOut 6
151 Load (ImmValue 1) 2
152 WriteInstr 2 (DirAddr 0)
153 EndProg
```



## Results

1 >>> 5024000

## Fib

### Source

```
1 procedure fib(int i, int res) {
2     if ((i < (3))) {
3         res = 1;
4     } else {
5         int a;
6         int b;
7         fib((i-1), a);
8         fib((i-2), b);
9         res = (a + b);
10    }
11 }
12 }
13
14 int a = 0;
15 fib(8, a);
16 print(a);
```

### Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 260)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
```

```
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 7) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 2 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
```

```
69 ComputeI Add 4 3 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Compute Add 7 0 6
73 Load (IndAddr 6) 6
74 ComputeI Add 6 1 6
75 Load (IndAddr 6) 5
76 Push 5
77 Load (ImmValue 3) 6
78 Push 6
79 Pop 3
80 Pop 2
81 Compute Lt 2 3 4
82 Push 4
83 Pop 6
84 ComputeI Xor 6 1 6
85 Branch 6 (Rel 17)
86 Compute Add 7 0 4
87 ComputeI Add 4 1 4
88 Store 7 (IndAddr 4)
89 Compute Add 4 0 7
90 Load (ImmValue 1) 6
91 Push 6
92 Compute Add 7 0 6
93 Load (IndAddr 6) 6
94 Load (IndAddr 6) 6
95 ComputeI Add 6 2 6
96 Pop 2
97 Store 2 (IndAddr 6)
98 Push 2
99 Pop 0
100 Load (IndAddr 7) 7
101 Jump (Rel 130)
102 Compute Add 7 0 4
103 ComputeI Add 4 1 4
104 Store 7 (IndAddr 4)
105 Compute Add 4 0 7
106 Compute Add 7 0 6
107 ComputeI Add 6 1 6
108 Store 0 (IndAddr 6)
109 Compute Add 7 0 6
110 ComputeI Add 6 2 6
111 Store 0 (IndAddr 6)
112 Compute Add 7 0 6
113 ComputeI Add 6 1 6
114 Load (IndAddr 6) 5
115 Push 5
116 Compute Add 7 0 6
```

```
117 Load (IndAddr 6) 6
118 Load (IndAddr 6) 6
119 ComputeI Add 6 1 6
120 Load (IndAddr 6) 5
121 Push 5
122 Load (ImmValue 1) 6
123 Push 6
124 Pop 3
125 Pop 2
126 Compute Sub 2 3 4
127 Push 4
128 Compute Add 7 0 4
129 ComputeI Add 4 3 4
130 Load (ImmValue 2) 5
131 Pop 3
132 Store 3 (IndAddr 4)
133 Compute Incr 4 0 4
134 Load (ImmValue (-1)) 3
135 Store 3 (IndAddr 4)
136 Compute Incr 4 0 4
137 Load (ImmValue (-1)) 3
138 Store 3 (IndAddr 4)
139 Compute Incr 4 0 4
140 Pop 3
141 Store 3 (IndAddr 4)
142 Compute Incr 4 0 4
143 Compute Add 7 0 6
144 ComputeI Add 6 1 6
145 Store 6 (IndAddr 4)
146 Compute Incr 4 0 4
147 Load (ImmValue (-1)) 3
148 Store 3 (IndAddr 4)
149 Compute Incr 4 0 4
150 Load (ImmValue 161) 6
151 Push 6
152 Pop 5
153 Store 5 (IndAddr 4)
154 Compute Incr 4 0 4
155 Store 7 (IndAddr 4)
156 Compute Add 4 0 7
157 Load (ImmValue 57) 6
158 Push 6
159 Pop 2
160 Jump (Ind 2)
161 Compute Add 7 0 6
162 ComputeI Add 6 2 6
163 Load (IndAddr 6) 5
164 Push 5
```

```
165 Compute Add 7 0 6
166 Load (IndAddr 6) 6
167 Load (IndAddr 6) 6
168 ComputeI Add 6 1 6
169 Load (IndAddr 6) 5
170 Push 5
171 Load (ImmValue 2) 6
172 Push 6
173 Pop 3
174 Pop 2
175 Compute Sub 2 3 4
176 Push 4
177 Compute Add 7 0 4
178 ComputeI Add 4 3 4
179 Load (ImmValue 2) 5
180 Pop 3
181 Store 3 (IndAddr 4)
182 Compute Incr 4 0 4
183 Load (ImmValue (-1)) 3
184 Store 3 (IndAddr 4)
185 Compute Incr 4 0 4
186 Load (ImmValue (-1)) 3
187 Store 3 (IndAddr 4)
188 Compute Incr 4 0 4
189 Pop 3
190 Store 3 (IndAddr 4)
191 Compute Incr 4 0 4
192 Compute Add 7 0 6
193 ComputeI Add 6 2 6
194 Store 6 (IndAddr 4)
195 Compute Incr 4 0 4
196 Load (ImmValue (-1)) 3
197 Store 3 (IndAddr 4)
198 Compute Incr 4 0 4
199 Load (ImmValue 210) 6
200 Push 6
201 Pop 5
202 Store 5 (IndAddr 4)
203 Compute Incr 4 0 4
204 Store 7 (IndAddr 4)
205 Compute Add 4 0 7
206 Load (ImmValue 57) 6
207 Push 6
208 Pop 2
209 Jump (Ind 2)
210 Compute Add 7 0 6
211 ComputeI Add 6 1 6
212 Load (IndAddr 6) 5
```

```
213 Push 5
214 Compute Add 7 0 6
215 ComputeI Add 6 2 6
216 Load (IndAddr 6) 5
217 Push 5
218 Pop 3
219 Pop 2
220 Compute Add 2 3 4
221 Push 4
222 Compute Add 7 0 6
223 Load (IndAddr 6) 6
224 Load (IndAddr 6) 6
225 ComputeI Add 6 2 6
226 Pop 2
227 Store 2 (IndAddr 6)
228 Push 2
229 Pop 0
230 Load (IndAddr 7) 7
231 Load (IndAddr 7) 7
232 Load (ImmValue 6) 2
233 Compute Sub 7 2 2
234 ComputeI Add 0 1 5
235 ComputeI Gt 5 2 6
236 Branch 6 (Rel 23)
237 Compute Add 7 5 6
238 Load (IndAddr 6) 4
239 Load (IndAddr 2) 3
240 Compute Lt 3 0 6
241 Branch 6 (Rel 2)
242 Store 4 (IndAddr 3)
243 Compute Incr 2 0 2
244 Load (IndAddr 2) 3
245 Compute Lt 3 0 6
246 Branch 6 (Rel 10)
247 Compute Add 3 0 6
248 TestAndSet (IndAddr 6)
249 Receive 6
250 Branch 6 (Rel 2)
251 Jump (Rel (-4))
252 ComputeI Add 3 1 3
253 WriteInstr 4 (IndAddr 3)
254 ComputeI Sub 3 1 3
255 WriteInstr 0 (IndAddr 3)
256 Compute Incr 5 0 5
257 ComputeI Add 2 2 2
258 Jump (Rel (-23))
259 Compute Decr 7 0 2
260 Load (IndAddr 2) 6
```

```
261 Load (IndAddr 7) 7
262 Jump (Ind 6)
263 Nop
264 Nop
265 Load (ImmValue 0) 6
266 Push 6
267 Compute Add 7 0 6
268 ComputeI Add 6 1 6
269 Pop 5
270 Store 5 (IndAddr 6)
271 Compute Add 7 0 6
272 ComputeI Add 6 1 6
273 Load (IndAddr 6) 5
274 Push 5
275 Load (ImmValue 8) 6
276 Push 6
277 Compute Add 7 0 4
278 ComputeI Add 4 2 4
279 Load (ImmValue 2) 5
280 Pop 3
281 Store 3 (IndAddr 4)
282 Compute Incr 4 0 4
283 Load (ImmValue (-1)) 3
284 Store 3 (IndAddr 4)
285 Compute Incr 4 0 4
286 Load (ImmValue (-1)) 3
287 Store 3 (IndAddr 4)
288 Compute Incr 4 0 4
289 Pop 3
290 Store 3 (IndAddr 4)
291 Compute Incr 4 0 4
292 Compute Add 7 0 6
293 ComputeI Add 6 1 6
294 Store 6 (IndAddr 4)
295 Compute Incr 4 0 4
296 Load (ImmValue (-1)) 3
297 Store 3 (IndAddr 4)
298 Compute Incr 4 0 4
299 Load (ImmValue 310) 6
300 Push 6
301 Pop 5
302 Store 5 (IndAddr 4)
303 Compute Incr 4 0 4
304 Store 7 (IndAddr 4)
305 Compute Add 4 0 7
306 Load (ImmValue 57) 6
307 Push 6
308 Pop 2
```

```
309 Jump (Ind 2)
310 Compute Add 7 0 6
311 ComputeI Add 6 1 6
312 Load (IndAddr 6) 5
313 Push 5
314 Pop 6
315 PrintOut 6
316 Load (ImmValue 1) 2
317 WriteInstr 2 (DirAddr 0)
318 EndProg
```

## Results

```
1 >>> 21
```

## If

### Source

```
1 bool condition = true;
2 if (condition) print(1); else print(0);
```

## Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 54)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
```



```
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Nop
58 Nop
59 Load (ImmValue 1) 6
60 Push 6
61 Compute Add 7 0 6
62 ComputeI Add 6 1 6
63 Pop 5
64 Store 5 (IndAddr 6)
65 Compute Add 7 0 6
66 ComputeI Add 6 1 6
67 Load (IndAddr 6) 5
68 Push 5
69 Pop 6
70 ComputeI Xor 6 1 6
71 Branch 6 (Rel 6)
```

```
72 Load (ImmValue 1) 6
73 Push 6
74 Pop 6
75 PrintOut 6
76 Jump (Rel 5)
77 Load (ImmValue 0) 6
78 Push 6
79 Pop 6
80 PrintOut 6
81 Load (ImmValue 1) 2
82 WriteInstr 2 (DirAddr 0)
83 EndProg
```

## Results

```
1 >>> 1
```

## If Else

### Source

```
1 int i = 4;
2 print (i);
3 if ((i == 2)) {
4     print(3,i);
5 } else if ((i == 1)) {{{
6     print(4,i);
7 }}} else {{{
8     print(5,i);
9 }}}
10
11
12 if ((i == 4)) {
13     print(3,i);
14 } else if ((i == 1)) {{{
15     print(4,i);
16 }}}}
```

## Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 54)
6 ReadInstr (DirAddr 0)
7 Receive 3
```

```
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
```

```
56  Jump (Abs 9)
57  Nop
58  Nop
59  Load (ImmValue 4) 6
60  Push 6
61  Compute Add 7 0 6
62  ComputeI Add 6 1 6
63  Pop 5
64  Store 5 (IndAddr 6)
65  Compute Add 7 0 6
66  ComputeI Add 6 1 6
67  Load (IndAddr 6) 5
68  Push 5
69  Pop 6
70  PrintOut 6
71  Compute Add 7 0 6
72  ComputeI Add 6 1 6
73  Load (IndAddr 6) 5
74  Push 5
75  Load (ImmValue 2) 6
76  Push 6
77  Pop 3
78  Pop 2
79  Compute Equal 2 3 4
80  Push 4
81  Pop 6
82  ComputeI Xor 6 1 6
83  Branch 6 (Rel 18)
84  Compute Add 7 0 4
85  ComputeI Add 4 2 4
86  Store 7 (IndAddr 4)
87  Compute Add 4 0 7
88  Compute Add 7 0 6
89  Load (IndAddr 6) 6
90  ComputeI Add 6 1 6
91  Load (IndAddr 6) 5
92  Push 5
93  Load (ImmValue 3) 6
94  Push 6
95  Pop 6
96  PrintOut 6
97  Pop 6
98  PrintOut 6
99  Load (IndAddr 7) 7
100 Jump (Rel 71)
101 Compute Add 7 0 6
102 ComputeI Add 6 1 6
103 Load (IndAddr 6) 5
```

```
104 Push 5
105 Load (ImmValue 1) 6
106 Push 6
107 Pop 3
108 Pop 2
109 Compute Equal 2 3 4
110 Push 4
111 Pop 6
112 ComputeI Xor 6 1 6
113 Branch 6 (Rel 30)
114 Compute Add 7 0 4
115 ComputeI Add 4 2 4
116 Store 7 (IndAddr 4)
117 Compute Add 4 0 7
118 Compute Add 7 0 4
119 ComputeI Add 4 1 4
120 Store 7 (IndAddr 4)
121 Compute Add 4 0 7
122 Compute Add 7 0 4
123 ComputeI Add 4 1 4
124 Store 7 (IndAddr 4)
125 Compute Add 4 0 7
126 Compute Add 7 0 6
127 Load (IndAddr 6) 6
128 Load (IndAddr 6) 6
129 Load (IndAddr 6) 6
130 ComputeI Add 6 1 6
131 Load (IndAddr 6) 5
132 Push 5
133 Load (ImmValue 4) 6
134 Push 6
135 Pop 6
136 PrintOut 6
137 Pop 6
138 PrintOut 6
139 Load (IndAddr 7) 7
140 Load (IndAddr 7) 7
141 Load (IndAddr 7) 7
142 Jump (Rel 29)
143 Compute Add 7 0 4
144 ComputeI Add 4 2 4
145 Store 7 (IndAddr 4)
146 Compute Add 4 0 7
147 Compute Add 7 0 4
148 ComputeI Add 4 1 4
149 Store 7 (IndAddr 4)
150 Compute Add 4 0 7
151 Compute Add 7 0 4
```

```
152 ComputeI Add 4 1 4
153 Store 7 (IndAddr 4)
154 Compute Add 4 0 7
155 Compute Add 7 0 6
156 Load (IndAddr 6) 6
157 Load (IndAddr 6) 6
158 Load (IndAddr 6) 6
159 ComputeI Add 6 1 6
160 Load (IndAddr 6) 5
161 Push 5
162 Load (ImmValue 5) 6
163 Push 6
164 Pop 6
165 PrintOut 6
166 Pop 6
167 PrintOut 6
168 Load (IndAddr 7) 7
169 Load (IndAddr 7) 7
170 Load (IndAddr 7) 7
171 Compute Add 7 0 6
172 ComputeI Add 6 1 6
173 Load (IndAddr 6) 5
174 Push 5
175 Load (ImmValue 4) 6
176 Push 6
177 Pop 3
178 Pop 2
179 Compute Equal 2 3 4
180 Push 4
181 Pop 6
182 ComputeI Xor 6 1 6
183 Branch 6 (Rel 18)
184 Compute Add 7 0 4
185 ComputeI Add 4 2 4
186 Store 7 (IndAddr 4)
187 Compute Add 4 0 7
188 Compute Add 7 0 6
189 Load (IndAddr 6) 6
190 ComputeI Add 6 1 6
191 Load (IndAddr 6) 5
192 Push 5
193 Load (ImmValue 3) 6
194 Push 6
195 Pop 6
196 PrintOut 6
197 Pop 6
198 PrintOut 6
199 Load (IndAddr 7) 7
```

```
200  Jump (Rel 42)
201  Compute Add 7 0 6
202  ComputeI Add 6 1 6
203  Load (IndAddr 6) 5
204  Push 5
205  Load (ImmValue 1) 6
206  Push 6
207  Pop 3
208  Pop 2
209  Compute Equal 2 3 4
210  Push 4
211  Pop 6
212  ComputeI Xor 6 1 6
213  Branch 6 (Rel 29)
214  Compute Add 7 0 4
215  ComputeI Add 4 2 4
216  Store 7 (IndAddr 4)
217  Compute Add 4 0 7
218  Compute Add 7 0 4
219  ComputeI Add 4 1 4
220  Store 7 (IndAddr 4)
221  Compute Add 4 0 7
222  Compute Add 7 0 4
223  ComputeI Add 4 1 4
224  Store 7 (IndAddr 4)
225  Compute Add 4 0 7
226  Compute Add 7 0 6
227  Load (IndAddr 6) 6
228  Load (IndAddr 6) 6
229  Load (IndAddr 6) 6
230  ComputeI Add 6 1 6
231  Load (IndAddr 6) 5
232  Push 5
233  Load (ImmValue 4) 6
234  Push 6
235  Pop 6
236  PrintOut 6
237  Pop 6
238  PrintOut 6
239  Load (IndAddr 7) 7
240  Load (IndAddr 7) 7
241  Load (IndAddr 7) 7
242  Load (ImmValue 1) 2
243  WriteInstr 2 (DirAddr 0)
244  EndProg
```

## Results

```
1 >>> 4
2 >>> 5
3 >>> 4
4 >>> 3
5 >>> 4
```

## Infinite Busy Loop

### Source

```
1 int i = 0;
2 int j = 1;
3 while (true) {
4     i = (i + j);
5     j = (j * i);
6     print(i,j);
7 }
```

### Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 54)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
```



```
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Nop
58 Nop
59 Load (ImmValue 0) 6
60 Push 6
61 Compute Add 7 0 6
62 ComputeI Add 6 1 6
63 Pop 5
64 Store 5 (IndAddr 6)
65 Load (ImmValue 1) 6
66 Push 6
67 Compute Add 7 0 6
68 ComputeI Add 6 2 6
69 Pop 5
70 Store 5 (IndAddr 6)
71 Load (ImmValue 1) 6
72 Push 6
73 Pop 6
```

```
74 ComputeI Xor 6 1 6
75 Branch 6 (Rel 63)
76 Compute Add 7 0 4
77 ComputeI Add 4 3 4
78 Store 7 (IndAddr 4)
79 Compute Add 4 0 7
80 Compute Add 7 0 6
81 Load (IndAddr 6) 6
82 ComputeI Add 6 1 6
83 Load (IndAddr 6) 5
84 Push 5
85 Compute Add 7 0 6
86 Load (IndAddr 6) 6
87 ComputeI Add 6 2 6
88 Load (IndAddr 6) 5
89 Push 5
90 Pop 3
91 Pop 2
92 Compute Add 2 3 4
93 Push 4
94 Compute Add 7 0 6
95 Load (IndAddr 6) 6
96 ComputeI Add 6 1 6
97 Pop 2
98 Store 2 (IndAddr 6)
99 Push 2
100 Pop 0
101 Compute Add 7 0 6
102 Load (IndAddr 6) 6
103 ComputeI Add 6 2 6
104 Load (IndAddr 6) 5
105 Push 5
106 Compute Add 7 0 6
107 Load (IndAddr 6) 6
108 ComputeI Add 6 1 6
109 Load (IndAddr 6) 5
110 Push 5
111 Pop 3
112 Pop 2
113 Compute Mul 2 3 4
114 Push 4
115 Compute Add 7 0 6
116 Load (IndAddr 6) 6
117 ComputeI Add 6 2 6
118 Pop 2
119 Store 2 (IndAddr 6)
120 Push 2
121 Pop 0
```

```
122 Compute Add 7 0 6
123 Load (IndAddr 6) 6
124 ComputeI Add 6 2 6
125 Load (IndAddr 6) 5
126 Push 5
127 Compute Add 7 0 6
128 Load (IndAddr 6) 6
129 ComputeI Add 6 1 6
130 Load (IndAddr 6) 5
131 Push 5
132 Pop 6
133 PrintOut 6
134 Pop 6
135 PrintOut 6
136 Load (IndAddr 7) 7
137 Jump (Rel (-66))
138 Load (ImmValue 1) 2
139 WriteInstr 2 (DirAddr 0)
140 EndProg
```

## Results

Gets stuck in an infinite loop, repeating the same output.

```
1 >>> 1
2 >>> 1
3 >>> 2
4 >>> 2
5 >>> 4
6 >>> 8
7 >>> 12
8 >>> 96
9 >>> 108
10 >>> 10368
11 >>> 10476
12 >>> 108615168
13 >>> 108625644
14 >>> 11798392572168192
15 >>> 11798392680793836
16 >>> -5570361874949185536
17 >>> -5558563482268391700
18 >>> 3671369242980155392
19 >>> -1887194239288236308
20 >>> -4483044364780175360
21 >>> -6370238604068411668
22 >>> -8730959061097906176
23 >>> 3345546408543233772
24 >>> -6745737849034768384
25 >>> -3400191440491534612
```

26 >>> -6096120617457680384  
27 >>> 8950432015760336620  
28 >>> -1019520187243692032  
29 >>> 7930911828516644588  
30 >>> -4809903748681826304  
31 >>> 3121008079834818284  
32 >>> 5865085819223539712  
33 >>> 8986093899058357996  
34 >>> 2740241432517279744  
35 >>> -6720408742133913876  
36 >>> 3246081813541552128  
37 >>> -3474326928592361748  
38 >>> -1859074291971129344  
39 >>> -5333401220563491092  
40 >>> 681350175863603200  
41 >>> -4652051044699887892  
42 >>> -8143132099134619648  
43 >>> 5651560929875044076  
44 >>> 6951259845357993984  
45 >>> -5843923298476513556  
46 >>> 4700992750881865728  
47 >>> -1142930547594647828  
48 >>> -8561800288468467712  
49 >>> 8742013237646436076  
50 >>> 7566188111470788608  
51 >>> -2138542724592326932  
52 >>> -6956372574427152384  
53 >>> -9094915299019479316  
54 >>> -8878846665360932864  
55 >>> 472982109329139436  
56 >>> 1756403854674493440  
57 >>> 2229385964003632876  
58 >>> -5152117973711847424  
59 >>> -2922732009708214548  
60 >>> 1585267068834414592  
61 >>> -1337464940873799956  
62 >>> 5188146770730811392  
63 >>> 3850681829857011436  
64 >>> 6917529027641081856  
65 >>> -7678533216211458324  
66 >>> -9223372036854775808  
67 >>> 1544838820643317484  
68 >>> 0  
69 >>> 1544838820643317484  
70 >>> 0  
71 >>> 1544838820643317484  
72 >>> 0  
73 >>> 1544838820643317484

```
74 >>> 0
75 \ldots
```

## Infinite Empty Loop

### Source

```
1 while (true) {
2     // do nothing
3 }
```

### Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 54)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
```

```
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Nop
58 Nop
59 Load (ImmValue 1) 6
60 Push 6
61 Pop 6
62 ComputeI Xor 6 1 6
63 Branch 6 (Rel 7)
64 Compute Add 7 0 4
65 ComputeI Add 4 1 4
66 Store 7 (IndAddr 4)
67 Compute Add 4 0 7
68 Load (IndAddr 7) 7
69 Jump (Rel (-10))
70 Load (ImmValue 1) 2
71 WriteInstr 2 (DirAddr 0)
72 EndProg
```

## Results

No output, gets stuck in an infinite loop.

## Join Test

### Source

```
1  global bool forever = true;
2
3  procedure neverending(bool j) {
4      while(j){
5
6      }
7  }
8
9  fork neverending(forever);
10 join;
11 print(1);
```

### Generated SprIL

```
0  Branch 1 (Rel 6)
1  TestAndSet (DirAddr 2)
2  Receive 6
3  Branch 6 (Rel 2)
4  Jump (Rel (-3))
5  Jump (Rel 115)
6  ReadInstr (DirAddr 0)
7  Receive 3
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
```

```
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 4) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 1 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 2 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Compute Add 7 0 6
73 Load (IndAddr 6) 6
74 ComputeI Add 6 1 6
75 Load (IndAddr 6) 5
76 Push 5
77 Pop 6
```



```
78  ComputeI Xor 6 1 6
79  Branch 6 (Rel 7)
80  Compute Add 7 0 4
81  ComputeI Add 4 1 4
82  Store 7 (IndAddr 4)
83  Compute Add 4 0 7
84  Load (IndAddr 7) 7
85  Jump (Rel (-13))
86  Load (IndAddr 7) 7
87  Load (ImmValue 3) 2
88  Compute Sub 7 2 2
89  ComputeI Add 0 1 5
90  ComputeI Gt 5 1 6
91  Branch 6 (Rel 23)
92  Compute Add 7 5 6
93  Load (IndAddr 6) 4
94  Load (IndAddr 2) 3
95  Compute Lt 3 0 6
96  Branch 6 (Rel 2)
97  Store 4 (IndAddr 3)
98  Compute Incr 2 0 2
99  Load (IndAddr 2) 3
100 Compute Lt 3 0 6
101 Branch 6 (Rel 10)
102 Compute Add 3 0 6
103 TestAndSet (IndAddr 6)
104 Receive 6
105 Branch 6 (Rel 2)
106 Jump (Rel (-4))
107 ComputeI Add 3 1 3
108 WriteInstr 4 (IndAddr 3)
109 ComputeI Sub 3 1 3
110 WriteInstr 0 (IndAddr 3)
111 Compute Incr 5 0 5
112 ComputeI Add 2 2 2
113 Jump (Rel (-23))
114 Compute Decr 7 0 2
115 Load (IndAddr 2) 6
116 Load (IndAddr 7) 7
117 Jump (Ind 6)
118 Nop
119 Nop
120 Load (ImmValue 1) 6
121 Push 6
122 Pop 6
123 Load (ImmValue 32) 2
124 TestAndSet (IndAddr 2)
125 Receive 3
```

```
126 Branch 3 (Rel 2)
127 Jump (Rel (-3))
128 Load (ImmValue 33) 4
129 WriteInstr 6 (IndAddr 4)
130 WriteInstr 0 (IndAddr 2)
131 TestAndSet (DirAddr 1)
132 Receive 6
133 Branch 6 (Rel 2)
134 Jump (Rel (-3))
135 Load (ImmValue 32) 2
136 TestAndSet (IndAddr 2)
137 Receive 3
138 Branch 3 (Rel 2)
139 Jump (Rel (-4))
140 Load (ImmValue 33) 4
141 ReadInstr (IndAddr 4)
142 Receive 5
143 Push 5
144 WriteInstr 0 (IndAddr 2)
145 Load (ImmValue 5) 4
146 Pop 3
147 WriteInstr 3 (IndAddr 4)
148 Compute Incr 4 0 4
149 Load (ImmValue (-1)) 3
150 WriteInstr 3 (IndAddr 4)
151 Compute Incr 4 0 4
152 Load (ImmValue 32) 3
153 WriteInstr 3 (IndAddr 4)
154 Compute Incr 4 0 4
155 Load (ImmValue 1) 5
156 WriteInstr 5 (DirAddr 4)
157 Load (ImmValue 57) 6
158 Push 6
159 Pop 5
160 WriteInstr 5 (DirAddr 3)
161 WriteInstr 0 (DirAddr 2)
162 Load (ImmValue 1) 3
163 ReadInstr (IndAddr 3)
164 Receive 6
165 Branch 6 (Rel 2)
166 Jump (Rel (-3))
167 Compute Equal 0 1 6
168 Branch 6 (Rel 4)
169 Load (ImmValue 2) 2
170 PrintOut 2
171 EndProg
172 Load (ImmValue 30) 3
173 Load (ImmValue 0) 2
```

```
174 ReadInstr (IndAddr 3)
175 Receive 4
176 Compute Add 2 4 2
177 ComputeI NEq 3 32 6
178 Compute Incr 3 0 3
179 Branch 6 (Rel (-5))
180 Compute Equal 2 0 6
181 Branch 6 (Rel 2)
182 Jump (Rel (-10))
183 Load (ImmValue 1) 6
184 Push 6
185 Pop 6
186 PrintOut 6
187 Load (ImmValue 1) 2
188 WriteInstr 2 (DirAddr 0)
189 EndProg
```

## Results

No output, gets stuck in an infinite loop.

## Multiple Globals

### Source

```
1  global int a = 8;
2  global int b = 9;
3  global int c = 10;
4  global int d = 11;
5  global int e = 12;
6  global int f = 13;
7
8  procedure printAll() {
9      print(a,b,c,d,e,f);
10 }
11
12 procedure printAllBW() {
13     print(f,e,d,c,b,a);
14 }
15
16
17 fork printAll();
18 fork printAllBW();
19 join;
```

## Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 292)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
```

```
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 1) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 0 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 1 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Load (ImmValue 43) 2
73 TestAndSet (IndAddr 2)
74 Receive 3
75 Branch 3 (Rel 2)
76 Jump (Rel (-4))
77 Load (ImmValue 44) 4
78 ReadInstr (IndAddr 4)
79 Receive 5
80 Push 5
81 WriteInstr 0 (IndAddr 2)
82 Load (ImmValue 41) 2
83 TestAndSet (IndAddr 2)
84 Receive 3
85 Branch 3 (Rel 2)
86 Jump (Rel (-4))
87 Load (ImmValue 42) 4
88 ReadInstr (IndAddr 4)
89 Receive 5
90 Push 5
91 WriteInstr 0 (IndAddr 2)
92 Load (ImmValue 39) 2
93 TestAndSet (IndAddr 2)
```

```
94 Receive 3
95 Branch 3 (Rel 2)
96 Jump (Rel (-4))
97 Load (ImmValue 40) 4
98 ReadInstr (IndAddr 4)
99 Receive 5
100 Push 5
101 WriteInstr 0 (IndAddr 2)
102 Load (ImmValue 37) 2
103 TestAndSet (IndAddr 2)
104 Receive 3
105 Branch 3 (Rel 2)
106 Jump (Rel (-4))
107 Load (ImmValue 38) 4
108 ReadInstr (IndAddr 4)
109 Receive 5
110 Push 5
111 WriteInstr 0 (IndAddr 2)
112 Load (ImmValue 35) 2
113 TestAndSet (IndAddr 2)
114 Receive 3
115 Branch 3 (Rel 2)
116 Jump (Rel (-4))
117 Load (ImmValue 36) 4
118 ReadInstr (IndAddr 4)
119 Receive 5
120 Push 5
121 WriteInstr 0 (IndAddr 2)
122 Load (ImmValue 33) 2
123 TestAndSet (IndAddr 2)
124 Receive 3
125 Branch 3 (Rel 2)
126 Jump (Rel (-4))
127 Load (ImmValue 34) 4
128 ReadInstr (IndAddr 4)
129 Receive 5
130 Push 5
131 WriteInstr 0 (IndAddr 2)
132 Pop 6
133 PrintOut 6
134 Pop 6
135 PrintOut 6
136 Pop 6
137 PrintOut 6
138 Pop 6
139 PrintOut 6
140 Pop 6
141 PrintOut 6
```

```
142 Pop 6
143 PrintOut 6
144 Load (IndAddr 7) 7
145 Load (ImmValue 0) 2
146 Compute Sub 7 2 2
147 ComputeI Add 0 1 5
148 ComputeI Gt 5 0 6
149 Branch 6 (Rel 23)
150 Compute Add 7 5 6
151 Load (IndAddr 6) 4
152 Load (IndAddr 2) 3
153 Compute Lt 3 0 6
154 Branch 6 (Rel 2)
155 Store 4 (IndAddr 3)
156 Compute Incr 2 0 2
157 Load (IndAddr 2) 3
158 Compute Lt 3 0 6
159 Branch 6 (Rel 10)
160 Compute Add 3 0 6
161 TestAndSet (IndAddr 6)
162 Receive 6
163 Branch 6 (Rel 2)
164 Jump (Rel (-4))
165 ComputeI Add 3 1 3
166 WriteInstr 4 (IndAddr 3)
167 ComputeI Sub 3 1 3
168 WriteInstr 0 (IndAddr 3)
169 Compute Incr 5 0 5
170 ComputeI Add 2 2 2
171 Jump (Rel (-23))
172 Compute Decr 7 0 2
173 Load (IndAddr 2) 6
174 Load (IndAddr 7) 7
175 Jump (Ind 6)
176 Load (ImmValue 1) 2
177 Compute Sub 7 2 2
178 Load (ImmValue 1) 5
179 ComputeI Gt 5 0 6
180 Branch 6 (Rel 7)
181 Load (IndAddr 2) 3
182 Compute Add 7 5 6
183 Store 3 (IndAddr 6)
184 Compute Incr 5 0 5
185 ComputeI Add 2 3 2
186 Jump (Rel (-7))
187 Compute Add 7 0 4
188 ComputeI Add 4 1 4
189 Store 7 (IndAddr 4)
```

```
190 Compute Add 4 0 7
191 Load (ImmValue 33) 2
192 TestAndSet (IndAddr 2)
193 Receive 3
194 Branch 3 (Rel 2)
195 Jump (Rel (-4))
196 Load (ImmValue 34) 4
197 ReadInstr (IndAddr 4)
198 Receive 5
199 Push 5
200 WriteInstr 0 (IndAddr 2)
201 Load (ImmValue 35) 2
202 TestAndSet (IndAddr 2)
203 Receive 3
204 Branch 3 (Rel 2)
205 Jump (Rel (-4))
206 Load (ImmValue 36) 4
207 ReadInstr (IndAddr 4)
208 Receive 5
209 Push 5
210 WriteInstr 0 (IndAddr 2)
211 Load (ImmValue 37) 2
212 TestAndSet (IndAddr 2)
213 Receive 3
214 Branch 3 (Rel 2)
215 Jump (Rel (-4))
216 Load (ImmValue 38) 4
217 ReadInstr (IndAddr 4)
218 Receive 5
219 Push 5
220 WriteInstr 0 (IndAddr 2)
221 Load (ImmValue 39) 2
222 TestAndSet (IndAddr 2)
223 Receive 3
224 Branch 3 (Rel 2)
225 Jump (Rel (-4))
226 Load (ImmValue 40) 4
227 ReadInstr (IndAddr 4)
228 Receive 5
229 Push 5
230 WriteInstr 0 (IndAddr 2)
231 Load (ImmValue 41) 2
232 TestAndSet (IndAddr 2)
233 Receive 3
234 Branch 3 (Rel 2)
235 Jump (Rel (-4))
236 Load (ImmValue 42) 4
237 ReadInstr (IndAddr 4)
```



```
238 Receive 5
239 Push 5
240 WriteInstr 0 (IndAddr 2)
241 Load (ImmValue 43) 2
242 TestAndSet (IndAddr 2)
243 Receive 3
244 Branch 3 (Rel 2)
245 Jump (Rel (-4))
246 Load (ImmValue 44) 4
247 ReadInstr (IndAddr 4)
248 Receive 5
249 Push 5
250 WriteInstr 0 (IndAddr 2)
251 Pop 6
252 PrintOut 6
253 Pop 6
254 PrintOut 6
255 Pop 6
256 PrintOut 6
257 Pop 6
258 PrintOut 6
259 Pop 6
260 PrintOut 6
261 Pop 6
262 PrintOut 6
263 Load (IndAddr 7) 7
264 Load (ImmValue 0) 2
265 Compute Sub 7 2 2
266 ComputeI Add 0 1 5
267 ComputeI Gt 5 0 6
268 Branch 6 (Rel 23)
269 Compute Add 7 5 6
270 Load (IndAddr 6) 4
271 Load (IndAddr 2) 3
272 Compute Lt 3 0 6
273 Branch 6 (Rel 2)
274 Store 4 (IndAddr 3)
275 Compute Incr 2 0 2
276 Load (IndAddr 2) 3
277 Compute Lt 3 0 6
278 Branch 6 (Rel 10)
279 Compute Add 3 0 6
280 TestAndSet (IndAddr 6)
281 Receive 6
282 Branch 6 (Rel 2)
283 Jump (Rel (-4))
284 ComputeI Add 3 1 3
285 WriteInstr 4 (IndAddr 3)
```

```
286 ComputeI Sub 3 1 3
287 WriteInstr 0 (IndAddr 3)
288 Compute Incr 5 0 5
289 ComputeI Add 2 2 2
290 Jump (Rel (-23))
291 Compute Decr 7 0 2
292 Load (IndAddr 2) 6
293 Load (IndAddr 7) 7
294 Jump (Ind 6)
295 Nop
296 Nop
297 Load (ImmValue 8) 6
298 Push 6
299 Pop 6
300 Load (ImmValue 33) 2
301 TestAndSet (IndAddr 2)
302 Receive 3
303 Branch 3 (Rel 2)
304 Jump (Rel (-3))
305 Load (ImmValue 34) 4
306 WriteInstr 6 (IndAddr 4)
307 WriteInstr 0 (IndAddr 2)
308 Load (ImmValue 9) 6
309 Push 6
310 Pop 6
311 Load (ImmValue 35) 2
312 TestAndSet (IndAddr 2)
313 Receive 3
314 Branch 3 (Rel 2)
315 Jump (Rel (-3))
316 Load (ImmValue 36) 4
317 WriteInstr 6 (IndAddr 4)
318 WriteInstr 0 (IndAddr 2)
319 Load (ImmValue 10) 6
320 Push 6
321 Pop 6
322 Load (ImmValue 37) 2
323 TestAndSet (IndAddr 2)
324 Receive 3
325 Branch 3 (Rel 2)
326 Jump (Rel (-3))
327 Load (ImmValue 38) 4
328 WriteInstr 6 (IndAddr 4)
329 WriteInstr 0 (IndAddr 2)
330 Load (ImmValue 11) 6
331 Push 6
332 Pop 6
333 Load (ImmValue 39) 2
```

```
334 TestAndSet (IndAddr 2)
335 Receive 3
336 Branch 3 (Rel 2)
337 Jump (Rel (-3))
338 Load (ImmValue 40) 4
339 WriteInstr 6 (IndAddr 4)
340 WriteInstr 0 (IndAddr 2)
341 Load (ImmValue 12) 6
342 Push 6
343 Pop 6
344 Load (ImmValue 41) 2
345 TestAndSet (IndAddr 2)
346 Receive 3
347 Branch 3 (Rel 2)
348 Jump (Rel (-3))
349 Load (ImmValue 42) 4
350 WriteInstr 6 (IndAddr 4)
351 WriteInstr 0 (IndAddr 2)
352 Load (ImmValue 13) 6
353 Push 6
354 Pop 6
355 Load (ImmValue 43) 2
356 TestAndSet (IndAddr 2)
357 Receive 3
358 Branch 3 (Rel 2)
359 Jump (Rel (-3))
360 Load (ImmValue 44) 4
361 WriteInstr 6 (IndAddr 4)
362 WriteInstr 0 (IndAddr 2)
363 TestAndSet (DirAddr 1)
364 Receive 6
365 Branch 6 (Rel 2)
366 Jump (Rel (-3))
367 Load (ImmValue 5) 4
368 Load (ImmValue 0) 5
369 WriteInstr 5 (DirAddr 4)
370 Load (ImmValue 57) 6
371 Push 6
372 Pop 5
373 WriteInstr 5 (DirAddr 3)
374 WriteInstr 0 (DirAddr 2)
375 Load (ImmValue 1) 3
376 ReadInstr (IndAddr 3)
377 Receive 6
378 Branch 6 (Rel 2)
379 Jump (Rel (-3))
380 TestAndSet (DirAddr 1)
381 Receive 6
```

```
382 Branch 6 (Rel 2)
383 Jump (Rel (-3))
384 Load (ImmValue 5) 4
385 Load (ImmValue 0) 5
386 WriteInstr 5 (DirAddr 4)
387 Load (ImmValue 176) 6
388 Push 6
389 Pop 5
390 WriteInstr 5 (DirAddr 3)
391 WriteInstr 0 (DirAddr 2)
392 Load (ImmValue 1) 3
393 ReadInstr (IndAddr 3)
394 Receive 6
395 Branch 6 (Rel 2)
396 Jump (Rel (-3))
397 Compute Equal 0 1 6
398 Branch 6 (Rel 4)
399 Load (ImmValue 2) 2
400 PrintOut 2
401 EndProg
402 Load (ImmValue 30) 3
403 Load (ImmValue 0) 2
404 ReadInstr (IndAddr 3)
405 Receive 4
406 Compute Add 2 4 2
407 ComputeI NEq 3 33 6
408 Compute Incr 3 0 3
409 Branch 6 (Rel (-5))
410 Compute Equal 2 0 6
411 Branch 6 (Rel 2)
412 Jump (Rel (-10))
413 Load (ImmValue 1) 2
414 WriteInstr 2 (DirAddr 0)
415 EndProg
```

## Results

```
1 >>> 8
2 >>> 9
3 >>> 10
4 >>> 11
5 >>> 12
6 >>> 13
7 >>> 13
8 >>> 12
9 >>> 11
10 >>> 10
11 >>> 9
```

12 >>> 8

## Nested Procedures

### Source

```
1  procedure p0() {
2      print(90);
3      p1();
4      print(91);
5      p2();
6      print(92);
7      p3();
8      print(93);
9      p4();
10     print(94);
11 }
12
13 procedure p1() {
14     print(10);
15     p2();
16     print(12);
17     p3();
18     print(13);
19     p4();
20     print(14);
21 }
22
23 procedure p2() {
24     print(20);
25     p3();
26     print(23);
27     p4();
28     print(24);
29 }
30
31 procedure p3() {
32     print(30);
33     p4();
34     print(34);
35 }
36
37 procedure p4() {
38     print(40);
39 }
40
41 p0();
```

## Generated SprIL

```
0  Branch 1 (Rel 6)
1  TestAndSet (DirAddr 2)
2  Receive 6
3  Branch 6 (Rel 2)
4  Jump (Rel (-3))
5  Jump (Rel 489)
6  ReadInstr (DirAddr 0)
7  Receive 3
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
```

```
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 1) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 0 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 1 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Load (ImmValue 90) 6
73 Push 6
74 Pop 6
75 PrintOut 6
76 Compute Add 7 0 4
77 ComputeI Add 4 1 4
78 Load (ImmValue 0) 5
79 Load (ImmValue 90) 6
80 Push 6
81 Pop 5
82 Store 5 (IndAddr 4)
83 Compute Incr 4 0 4
84 Store 7 (IndAddr 4)
85 Compute Add 4 0 7
86 Load (ImmValue 180) 6
87 Push 6
88 Pop 2
89 Jump (Ind 2)
90 Load (ImmValue 91) 6
91 Push 6
92 Pop 6
93 PrintOut 6
```

```
94  Compute Add 7 0 4
95  ComputeI Add 4 1 4
96  Load (ImmValue 0) 5
97  Load (ImmValue 108) 6
98  Push 6
99  Pop 5
100 Store 5 (IndAddr 4)
101 Compute Incr 4 0 4
102 Store 7 (IndAddr 4)
103 Compute Add 4 0 7
104 Load (ImmValue 285) 6
105 Push 6
106 Pop 2
107 Jump (Ind 2)
108 Load (ImmValue 92) 6
109 Push 6
110 Pop 6
111 PrintOut 6
112 Compute Add 7 0 4
113 ComputeI Add 4 1 4
114 Load (ImmValue 0) 5
115 Load (ImmValue 126) 6
116 Push 6
117 Pop 5
118 Store 5 (IndAddr 4)
119 Compute Incr 4 0 4
120 Store 7 (IndAddr 4)
121 Compute Add 4 0 7
122 Load (ImmValue 372) 6
123 Push 6
124 Pop 2
125 Jump (Ind 2)
126 Load (ImmValue 93) 6
127 Push 6
128 Pop 6
129 PrintOut 6
130 Compute Add 7 0 4
131 ComputeI Add 4 1 4
132 Load (ImmValue 0) 5
133 Load (ImmValue 144) 6
134 Push 6
135 Pop 5
136 Store 5 (IndAddr 4)
137 Compute Incr 4 0 4
138 Store 7 (IndAddr 4)
139 Compute Add 4 0 7
140 Load (ImmValue 441) 6
141 Push 6
```



```
142 Pop 2
143 Jump (Ind 2)
144 Load (ImmValue 94) 6
145 Push 6
146 Pop 6
147 PrintOut 6
148 Load (IndAddr 7) 7
149 Load (ImmValue 0) 2
150 Compute Sub 7 2 2
151 ComputeI Add 0 1 5
152 ComputeI Gt 5 0 6
153 Branch 6 (Rel 23)
154 Compute Add 7 5 6
155 Load (IndAddr 6) 4
156 Load (IndAddr 2) 3
157 Compute Lt 3 0 6
158 Branch 6 (Rel 2)
159 Store 4 (IndAddr 3)
160 Compute Incr 2 0 2
161 Load (IndAddr 2) 3
162 Compute Lt 3 0 6
163 Branch 6 (Rel 10)
164 Compute Add 3 0 6
165 TestAndSet (IndAddr 6)
166 Receive 6
167 Branch 6 (Rel 2)
168 Jump (Rel (-4))
169 ComputeI Add 3 1 3
170 WriteInstr 4 (IndAddr 3)
171 ComputeI Sub 3 1 3
172 WriteInstr 0 (IndAddr 3)
173 Compute Incr 5 0 5
174 ComputeI Add 2 2 2
175 Jump (Rel (-23))
176 Compute Decr 7 0 2
177 Load (IndAddr 2) 6
178 Load (IndAddr 7) 7
179 Jump (Ind 6)
180 Load (ImmValue 1) 2
181 Compute Sub 7 2 2
182 Load (ImmValue 1) 5
183 ComputeI Gt 5 0 6
184 Branch 6 (Rel 7)
185 Load (IndAddr 2) 3
186 Compute Add 7 5 6
187 Store 3 (IndAddr 6)
188 Compute Incr 5 0 5
189 ComputeI Add 2 3 2
```

```
190  Jump (Rel (-7))
191  Compute Add 7 0 4
192  ComputeI Add 4 1 4
193  Store 7 (IndAddr 4)
194  Compute Add 4 0 7
195  Load (ImmValue 10) 6
196  Push 6
197  Pop 6
198  PrintOut 6
199  Compute Add 7 0 4
200  ComputeI Add 4 1 4
201  Load (ImmValue 0) 5
202  Load (ImmValue 213) 6
203  Push 6
204  Pop 5
205  Store 5 (IndAddr 4)
206  Compute Incr 4 0 4
207  Store 7 (IndAddr 4)
208  Compute Add 4 0 7
209  Load (ImmValue 285) 6
210  Push 6
211  Pop 2
212  Jump (Ind 2)
213  Load (ImmValue 12) 6
214  Push 6
215  Pop 6
216  PrintOut 6
217  Compute Add 7 0 4
218  ComputeI Add 4 1 4
219  Load (ImmValue 0) 5
220  Load (ImmValue 231) 6
221  Push 6
222  Pop 5
223  Store 5 (IndAddr 4)
224  Compute Incr 4 0 4
225  Store 7 (IndAddr 4)
226  Compute Add 4 0 7
227  Load (ImmValue 372) 6
228  Push 6
229  Pop 2
230  Jump (Ind 2)
231  Load (ImmValue 13) 6
232  Push 6
233  Pop 6
234  PrintOut 6
235  Compute Add 7 0 4
236  ComputeI Add 4 1 4
237  Load (ImmValue 0) 5
```

```
238 Load (ImmValue 249) 6
239 Push 6
240 Pop 5
241 Store 5 (IndAddr 4)
242 Compute Incr 4 0 4
243 Store 7 (IndAddr 4)
244 Compute Add 4 0 7
245 Load (ImmValue 441) 6
246 Push 6
247 Pop 2
248 Jump (Ind 2)
249 Load (ImmValue 14) 6
250 Push 6
251 Pop 6
252 PrintOut 6
253 Load (IndAddr 7) 7
254 Load (ImmValue 0) 2
255 Compute Sub 7 2 2
256 ComputeI Add 0 1 5
257 ComputeI Gt 5 0 6
258 Branch 6 (Rel 23)
259 Compute Add 7 5 6
260 Load (IndAddr 6) 4
261 Load (IndAddr 2) 3
262 Compute Lt 3 0 6
263 Branch 6 (Rel 2)
264 Store 4 (IndAddr 3)
265 Compute Incr 2 0 2
266 Load (IndAddr 2) 3
267 Compute Lt 3 0 6
268 Branch 6 (Rel 10)
269 Compute Add 3 0 6
270 TestAndSet (IndAddr 6)
271 Receive 6
272 Branch 6 (Rel 2)
273 Jump (Rel (-4))
274 ComputeI Add 3 1 3
275 WriteInstr 4 (IndAddr 3)
276 ComputeI Sub 3 1 3
277 WriteInstr 0 (IndAddr 3)
278 Compute Incr 5 0 5
279 ComputeI Add 2 2 2
280 Jump (Rel (-23))
281 Compute Decr 7 0 2
282 Load (IndAddr 2) 6
283 Load (IndAddr 7) 7
284 Jump (Ind 6)
285 Load (ImmValue 1) 2
```

```
286 Compute Sub 7 2 2
287 Load (ImmValue 1) 5
288 ComputeI Gt 5 0 6
289 Branch 6 (Rel 7)
290 Load (IndAddr 2) 3
291 Compute Add 7 5 6
292 Store 3 (IndAddr 6)
293 Compute Incr 5 0 5
294 ComputeI Add 2 3 2
295 Jump (Rel (-7))
296 Compute Add 7 0 4
297 ComputeI Add 4 1 4
298 Store 7 (IndAddr 4)
299 Compute Add 4 0 7
300 Load (ImmValue 20) 6
301 Push 6
302 Pop 6
303 PrintOut 6
304 Compute Add 7 0 4
305 ComputeI Add 4 1 4
306 Load (ImmValue 0) 5
307 Load (ImmValue 318) 6
308 Push 6
309 Pop 5
310 Store 5 (IndAddr 4)
311 Compute Incr 4 0 4
312 Store 7 (IndAddr 4)
313 Compute Add 4 0 7
314 Load (ImmValue 372) 6
315 Push 6
316 Pop 2
317 Jump (Ind 2)
318 Load (ImmValue 23) 6
319 Push 6
320 Pop 6
321 PrintOut 6
322 Compute Add 7 0 4
323 ComputeI Add 4 1 4
324 Load (ImmValue 0) 5
325 Load (ImmValue 336) 6
326 Push 6
327 Pop 5
328 Store 5 (IndAddr 4)
329 Compute Incr 4 0 4
330 Store 7 (IndAddr 4)
331 Compute Add 4 0 7
332 Load (ImmValue 441) 6
333 Push 6
```

```
334 Pop 2
335 Jump (Ind 2)
336 Load (ImmValue 24) 6
337 Push 6
338 Pop 6
339 PrintOut 6
340 Load (IndAddr 7) 7
341 Load (ImmValue 0) 2
342 Compute Sub 7 2 2
343 ComputeI Add 0 1 5
344 ComputeI Gt 5 0 6
345 Branch 6 (Rel 23)
346 Compute Add 7 5 6
347 Load (IndAddr 6) 4
348 Load (IndAddr 2) 3
349 Compute Lt 3 0 6
350 Branch 6 (Rel 2)
351 Store 4 (IndAddr 3)
352 Compute Incr 2 0 2
353 Load (IndAddr 2) 3
354 Compute Lt 3 0 6
355 Branch 6 (Rel 10)
356 Compute Add 3 0 6
357 TestAndSet (IndAddr 6)
358 Receive 6
359 Branch 6 (Rel 2)
360 Jump (Rel (-4))
361 ComputeI Add 3 1 3
362 WriteInstr 4 (IndAddr 3)
363 ComputeI Sub 3 1 3
364 WriteInstr 0 (IndAddr 3)
365 Compute Incr 5 0 5
366 ComputeI Add 2 2 2
367 Jump (Rel (-23))
368 Compute Decr 7 0 2
369 Load (IndAddr 2) 6
370 Load (IndAddr 7) 7
371 Jump (Ind 6)
372 Load (ImmValue 1) 2
373 Compute Sub 7 2 2
374 Load (ImmValue 1) 5
375 ComputeI Gt 5 0 6
376 Branch 6 (Rel 7)
377 Load (IndAddr 2) 3
378 Compute Add 7 5 6
379 Store 3 (IndAddr 6)
380 Compute Incr 5 0 5
381 ComputeI Add 2 3 2
```

```
382  Jump (Rel (-7))
383  Compute Add 7 0 4
384  ComputeI Add 4 1 4
385  Store 7 (IndAddr 4)
386  Compute Add 4 0 7
387  Load (ImmValue 30) 6
388  Push 6
389  Pop 6
390  PrintOut 6
391  Compute Add 7 0 4
392  ComputeI Add 4 1 4
393  Load (ImmValue 0) 5
394  Load (ImmValue 405) 6
395  Push 6
396  Pop 5
397  Store 5 (IndAddr 4)
398  Compute Incr 4 0 4
399  Store 7 (IndAddr 4)
400  Compute Add 4 0 7
401  Load (ImmValue 441) 6
402  Push 6
403  Pop 2
404  Jump (Ind 2)
405  Load (ImmValue 34) 6
406  Push 6
407  Pop 6
408  PrintOut 6
409  Load (IndAddr 7) 7
410  Load (ImmValue 0) 2
411  Compute Sub 7 2 2
412  ComputeI Add 0 1 5
413  ComputeI Gt 5 0 6
414  Branch 6 (Rel 23)
415  Compute Add 7 5 6
416  Load (IndAddr 6) 4
417  Load (IndAddr 2) 3
418  Compute Lt 3 0 6
419  Branch 6 (Rel 2)
420  Store 4 (IndAddr 3)
421  Compute Incr 2 0 2
422  Load (IndAddr 2) 3
423  Compute Lt 3 0 6
424  Branch 6 (Rel 10)
425  Compute Add 3 0 6
426  TestAndSet (IndAddr 6)
427  Receive 6
428  Branch 6 (Rel 2)
429  Jump (Rel (-4))
```

```
430 ComputeI Add 3 1 3
431 WriteInstr 4 (IndAddr 3)
432 ComputeI Sub 3 1 3
433 WriteInstr 0 (IndAddr 3)
434 Compute Incr 5 0 5
435 ComputeI Add 2 2 2
436 Jump (Rel (-23))
437 Compute Decr 7 0 2
438 Load (IndAddr 2) 6
439 Load (IndAddr 7) 7
440 Jump (Ind 6)
441 Load (ImmValue 1) 2
442 Compute Sub 7 2 2
443 Load (ImmValue 1) 5
444 ComputeI Gt 5 0 6
445 Branch 6 (Rel 7)
446 Load (IndAddr 2) 3
447 Compute Add 7 5 6
448 Store 3 (IndAddr 6)
449 Compute Incr 5 0 5
450 ComputeI Add 2 3 2
451 Jump (Rel (-7))
452 Compute Add 7 0 4
453 ComputeI Add 4 1 4
454 Store 7 (IndAddr 4)
455 Compute Add 4 0 7
456 Load (ImmValue 40) 6
457 Push 6
458 Pop 6
459 PrintOut 6
460 Load (IndAddr 7) 7
461 Load (ImmValue 0) 2
462 Compute Sub 7 2 2
463 ComputeI Add 0 1 5
464 ComputeI Gt 5 0 6
465 Branch 6 (Rel 23)
466 Compute Add 7 5 6
467 Load (IndAddr 6) 4
468 Load (IndAddr 2) 3
469 Compute Lt 3 0 6
470 Branch 6 (Rel 2)
471 Store 4 (IndAddr 3)
472 Compute Incr 2 0 2
473 Load (IndAddr 2) 3
474 Compute Lt 3 0 6
475 Branch 6 (Rel 10)
476 Compute Add 3 0 6
477 TestAndSet (IndAddr 6)
```

```
478 Receive 6
479 Branch 6 (Rel 2)
480 Jump (Rel (-4))
481 ComputeI Add 3 1 3
482 WriteInstr 4 (IndAddr 3)
483 ComputeI Sub 3 1 3
484 WriteInstr 0 (IndAddr 3)
485 Compute Incr 5 0 5
486 ComputeI Add 2 2 2
487 Jump (Rel (-23))
488 Compute Decr 7 0 2
489 Load (IndAddr 2) 6
490 Load (IndAddr 7) 7
491 Jump (Ind 6)
492 Nop
493 Nop
494 Compute Add 7 0 4
495 ComputeI Add 4 1 4
496 Load (ImmValue 0) 5
497 Load (ImmValue 508) 6
498 Push 6
499 Pop 5
500 Store 5 (IndAddr 4)
501 Compute Incr 4 0 4
502 Store 7 (IndAddr 4)
503 Compute Add 4 0 7
504 Load (ImmValue 57) 6
505 Push 6
506 Pop 2
507 Jump (Ind 2)
508 Load (ImmValue 1) 2
509 WriteInstr 2 (DirAddr 0)
510 EndProg
```

## Results

```
1 >>> 90
2 >>> 10
3 >>> 20
4 >>> 30
5 >>> 40
6 >>> 34
7 >>> 23
8 >>> 40
9 >>> 24
10 >>> 12
11 >>> 30
12 >>> 40
```



```
13 >>> 34
14 >>> 13
15 >>> 40
16 >>> 14
17 >>> 91
18 >>> 20
19 >>> 30
20 >>> 40
21 >>> 34
22 >>> 23
23 >>> 40
24 >>> 24
25 >>> 92
26 >>> 30
27 >>> 40
28 >>> 34
29 >>> 93
30 >>> 40
31 >>> 94
```

## Peterson

### Source

```
1  global bool flag_0 = false;
2  global bool flag_1 = false;
3  global int turn = 0;
4  global int i = 0;
5
6  procedure p_0() {
7      flag_0 = true;
8      turn = 1;
9      while ((flag_1 && (turn == 1))) {
10         // wait
11     }
12     // begin critical section
13     int j = 5;
14     while ((j > 0)) {
15         i = ++i;
16         j = --j;
17     }
18     // end critical section
19     flag_0 = false;
20 }
21
22 procedure p_1() {
23     flag_1 = true;
24     turn = 0;
```

```
25     while ((flag_0 && (turn == 0))) {
26         // wait
27     }
28     // begin critical section
29     int j = 5;
30     while ((j > 0)) {
31         i = --i;
32         j = --j;
33     }
34     // end critical section
35     flag_1 = false;
36 }
37
38 procedure test1(int j) {
39     while ((j > 0)) {
40         fork p_0();
41         fork p_1();
42         join;
43         print(i);
44
45         fork p_1();
46         fork p_0();
47         join;
48         print(i);
49
50         j = --j;
51     }
52 }
53
54 test1(10);
```

## Generated SprIL

```
0  Compute Equal 1 0 6
1  Branch 6 (Rel 2)
2  Jump (Rel 7)
3  TestAndSet (DirAddr 2)
4  Receive 6
5  Branch 6 (Rel 2)
6  Jump (Rel (-3))
7  Load (ImmValue 0) 7
8  Jump (Rel 630)
9  ReadInstr (DirAddr 0)
10 Receive 3
11 Compute Equal 3 0 6
12 Branch 6 (Rel 2)
13 EndProg
14 TestAndSet (DirAddr 2)
```

```
15 Receive 6
16 Branch 6 (Rel 2)
17 Jump (Rel (-8))
18 ComputeI Add 1 30 3
19 TestAndSet (IndAddr 3)
20 Receive 6
21 Branch 6 (Rel 2)
22 Jump (Rel (-3))
23 ReadInstr (DirAddr 3)
24 Receive 3
25 Push 3
26 ComputeI Add 7 1 4
27 ReadInstr (DirAddr 4)
28 Receive 5
29 Load (ImmValue 5) 2
30 Compute Equal 5 0 6
31 Branch 6 (Rel 18)
32 ReadInstr (IndAddr 2)
33 Receive 3
34 Store 3 (IndAddr 4)
35 Compute Incr 2 0 2
36 Compute Incr 4 0 4
37 ReadInstr (IndAddr 2)
38 Receive 3
39 Store 3 (IndAddr 4)
40 Compute Incr 2 0 2
41 Compute Incr 4 0 4
42 ReadInstr (IndAddr 2)
43 Receive 3
44 Store 3 (IndAddr 4)
45 Compute Incr 2 0 2
46 Compute Incr 4 0 4
47 Compute Decr 5 0 5
48 Jump (Rel (-18))
49 Load (ImmValue 57) 5
50 Store 5 (IndAddr 4)
51 Compute Incr 4 0 4
52 Store 7 (IndAddr 4)
53 Compute Add 4 0 7
54 Pop 2
55 WriteInstr 0 (DirAddr 1)
56 Jump (Ind 2)
57 ComputeI Add 1 30 3
58 WriteInstr 0 (IndAddr 3)
59 Jump (Abs 9)
60 Load (ImmValue 1) 2
61 Compute Sub 7 2 2
62 Load (ImmValue 1) 5
```

```
63 ComputeI Gt 5 0 6
64 Branch 6 (Rel 7)
65 Load (IndAddr 2) 3
66 Compute Add 7 5 6
67 Store 3 (IndAddr 6)
68 Compute Incr 5 0 5
69 ComputeI Add 2 3 2
70 Jump (Rel (-7))
71 Compute Add 7 0 4
72 ComputeI Add 4 1 4
73 Store 7 (IndAddr 4)
74 Compute Add 4 0 7
75 Load (ImmValue 1) 6
76 Push 6
77 Load (ImmValue 33) 2
78 TestAndSet (IndAddr 2)
79 Receive 3
80 Branch 3 (Rel 2)
81 Jump (Rel (-4))
82 Load (ImmValue 34) 4
83 Pop 6
84 WriteInstr 6 (IndAddr 4)
85 WriteInstr 0 (IndAddr 2)
86 Pop 0
87 Load (ImmValue 1) 6
88 Push 6
89 Load (ImmValue 39) 2
90 TestAndSet (IndAddr 2)
91 Receive 3
92 Branch 3 (Rel 2)
93 Jump (Rel (-4))
94 Load (ImmValue 40) 4
95 Pop 6
96 WriteInstr 6 (IndAddr 4)
97 WriteInstr 0 (IndAddr 2)
98 Pop 0
99 Load (ImmValue 35) 2
100 TestAndSet (IndAddr 2)
101 Receive 3
102 Branch 3 (Rel 2)
103 Jump (Rel (-4))
104 Load (ImmValue 36) 4
105 ReadInstr (IndAddr 4)
106 Receive 5
107 Push 5
108 WriteInstr 0 (IndAddr 2)
109 Load (ImmValue 39) 2
110 TestAndSet (IndAddr 2)
```

```
111 Receive 3
112 Branch 3 (Rel 2)
113 Jump (Rel (-4))
114 Load (ImmValue 40) 4
115 ReadInstr (IndAddr 4)
116 Receive 5
117 Push 5
118 WriteInstr 0 (IndAddr 2)
119 Load (ImmValue 1) 6
120 Push 6
121 Pop 3
122 Pop 2
123 Compute Equal 2 3 4
124 Push 4
125 Pop 3
126 Pop 2
127 Compute And 2 3 4
128 Push 4
129 Pop 6
130 ComputeI Xor 6 1 6
131 Branch 6 (Rel 7)
132 Compute Add 7 0 4
133 ComputeI Add 4 1 4
134 Store 7 (IndAddr 4)
135 Compute Add 4 0 7
136 Load (IndAddr 7) 7
137 Jump (Rel (-38))
138 Load (ImmValue 5) 6
139 Push 6
140 Compute Add 7 0 6
141 ComputeI Add 6 1 6
142 Pop 5
143 Store 5 (IndAddr 6)
144 Compute Add 7 0 6
145 ComputeI Add 6 1 6
146 Load (IndAddr 6) 5
147 Push 5
148 Load (ImmValue 0) 6
149 Push 6
150 Pop 3
151 Pop 2
152 Compute Gt 2 3 4
153 Push 4
154 Pop 6
155 ComputeI Xor 6 1 6
156 Branch 6 (Rel 45)
157 Compute Add 7 0 4
158 ComputeI Add 4 2 4
```

```
159 Store 7 (IndAddr 4)
160 Compute Add 4 0 7
161 Load (ImmValue 37) 2
162 TestAndSet (IndAddr 2)
163 Receive 3
164 Branch 3 (Rel 2)
165 Jump (Rel (-4))
166 Load (ImmValue 38) 4
167 ReadInstr (IndAddr 4)
168 Receive 5
169 Push 5
170 WriteInstr 0 (IndAddr 2)
171 Pop 2
172 Compute Incr 2 0 4
173 Push 4
174 Load (ImmValue 37) 2
175 TestAndSet (IndAddr 2)
176 Receive 3
177 Branch 3 (Rel 2)
178 Jump (Rel (-4))
179 Load (ImmValue 38) 4
180 Pop 6
181 WriteInstr 6 (IndAddr 4)
182 WriteInstr 0 (IndAddr 2)
183 Pop 0
184 Compute Add 7 0 6
185 Load (IndAddr 6) 6
186 ComputeI Add 6 1 6
187 Load (IndAddr 6) 5
188 Push 5
189 Pop 2
190 Compute Decr 2 0 4
191 Push 4
192 Compute Add 7 0 6
193 Load (IndAddr 6) 6
194 ComputeI Add 6 1 6
195 Pop 2
196 Store 2 (IndAddr 6)
197 Push 2
198 Pop 0
199 Load (IndAddr 7) 7
200 Jump (Rel (-56))
201 Load (ImmValue 0) 6
202 Push 6
203 Load (ImmValue 33) 2
204 TestAndSet (IndAddr 2)
205 Receive 3
206 Branch 3 (Rel 2)
```

```
207  Jump (Rel (-4))
208  Load (ImmValue 34) 4
209  Pop 6
210  WriteInstr 6 (IndAddr 4)
211  WriteInstr 0 (IndAddr 2)
212  Pop 0
213  Load (IndAddr 7) 7
214  Load (ImmValue 0) 2
215  Compute Sub 7 2 2
216  ComputeI Add 0 1 5
217  ComputeI Gt 5 0 6
218  Branch 6 (Rel 23)
219  Compute Add 7 5 6
220  Load (IndAddr 6) 4
221  Load (IndAddr 2) 3
222  Compute Lt 3 0 6
223  Branch 6 (Rel 2)
224  Store 4 (IndAddr 3)
225  Compute Incr 2 0 2
226  Load (IndAddr 2) 3
227  Compute Lt 3 0 6
228  Branch 6 (Rel 10)
229  Compute Add 3 0 6
230  TestAndSet (IndAddr 6)
231  Receive 6
232  Branch 6 (Rel 2)
233  Jump (Rel (-4))
234  ComputeI Add 3 1 3
235  WriteInstr 4 (IndAddr 3)
236  ComputeI Sub 3 1 3
237  WriteInstr 0 (IndAddr 3)
238  Compute Incr 5 0 5
239  ComputeI Add 2 2 2
240  Jump (Rel (-23))
241  Compute Decr 7 0 2
242  Load (IndAddr 2) 6
243  Load (IndAddr 7) 7
244  Jump (Ind 6)
245  Load (ImmValue 1) 2
246  Compute Sub 7 2 2
247  Load (ImmValue 1) 5
248  ComputeI Gt 5 0 6
249  Branch 6 (Rel 7)
250  Load (IndAddr 2) 3
251  Compute Add 7 5 6
252  Store 3 (IndAddr 6)
253  Compute Incr 5 0 5
254  ComputeI Add 2 3 2
```

```
255  Jump (Rel (-7))
256  Compute Add 7 0 4
257  ComputeI Add 4 1 4
258  Store 7 (IndAddr 4)
259  Compute Add 4 0 7
260  Load (ImmValue 1) 6
261  Push 6
262  Load (ImmValue 35) 2
263  TestAndSet (IndAddr 2)
264  Receive 3
265  Branch 3 (Rel 2)
266  Jump (Rel (-4))
267  Load (ImmValue 36) 4
268  Pop 6
269  WriteInstr 6 (IndAddr 4)
270  WriteInstr 0 (IndAddr 2)
271  Pop 0
272  Load (ImmValue 0) 6
273  Push 6
274  Load (ImmValue 39) 2
275  TestAndSet (IndAddr 2)
276  Receive 3
277  Branch 3 (Rel 2)
278  Jump (Rel (-4))
279  Load (ImmValue 40) 4
280  Pop 6
281  WriteInstr 6 (IndAddr 4)
282  WriteInstr 0 (IndAddr 2)
283  Pop 0
284  Load (ImmValue 33) 2
285  TestAndSet (IndAddr 2)
286  Receive 3
287  Branch 3 (Rel 2)
288  Jump (Rel (-4))
289  Load (ImmValue 34) 4
290  ReadInstr (IndAddr 4)
291  Receive 5
292  Push 5
293  WriteInstr 0 (IndAddr 2)
294  Load (ImmValue 39) 2
295  TestAndSet (IndAddr 2)
296  Receive 3
297  Branch 3 (Rel 2)
298  Jump (Rel (-4))
299  Load (ImmValue 40) 4
300  ReadInstr (IndAddr 4)
301  Receive 5
302  Push 5
```



```
303 WriteInstr 0 (IndAddr 2)
304 Load (ImmValue 0) 6
305 Push 6
306 Pop 3
307 Pop 2
308 Compute Equal 2 3 4
309 Push 4
310 Pop 3
311 Pop 2
312 Compute And 2 3 4
313 Push 4
314 Pop 6
315 ComputeI Xor 6 1 6
316 Branch 6 (Rel 7)
317 Compute Add 7 0 4
318 ComputeI Add 4 1 4
319 Store 7 (IndAddr 4)
320 Compute Add 4 0 7
321 Load (IndAddr 7) 7
322 Jump (Rel (-38))
323 Load (ImmValue 5) 6
324 Push 6
325 Compute Add 7 0 6
326 ComputeI Add 6 1 6
327 Pop 5
328 Store 5 (IndAddr 6)
329 Compute Add 7 0 6
330 ComputeI Add 6 1 6
331 Load (IndAddr 6) 5
332 Push 5
333 Load (ImmValue 0) 6
334 Push 6
335 Pop 3
336 Pop 2
337 Compute Gt 2 3 4
338 Push 4
339 Pop 6
340 ComputeI Xor 6 1 6
341 Branch 6 (Rel 45)
342 Compute Add 7 0 4
343 ComputeI Add 4 2 4
344 Store 7 (IndAddr 4)
345 Compute Add 4 0 7
346 Load (ImmValue 37) 2
347 TestAndSet (IndAddr 2)
348 Receive 3
349 Branch 3 (Rel 2)
350 Jump (Rel (-4))
```

```
351 Load (ImmValue 38) 4
352 ReadInstr (IndAddr 4)
353 Receive 5
354 Push 5
355 WriteInstr 0 (IndAddr 2)
356 Pop 2
357 Compute Decr 2 0 4
358 Push 4
359 Load (ImmValue 37) 2
360 TestAndSet (IndAddr 2)
361 Receive 3
362 Branch 3 (Rel 2)
363 Jump (Rel (-4))
364 Load (ImmValue 38) 4
365 Pop 6
366 WriteInstr 6 (IndAddr 4)
367 WriteInstr 0 (IndAddr 2)
368 Pop 0
369 Compute Add 7 0 6
370 Load (IndAddr 6) 6
371 ComputeI Add 6 1 6
372 Load (IndAddr 6) 5
373 Push 5
374 Pop 2
375 Compute Decr 2 0 4
376 Push 4
377 Compute Add 7 0 6
378 Load (IndAddr 6) 6
379 ComputeI Add 6 1 6
380 Pop 2
381 Store 2 (IndAddr 6)
382 Push 2
383 Pop 0
384 Load (IndAddr 7) 7
385 Jump (Rel (-56))
386 Load (ImmValue 0) 6
387 Push 6
388 Load (ImmValue 35) 2
389 TestAndSet (IndAddr 2)
390 Receive 3
391 Branch 3 (Rel 2)
392 Jump (Rel (-4))
393 Load (ImmValue 36) 4
394 Pop 6
395 WriteInstr 6 (IndAddr 4)
396 WriteInstr 0 (IndAddr 2)
397 Pop 0
398 Load (IndAddr 7) 7
```

```
399 Load (ImmValue 0) 2
400 Compute Sub 7 2 2
401 ComputeI Add 0 1 5
402 ComputeI Gt 5 0 6
403 Branch 6 (Rel 23)
404 Compute Add 7 5 6
405 Load (IndAddr 6) 4
406 Load (IndAddr 2) 3
407 Compute Lt 3 0 6
408 Branch 6 (Rel 2)
409 Store 4 (IndAddr 3)
410 Compute Incr 2 0 2
411 Load (IndAddr 2) 3
412 Compute Lt 3 0 6
413 Branch 6 (Rel 10)
414 Compute Add 3 0 6
415 TestAndSet (IndAddr 6)
416 Receive 6
417 Branch 6 (Rel 2)
418 Jump (Rel (-4))
419 ComputeI Add 3 1 3
420 WriteInstr 4 (IndAddr 3)
421 ComputeI Sub 3 1 3
422 WriteInstr 0 (IndAddr 3)
423 Compute Incr 5 0 5
424 ComputeI Add 2 2 2
425 Jump (Rel (-23))
426 Compute Decr 7 0 2
427 Load (IndAddr 2) 6
428 Load (IndAddr 7) 7
429 Jump (Ind 6)
430 Load (ImmValue 4) 2
431 Compute Sub 7 2 2
432 Load (ImmValue 1) 5
433 ComputeI Gt 5 1 6
434 Branch 6 (Rel 7)
435 Load (IndAddr 2) 3
436 Compute Add 7 5 6
437 Store 3 (IndAddr 6)
438 Compute Incr 5 0 5
439 ComputeI Add 2 3 2
440 Jump (Rel (-7))
441 Compute Add 7 0 4
442 ComputeI Add 4 2 4
443 Store 7 (IndAddr 4)
444 Compute Add 4 0 7
445 Compute Add 7 0 6
446 Load (IndAddr 6) 6
```

```
447 ComputeI Add 6 1 6
448 Load (IndAddr 6) 5
449 Push 5
450 Load (ImmValue 0) 6
451 Push 6
452 Pop 3
453 Pop 2
454 Compute Gt 2 3 4
455 Push 4
456 Pop 6
457 ComputeI Xor 6 1 6
458 Branch 6 (Rel 148)
459 Compute Add 7 0 4
460 ComputeI Add 4 1 4
461 Store 7 (IndAddr 4)
462 Compute Add 4 0 7
463 TestAndSet (DirAddr 1)
464 Receive 6
465 Branch 6 (Rel 2)
466 Jump (Rel (-3))
467 Load (ImmValue 5) 4
468 Load (ImmValue 0) 5
469 WriteInstr 5 (DirAddr 4)
470 Load (ImmValue 60) 6
471 Push 6
472 Pop 5
473 WriteInstr 5 (DirAddr 3)
474 WriteInstr 0 (DirAddr 2)
475 Load (ImmValue 1) 3
476 ReadInstr (IndAddr 3)
477 Receive 6
478 Branch 6 (Rel 2)
479 Jump (Rel (-3))
480 TestAndSet (DirAddr 1)
481 Receive 6
482 Branch 6 (Rel 2)
483 Jump (Rel (-3))
484 Load (ImmValue 5) 4
485 Load (ImmValue 0) 5
486 WriteInstr 5 (DirAddr 4)
487 Load (ImmValue 245) 6
488 Push 6
489 Pop 5
490 WriteInstr 5 (DirAddr 3)
491 WriteInstr 0 (DirAddr 2)
492 Load (ImmValue 1) 3
493 ReadInstr (IndAddr 3)
494 Receive 6
```

```
495 Branch 6 (Rel 2)
496 Jump (Rel (-3))
497 Compute Equal 0 1 6
498 Branch 6 (Rel 4)
499 Load (ImmValue 2) 2
500 PrintOut 2
501 EndProg
502 Load (ImmValue 30) 3
503 Load (ImmValue 0) 2
504 ReadInstr (IndAddr 3)
505 Receive 4
506 Compute Add 2 4 2
507 ComputeI NEq 3 33 6
508 Compute Incr 3 0 3
509 Branch 6 (Rel (-5))
510 Compute Equal 2 0 6
511 Branch 6 (Rel 2)
512 Jump (Rel (-10))
513 Load (ImmValue 37) 2
514 TestAndSet (IndAddr 2)
515 Receive 3
516 Branch 3 (Rel 2)
517 Jump (Rel (-4))
518 Load (ImmValue 38) 4
519 ReadInstr (IndAddr 4)
520 Receive 5
521 Push 5
522 WriteInstr 0 (IndAddr 2)
523 Pop 6
524 PrintOut 6
525 TestAndSet (DirAddr 1)
526 Receive 6
527 Branch 6 (Rel 2)
528 Jump (Rel (-3))
529 Load (ImmValue 5) 4
530 Load (ImmValue 0) 5
531 WriteInstr 5 (DirAddr 4)
532 Load (ImmValue 245) 6
533 Push 6
534 Pop 5
535 WriteInstr 5 (DirAddr 3)
536 WriteInstr 0 (DirAddr 2)
537 Load (ImmValue 1) 3
538 ReadInstr (IndAddr 3)
539 Receive 6
540 Branch 6 (Rel 2)
541 Jump (Rel (-3))
542 TestAndSet (DirAddr 1)
```

```
543 Receive 6
544 Branch 6 (Rel 2)
545 Jump (Rel (-3))
546 Load (ImmValue 5) 4
547 Load (ImmValue 0) 5
548 WriteInstr 5 (DirAddr 4)
549 Load (ImmValue 60) 6
550 Push 6
551 Pop 5
552 WriteInstr 5 (DirAddr 3)
553 WriteInstr 0 (DirAddr 2)
554 Load (ImmValue 1) 3
555 ReadInstr (IndAddr 3)
556 Receive 6
557 Branch 6 (Rel 2)
558 Jump (Rel (-3))
559 Compute Equal 0 1 6
560 Branch 6 (Rel 4)
561 Load (ImmValue 2) 2
562 PrintOut 2
563 EndProg
564 Load (ImmValue 30) 3
565 Load (ImmValue 0) 2
566 ReadInstr (IndAddr 3)
567 Receive 4
568 Compute Add 2 4 2
569 ComputeI NEq 3 33 6
570 Compute Incr 3 0 3
571 Branch 6 (Rel (-5))
572 Compute Equal 2 0 6
573 Branch 6 (Rel 2)
574 Jump (Rel (-10))
575 Load (ImmValue 37) 2
576 TestAndSet (IndAddr 2)
577 Receive 3
578 Branch 3 (Rel 2)
579 Jump (Rel (-4))
580 Load (ImmValue 38) 4
581 ReadInstr (IndAddr 4)
582 Receive 5
583 Push 5
584 WriteInstr 0 (IndAddr 2)
585 Pop 6
586 PrintOut 6
587 Compute Add 7 0 6
588 Load (IndAddr 6) 6
589 Load (IndAddr 6) 6
590 ComputeI Add 6 1 6
```

```
591 Load (IndAddr 6) 5
592 Push 5
593 Pop 2
594 Compute Decr 2 0 4
595 Push 4
596 Compute Add 7 0 6
597 Load (IndAddr 6) 6
598 Load (IndAddr 6) 6
599 ComputeI Add 6 1 6
600 Pop 2
601 Store 2 (IndAddr 6)
602 Push 2
603 Pop 0
604 Load (IndAddr 7) 7
605 Jump (Rel (-160))
606 Load (IndAddr 7) 7
607 Load (ImmValue 3) 2
608 Compute Sub 7 2 2
609 ComputeI Add 0 1 5
610 ComputeI Gt 5 1 6
611 Branch 6 (Rel 23)
612 Compute Add 7 5 6
613 Load (IndAddr 6) 4
614 Load (IndAddr 2) 3
615 Compute Lt 3 0 6
616 Branch 6 (Rel 2)
617 Store 4 (IndAddr 3)
618 Compute Incr 2 0 2
619 Load (IndAddr 2) 3
620 Compute Lt 3 0 6
621 Branch 6 (Rel 10)
622 Compute Add 3 0 6
623 TestAndSet (IndAddr 6)
624 Receive 6
625 Branch 6 (Rel 2)
626 Jump (Rel (-4))
627 ComputeI Add 3 1 3
628 WriteInstr 4 (IndAddr 3)
629 ComputeI Sub 3 1 3
630 WriteInstr 0 (IndAddr 3)
631 Compute Incr 5 0 5
632 ComputeI Add 2 2 2
633 Jump (Rel (-23))
634 Compute Decr 7 0 2
635 Load (IndAddr 2) 6
636 Load (IndAddr 7) 7
637 Jump (Ind 6)
638 Load (ImmValue 0) 6
```

```
639 Push 6
640 Pop 6
641 Load (ImmValue 33) 2
642 TestAndSet (IndAddr 2)
643 Receive 3
644 Branch 3 (Rel 2)
645 Jump (Rel (-3))
646 Load (ImmValue 34) 4
647 WriteInstr 6 (IndAddr 4)
648 WriteInstr 0 (IndAddr 2)
649 Load (ImmValue 0) 6
650 Push 6
651 Pop 6
652 Load (ImmValue 35) 2
653 TestAndSet (IndAddr 2)
654 Receive 3
655 Branch 3 (Rel 2)
656 Jump (Rel (-3))
657 Load (ImmValue 36) 4
658 WriteInstr 6 (IndAddr 4)
659 WriteInstr 0 (IndAddr 2)
660 Load (ImmValue 0) 6
661 Push 6
662 Pop 6
663 Load (ImmValue 39) 2
664 TestAndSet (IndAddr 2)
665 Receive 3
666 Branch 3 (Rel 2)
667 Jump (Rel (-3))
668 Load (ImmValue 40) 4
669 WriteInstr 6 (IndAddr 4)
670 WriteInstr 0 (IndAddr 2)
671 Load (ImmValue 0) 6
672 Push 6
673 Pop 6
674 Load (ImmValue 37) 2
675 TestAndSet (IndAddr 2)
676 Receive 3
677 Branch 3 (Rel 2)
678 Jump (Rel (-3))
679 Load (ImmValue 38) 4
680 WriteInstr 6 (IndAddr 4)
681 WriteInstr 0 (IndAddr 2)
682 Load (ImmValue 10) 6
683 Push 6
684 Compute Add 7 0 4
685 ComputeI Add 4 1 4
686 Load (ImmValue 1) 5
```



```
687 Pop 3
688 Store 3 (IndAddr 4)
689 Compute Incr 4 0 4
690 Load (ImmValue (-1)) 3
691 Store 3 (IndAddr 4)
692 Compute Incr 4 0 4
693 Load (ImmValue (-1)) 3
694 Store 3 (IndAddr 4)
695 Compute Incr 4 0 4
696 Load (ImmValue 707) 6
697 Push 6
698 Pop 5
699 Store 5 (IndAddr 4)
700 Compute Incr 4 0 4
701 Store 7 (IndAddr 4)
702 Compute Add 4 0 7
703 Load (ImmValue 430) 6
704 Push 6
705 Pop 2
706 Jump (Ind 2)
707 Load (ImmValue 1) 2
708 WriteInstr 2 (DirAddr 0)
709 EndProg
```

## Results

```
1 >>> 0
2 >>> 0
3 >>> 0
4 >>> 0
5 >>> 0
6 >>> 0
7 >>> 0
8 >>> 0
9 >>> 0
10 >>> 0
11 >>> 0
12 >>> 0
13 >>> 0
14 >>> 0
15 >>> 0
16 >>> 0
17 >>> 0
18 >>> 0
19 >>> 0
20 >>> 0
```

## Recursion

### Source

```
1  procedure rec(int i) {
2      if ((i < 3)) {
3          print(i);
4          i = (i + 1);
5          rec(i);
6      } else {
7          print(i);
8      }
9  }
10
11  int i = 0;
12  rec(i);
```

### Generated SprIL

```
0  Branch 1 (Rel 6)
1  TestAndSet (DirAddr 2)
2  Receive 6
3  Branch 6 (Rel 2)
4  Jump (Rel (-3))
5  Jump (Rel 194)
6  ReadInstr (DirAddr 0)
7  Receive 3
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
```

```
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 4) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 1 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 2 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Compute Add 7 0 6
73 Load (IndAddr 6) 6
74 ComputeI Add 6 1 6
75 Load (IndAddr 6) 5
76 Push 5
```

```
77 Load (ImmValue 3) 6
78 Push 6
79 Pop 3
80 Pop 2
81 Compute Lt 2 3 4
82 Push 4
83 Pop 6
84 ComputeI Xor 6 1 6
85 Branch 6 (Rel 67)
86 Compute Add 7 0 4
87 ComputeI Add 4 1 4
88 Store 7 (IndAddr 4)
89 Compute Add 4 0 7
90 Compute Add 7 0 6
91 Load (IndAddr 6) 6
92 Load (IndAddr 6) 6
93 ComputeI Add 6 1 6
94 Load (IndAddr 6) 5
95 Push 5
96 Pop 6
97 PrintOut 6
98 Compute Add 7 0 6
99 Load (IndAddr 6) 6
100 Load (IndAddr 6) 6
101 ComputeI Add 6 1 6
102 Load (IndAddr 6) 5
103 Push 5
104 Load (ImmValue 1) 6
105 Push 6
106 Pop 3
107 Pop 2
108 Compute Add 2 3 4
109 Push 4
110 Compute Add 7 0 6
111 Load (IndAddr 6) 6
112 Load (IndAddr 6) 6
113 ComputeI Add 6 1 6
114 Pop 2
115 Store 2 (IndAddr 6)
116 Push 2
117 Pop 0
118 Compute Add 7 0 6
119 Load (IndAddr 6) 6
120 Load (IndAddr 6) 6
121 ComputeI Add 6 1 6
122 Load (IndAddr 6) 5
123 Push 5
124 Compute Add 7 0 4
```

```
125 ComputeI Add 4 1 4
126 Load (ImmValue 1) 5
127 Pop 3
128 Store 3 (IndAddr 4)
129 Compute Incr 4 0 4
130 Compute Add 7 0 6
131 Load (IndAddr 6) 6
132 Load (IndAddr 6) 6
133 ComputeI Add 6 1 6
134 Store 6 (IndAddr 4)
135 Compute Incr 4 0 4
136 Load (ImmValue (-1)) 3
137 Store 3 (IndAddr 4)
138 Compute Incr 4 0 4
139 Load (ImmValue 150) 6
140 Push 6
141 Pop 5
142 Store 5 (IndAddr 4)
143 Compute Incr 4 0 4
144 Store 7 (IndAddr 4)
145 Compute Add 4 0 7
146 Load (ImmValue 57) 6
147 Push 6
148 Pop 2
149 Jump (Ind 2)
150 Load (IndAddr 7) 7
151 Jump (Rel 14)
152 Compute Add 7 0 4
153 ComputeI Add 4 1 4
154 Store 7 (IndAddr 4)
155 Compute Add 4 0 7
156 Compute Add 7 0 6
157 Load (IndAddr 6) 6
158 Load (IndAddr 6) 6
159 ComputeI Add 6 1 6
160 Load (IndAddr 6) 5
161 Push 5
162 Pop 6
163 PrintOut 6
164 Load (IndAddr 7) 7
165 Load (IndAddr 7) 7
166 Load (ImmValue 3) 2
167 Compute Sub 7 2 2
168 ComputeI Add 0 1 5
169 ComputeI Gt 5 1 6
170 Branch 6 (Rel 23)
171 Compute Add 7 5 6
172 Load (IndAddr 6) 4
```

```
173 Load (IndAddr 2) 3
174 Compute Lt 3 0 6
175 Branch 6 (Rel 2)
176 Store 4 (IndAddr 3)
177 Compute Incr 2 0 2
178 Load (IndAddr 2) 3
179 Compute Lt 3 0 6
180 Branch 6 (Rel 10)
181 Compute Add 3 0 6
182 TestAndSet (IndAddr 6)
183 Receive 6
184 Branch 6 (Rel 2)
185 Jump (Rel (-4))
186 ComputeI Add 3 1 3
187 WriteInstr 4 (IndAddr 3)
188 ComputeI Sub 3 1 3
189 WriteInstr 0 (IndAddr 3)
190 Compute Incr 5 0 5
191 ComputeI Add 2 2 2
192 Jump (Rel (-23))
193 Compute Decr 7 0 2
194 Load (IndAddr 2) 6
195 Load (IndAddr 7) 7
196 Jump (Ind 6)
197 Nop
198 Nop
199 Load (ImmValue 0) 6
200 Push 6
201 Compute Add 7 0 6
202 ComputeI Add 6 1 6
203 Pop 5
204 Store 5 (IndAddr 6)
205 Compute Add 7 0 6
206 ComputeI Add 6 1 6
207 Load (IndAddr 6) 5
208 Push 5
209 Compute Add 7 0 4
210 ComputeI Add 4 2 4
211 Load (ImmValue 1) 5
212 Pop 3
213 Store 3 (IndAddr 4)
214 Compute Incr 4 0 4
215 Compute Add 7 0 6
216 ComputeI Add 6 1 6
217 Store 6 (IndAddr 4)
218 Compute Incr 4 0 4
219 Load (ImmValue (-1)) 3
220 Store 3 (IndAddr 4)
```

```
221 Compute Incr 4 0 4
222 Load (ImmValue 233) 6
223 Push 6
224 Pop 5
225 Store 5 (IndAddr 4)
226 Compute Incr 4 0 4
227 Store 7 (IndAddr 4)
228 Compute Add 4 0 7
229 Load (ImmValue 57) 6
230 Push 6
231 Pop 2
232 Jump (Ind 2)
233 Load (ImmValue 1) 2
234 WriteInstr 2 (DirAddr 0)
235 EndProg
```

## Results

```
1 >>> 0
2 >>> 1
3 >>> 2
4 >>> 3
```

## Simple Concurrency

### Source

```
1 global int num = 5;
2
3 procedure set_four() {
4     (3+(2*(2*(2*332)))));
5     num = 4;
6     print(num);
7 }
8
9 procedure set_six() {
10     num = 6;
11     print(num);
12 }
13
14 fork set_four();
15 fork set_six();
16 join;
17 print(num);
```

**Generated SprIL**

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 223)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
```



```
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 1) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 0 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 1 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Load (ImmValue 3) 6
73 Push 6
74 Load (ImmValue 2) 6
75 Push 6
76 Load (ImmValue 2) 6
77 Push 6
78 Load (ImmValue 2) 6
79 Push 6
80 Load (ImmValue 332) 6
81 Push 6
82 Pop 3
83 Pop 2
84 Compute Mul 2 3 4
85 Push 4
86 Pop 3
87 Pop 2
88 Compute Mul 2 3 4
89 Push 4
90 Pop 3
91 Pop 2
92 Compute Mul 2 3 4
93 Push 4
```

```
94 Pop 3
95 Pop 2
96 Compute Add 2 3 4
97 Push 4
98 Pop 0
99 Load (ImmValue 4) 6
100 Push 6
101 Load (ImmValue 33) 2
102 TestAndSet (IndAddr 2)
103 Receive 3
104 Branch 3 (Rel 2)
105 Jump (Rel (-4))
106 Load (ImmValue 34) 4
107 Pop 6
108 WriteInstr 6 (IndAddr 4)
109 WriteInstr 0 (IndAddr 2)
110 Pop 0
111 Load (ImmValue 33) 2
112 TestAndSet (IndAddr 2)
113 Receive 3
114 Branch 3 (Rel 2)
115 Jump (Rel (-4))
116 Load (ImmValue 34) 4
117 ReadInstr (IndAddr 4)
118 Receive 5
119 Push 5
120 WriteInstr 0 (IndAddr 2)
121 Pop 6
122 PrintOut 6
123 Load (IndAddr 7) 7
124 Load (ImmValue 0) 2
125 Compute Sub 7 2 2
126 ComputeI Add 0 1 5
127 ComputeI Gt 5 0 6
128 Branch 6 (Rel 23)
129 Compute Add 7 5 6
130 Load (IndAddr 6) 4
131 Load (IndAddr 2) 3
132 Compute Lt 3 0 6
133 Branch 6 (Rel 2)
134 Store 4 (IndAddr 3)
135 Compute Incr 2 0 2
136 Load (IndAddr 2) 3
137 Compute Lt 3 0 6
138 Branch 6 (Rel 10)
139 Compute Add 3 0 6
140 TestAndSet (IndAddr 6)
141 Receive 6
```

```
142 Branch 6 (Rel 2)
143 Jump (Rel (-4))
144 ComputeI Add 3 1 3
145 WriteInstr 4 (IndAddr 3)
146 ComputeI Sub 3 1 3
147 WriteInstr 0 (IndAddr 3)
148 Compute Incr 5 0 5
149 ComputeI Add 2 2 2
150 Jump (Rel (-23))
151 Compute Decr 7 0 2
152 Load (IndAddr 2) 6
153 Load (IndAddr 7) 7
154 Jump (Ind 6)
155 Load (ImmValue 1) 2
156 Compute Sub 7 2 2
157 Load (ImmValue 1) 5
158 ComputeI Gt 5 0 6
159 Branch 6 (Rel 7)
160 Load (IndAddr 2) 3
161 Compute Add 7 5 6
162 Store 3 (IndAddr 6)
163 Compute Incr 5 0 5
164 ComputeI Add 2 3 2
165 Jump (Rel (-7))
166 Compute Add 7 0 4
167 ComputeI Add 4 1 4
168 Store 7 (IndAddr 4)
169 Compute Add 4 0 7
170 Load (ImmValue 6) 6
171 Push 6
172 Load (ImmValue 33) 2
173 TestAndSet (IndAddr 2)
174 Receive 3
175 Branch 3 (Rel 2)
176 Jump (Rel (-4))
177 Load (ImmValue 34) 4
178 Pop 6
179 WriteInstr 6 (IndAddr 4)
180 WriteInstr 0 (IndAddr 2)
181 Pop 0
182 Load (ImmValue 33) 2
183 TestAndSet (IndAddr 2)
184 Receive 3
185 Branch 3 (Rel 2)
186 Jump (Rel (-4))
187 Load (ImmValue 34) 4
188 ReadInstr (IndAddr 4)
189 Receive 5
```

```
190 Push 5
191 WriteInstr 0 (IndAddr 2)
192 Pop 6
193 PrintOut 6
194 Load (IndAddr 7) 7
195 Load (ImmValue 0) 2
196 Compute Sub 7 2 2
197 ComputeI Add 0 1 5
198 ComputeI Gt 5 0 6
199 Branch 6 (Rel 23)
200 Compute Add 7 5 6
201 Load (IndAddr 6) 4
202 Load (IndAddr 2) 3
203 Compute Lt 3 0 6
204 Branch 6 (Rel 2)
205 Store 4 (IndAddr 3)
206 Compute Incr 2 0 2
207 Load (IndAddr 2) 3
208 Compute Lt 3 0 6
209 Branch 6 (Rel 10)
210 Compute Add 3 0 6
211 TestAndSet (IndAddr 6)
212 Receive 6
213 Branch 6 (Rel 2)
214 Jump (Rel (-4))
215 ComputeI Add 3 1 3
216 WriteInstr 4 (IndAddr 3)
217 ComputeI Sub 3 1 3
218 WriteInstr 0 (IndAddr 3)
219 Compute Incr 5 0 5
220 ComputeI Add 2 2 2
221 Jump (Rel (-23))
222 Compute Decr 7 0 2
223 Load (IndAddr 2) 6
224 Load (IndAddr 7) 7
225 Jump (Ind 6)
226 Nop
227 Nop
228 Load (ImmValue 5) 6
229 Push 6
230 Pop 6
231 Load (ImmValue 33) 2
232 TestAndSet (IndAddr 2)
233 Receive 3
234 Branch 3 (Rel 2)
235 Jump (Rel (-3))
236 Load (ImmValue 34) 4
237 WriteInstr 6 (IndAddr 4)
```

```
238 WriteInstr 0 (IndAddr 2)
239 TestAndSet (DirAddr 1)
240 Receive 6
241 Branch 6 (Rel 2)
242 Jump (Rel (-3))
243 Load (ImmValue 5) 4
244 Load (ImmValue 0) 5
245 WriteInstr 5 (DirAddr 4)
246 Load (ImmValue 57) 6
247 Push 6
248 Pop 5
249 WriteInstr 5 (DirAddr 3)
250 WriteInstr 0 (DirAddr 2)
251 Load (ImmValue 1) 3
252 ReadInstr (IndAddr 3)
253 Receive 6
254 Branch 6 (Rel 2)
255 Jump (Rel (-3))
256 TestAndSet (DirAddr 1)
257 Receive 6
258 Branch 6 (Rel 2)
259 Jump (Rel (-3))
260 Load (ImmValue 5) 4
261 Load (ImmValue 0) 5
262 WriteInstr 5 (DirAddr 4)
263 Load (ImmValue 155) 6
264 Push 6
265 Pop 5
266 WriteInstr 5 (DirAddr 3)
267 WriteInstr 0 (DirAddr 2)
268 Load (ImmValue 1) 3
269 ReadInstr (IndAddr 3)
270 Receive 6
271 Branch 6 (Rel 2)
272 Jump (Rel (-3))
273 Compute Equal 0 1 6
274 Branch 6 (Rel 4)
275 Load (ImmValue 2) 2
276 PrintOut 2
277 EndProg
278 Load (ImmValue 30) 3
279 Load (ImmValue 0) 2
280 ReadInstr (IndAddr 3)
281 Receive 4
282 Compute Add 2 4 2
283 ComputeI NEq 3 33 6
284 Compute Incr 3 0 3
285 Branch 6 (Rel (-5))
```

```
286 Compute Equal 2 0 6
287 Branch 6 (Rel 2)
288 Jump (Rel (-10))
289 Load (ImmValue 33) 2
290 TestAndSet (IndAddr 2)
291 Receive 3
292 Branch 3 (Rel 2)
293 Jump (Rel (-4))
294 Load (ImmValue 34) 4
295 ReadInstr (IndAddr 4)
296 Receive 5
297 Push 5
298 WriteInstr 0 (IndAddr 2)
299 Pop 6
300 PrintOut 6
301 Load (ImmValue 1) 2
302 WriteInstr 2 (DirAddr 0)
303 EndProg
```

## Results

```
1 >>> 4
2 >>> 6
3 >>> 6
```

## Simple Procedures

### Source

```
1 global int a = 3;
2
3 procedure p0(int c) {
4     a = c;
5     c = (c + 2);
6 }
7
8 int b = 2;
9 print(b); // should print 2
10
11 a = 1;
12
13 p0(b);
14 print(b); // should print 4
15 print(0);
16 print(a); // should print 2
```

## Generated SprIL

```
0 Branch 1 (Rel 6)
1 TestAndSet (DirAddr 2)
2 Receive 6
3 Branch 6 (Rel 2)
4 Jump (Rel (-3))
5 Jump (Rel 134)
6 ReadInstr (DirAddr 0)
7 Receive 3
8 Compute Equal 3 0 6
9 Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
```

```
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Load (ImmValue 4) 2
58 Compute Sub 7 2 2
59 Load (ImmValue 1) 5
60 ComputeI Gt 5 1 6
61 Branch 6 (Rel 7)
62 Load (IndAddr 2) 3
63 Compute Add 7 5 6
64 Store 3 (IndAddr 6)
65 Compute Incr 5 0 5
66 ComputeI Add 2 3 2
67 Jump (Rel (-7))
68 Compute Add 7 0 4
69 ComputeI Add 4 2 4
70 Store 7 (IndAddr 4)
71 Compute Add 4 0 7
72 Compute Add 7 0 6
73 Load (IndAddr 6) 6
74 ComputeI Add 6 1 6
75 Load (IndAddr 6) 5
76 Push 5
77 Load (ImmValue 31) 2
78 TestAndSet (IndAddr 2)
79 Receive 3
80 Branch 3 (Rel 2)
81 Jump (Rel (-4))
82 Load (ImmValue 32) 4
83 Pop 6
84 WriteInstr 6 (IndAddr 4)
85 WriteInstr 0 (IndAddr 2)
86 Pop 0
87 Compute Add 7 0 6
88 Load (IndAddr 6) 6
89 ComputeI Add 6 1 6
90 Load (IndAddr 6) 5
91 Push 5
92 Load (ImmValue 2) 6
93 Push 6
```



```
94 Pop 3
95 Pop 2
96 Compute Add 2 3 4
97 Push 4
98 Compute Add 7 0 6
99 Load (IndAddr 6) 6
100 ComputeI Add 6 1 6
101 Pop 2
102 Store 2 (IndAddr 6)
103 Push 2
104 Pop 0
105 Load (IndAddr 7) 7
106 Load (ImmValue 3) 2
107 Compute Sub 7 2 2
108 ComputeI Add 0 1 5
109 ComputeI Gt 5 1 6
110 Branch 6 (Rel 23)
111 Compute Add 7 5 6
112 Load (IndAddr 6) 4
113 Load (IndAddr 2) 3
114 Compute Lt 3 0 6
115 Branch 6 (Rel 2)
116 Store 4 (IndAddr 3)
117 Compute Incr 2 0 2
118 Load (IndAddr 2) 3
119 Compute Lt 3 0 6
120 Branch 6 (Rel 10)
121 Compute Add 3 0 6
122 TestAndSet (IndAddr 6)
123 Receive 6
124 Branch 6 (Rel 2)
125 Jump (Rel (-4))
126 ComputeI Add 3 1 3
127 WriteInstr 4 (IndAddr 3)
128 ComputeI Sub 3 1 3
129 WriteInstr 0 (IndAddr 3)
130 Compute Incr 5 0 5
131 ComputeI Add 2 2 2
132 Jump (Rel (-23))
133 Compute Decr 7 0 2
134 Load (IndAddr 2) 6
135 Load (IndAddr 7) 7
136 Jump (Ind 6)
137 Nop
138 Nop
139 Load (ImmValue 3) 6
140 Push 6
141 Pop 6
```

```
142 Load (ImmValue 31) 2
143 TestAndSet (IndAddr 2)
144 Receive 3
145 Branch 3 (Rel 2)
146 Jump (Rel (-3))
147 Load (ImmValue 32) 4
148 WriteInstr 6 (IndAddr 4)
149 WriteInstr 0 (IndAddr 2)
150 Load (ImmValue 2) 6
151 Push 6
152 Compute Add 7 0 6
153 ComputeI Add 6 1 6
154 Pop 5
155 Store 5 (IndAddr 6)
156 Compute Add 7 0 6
157 ComputeI Add 6 1 6
158 Load (IndAddr 6) 5
159 Push 5
160 Pop 6
161 PrintOut 6
162 Load (ImmValue 1) 6
163 Push 6
164 Load (ImmValue 31) 2
165 TestAndSet (IndAddr 2)
166 Receive 3
167 Branch 3 (Rel 2)
168 Jump (Rel (-4))
169 Load (ImmValue 32) 4
170 Pop 6
171 WriteInstr 6 (IndAddr 4)
172 WriteInstr 0 (IndAddr 2)
173 Pop 0
174 Compute Add 7 0 6
175 ComputeI Add 6 1 6
176 Load (IndAddr 6) 5
177 Push 5
178 Compute Add 7 0 4
179 ComputeI Add 4 2 4
180 Load (ImmValue 1) 5
181 Pop 3
182 Store 3 (IndAddr 4)
183 Compute Incr 4 0 4
184 Compute Add 7 0 6
185 ComputeI Add 6 1 6
186 Store 6 (IndAddr 4)
187 Compute Incr 4 0 4
188 Load (ImmValue (-1)) 3
189 Store 3 (IndAddr 4)
```

```
190 Compute Incr 4 0 4
191 Load (ImmValue 202) 6
192 Push 6
193 Pop 5
194 Store 5 (IndAddr 4)
195 Compute Incr 4 0 4
196 Store 7 (IndAddr 4)
197 Compute Add 4 0 7
198 Load (ImmValue 57) 6
199 Push 6
200 Pop 2
201 Jump (Ind 2)
202 Compute Add 7 0 6
203 ComputeI Add 6 1 6
204 Load (IndAddr 6) 5
205 Push 5
206 Pop 6
207 PrintOut 6
208 Load (ImmValue 0) 6
209 Push 6
210 Pop 6
211 PrintOut 6
212 Load (ImmValue 31) 2
213 TestAndSet (IndAddr 2)
214 Receive 3
215 Branch 3 (Rel 2)
216 Jump (Rel (-4))
217 Load (ImmValue 32) 4
218 ReadInstr (IndAddr 4)
219 Receive 5
220 Push 5
221 WriteInstr 0 (IndAddr 2)
222 Pop 6
223 PrintOut 6
224 Load (ImmValue 1) 2
225 WriteInstr 2 (DirAddr 0)
226 EndProg
```

## Results

```
1 >>> 2
2 >>> 4
3 >>> 0
4 >>> 2
```

## While

### Source

```
1  int i = 100;
2  while ((i >= 0)) {
3      1;
4      print(i);
5      i = (i - 1);
6  }
```

### Generated SprIL

```
0  Branch 1 (Rel 6)
1  TestAndSet (DirAddr 2)
2  Receive 6
3  Branch 6 (Rel 2)
4  Jump (Rel (-3))
5  Jump (Rel 54)
6  ReadInstr (DirAddr 0)
7  Receive 3
8  Compute Equal 3 0 6
9  Branch 6 (Rel 2)
10 EndProg
11 TestAndSet (DirAddr 2)
12 Receive 6
13 Branch 6 (Rel 2)
14 Jump (Rel (-8))
15 ComputeI Add 1 30 3
16 TestAndSet (IndAddr 3)
17 Receive 6
18 Branch 6 (Rel 2)
19 Jump (Rel (-3))
20 ReadInstr (DirAddr 3)
21 Receive 3
22 Push 3
23 ComputeI Add 7 1 4
24 ReadInstr (DirAddr 4)
25 Receive 5
26 Load (ImmValue 5) 2
27 Compute Equal 5 0 6
28 Branch 6 (Rel 18)
29 ReadInstr (IndAddr 2)
30 Receive 3
31 Store 3 (IndAddr 4)
32 Compute Incr 2 0 2
33 Compute Incr 4 0 4
34 ReadInstr (IndAddr 2)
```

```
35 Receive 3
36 Store 3 (IndAddr 4)
37 Compute Incr 2 0 2
38 Compute Incr 4 0 4
39 ReadInstr (IndAddr 2)
40 Receive 3
41 Store 3 (IndAddr 4)
42 Compute Incr 2 0 2
43 Compute Incr 4 0 4
44 Compute Decr 5 0 5
45 Jump (Rel (-18))
46 Load (ImmValue 54) 5
47 Store 5 (IndAddr 4)
48 Compute Incr 4 0 4
49 Store 7 (IndAddr 4)
50 Compute Add 4 0 7
51 Pop 2
52 WriteInstr 0 (DirAddr 1)
53 Jump (Ind 2)
54 ComputeI Add 1 30 3
55 WriteInstr 0 (IndAddr 3)
56 Jump (Abs 9)
57 Nop
58 Nop
59 Load (ImmValue 100) 6
60 Push 6
61 Compute Add 7 0 6
62 ComputeI Add 6 1 6
63 Pop 5
64 Store 5 (IndAddr 6)
65 Compute Add 7 0 6
66 ComputeI Add 6 1 6
67 Load (IndAddr 6) 5
68 Push 5
69 Load (ImmValue 0) 6
70 Push 6
71 Pop 3
72 Pop 2
73 Compute GtE 2 3 4
74 Push 4
75 Pop 6
76 ComputeI Xor 6 1 6
77 Branch 6 (Rel 35)
78 Compute Add 7 0 4
79 ComputeI Add 4 2 4
80 Store 7 (IndAddr 4)
81 Compute Add 4 0 7
82 Load (ImmValue 1) 6
```

```
83  Push 6
84  Pop 0
85  Compute Add 7 0 6
86  Load (IndAddr 6) 6
87  ComputeI Add 6 1 6
88  Load (IndAddr 6) 5
89  Push 5
90  Pop 6
91  PrintOut 6
92  Compute Add 7 0 6
93  Load (IndAddr 6) 6
94  ComputeI Add 6 1 6
95  Load (IndAddr 6) 5
96  Push 5
97  Load (ImmValue 1) 6
98  Push 6
99  Pop 3
100 Pop 2
101 Compute Sub 2 3 4
102 Push 4
103 Compute Add 7 0 6
104 Load (IndAddr 6) 6
105 ComputeI Add 6 1 6
106 Pop 2
107 Store 2 (IndAddr 6)
108 Push 2
109 Pop 0
110 Load (IndAddr 7) 7
111 Jump (Rel (-46))
112 Load (ImmValue 1) 2
113 WriteInstr 2 (DirAddr 0)
114 EndProg
```

## Results

```
1  >>> 100
2  >>> 99
3  >>> 98
4  >>> 97
5  >>> 96
6  >>> 95
7  >>> 94
8  >>> 93
9  >>> 92
10 >>> 91
11 >>> 90
12 >>> 89
13 >>> 88
```

```
14 >>> 87
15 >>> 86
16 >>> 85
17 >>> 84
18 >>> 83
19 >>> 82
20 >>> 81
21 >>> 80
22 >>> 79
23 >>> 78
24 >>> 77
25 >>> 76
26 >>> 75
27 >>> 74
28 >>> 73
29 >>> 72
30 >>> 71
31 >>> 70
32 >>> 69
33 >>> 68
34 >>> 67
35 >>> 66
36 >>> 65
37 >>> 64
38 >>> 63
39 >>> 62
40 >>> 61
41 >>> 60
42 >>> 59
43 >>> 58
44 >>> 57
45 >>> 56
46 >>> 55
47 >>> 54
48 >>> 53
49 >>> 52
50 >>> 51
51 >>> 50
52 >>> 49
53 >>> 48
54 >>> 47
55 >>> 46
56 >>> 45
57 >>> 44
58 >>> 43
59 >>> 42
60 >>> 41
61 >>> 40
```

```
62 >>> 39
63 >>> 38
64 >>> 37
65 >>> 36
66 >>> 35
67 >>> 34
68 >>> 33
69 >>> 32
70 >>> 31
71 >>> 30
72 >>> 29
73 >>> 28
74 >>> 27
75 >>> 26
76 >>> 25
77 >>> 24
78 >>> 23
79 >>> 22
80 >>> 21
81 >>> 20
82 >>> 19
83 >>> 18
84 >>> 17
85 >>> 16
86 >>> 15
87 >>> 14
88 >>> 13
89 >>> 12
90 >>> 11
91 >>> 10
92 >>> 9
93 >>> 8
94 >>> 7
95 >>> 6
96 >>> 5
97 >>> 4
98 >>> 3
99 >>> 2
100 >>> 1
101 >>> 0
```