

Final Exam

● Graded

Student

Total Points

71 / 102 pts

Question 1

Problem 1

19 / 20 pts

1.1

a

2 / 2 pts

 - 0 pts Correct**- 1 pt** Click here to replace this description.

1.2

b

3 / 3 pts

 - 0 pts Correct**- 1 pt** Click here to replace this description.**- 2 pts** Wrong shape and not properly labelled**- 1 pt** Wrong shape in the oxide**- 1 pt** Wrong shape in p-Si

1.3

c

1 / 1 pt

 - 0 pts Correct**- 0.5 pts** Correct formula but wrong application**- 0 pts** OK based on prior work**- 1 pt** Incorrect

1.4

d

3 / 3 pts

 - 0 pts Correct**- 3 pts** Totally incorrect**- 1 pt** Close but....**- 0 pts** Based on prior work**- 2 pts** Wrong but good effort**- 3 pts** No work shown / no attempt

1.5

e

3 / 3 pts

- 0 pts Correct

- 2 pts Incorrect but good effort. Wrong formulation.

✓ - 0 pts OK but this is the hard way and you do not know the bias.

- 3 pts No attempt

- 3 pts Incorrect

but there is a much simpler way based on the voltage drop in the silicon depletion layer

1.6

f

2 / 2 pts

✓ - 0 pts Correct

- 1 pt state of the interface is wrong and credit given for prior work

- 0 pts State of the interface is correct and credit given for prior work on depletion layer width

- 1 pt State of the Is/Sio@ interface is correct but depletion layer width is qrong

- 2 pts No attempt

1.7

g

3 / 3 pts

- 0 pts Correct

- 2 pts Wrong approach but good effort

- 3 pts Completely wrong

- 3 pts No attempt

- 1 pt Right approach but flawed formulation

✓ - 0 pts interesting approach but may have a flaw because you do not know the applied bias

1.8

h

2 / 3 pts

- 0 pts Correct

✓ - 1 pt It is just the oxide capacitance by intuition. It is an oxide layer between two inversion layers

- 2 pts Wrong formulation

- 3 pts No attempt

Question 2

Problem 2

20 / 20 pts

2.1

a

3 / 3 pts

✓ - 0 pts Correct

- 1 pt No need for calculations and tox is incorrect
- 2 pts Wrong formulation and numbers but good effort. No need for calculations for threshold voltage and flatland voltage
- 3 pts Wrong formulation
- 0.5 pts Wrong units / scale for oxide thickness
- 2 pts Only one item correct
- 1 pt Oxide thickness calculation wrong
- 1 pt Threshold voltage incorrect

2.2

b

3 / 3 pts

✓ - 0 pts Correct

- 2 pts No inversion layer included as source of free carriers. Wrong formulation
- 3 pts No attempt or effort
- 0 pts Mostly correct. Correct formulation. Error including V_DS in the expression.
- 1 pt Almost correct formulation. Did not use inversion layer charge density.
- 2.5 pts Wrong formulation but good effort

2.3

c

2 / 2 pts

✓ - 0 pts Correct

- 2 pts Wrong formulation or no effort
- 1 pt right formulation but error in solving problem resulting in incorrect expression

2.4

d

3 / 3 pts

✓ - 0 pts Correct

- 3 pts Wrong formulation or no effort
- 2 pts Wrong operating Regime
- 1 pt Wright formulation, slight error

2.5

e

3 / 3 pts

✓ - 0 pts Correct

- 3 pts Not attempt to provide an answer

- 2 pts Explanation does not provide the reason why there's is a difference in the models

- 1 pt The explanation failed to account for the impact of the applied voltage on the emersion layer charge as a function of position.

2.6

f

2 / 2 pts

✓ - 0 pts Correct

- 2 pts No attempt

- 2 pts In correct expression

- 1 pt Incorrect expression but a clear attempt.

2.7

g

4 / 4 pts

✓ - 0 pts Correct

- 1 pt Click here to replace this description.

- 2 pts Wrong formulation but attempt made to get average E field

- 3 pts Wrong formulation

- 2.5 pts Wrong formulation but an attempt was made to solve the problem

- 3.5 pts No real attempt to solve the problem.

- 1.5 pts Click here to replace this description.

- 0.5 pts Click here to replace this description.

- 4 pts No attempt or totally incorrect

- 0 pts Largely correct but slight error

Question 3

Problem 3

6 / 20 pts

3.1 a 2 / 4 pts

- 0 pts Correct

✓ - 2 pts Incorrect but well argued

- 1 pt right conclusion but reasoning does not address why SCE is controlled.

- 3 pts Click here to replace this description.

- 0 pts Click here to replace this description.

- 4 pts No attempt at solving the problem

3.2 b 4 / 4 pts

✓ - 0 pts Correct

- 2 pts Incorrect but well reasoned.

- 4 pts No attempt at solving the problem

- 1 pt Conclusion rather off the mark though the arguments are well reasoned.

- 1 pt The explanation is not clear.

- 0 pts Click here to replace this description.

3.3 c 0 / 4 pts

- 0 pts Correct

- 1 pt Click here to replace this description.

- 2 pts incorrect but well reasoned.

- 3 pts wrong conclusion but also no reasons given

✓ - 4 pts Click here to replace this description.

3.4 d 0 / 4 pts

- 0 pts Correct

- 1 pt incomplete answer

- 2 pts It is not clear what your conclusion is and what your reasons are

- 3 pts Click here to replace this description.

✓ - 4 pts No attempt to solve the problem

- 0 pts OK but the explanation is inadequate

- 0 pts Correct

- 1 pt Wrong formulation but excellent explation of position taken

- 2 pts Wrong formulation but reasonable explanation of position taken

- 3 pts Wrong formulation bad explanation of position taken

✓ - 4 pts Click here to replace this description.

- 0 pts OK

Question 4

Problem 4

9 / 20 pts

4.1

a

1 / 2 pts

+ 2 pts Correct

✓ + 1 pt Correct expression for depletion region in equilibrium

+ 1 pt Correct Φ_B

✓ + 0 pts Check official answer

4.2

b

6 / 6 pts

✓ + 6 pts Correct

+ 0 pts Check official answer

+ 2 pts Correct minority carrier concentration in equilibrium

+ 2 pts Law of the junction

+ 2 pts Correct math

4.3

c

2 / 4 pts

+ 4 pts Correct

+ 2 pts Correct E field in depletion regions

+ 2 pts Correct E field in QNR

✓ + 0 pts Check official answer

💬 + 2 pts The first answer was correct

4.4

d

0 / 4 pts

+ 4 pts Correct

+ 2 pts Diffusion current equation

+ 1 pt Correct boundary conditions

+ 1 pt Correct sign for emitter current.

✓ + 0 pts Check official answer

4.5

e

0 / 2 pts

+ 2 pts Correct

+ 1 pt Correct answer, no/wrong explanation

✓ + 0 pts Check official answer

4.6

f

0 / 2 pts

+ 2 pts Correct

+ 1 pt Only one correct answer

✓ + 0 pts Check official solution

Question 5

Problem 5

17 / 22 pts

5.1

a

3 / 3 pts

 + 3 pts Correct

+ 2 pts Correct answer, no/wrong explanation

+ 0 pts Check official answer

5.2

b

3 / 3 pts

 + 3 pts Correct

+ 1 pt Correct expression for depletion region

+ 1 pt Correct value for depletion region

+ 1 pt Correct comparison

+ 0 pts Check official answer

5.3

c

11 / 12 pts

 + 2 pts Correct charge density at the gate contacts + 2 pts Correct charge density in depletion region + 1 pt Correct E field in left-side oxide + 1 pt Correct use of different dielectric constants + 1 pt Correct E field in depletion region + 1 pt Correct E field in right-side oxide + 1 pt Correct potential in oxide + 2 pts quadratic potential in depletion region

+ 1 pt No potential difference between gate electrodes

+ 0 pts Check official solution

5.4

d

0 / 2 pts

+ 2 pts Correct (even if wrong numerical value)

+ 1 pt Correct formula

 + 0 pts Check official solution

+ 2 pts Correct (even if wrong numerical value)

+ 1 pt Correct expression for V_t

✓ + 0 pts Check official solution

Massachusetts Institute of Technology

6.012 Nanoelectronics and Computation Systems Fall Term 2021

Final Examination

Wednesday, December 15, 2021

Total Points: 100

Time Limit: 180 minutes

NAME _____

Recitation Time _____

10 AM

Question	Points
1	
2	
3	
4	
5	
Total Points (out of 100)	

General guidelines (please read carefully before starting):

- Make sure to write your name in the space provided above.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back of the previous page.
- You have 180 minutes to complete the final examination.
- Where required, make reasonable approximations and *state them*.
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. N_d , n_o , etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature.

$$n_i = 1.0 \times 10^{10} \text{ cm}^{-3}$$

$$kT/q = 0.026 \text{ V}$$

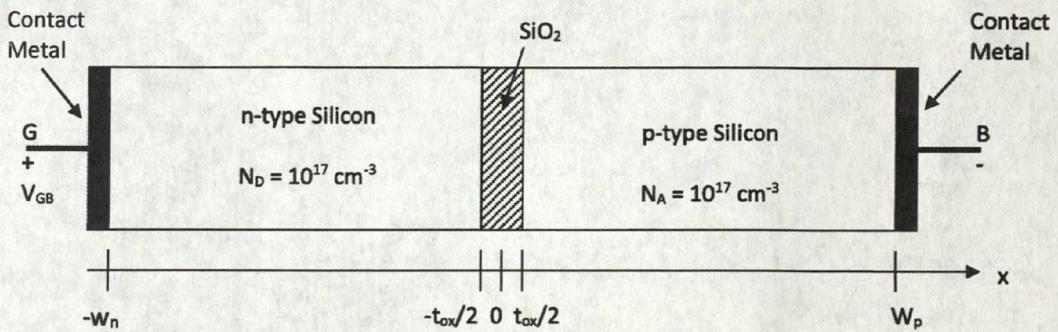
$$q = 1.60 \times 10^{-19} \text{ C}$$

$$\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$$

$$\epsilon_s = 11.7 \quad \epsilon_o = 1.04 \times 10^{-12} \text{ F/cm}$$

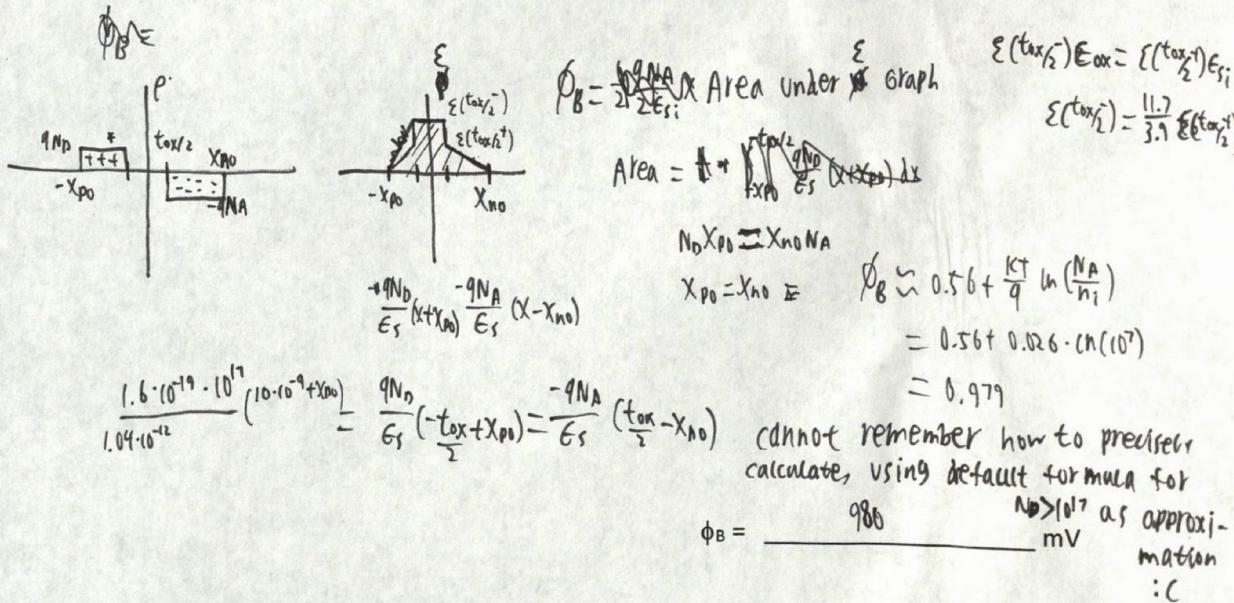
$$\epsilon_{ox} = 3.9 \quad \epsilon_o = 3.45 \times 10^{-13} \text{ F/cm}$$

Problem 1 Semiconductor Electrostatics, pn junction and MOS junction [20 points]

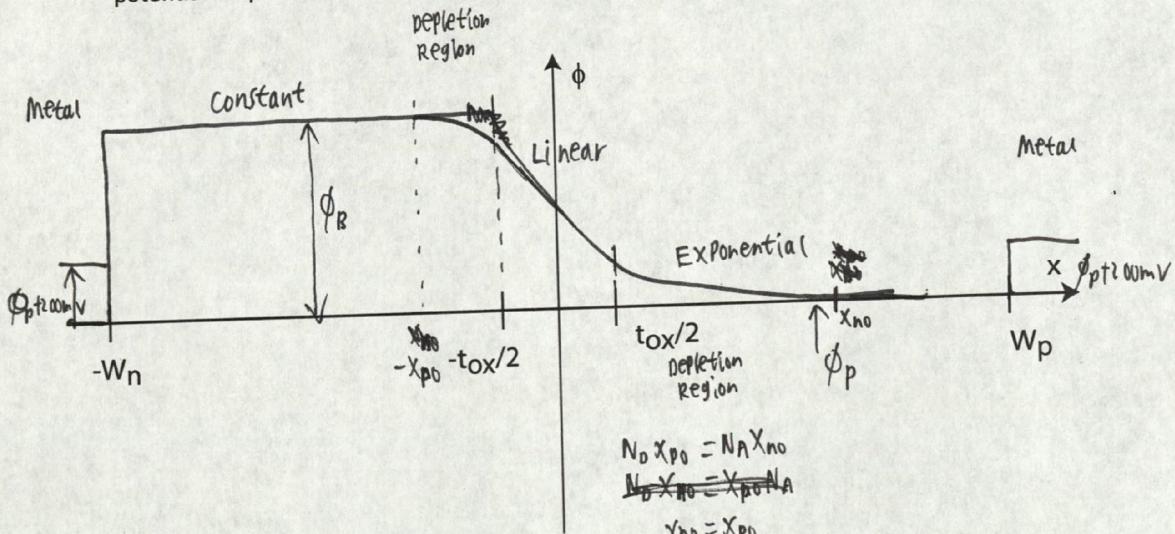


Consider the Semiconductor-Oxide-Semiconductor (SOS) structure illustrated above. It resulted from a mistake made by a 6.152 student that was trying to make n⁺-Si-gate/oxide/p-Si substrate (MOS) structure. The SOS structure which resulted is an n-Si-gate/oxide/p-Si substrate (MOS) structure. Your job as a device engineer is to analyze this structure. All of the dimensions and doping levels you will need to work this problem are indicated in the figure. The oxide thickness, t_{ox} , is 20 nm; the electrostatic potential in the metal relative to intrinsic Si potential is +200 mV. Assume that the electrostatics of this structure can be modeled using the depletion approximation formulation we have used with the p-n junction and the MOSFET.

- (a) Assuming that $V_{GB} = 0 \text{ V}$, what is the electrostatic potential drop, ϕ_B , between the n-type silicon and in the p-type silicon in the quasi-neutral regions (i.e., far from the contacts and far from semiconductor-oxide interface)? Show your work. [2 points]



- (b) On the axes provided below sketch the electrostatic potential through this structure moving from G to B assuming that $V_{GB} = 0$ V. Indicate the general features of the potential variation and transition region widths, but do not try to quantify the transition region widths or relative potential drops at interfaces. Include the metal layer in your sketch. [3 points]



- (c) What is the flat band voltage, V_{FB} , for this device? [1 point]

$$V_{FB} = -\phi_B = -0.839 - 0.980 \text{ V}$$

Now consider this structure when a voltage, V_{GB} , is applied bringing the surface of the p-type silicon at $x = t_{ox}/2$ just above the threshold of inversion, i.e. a few mV beyond the threshold voltage.

- (d) What is the potential drop across the depletion region of the p-Si ($\Delta\phi = \phi(t_{ox}/2) - \phi(x_p)$) with this applied bias? {Note that x_p denotes the edge of the depletion region in the p-Si} [3 points]

$$\Delta\phi = 2\phi_p = 2 \frac{kT}{q} \ln \frac{N_A}{N_i} = 2 \cdot 0.026 \ln(10^7)$$

$$\Delta\phi = \phi(t_{ox}/2) - \phi(x_p) = \underline{\quad 0.839 \quad} \text{ V}$$

- (e) What is the width of the depletion region in the p-type silicon, $x_p - t_{ox}/2$, with this applied bias?

{Note that x_p denotes the edge of the depletion region in the p-Si} [3 points]

$$X_d = \frac{\epsilon_s}{C_{ox}} \left[\sqrt{1 + 2 \frac{C_{ox}^2 (\phi_B + 2\phi_p)}{\epsilon_s q N_A}} - 1 \right]$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \cdot 10^{-13}}{20 \cdot 10^{-9}}$$

$$\phi_B = 0.98 \text{ V} \quad 2\phi_p = 0.938 \text{ V}$$

$$= 15 \text{ } \mu\text{m}$$

$$x_p - t_{ox}/2 = \underline{\hspace{2cm} 15 \hspace{2cm}} \mu\text{m}$$

- (f) What is the condition of the surface of the n-type silicon at $x = -t_{ox}/2$ with this applied bias?

Select a condition and provide the corresponding depletion layer width in the n-Si ($x_n - t_{ox}/2$) assuming that $-x_n$ denotes the edge of the depletion region in n-Si: [2 points]

- Accumulated
 Depleted Same doping as p-type, so should be symmetrical
 Inverted

$$x_n - t_{ox}/2 = \underline{\hspace{2cm} 15 \hspace{2cm}} \mu\text{m}$$

Problem 1

(g) What is the potential drop across the oxide with this bias applied? [3 points]

$$V_T = V_{FB} + 2\phi_p + \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_A (2\phi_p)}$$

$$\Delta\phi = V_T - 2\phi_p = V_{FB} + \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_A (2\phi_p)} \\ = -9.80 - 0.98 + 0.0097$$

$$V_T - V_{FB} = 2 \cdot (2\phi_p) + \Delta\phi$$

$$\Delta\phi = V_T - V_{FB} - 2 \cdot (2\phi_p)$$

$$\Delta\phi \approx \epsilon \Delta\phi = \epsilon_{ox} \cdot t_{ox} = \frac{qN_A}{\epsilon_{ox}} (30 \text{ nM}) \cdot t_{ox} \\ = 0.028 \text{ V}$$

$$\Delta\phi = \phi(-t_{ox}/2) - \phi(t_{ox}/2) = \underline{\hspace{10em}} 0.028 \text{ V } \underline{\hspace{10em}}$$

(h) What is the incremental capacitance per unit area of this structure when it is biased with V_{GB} just above threshold of inversion in the p-Si? [3 points]

$$C = C_{ox} + 2 \cdot \frac{\epsilon_{si}}{x_p} - \frac{\epsilon_{ox}}{t_{ox}} + 2 \cdot \underline{\hspace{10em}}$$

$$\frac{F}{m} \cdot \frac{n}{cm}$$

$$C = \left(\frac{1}{C_{ox}} + \frac{2}{C_{si}} \right)^{-1} = \left(\frac{1}{\epsilon_{ox} \cdot t_{ox}} + \frac{2 \cdot x_p}{\epsilon_{si}} \right)^{-1} = 3.46 \cdot 10^{-8} \text{ F/m} = 3.46 \cdot 10^{-7} \text{ F/cm}$$

$$C_{\text{structure}} = \underline{\hspace{10em}} 3.46 \cdot 10^{-7} \text{ F/cm}^2 \underline{\hspace{10em}}$$

End of Problem 1

Problem 2 MOSFET [20 points]

The structure shown in Figure 2(a) below is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The semiconductor is silicon while the insulator (oxide) is silicon dioxide. A capacitance voltage measurement was taken and the result is shown in Figure 3(b). The gate width $W = 5 \mu\text{m}$, the gate length is $L = 0.25 \mu\text{m}$ and electron mobility in the channel under inversion is $\mu_N = 400 \text{ cm}^2/\text{V}\cdot\text{s}$.

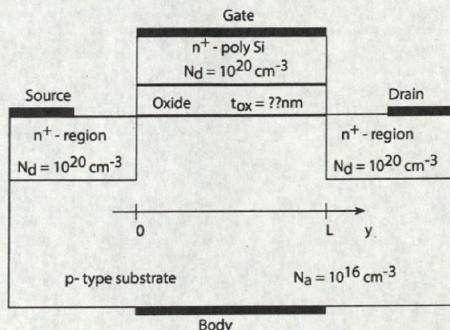


Figure 2(a)

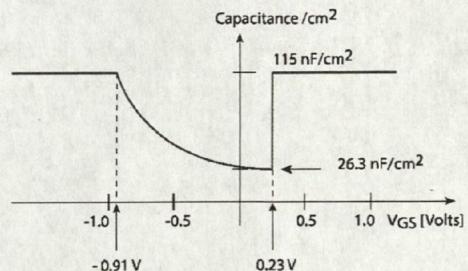


Figure 2(b)

- (a) From the plot, determine the threshold voltage and flat band voltages, and the oxide thickness. [3 points]

$$C = \frac{\epsilon_0}{t_{ox}} \quad \text{when } V_{GS} < V_{FB}$$

$$115 \text{ nF/cm}^2 = \frac{3.45 \cdot 10^{-13} \text{ F/cm}^2}{t_{ox}}$$

$$t_{ox} = \frac{3.45 \cdot 10^{-13} \text{ F/cm}^2}{115 \text{ nF/cm}^2} = 3 \cdot 10^{-7} \text{ m} = 0.03 \mu\text{m}$$

$$t_{ox} = \sqrt{\frac{\epsilon_0}{3 \cdot 10^{-6} \text{ cm} \cdot \frac{10^{-13}}{\text{cm}}}} = 3 \cdot 10^{-7} \text{ m} = 0.03 \mu\text{m}$$

$$V_{FB} = -0.91 \text{ V}$$

$$V_T = 0.23 \text{ V}$$

$$t_{ox} = 3 \cdot 10^{-7} \text{ m} = 0.03 \mu\text{m}$$

Problem 2

- (b) What is the expression for the linear resistance, of the channel in Ohm under conditions: $V_{GS}=3$ V, $V_{DS}=0$ V, and $V_{BS}=0$ V. [3 points]

Linear Regime

$$I_D = \frac{W}{L} \mu_n C_{ox} [V_{GS} - V_T] V_{DS}$$

$$R_{SD} = \frac{V_{DS}}{I_D} = \left(\frac{W}{L} \mu_n C_{ox} [V_{GS} - V_T] \right)^{-1} = \left(\frac{5}{0.25} \cdot 400 \frac{\text{cm}^2}{\text{Vs}} [3 - 0.23] \text{V} \right)^{-1} \cdot 115 \frac{\text{nF}}{\text{cm}^2} = \frac{(0.0025 \frac{\text{nF}}{\text{s}})^{-1}}{0.025} = 400 \frac{\text{s}}{\text{F}}$$

$$R_{SD} = \frac{0.0025 \frac{1}{\text{s}}}{400 \frac{\text{s}}{\text{F}}} = 0.00000625 \Omega$$

- (c) For $V_{DS}=0.5$ V and everything else the same as in question (b) write an expression for the current $I_{D,R}$ that would flow assuming the value of R_{SD} is the same as in (b) throughout the channel. [2 points]

~~$V_{GS} = V_T = 2.77$~~

Assuming constant R_{SD} , \rightarrow Linear Regime

~~$V_{DS} \approx V_G - V_T$~~

$$I_{D,R} = \frac{W}{L} \mu_n C_{ox} [V_{GS} - V_T] V_{DS}$$

$$\approx 0.00127 \text{A}$$

- (d) Now write an expression for the current I_D under the conditions in question (c) but treating the device as a proper MOSFET operating in the appropriate operating region. [3 points]

Triode Regime

$$I_D = \frac{W}{L} M_n C_{ox} \left[V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}$$

$$= \cancel{0.0012A} \approx 0.001159 A$$

$$I_D = \frac{W}{L} M_n C_{ox} \left[V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}$$

- (e) Compare your answers in (c) and (d) and briefly (no more than a maximum of 100 words) explain their difference. [3 points]

For (c), because we are assuming constant resistance across the channel, it is a linear function, while for (d), because we are operating in the triode regime, it is no longer linear, but depends on V_{DS}^2 . For (d), resistance increase ~~non-uniformly~~ across the channel, resulting in a lower current compared to (c)

Problem 2

- (f) Write an expression for the charge density of electrons at the source end $Q_N(y=0)$ under the bias conditions: $V_{GS}=3$ V, $V_{DS}=0.5$ V, and $V_{BS}=0$ V. [2 points]

$$Q_N(y=0) = -C_{ox} [V_{GS} - V_T] = -(15 \text{ NF/cm}^2) [3 - 0.23] = -3.19 \cdot 10^{-7} \frac{\text{F} \cdot \text{V}}{\text{cm}^2}$$

$$-C_{ox} [V_{GS} - V_T]$$

$$Q_N(y=0) = \frac{-3.19 \cdot 10^{-7} \frac{\text{F} \cdot \text{V}}{\text{cm}^2}}{}$$

- (g) What is the lateral electrostatic field at the source end $E_y(y=0)$ under the bias conditions: $V_{GS}=3$ V, $V_{DS}=0.5$ V, and $V_{BS}=0$ V.? [You only need to give us an expression]. [4 points]

$$\{ = \frac{\Delta V}{\Delta L}$$

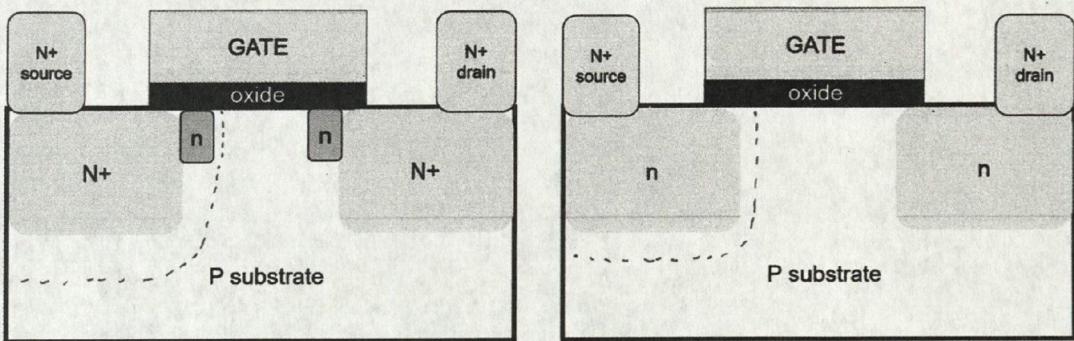
$$E_y(y=0) = \underline{\hspace{10cm}}$$

End of Problem 2

Problem 3: Thinking On Your Feet about MOSFETs [20 points]

A new PhD student wants to come up with some fresh, new ideas to impress the world. The student came up with the following ideas – can you help the new student vet the ideas?

To simplify the fabrication process of a MOSFET, the student wants to modify the Lightly Doped Drain (LDD) process (shown below on the left). Instead of having 2 doped regions (N+ source/drain and N LDD regions), student decided s/he could just have one single region doped N (shown on the right).



- a) [4 points] Will the student's transistor be worse, just as effective, or even more effective compared to regular LDD at controlling short channel effects? Explain.

It would be worse. Without the ~~LDD~~ LDD region, the voltage at the p-n interface on drain side is higher, amplifying CDM, drain induced barrier lowering, and other short channel ~~effe~~ effects. His resistance is also higher, which means more power use.

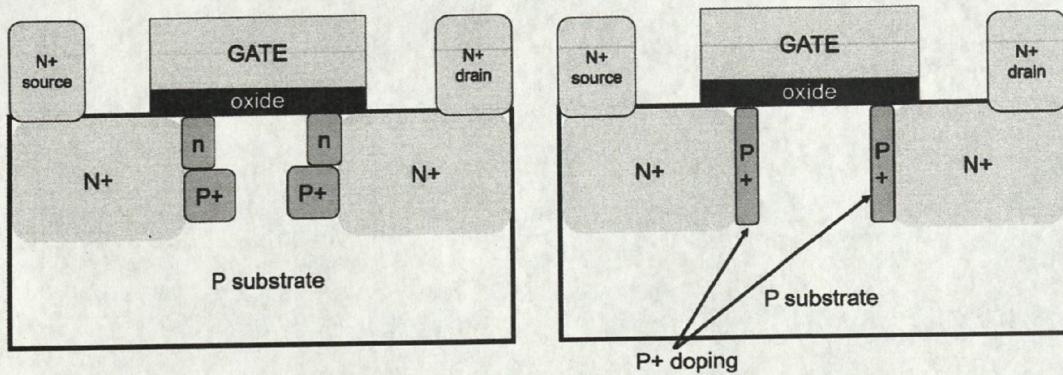
- b) [4 points] Is his/her idea a good idea? Explain.

No, besides the reasons mentioned above, the student's solution also has a lower barrier in the body, ~~which was~~ due to the lower uniform doping, causing leakage energy to increase.



Problem 3

When the student looked at a device that has LDD and halo doping (below, left), it looked like a bunch of extra doping steps. The student thinks LDD and halo doping can be combined to make the device below (below, right).

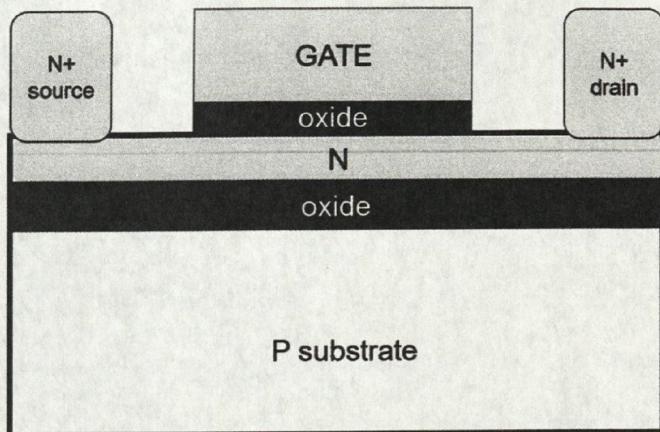


- c) [4 points] Will his/her approach still help to improve charge sharing factor (CSF)?

No, with the

- d) [4 points] Is the student's approach smart? Or will it have unintended consequences?

- e) [4 points] The student now decided to go even simpler – and just have a SINGLE doping under the gate, just N, separated from the substrate by a thick layer of oxide.



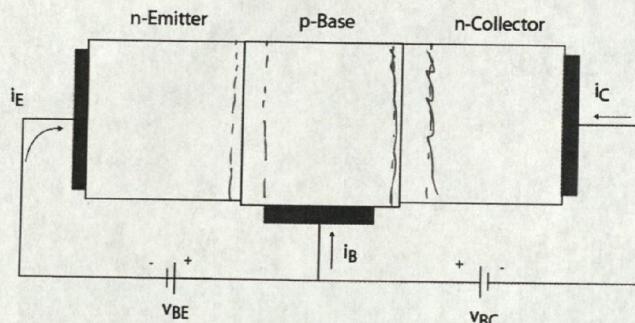
Can this still operate as a transistor? Explain why or not why.

End of Problem 3

Problem 4 Bipolar Junction Transistor (BJT) [20 points]

If you don't remember anything about BJT's... DON'T WORRY. We will walk you through the analysis. A BJT is just two pn diodes back-to-back...

Consider an npn Si-based bipolar junction transistor operating at 300 K with the following parameters:



$N_{dE} = 10^{18} \text{ cm}^{-3}$ (doping in emitter)
 $N_{dB} = 10^{17} \text{ cm}^{-3}$ (doping in base)
 $N_{dC} = 10^{16} \text{ cm}^{-3}$ (doping in collector)
 $W_E = 1 \mu\text{m}$ (width of emitter)
 $W_B = 1 \mu\text{m}$ (width of base)
 $W_C = 1 \mu\text{m}$ (width of collector)
 $D_{nB} = 20.0 \text{ cm}^2\text{s}^{-1}$ (diffusion coefficient for electrons in base)
 $D_{pE} = 10.0 \text{ cm}^2\text{s}^{-1}$ (diffusion coefficient for holes in emitter)
 $\epsilon_{Si} = 11.7 \times 8.85 \times 10^{-14} \text{ Fcm}^{-1}$
Emitter area, $A_E = 100 \mu\text{m} \times 100 \mu\text{m}$

Unless indicated otherwise, assume that the transistor is biased with a base-emitter voltage, V_{BE} , of 0.72 V and a base-collector voltage, V_{BC} , of -0.48 V. Also, independently of the bias that you apply to the transistor, you can assume that the minority carrier concentration at the contacts is equal to the one in thermal equilibrium.

- (a) [2 points] Calculate the width of the depletion region at the emitter-base junction.

Can use PN junction formula

$$X_{dBE} = \sqrt{\frac{2\epsilon_{Si} N_A p_B}{q}} \cdot \sqrt{1 - \frac{V_B}{p_B}} - 4.59 \cdot 10^{-6} \text{ m}$$

$$p_B = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$= 0.898 \text{ V}$$

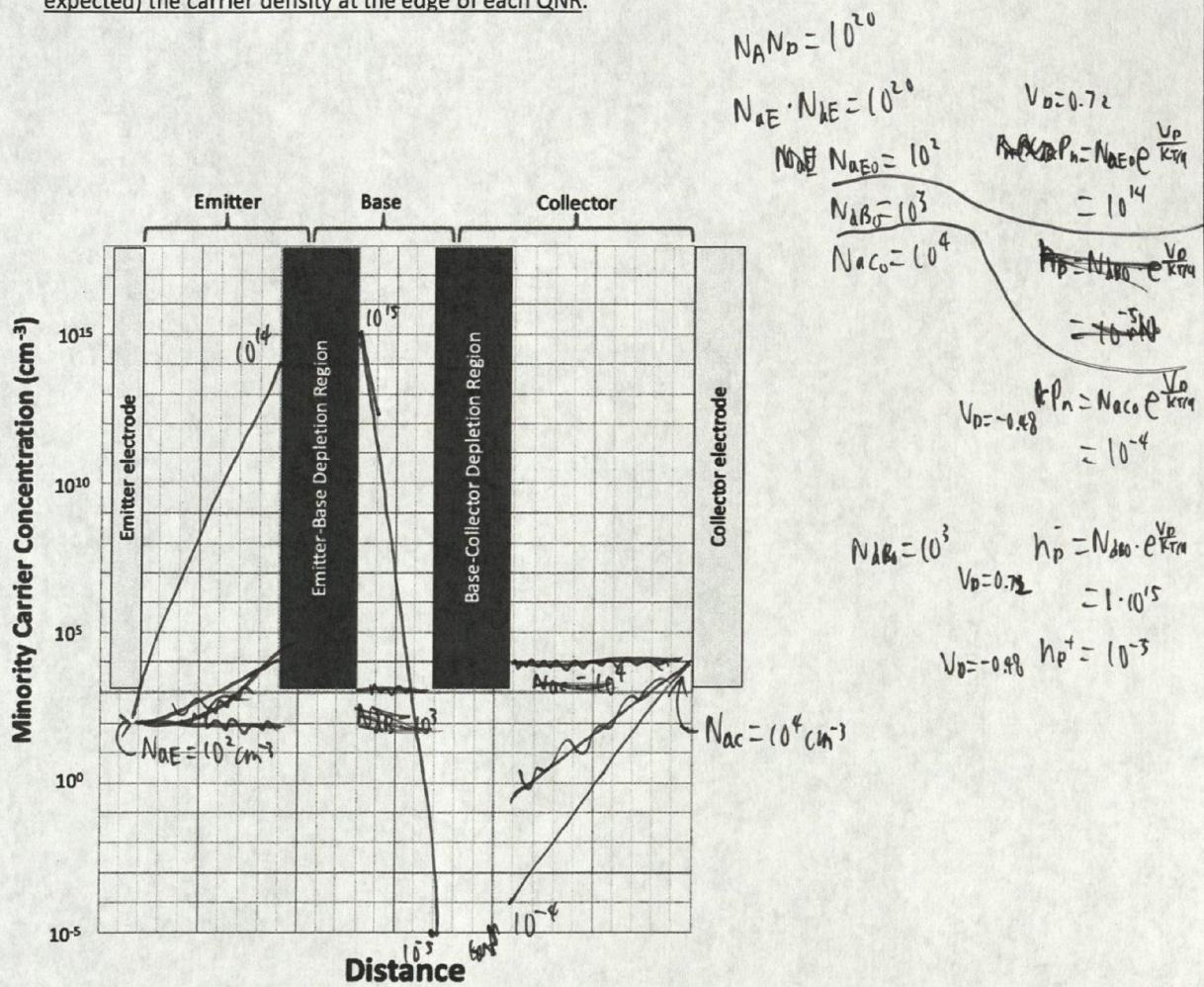
$$X_{dA} = \sqrt{\frac{2\epsilon_{Si} (N_A + N_D) p_B}{q N_A N_D}}$$

$$X_{dBC} = X_{dA} \sqrt{1 - \frac{V_B}{p_B}} = 5 \cdot 10^{-6} \text{ m}$$

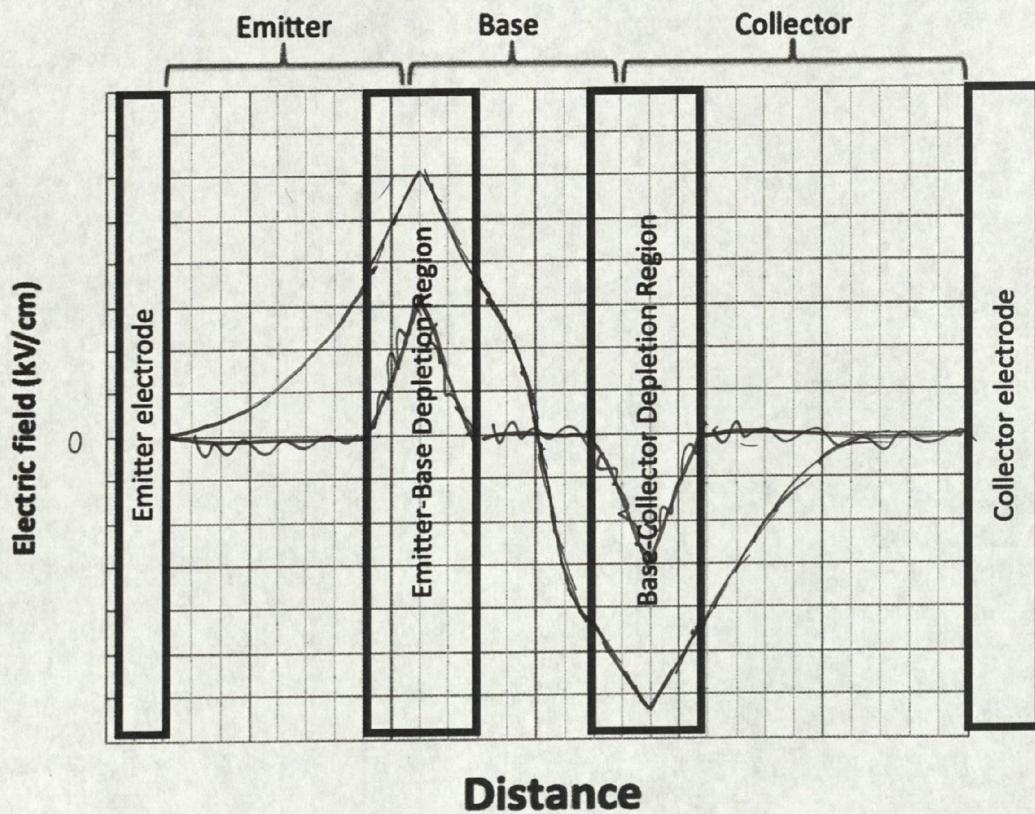
5 μm

$$x_{dBE} = \frac{4.59 \cdot 10^{-6} \text{ m}}{5 \cdot 10^{-6} \text{ m}} = 4.59 \text{ μm}$$

- (b) [6 points] Plot the minority carrier distribution in the quasi-neutral-regions (QNR) regions of the transistor, that is outside of the depletion regions. Make sure to label (i.e. numerical values are expected) the carrier density at the edge of each QNR.



- (c) [4 points] Sketch (i.e. no need to calculate numerical values) the electric field in the different regions of the transistor.



Problem 4

(d) [4 points] Calculate an expression for the emitter current for the bias conditions: $V_{BE}=0.72$ V, $V_{BC}=-0.48$ V. You don't need to provide a numerical value. You can assume that the minority carrier concentration changes linearly within the QNRs of the device, and that the emitter current is dominated by electrons injected into the base region and that diffuse there.

Problem 4

(e) [2 points] How will the emitter current change as you reduce the width of the base region?

It will increase It will decrease It will stay constant

Because... There is less area, as $I \propto J \cdot A$

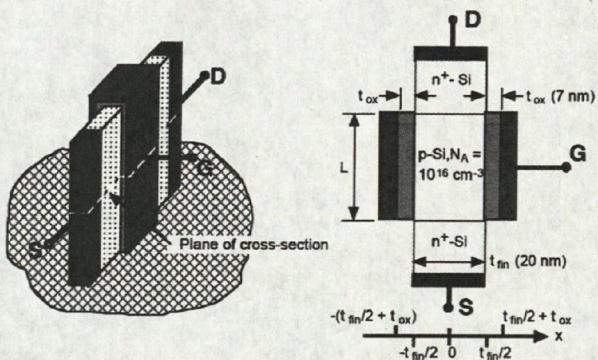
(f) [2 points] How can you ensure that the emitter current is much larger than the control current (i.e. the base current)? Check all that applies.

- Increasing the doping in the emitter
- Increasing the doping in the base
- Reducing the doping in the emitter
- Reducing the doping in the base

End of Problem 4

Problem 5: MOSFET Scaling: FinFET [20 points]

State-of-the-art Si MOSFETs are all based on the finFET device architecture which allows significant gate length scaling beyond what is possible with regular planar MOSFETs (i.e., channel lengths under 20 nm). It is basically a vertical rectangular bar (fin) of silicon sitting on an insulating surface with source and drain regions on either end and with a gate dielectric and metal draped over its middle, as illustrated in the cartoon below left. The cross-section of a finFET you can use for a 6.012 type one-dimensional electrostatic analysis is shown on the right.



Looking at the cross-sectional figure, note several features: there is no body contact, B; the structure is symmetrical left to right; and an inversion channel forms along the upper, left-hand and right-hand oxide-semiconductor interfaces.

- a) [3 pt] Is the finFET illustrated above an NMOS or PMOS? Why?

NMOS PMOS

Because... The channel is p type, while source and drain are n type, requiring an active voltage to turn on.

- b) [3 pts] Consider first a conventional planar MOS capacitor fabricated on a thick p-type silicon wafer with $N_A = 10^{16} \text{ cm}^{-3}$.

- i) In this structure, how wide would the depletion region be at the threshold of strong inversion,

$$V_{GS} = V_T$$

$$X_D = \frac{\epsilon_s}{C_{ox}} \left(\sqrt{1 + \frac{2C_{ox}(V_T - \phi_p)}{\epsilon_s N_A}} - 1 \right) = \text{Assume } t_{ox} = 20\text{nm} 7\text{nm} \quad 3000 \quad 300 \quad ? \quad 300 \cdot 10^{-6} \\ \approx 4.6 \cdot 10^{-3} = \frac{4.6 \cdot 10^{-3}}{10^{-9}} \cdot 10^{-9}$$

$$X_D = \sqrt{\frac{2\epsilon_s - 2\phi_p}{qN_A}} = 3 \cdot 10^{-5} \text{ m} = 30000 \cdot 10^{-9} \text{ nm}$$

$$X_D @ V_{GS} = V_T: \frac{30000}{0.00046} \text{ nm}$$

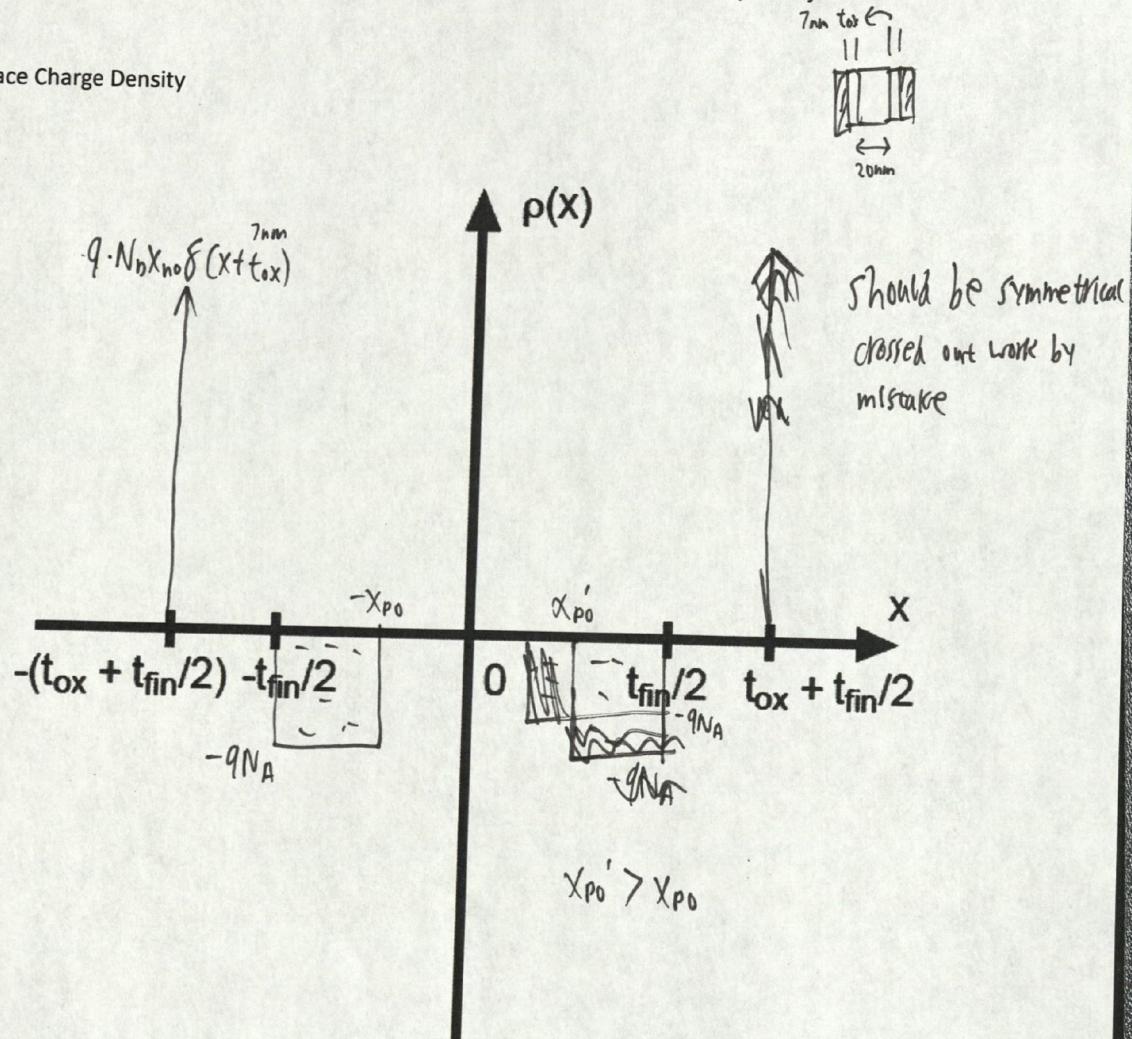
- ii) The width of the fin in a typical finFET, t_{FIN} , is 20nm. How does this compare with your answer in part i), and what does it indicate about the finFET at threshold?

It is significantly smaller, indicating the depletion is < 20 nm in the finFET at threshold.

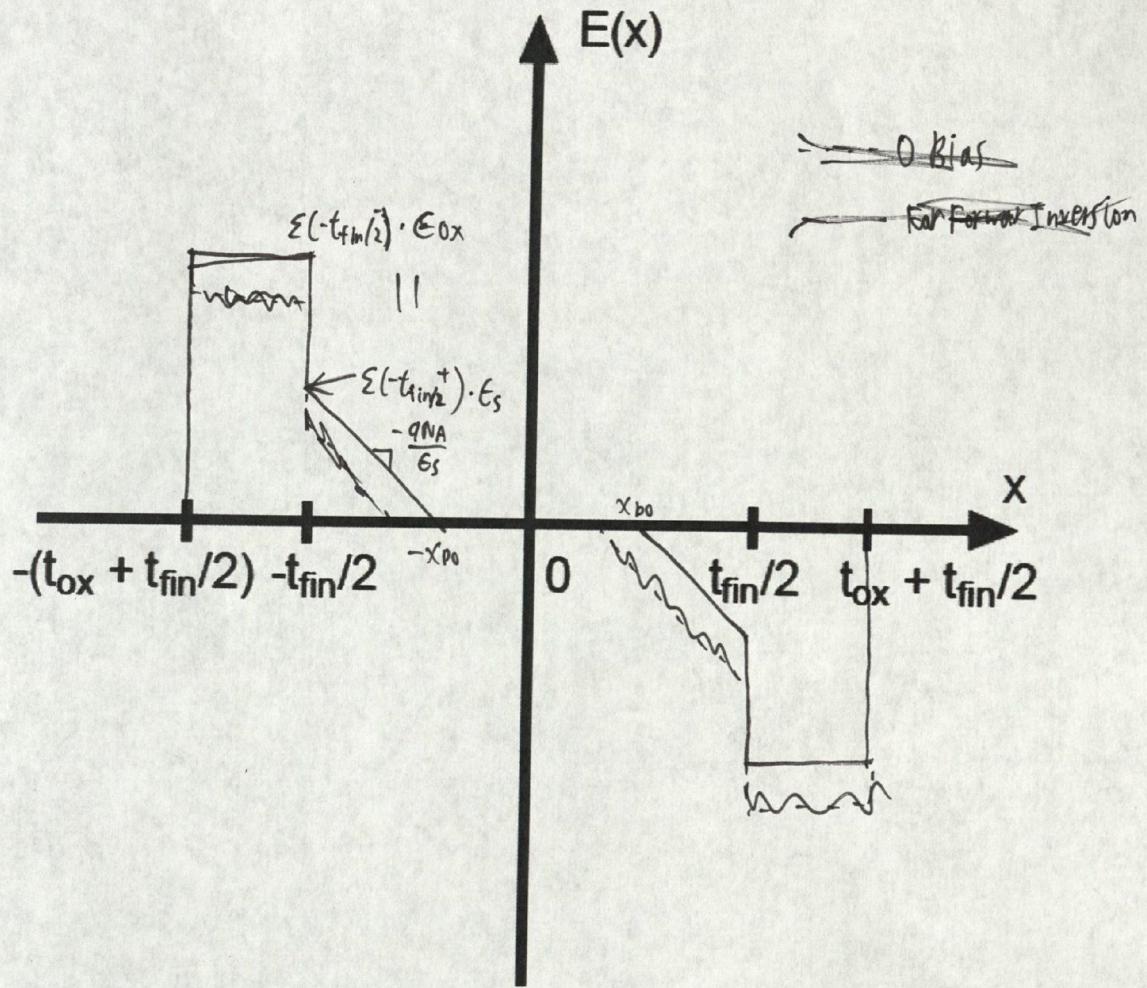
- c) [12 pts] On the axes provided below sketch the net charge density, $\rho(x)$, electric field, $E(x)$, and the electrostatic potential, $\phi(x)$, in this finFET from within the gate metal on the left into the gate metal on the right, when it is biased at threshold, $v_{GS}=V_T$, i.e., just at the onset of strong inversion.

Assume that the oxide thickness, t_{ox} , is 7 nm, the fin thickness, t_{fin} , is 20 nm, the silicon doping level, N_A , is 10^{16} cm^{-3} , and the electrostatic potential of the metal, ϕ_m , is -0.3 V with respect to the potential of intrinsic silicon. Hint: Use symmetry where possible to make your work easier and $x=0$ as your reference.

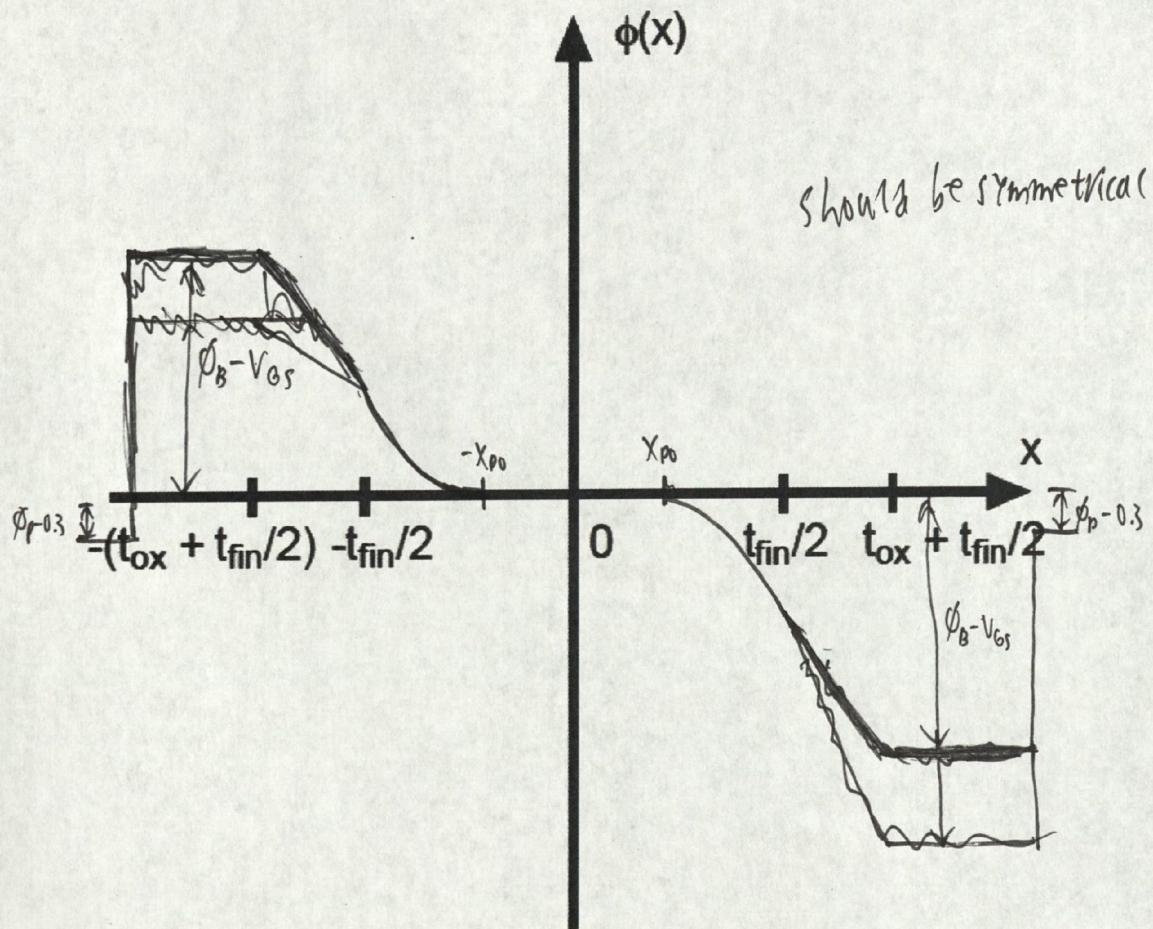
Space Charge Density



Electrostatic Field



Potential



d) [2 pts] What is the flatband voltage, V_{FB} , of this device?

$$\phi_p = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) = 0.026 \ln(10^6) = 0.359 \text{ V}$$

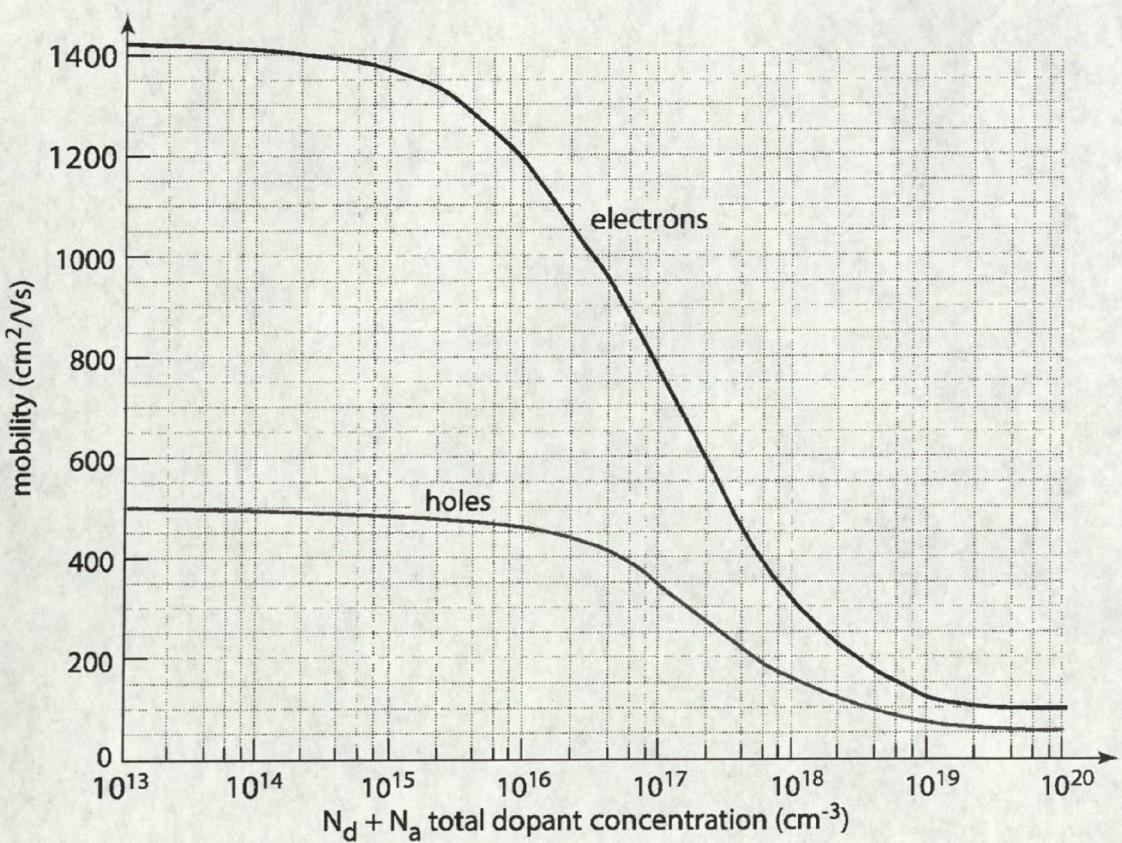
$$V_{FB} = \underline{\hspace{2cm}} \text{ V}$$

e) [2 pts] What is the threshold voltage, V_T , of this device?

$$V_T = \underline{\hspace{2cm}} \text{ V}$$

End of Problem 5 and 6.012 FT21 Final Examinations

APPENDIX



Linear-log plot of electron and hole mobilities at room temperature, as functions of total doping concentration $N_a + N_d$.