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# An Approach to Achieve Zero Turnaround Time in TDD Operation on SDR Front-End

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**ABSTRACT** Thanks to the digitization and softwarization of radio communication, the development cycle of new radio technologies can be significantly accelerated by prototyping on software-defined radio (SDR) platforms. However, a slow turnaround time (TT) of the front-end of an SDR for switching from receiving mode to transmitting mode or vice versa, are jeopardizing the prototyping of wireless protocols, standards, or systems with stringent latency requirements. In this paper, a novel solution called BaseBand processing unit operating in Half Duplex mode and analog Radio Frequency front-end operating in Full Duplex mode, BBHD-RFFD, is presented to reduce the TT on SDR. A prototype is realized on the widely adopted AD9361 radio frequency frontend to prove the validity of the proposed solution. Experiments unveil that for any type of application, the TT in time division duplex (TDD) operation mode can be reduced to zero by the BBHD-RFFD approach, with negligible impact on the communication system in terms of receiver sensitivity. The impact is measured for an in-house IEEE 802.15.4 compliant transceiver. When compared against the conventional TDD approach, only a 7.5-dB degradation is observed with the BBHD-RFFD approach. The measured sensitivity of  $-91$  dBm is still well above the minimum level (i.e.,  $-85$  dBm at 2.4 GHz) defined by the IEEE 802.15.4 standard.

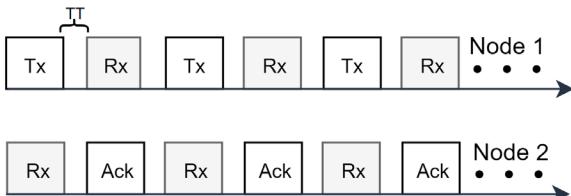
**INDEX TERMS** RF front-end, SDR, TDD, turnaround time.

## I. INTRODUCTION

Software Defined Radio (SDR) is increasingly used in diverse wireless applications, thanks to its flexible and programmable features compared with traditional radio chips. From the day of its invention, it has been successfully adopted for experimental performance evaluation within the wireless research community. An SDR is primarily composed of 2 parts: a programmable digital component and a configurable analog Radio Frequency (RF) front-end. The digital component, which consists of a number of digital Baseband Processing Units (BPUs) implemented on programmable devices, such as Digital Signal Processor (DSP), a Field Programmable Gate Array (FPGA), or a Central Processing Unit (CPU). The reconfigurable analog RF front-end of an SDR is simply everything between the BPUs and the antenna. The general components pertaining to an RF front-end are amplifier, mixer, filters, Digital to Analog Converter (DAC), and Analog to Digital Converter (ADC).

When implementing a wireless standard that uses Time Division Duplex (TDD), the SDR needs to be switched

regularly between Receiving (Rx) and Transmitting (Tx) modes. The switching time or Turnaround Time (TT) is defined as the time required by the PHYsical (PHY) layer to change from Rx mode to Tx mode or vice versa. During TT, the components in the analog RF front-end are powered up and stabilized, which consumes a considerable amount of time. This time consumption becomes more critical for low latency feedback applications, such as process control loops in industrial systems where remote control of robotic arms or other machineries are involved. The influence of TT on latency of a wireless system in a simple Device-to-Device (D2D) topology is illustrated in Fig. 1. It is evident that during TT there is no data transfer, and the wireless channel capacity is wasted. Normally, the negative impact of TT becomes more severe when smaller packets and faster switching scenarios are considered. For example, a special technique proposed in [1] actually leverages the fast and frequent Tx/Rx switching to achieve “virtual Full Duplex”. In this solution, a Tx or Rx slot is in the order of microseconds, and only a few physical layer symbols instead of



**FIGURE 1.** The impact of turnaround time on latency during TDD operation in a D2D scenario.

a complete packet is transferred in a slot. Since the Tx/Rx switching occurs very frequently, it appears as if both nodes are transmitting and receiving concurrently, creating the perception of real Full Duplex (FD) realized with a Half-Duplex (HD) implementation. This solution is however based on the assumption that TT is in the order of nanoseconds, and is only validated in simulation environment. Unfortunately TT of an SDR front-end is generally much higher (i.e.,  $\approx 18 \mu s$  in case of AD9361 [5]). AD9361 introduced by Analog Devices is an RF transceiver chip widely used on SDR RF front-ends, including several devices (e.g., B200 and E310) in the popular USRP family [3], and a range of the FMCOMMS boards [5], [18], [19]. As such, a short TT cannot be taken for granted on the current mainstream SDR platforms. This is one of the main differences between SDR and commercial transceiver chipsets today.

The TT not only plays an important role for a single D2D link scenario, but also for low latency operation in larger scale networks involving many wireless nodes sharing the same spectrum. Several common wireless standards implementing TDD clearly have to cope with hardware limitations related to TT. For instance, the Short InterFrame Space (SIFS) in the Wi-Fi standard, which is the maximum interval a transceiver will wait for receiving the first symbol of the acknowledgement after sending a packet, is limited by the duration of the TT [2]. The SIFS of IEEE 802.11a/g is  $10 \mu s$ , whereas the 60 GHz Wi-Fi standard (IEEE802.11ad) has a shorter SIFS of  $3 \mu s$ . As mentioned earlier, the switching time of an SDR's RF Front-End (SDR RF-FE) is much higher, which makes it infeasible for implementing standards requiring a stringent TT at Medium Access Control (MAC) level.

In summary, (i) squeezing the TT directly reduces the latency of a D2D wireless link, (ii) a sufficiently short TT is a prerequisite to realize wireless standards with stringent timing requirements, and (iii) the TT of today's SDR RF-FE is significantly larger than the majority of commercial wireless chipsets and therefore reduction of the TT on an SDR RF-FE is essential for prototyping existing state-of-the-art and future new wireless standards.

In this paper, a novel approach called BBHD-RFFD – BaseBand processing unit operating in Half Duplex mode and analog Radio Frequency front-end operating in Full Duplex mode – is introduced to reduce the TT on an SDR RF-FE. The remainder of this paper is organized as follows: Related works and motivation are discussed in Section II, implementation of the BBHD-RFFD approach is presented

in Sections III, performance comparison with traditional TDD approach is made in Sections IV and V, and concluding remarks are given in Section VI.

## II. RELATED WORK AND MOTIVATION

Many high-end wireless standards have stringent requirements in terms of latency to ensure the correctness of MAC protocols (some MACs even require precision of response time at the granularity of microseconds. For example, SIFS value of Wi-Fi standards). Commercially available radio chips that are built on DSPs or ASICs easily satisfy these requirements as they are optimized for these specific wireless protocols and specific spectral bands. Most SDRs, on the other hand, are generic and are optimized to operate in a wide range of spectral bands and for a wide range of wireless technologies. Despite the overall decent performance of SDRs, they are generally less optimized in comparison to DSPs or ASICs. For example a typical ASIC for Wi-Fi has a TT of  $1 \mu s$  [7], whereas it is  $18 \mu s$  for AD9361. While  $18 \mu s$  is considerably low, it is not sufficient to support Wi-Fi or self-contained TDD operation in 5G New Radio (NR) [11].

SDRs can be, in general, categorized into two groups: General Purpose Processor (GPP) based SDR, and non-GPP based SDR. The following sections discuss latency performance of the two groups.

### A. GPP BASED SDR

GPP based SDR usually consists of an RF front-end, ADC/DACs, embedded up and down converters on FPGA or DSP boards, and a GPP based host machine. A bridge interface, such as Ethernet or USB, is used to exchange the radio samples between GPP and the radio. In these SDRs, most of the baseband signal operations are offloaded to GPP. USRP N-Series are the examples of such architectures [3]. USRPs are modular so they can deal with the applications operating from DC up to 6GHz. While their performance is suitable for research experiments and quick prototyping, these platforms do not necessarily meet the requirements of time critical communication standards. For instance, the authors of [4] measure the latency of a number of USRPs. The measured round trip latency between RF front-end and host computer for N210 is  $103 \mu s$ . This latency does not include any preprocessing of the data which would have to be included in the latency calculations of a specific protocol implementation. This relatively high latency makes GPP based SDR impractical for time critical standards and applications (e.g., SIFS value of Wi-Fi).

### B. NON-GPP BASED SDR

In a non-GPP based SDR architecture, in general, while PHY layer is implemented on hardware (e.g., FPGA or DSP), the MAC layer is implemented on an embedded processor. The USRP Embedded (E) series (USRP E-Series), USRP X-Series [3], Xilinx FPGA with FMCOMMSx RF front-end board (FMCOMMS SDR) [5], and the WARP v3 [6] are the examples of such architecture. Where, USRP E-Series

incorporate Xilinx SoCs to develop standalone SDR, and WARP v3 contains a Xilinx Virtex-6 FPGA, which includes two MicroBlaze processors. The compact architecture of non-GPP based SDR makes it more suitable for prototyping any low latency wireless standard.

The non-GPP based SDRs can be sub-categorized into two groups: narrowband non-GPP based SDRs, wideband non-GPP based SDRs.

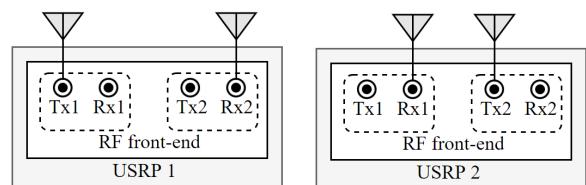
### 1) NARROWBAND NON-GPP BASED SDR

Narrowband non-GPP based SDRs are capable of prototyping low latency wireless protocols, but in limited spectrum. The main hindrance in such kind of SDR is its RF front-end. For example, any time critical communication standards realized on WARP SDR platform would be operating only at 2.4GHz or 5GHz ISM bands. This is because WARP SDR platform employs MAX2829 chipset [7] as RF front-end, which can only operate on the aforementioned ISM bands. The WARP 802.11 reference design [8] is an example of implementation on WARP platform, which meets the SIFS requirements of this standard.

### 2) WIDEBAND NON-GPP BASED SDR

On the other hand, URSP E-Series, URSP X-Series and FMCOMMS SDR platforms, which are examples of wideband non-GPP based SDR, can be operated over relatively wide spectrum, because they utilize commodity wideband RF (WB-RF) front-ends. For instance, USRP E310 and Xilinx FPGA with FMCOMMS2 board incorporate AD9361 as a RF front-end that can be operated up to 6GHz. It is observed that WB-RF front-ends have relatively high TT (e.g.,  $\approx 18\mu s$  in AD9361), which makes them unfeasible for prototyping the time-critical wireless standards (for example: SIFS values of Wi-Fi standards). In a nutshell, a wideband SDR platform with negligible TT (fast switching Tx to Rx or vice versa) is always desired. In literature, a very few real-time SDR based works have been presented.

Authors in [9] use Xilinx Zynq FPGA with AD9361 RF-FE to prototype the IEEE 802.11a standard, but their implementation is not real-time. Wu *et al.* [10] has exploited the AD9371 SDR RF-FE [14], which is the next generation of AD9361 and it has the same TT as that of AD9361, to implement the Wi-Fi standard. They introduce a new SDR architecture based on hardware and software co-design, called tick programmable low latency SDR system in their work. IEEE 802.11ac SISO and MIMO and full-duplex 802.11a/g are implemented. They claim that the SIFS requirement of 802.11ac standard can be achieved with their proposed implementation by giving extensive measurements both at MAC and PHY layers. However, their break-down analysis does not include TT of AD9371 RF-FE. They prototype a real-time system with separate Rx and Tx setups. Since the Rx and Tx setups do not switch their state, TT of RF-FE does not affect the performance of their setup (which is not a case of real-life system). To conclude, they claim that their implementation for IEEE 802.11ac SISO meets



**FIGURE 2.** Antenna connections in 802.11 application framework.

SIFS requirement, without including the TT of RF-FE, which is inevitable for systems operating in our real-life.

Recently, IEEE 802.11 Application Framework [12] introduced by National Instruments (NI) is able to meet SIFS. It, however, uses 2 USRPs with each having two RF transceivers. In this setup, one of the two RF transceivers of an USRP configures in Rx mode only, while other in Tx mode only. As shown in Fig. 2, Rx port of one USRP is connected with the Tx port of other and vice versa. This setup does not need to switch RF transceiver between Tx and Rx mode (i.e., zero TT), but it employs more than one transceivers to achieve this. We however achieve the same results with one transceiver. Throughout this paper we use SDR for wideband non-GPP based SDR.

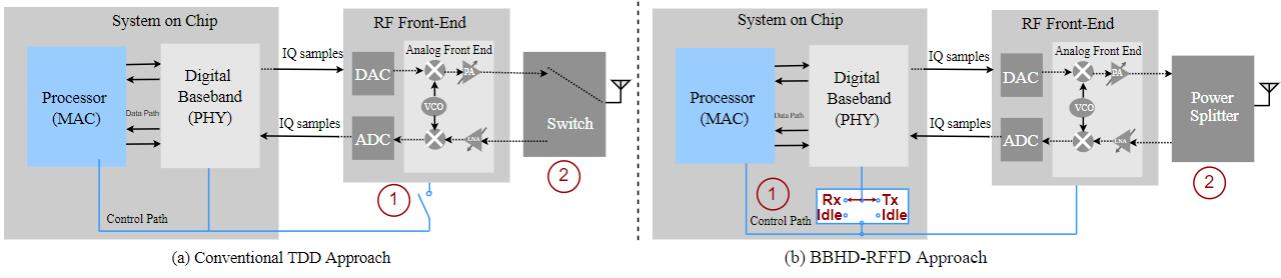
In this paper, we have performed an extensive study on SDR RF-FE and proposed a unique approach that enables researcher to implement any low latency application on a mainstream SDR platform.

### III. THE PROPOSED SOLUTION

To decrease the TT in TDD operation in SDR devices, this paper explores a new paradigm called BBHD-RFFD – baseband processing unit operates at HD, while RF front-end at FD mode. The conventional way to configure the RF front-end for TDD operation (referred to as conventional TDD approach hereafter), is presented in Fig. 3-a for the ease of comparison and discussion, whereas Fig. 3-b illustrates our proposed approach.

Fig. 3-a and Fig. 3-b both have the basic blocks in the radio communication stack, namely the MAC, PHY and RF front-end. For experimental validation we have implemented MAC and PHY on a “System on Chip” hardware architecture. More information on this implementation is provided in the next paragraph. The exact way how MAC and PHY are realized, is not relevant for the BBHD-RFFD approach, the only thing that matters is the control path (blue lines) towards the “RF Front-End”. In a conventional TDD approach, the respective RF front-end components are switched on or off upon transition between Tx and Rx modes, as indicated by ① in Fig. 3-a. Since most of the RF components are analog, they consume more time to be turned on and stabilized than digital components. The turn-on time in combination with their software commands considerably contribute to the overall TT of a wireless system.

In the BBHD-RFFD approach, the RF components of transmitter and receiver remain on all the time, thus no time



**FIGURE 3.** Block diagram of (a) the conventional TDD and (b) the proposed BBHD-RFFD approaches.

is required to turn on the analog components. Apparently, this configuration comes with more power consumption, therefore we also introduce Power Saving Scheme (PSS) in the BBHD-RFFD approach. More information on the PSS can be found in Section V-D. In this case, switching only occurs in digital baseband domain, as indicated by ① in Fig. 3-b. In general, physical layer functionality is comprised of multiple Baseband Processing Units (BPUs). Essentially, the Tx/Rx switching comes down to activating the respective BPUs either in the Tx or the Rx path. The software controlling the switching ensures the HD operation by enabling only one set of BPUs at a time. Since Tx and Rx paths have separate BPUs, the respective path can be attached to the corresponding In-phase and Quadrature phase (IQ) samples of the radio board. For instance, in Tx mode, BPUs related to Tx path are attached to IQ samples of DAC, meanwhile BPUs related to Rx path are detached from IQ samples of ADC. Thanks to microelectronics, the time consumed for digital switching action takes a few nanoseconds. Our digital system is operating at 100MHz, therefore it takes only 10 ns to switch between Tx and Rx modes. The proposed scheme is however not applicable for most single-standard commercial off-the-shelf chips. For instance, the IEEE 802.15.4 compliant chip CC2538 cannot turn on Tx and Rx related RF components at the same time [16], hence it can only support the conventional TDD approach.

The BBHD-RFFD approach is realized on an off-the-shelf SDR hardware platform as follows. The FMCOMMS2 [5] board with AD9361 chipset is exploited as SDR RF-FE, while IEEE 802.15.4 [15] standard compliant PHY and ALOHA MAC layer are implemented in the programmable logic (PL) and processor system (PS) parts of a Zynq-7000 All Programmable System on Chip (AP SoC) (i.e., ZedBoard in our setting) [17]. The FMCOMMS board is usually accompanied by a Xilinx FPGA board to form a complete SDR platform, which is also the case in our setup. The FMCOMMS2 board has separate Tx and Rx antenna ports, a Mini-Circuits' ZN2PD2-63+ power splitter [20] is used to attach both Tx and Rx ports to the antenna, as shown at ② in Fig. 3-b, without using an antenna switch as shown at ② in Fig. 3-a. The function of the power splitter is twofold, (i) it allows us to transmit or receive the RF signal via a single antenna; and (ii) it gives an isolation of more than 20 dB between the

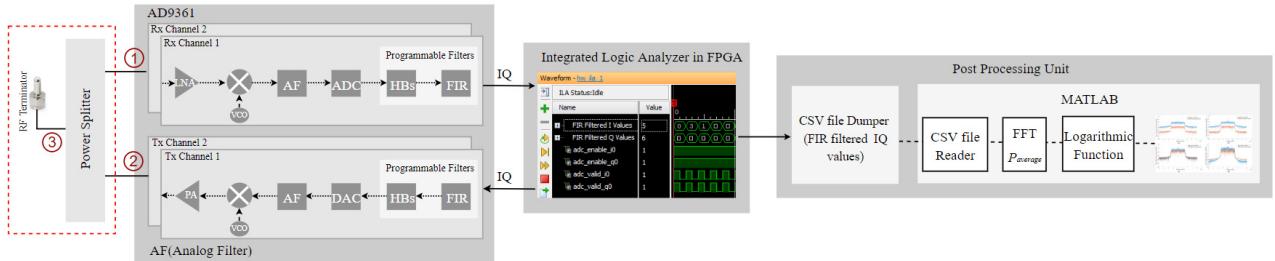
Tx and Rx ports. This isolation is important to our solution, because when leaving the RF components constantly activated, the Rx path is impacted by self-interference even when the Tx BPUs are deactivated. In this paper, the DC leakage and internal noise of various components in both transmit and receive path are collectively defined as self-interference. The power splitter is a low cost and effective approach to mitigate the impact of self-interference, as is further detailed in Section IV.

This paper also investigates how the different operation modes of the AD9361 chipset can be used for the conventional TDD and the BBHD-RFFD approaches. The AD9361 can be operated in the following three duplex modes:

- 1) TDD WithOut Calibration (TDD-WOC): In this mode, RF components are calibrated once during initialization phase, afterwards the components specific to Tx or Rx chains are simply turned on without calibration. Calibration refers to activities such as tuning the Voltage Controlled Oscillator (VCO) and waiting for the Phase Locked Loop (PLL) to stabilize around the desired output frequency
- 2) TDD With Calibration (TDD-WC): In this mode all the RF components are turned on and then calibrated every time when switching between Tx and Rx occurs
- 3) Frequency Division Duplex (FDD): In this mode, all the RF components are turned on and calibrated during initialization in FDD mode, and all the RF components pertaining to Rx and Tx chains remain operational afterwards. Since both Tx and Rx paths remains on all the time, there is no need of switching (Tx to Rx or vice versa) in FDD mode.

In this paper, both TDD-WC or TDD-WOC can be exploited to implement the conventional TDD approach. It is recommended to repeat calibration in AD9361 each time the operating channel frequency is changed. Thus, TDD-WC should be employed in a situation where regular change of Tx/Rx frequency occurs (e.g., Bluetooth). The FDD mode of AD9361 is exploited to implement the BBHD-RFFD approach.

In addition to the three duplex modes, the ‘DC offset calibration and tracking feature’ of AD9361 helps to minimize the DC offset in the received IQ samples, while the ‘quadrature calibration and tracking’ feature aims to maintain



**FIGURE 4.** Experimental setup to capture IQ samples from AD9361 and post processing.

orthogonal relation between the received I and Q samples by performing IQ correction [13]. The aforementioned calibration and tracking features of AD9361 are hereinafter referred to as DC/IQ tracking, which is further explored in experiments to suppress the DC component in the self-interference.

#### IV. EXPERIMENTS

In this section, we first measure the amount of self-interference under different settings, and derive the optimal setting to implement the BBHD-RFFD approach, and then experiments are conducted to benchmark our proposed approach against the conventional TDD approach, in terms of performance in TT and receiver sensitivity.

##### A. ANALYSIS OF SELF-INTERFERENCE

###### 1) MEASUREMENT SETUP

Fig. 4 shows the setup utilized to measure the self-interference under different conditions and configuration of AD9361, an RF front-end in the FMCOMMS2 board used in our experimental setting. All measurements in this section use 2.41 GHz as center frequency. AD9361 has two identical and independently controlled transmit and receive paths, which are both shown in Fig. 4, though only one set of Tx/Rx channel is used in the measurement. The measurement is performed in the following 3 steps:

- 1) unintended RF signals (i.e., self-interference) pass through Rx chain of AD9361. In this chain, the I and Q samples obtained at the output of ADC, operating at 8 Msps, are filtered by a low pass Finite Impulse Response (FIR) filter with cutoff frequency of 2.6 MHz,<sup>1</sup>
- 2) Integrated Logic Analyzer (ILA), a logic analyzer core that can be used to monitor the internal signals of a design, in FPGA (the PL part of Zynq 7000 SoC) is used to capture the filtered IQ samples,
- 3) post processing of the collected IQ samples is done in MATLAB (a high-performance computer software for technical computing), to obtain the Power Spectrum Density (PSD) and the average power of the

<sup>1</sup>We choose 2.6 MHz as the cut off frequency because we later on use IEEE 802.15.4 compliant PHY to measure the receiver sensitivity, 2.6 MHz is adequate to offer the signal bandwidth defined in the standard.

IQ samples, using (1) and (2) respectively.

$$PSD = 10 \times \log_{10} (|Y_k|^2) \quad \text{where}$$

$$Y_k = \sum_{n=0}^{N-1} ((I_{fir} + iQ_{fir})_n \cdot e^{-\frac{2\pi i}{N} kn}), \quad 0 \leq k \leq N - 1 \quad (1)$$

$$P_{avg} = 10 \times \log_{10} \left( \frac{1}{N} \sum_{n=0}^{N-1} (I_{fir}[n]^2 + Q_{fir}[n]^2) \right) \quad (2)$$

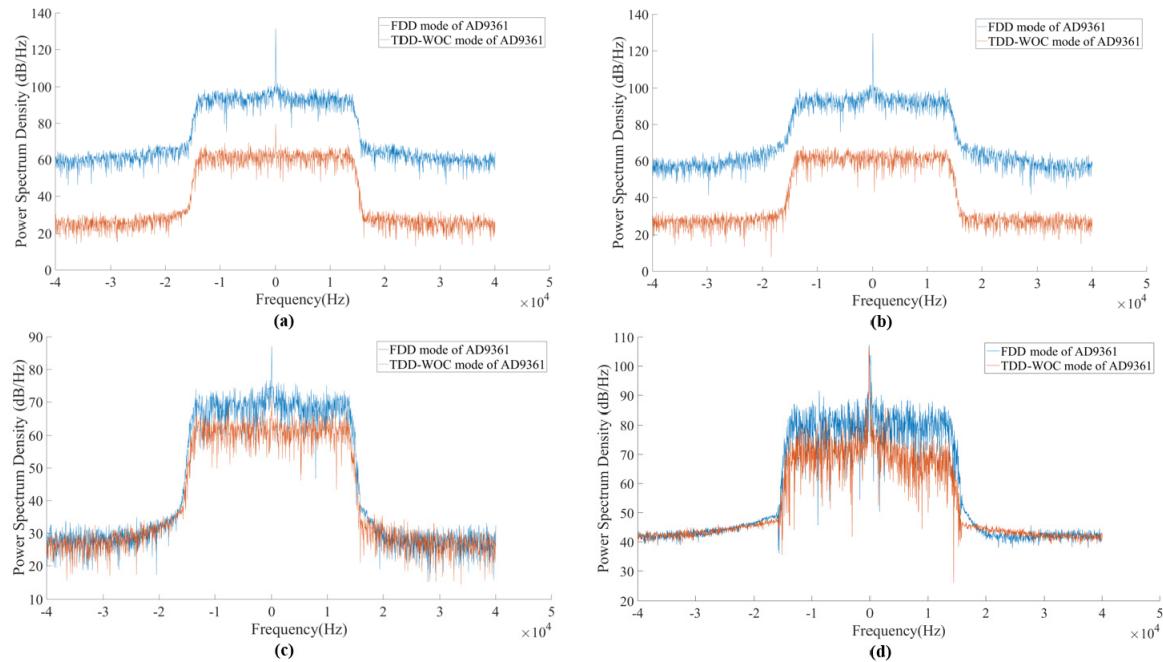
where  $I_{fir}$  or  $Q_{fir}$  denote the filtered IQ samples at the output of AD9361 FIR filter, and  $N$  denotes the total number of collected IQ samples. The  $PSD$  is obtained by squaring the outputs (i.e.,  $Y_k$ ) of the Fourier Transform. The  $P_{avg}$ 's unit is dB, because it has not been calibrated. However this suffices our purpose to compare the strength of self-interference under various conditions.

The self-interference when no transmission takes place has been analysed with PSD measurements for the TDD-WOC and FDD modes of AD9361 for the following 4 cases:

- 1) **case 1** (see Fig. 5-a): DC/IQ tracking is disabled, Tx and Rx ports (① and ② in Fig. 4) are directly connected without any power splitter
- 2) **case 2** (see Fig. 5-b): DC/IQ tracking is enabled, Tx and Rx ports are directly connected without any power splitter
- 3) **case 3** (see Fig. 5-c): DC tracking is enabled, Tx and Rx ports are connected via power splitter, the 3rd port of power splitter is terminated, to prevent external interference, as shown in the dashed red rectangular of Fig. 4
- 4) **case 4** (see Fig. 5-d): DC tracking is enabled, Tx and Rx ports (① and ② in Fig. 4) are attached to two antennas, positioned orthogonal to each other. Extra measures have been taken to ensure that the operational band is clean at the time of the experiment.

As there is no self-interference in the TDD-WOC mode, the average power difference between FDD and TDD-WOC modes represents the intensity of the self-interference. This is calculated according to (3)

$$P_{diff} = P_{fdd} - P_{tdd-woc} \quad (3)$$



**FIGURE 5.** The comparison of self-interference (visualized by PSD), between FDD and TDD-WOC modes of AD9361, under the following settings: (a) Tx and Rx ports are directly connected and DC tracking is disabled; (b) Tx and Rx ports are directly connected and DC tracking is enabled; (c) Tx and Rx ports are connected through a power splitter with DC tracking enabled; (d) Tx and Rx ports are connected to two antennas, placed orthogonal to each other.

**TABLE 1.** Self-interference measured by power difference in the 4 cases.

Case	$P_{fdd}$ (dB)	$P_{tdd-woc}$ (dB)	$P_{diff}$ (dB)
Case 1	65.75	26.84	38.9
Case 2	64.43	26.85	37.6
Case 3	34.65	26.45	8.2
Case 4	47.23	44.03	3.2

where  $P_{fdd}$  and  $P_{tdd-woc}$ , denote  $P_{avg}$  obtained during FDD and TDD-WOC modes, respectively. The  $P_{diff}$  for all the aforementioned four cases are listed in Table 1.

## B. MEASUREMENT ANALYSIS

Among the 4 cases, **case 1** is used as a benchmark, as it does not involve any effort to remove self-interference. When comparing **case 2** with **case 1**, the self-interference of FDD mode is reduced by 1.3dB, thanks to the DC tracking feature of AD9361. When comparing **case 3** with **case 1**, the self-interference of FDD mode is suppressed by 30.7dB. The high-quality isolation (i.e., observed 29.4dB at 2.41GHz) between two ports of the power splitter, together with the DC tracking feature in **case 3** helps to mitigate the effect of self-interference of FDD mode. Although the power splitter has strongly reduced the self-interference, it also causes the Tx power degradation by a factor of 3.6dB, due to the insertion loss of the splitter. The observed self-interference reduction in **case 4** is further improved by 5 dB compared to **case 3**, indicating that this setup offers the better results in terms

of performance. **Case 4** has the advantage of less Tx power loss, however it requires accurate antenna placement (orthogonal) to achieve optimal performance, whereas **case 3** is easier to implement and likely to offer more repeatable measurements.

In conclusion, the setup in **case 3** – TDD-WOC and FDD modes of AD9361 along with power splitter and DC tracking enabled feature – has been selected to implement the conventional TDD approach and BBHD-RFFD approach, respectively.

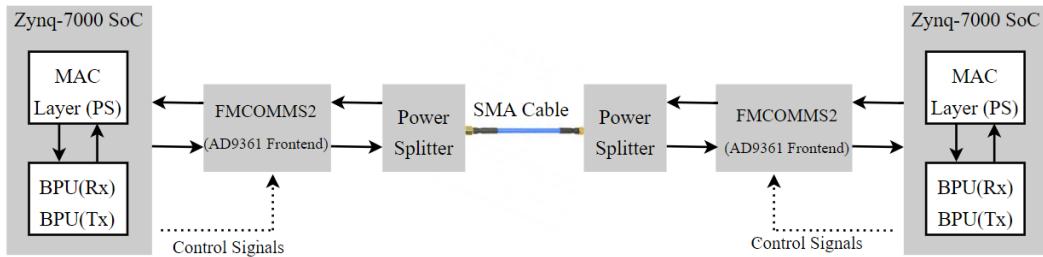
## V. ANALYSIS OF TURNAROUND TIME AND RECEIVER SENSITIVITY

### A. GENERAL MEASUREMENT SETUP

The experiment setup used for TT and receiver sensitivity measurements is illustrated in Fig. 6, consisting of two identical SDR nodes. In terms of hardware, each SDR node is composed of a Zynq-7000 SoC (i.e., ZedBoard in our setting), an FMCOMMS2 board which incorporates AD9361 front-end, and a power splitter. A SubMiniature version A (SMA) cable is used to connect the two SDR nodes, ensuring interference-free condition for the sensitivity measurement. Each SDR node is configured to act as an IEEE 802.15.4 compliant transceiver.

### B. TT MEASUREMENT AND ANALYSIS

The TT measurement is relatively simple; it requires only one SDR node, TT is determined by accessing relevant registers of AD9361. More specifically, the following steps are used to measure the TT:



**FIGURE 6.** Experimental setting for turnaround time and receiver sensitivity measurements.

- 1) A MAC application running on PS (as shown in Fig. 6) issues commands to AD9361 to trigger Tx/Rx switching,
- 2) in parallel a global timer on PS is enabled and started,
- 3) the MAC application continuously read the status register of AD9361 (i.e., polling),
- 4) upon obtaining the desired status (i.e., polling ended, and related registers of Rx or Tx have changed their status), the global timer is stopped and TT is calculated by reading the current value of the global timer.

Fig. 7 summarizes the aforementioned procedure used for TT measurements with pseudo code. `GetTime()` is used to get the current values of the running global timer, while ENSM controls the switching state of AD9361. `CalFunc()` provides the calculated TT consumed during Tx to Rx switching or vice versa. The ENSM command switches the AD9361 to the desired state specified in its input parameter. There are two possible states of ENSM in our implementation: with RX as input parameter, the AD9361 is switched into Rx mode, while the input parameter TX forces the AD9361 into Tx mode.

Table 2 shows the TT consumed by all three modes of AD9361 whenever switching takes place. It can be observed that Rx to Tx switching always takes more time because the turn-on time of DAC is higher than that of ADC in AD9361. The worst TT values are observed in TDD-WC mode whereas nearly zero (i.e.,  $\approx 10$  ns) TT is observed in FDD mode (i.e., BBHD-RFFD approach). The maximum TT specified by the IEEE 802.15.4 standard is  $192\ \mu s$  [15], therefore this standard can be implemented with any of the three modes of AD9361. The short inter-frame space (SIFS) values for IEEE 802.11 standard are  $10\ \mu s$  (2.4GHz) [2] and  $3\ \mu s$  (60GHz) [21]. Both TDD-WC and TDD WOC of AD9361 would fail to meet SIFS (TT is one of the many parts of SIFS) requirements of Wi-Fi, but our proposed approach makes this feasible. In fact, any standard with stringent TT can be realized with our approach.

### C. RECEIVER SENSITIVITY MEASUREMENT AND ANALYSIS

As mentioned before, since RF parts of both transmitter and receiver are constantly activated in our approach, the receiving path is suffering from self-interference. In section IV the self-interference has been analyzed to be  $8.2\ dB$  and

--Rx To Tx Switching	--Tx To Rx Switching
1: <code>GetTime(t0)</code>	1: <code>GetTime(t0)</code>
2: <code>ENSM(TX)</code>	2: <code>ENSM(RX)</code>
3: <code>GetTime(t1)</code>	3: <code>GetTime(t1)</code>
4: <code>CalFunc(t1-t0)</code>	4: <code>CalFunc(t1-t0)</code>

**FIGURE 7.** Pseudo codes for the TT measurements.

**TABLE 2.** The average TT measured under three duplex operation modes of AD9361 with a standard deviation of around  $1\ \mu s$ .

TT ( $\mu s$ )	TDD-WC	TDD-DOC (conventional TDD)	FDD (BBHD-RFFD)
Tx to Rx	40.2	4.2	$\approx 0$
Rx to Tx	53.0	17.2	$\approx 0$

this causes the noise to increase by the same amount. It is therefore expected that the receiver sensitivity of the system will be equally affected. We are using IEEE 802.15.4 compliant BPUs, therefore the sensitivity is measured according to this standard requirements [15]. The sensitivity of a receiver is defined as the input power level when the Packet Error Rate (PER) drops to 1%. PER is measured by counting the proportion of packets lost during transmission against 10,000 transmitted packets, each containing 20 octets with 14 bytes PHY payload. In order to determine the receiver sensitivity, the PER measurement is repeated when packets are sent with different Tx powers, which is controlled by tuning the variable attenuator (i.e., PA block in Fig. 3-b) in the AD9361 Tx chain.

For determining receiver sensitivity, however, PER needs to be mapped to the input power of the receiver rather than Tx attenuation. The translation from the Tx attenuation (dB) to absolute Rx power (dBm) is achieved using the following steps: (1) the SMA cable along with power splitter is detached from the receiver AD9361 RF front-end and attached to an Anritsu MS2690 A spectrum analyzer [22], in another word, the spectrum analyzer replaces the receiver SDR in the setup depicted in Fig. 6, (2) the Rx power is measured via spectrum analyzer when different settings of the attenuator are applied to AD9361. Fig. 8 shows that the relation between the Tx attenuation and the measured Rx power by the spectrum analyzer is approximately linear. By making use of this

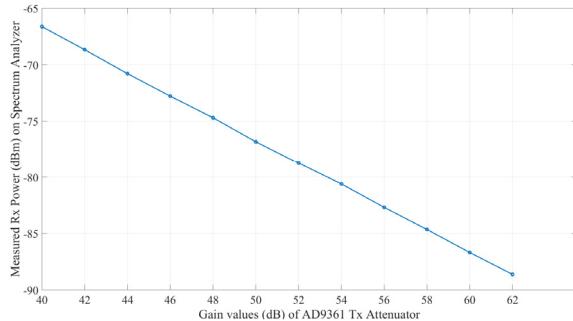


FIGURE 8. Measured Rx power (in dBm) vs AD9361 Tx attenuator.

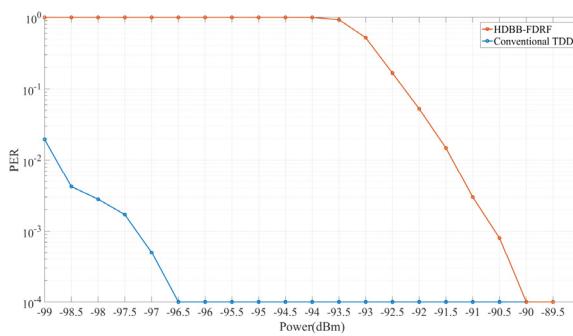


FIGURE 9. Receiver Sensitivity measurements.

linear relation, Tx attenuation can be easily translated into absolute power level, which is then used to acquire the receiver sensitivity.

The PER obtained under a range of Rx input power are illustrated in Fig. 9. It can be observed from Fig. 9 that the receiver sensitivity of BBHD-RFFD and the conventional TDD are  $-91\text{dBm}$  and  $-98.5\text{dBm}$ , respectively. The measured receiver sensitivity of the conventional TDD approach is comparable with that of commercial chipsets. For instance, cc2538 chipset has the receiver sensitivity of  $-97\text{dBm}$  [16]). It can be concluded from the measurements that the receiver sensitivity of our approach is degraded by  $7.5\text{dB}$ , compared to the conventional TDD. This degradation is obviously caused by the  $8.2\text{dB}$  self-interference, however it is not exactly aligned (i.e.,  $0.7\text{dB}$  difference). This is because DC leakage is a part of the self-interference, which does not affect the receiver sensitivity. In conclusion, despite the degradation, the receiver sensitivity in BBHD-RFFD approach is still well above the minimum requirement by the standard (i.e.,  $-85\text{dBm}$  at  $2.4\text{GHz}$ ). We thus expect no severe impact on other systems.

#### D. POWER REDUCTION SCHEME

To reduce power consumption, a Finite State Machine (FSM) is introduced in BBHD-RFFD approach. It alleviates the power consumption by ensuring a smart switching of the SDR node among different modes. The proposed FSM illustrated in Fig. 10 has 4 states:

- 1) State 0: after initialization, the SDR node enters into sleep mode, where Tx and Rx related BPUs and

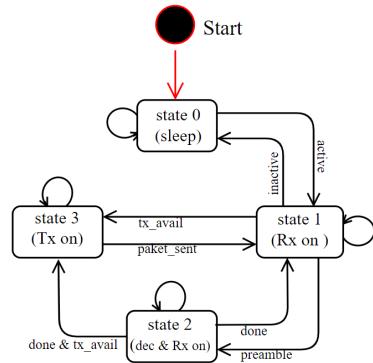


FIGURE 10. State machine diagram of operating modes used in BBHD-RFFD approach.

analog RF front-end remain off, indicating no power consumption.

- 2) State 1: upon receiving active signal from the upper layer, the SDR node switches to Rx mode. The Rx mode enables the SDR node to receive a packet by turning on Rx path (i.e., both BPUs and analog parts). Our implementation has completely separated Tx and Rx paths, and these paths can be controlled without affecting each other. Hence, Tx path (Both analog and BPUs parts) is turned off in this mode. However, during state 1, the upper layer can issue “tx\_avail” signal in case there is a packet to be transmitted. SDR node responds to this command by switching its Rx mode to Tx (state 3 in Fig. 10).
- 3) State 2: the SDR node in Rx mode continuously scans the channel and it starts decoding if there is a valid packet in the air. Upon preamble detection, SDR node changes its state from Rx to decoding state. In decoding state, the SDR node performs two actions in parallel, 1) it continues to decode the packet; 2) it starts to activate the Tx path. When decoding process is completed (indicated by “done” in Fig. 10), SDR node enters into state 3 if “tx\_avail” request is asserted by upper layer, otherwise it returns to state 1.
- 4) State 3: in Tx mode the SDR node is able to transmit a packet if there is a transmit packet request from the upper layer. The FSM can enter into state 3 either via state 1 or 2. In both cases zero TT from Rx to Tx is ensured. During state 1 to state 3 transition, this can be realized by the upper layer, which can send “tx\_avail” command in advance (e.g., it can send this command during packet preparation). Similarly during state 2 to 3 transition, it is achieved by activating Tx path during decoding process of state 2. Furthermore, In Tx mode, SDR node starts to activate its Rx mode at some moment during transmission and this moment is decided by transmitting packet length. The SDR node turn off its Tx mode immediately after completing the transmission. This smart scheduling makes Tx to Rx switching time (or TT) zero, because Rx switching is initiated during transmission.

Conclusively, the smart switching in the proposed FSM makes BBHD-RFFD approach feasible for real-time system where energy consumption is one of the utmost requirements.

## VI. CONCLUSIONS

SDR, consisting of programmable digital baseband processing unit and configurable RF front-end, has been widely adopted due to its flexibility and re-programmability. However, the slow Turnaround Time (TT) of an SDR RF front-end hinders the SDR from prototyping a wireless communication system in which strict latency requirement is desired. In this paper, different operational modes of AD9361, a widely used SDR RF front-end in SDR community, are thoroughly investigated. To reduce TT on an SDR RF front-end, an innovative approach BBHD-RFFD is proposed and implemented using AD9361. Furthermore, the approach is made energy-efficient by introducing a smart switching scheme. Our approach enables researchers and wireless developers to prototype today's and future time critical communication standards on SDR platform over wide range of radio spectrum. The main challenge of using the proposed approach is to minimize the impact of self-interference. This can be done by using a power splitter with high quality isolation, or by simply placing antennas attached to Tx/Rx ports orthogonal to each other. Experimental results show that the impact of self-interference on receiver sensitivity can be limited to 7.5 dB, when suggested instructions are taken into account. The proposed approach is straightforward to use, and is generally applicable to any wireless standard, hence making SDR a powerful tool for rapid prototyping of real-life communication protocols.

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