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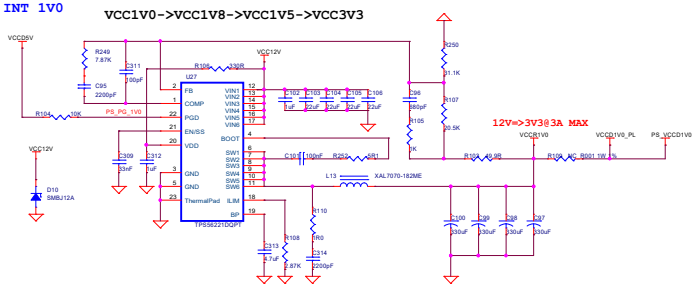
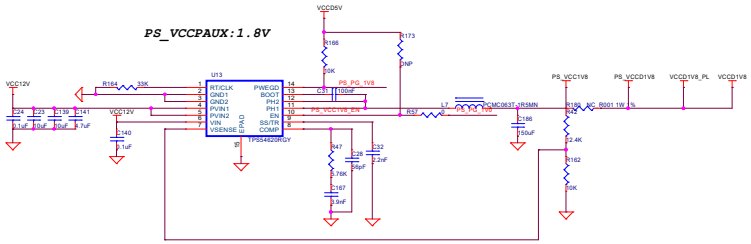
01 FPGA POWER SECTION

FPGA INT 1V0

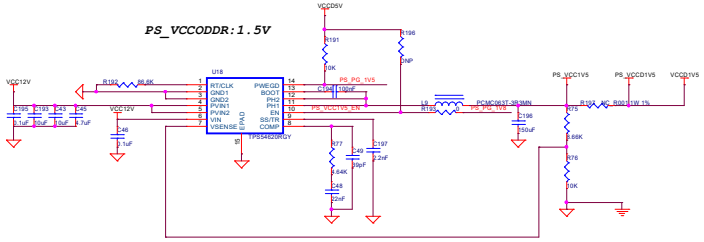
VCC1V0->VCC1V8->VCC1V5->VCC3V3



PS_VCCPAUX:1.8V

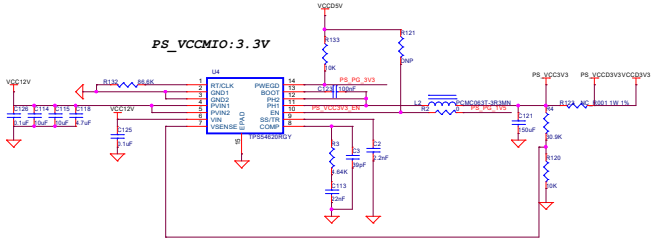


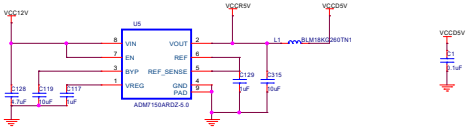
PS_VCCODDR:1.5V



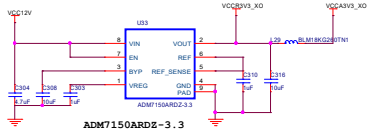
Vout = 0.765*(1+R1/R2),R2=22.1K

PS_VCCMIO:3.3V





ADM7150ARDZ-5.0



ADM7150ARDZ-3.3

KINTEX 7 WORK CONDITIONS		
1	VCCINT	1.0V
2	VCCAUX	1.8V
3	VCCO	1.35V~3.3V
4	VCCBAT	1.0V~1.8V,if not used to GND or VCCAUX
5	VCCAUX_IO	1.8V(DEFAULT) 2.0V(PEFORMANCE)
6	MGTAVCC	1.0V
7	MGTAVTT	1.2V
8	MGTAVTTRCAL	1.2V
9	MGTVCCAUX	1.8V
10	VCCBRAM	1.0V
11	VCCADC	1.8V
12	VCCREFP	1.25V

File	01_FPGA_POWER		
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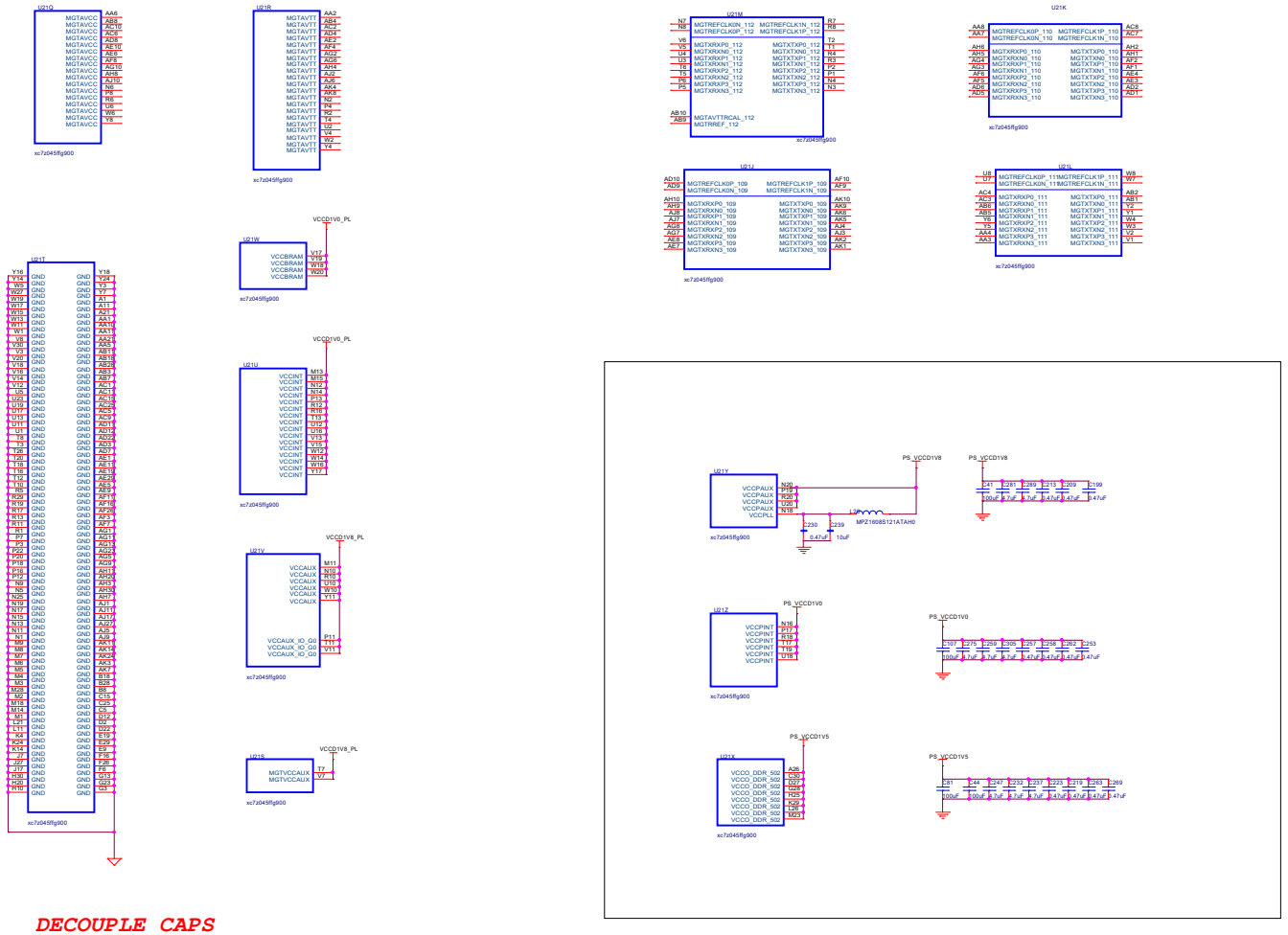
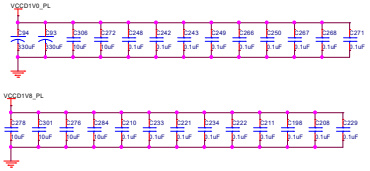


CFGBVS:
0-1.8V or 1.5 V (include bank14 && bank 15).
1-2.5V or 3.3V (include bank 14 && bank 15)

ZYNQ7000(030,045) WORK CONDITIONS

PS	1	VCCPINT	1.0V
	2	VCCPAUX	1.8V
	3	VCCPLL	1.8V
	4	VCCODDR	1.14~1.89
	5	VCCMIO	1.71~3.465
	6	VPIN	VCCODDR+0.2V VCCMIO+0.2V
PL	7	VCCINT	1.0V
	8	VCCBRAM	1.0V
	9	VCCAUX	1.8V
	10	VCCO	1.1~1.89(HP) 1.1~3.45(HR)
	11	VCCAUX_IO	1.8(NORMAL) 2.0(PERFORMANCE)
	12	VCCBAT	0~1.8V(NOT USED TO GND)
	13	MGTAVCC	1.0V
	14	MGTAVTT	1.2V
	15	MGTAVTTRCAL	1.2V
	16	MGTVCCAUX	1.8V
	17	VCCADC	1.8V
	18	VCCREFP	1.25V

DECOUPLE CAPS



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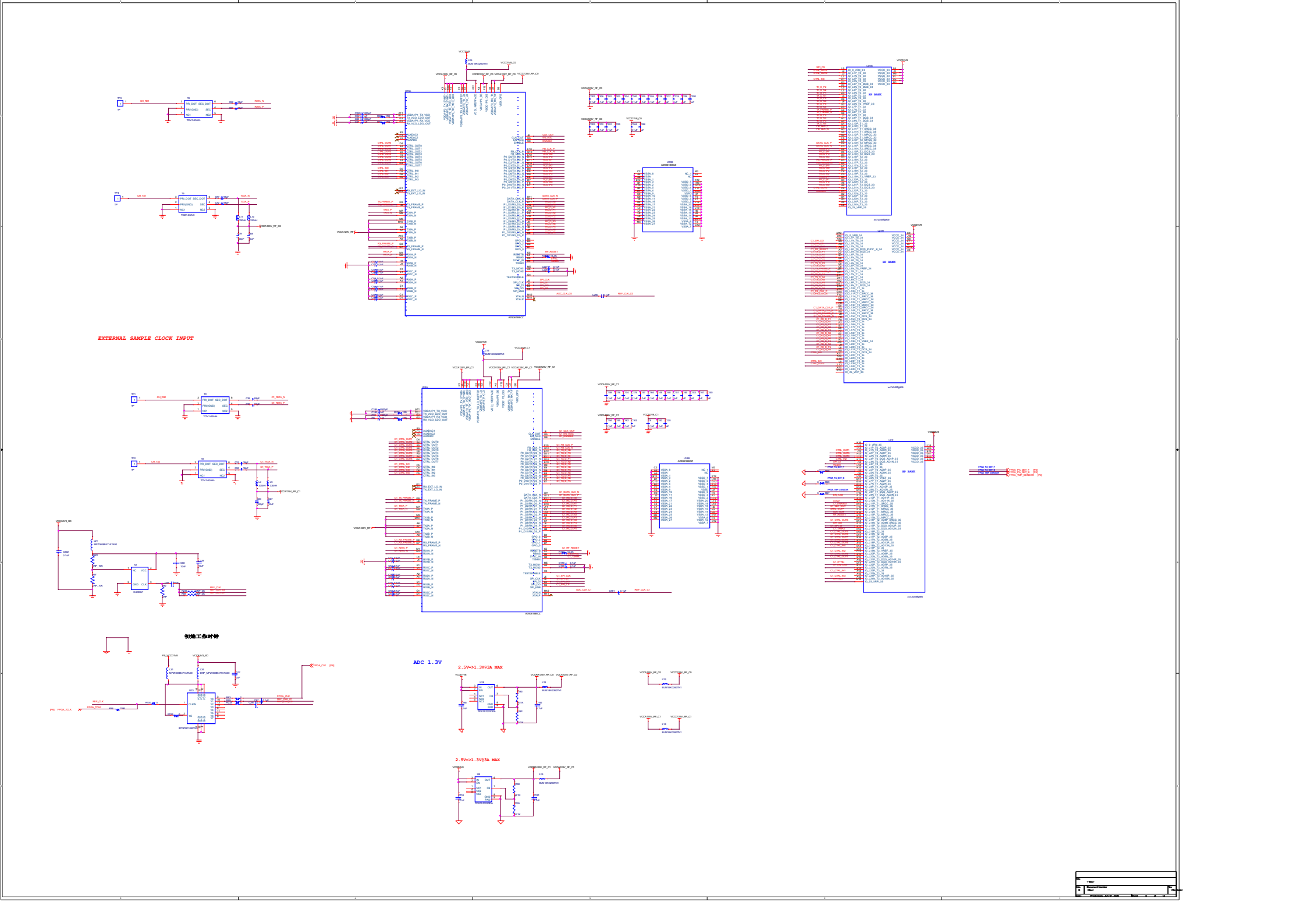
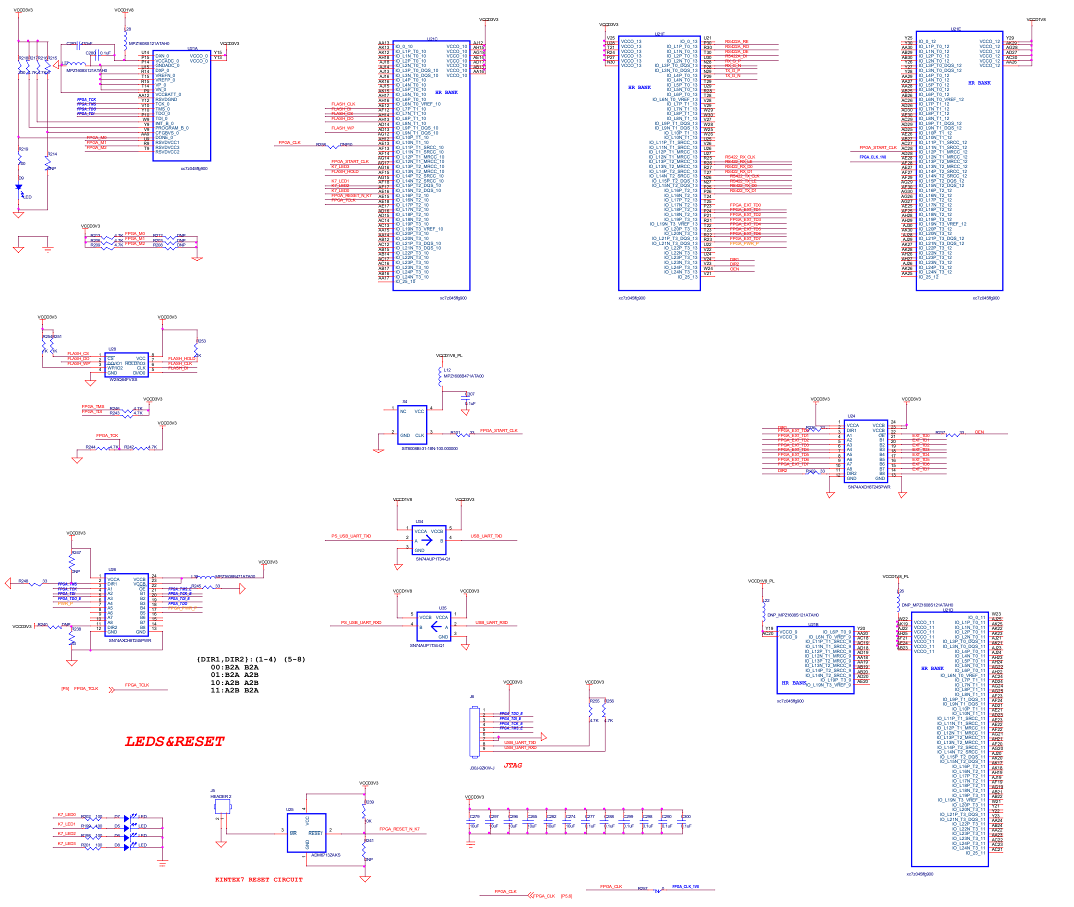
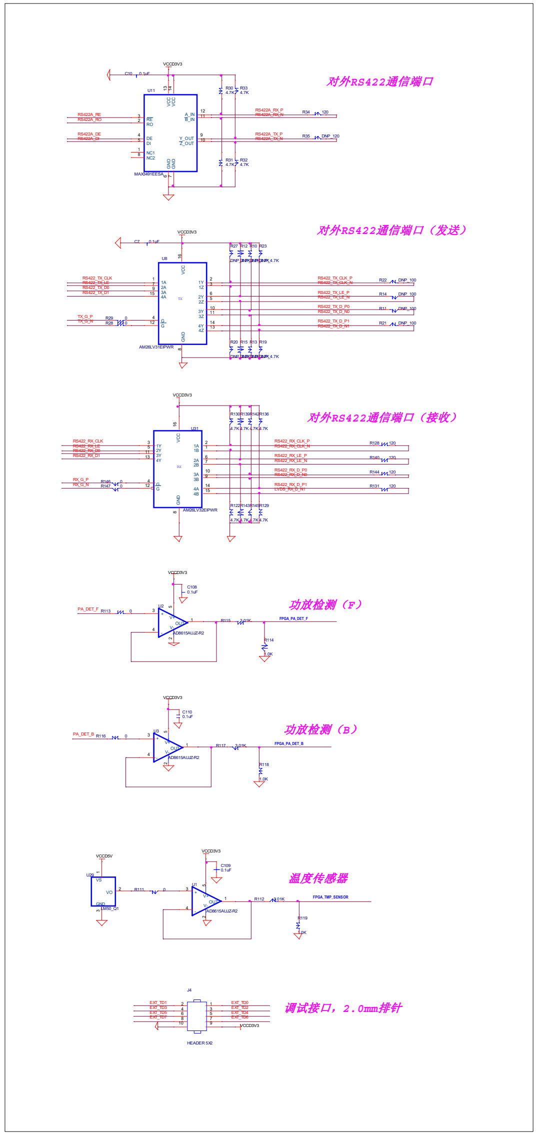
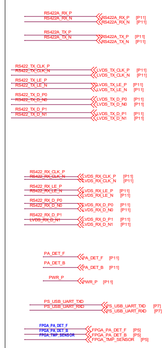

EXTERNAL SAMPLE CLOCK INPUT
初始工作时钟
ADC 1.3V
2.5V=>1.3V@3A MAX
2.5V=>1.3V@3A MAX

CFGBVS:
0-1.8V or 1.5 V (include bank14 && bank 15).
1-2.5V or 3.3V (include bank 14 && bank 15)

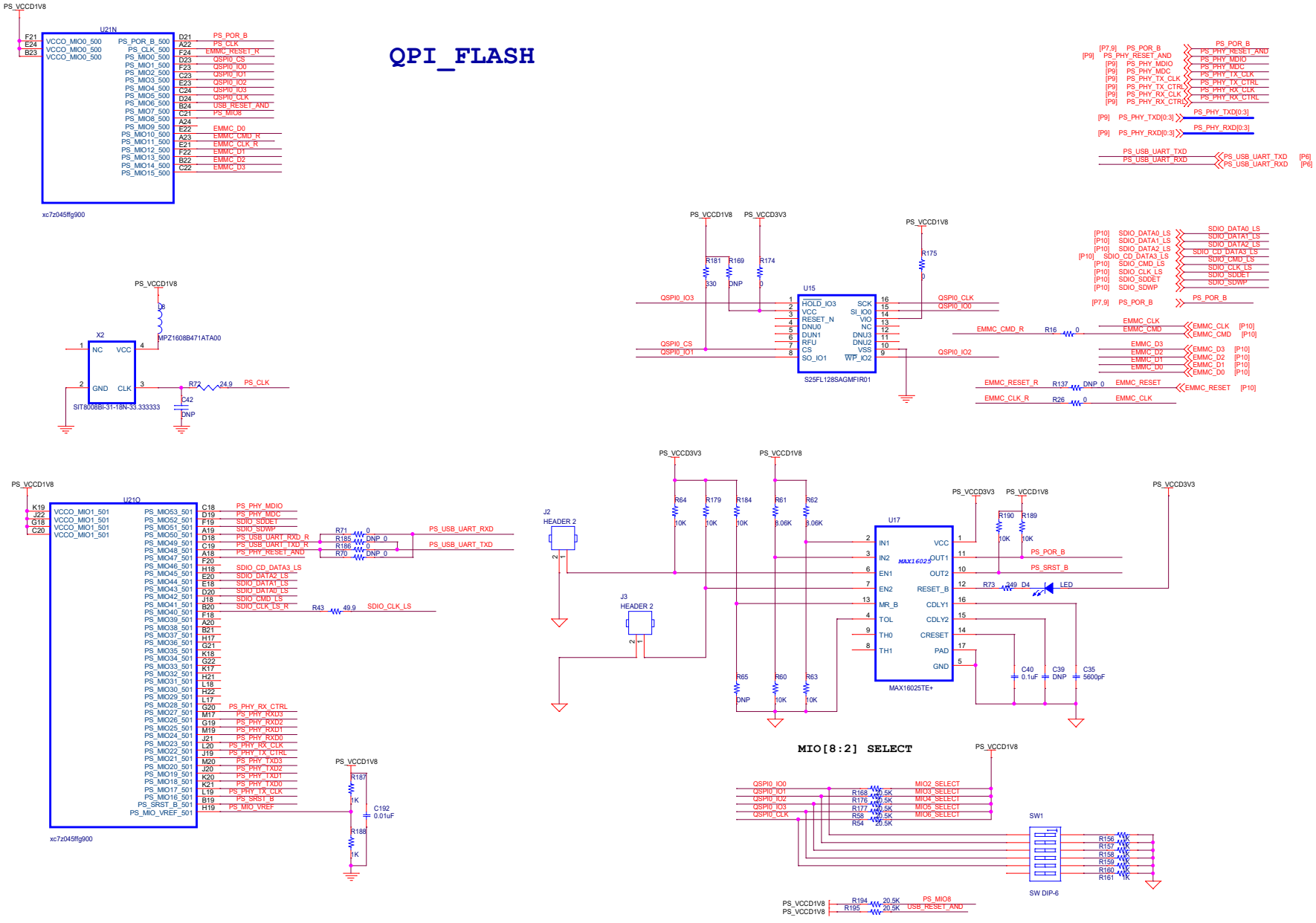






KINTEX 7 WORK CONDITIONS		
1	VCCINT	1.0V
2	VCCAUX	1.8V
3	VCCO	1.35V~3.3V
4	VCCBAT	1.0V~1.8V,if not used to GND or VCCAUX
5	VCCAUX_IO	1.8V(DEFAULT) 2.0V(PEFORMANCE)
6	MGTAVCC	1.0V
7	MGTAVTT	1.2V
8	MGTAVTTRCAL	1.2V
9	MGTVCCAUX	1.8V
10	VCCBRAM	1.0V
11	VCCADC	1.8V
12	VCCREFP	1.25V

QPI_FLASH



20.5K 电阻必须摆放在SPI走线中间

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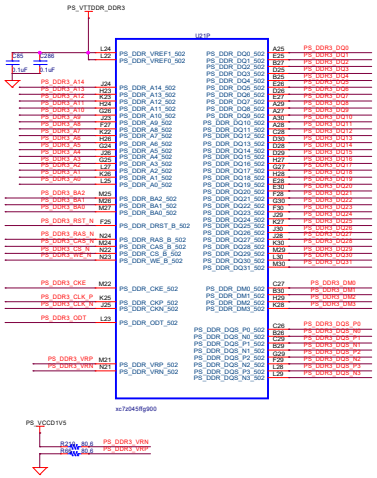
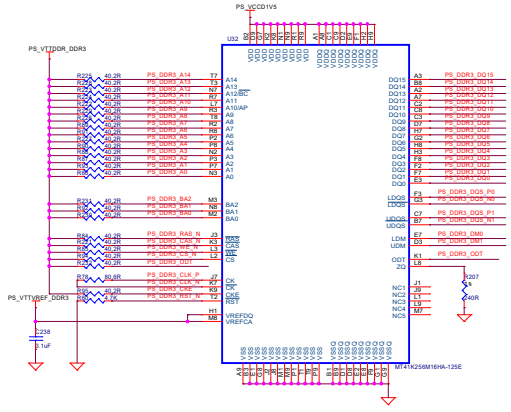
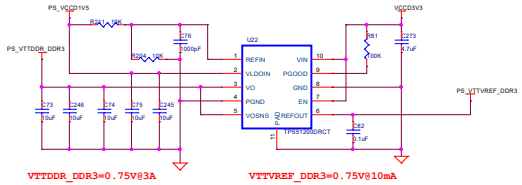
05 FPGA DDR3 SDRAM INTERFACE SECTION



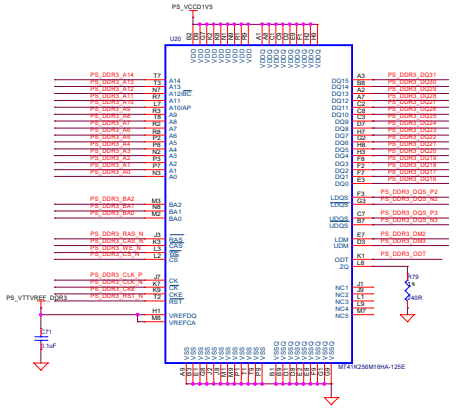


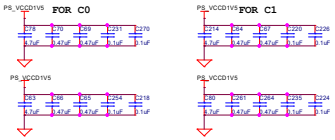
DDR3 POWER CONFIG



VTTDDR_DDR3=0.75V@3A

VTTVREF_DDR3=0.75V@10mA





Place near DDR3 pin.

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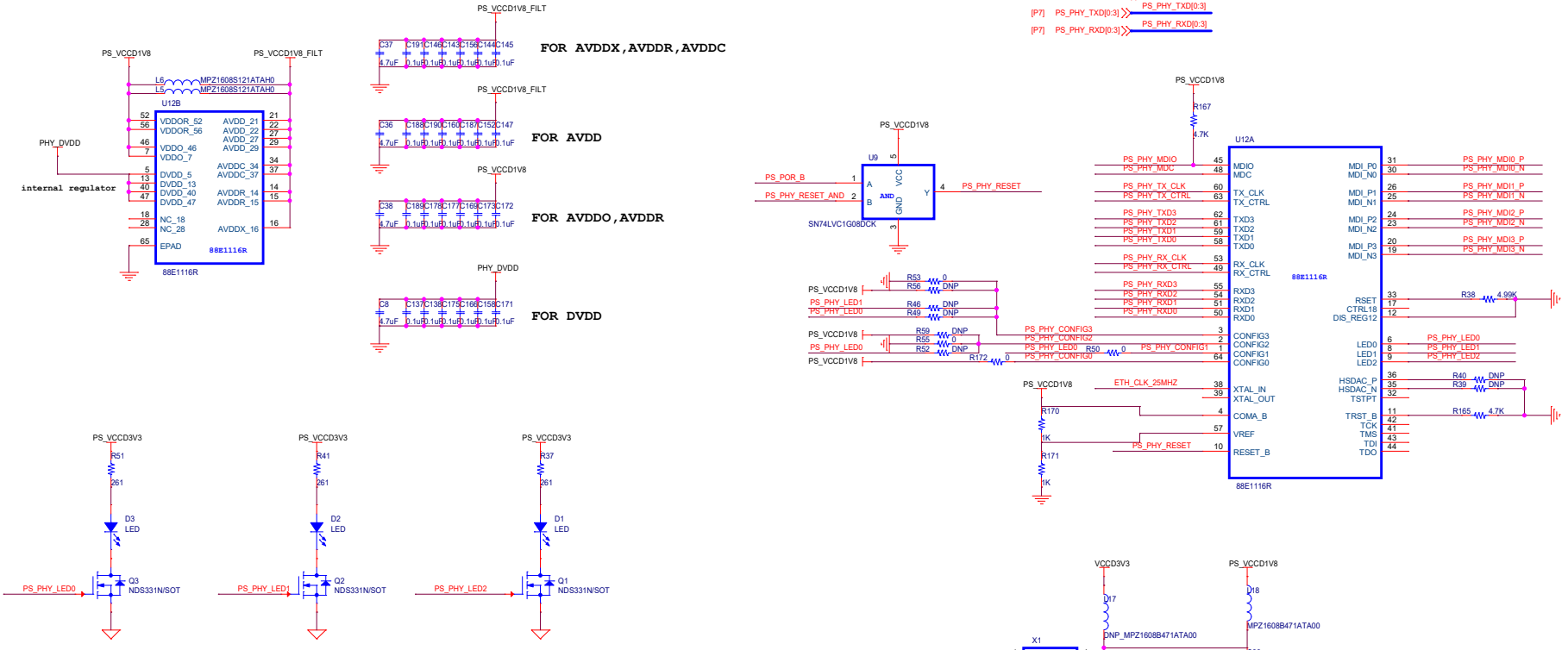
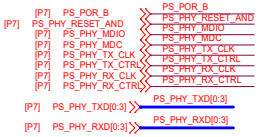
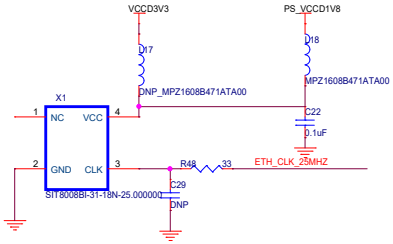
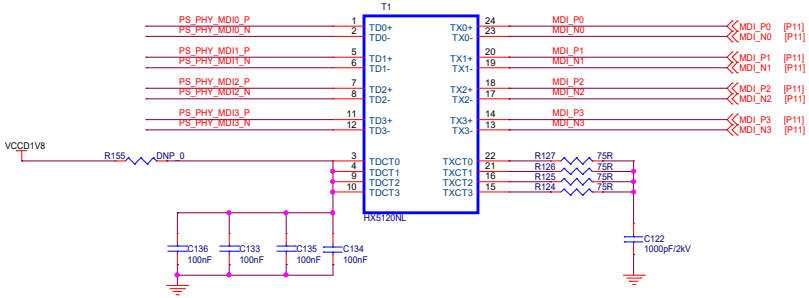
1000/100/10M ETHERNET









CONFIGURATION MAPPINGS

PIN	SETTINGS	CONFIGURATIONS	
CONFIG0	VCCO_MIO1	PHY_ADD[1]=1	PHY_ADD[0]=1
CONFIG1	EPHY_LED0	PHY_ADD[3]=0	PHY_ADD[2]=1
CONFIG2	GND	ENA_XC=0	PHY_ADD[4]=0
	EPHY_LED0	ENA_XC=0	PHY_ADD[4]=1
	VCCO_MIO1	ENA_XC=1	PHY_ADD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_TX=1

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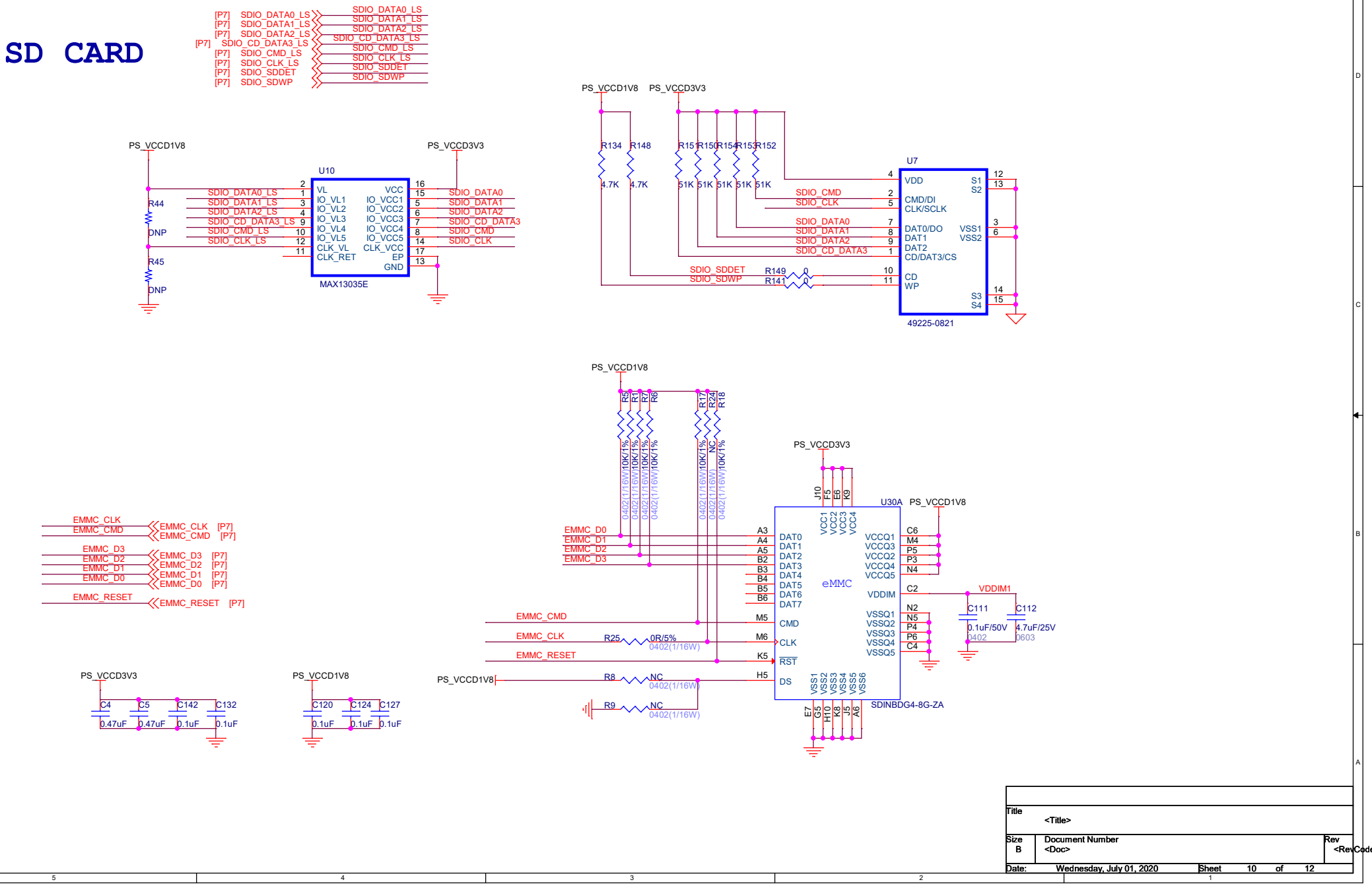
SD CARD



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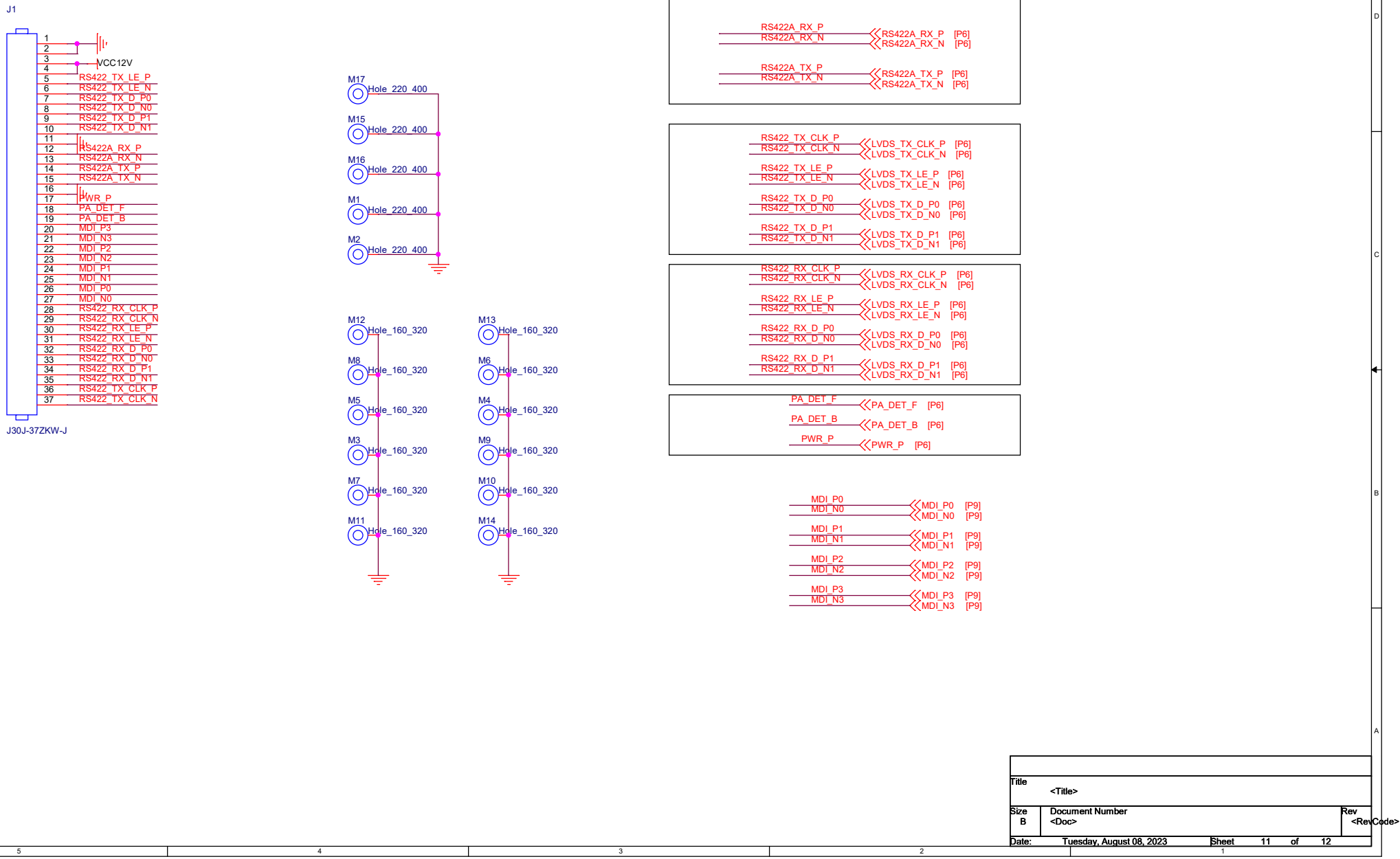
J1
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32
33
34
35
36
37
VCC12V
RS422_TX_LE_P
RS422_TX_LE_N
RS422_TX_D_P0
RS422_TX_D_N0
RS422_TX_D_P1
RS422_TX_D_N1
RS422A_RX_P
RS422A_RX_N
RS422A_TX_P
RS422A_TX_N
PWR_P
PA_DET_F
PA_DET_B
MDI_P3
MDI_N3
MDI_P2
MDI_N2
MDI_P1
MDI_N1
MDI_P0
MDI_N0
RS422_RX_CLK_P
RS422_RX_CLK_N
RS422_RX_LE_P
RS422_RX_LE_N
RS422_RX_D_P0
RS422_RX_D_N0
RS422_RX_D_P1
RS422_RX_D_N1
RS422_TX_CLK_P
RS422_TX_CLK_N
J30J-37ZKW-J
M17
Hole_220_400
M15
Hole_220_400
M16
Hole_220_400
M1
Hole_220_400
M2
Hole_220_400
M12
Hole_160_320
M8
Hole_160_320
M5
Hole_160_320
M3
Hole_160_320
M7
Hole_160_320
M11
Hole_160_320
M13
Hole_160_320
M6
Hole_160_320
M4
Hole_160_320
M9
Hole_160_320
M10
Hole_160_320
M14
Hole_160_320
RS422A_RX_P
RS422A_RX_N
RS422A_RX_P [P6]
RS422A_RX_N [P6]
RS422A_TX_P
RS422A_TX_N
RS422A_TX_P [P6]
RS422A_TX_N [P6]
RS422_TX_CLK_P
RS422_TX_CLK_N
LVDS_TX_CLK_P [P6]
LVDS_TX_CLK_N [P6]
RS422_TX_LE_P
RS422_TX_LE_N
LVDS_TX_LE_P [P6]
LVDS_TX_LE_N [P6]
RS422_TX_D_P0
RS422_TX_D_N0
LVDS_TX_D_P0 [P6]
LVDS_TX_D_N0 [P6]
RS422_TX_D_P1
RS422_TX_D_N1
LVDS_TX_D_P1 [P6]
LVDS_TX_D_N1 [P6]
RS422_RX_CLK_P
RS422_RX_CLK_N
LVDS_RX_CLK_P [P6]
LVDS_RX_CLK_N [P6]
RS422_RX_LE_P
RS422_RX_LE_N
LVDS_RX_LE_P [P6]
LVDS_RX_LE_N [P6]
RS422_RX_D_P0
RS422_RX_D_N0
LVDS_RX_D_P0 [P6]
LVDS_RX_D_N0 [P6]
RS422_RX_D_P1
RS422_RX_D_N1
LVDS_RX_D_P1 [P6]
LVDS_RX_D_N1 [P6]
PA_DET_F
PA_DET_F [P6]
PA_DET_B
PA_DET_B [P6]
PWR_P
PWR_P [P6]
MDI_P0
MDI_N0
MDI_P0 [P9]
MDI_N0 [P9]
MDI_P1
MDI_N1
MDI_P1 [P9]
MDI_N1 [P9]
MDI_P2
MDI_N2
MDI_P2 [P9]
MDI_N2 [P9]
MDI_P3
MDI_N3
MDI_P3 [P9]
MDI_N3 [P9]
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<Title>
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修改记录：

2020-03-08	1．完善原理图，硬件原理图绘制完毕。
2020-03-09	1．完善原理图，增加以太网接口。
2020-03-20	1．修改原理图，修改9361电源独立供电
	2．修改原理图，百兆网口修改为千兆网口

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