IC 基本电气特性

Quiescent current 静态电流

Standby current 低功耗电

Dropout voltage (LDO 4)压降的输 电压

Efficiency 功率

Transient response 顺势

Line regulation 线 调整器

Load regulation 负载调

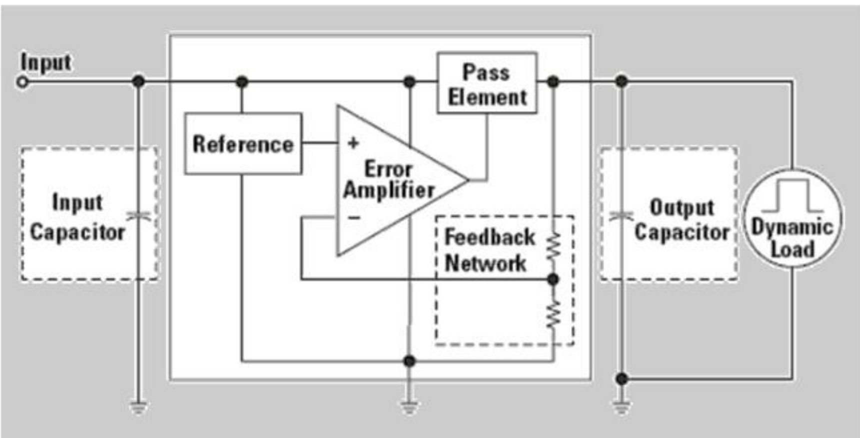
*Power supply rejection 电 /ø^*

Noise

Accuracy †4

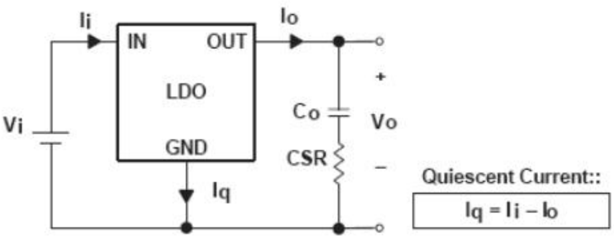
IC 量测

IC（LDO）结构框图



Capacitor 电容 reference 参考（电压）error amplifier 误差信号放大器
Pass element 无源元件（二极管）dynamic load 动态负载
主要模块包括;
Voltage Reference 参考（电压）**Error Amplifier** 误差信号放大器
Feedback Network 反馈网络 Series-pass Element 无源元件（二极管）
优点：简单、输出纹波电压低 、出色的 line 和负载稳压、对负载和 line 的变化响应迅速 、电磁干扰 (EMI) 低
缺点：效率低 、如果需要冷却设备，则要求较大的空间

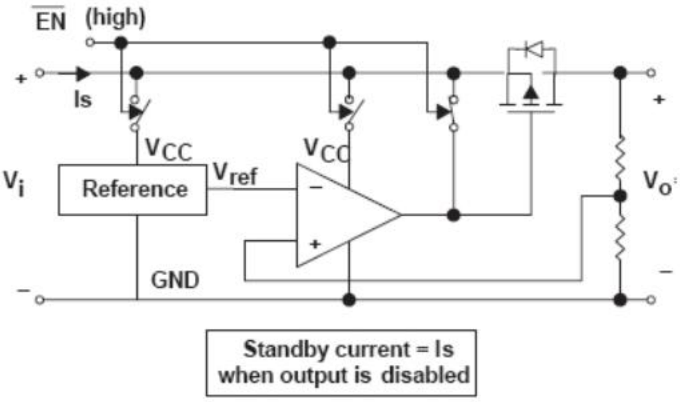
IC基本电气特性—Quiescent Current & Standby Current



Quiescent Current(Ground current):

The difference between input and output。

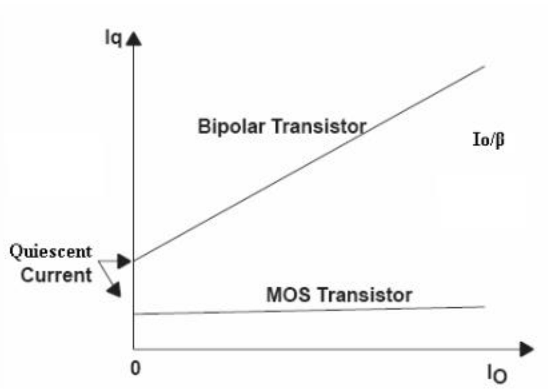
Low quiescent current is necessary to maximize the efficiency. 低静态电流是最大限度地提高效率必要条件 。



Standby Current:

The input current drawn by a regulator when the output voltage is disabled by a shutdown signal.

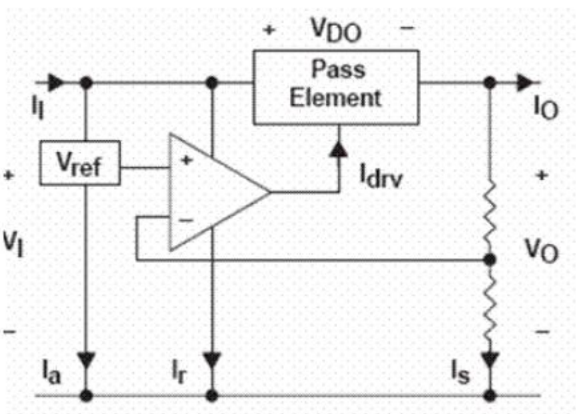
Quiescent Current and Output Current



The value of quiescent current is mostly determined by the series pass element, topologies, ambient temperature, etc. 静态电流的值主要是一系列无源元件，拓扑结构，环境温度等 确定的

具体特性与IC 结构、制程密切相关

IC 基本电气特性— Dropout Voltage（特有规格）



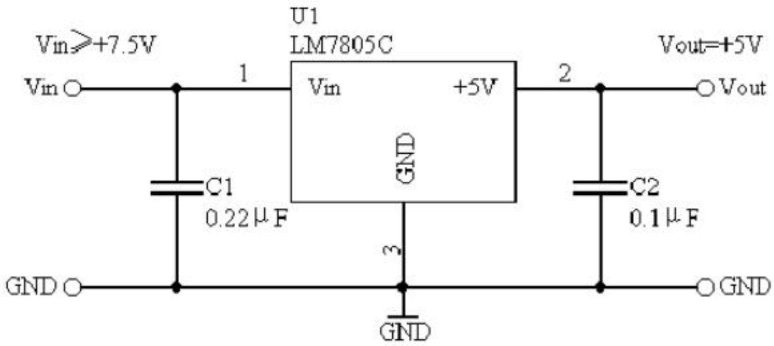
- **Low-Dropout Linear Regulators**
  低压差线性稳压器
- **传统的三端稳压器如：LM78xx**

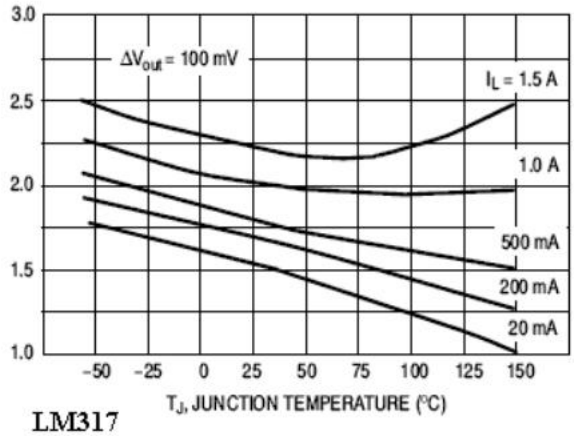
Vdrop 的典型值是 2V，看到很多 7805 应用 时都会背着一个散热器。

LM317 2V

LM1117 1.2V。

LM78XX 系列三端稳压器典型电路



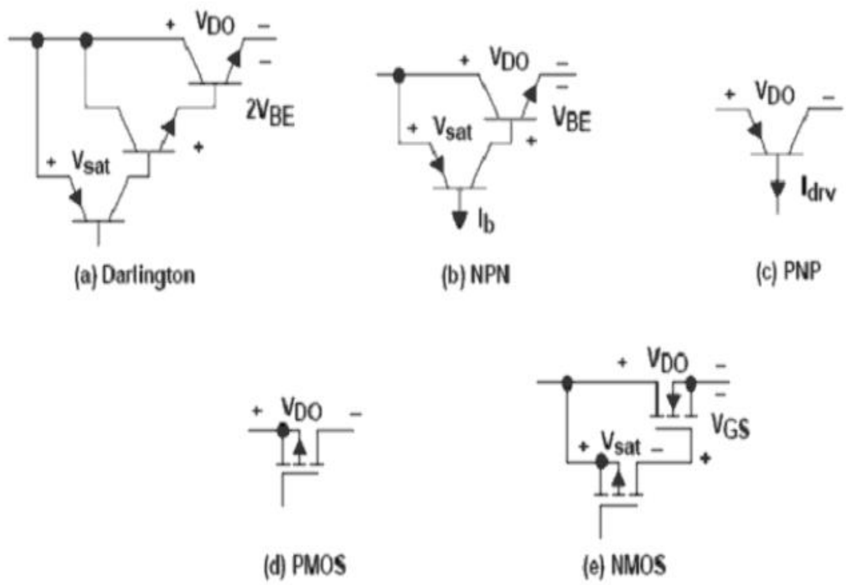


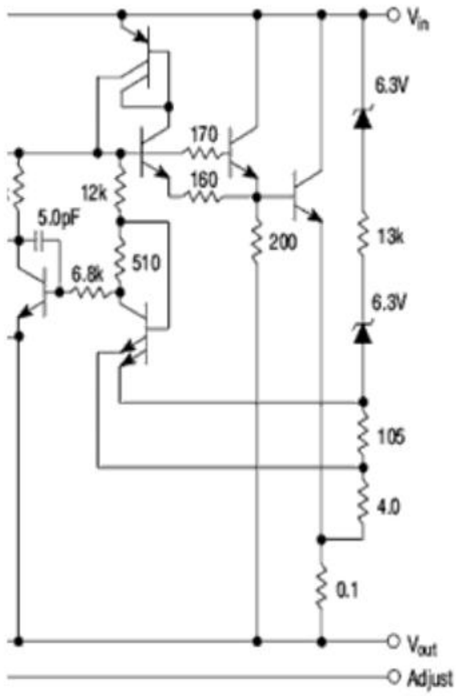
LM317

Figure 8. Dropout Voltage

◆ 调整管采用的结构

LM317 输出



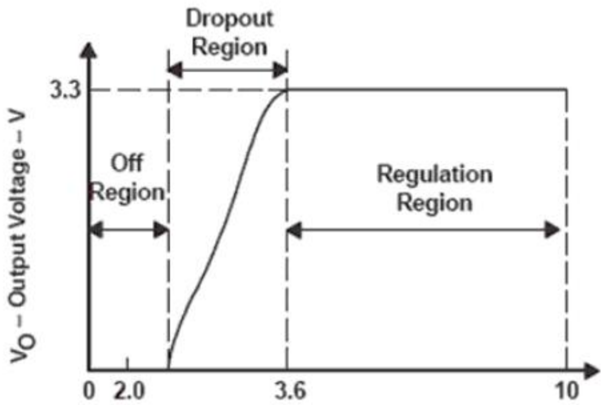


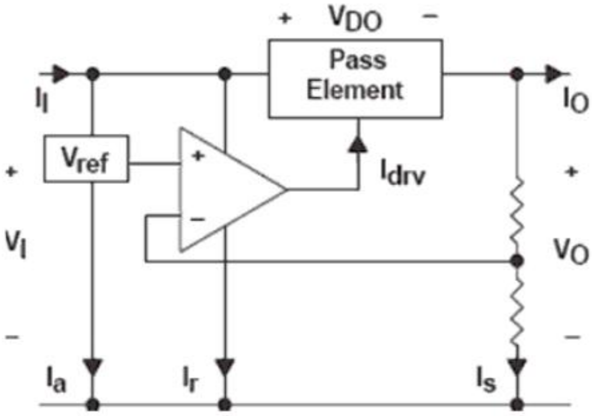
Darlingtong Vdrop=Vsat+2Vbe 1.6~2.5V
NPN Vdrop=Vsat+Vbe >0.9V
PNP Vdrop=Vsat 0.15~0.4V
PMOS Vdrop=Io X Ron 35~350mv
NMOS Vdrop=Vsat+Vgs 1V

◆ 不同调整管结构的比较：

PARAMETER	DARLINGTON	NPN	PNP	NMOS	PMOS
$I_{o,max}$	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{dropout}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	$V_{ce(sat)}$	$V_{sat}+V_{gs}$	$V_{SD(sat)}$
Speed	Fast	Fast	Slow	Medium	Medium

1. **The NMOS pass element is most advantageous due to its low on resistance. Unfortunately, the gate drive difficulties make it less than ideal in applicaitons and as a result there are few NMOS LDOs available.** 传统上,PNP 双极型晶体管应用到低压线性稳压器，主要是因为它很容易实现了低压降电压。
2. **Traditionally, the PNP bipolar transistor has been applied to low dropout applications, primarily because it easily enables a low drop out voltage. However, it has a high quiescent current and low efficiency, which are not ideal in applications where maximizing efficiency is a priority.** 然而，它的高静态电流和低效率，这是不理想的应用最大限度地提高了效率是一个优先事项。
3. **PMOS devices have been highly developed and now have performance levels exceeding most bipolar devices.** PMOS 上设备已经高度发达，现在的性能水平超过最双极器件。





- **Dropout voltage：the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage.** 压降: 对输入至输出差分电压在电路不再规范对进一步削减输入电压;这一点时发生的输入电压接近输出电压。

Vds=Vo-Vin

Dropout Voltage (Note 7)	V_{DROP}	V_{DD} = 5V, I_{OUT} = 2A	--	230	300	mV
		V_{DD} = 5V, I_{OUT} = 1A	--	115	150	

Note 7. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ – 100mV.

IC 基本电气特性—Efficiency

- **The efficiency of a LDO regulator is limited by the quiescent current and input/output voltage as follows:** 效率是有限的 LDO 稳压器的静态电流和输入/输出电压如下: 输入电压降低;这一点时发生的输入电压接近输出电压。

$$Efficiency = \frac{I_o V_o}{\left(I_o + I_q\right) V_i} \times 100 \qquad V_{i\_\min} = V_o + V_{drop}$$

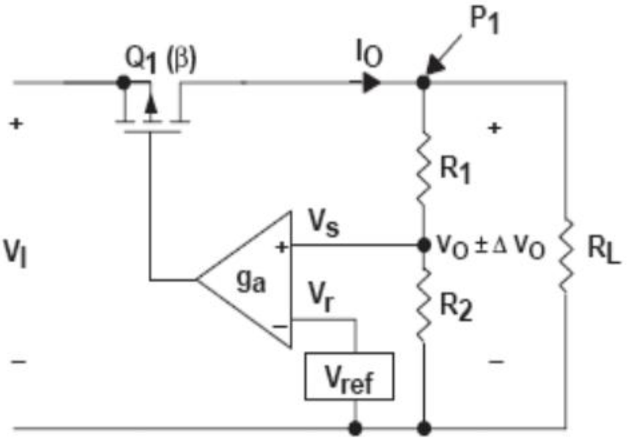
- **To have a high efficiency LDO regulator, drop out voltage and quiescent current must be minimized.** 具有高效率的 LDO 稳压器，电压和辍学静态电流必须减少到最低限度

IC 基本电气特性—Load Regulation

◆ Load Regulation:

A measure of the circuit’s ability to maintain the specified output voltage under varying load conditions. 衡量电路的能力，保持指定的输出电压在不同负载条件下。

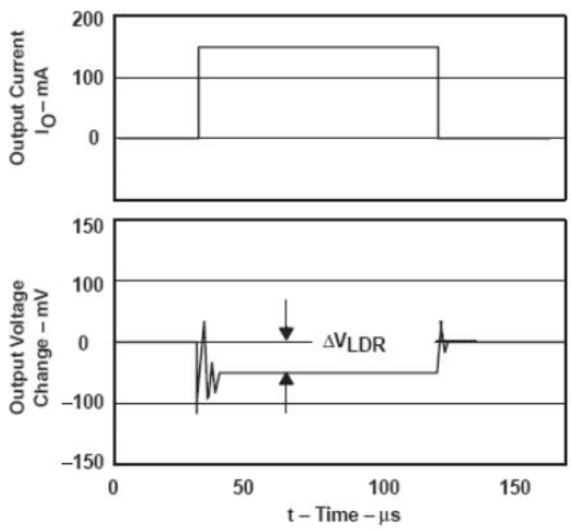
$$\left(\Delta Vo / \Delta Io\right)$$

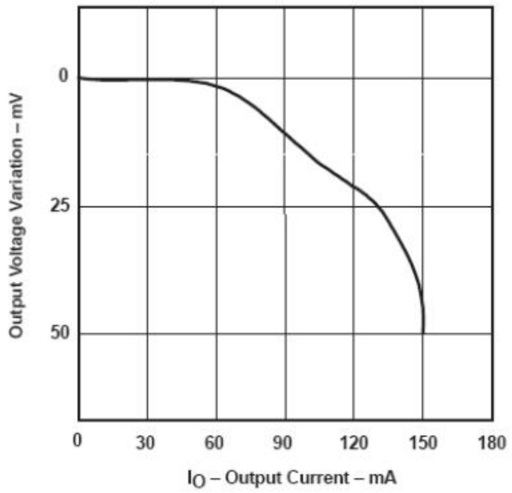


$$\Delta I_o = \beta\ g_a \Delta V_s = \beta\ g_a \left(\frac{R_2}{R_1 + R_2}\right) \Delta V_o$$

$$\frac{\Delta V_o}{\Delta I_o} = \frac{1}{\beta g_a} \left(\frac{R_1 + R_2}{R_2}\right)$$

The load regulation is limited by the open loop current gain of the system. As noted from the above equation, increasing dc open-loop current gain improves load regulation. 负荷调节是有限的开环电流增益的系统。正如上述方程，增加直流开环电流增益改善负载调节。





V_{OUT} Load Regulation (Note 6)	ΔV_{LOAD}	V_{DD} = 5V, I_{OUT} = 2A, V_{IN} = V_{OUT} + 1V	--	0.2	1	%

RT9025

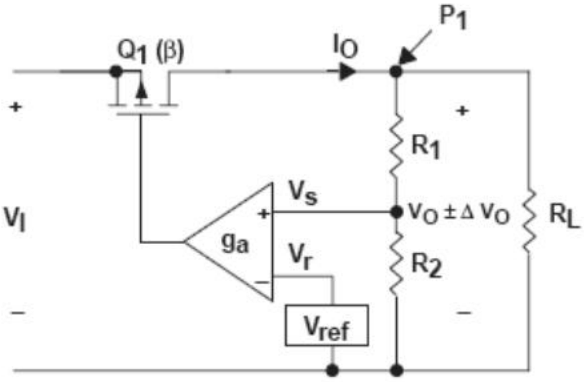
Note 6. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 1mA to 2A.

◆ **Line Regulation:**

a measure of the circuit's ability to maintain the specified output voltage with varying input voltage. 衡量这条赛道的能力，保持指定的输出电 voltage. open 环电流增益改善负载调节。

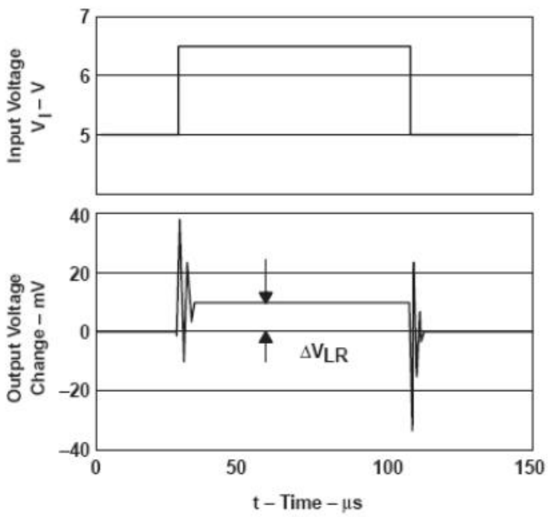
$$(\Delta Vo / \Delta Vi)$$

$$\frac{\Delta V_O}{\Delta V_I} = \left[\frac{1}{(R_{ds} + R_L)\beta g_a}\right]\left(\frac{R_1 + R_2}{R_2}\right)$$

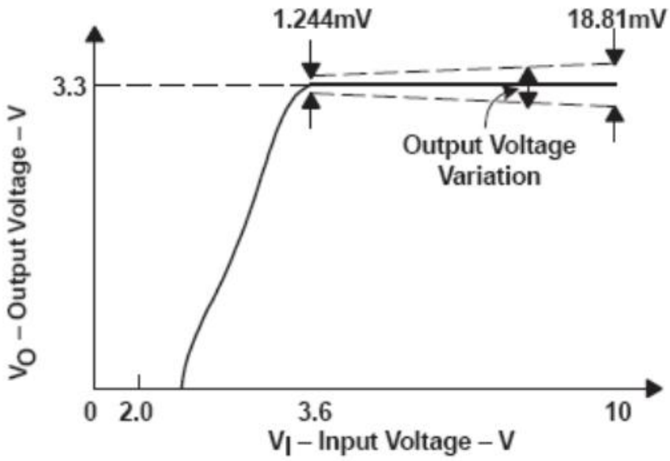


其中， Rds 为调整管 Q1 源漏等效电阻。

◆ **Increasing dc open loop current gain improves the line regulation.** 提高直流开环电流增益提高了线路调整



Line Transient Response



Output Voltage With Respect to Input Voltage

V_{OUT} Line Regulation (V_{IN})	ΔV_{LINE_IN}	V_{DD} = 5V, V_{IN} = V_{OUT} + 1V to 5V I_{OUT} = 1mA	--	0.2	0.6	%

RT9025

Line Regulation1	$\Delta V_{LNR}1$	V_{IN}=6V to 25V, Io=1mA, V_O=3.3V/3.5V V_{IN}=7V to 25V, Io=1mA, V_O=5V	---	5	30	mV
Line Regulation2	$\Delta V_{LNR}2$	V_{IN} =6V to 25V, Io=1µA, V_O=3.3V/3.5V V_{IN} =7V to 25V, Io=1µA, V_O=5V	---	5	30	mV

G920

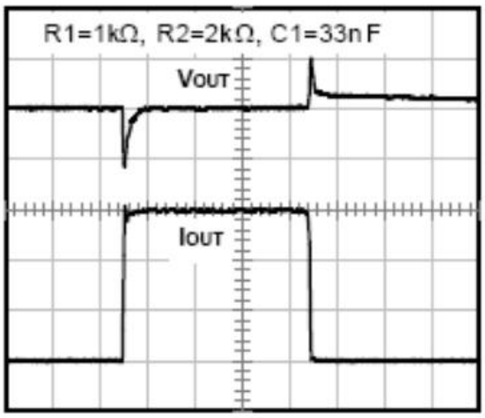
IC 基本电气特性—Transient Response

- **Transient Response:**
  the maximum allowable output voltage variation for a load current (input voltage) step change. 瞬态响应：允许的最大输出电压变化的负载电流（输入电压）一步变化。

- The transient response is a function of the output capacitor value (Co), the ESR of the output capacitor, the buypass capacitor (Cb), and the maximum load-current (Io,max). 瞬态响应是一个功能的输出电容值（公司）中，电子自旋共振的输出电容器，电容器的 buypass （炭黑），最大负载电流（ Io ，最大值）。

$$\Delta V_{tr,\,max} = \frac{I_{o,max}}{C_o + C_b}\,\Delta t_1 + \Delta V_{ESR}$$

I_{OUT} = 10mA -> 3A ->10mA



Where △t1 corresponds to the closed loop bandwidth. △ESR is the voltage variation resulting from the presence of the ESR of the output capacitor. △ESR is proportional to ESR.

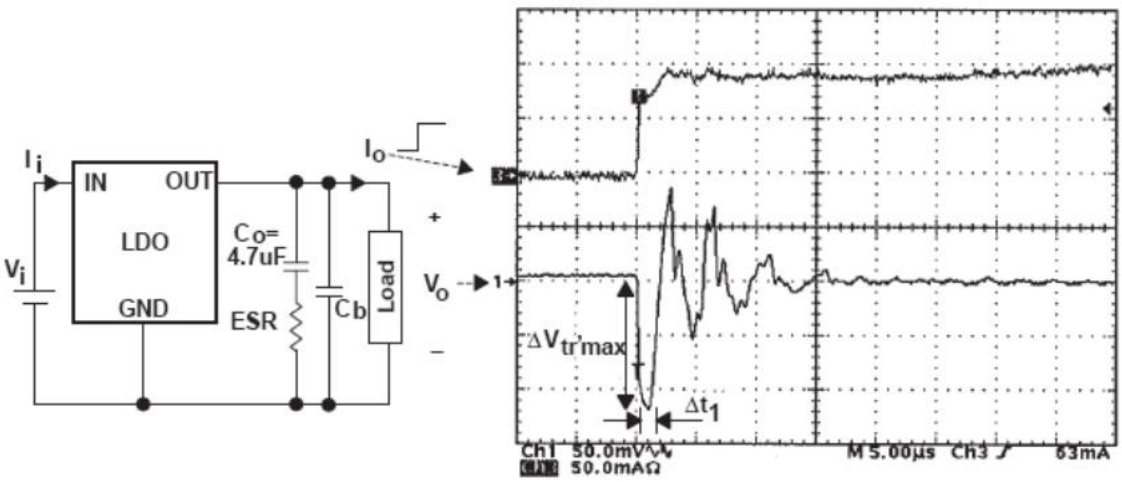
凡△ t1 闭环带宽。△esr 是电压变化造成在场的情况下的 ESR 的输出电容器。△esr 成正比 esr。

Ch1 : V_{OUT}, 50mV/Div

Ch2 : I_{OUT}, 1A/Div

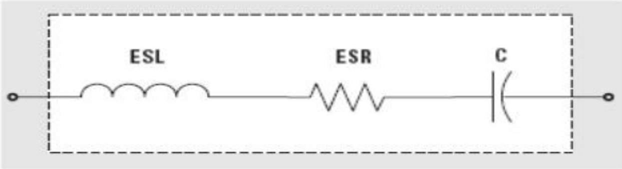
Time : 20µS/Div

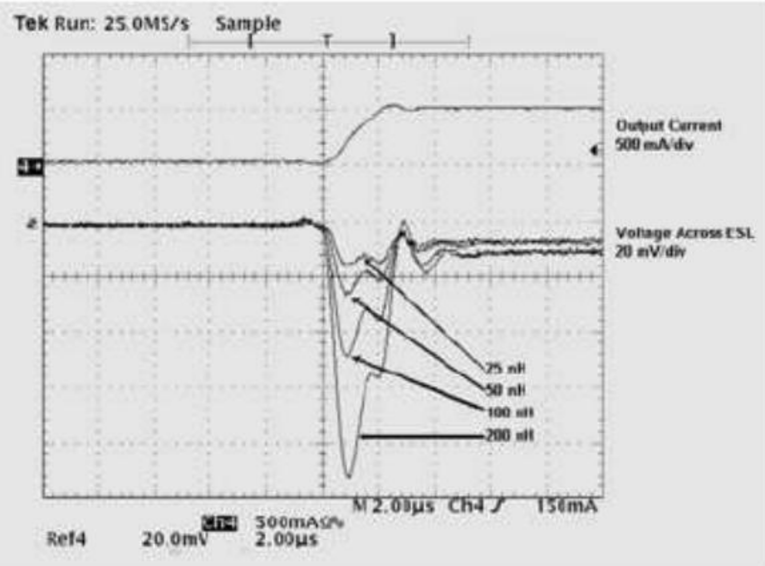
APL5913

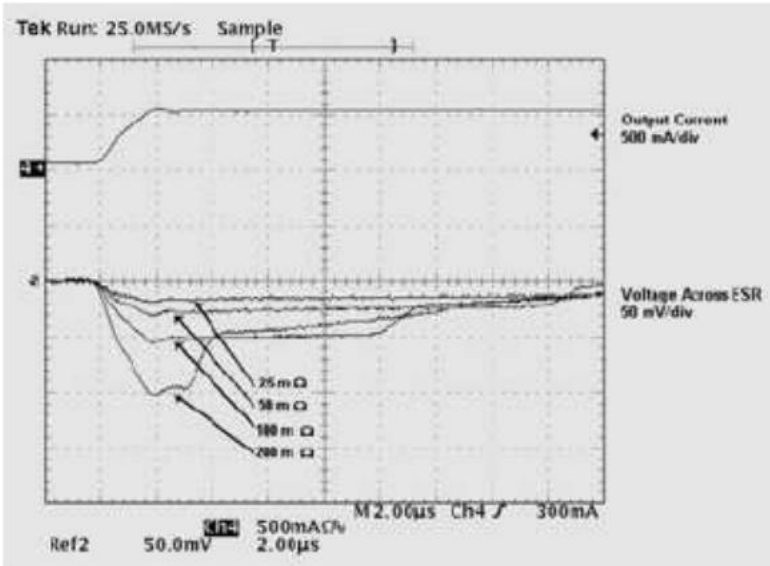


Transient Response of LDO Regulator 瞬态响应 LDO 稳压器

◆ 输出电容的影响







ESL load-transient response 负载瞬态响应 ESR load-transient response

ESL 影响比较小，但不合适的 PCB 布线同样使得性能下降。

ESR 是越小越好，但 成本＋稳定性

IC 基本电气特性－ Power Supply Rejection

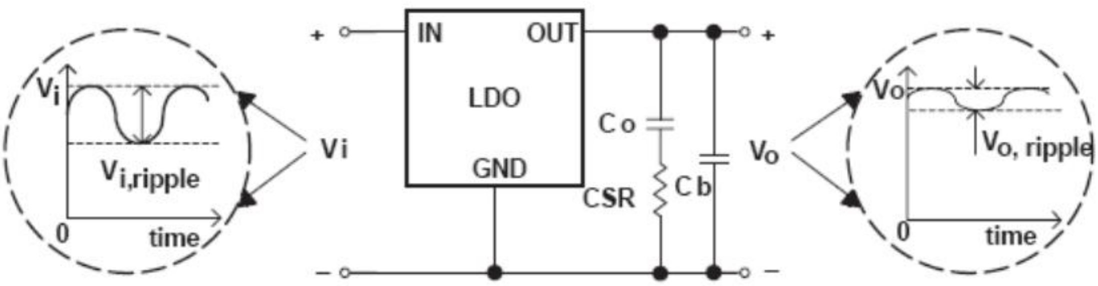
◆ **PSRR:**

also known as ripple rejection, measures the LDO regulator's ability to prevent the regulated output voltage fluctuating caused by input voltage variations. 也被称为纹波抑制，措施的 LDO 稳压器的能力，以防止输出电压波动所造成的输入电压的变化

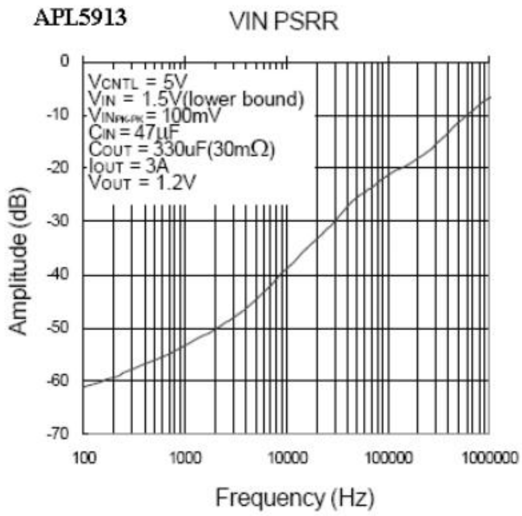
$$\boxed{PSRR = \frac{V_{o,\,ripple}}{V_{i,ripple}} \text{ at all frequencies}}$$

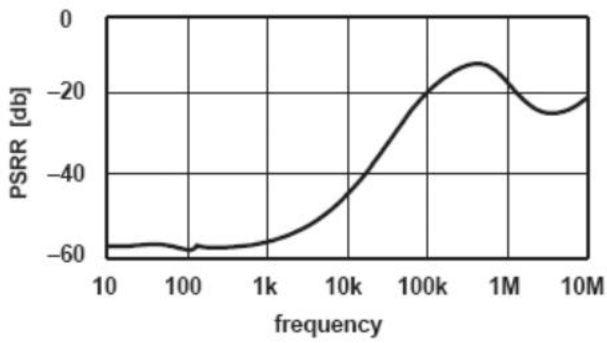
The same relation for line regulation applies to PSRR except that the whole frequency spectrum is considered. 同样的关系线适用于的 PSRR ，但整个频谱是考虑。

PSRR is based on small signals, whereas line transients are large signals. PSRR 是基于小信号，而电压瞬态大信号。



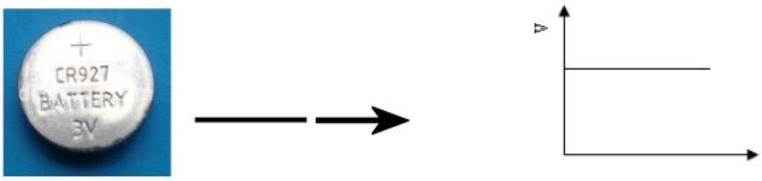
Very critical in many RF and wireless application 非常关键的在许多射频和无线应用



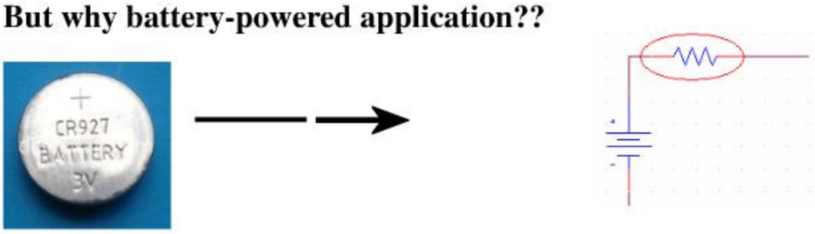


supply rejection in the frequency band between 100 kHz and 1 MHz is especially important in applications where the output of a dc/dc switch mode power supply (SMPS) is used to power the linear regulator 抑制频带在 100 kHz 和 1 MHz 的是特别重要的应用场合中的输出的 DC / DC 开关模式电源（ SMPS ）是用于功率的线性稳压器

But why battery-powered application??

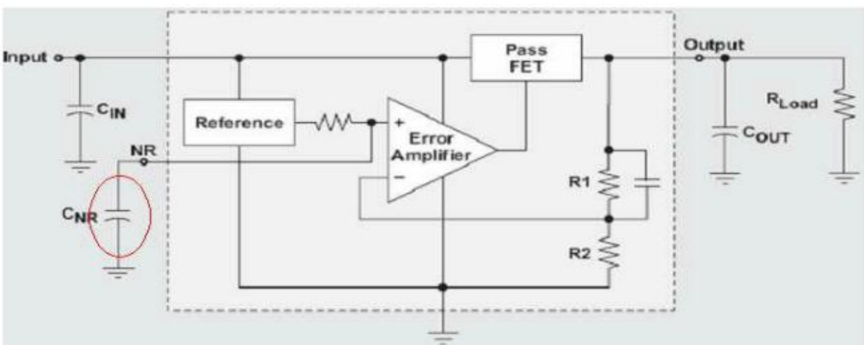


But why battery-powered application??



The output voltage will show a large variation based upon the current drawn from that battery. 输出电压将出现大的变化根据目前从该电池。

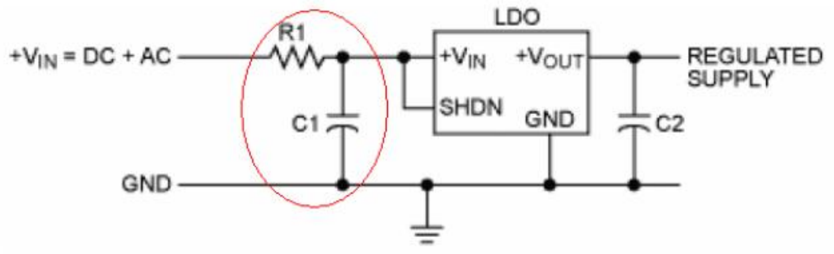
In GSM, transmit and receive cycles in the RF draw a huge amount of current, causing a large change in voltage on the output of the battery. That change in voltage is seen throughout the system and on inputs to all of the system regulators. 在 GSM ，传输和接收周期中的射频吸引了大量的电流，造成一个大的变化对输出电压的电池。这一变化在电压是整个系统，并投入到所有的系统监管。



One of the dominant internal sources of PSRR in an LDO is the bandgap reference. so it's important to have a bandgap reference with high PSRR. 其中一个主要的内部来源的 PSRR 的 LDO 中的带隙基准。因此，必须有一个带隙基准高的 PSRR 。

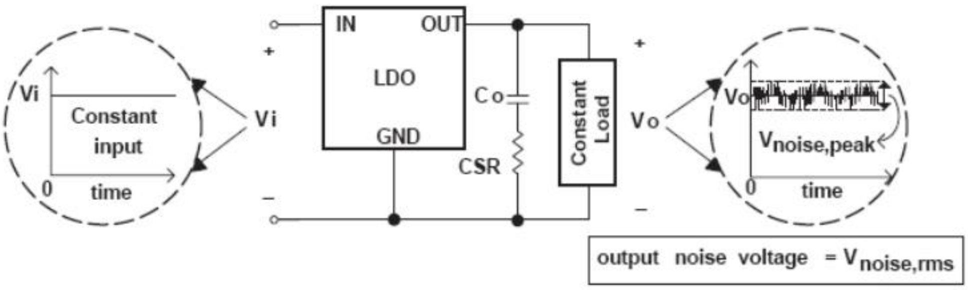
Board layout must be carefully done to reduce the feedthrough from input to output via board parasitics. 电路板布局必须认真进行，以减少馈从输入输出通过董事会寄生。

- **Improved Power Supply Rejection For IC Linear Regulators**



- **LC filter** 滤波器……

IC 基本电气特性－ Noise



- 在输出信号中包含我们不需要的信号。

  PSRR、**NOISE** 容易混淆的概念！

  PSRR 一输入变化引起输出的变化，抑制能力

  NOISE－固有特性，和外部无关，主要由芯片内部电阻、晶体管产生。

- 衡量 **NOISE** 的两种式：

Spectral 谱线 **noise density** 密度 **—a curve** 曲线 **that shows noise (uV/ √Hz) versus** 相对 **frequency** 频率**,that is,noise spectral density cure with units uV/ √Hz plotted over frequency**

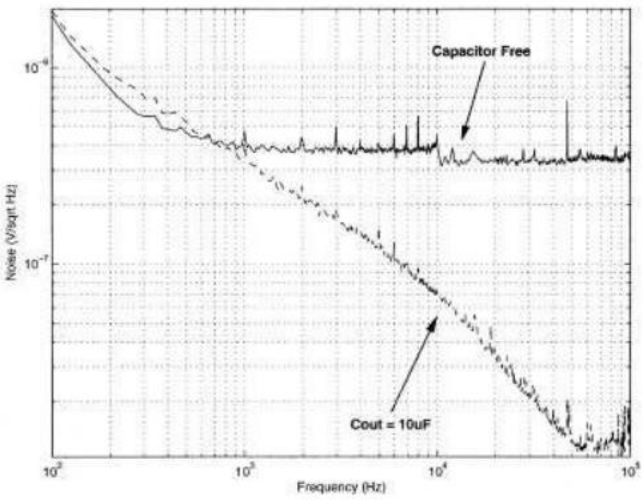
Equipment 设备**:**
spectrum analyzer 光谱分析器.

Integrated 综合的 **output noise — output noise voltage (in µ Vrms)**

spectral noise density integrated over a certainfrequency range and can therefore be thought of as the total noise in a specified frequency range.

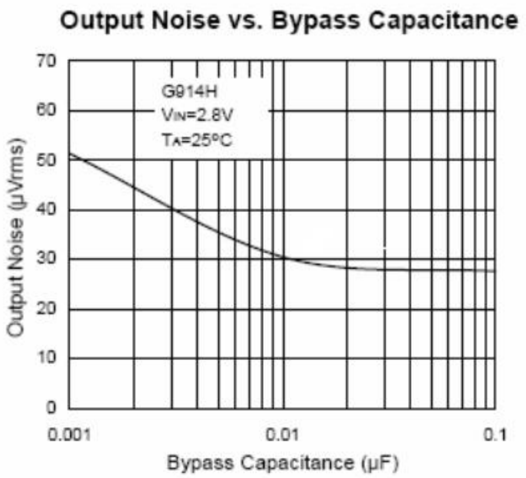
Equipment:
True root-mean-square(Rms)meter

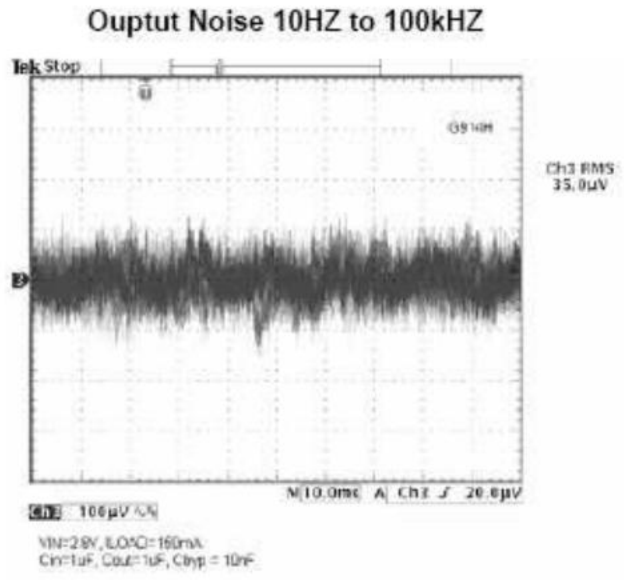
Absolute measurement with units uV-RMS(root mean square)take over a fixed bandwidth

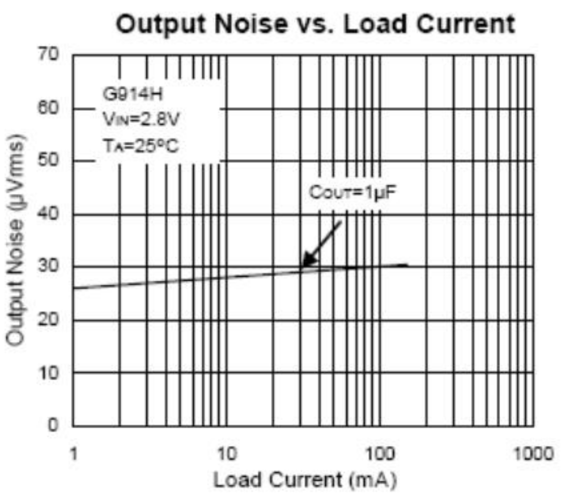


真有效值测量 **AC / DC**

Output Noise Voltage (RMS)	f = 100Hz to 100kHz, I_{LOAD} = 10mA	MAX8840	11	µV
		MAX8841/MAX8842	230	
	f = 100Hz to 100kHz, I_{LOAD} = 80mA	MAX8840	13	
		MAX8841/MAX8842	230	







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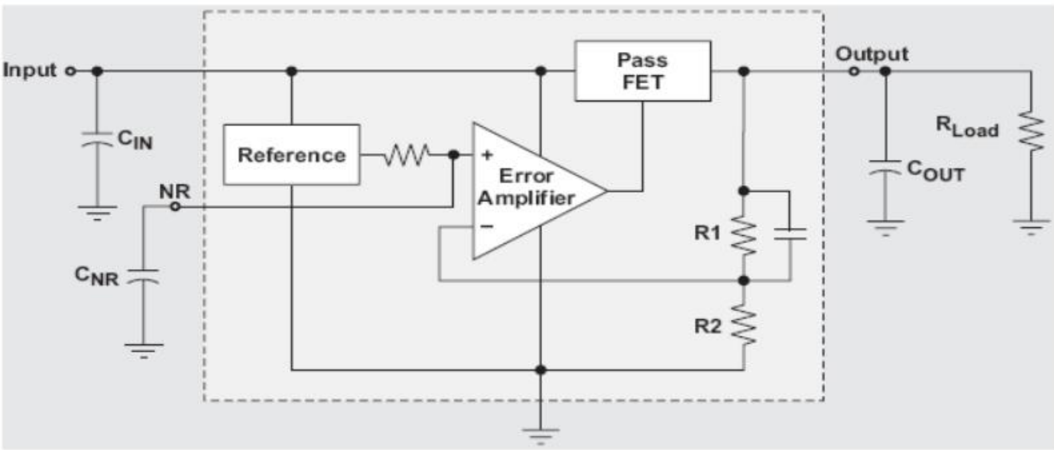
Output Voltage Noise (10Hz to 100kHz) (G914H)	C_{OUT} = 1μF, I_{OUT} = 150mA, C_{BYP}=1nF	---	52	---	μV_{RMS}
	C_{OUT} = 1μF, I_{OUT} = 150mA, C_{BYP}=10nF	---	35	---	
	C_{OUT} = 1μF, I_{OUT} = 150mA, C_{BYP}= 100nF	---	30	---	
	C_{OUT} = 1μF, I_{OUT} = 1mA, C_{BYP} = 10nF	---	26	---	



◆ 噪声源：

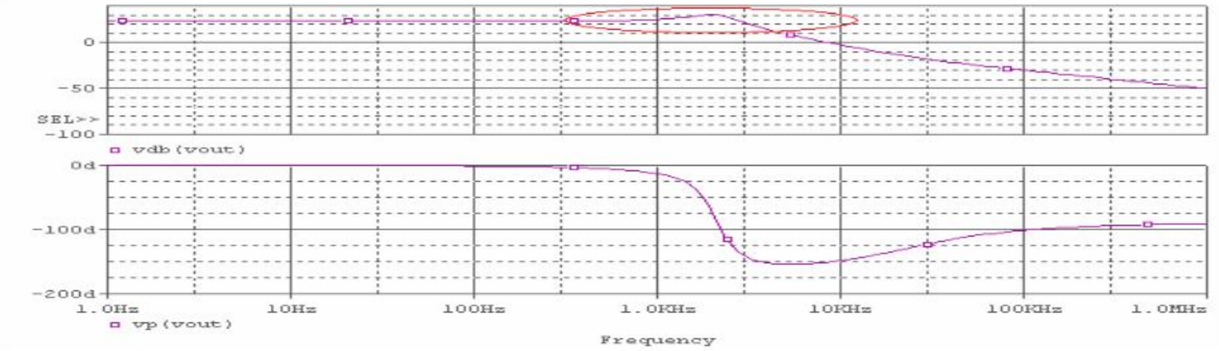
Reference 一重要因素，通过外接 LPF 来减小基准噪声的影响。但电容也不能太大，否则会对启动产生影响。LPF 的 CUTOFF 频率一般会设在 1-500KHz

resistor divider 电阻分割器 一热噪声 4KTR，要减小噪声，采样电阻的阻值不能取很大。和低功耗要求相矛盾，如果噪声是必须考虑的因素，也只有部分的牺牲功耗。

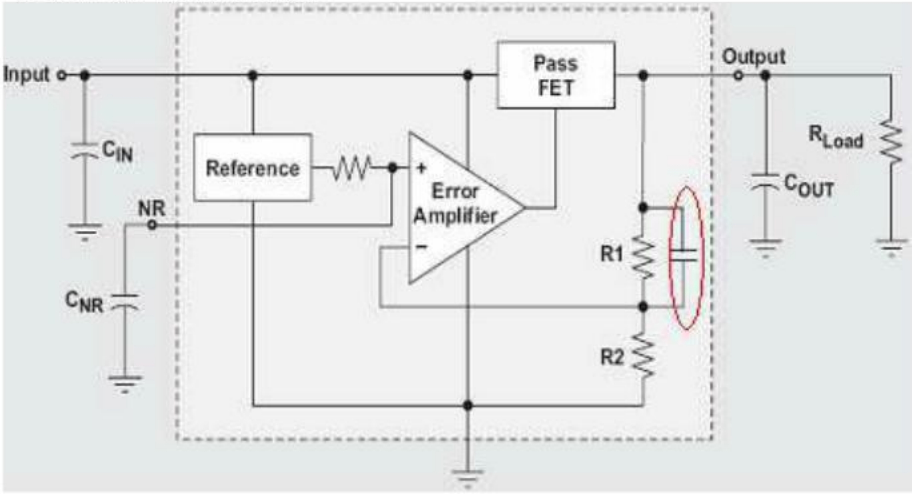
EA -- 若是 2 级运放，则低噪声设计，第一级提供大部分的 GAIN。

PASS FET 一调整管虽然占芯片比较大的面积，对 NOISE 的影响不大，因为和其它几个因素相比，PASS FET 缺少了增益级。

◆ 整个环路的频率特性也会对 NOISE 产生影响。



相位裕度减小，环路趋于不稳定，增益的峰值变大。output noise voltage (in μVrms) 是对频域的噪声做积分，噪声的增益大了，所以噪声也会大。所以对于低噪声的设计，尽量采用大的相位裕度。



如果可以的话可以在 R1 两端并一个小电容,这样在高频时,基准到输出之间是一个单位增益的放大器。

IC 基本电气特性－ Accuracy 准确性

◆ **Accuracy:**

specifies all effects of line regulation (△VLR), load regulation (△VLDR), reference voltage drift (△Vo,ref), error amplifier voltage drift (△Vo,a),external sampling resistor tolerance (△Vo,r), and temperature coefficient (△VTC). 指定所有影响线路调整，负载调节，参考电压漂移，误差放大器电压漂移，外部取样电阻宽容，和温度系数。

$$Accuracy \approx \frac{|\Delta V_{LR}| + |\Delta V_{LDR}| + \sqrt{\Delta V_{0,ref}^2 + \Delta V_{0,a}^2 + \Delta V_{0,r}^2 + \Delta V_{TC}^2}}{V_0} \times 100$$