Gate-Level Analysis of LSTM Structures for Digital Predistortion of RF Power Amplifiers

Qiyuan Wu
School of Communication Engineering
Xi'an University of Electronic Science and Technology
Email: qiyuan.wu@example.com

***Abstract*—This paper investigates the role of individual gate components in LSTM architectures for digital predistortion (DPD) of power amplifiers...**

***Index Terms*—Digital Predistortion, LSTM, Gate Analysis, Power Amplifier, Neural Networks**

I. Introduction

- Background of DPD and its importance in PA linearization.
- Motivation for using LSTM-based neural networks.
- Research gap: lack of gate-level analysis.
- Contributions and paper organization.

II. Related Work

A. Neural Networks for PA Behavioral Modeling

Review of traditional and deep learning DPD models.

B. Gated Recurrent Architectures in DPD

Overview of LSTM, GRU, and RRU structures; discussion of prior work.

III. Proposed Methodology

A. Problem Formulation

Define the DPD modeling objective and data representation.

B. Model Variants Design

Describe different LSTM gate modifications: NFG, NIG, NIAF, CIFG, etc.

C. Evaluation Framework

Metrics: NMSE, EVM, ACLR, N_PARAM; training setup and comparison design.

IV. Experimental Setup

Hardware, dataset preprocessing, hyperparameters, and configuration.

V. Results and Analysis

A. Performance Comparison

Quantitative results for all models.

B. Gate-Level Importance Discussion

Analysis of each gate's contribution to DPD performance.

C. Complexity and Efficiency

Trade-off between performance and parameter count.

VI. Discussion

Interpretation of results, implications, and relation to prior work.

VII. Conclusion and Future Work

Summary of findings and future research directions.

References