ECE 550D
Fundamentals of Computer Systems and Engineering

Fall 2023

Storage and Clocking

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Slides are derived from work by
Andrew Hilton, Tyler Bletsch and Rabih Younes (Duke)

Last time…

- Who can remind us what we did last time?
  - Add
  - Substract
  - Bit shift
  - Floating point

So far…

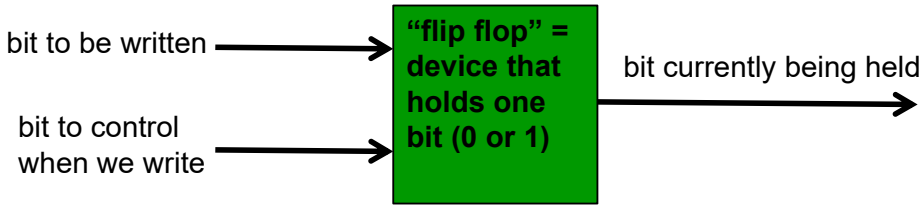
- We can make logic to compute "math"
  - Add, subtract,… (we'll see multiply/divide later)
  - Bitwise: AND, OR, NOT,…
  - Shifts
  - Selection (MUX)
  - …pretty much anything
- But processors need state (hold value)
  - Registers
  - …

Memory Elements

- All the circuits we looked at so far are combinational circuits: the output is a Boolean function of the inputs.
- We need circuits that can remember values (registers, memory)
- The output of the circuit is a function of the input and a function of a stored value (state)
- Circuits with storage are called sequential circuits
- Key to storage: feedback loops from outputs to inputs

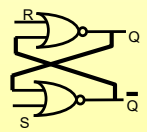
Ideal Storage – Where We're Headed

- Ultimately, we want something that can hold 1 bit and we want to control when it is re-written

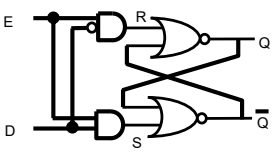


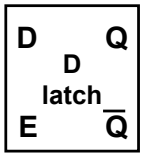
- However, instead of just giving it to you as a magic black box, we're going to first dig a bit into the box

Building up to the D Flip-Flop and beyond

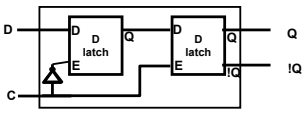


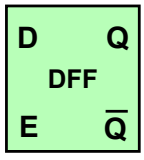
SR Latch
(too awkward)



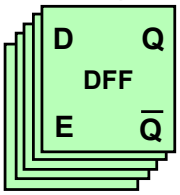


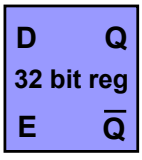
D Latch
(bad timing)





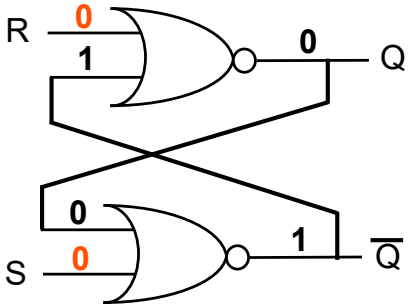
D Flip-Flop
(okay but only one bit)

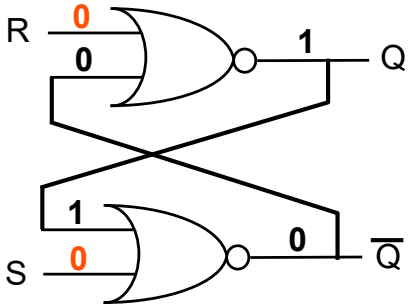




Register
(*nice!*)

FF Step #1: NOR-based Set-Reset (SR) Latch

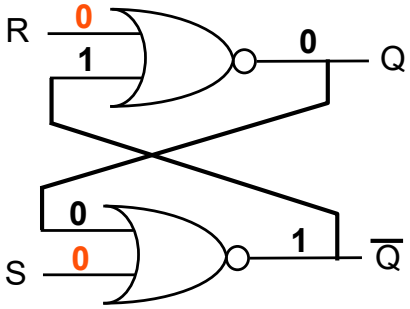


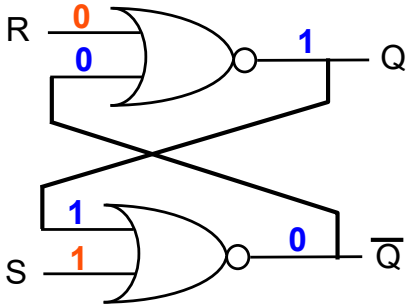


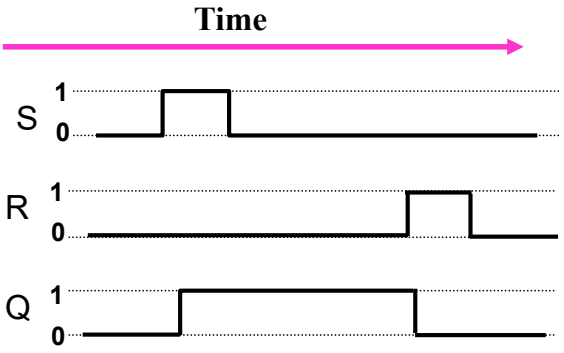
R	S	Q
0	0	Q
0	1	1
1	0	0
1	1	–

Don't set both S & R to 1.
Seriously, don't do it.

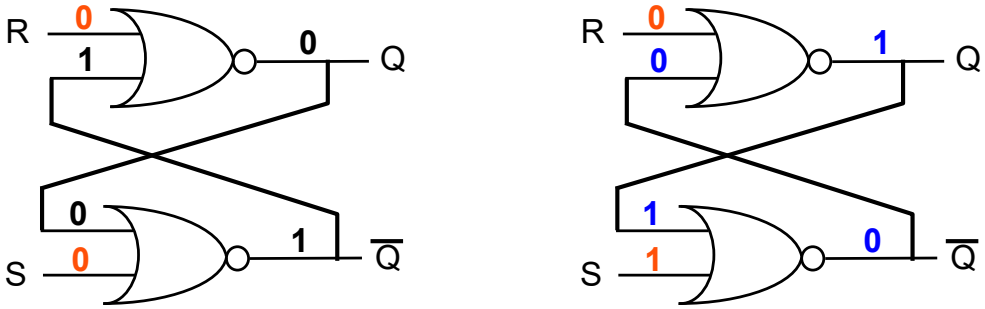
Set-Reset Latch (Continued)

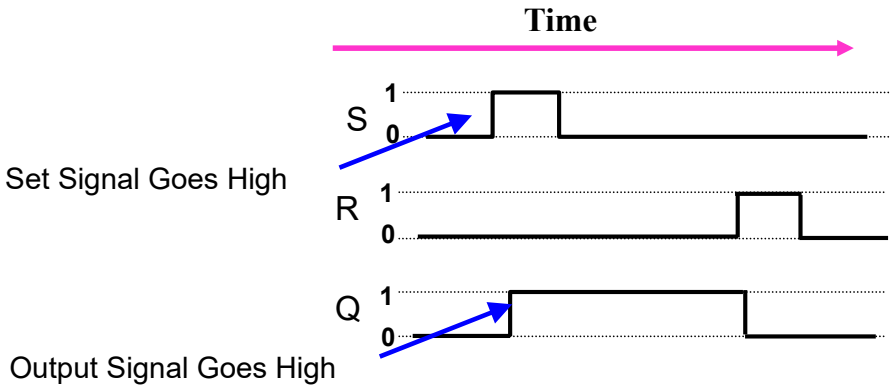




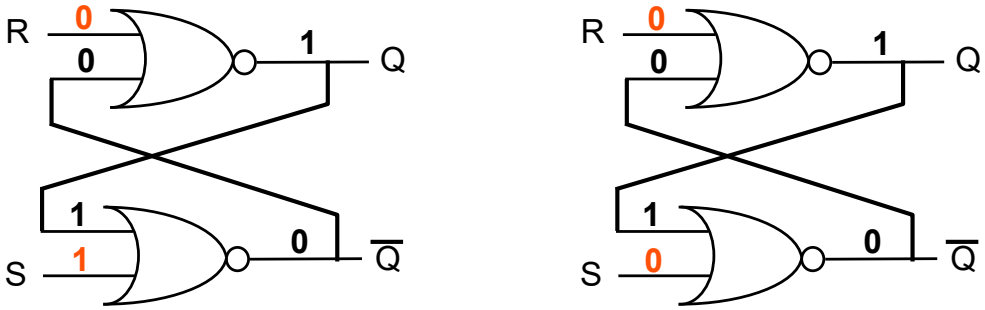


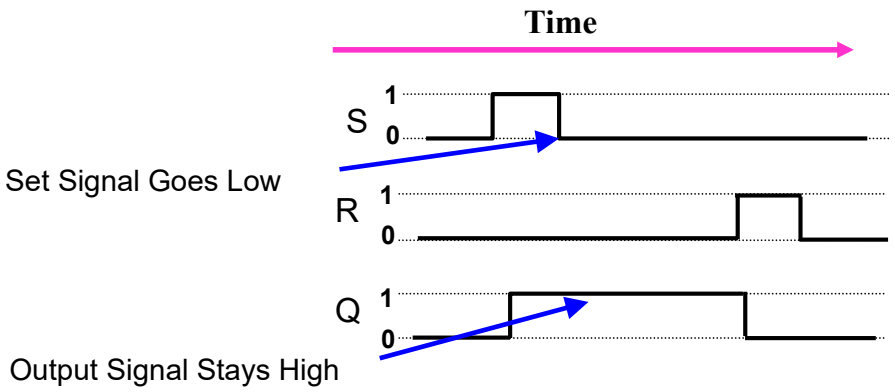
Set-Reset Latch (Continued)



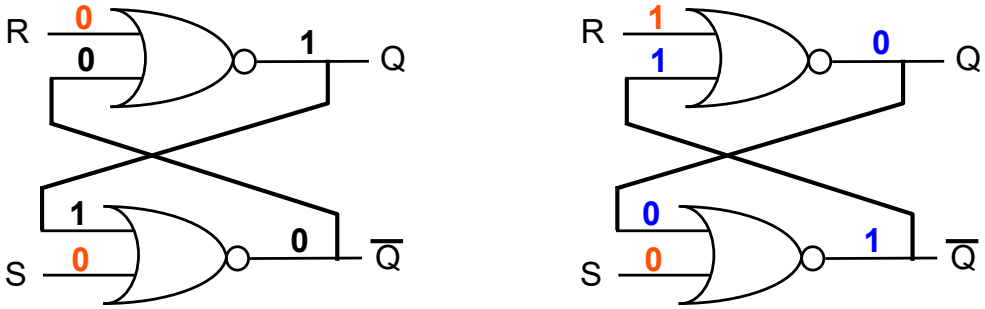


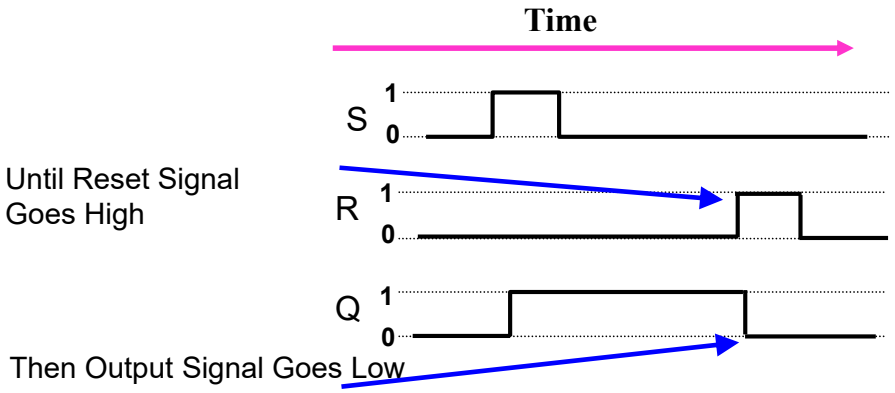
Set-Reset Latch (Continued)





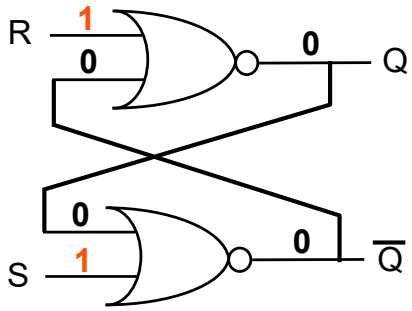
Set-Reset Latch (Continued)



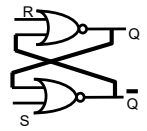


SR Latch

- Downside: S and R at once = chaos
- Downside: Bad interface
- So let's build on it to do better

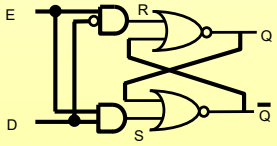


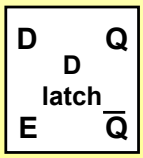
Building up to the D Flip-Flop and beyond



SR Latch

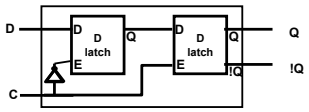
(too awkward)

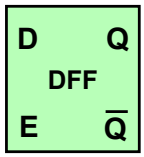




D Latch

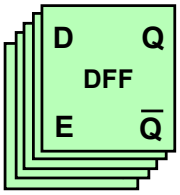
(bad timing)

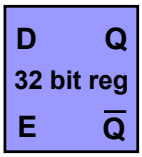




D Flip-Flop

(okay but only one bit)





Register

(*nice!*)

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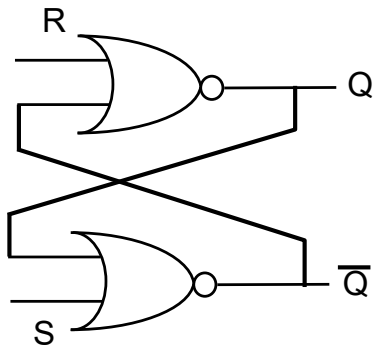
FF Step #2: Data Latch ("D Latch")



Starting with SR Latch

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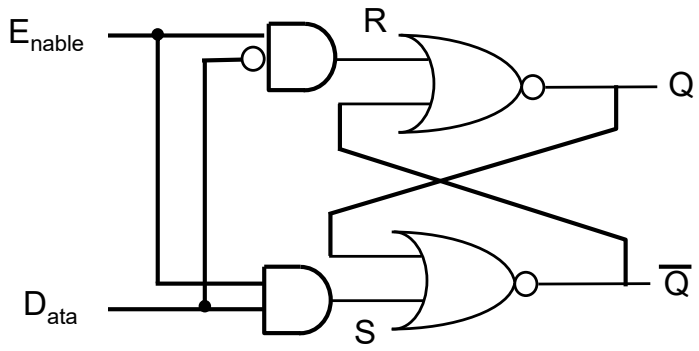
Data Latch (D Latch)

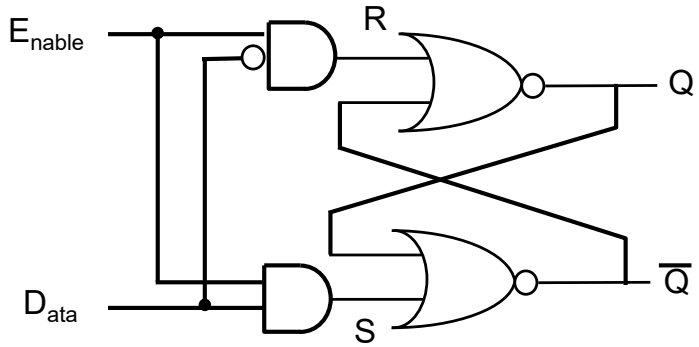


Starting with SR Latch

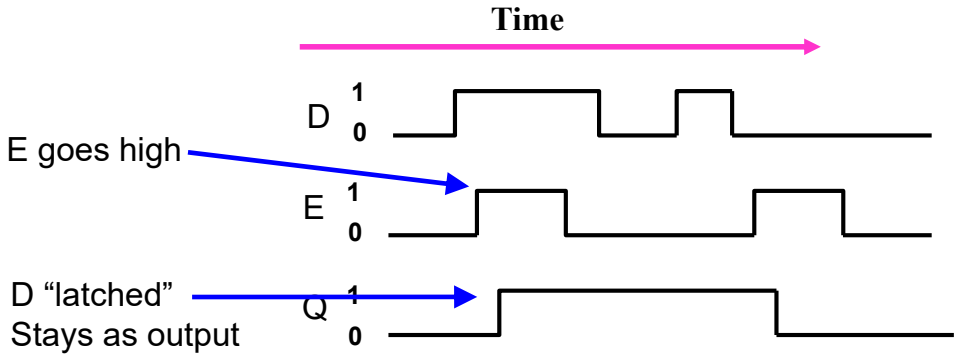
Change interface to
Data + Enable (D + E)

If E=0, then R=S=0.
If E=1, then S=D and R=!D

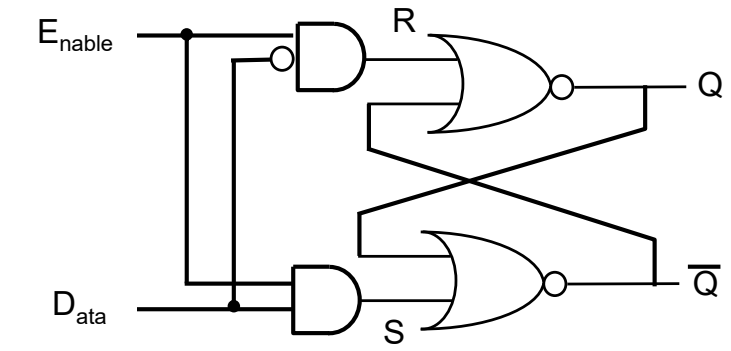
Data Latch (D Latch)



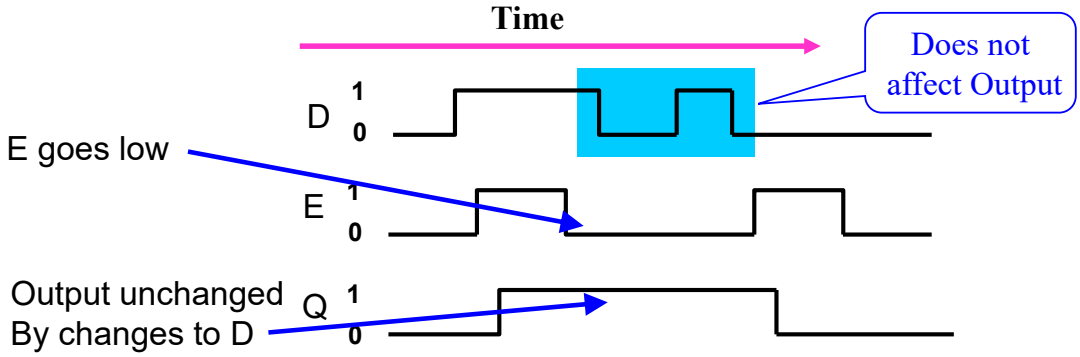
D	E	Q
0	1	0
1	1	1
-	0	Q



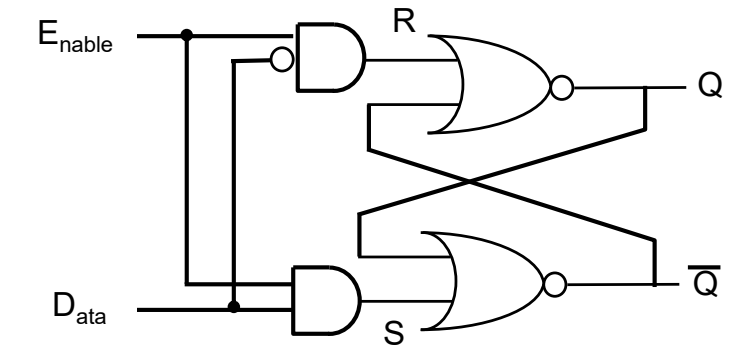
Data Latch (D Latch)



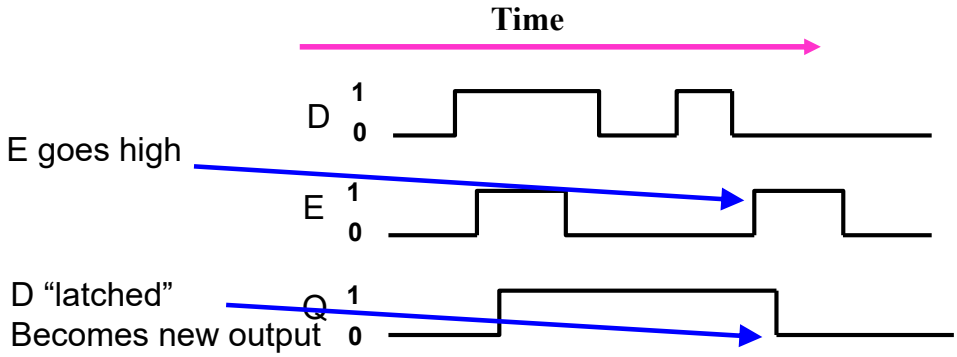
D	E	Q
0	1	0
1	1	1
-	0	Q



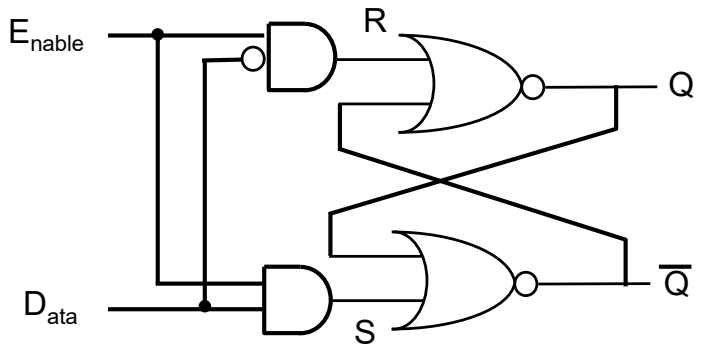
Data Latch (D Latch)



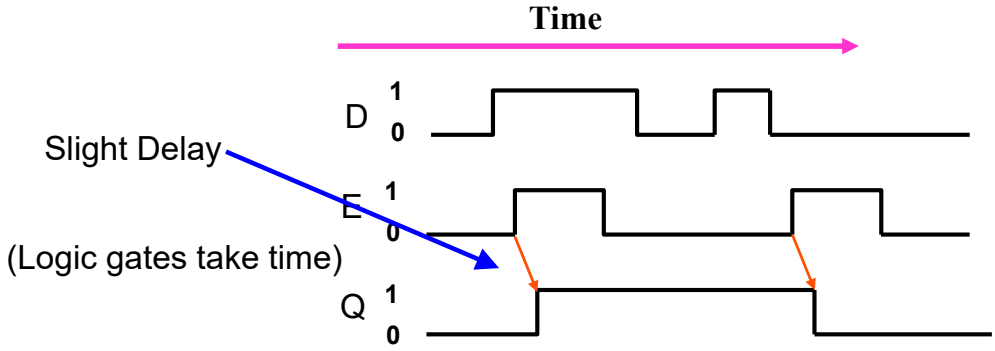
D	E	Q
0	1	0
1	1	1
-	0	Q



Data Latch (D Latch)



D	E	Q
0	1	0
1	1	1
-	0	Q

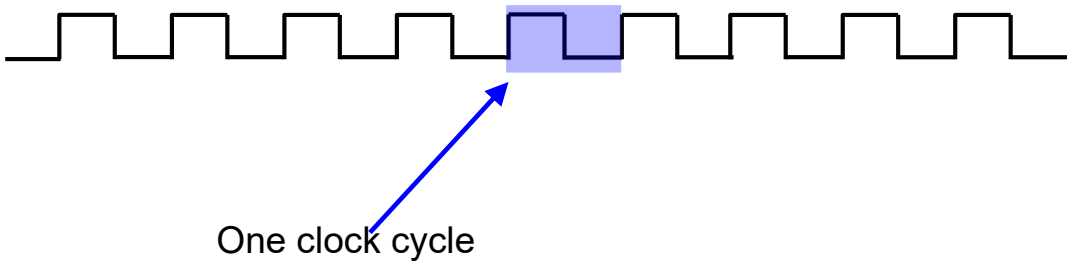


Logic Takes Time

- Logic takes time:
  - Gate delays: delay to switch each gate
  - Wire delays: delay for signal to travel down wire
  - Other factors (not going into them here)
- Need to make sure that signals timing is right
  - Don't want to have races or wacky conditions..

Clocks

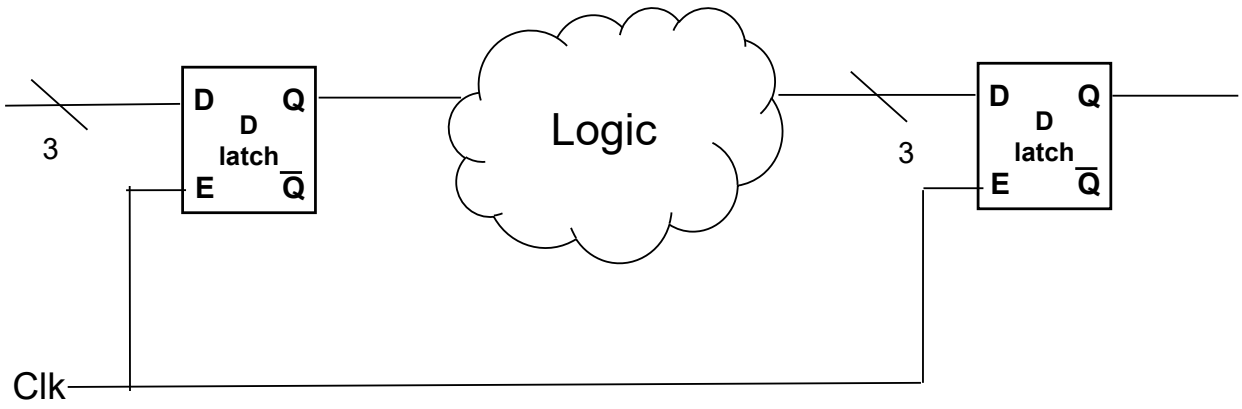
- Processors have a clock:
  - Alternates 0 1 0 1
  - Like the processor's internal metronome
  - Latch → logic → latch in one clock cycle



  - 3.4 GHz processor = 3.4 Billion clock cycles/sec

FF Step #3: Using Level-Triggered D Latches

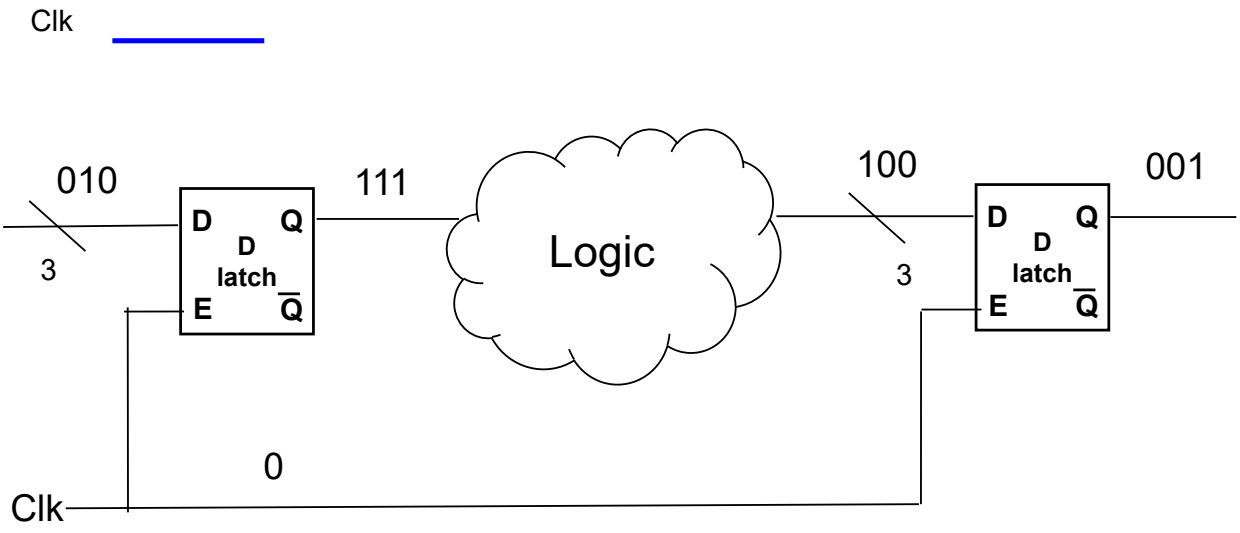
- First thoughts: Level Triggered
  - Latch enabled when clock is high
  - Hold value when clock is low



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

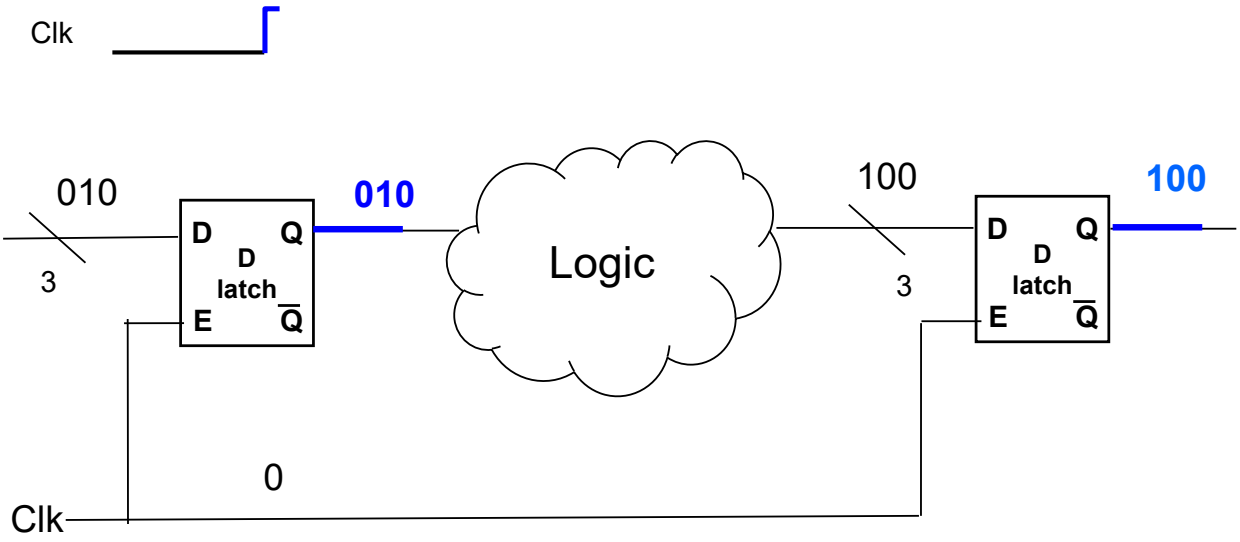
- How we'd like this to work
  - Clock is low, all values stable



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

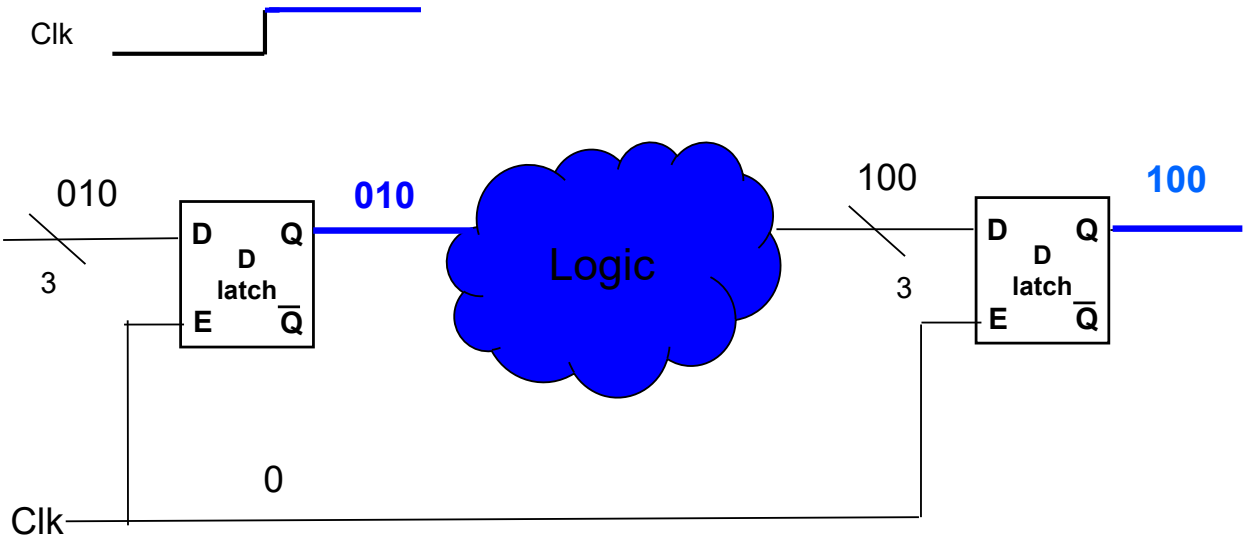
- How we'd like this to work
  - Clock goes high and latches capture new values



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

- How we'd like this to work
  - Signals work their way through logic w/ high clk



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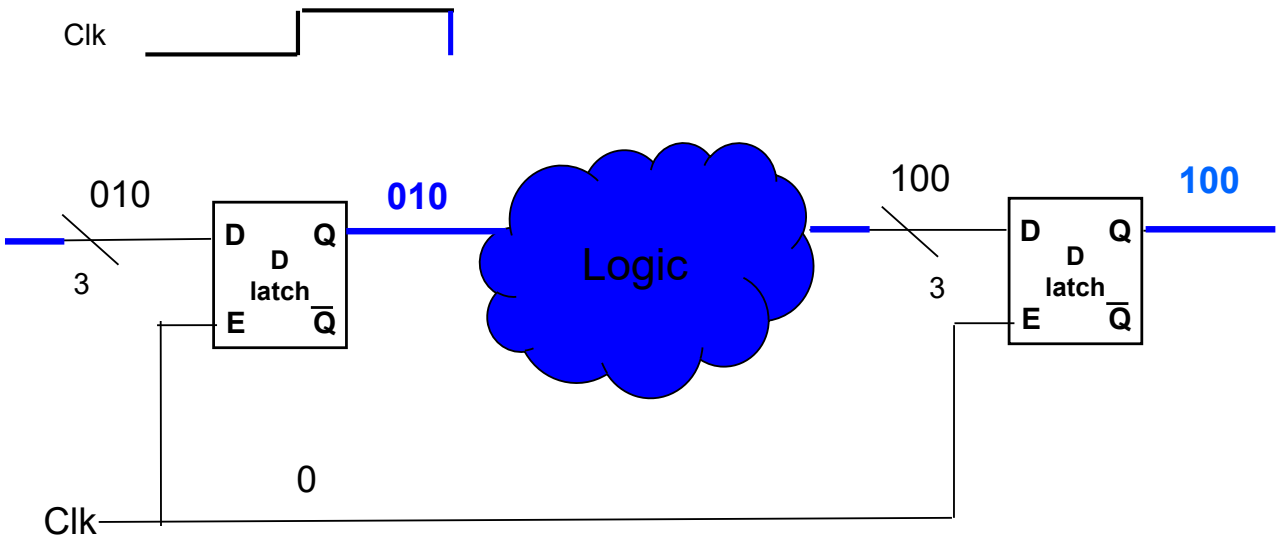
Strawman: Level Triggered

- How we'd like this to work
  - Clock goes low before signals reach next latch



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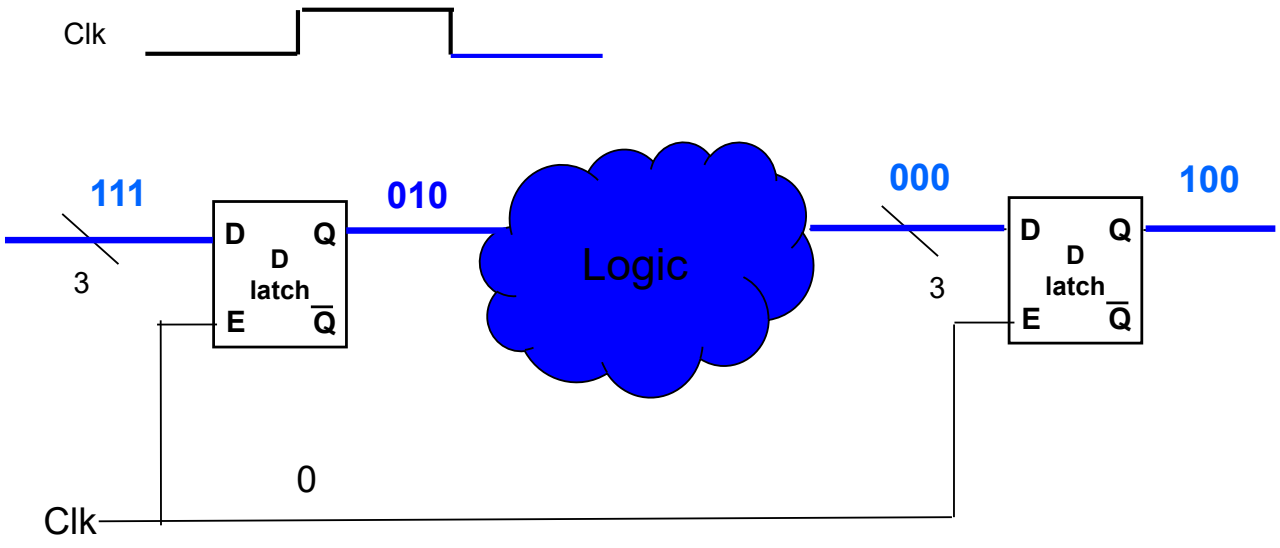
Strawman: Level Triggered

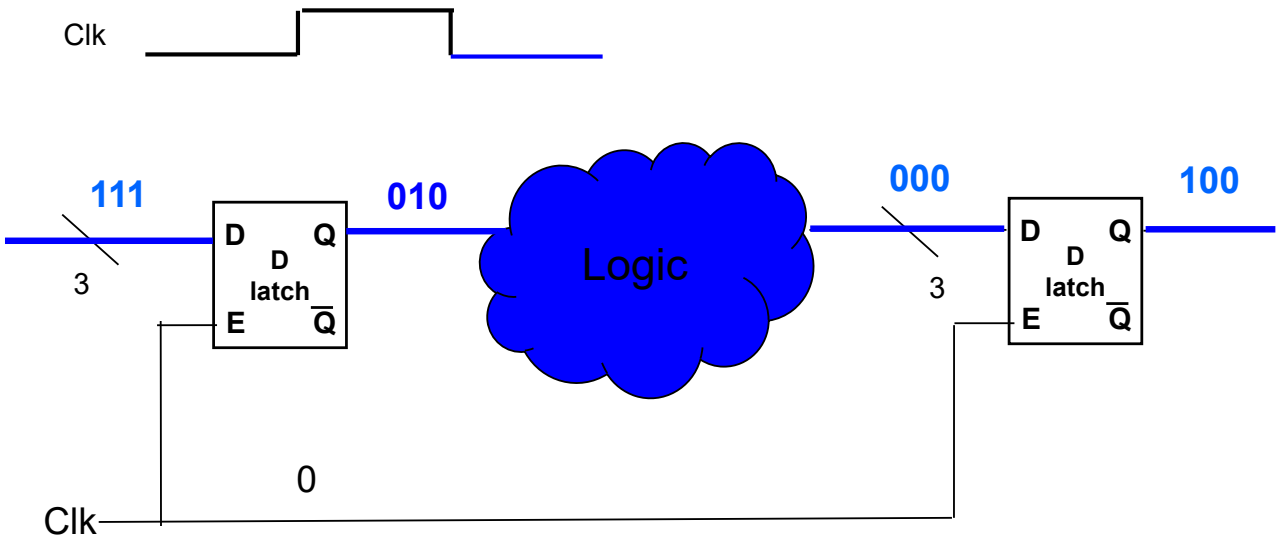
- How we'd like this to work
  - Clock goes low before signals reach next latch



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

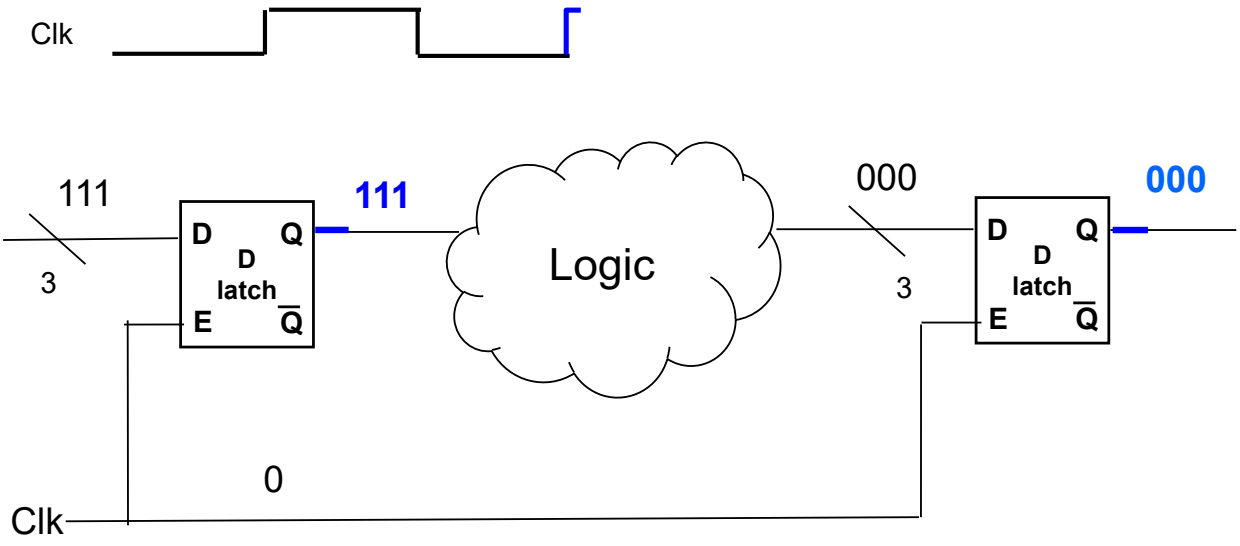
- How we'd like this to work
  - Everything stable before clk goes high



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

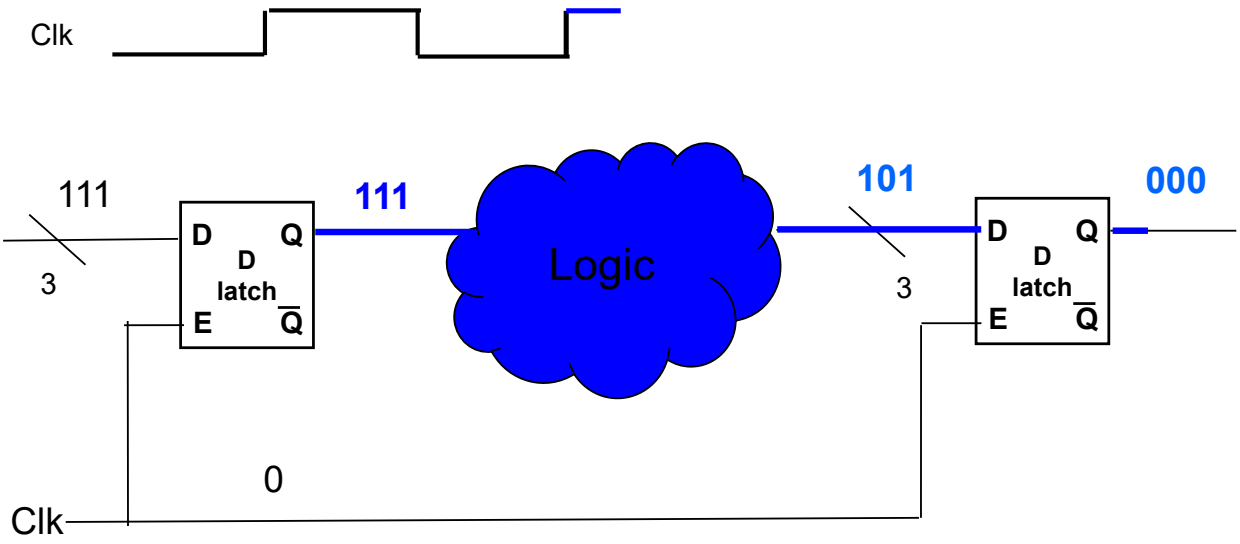
- How we'd like this to work
  - Clk goes high again, repeat



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

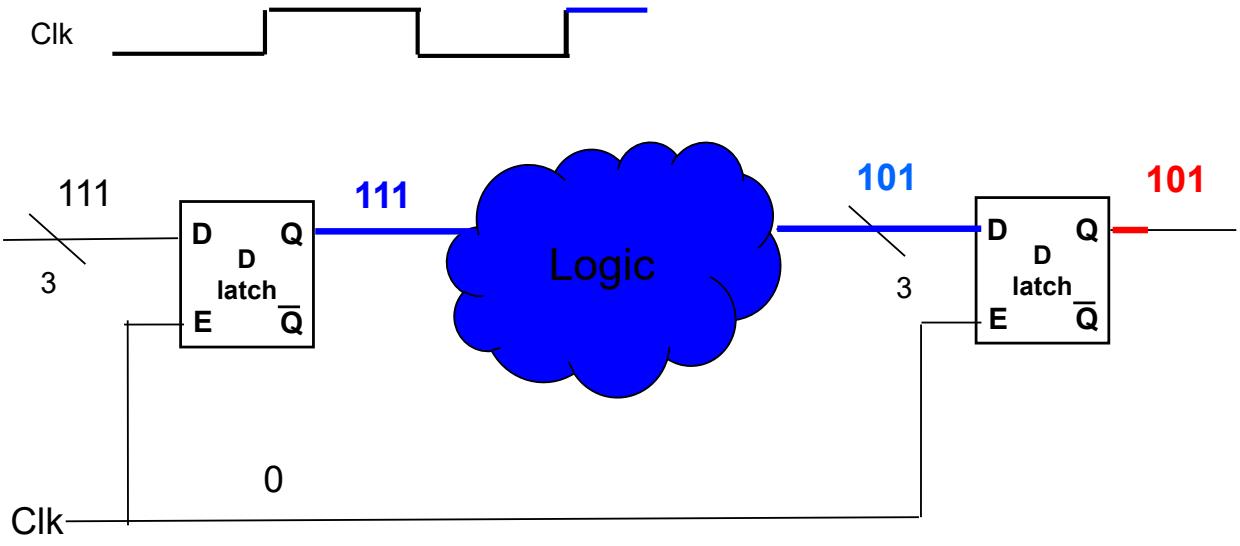
- Problem: What if signal reaches latch too early?
  - I.e., while clk is still high



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

Strawman: Level Triggered

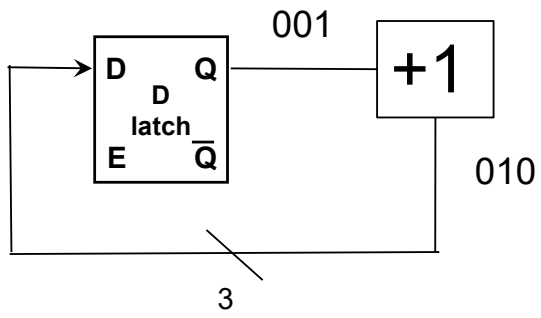
- Problem: What if signal reaches latch too early?
  - Signal goes right through latch, into next stage..



This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

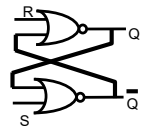
That would be bad…

- Getting into a stage too early is bad
  - Something else is going on there → corrupted
  - Also may be a loop with one latch
- Consider incrementing counter (or PC)
  - Too fast: increment twice?



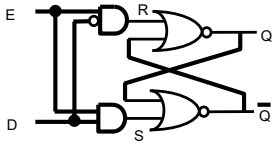
This slide describes how D-latches can malfunction because they were level triggered. Real D-flip-flops are *edge-triggered*, and we're showing you ***why*** that's important.

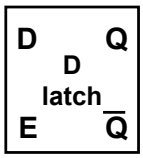
Building up to the D Flip-Flop and beyond



SR Latch

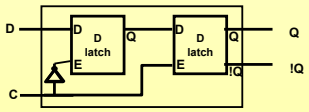
(too awkward)

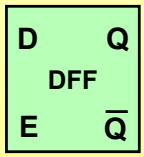




D Latch

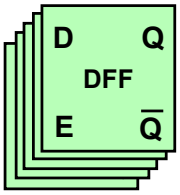
(bad timing)

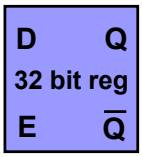




D Flip-Flop

(okay but only one bit)





Register

(*nice!*)

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Summary

Can layout logic to compute things

- Add, subtract,…

Now can store things

- SR latch
- D latch

Also understand clocks