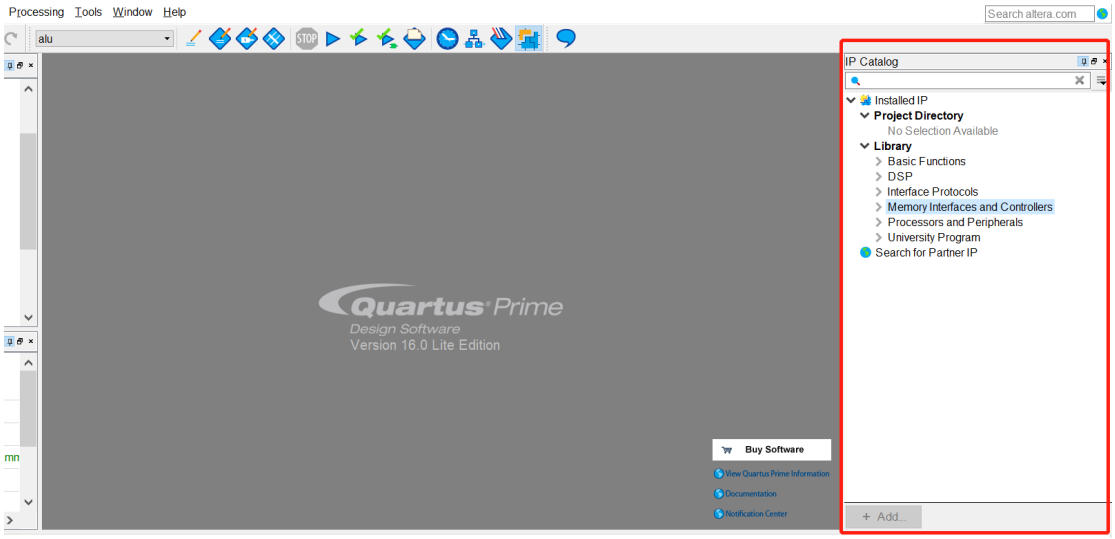
Hints for using IP core to generate memory components

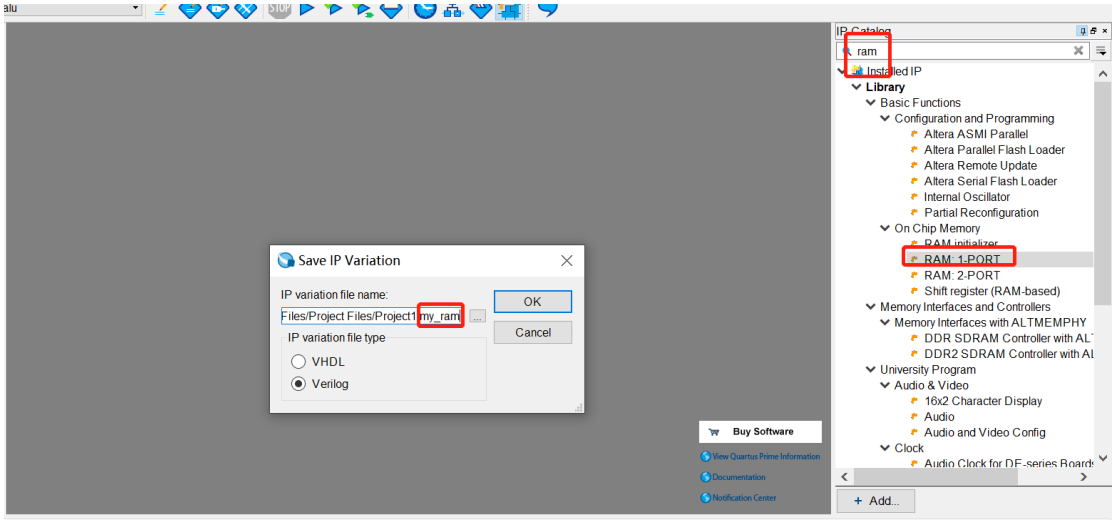
There is a handy way to design your circuit easily and fast is to introduce IP core: a predesigned library for you to use, just like calling `printf` which resides in libc in your C program.

You can click Tools -> IP Catalog to display the window for configuration. It is something shown below:

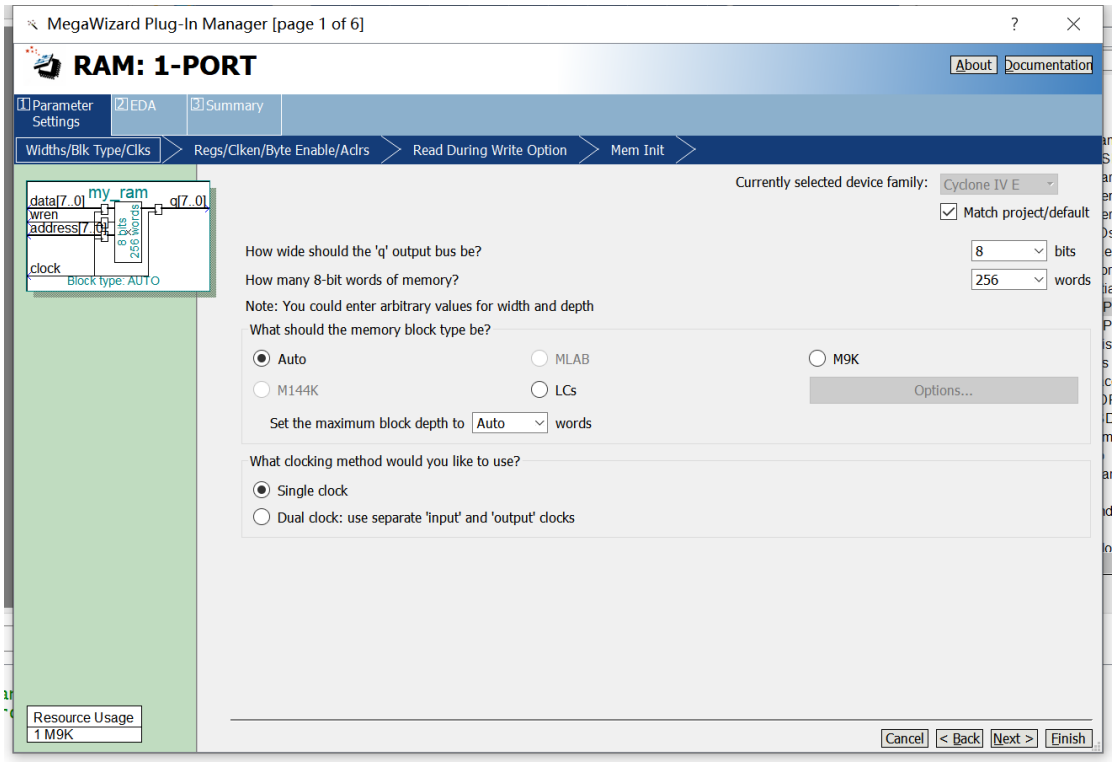



You can search the IP core you want by filling in the blank next to the magnificent lens icon.

For example, if I would like to use a 1-port RAM (this maybe not the component you will use in your project, just for demonstration purpose), I will simply type RAM in the blank and double click the exact component I would like to use just shown as below.

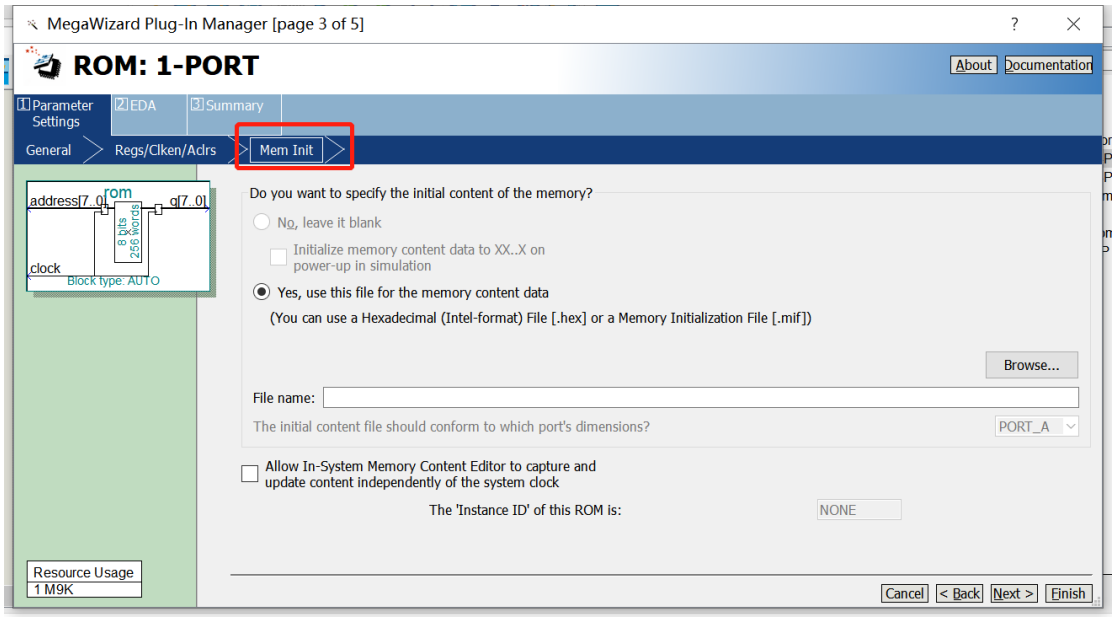



After clicking OK, the configuration window will prompt, just like below




After tailoring the component's parameters to what you need, you can click finish you create the component. The EDA software, specifically quartus in our project, will generate a Verilog file to realize the component with parameters defined by you. After that, you can instantiate the memory module generated by the software and connect it to your circuit to use this component, just like any regular module you defined.

To be noted, RAM is Read-Write and ROM is read-only, you may need to predefine the memory content on the parameters configuration window if you would like to use ROM.




Please refer to [this page] if you would like to get further information on what the parameters

mean for the memory components.