Final Project

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ECE485

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Introduction

This report contains initial information regarding the final project

Initial Estimates

1. Unit cost: 80
   (a) Memory consists of M1 x 1, M3 x 10
   (b) Memory capacity is 10.2 kB
   (c) Best case/worst case memory latency is 1 clock cycles / 15 clock cycles
2. Communication cost: .95 dollars
3. Cumulative latency: 2976 clock cycles

Task list

1. Initial design of architecture (Will, Ahmed)
   (a) Make design decisions on the types of memory to use and how to implement
   (b) Document design decisions
2. Program initial simulation (Will)
   (a) Program initial simulation in python using MyHDL
   (b) Document tool chain (MyHDL, other python libraries needed to run simulation)

(c) Provide ample documentation on use and implementation

3. Debug and test initial simulation (Will, Ahmed)
   (a) Use initial traffic file in simulation
   (b) Generate waveforms with test bench
   (c) Verify that simulation performs as expected
   (d) Eliminate any bugs as needed
   (e) Document performance
4. Design review (Will, Ahmed)
   (a) Go over the performance of the design in the simulation
   (b) Discuss possible changes regarding design
   (c) Document any decisions and/or pending changes
5. Implement final changes (Will, Ahmed)
6. Complete documentation (Ahmed)

Project Timeline ✓= complete by

Milestone	Nov 18	Nov 22	Nov 25	Nov 27	Nov 29	Nov 30	Dec 1
Initial design of arch.	✓						
Initial simulation		✓					
Debug and test initial sim.			✓				
Design review				✓			
Implement final changes					✓		
Complete documentation						✓	
Final test and completion							✓