Development of a Low-Cost and Open Source CubeSat Command, Control and Communications System

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The Portland State Aerospace Society (PSAS) is a student aerospace engineering group at Portland State University (PSU) dedicated to building low-cost, open-source sounding rockets that feature some of the most sophisticated amateur rocket avionics systems in the world.[1] In 2015, PSAS created the Oregon Small Satellite Project whose goal is to build and fly "OreSat", Oregon's first educational "CubeSat" nanosatellite.[2] OreSat's most mission critical system is its Command, Control, and Communications (C3) module. This module, code-named "Sputnik" because of its requirement to be a simple, reliable space system, is a system of two printed circuit boards connected via a standard backplane. One board is responsible for long distance communications, and the other for executing and conveying mission critical commands as well as monitoring and controlling power distribution to the rest of the CubeSat. This system was designed, developed, manufactured and successfully tested within a 20 week time frame for less than the proposed $1000 USD budget.

Nomenclature

This section contains definitions for acronyms used in this report.

$PSAS$	Portland State Aerospace Society
PSU	Portland State University
LGR	Low Gain Radio
SC	System Controller
SEU	Single Event Upset
PA	Power Amplifier
LNA	Low Noise Amplifier
LID	PSU Lab for Interconnected Devices
MCU	Microcontroller
OTS	Off The Shelf
$COTS$	Commercial Off The Shelf
$kw0x$	NXP MKW01Z128 microcontroller
Tx/Rx	Transmit/Receive
IMU	Inertial Measurement Unit
DNP	Do Not Populate
DOF	Degree(s) of Freedom
USD	U.S. Dollars

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I. Introduction

I.A. PSAS

The Portland State Aerospace Society (PSAS) is an open source student aerospace engineering group at Portland State University (PSU) that has been launching and developing amateur rockets since 1998.[1,3]

Their most recent launch (*July, 2015*) featured a 3.4m sounding rocket capable of a 5 km apogee and low supersonic velocities. This flight demonstrated operation of a Linux-based flight computer running a Software Defined Radio (SDR) GPS receiver, 1-DOF Roll Control using canard control surfaces, full 9 degrees of freedom IMU data, a Raspberry Pi camera feed, with data downlinked to the ground in real time using a custom-built long distance WiFi telemetry system.

I.B. OreSat

Oresat was established in 2015 by PSAS, along with partners at other Oregon universities, with the goal of building and launching Oregon's first educational satellite. It represents Oregon's first participation in the Educational Launch of Nanosatellites (ELaNa), part of Nasa's CubeSat Launch Initiative (CSLI).[a]

A "CubeSat" is a standard nanosatellite form factor originally developed at Cal Poly for use in educational space projects. This new form factor – a series of 10 cm cubes with a maximum weight of 1.33 kg per cube – has now also become a standard in new commercial space applications including satellite constellations for Earth observation.

I.C. Project Background

An essential piece of any CubeSat is a module that has the ability to monitor system health and rectify issues, while also being able to communicate information to/from earth. These capabilities are collectively referred to as C3, which stands for Command, Control, and Communications.

These terms are defined more precisely as follows:[4]

Command: The exercise of authority based upon certain knowledge to attain an objective.

Control: The process of verifying and correcting activity such that the objective or goal of command is accomplished.

Communications: The ability to exercise the necessary liaison to exercise effective command between tactical or strategic units to command.

OreSat's need for a C3 module resulted in PSAS sponsoring a 20 week long PSU ECE senior capstone project to develop a prototype with these capabilities. This module must perform these most essential tasks of the CubeSat reliably in a high radiation environment over a wide temperature range. Radiation is one of the top concerns in space and can be particularly harmful to digital components, creating what are called "Single-event upsets" (SEUs). Radiation hardened (rad-hard) parts can be expensive, so it is preferable to use over the shelf (OTS) parts when possible. In order to get around the effects of radiation, the design approach for this project had to involve designing a rad-hard portion of hardware with a rad-hard micro-controller to power-cycle other modules on the CubeSat when they experience SEUs.

Another goal of this project was to contribute to the open-source hardware and software community. As such all project information is made available on the Github collaboration site under the GNU General Public License Version 2 open source license.[b,c]

II. Design

II.A. Requirements

The requirements for the Sputnik system are:

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[a]http://www.nasa.gov/content/about-cubesat-launch-initiative
[b]https://github.com/oresat/low-gain-radio
[c]https://github.com/oresat/system-controller

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- Must

  - Environment

    * Use parts rated in an Industrial Operating Temperature Range ($-40°$C to $80°$C)

  - Communication system

    * Meet FCC Amateur Radio Licensing requirements (Title 47 CFR part 97)[5]
    * Use IARU specified frequency for spacecraft RF communications
    * Operate in the 70 cm band (436 to 438 MHz)
    * Meet 400 km LEO link budget
    * Local storage for communication in/out queues

  - System controller

    * Radiation tolerant "system watchdog" controller
    * Power switches to turn other modules on and off
    * Communicate with communication system

  - CubeSat requirements

    * System conforms to latest CubeSat specification
    * System fits in 0.25 of a 1U CubeSat
    * System weighs less than 250 g

- Should

  - Construction

    * Use as many COTS (Commercial Off The Shelf) parts as possible

  - Environment

    * Operate in the Automotive Operating Temperature Range ($-40°$C to $125°$C)
    * Be able to operate in a vacuum
    * Handle 15 g acceleration in the "Z" axis

  - Communication system

    * Use a frequency of 436.5 MHz for RF communication

- May

  - Environment

    * Operate in Military Operating Temperature Range ($-55°$C to $125°$C)

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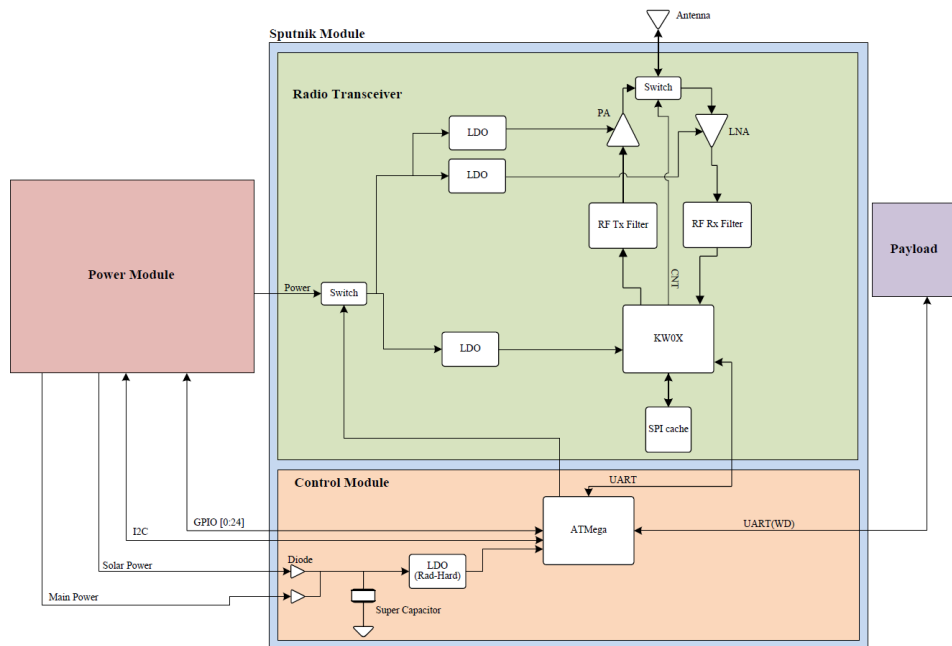
II.B. System Level Design

Figure 1. System Level Design of Sputnik. Only the portion surrounded in blue pertains to the project. The Power Module and Payload are other modules within the CubeSat system.

The Sputnik module is split up into two separate sub-modules: the radio transceiver module, or Low Gain Radio (LGR), and a control module, or System Controller (SC).

The LGR is based on a combined microcontroller and sub-GHz radio chip, the NXP MKW01Z128 microcontroller (nicknamed the "kw0x"). The LGR also has two bandpass filters, AC blocking network, a Low-Noise Amplifier (LNA), and a Power Amplifier (PA). It is capable of transmitting 1 W (30 dBm) for long distance communication and because of its low gain, capable of communicating regardless of the satellite's orientation. Other than the crystals (which will be swept for radiation protection), the final revision of the LGR will use COTS parts for decreased costs.

The SC is a watchdog responsible for detecting SEUs and rebooting subsystems. It is connected to the Power module via I2C and to the Payload via UART. A super capacitor provides charge to the MCU during a power cycle of the power module so that it can remain operational. COTS parts that have analogous radiation hardened parts were chosen to reduce prototyping and non-flight unit build costs. The power module and primary mission payload are their own separate modules outside the scope of this project. It is assumed that they comply with the defined interfaces.

A budget of $1,000 USD was granted from PSAS to ensure low cost prototyping. It was estimated that three boards for each module would allow for thorough testing while still falling under the budget restraint. Consequently, rad-hard parts were not used for the prototype as they can be as much as $1,000 per component.

II.C. Isolation

Galvanic isolation is used between the SC and other modules in order to secure the power domain of the SC, preventing shorts and other malfunctions that could incapacitate the SC. High-speed digital output opto-isolators were used on the UART lines between the SC and the LGR, and between the SC and the payload module. Furthermore, to ensure the success of the watchdog and to simplify design, the LGR and

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SC were separated into two different printed circuit boards.
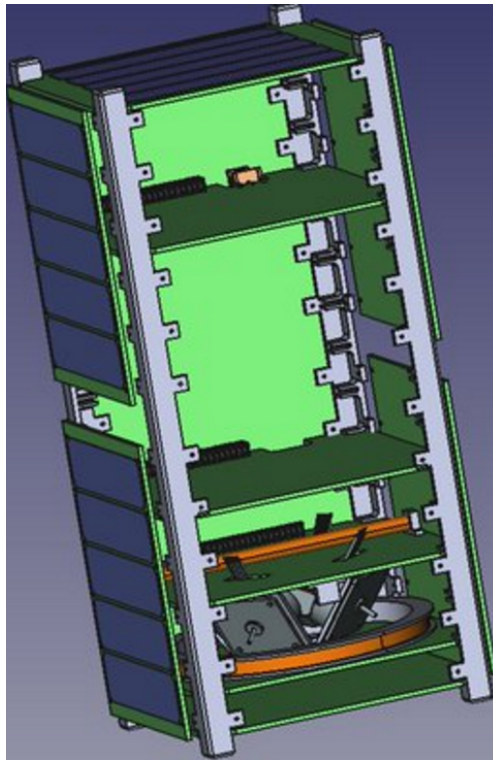
II.D. Form Factor

Figure 2. PSAS CubeSat CAD Model. Note the shelf like structure where different modules can be slid into the satellite.

Figure 2 shows the CAD model developed by PSAS for the CubeSat. Each module is a printed circuit board that slides into a card slot and connects to a common back plane.

II.E. Part Selection

In general, COTS parts were selected whenever possible based on three main criteria: required functionality, availability, and cost. However, parts for the system controller had a further constraint: the availability of a radiation hardened analogue, since this system was critical to mission success. According to the power module specifications given by PSAS, all parts needed to be able to be powered by a voltage rail from 3-5 V although LDOs were used for many parts that needed a consistent supply voltage. An example COTS part selection was the PA (Skyworks SKY65116-21) with an output of at least 30 dBm that could be powered within this voltage range. The LNA (MACOM's MAAL-010704) is another example COTS part that could operate within this range. However, there were not many LNAs that could meet the needed noise factor of less than 0.7 dB at 436.5 MHz. In fact, for this project, the LNA only has this ability at temperatures below $0°C$, meaning a better LNA will be necessary for future revisions.

Once functionality and availability were confirmed, cost was the next deciding factor. Radiation hardened parts are necessary for the System Controller since it is a mission critical system. Since radiation hardened parts are also particularly expensive, COTS analogues when found were bought for testing purposes. Though functionality is similar, the unique footprints of many rad-hard parts will require that the board layout be modified during later development stages.

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The bill of materials for the respective boards,[d,e] as well as list of parts used and specific reasons for these choices, can also be found on the project's Github repository.[f,g]

III.   Development

III.A.   Prototyping

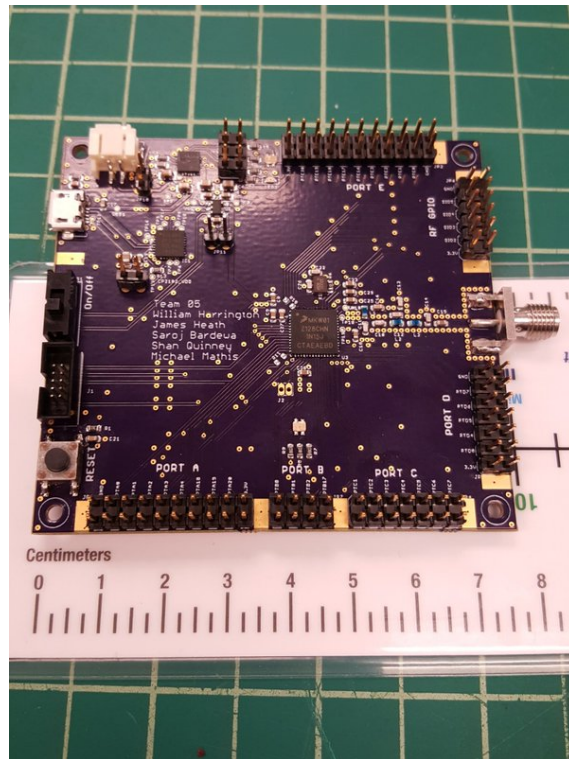**MCU Breakout Board**

Figure 3. kw0x breakout board prototype. Measured to fit within the 10 cm confines of a Cubesat at around 8 cm x 8 cm.

A breakout board was produced for the microcontroller that was used on the LGR (NXP's MKW01Z128, also sometimes referred to as kw0x). The purpose of this was to create a platform for firmware development and further hardware development. As such, the design was aimed at maximizing accessibility to all the features of the kw0x and providing the supporting hardware. Ease of use was also considered in its design, emulating Arduino architecture when it came to the pin-out design. A simple monopole whip antenna and bandpass filter were developed for this board and were used to accommodate RF communications in the 70cm (420 MHz - 450 Mhz) band. The basic supporting hardware included a battery charging connector, battery charger management unit, an LDO, and a UART to USB chip for easily debugging messages. Lithium Polymer batteries were also included to enable mobile use.

A development board for the kw0x was available at the time, but this board was deemed unacceptable due to expense constraints, that it did not allow for Rx/Tx in the 70cm band, and did not fit the project's design criteria. No such breakout board was produced for the microcontroller used on the SysCon (ATMega128). Instead, an ATMega128 development board was purchased to be a platform for firmware development and hardware development.

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[d]https://github.com/oresat/system-controller/blob/master/docs/BOM_SC.xls
[e]https://github.com/oresat/low-gain-radio/blob/v1_2/docs/low-gain-radio_BOM.xlsx
[f]https://github.com/oresat/low-gain-radio/blob/master/docs/Parts_Selection.md#parts-selection-for-low-gain-radio
[g]https://github.com/oresat/system-controller/blob/master/docs/PartsSelection.md#parts-selection-for-system-controller

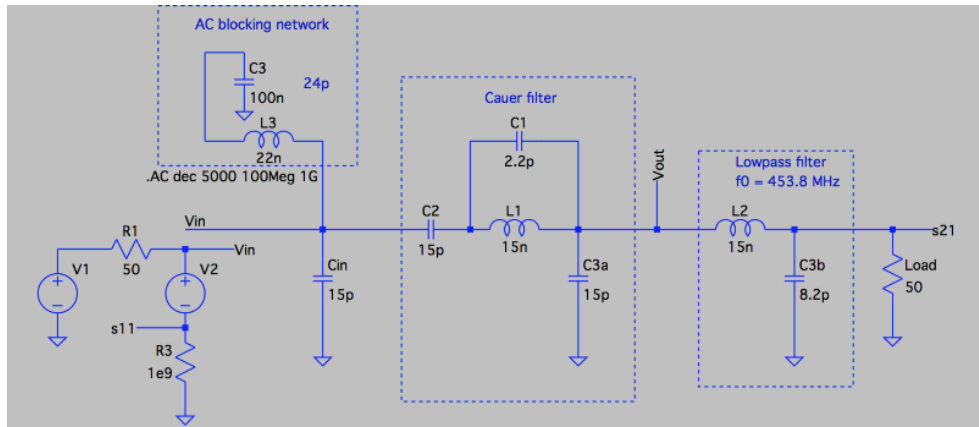American Institute of Aeronautics and Astronautics

Radio Filter

Figure 4. LTSpice model of suggested Cauer bandpass filter from the MKW01X128 datasheet.

A bandpass filter was required for the front-end of the kw0x transceiver in order to enable communication in the 70cm band. Since both receiving (Rx) and transmitting (Tx) involved the same channel width, the same filter was used on both Tx and Rx paths between the antenna and the transceiver. The original design of the filter was taken from the suggested Cauer Filter in the MKW01Z128's datasheet and is shown modeled in LTSpice in Figure 4 above.[6]

Figure 5. LTSpice simulation results. The first marker shows losses at 436.5 MHz at -246.7 mdB. The second marker shows -74.5 dB at the second harmonic (873 MHz) satisfying FCC regulations.

The simulated results using LTSpice are seen in Figure 5. The filter showed acceptable losses at the desired frequency of 436.5 MHz, only losing roughly 250 mdB. More importantly, the second harmonic showed a simulated drop to around -74.5 dB satisfying the FCC requirement being well below -40 dB of the transmitted signal.
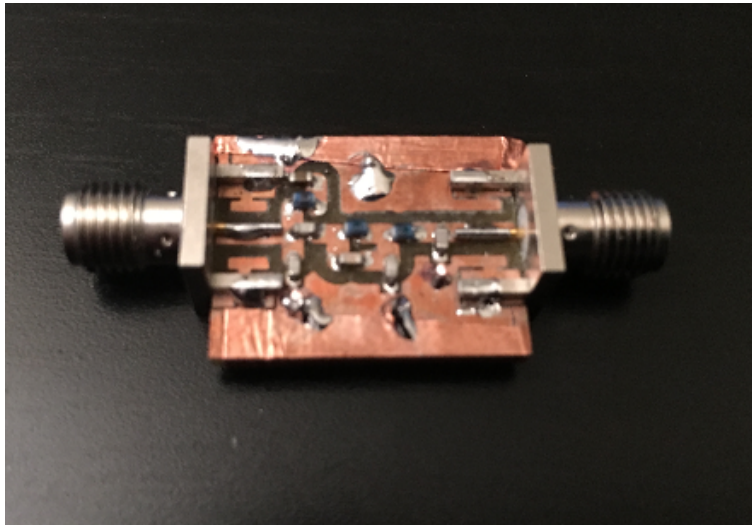
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Figure 6. An example of a proto-board built for measuring the front-end filter with a Vector Network Analyzer (VNA).

Once the simulation was finished, the filter was then rapidly prototyped for testing. Figure 6 is an example of one of the finished proto-boards created in the Portland State Lab for Interconnected Devices (LID).[h] Figure 7 below shows the tested results of this board on a VNA.
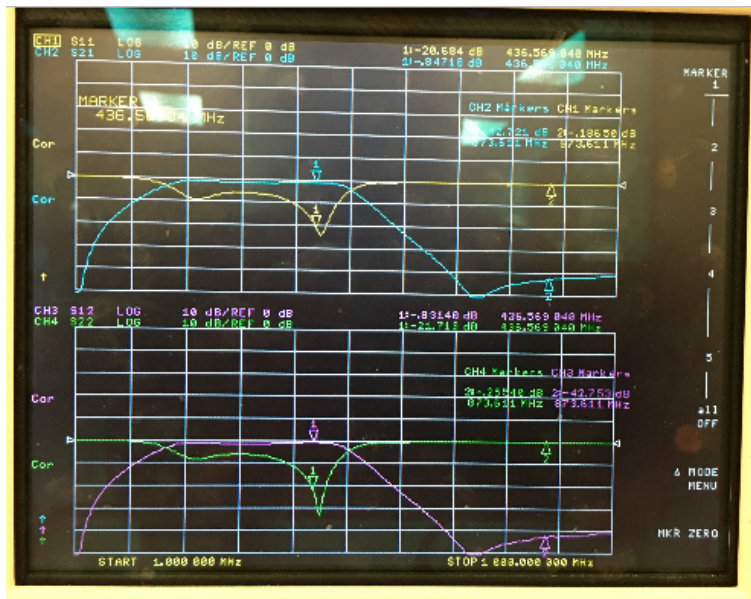

Figure 7. The S-parameters of the proto-board signal on a VNA. The blue line (S_{21}) shows a loss of -0.847 dB at 436.5 MHz and -42.75 dB at the 2nd harmonic 873 MHz.

The empirical results differed from those simulated. At the passband, the S_{21} measurement (the blue line in figure) shows roughly a -850 mdB loss as opposed to the simulated -250 mdB. Also, the 2nd harmonic rose from the simulated -74.5 dB to around -42 dB, however this still satisfied the FCC regulations requirement of being -40 dB less than the transmitted signal. Since this design satisfied the requirements, this filter was implemented in the hardware for the kw0x breakout board and the LGR.

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[h]https://psu-epl.github.io/

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III.B.   Schematic/PCB

This section focuses on the schematic and layout design choices made for this project starting with the LGR and then following with the SC.

III.B.1.   LGR Parts/Schematic

The majority of the schematic designs for the LGR came from the manufacturers suggested applications found within their datasheets. Since the schematic resolution is large, it was broken down into several portions to fit within this report. Each section is explained individually. The datasheets for all the parts used are located on the Github repository for this project.[i]

Figure 8. LGR MCU schematic. Blue lines are buses to the SPI cache and the forty pin connector to the back plane.

One of the critical components of this module, which is responsible for communication, is the MKW01Z128, a NXP microcontroller with an integrated transceiver and basic radio infrastructure. The radio infrastructure consists of a bandpass filter, AC blocking network, a Low-Noise Amplifier, and a Power Amplifier. The output of the RF circuitry will be expecting a 50Ω impedance for its load. It is connected to the SC's MCU and the payload via UART.

The LGR's MCU schematic is shown in Figure 8. In the bottom right of the figure there is a JTAG header for programming the chip. In Figure 9 below, blue bus lines carrying multiple pins to a forty pin-out back plane attachment, as well as a debugging port for testing. As many pins as possible were used on the MCU for the purpose of debugging or in the case of the addition of features.

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[i]https://github.com/oresat/low-gain-radio/blob/master/docs/Parts_Selection.md#parts-selection-for-low-gain-radio
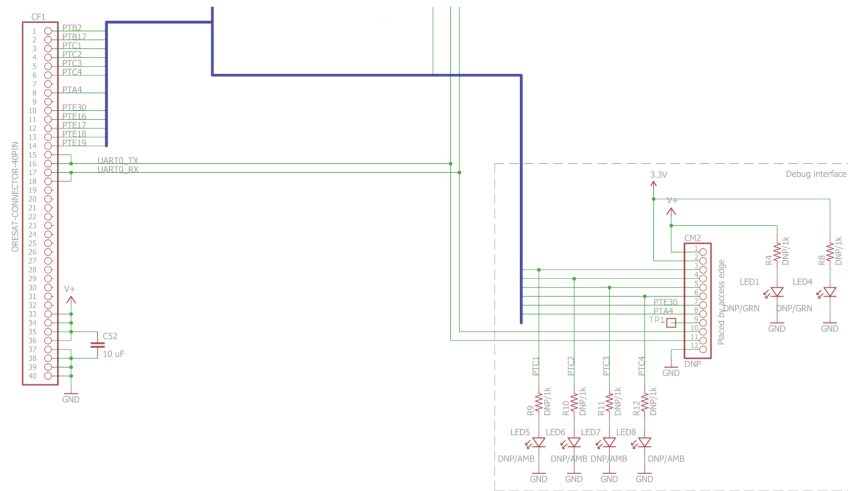
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Figure 9. Forty pin connector and debug pinout Schematic. LEDs were attached to the GPIO lines to note when data is sent or received for debugging purposes.
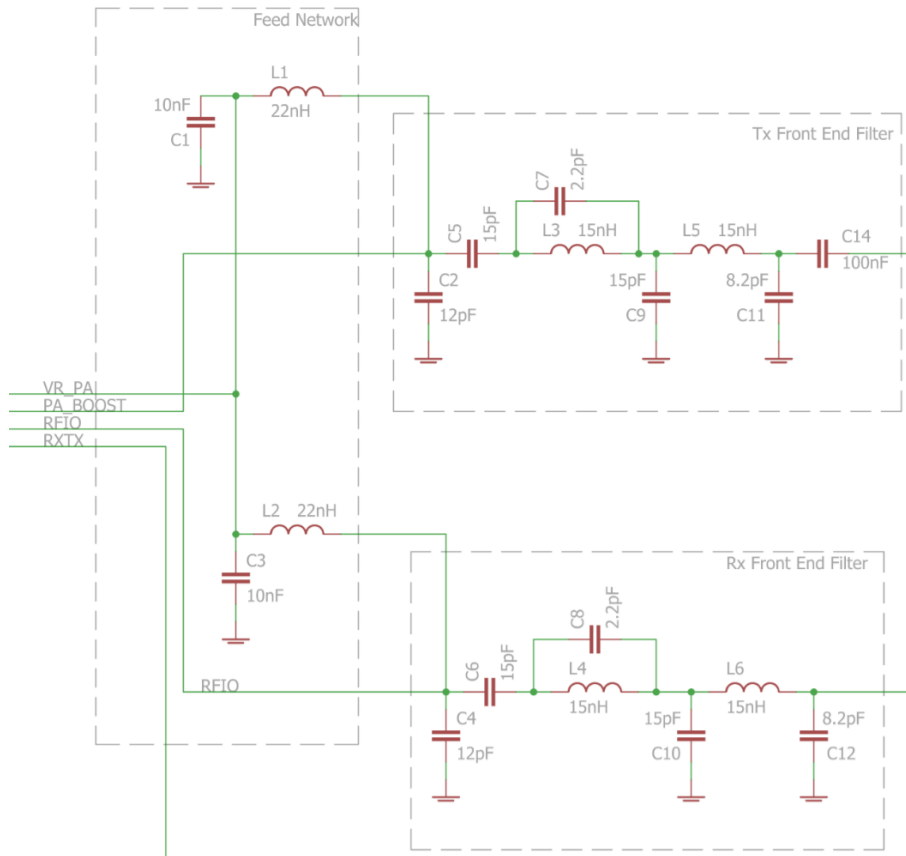

Figure 10. Bidirectional filter Schematic for both Rx and Tx lines. The PA_BOOST line comes from an amplifier within the kw0x that is set to 0 dB to prevent damage to the PA input.

Figure 10 show the implementation of the bandpass filter for the LGR transceiver. For more information on the filter, see Radio Filter in section III.A.
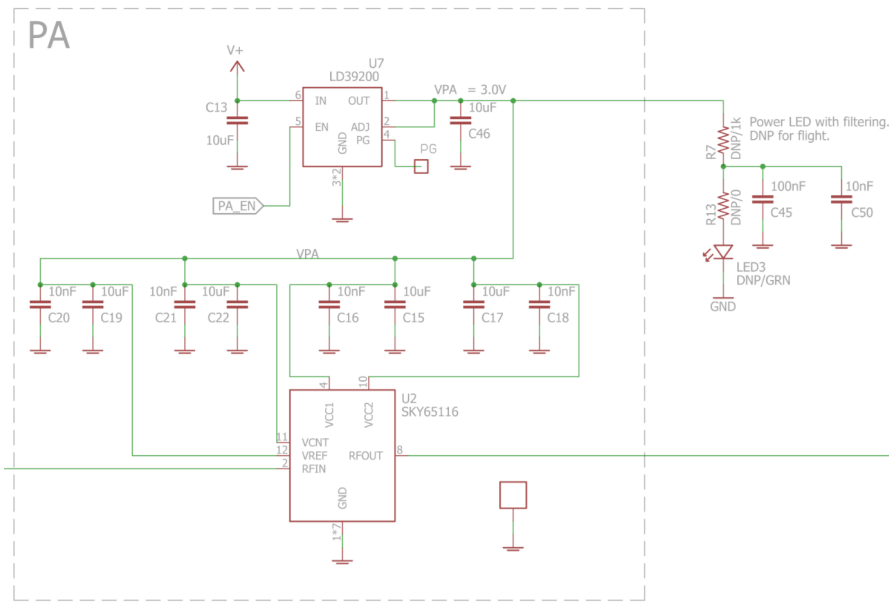
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Figure 11. Schematic of the Power Amplifier and its LDO. Component values were taken straight from their respective datasheets.[7]

The PA schematic for the Tx line is shown in Figure 11. This PA was chosen because it could meet the output power requirement of 1 Watt (30dBm). It also had low enough voltage rails that it could be powered without using extra parts such as a buck-converter. Because of the low voltage requirement, the current draw of the PA was higher than others, around 1 to 1.3 A. Since the PA requires so much amperage, it was decided that it needed a dedicated LDO to deliver a consistent power supply voltage; a consistent power supply voltage for the PA ensures a consistent current draw. An LED is attached to the enable line of the PA for debugging purposes and is DNP for flight.
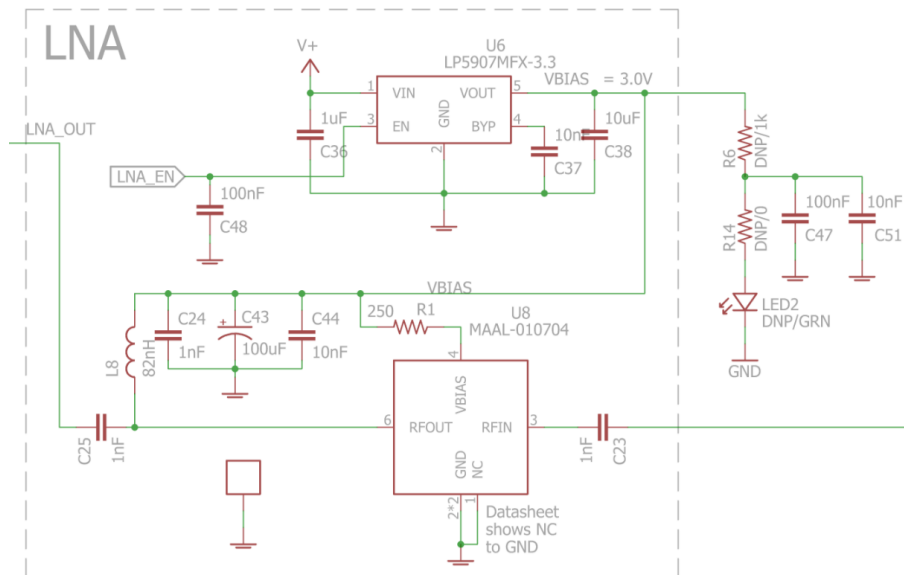

Figure 12. LNA and its LDO schematic. The LDO used here is the same type as used for the MCU since they require the same amount of voltage and circuitry. Also to decrease cost of parts when buying in bulk.

The LNA schematic is shown in Figure 12. Choosing an LNA for the project ended up being difficult, as few LNAs could handle the requirements asked for by the projects link budget of 400 km. This was mostly due to needing a 0.7 dB noise factor at the desired frequency. Originally, Hittite's HMC616LP3 was

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a promising solution boasting a <0.7 dB noise factor across temperatures from -40°C to 85°C. However, this product was too difficult to source after Hittite was purchased by Analog devices and the resources available to the project. The second choice was MACOM's MAAL-010704. Since the Hittite chip was no longer in production, this was the chip used for this revision. While the MAAL-010704 met the noise figure requirement, it was only at lower temperatures below 0C, meaning there will be heavier losses at the higher temperature values in space. Therefore, while satisfying a portion of the requirements for this project, the LNA will likely need to be replaced in future revisions.

The design for this portion of the project was taken from MAACOM's suggested orientation in the LNA datasheet.[8] The values for the components in particular were decided based off the IDQ vs Rbias graphs in the datasheet. To make sure to meet the desired noise figure at -40°C according to these graphs, a combination of values giving an IDQ value around 30 to 60 mA was desired. The LDO above was needed to keep the LNA from receiving fluctuating input values, as this could alter the noise figure through current changes. To the right, another LED was attached to the enable line of the LNA for debugging purposes.
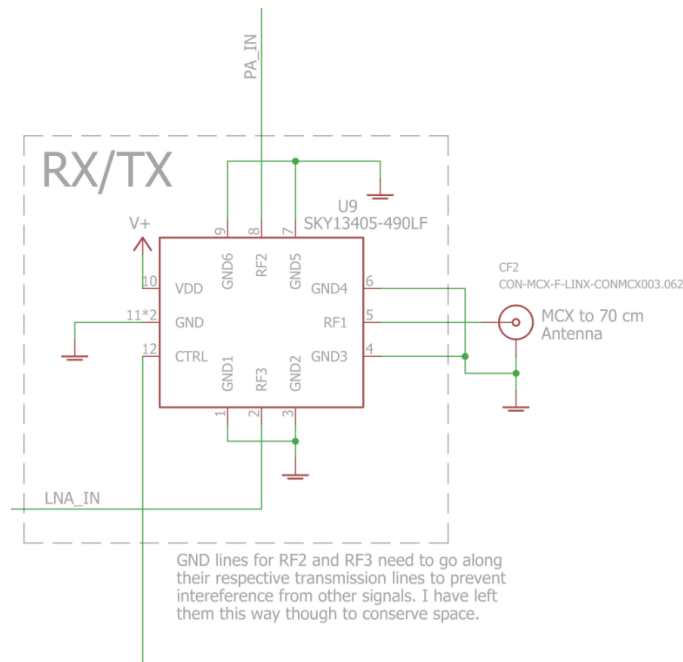

Figure 13. RF Switch Schematic. The CTRL line comes from an inverter that isn't shown to reduce diagram complexity. An MCX connector is used for connection to the satellite's antenna.

In Figure 13, the schematic for the RF Switch is shown. An RF Switch was necessary for the project since there were separate Tx and Rx lines leading to the same antenna. Skywork's SKY_13405490F was the part chosen for the RF Switch. Skywork's products have proved efficient for RF circuitry for other parts, so the switch was chosen based on the manufacturer's reliability. The switch also had low insertion loss (0.3 dB) and a relatively small footprint.

An oversight to this choice was the footprint topography of the RF Switch happened to be reverse that of the kw0x MCU's Tx and Rx pins. This means an inverter was required on the control line to allow for proper usage of the switch. Since this took up more board space and added complexity to the circuitry, a replacement was found for the next revision of the board. This replacement part was Peregrine-Semiconductor's PE42723A-Z, which has proper layout topography for the board. It also has lower insertion loss and similar footprint making replacement easy.

The circuit topography was taken from the suggested application from Skyworks' datasheet.[9] The RF Switch design however came with complications. Since the topography of the switch ended up being reverse of what was desired, an inverter (not shown) had to be used on the control (CTRL) line of the switch. In

future revisions, this RF Switch should be replaced to save on parts and complexity.

Below in Figure 14 is Winbond's W25Q80DVSNIG 8MB SPI cache for future implementation of a boot loader for the LGR. The setup was taken from the datasheet for the chip.[10] Though the SPI Cache placement was included in this revision of the board, programming and testing the SPI Cache itself was outside of the boundaries of this project.
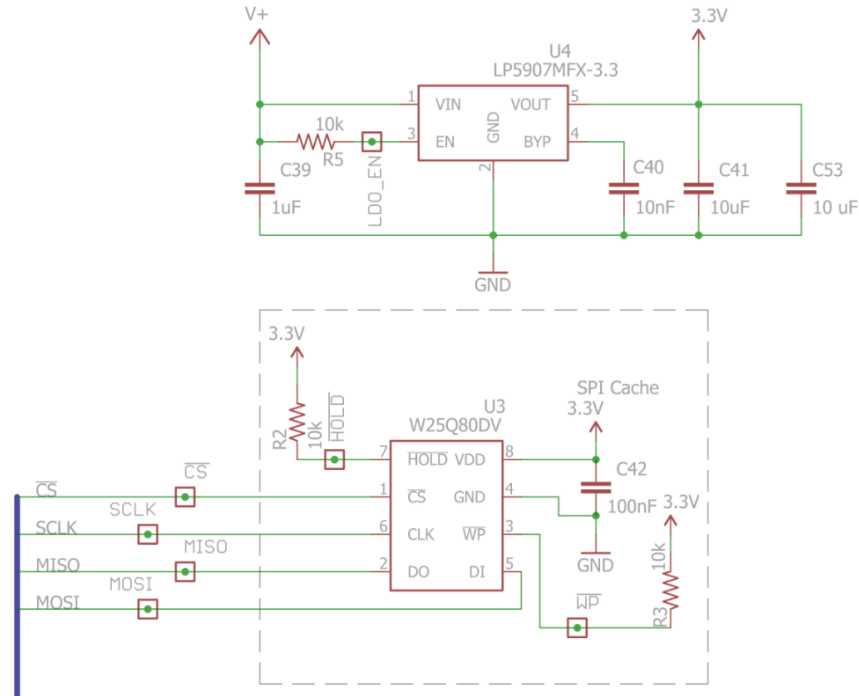

Figure 14. SPI Cache and MCU LDO schematic. 10 kΩ resistors are used as pullup resistors to prevent floating pins. LDO setup is the same as that for the LNA.

III.B.2.   SC Parts/Schematic

As noted in the Low Gain Radio section, all parts chosen for this project and their datasheets can be found on the Github repository.[j]
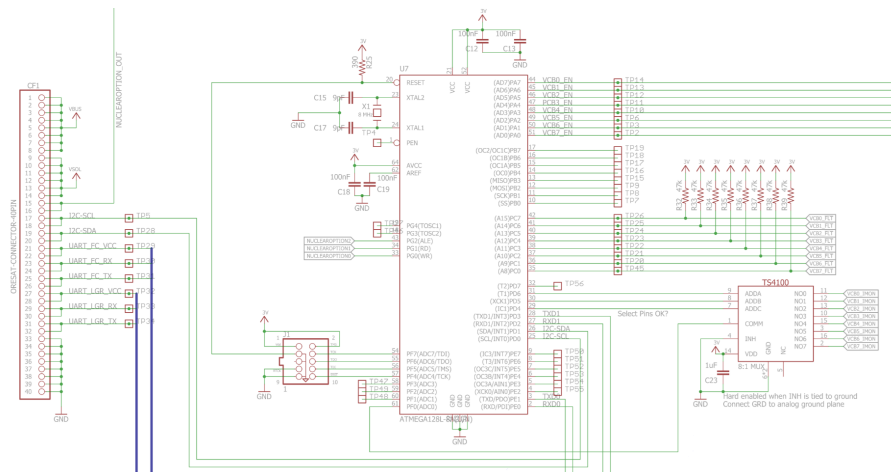

Figure 15. Schematic for SC's MCU, Atmel's ATMega128. An 8 to 1 MUX is used for containing the information from the 8 Efuses into one pin.

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[j]https://github.com/oresat/system-controller/blob/master/docs/PartsSelection.md#parts-selection-for-system-controller

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The SC's most important component is Atmel's ATMega128. The largest contributing factor for this choice was the chip's space-rated counterpart, the ATMegaS128. Functionality between both models is the same, allowing testing on less expensive OTS parts before investing in the space-rated hardware. It also has an easy development platform in Arduino and is reliable for simple tasks.

Figure 15 shows the schematic design for the ATMega128. Almost every pin on the MCU has a test point for debugging. There is also a JTAG for programming and an 8 to 1 MUX needed for current reading from the eight Efuses. On the left side of the schematic, one of the forty pin connectors for the back plane can be seen as well with the UART Tx and Rx lines going to both the payload and LGR.
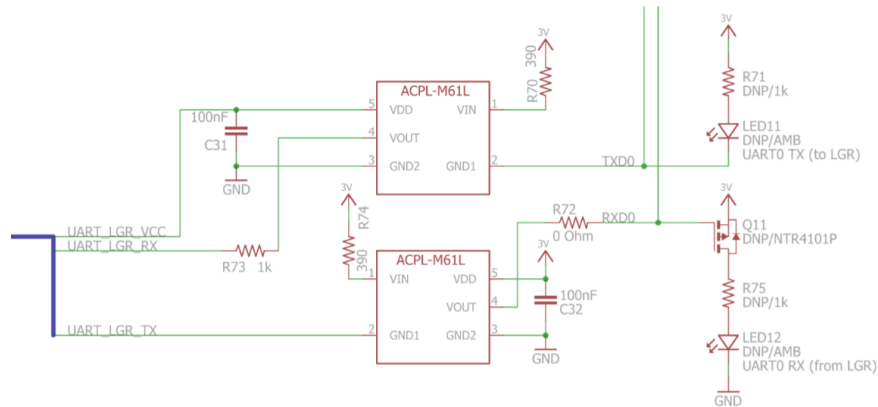

Figure 16. Opto-isolator Schematic. The LED setups allow the user to see when UART data is being transmitted and received.

In Figure 16, the design for the opto-isolators on the UART lines to the LGR are shown. Not shown are two more identical UART lines to the payload in order to simplify the diagram. These isolators are necessary to ensure that failures in other systems would not directly effect the SC's operation due to shorts or other possibly electrical failures from SEUs. As stated under Parts Selection, this chip was selected due to the relatively low circuit complexity.

Broadcom Limited's ACPL-M61L-000E ICs were chosen mainly for their relatively simple circuitry. The chip can be powered from a 3.0 V supply and features a low 1.6 mA input current. The temperature range also exceeds requirements on the high end (-40°C to 105°C). Note that the output is inverted to prevent the LEDs from being permanently on.
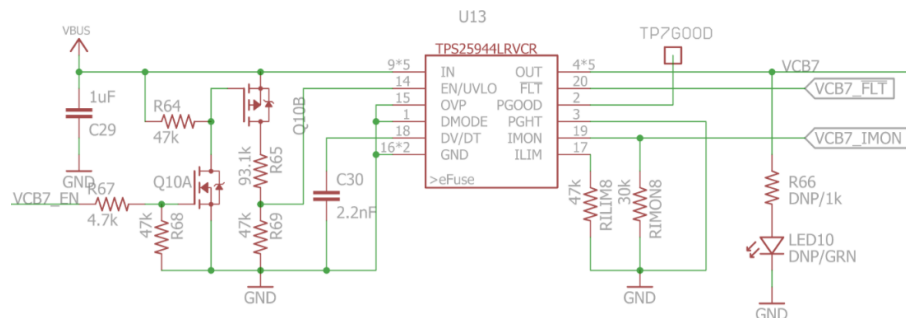

Figure 17. Efuse Schematic. The transistors on the left portion help separate the voltage domains of the supply bus and the enable line.

The Efuse circuitry is shown in Figure 17. LEDs are attached to all the Efuses on the board to debug and indicate that Efuses are receiving power. Texas Instrument's TPS25944LRVCR IC offered the most complete solution compared to the competition. The chip can be powered from a 3.0 V supply (has an operating voltage range of 2.7 V to 18 V). It has a current limiting feature, which is set by an external

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resistor. It allows for current monitoring, undervoltage protection, overvoltage protection, and the slew rate is adjustable by use of an external capacitor.

VCB_EN is an enable line from the MCU to the fuse for activation and deactivation. The $\overline{FLT}$ (Fault) output from the fuse will trigger if the EFuse trips due to a failure in its attached system. If this happens, the resistor on RILIM line sets the current and The VCB_IMON line sets the gain for the current monitor which feeds into the 8 to 1 MUX leading to the MCU for current readings in the case of a short.
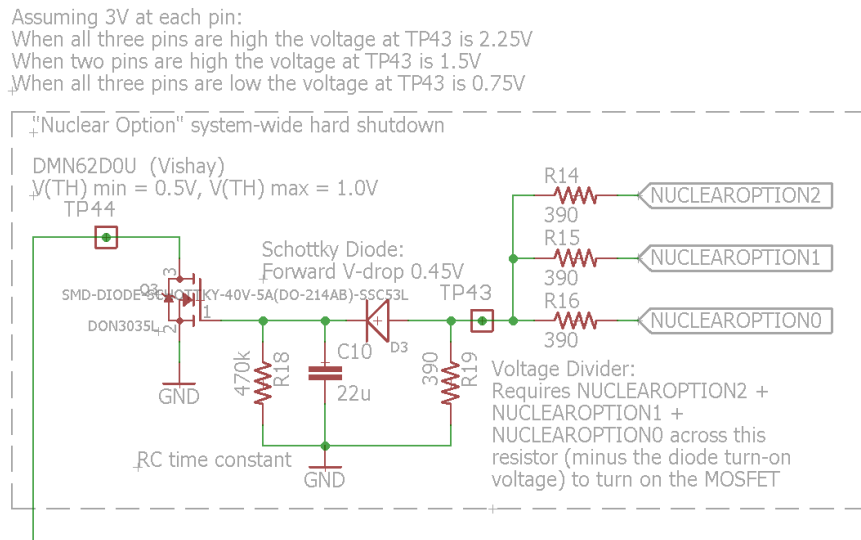

Figure 18. "Nuclear option" portion of the schematic. When Nuclear options 1, 2, and 3 go high, then the entire Cubesat is reset with the except of the SC which is powered by a 220 mF Super-Cap.

The final main portion of the System Controller schematic is a system hard shutdown option, nicknamed the "nuclear option," in Figure 18. This option is used when the Cubesat is under the highest levels of malfunction due to catastrophic events or failures necessitating a complete reset. When performing a full reset, the three lines on the right portion of the figure will pull high and turn on the MOSFET transistor on the left portion of the figure through voltage division. This line will lead to the Power Management System and shut down the power to the entire satellite. The exception to this is the System Controller itself, which will be powered via a 220 mF super-capacitor to reset the system for roughly 25 to 50 seconds, depending on the voltage level from the power rail at the time.

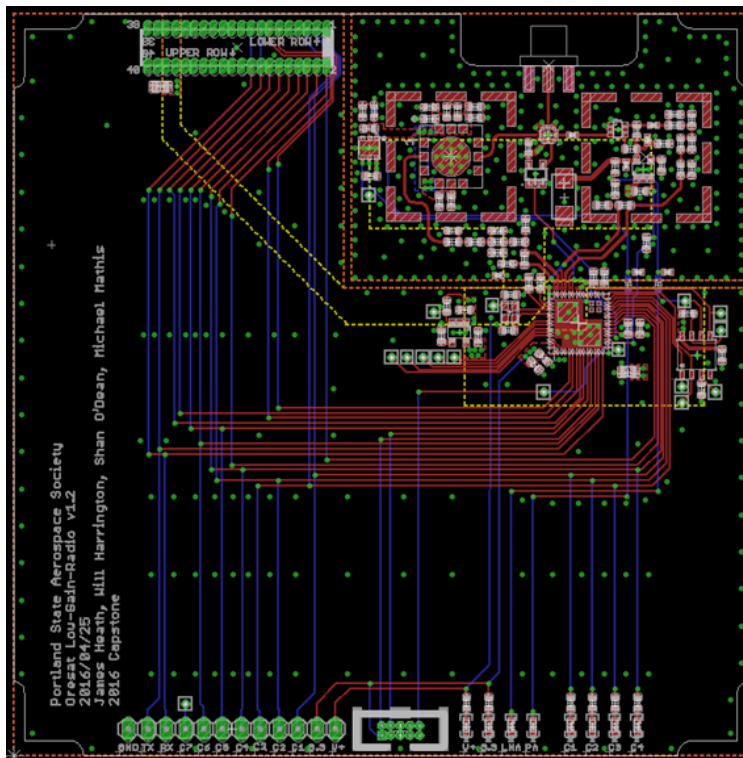American Institute of Aeronautics and Astronautics

Figure 19. PCB layout for the Low Gain Radio. The radio itself is isolated in the upper right hand corner of the board via an AC Ground plane that is connected to the DC ground through the kw0x.

Figure 19 is the PCB layout for the LGR. The board is oriented so that the top portion is the side that plugs into the back plane of the Cubesat via the forty pin connector on the upper left part of the figure. The upper right portion of the board is where the Tx and Rx lines are connected between the MCX to the antenna and the transceiver within the kw0x. The radio portion of board is on an isolated ground plane to help prevent extra interference between the AC and DC signals. This ground is connected via the two ground pads on the kw0x.

The left portion of the radio is the Tx line. It may be seen that the filter was placed out of the RF shield (indicated by the red rectangles) containing the PA due to size restraints. The radio signal is then sent out of the right portion of the RF shield and into the RF Switch. The right portion of the radio is where the Rx line is placed. Since the LNA was significantly smaller than the PA, the full filter was included within its RF shield as well however the tantalum capacitor was too large to include inside the shield.

Between the shield is the control line for the RF switch. This line is fed through an inverter from the kw0x and into the CTRL pin of the switch, due to the topology of the two chips.

To the right of the board is the SPI cache and along the bottom portion of the figure is the debugger pin-out, JTAG connector and debugging LEDs for easy access and line of site when the board is placed within the Cubesat structure.
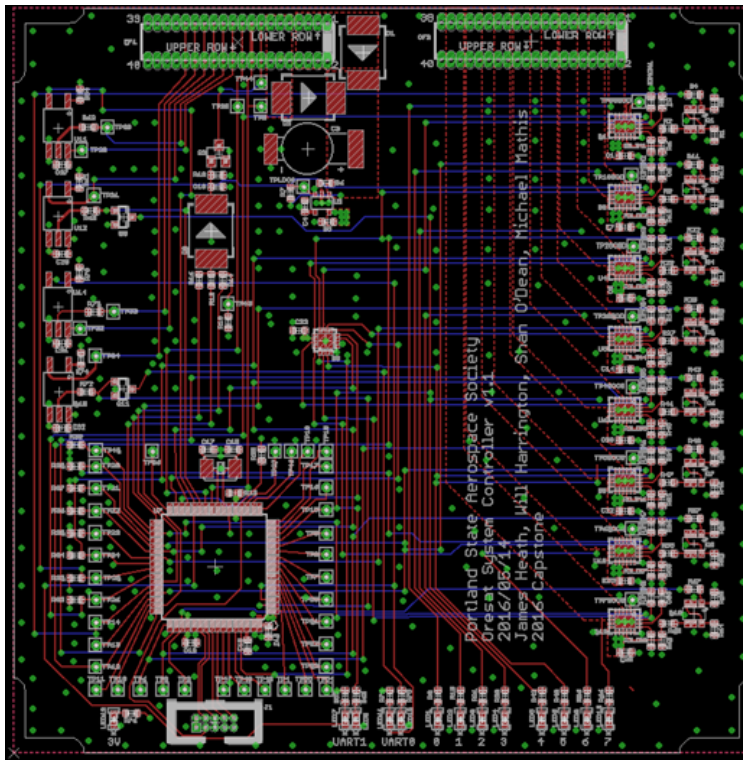
Figure 20. PCB layout for the System Controller. Test points were placed on as many available pins as possible for debugging purposes.

Figure 20 is the board layout for the System Controller. At the top of the board, two forty pin connectors are placed for plugging into the back plane of the Cubesat for communication to the rest of the satellite. In the bottom left hand corner of the Figure is the ATMega MCU. The far right portion of the board contains the Efuses. The lines through these chips are sent through the fuses from the ATMega MCU and connected to the forty pin connector on the upper right portion of the board. On the left hand side are the UART Tx and Rx between the MCU and left-hand forty pin connector via 4 opto-isolators.

The aforementioned nuclear option is seen directly right of the opto-isolators, where diode D1 is seen pointing towards the top of the board. To the upper right of that is the super-capacitor with two diodes ORing incoming power to charge the capacitor in the case a complete power down of the satellite is necessary.

Like the LGR board, the bottom portion of the board also contains a JTAG connector for programming and LEDs for debugging and testing.

III.C. Firmware

The microcontroller used for the LGR was the MKW01Z128 (aka kw0x) by NXP which features an integrated transceiver capable of Sub-GHz RF communications. The firmware developed for the kw0x includes basic pin configuration, clock configuration, transceiver configuration, and drivers for interfacing via SPI and UART. This firmware was the first instance of open source code for the kw0x.

The SPI driver for the MKW01Z128 is of importance because the integrated transceiver is not a memory-mapped peripheral. Instead, the transceiver is on its own piece of silicon but connected to the MCU via SPI. Therefore, a SPI driver is required to use the transceiver. The UART driver is also of importance as it is how the LGR communicates with the SC so that commands can be conveyed for execution. The drivers developed for SPI and UART offer a hardware abstraction layer that allows for easy initialization and use. Interrupts were also later developed to create an interrupt driven infinite main loop.

Development of the SC firmware was facilitated by open-source code from existing AVR libraries since

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the MCU (Atmel ATMega128) was AVR-based. An interrupt driven infinite main loop was developed in which the SC listens on UART for keep alive signals from the power module, LGR, and primary mission payload along with commands being communicated from the LGR. After enough missed keep alive signals, the MCU will power cycle the corresponding module. A simple command protocol is still being developed, however, a very basic way to power cycle modules was implemented by sending specific bytes via UART.

IV.   Testing & Results

The main portions of system testing were broken up into the three different areas: command, control, and communication. Other testing included component testing and power supply range tests. Component tests are imperative to the core operation of integrated circuits (microcontrollers, voltage regulators, etc.) that implement the desired functionality for the module they are a part of. These were usually small, simple tests that ensured that everything was working properly before attempting any tests for functionality. A basic overview of results will also be discussed. For a more comprehensive analysis of the results, please see the Github,[k] since the many of these results cannot adequately be shown via figures.

IV.A.   Supply Range Test

The Supply Range Test was for testing the voltage range operation of the LGR and SysCon. This was needed since both modules will be receiving a range of voltages from 3-5V from the power management system (another module in the CubeSat). This test was done by gradually changing the output voltage on the power supply from 3V-5V and checking that the board still operated. This test also doubled as a test for the crystal frequency and operation, since by checking the crystal it can secure that the MCU on either board is operating. Both boards operated with complete functionality for all ranges conducted in this test. Crystal frequency and voltage from the LDOs showed no fluctuations to the ICs they were powering when probed via oscilloscope.

IV.B.   Communication Test

The purpose of this test was to confirm that the radio was capable of transmission and reception, as well as switching between the Tx and Rx lines. This test was performed by sending a carrier signal from one board to the other and lighting an LED when receiving the signal. The test was performed within the LID lab from a range of roughly 5 meters. This was predetermined based on both convenience and also where the least restricted signal propagation path will occur.
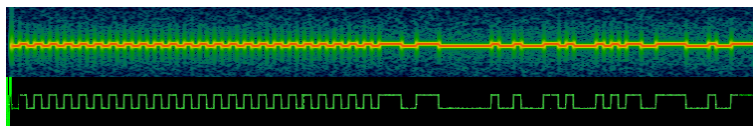

Figure 21.   Transmission of preamble and a message of 0-9 seen through an SDR's modulator

In Figure 21, the transmitted signal is shown via an SDR. The beginning portion (left side) of the Figure shows the preamble, followed by the transmission of 0 1 2 3 4 5 6 7 8 9 in a binary format. This test was successful, as the receiver was able to relay this message by UART, blinking this same pattern when receiving the transmitted data.

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[k]https://github.com/oresat/low-gain-radio/blob/v1_2/docs/Test_Plan_Sputnik_Capstone.md#sputnik-capstone-test-plan

Figure 22. Power Reading from the LGR on an Agilent E4418B Power Meter using a 5 dB attenuator.
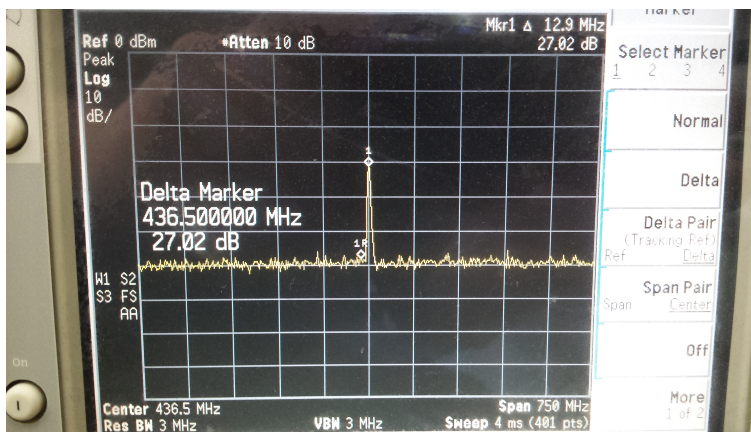

Figure 23. Photograph of the LGR signal on an Agilent E4405B spectrum analyzer. The signal center shows to be almost exactly at the target frequency of 436.5 MHz.

Figure 22 and 23 show the power meter and spectrum analyzer readings for the board. Since the limits on this equipment only allow a maximum input of 30 dBm, a 5 dBm attenuator was used, meaning the results were slightly lower than their actual values.

IV.C.   Command Test

The Command Test indicates whether the board is able to issue commands and update or respond based on these commands. To test this, the microcontroller sent a command to an LED to light up. If the LED lit up, then the command was successful, indicating that the board was able to issue commands.

This test was a success. When commands were sent via keyboard, specified LEDs would light up in accordance to how they were programmed.

IV.D.   Control Test

The system controller acts as the guardian of the system. Not shown, are two more identical UART lines to the payload in order to simplify the diagram. (ATMegaS128) with supporting radiation hardened LDO. For the purpose of prototyping, the controller is a standard, off-the-shelf ATMega128 chip.

To test the control system, a method to simulate a latch-up event was used to trigger the watchdog into action. In this test, the crystal on the kw0x was shorted to cause an error in the radio system. The ATMega

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should sense that the radio is no longer functioning properly and trigger the reset line on the kw0x to initiate a reboot. This was emulated via shorting the crystal with a wire. Once triggered, the SC successfully rebooted the system, indicating the ability to sense latch up like symptoms and resetting to help solve the problem.

IV.E. Functionality Test

The main and final test for this particular design was a 10km distance test. Two LGR setups were needed and were referred to as Board Tx and Board Rx. Board Tx sends a command to the other module that will cause it to output a desired payload. Board Rx listens for a command that will cause it to output the payload on a computer terminal via UART.

The location for this test was from the OHSU building in Portland, OR across the city to Rocky Butte. A map for reference can be seen in Figure 24.
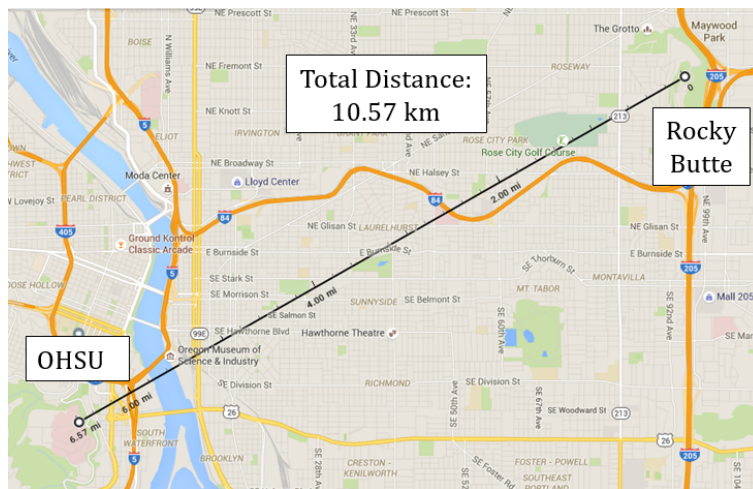

Figure 24. Map of the distance between the two modules for the Functionality Test at a 10.57 km range.

This final test was also successful. The data was transmitted and received successfully across 10 km. A video was filmed to show the success of this test, posted on PSAS' Twitter account.[1]

V.   Conclusion

The establishment of OreSat by PSAS in late 2015 prompted the need for a C3 module. An ECE senior capstone project at PSU was sponsored by PSAS to create this module within a 20 week time frame and a $1000 USD budget. The project was code named Sputnik because of its requirements to be a simple and reliable space system. The design of this space system was broken down into two sub-modules: the Low Gain Radio (LGR) and System Controller (SC). Both modules meet a form factor that allows them to slide into the CubeSat and connect to a common backplane.

The LGR is an important communications pipeline for the CubeSat that is capable of transmitting RF signals at 1 W (30 dBm); and because of its low gain communication can reach the CubeSat regardless of its orientation. Other than the crystal, which will need to be swept for radiation protection, the prototype produced used all COTS parts to minimize cost. This was difficult to do because LNAs that sufficiently met the noise figure needed for the 400km link budget were scarce. Therefore, the LNA used for the prototype produced only meets this requirement for a portion of the temperature range outlined in the requirements. The LGR interfaces with the SC via UART, and is connected to the power module via a switch that is controlled by the SC. This allows the SC to power cycle when SEUs occur. An antenna is connected to the

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[1]https://twitter.com/pdxaerospace/status/740772305966628865

LGR through the common backplane.

The SC is a watchdog responsible for detecting SEU's and rebooting subsystems. It is intended to be a radiation hardened (rad-hard) portion of the module therefore COTS components that have rad-hard analogues were used for the prototype produced. The rad-hard analogues often times have PCB footprints that differ from their OTS counterparts. Therefore, the SC that is actually used for flight will have a PCB layout different from the one presented in this report.

Firmware was also developed for the kw0x, the microcontroller that was used on the LGR, that supported the defined interfaces along with the use of the transceiver. Firmware for the SC microcontroller did not need to be developed since it was AVR-based. This allowed for the use of open-source software which increased the speed of producing the prototype.

The prototypes for the LGR and SC were designed, developed, manufactured and successfully tested within a 20 week time frame. The total cost of development was $901.70 USD. This module was the first avionics module for Oregon's first educational nanosatellite, and all material for the project is available online under an open-source license.

Appendix

Acknowledgments

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