This XML file does not appear to have any style information associated with it. The document tree is shown below.

```
− <root>
  − <simulation>
      <result_generated_time/>
      2020-08-17 20:07:14
    − <layer>
        <layer_spec/>
        {'B': 1, 'K': 384, 'C': 192, 'OY': 13, 'OX': 13, 'IY': 15, 'IX': 15, 'FY': 3, 'FX': 3,
        'SY': 1, 'SX': 1, 'SFY': 1, 'SFX': 1}
        <total_MAC_operation/>
        112140288
        <total_data_size_element/>
        {'W': 663552, 'I': 43200, 'O': 64896}
        <total_data_reuse/>
        {'W': 169, 'I': 2595.84, 'O': 1728}
      </layer>
    − <search_engine>
      − <mem_hierarchy_search>
          <mode/>
          exhaustive search
          <area_constraint/>
          3.5e6
          <area_utilization_threshold/>
          ≥ 0.75
          <consecutive_memory_level_size_ratio/>
          ≥ 8
          <max_inner_PE_mem_size_bit/>
          3000
          <max_inner_PE_mem_level/>
          2
          <max_outer_PE_mem_level/>
          2
          <mem_scheme_index/>
          6/8
        </mem_hierarchy_search>
      − <spatial_mapping_search>
          <mode/>
          heuristic search v2
          <spatial_utilization_threshold/>
```

0.9
<unrolling_scheme_index/>
5/5
</spatial_mapping_search>
− <temporal_mapping_search>
<mode/>
iterative search
<memory_utilization_hint/>
{'W': [0.7, 0.7, 0.7], 'I': [0.7, 0.7, 0.7], 'O': [0.7, 0.7, 0.7]}
<valid_temporal_mapping_found/>
{'partial': 681, 'final': 94}
</temporal_mapping_search>
</search_engine>
− <hw_spec>
− <PE_array>
<precision_bit/>
{'W': 16, 'I': 16, 'O_partial': 16, 'O_final': 16}
<array_size/>
{'Col': 14, 'Row': 12}
</PE_array>
− <memory_hierarchy>
− <mem_name_in_the_hierarchy>
<W/>
['rf512', 'sram128kb', 'sram16Mb']
<I/>
['rf512', 'sram128kb', 'sram16Mb']
<O/>
['rf512', 'sram16kb', 'sram16Mb']
</mem_name_in_the_hierarchy>
<mem_size_bit/>
{'W': [512.0, 524288.0, 16777216], 'I': [512.0, 524288.0, 16777216], 'O': [512.0, 65536.0, 16777216]}
<mem_bw_bit_per_cycle_or_mem_wordlength/>
{'W': [[32.0, 32.0], [128.0, 128.0], [128, 128]], 'I': [[32.0, 32.0], [128.0, 128.0], [128, 128]], 'O': [[32.0, 32.0], [128.0, 128.0], [128, 128]]}
<mem_access_energy_per_word/>
{'W': [[1.858, 2.573], [38.176, 41.952], [240, 240]], 'I': [[1.858, 2.573], [38.176, 41.952], [240, 240]], 'O': [[1.858, 2.573], [16.356, 17.804], [240, 240]]}
<mem_type/>
{'W': ['dp_sb', 'dp_sb', 'dp_sb'], 'I': ['dp_sb', 'dp_sb', 'dp_sb'], 'O': ['dp_sb', 'dp_sb', 'dp_sb']}
<mem_share/>
{1: [('O', 'sram16Mb'), ('I', 'sram16Mb'), ('W', 'sram16Mb')]}

<mem_area_single_module/>
{'W': [2847.0, 127880.0, 1000000], 'I': [2847.0, 127880.0, 1000000], 'O': [2847.0, 20636.0, 1000000]}
<mem_unroll/>
{'W': [156, 1, 1], 'I': [156, 1, 1], 'O': [156, 1, 1]}
</memory_hierarchy>
</hw_spec>
− <results>
− <basic_info>
− <spatial_unrolling>
<W/>
[[], [[('OY', 13)], [('FY', 3), ('C', 4)]], [], []]
<I/>
[[], [[('OY', 13)], [('FY', 3), ('C', 4)]], [], []]
<O/>
[[], [[('OY', 13)], [('FY', 3), ('C', 4)]], [], []]
</spatial_unrolling>
− <temporal_mapping>
<W/>
[[('OX', 13), ('K', 4), ('C', 2), ('FX', 3)], [('K', 6), ('C', 12)], [('K', 16), ('C', 2)]]
<I/>
[[('OX', 13), ('K', 4), ('C', 2), ('FX', 3), ('K', 6)], [('C', 12), ('K', 16)], [('C', 2)]]
<O/>
[[], [('OX', 13), ('K', 4), ('C', 2), ('FX', 3), ('K', 6), ('C', 12)], [('K', 16), ('C', 2)]]
</temporal_mapping>
<data_reuse/>
{'W': [13.0, 13, 1, 1], 'I': [2.6, 62.4, 16.0, 1.0], 'O': [12.0, 1, 72, 2]}
<I_pr_diagonally_broadcast_or_fifo_effect/>
'I': [True, False, False, False]
<used_mem_size_bit/>
{'W': [384, 331776, 10616832], 'I': [480, 345600, 691200], 'O': [16, 64896, 1038336], 'O_partial': [16, 64896, 1038336], 'O_final': [0, 0, 0]}
<actual_mem_utilization_individual/>
{'W': [0.75, 0.63, 0.63], 'I': [0.94, 0.66, 0.04], 'O': [0.03, 0.99, 0.06]}
<actual_mem_utilization_shared/>
{'W': [0.75, 0.63, 0.74], 'I': [0.94, 0.66, 0.74], 'O': [0.03, 0.99, 0.74]}
<effective_mem_size_bit/>
{'W': [96.0, 55296.0, 663552.0], 'I': [480, 345600, 345600.0], 'O': [16, 64896, 1038336], 'O_partial': [16, 64896, 1038336], 'O_final': [0, 0, 0]}
<total_unit_count/>
{'W': [156, 156, 1, 1], 'I': [156, 156, 1, 1], 'O': [156, 156, 1, 1]}

<unique_unit_count/>
{'W': [12, 12, 1, 1], 'I': [60, 60, 1, 1], 'O': [13, 13, 1, 1]}
<duplicate_unit_count/>
{'W': [13.0, 13.0, 1.0, 1.0], 'I': [2.6, 2.6, 1.0, 1.0], 'O': [12.0, 12.0, 1.0, 1.0]}
− <mem_access_count_elem>
<W/>
[[8626176, 663552], [663552, 663552], [663552, 0]]
<I/>
[[112140288, 691200], [691200, 43200], [43200, 0]]
<O/>
[[(112075392, 112140288), (9345024, 9280128)], [(9280128, 9345024), (129792, 64896)], [(64896, 129792), (0, 0)]]
<O_partial/>
[[(112075392, 112140288), (9345024, 9280128)], [(9280128, 9345024), (129792, 64896)], [(64896, 129792), (0, 0)]]
<O_final/>
[[(0, 0), (0, 0)], [(0, 0), (0, 0)], [(0, 0), (0, 0)]]
</mem_access_count_elem>
</basic_info>
− <energy>
<total_energy/>
2254581115.6
− <mem_energy_breakdown>
<W/>
[8867377.2, 6646136.8, 19906560.0]
<I/>
[105067556.4, 3524947.2, 1296000.0]
<O/>
[269006931.6, 40180358.4, 5840640.0]
</mem_energy_breakdown>
<mac_energy/>
1794244608
</energy>
− <performance>
− <mac_array_utilization>
<utilization_with_data_loading/>
0.4375
<utilization_without_data_loading/>
0.4644
<utilization_spatial/>
0.9286
<utilization_temporal_with_data_loading/>
0.4711

<mac_utilize_temporal_without_data_loading/>
0.5001
</mac_array_utilization>
<latency>
<latency_cycle_with_data_loading/>
1525776
<latency_cycle_without_data_loading/>
1437432
<ideal_computing_cycle/>
718848
<data_loading>
<load_cycle_total/>
88344
<load_cycle_individual/>
{'W': [36, 2592, 82944], 'I': [225, 2700, 5400]}
<load_cycle_combined/>
{'W': 82944, 'I': 5400}
</data_loading>
<mem_stalling>
<mem_stall_cycle_total/>
718584
<mem_stall_cycle_individual/>
{'W': [[-359424.0], [-691200.0, -635904.0], [-635904.0, -635904.0]],
'I': [[-359424.0], [-34176.0, 46464.0], [-39528.0, -39528.0]], 'O':
[[-359424.0], [0.0, 449280.0], [16223.999999999998, -43680.0]]}
<mem_stall_cycle_shared/>
{'W': [[-359424.0], [-691200.0, -635904.0], [-635904.0, 718584.0]],
'I': [[-359424.0], [-34176.0, 46464.0], [-39528.0, 718584.0]], 'O':
[[-359424.0], [0.0, 449280.0], [16223.999999999998, 718584.0]]}
<req_mem_bw_bit_per_cycle_individual/>
{'W': [[16.0, 1.2], [14.8, 14.8], [14.8, 0]], 'I': [[16.0, 4.6], [276.9,
15.4], [15.4, 0]], 'O': [[32.0, 32.0], [242.7, 242.7], [34.7, 34.7]]}
<req_mem_bw_bit_per_cycle_shared/>
{'W': [[16.0, 1.2], [14.8, 14.8], [64.8, 34.7]], 'I': [[16.0, 4.6], [276.9,
15.4], [64.8, 34.7]], 'O': [[32.0, 32.0], [242.7, 242.7], [64.8, 34.7]]}
<mem_bw_requirement_meet/>
{'W': [[True, True], [True, True], [True, True]], 'I': [[True, True],
[False, True], [True, True]], 'O': [[True, True], [False, False], [True,
True]]}
</mem_stalling>
</latency>
</performance>
<area/>
2711284.0

```
    </results>
    <elapsed_time_second/>
    416.601
  </simulation>
</root>
```