SINO WEALTH

SH79F6484

band 12 Place ADC Enhanced 8051 Microcontrollers

1. characteristic

- based on 8051 Instruction pipeline structure 8 Bit microcontroller
- Flash ROM : 64K byte
- RAM :internal 256 Bytes, outside 1280 byte, LCD RAM 28 byte
- class EEPROM : 1024 byte
- Operating Voltage:
  f_{OSC} = 32.768kHz - 16MHz , V_{DD} = 2.0V - 5.5V
- Oscillator (code option):
  - Crystal resonator: 32.768kHz
  - Crystal resonator: 2MHz - 16MHz
  - Ceramic Resonator: 2MHz - 16MHz
  - internal RC Oscillator: 12MHz (± 2%) / 128K
- 46/42 More CMOS Two-way I / O Pin
- 2 Selectable open-drain I / O mouth
- I / O Built-in pull-up resistor
- 4 More 16 Bit timer / counter: T2 , T3 , T4 with T5
- One 12 Place PWM Timer
- One 8 Place PWM Timer
- Interrupt sources:
  - Timer 2 , 3 , 4 , 5
  - External Interrupt 0 , 1 , 2 , 3
  - External Interrupt 4 : 8 Entry
  - ADC , EUART , SCM , LPD
  - PWM , CMP , SPI
- 2 Two enhanced EUART
- SPI Interface (master-slave mode)
- Built-in buzzer
- 9 aisle 12 Bit analog to digital converter (ADC), Built-in compare function
- Built-frequency detection module (with controllable feedback resistor)
- Built-in 2 A comparator (Schmitt window)
- led driver:
  - 3-8 X 8 segment(1 / 3-1 / 8 Duty cycle)
- LCD driver:(48 foot/ 44 foot)
  - 8 X 24 segment/ 20 segment(1/8 Duty cycle, 1/4 Bias)
  - 6 X 26 segment/ twenty two segment(1/6 Duty cycle, 1/4 or 1/3 Bias)
  - 5 X 27 segment/ twenty three segment(1/5 Duty cycle, 1/3 Bias)
  - 4 X 28 segment/ twenty four segment(1/4 Duty cycle, 1/3 Bias)
- Built-in low voltage reset (LVR) (Code Option)
  - LVR Voltage 1 : 4.1V
  - LVR Voltage 2 : 3.7V
  - LVR Voltage 1 : 2.8V
  - LVR Voltage 2 : 2.1V
- Built-in CRC Verifying module, optional check space
- Support single-line programming and simulation
- CPU Machine cycle: 1 Oscillator cycles
- Watchdog Timer (WDT)
- Warm-up
- Supports power saving modes of operation:
  - Idle Mode
  - Power-down mode
- Flash type
- Package: TQFP48 / LQFP44

2. Outline

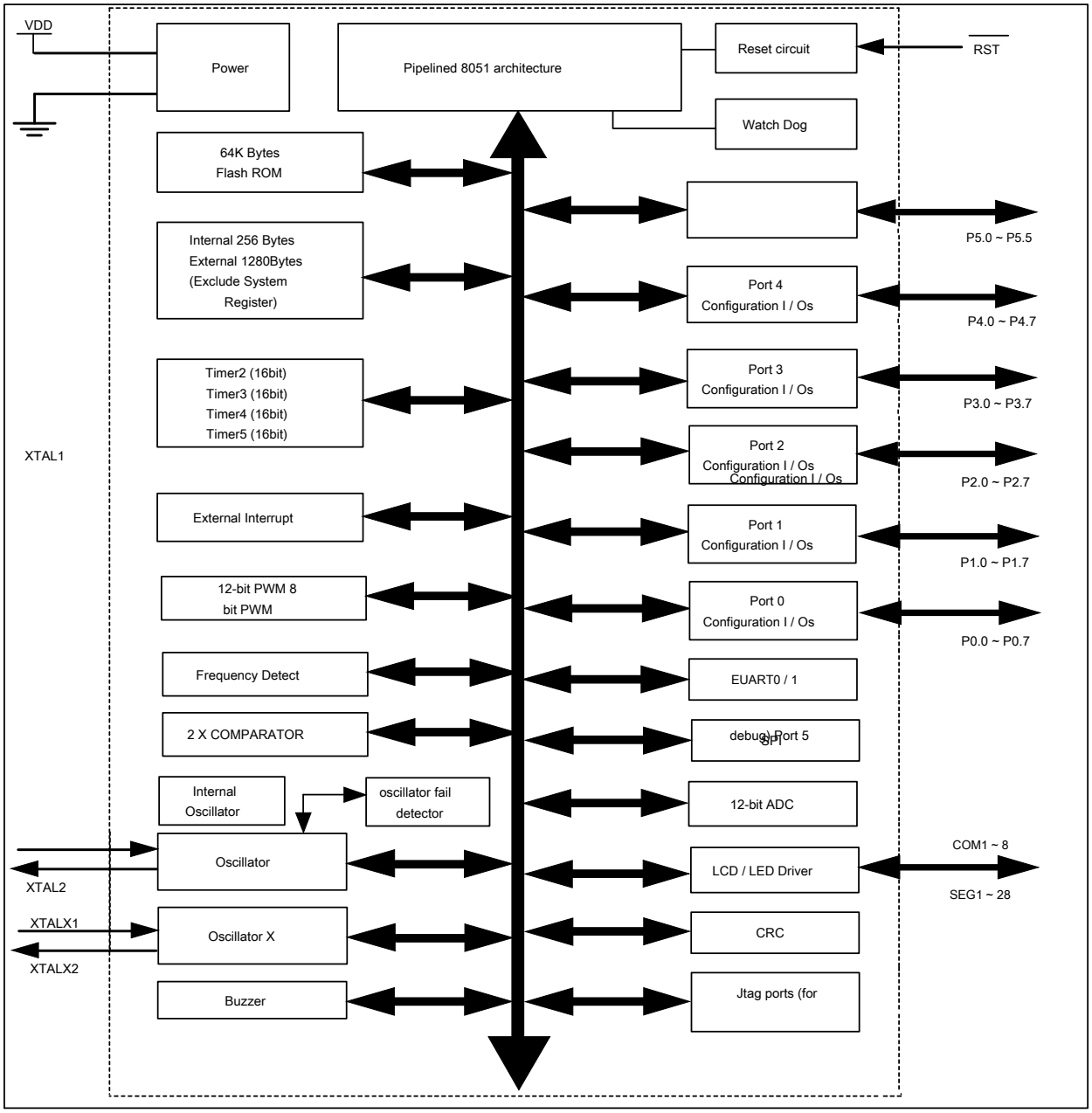
SH79F6484 It is a high speed high efficiency 8051 Compatible microcontroller. At the same frequency of oscillation, than the traditional 8051 It has a chip to run faster and superior characteristics.

SH79F6484 It retains the standard 8051 Most of the characteristics of the chip. These features include internal 256 byte RAM , UART And external interrupts INT0 , INT1 , INT2 with INT3 . In addition, SH79F6484 Integrating the external 1280 byte RAM Compatible with 8052 Chip 16 Bit timer / counter (Timer2). The microcontroller further includes a stored program adapted to 64K byte Flash Piece.

SH79F6484 Not only integrates such EUART / SPI And other standard communication modules, also integrated LCD Drive, having a built-in function of the comparison ADC , PWM Timers and other modules.

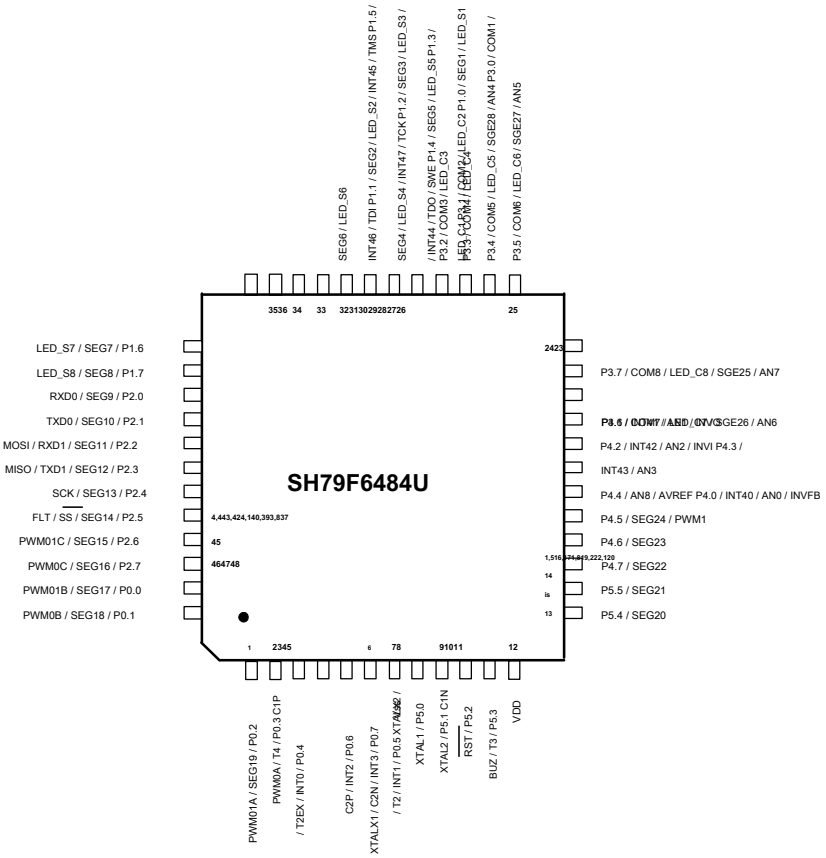
In addition, SH79F6484 Built CRC Module, and a frequency detection module 2 A comparator module. For high reliability and low power consumption, SH79F6484 Built watchdog timer, a low voltage reset and the system clock monitoring. Moreover SH79F6484 Also provides 2 Low-power saving mode.

3. Block diagram



4. Pin Configuration

48 4.1 Pin TQFP Package

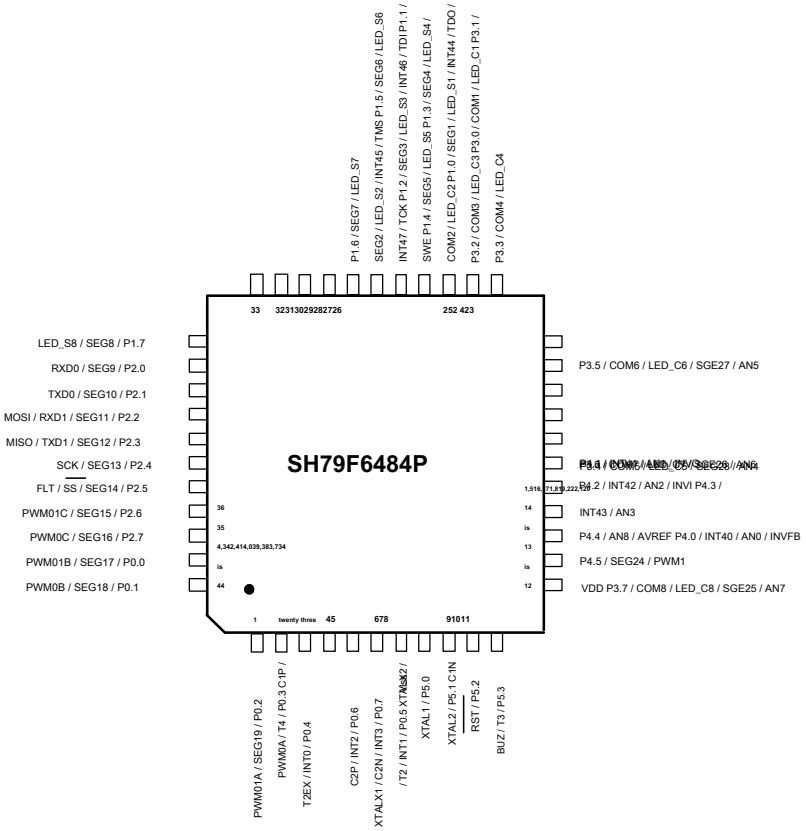


TQFP48 Pin Configuration

note:

Pin nomenclature, written on the outside of most pin function has the highest priority, the innermost pin function has the lowest priority (See Pin Configuration). When a pin is occupied by a higher priority function, *even if the low priority function is enabled, the pin can not be used as low-priority function. Only when the software is prohibited pin high-priority function, the corresponding pin be released for the low priority port.*

44 4.2 Pin LQFP Package



LQFP44 Pin Configuration

note:

Pin nomenclature, written on the outside of most pin function has the highest priority, the innermost pin function has the lowest priority (See Pin Configuration). When a pin is occupied by a higher priority function, *even if the low priority function is enabled, the pin can not be used as low-priority function. Only when the software is prohibited pin high-priority function, the corresponding pin be released for the low priority port.*

Table 4.1 Pin Function

Pin Number (TQFP48)	Pin Number (LQFP44)	Pin name	The default function
1	1	PWM01A / SEG19 / P0.2	P0.2
2	2	PWM0A / T4 / P0.3	P0.3
* 3	* 3	C1P / T2EX / INT0 / P0.4	P0.4
* 4	* 4	C1N / T2 / INT1 / P0.5	P0.5
5	5	XTALX2 / C2P / INT2 / P0.6	P0.6
6	6	XTALX1 / C2N / INT3 / P0.7	P0.7
7	7	V_{SS}	----
8	8	XTAL1 / P5.0	----
9	9	XTAL2 / P5.1	----
10	10	RST /P5.2	RST
11	11	BUZ / T3 / P5.3	P5.3
12	12	V_{DD}	----
13	-	SEG20 / P5.4	P5.4
14	-	SEG21 / P5.5	P5.5
15	-	SEG22 / P4.7	P4.7
16	-	SEG23 / P4.6	P4.6
17	13	PWM1 / SEG24 / P4.5	P4.5
18	14	AVREF / AN8 / P4.4	P4.4
19	15	AN3 / INT43 / P4.3	P4.3
20	16	INVI / AN2 / INT42 / P4.2	P4.2
twenty one	17	INVO / AN1 / INT41 / P4.1	P4.1
twenty two	18	INVFB / AN0 / INT40 / P4.0	P4.0
twenty three	19	AN7 / SEG25 / LED_C8 / COM8 / P3.7	P3.7
twenty four	20	AN6 / SEG26 / LED_C7 / COM7 / P3.6	P3.6
25	twenty one	AN5 / SEG27 / LED_C6 / COM6 / P3.5	P3.5
26	twenty two	AN4 / SEG28 / LED_C5 / COM5 / P3.4	P3.4
27	twenty three	LED_C4 / COM4 / P3.3	P3.3
28	twenty four	LED_C3 / COM3 / P3.2	P3.2
29	25	LED_C2 / COM2 / P3.1	P3.1
30	26	LED_C1 / COM1 / P3.0	P3.0
31	27	INT44 / LED_S1 / SEG1 / P1.0	P1.0
32	28	INT45 / LED_S2 / SEG2 / P1.1	P1.1

Continued on table

Pin Number (TQFP48)	Pin Number (LQFP44)	Pin name	The default function
33	29	INT46 / LED_S3 / SEG3 / P1.2	P1.2
34	30	INT47 / LED_S4 / SEG4 / P1.3	P1.3
35	31	LED_S5 / SEG5 / P1.4	P1.4
36	32	LED_S6 / SEG6 / P1.5	P1.5
37	33	LED_S7 / SEG7 / P1.6	P1.6
38	34	LED_S8 / SEG8 / P1.7	P1.7
39	35	RXD0 / SEG9 / P2.0	P2.0
40	36	TXD0 / SEG10 / P2.1	P2.1
41	37	MOSI / RXD1 / SEG11 / P2.2	P2.2
42	38	MISO / TXD1 / SEG12 / P2.3	P2.3
43	39	SCK / SEG13 / P2.4	P2.4
44	40	FLT / SS / SEG14 / P2.5	P2.5
45	41	PWM01C / SEG15 / P2.6	P2.6
46	42	PWM0C / SEG16 / P2.7	P2.7
47	43	PWM01B / SEG17 / P0.0	P0.0
48	44	PWM0B / SEG18 / P0.1	P0.1

*: *The port as a N- Open-drain channel*

5. Pin Description

Pin name	Types of	Explanation
I / O port		
P0.0 - P0.7	I / O	8 Bit bidirectional I / O port
P1.0 - P1.7	I / O	8 Bit bidirectional I / O port
P2.0 - P2.7	I / O	8 Bit bidirectional I / O port
P3.0 - P3.7	I / O	8 Bit bidirectional I / O port
P4.0 - P4.7	I / O	8 Bit bidirectional I / O port
P5.0 - P5.5	I / O	6 Bit bidirectional I / O port
Timer		
T2	I / O	Timer 2 External input / output baud clock
T3	I	Timer 3 External input
T4	I / O	Timer 4 External input / output compare
T2EX	I	Timer 2 Overload / Capture / direction control
PWM Controller		
PWM0A / 0B / 0C	O	12 Place PWM0 Timer output pin
PWM01A / 01B / 01C	O	12 Place PWM0 Complementary timer output pin
FLT	I	PWM0 Fault detection input pin
PWM1	O	8 Place PWM1 Timer output pin
EUART		
RXD0 / 1	I	EUART0 / 1 Data input pin
TXD0 / 1	O	EUART0 / 1 Data output pin
SPI		
MOSI	I / O	SPI The main output from the input pin
MISO	I / O	SPI Main input from the output pin
SCK	I / O	SPI The serial clock pin
$\overline{SS}$	I	SPI Slave select pin
ADC		
AN0 - AN7	I	ADC Input channel
AVREF	I	ADC External reference pins
LCD Controller		
COM1 - COM8	O	LCD display COM Signal output pin
SEG1-SEG19 SEG24-SEG28	O	LCD display Segment Signal output pin
led driver		
LED_C1 - LED_C8	O	led display COM Signal output pin
LED_S1 - LED_S8	O	led display Segment Signal output pin

Continued on table

Pin name	Types of	Explanation
Internal analog comparator		
C1N	I	Comparators 1 Inverting input terminal
C1P	I	Comparators 1 Inverting input terminal
C2N	I	Comparators 2 Inverting input terminal
C2P	I	Comparators 2 Inverting input terminal
Frequency detection module		
INVI	I	An input frequency detection
INVO	O	Output frequency detection
INVFB	O	Feedback output frequency detection
Interrupt & Reset & Clock & Power		
INT0 - INT3	I	External Interrupt 0--3
INT40 - INT47	I	External Interrupt 40--47
RST	I	Keeping the pin 10μs Above the low level, CPU Will be reset. An internal 30kΩ Pull-up resistor is connected to the V_{DD} , Only the connected external capacitor to a power-on reset
XTAL1	I	Input resonator
XTAL2	O	Oscillator output
XTALX1	I	Resonator X Entry
XTALX2	O	Resonator X Export
V_{SS}	P	Ground
V_{DD}	P	power supply(2.0 - 5.5V)
buzzer		
BUZ	O	Buzzer output
Programming Interface		
TDO (P1.0)	O	Four-wire debug interface: test data output
TMS (P1.1)	I	Four-wire debug interface: Test Mode Select
TDI (P1.2)	I	Four-wire debug interface: Test Data
TCK (P1.3)	I	Four-wire debug interface: Test clock input
SWE (P1.0)	I / O	Single-line simulation interface
note: *when P1.0-1.3 As a debugging interfaces, the original function is disabled*		

6. SFR Image

SH79F6484 Internal 256 Bytes of the registers comprising general purpose data memory and special function registers (SFR), SH79F6484 of SFR It is the following ::

CPU Core Register: ACC , B , PSW , SP , DPL , DPH

CPU Kernel enhancements register: AUXC , DPL1 , DPH1 , INSCON , XPAGE

Power Control Register Clock: PCON , SUSLO

Flash register: IB_OFFSET , IB_DATA , IB_CON1 , IB_CON2 , IB_CON3 , IB_CON4 , IB_CON5

Data Page Register Control: XPAGE

Watchdog Timer Register: RSTSTAT

The system clock control register: CLKCON , SCMCON

Interrupt Register: IEN0 , IEN1 , IENC , IPH0 , IPL0 , IPH1 , IPL1 , EXF0 , EXF1 , EXCON

I / O The registers of: P0 , P1 , P2 , P3 , P4 , P5 , P0CR , P1CR , P2CR , P3CR , P4CR , P5CR , P0PCR , P1PCR , P2PCR , P3PCR , P4PCR , P5PCR , P0OS

Timer register: TCON , T2CON , T2MOD , TH2 , TL2 , RCAP2L , RCAP2H , T3CON , TH3 , TL3 , T4CON , TH4 , TL4 , SWTHL , T5CON , TH5 , TL5

EUART register: SCON , SBUF , SADEN , SADDR , PCON , SCON1 , SBUF1 , SADEN1 , SADDR1 , SBRTL , SBRTH , BFINE

SPI register: SPCON , SPSTA , SPDAT

ADC register: ADCON , ADT , ADCH , ADDL , ADDH , ADCON1

LCD register: DISPCON , DISPCON1 , DISPCLK0 , P0SS , P1SS , P2SS , P3SS

led register: DISPCON , DISPCLK0 , P1SS , P3SS

BUZZER register: BUZCON

Comparator module: CMP1CON , CMP2CON , CMPCON0 , CMPCON1

The inverter module: INVCON , INVCTL , INVCTH

PWM register: PWMEN , PWMEN1 , PWM0C , PWM0PL , PWM0PH , PWM0DL , PWM0DH , PWM1C , PWM1P , PWM1D

LPD register: LPDCON

CRC register: CRCCON , CRCDL , CRCDH

Table 6.1 C51 nuclear SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
ACC	E0H	accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW D0H		Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Low byte data pointer	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	High byte data pointer	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON 86H		Data pointer select	--0--00-0	-	BKS0	-	-	DIV	MUL	-	DPS

Table 6.2 Power Control Clock SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
PCON	87H	power control	000-0000	SMOD	SSTAT	SSTAT1	-	GF1	GF0	PD	IDL
SUSLO 8EH		Power control and protection word	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 6.3 Flash control SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
IB_OFF SET	FBH Bank0	Programmable flash Low byte offset	00000000	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
IB_DATA FCH	Bank0	Programmable flash Data register	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1 F2H	Bank0	flash Control register 1	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2 F3H	Bank0	flash Control register 2	-----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3 F4H	Bank0	flash Control register 3	-----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4 F5H	Bank0	flash Control register 4	-----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5 F6H	Bank0	flash Control register 5	-----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
XPAGE F7H	Bank0	Programming address selection register	00000000	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
FLASHCON A7H	Bank0	flash Control register	------- 0	-	-	-	-	-	-	-	FAC

Table 6.4 WDT SFR

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
RSTSTAT B1H	Bank0	Watchdog timer control register	0-000000 *	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

note:* It stands for resetting different situations decision RSTSTAT Registers reset value, see WDT chapter

Table 6.5 Clock Control SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
CLKCON B2H	Bank0	System Clock Selection	111000--	32k_ SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	-	-
SCMCON A1H	Bank0	SCM Clock Select	-----011	-	-	-	-	-	SCK2	SCK1	SCK0

T able 6.6 Interrupt SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
IEN0	A8H Bank0	Interrupt Enable Control 0	00000000	EA	EADC	ET2	ES	ECMP	EX1	ET5	EX0
IEN1	A9H Bank0	Interrupt Enable Control 1	00000000	ESCM_LPD _CRC	ET4	EPWM	ET3_ES1	EX4	EX3	EX2	ESPI
IENC	BAH Bank0	Interrupt channel allows control	00000000	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
IENC1	BBH Bank0	Interrupt channel allows control 1	--0000000	-	ECRC	ES1	ET3	ECMP1	ECMP2	ESCM	ELPD
IPH0	B4H Bank0	High priority interrupt control 0	--0000000	-	PADCH	PT2H	PSH	PCMPH	PX1H	PT5H	PX0H
IPL0	B8H Bank0	Low interrupt priority control 0	--0000000	-	PADCL	PT2L	PSL	PCMPL	PX1L	PT5L	PX0L
IPH1	B5H Bank0	High priority interrupt control 1	00000000	PSCMH	PT4H	PPWMH	PT3S1H	PX4H	PX3H	PX2H	PSPIH
IPL1	B9H Bank0	Low interrupt priority control 1	00000000	PSCML	PT4L	PPWML	PT3S1L	PX4L	PX3L	PX2L	PSPIL
EXF0	E8H Bank0	External interrupt register 0	00000000	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
EXF1	D8H Bank0	External interrupt register 1	00000000	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
EXCON 8BH	Bank0	External interrupt sampling control	00000000	I1PS1	I1PS0	I1SN1	I1SN0	I0PS1	I0PS0	I0SN1	I0SN0

Table 6.7 port SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
P0	80H Bank0	8 Bit port 0	00000000	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1	90H Bank0	8 Bit port 1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2	A0H Bank0	8 Bit port 2	00000000	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3	B0H Bank0	8 Bit port 3	00000000	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4	C0H Bank0	6 Bit port 4	---000 000	-	-	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5	80H Bank1	4 Bit port 5	-----0000	-	-	-	-	P5.3	P5.2	P5.1	P5.0
P0CR	E1H Bank0	port 0 Input / output direction control	00000000	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR	E2H Bank0	port 1 Input / output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR	E3H Bank0	port 2 Input / output direction control	00000000	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR	E4H Bank0	port 3 Input / output direction control	00000000	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR	E5H Bank0	port 4 Input / output direction control	---000 000	-	-	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR	E1H Bank1	port 5 Input / output direction control	-----0000	-	-	-	-	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P0PCR	E9H Bank0	port 0 Pull allow the internal	00000000	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR	EAH Bank0	port 1 Pull allow the internal	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR	EBH Bank0	port 2 Pull allow the internal	00000000	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR	ECH Bank0	port 3 Pull allow the internal	00000000	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR	EDH Bank0	port 4 Pull allow the internal	---000 000	-	-	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR	E9H Bank1	port 5 Pull allow the internal	-----0000	-	-	-	-	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
P0OS	EFH Bank0	Output Mode Selection	-- 00 ----	-	-	P0OS.5	P0OS.4	-	-	-	-

T able 6.8 Timer SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
TCON	88H Bank0	Timer / Counter Control Register	-----0000	-	-	-	-	IE1	IT1	IE0	IT0
T2CON C8H	Bank0	Timer / Counters 2 Control register	00000000	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / T 2	CP / R L 2
T2MOD C9H	Bank0	Timer / Counters 2 Mode register	0 ----- 00	TCLKP2	-	-	-	-	-	T2OE	DCEN
RCAP2L CAH	Bank0	Timer / Counters 2 Overload / low byte interception 00000000		RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H CBH	Bank0	Timer / Counters 2 Overload / interception high byte 00000000		RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH Bank0	Timer / Counters 2 Low byte	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH Bank0	Timer / Counters 2 High byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
T3CON	88H Bank1	Timer / Counters 3 Control register	0-00-000	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
SWTHL	89H Bank1	Timer / counter read the data switching control	-------00	-	-	-	-	-	- T5HLCON	T3HLCON	
TL3	8CH Bank1	Timer / Counters 3 Low byte	00000000	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	8DH Bank1	Timer / Counters 3 High byte	00000000	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
T4CON C8H	Bank1	Timer / Counters 4 Control register	00000000	TF4	TC4	T4PS1	T4PS0	T4M1	T4M0	TR4	T4CLKS
TL4	CCH Bank1	Timer / Counters 4 Low byte	00000000	TL4.7	TL4.6	TL4.5	TL4.4	TL4.3	TL4.2	TL4.1	TL4.0
TH4	CDH Bank1	Timer / Counters 4 High byte	00000000	TH4.7	TH4.6	TH4.5	TH4.4	TH4.3	TH4.2	TH4.1	TH4.0
T5CON C0H	Bank1	Timer / Counters 5 Control register	0-00--0-	TF5	-	T5PS1	T5PS0	-	-	TR5	-
TL5	CEH Bank1	Timer / Counters 5 Low byte	00000000	TL5.7	TL5.6	TL5.5	TL5.4	TL5.3	TL5.2	TL5.1	TL5.0
TH5	CFH Bank1	Timer / Counters 5 High byte	00000000	TH5.7	TH5.6	TH5.5	TH5.4	TH5.3	TH5.2	TH5.1	TH5.0

Table 6.9 E UART SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
SCON	98H Bank0	EUART0 Serial Control	00000000	SM0 / FE	SM1 / RXOV	SM2 / TXCOL	REN	TB8	RB8	TI	RI
SBUF	99H Bank0	EUART0 Serial data buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADEN 9BH	Bank0	EUART0 Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
SADDR 9AH	Bank0	EUART0 Slave address	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
PCON	87H Bank0	Power control and serial	00--0000	SMOD	SSTAT	–	-	GF1	GF0	PD	IDL
SCON1	98H Bank1	EUART1 Serial Control	00000000	SM10 / FE1	SM11 / RXOV1	SM12 / TXCOL1	REN1	TB18	RB18	TI1	RI1
SBUF1	99H Bank1	EUART1 Serial data buffer	00000000	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
SADEN1 9AH	Bank1	EUART1 Slave Address Mask	00000000	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
SADDR1 9BH	Bank1	EUART1 Slave address	00000000	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
SBRTH 9DH	Bank1	EUART1 High baud rate generator	00000000	SBRTEN	SBRT.14		SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL	9CH Bank1	EUART1 Low baud rate generator	00000000	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
BFINE	9EH Bank1	EUART1 Baud rate generator fine tuning	0000 ----	BFINE.7	BFINE.6	BFINE.5	BFINE.4	-	-	–	-

Table 6.10 SPI SF Rs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
SPCON A2H	Bank0	SPI Control register	00000000	DIR	MSTR	CPHA	CPOL	SSDIS	SPR2	SPR1	SPR0
SPSTA	F8H Bank0	SPI Status Register	00000 ---	SPEN	SPIF	MODF	WCOL	RXOV	-	-	-
SPDAT	A3H Bank0	SPI Data register	00000000	SPDAT7	SPDAT6	SPDAT5	SPDAT4	SPDAT3	SPDAT2	SPDAT1	SPDAT0

Table 6.11 ADC SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
ADCON 93H	Bank0	ADC control	00000000	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	GO / DONE
ADT	94H Bank0	ADC Time Configuration	00000000	TADC2	TADC1	TADC0	CDIR	TS3	TS2	TS1	TS0
ADCH	95H Bank0	ADC Channel configuration	00000000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
ADDL	96H Bank0	ADC Low byte of data	-----0000	-	-	-	-	A3	A2	A1	A0
ADDH	97H Bank0	ADC High data byte	00000000	A11	A10	A9	A8	A7	A6	A5	A4
ADCON1 92H	Bank0	ADC control 1	-----000	-	-	-	-	-	RESO	CH8	SCH3

Table 6.12 Buzzer SFR

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
BUZCON BDH	Bank0	Buzzer output control	-----0000	-	-	-	-	BCA2	BCA1	BCA0	BZEN

Table 6.13 LCD SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
DISPCON ABH	Bank0	LCD Control register	00000000	DISPSEL	LCDON	ELCC	DUTY0	VOL3	VOL2	VOL1	VOL0
DISPCON1 ADH	Bank0	LCD Control register 1	00000000	MODSW DUTY2		DUTY1	RLCD	FCCTL1	FCCTL0	MOD1	MOD0
DISPCLK0 ACH	Bank0	LCD Clock control register 0	-------00	-	-	-	-	-	-	DCK1	DCK0
P0SS	B6H Bank0	P0 Mode Select Register	---0--000	-	-	P4S5	-	-	P0S2	P0S1	P0S0
P1SS	9CH Bank0	P1 Mode Select Register	00000000	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
P2SS	9DH Bank0	P2 Mode Select Register	00000000	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
P3SS	9EH Bank0	P3 Mode Select Register	00000000	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0

Table 6.14 LED SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
DISPCON ABH	Bank0	led Control register	00-0 ----	DISPSEL	LEDON	-	DUTY0	-	-	-	-
DISPCON1 ADH	Bank0	led Control register 1	000 -----	MODSW DUTY2		DUTY1	-	-	-	-	-
DISPCLK0 ACH	Bank0	led Clock control register 0	-------00	-	-	-	-	-	-	DCK1	DCK0
P1SS	9CH Bank0	P1 Mode Select Register	00000000	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
P3SS	9EH Bank0	P3 Mode Select Register	00000000	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0

Table 6.15 PWM SFRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
PWMEN CFH	Bank0	PWM0 Timer allows	00000000	EPWM0	EFLT	PWM01COE	PWM01BOE	PWM01AOE	PWM0COE	PWM0BOE	PWM0AOE
PWMLO E7H	Bank0	PWM0 protection	00000000	PWMLO.7	PWMLO.6	PWMLO.5	PWMLO.4	PWMLO.3	PWMLO.2	PWMLO.1	PWMLO.0
PWM0C D2H	Bank0	12 Place PWM0 control	00000000	PWM0IE	PWM0IF	TnCK02	FLTS	FLTC	PWM0S	TnCK01	TnCK00
PWM0PL D3H	Bank0	12 Place PWM0 Low cycle control	00000000	PP0.7	PP0.6	PP0.5	PP.4	PP0.3	PP0.2	PP0.1	PP0.0
PWM0PH D4H	Bank0	12 Place PWM0 High cycle control	----0000	-	-	-	-	PP0.11	PP0.10	PP0.9	PP0.8
PWM0DL D5H	Bank0	12 Place PWM0 Low duty cycle control	00000000	PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
PWM0DH D6H	Bank0	12 Place PWM0 High duty cycle control	----0000	-	-	-	-	PD0.11	PD0.10	PD0.9	PD0.8
PWM0DT D1H	Bank0	12 Place PWM0 Dead-time control	00000000	DT0.7	DT0.6	DT0.5	DT0.4	DT0.3	DT0.2	DT0.1	DT0.0
PWM1C D9H	Bank0	8 Place PWM1 Control register	0000-000	PWM1EN	PWM1S	TnCK11	TnCK10	-	PWM1IE	PWM1IF	PWM1OE
PWM1P DAH	Bank0	8 Place PWM1 Cycle register	00000000	PP1.7	PP1.6	PP1.5	PP1.4	PP1.3	PP1.2	PP1.1	PP1.0
PWM1D DBH	Bank0	8 Place PWM1 Duty register	00000000	PD1.7	PD1.6	PD1.5	PD1.4	PD1.3	PD1.2	PD1.1	PD1.0

Table 6.16 LPD S FR

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
LPDCON B3H	Bank0	LPD control	00000000	LPDEN	LPDF	LPDMD	LPDIF	LPDS3	LPDS2	LPDS1	LPDS0

Table 6.17 Frequency Detect SFR

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
INVCON C5H	Bank0	Inverter control	0--00000	INVEN	-	-	FBEN	RESFB1	RESFB0	INVDEB1	INVDEB0
INVCTL C6H	Bank0	Inverter Counter Low	00000000	INVC7	INVC6	INVC5	INVC4	INVC3	INVC2	INVC1	INVC0
INVCTH C7H	Bank0	Inverter Counter High	00000000	INVC15	INVC14	INV C13	INVC12	INVC11	INVC10	INVC9	INVC8

Table 6.18 Comparators SFR

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
CMP1CON C1H	Bank0	Comparators 1 control	00000-00	CMP1EN	C1NCHS1	C1NCHS0		C1OUT	C1IF	C1RFS	C1DEB1	C1DEB0
CMP2CON C2H	Bank0	Comparators 2 control	00000-00	CMP2EN	C2NCHS1	C2NCHS0		C2OUT	C2IF	C2RFS	C2DEB1	C2DEB0
CMPCON0 C3H	Bank0	Compare auxiliary control 0	00000000	C2IFS1	C2IFS0	C1IFS1	C1IFS0	C2SMT1	C2SMT0	C1SMT1	C1SMT0
CMPCON1 C4H	Bank0	Compare auxiliary control 1	------- 1	-	-	-	-	-	-	-	C2LIMEN

Table 6.19 CRC S FRs

symbol address		name	POR / WDT / LVR / PIN Reset value	The first 7 Place	The first 6 Place	The first 5 Place	The first 4 Place	The first 3 Place	The first 2 Place	The first 1 Place	The first 0 Place
CRCCON FDH	Bank0	CRC Check control	00-00000	CRC_GO	CRCIF	-	CRCADR4	CRCADR3	CRCADR2	CRCADR1	CRCADR0	
CRCDL	F9H Bank0	CRC Low check results	00000000	CRCD7	CRCD6	CRCD5	CRCD4	CRCD3	CRCD2	CRCD1	CRCD0
CRCDH FAH	Bank0	CRC Check the results of the high	00000000	CRCD15	CRCD14	CRCD13	CRCD12	CRCD11	CRCD10	CRCD9	CRCD8

Note: -: Reserved bits.

SFR Image Map

Bank0

	Bit addressable	Not bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8H	SPSTA	CRCDL	CRCDH	IB_OFFSET	IB_DATA	CRCCON			FFH
F0H	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7H
E8H	EXF0	P0PCR	P1PCR	P2PCR	P3PCR	P4PCR		P0OS	EFH
E0H	ACC	P0CR	P1CR	P2CR	P3CR	P4CR		PWMLO	E7H
D8H	EXF1	PWM1C	PWM1P	PWM1D					DFH
D0H	PSW	PWM0DT	PWM0C	PWM0PL	PWM0PH	PWM0DL	PWM0DH		D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		PWMEN	CFH
C0H	P4	CMP1CON	CMP2CON	CMPCON0	CMPCON1		INVCON	INVCTL	INVCTH C7H
B8H	IPL0	IPL1	IENC	IENC1		BUZCON			BFH
B0H	P3	RSTSTAT	CLKCON	LPDCON		IPH0	IPH1	P0SS	B7H
A8H	IEN0	IEN1	DISPCLK1	DISPCON	DISPCLK0	DISPCON1			AFH
A0H	P2	SCMCON	SPCON		SPDAT		ISPLO	ISPCON	FLASHCON A7H
98H	SCON	SBUF	SADDR	SADEN	P1SS	P2SS	P3SS		9FH
90H	P1		ADCON1	ADCON	ADT	ADCH	ADDL	ADDH	97H
88H	TCON			EXCON			SUSLO		8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Bank1

	Bit addressable	Not bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8H									FFH
F0H	B	AUXC						XPAGE	F7H
E8H		P5PCR							EFH
E0H	ACC	P5CR							E7H
D8H									DFH
D0H	PSW								D7H
C8H	T4CON				TL4	TH4	TL5	TH5	CFH
C0H	T5CON								C7H
B8H	IPL0	IPL1							BFH
B0H					IPH0	IPH1			B7H
A8H	IEN0	IEN1							AFH
A0H									A7H
98H	SCON1	SBUF1	SADDR1	SADEN1	SBRTL	SBRTH	BFINE		9FH
90H									97H
88H	T3CON	SWTHL			TL3	TH3	SUSLO		8FH
80H	P5	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

***note:** Unused SFR Address prohibited to read and write.*

7. Standard features

7.1 CPU

7.1.1 CPU Core characteristics Special Function

Registers

- CPU Core Register: ACC , B , PSW , SP , DPL , DPH

accumulator

accumulator ACC It is a common special register, the instruction used in the system A As the mnemonic accumulator.

B register

In the multiply and divide instructions, will be used B register. In other instructions, B It may be used as a scratchpad register.

Stack pointer (SP)

Stack Pointer SP Is a 8 Bit special purpose registers, the execution PUSH Various subroutine call, interrupt response and other instruction, SP Before adding 1 And then push data; performing POP , RET , RETI Once instruction, the data stack exit SP Minus 1 . The stack may be an internal on-chip RAM (00H-FFH) After any address, reset, SP Initialized 07H , By the fact that the stack 08H Address start.

Program status word (PSW)register

Program status word (PSW) Register contains the program status information.

Data Pointer (DPTR)

Data Pointer DPTR Is a 16 Bit special purpose registers, with the high byte DPH He indicates low byte with DPL Representation. They either as a 16 Bit register DPTR To deal with, or as 2 Independent 8 Bit register DPH with DPL To deal with.

Table 7.1 PSW register

D0H	The first 7 No. 6 No. 5 No. 4 No. 3 No. 2 No. 1 No. 0 Place							
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	Read / Write	read
Reset value (POR / WDT / LVR / PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Symbol	Explanation
7	CY	Carry flag 0 : Arithmetic or logical operation, without carry or borrow 1 : Arithmetic or logic operation, a carry or borrow
6	AC	Auxiliary carry flag 0 : Arithmetic or logic operation, no carry or borrow 1 : Arithmetic or logic operation, an auxiliary carry or borrow
5	F0	F0 Flag User-defined flags
4-3	RS [1: 0]	R0-R7 Register page select bits 00 :page 0 (Mapped to 00H-07H) 01 :page 1 (Mapped to 08H-0FH) 10 :page 2 (Mapped to 10H-17H) 11 :page 3 (Mapped to 18H-1FH)
2	OV	Overflow flag 0 : No overflow has occurred 1 : There is an overflow occurs
1	F1	F1 Flag User-defined flags
0	P	Parity 0 :accumulator A Median 1 An even number of digits 1 :accumulator A Median 1 The median odd