**Class Proceedings**

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| **Course:** | **Computer Organization** | **Faculty Member:** | **Rehan Azmat** |

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| **S.no** | **Date** | **Topics** | **Status** |
| 13 | Thursday, Feb 28,2013 | Number of Address, Types of Operand, Types of operations | **P** |
| 12 | Thursday, Feb 28,2013 | Introduction Instruction Set Architecture, Types of operations. | **P** |
| 11 | Wednesday, Feb 27,2013 | Vrtual Memory, Inverted Page Table, TLB, Segmentation, Processor Register, Instruction cycle, Instruction execution | **P** |
| 10 | Tuesday, Feb 26,2013 | Memory Management, Partitioning, Paging | **P** |
| 9 | Wednesday, Feb 20,2013 | Replacement Algo, Write Policies, Line Size, Multi level Cache and Unified vs Split Cache. | **P** |
| 8 | Tuesday, Feb 19,2013 | Cache Design. | **P** |
| 7 | Thursday, Feb 14,2013 | Lab: Module Design in Verilog | **A** |
| 6 | Thursday, Feb 14,2013 | Lab: Module Design in Verilog | **A** |
| 5 | Wednesday, Feb 13,2013 | Memory Hierarchy, Introduction of Cache | **P** |
| 4 | Tuesday, Feb 12,2013 | Memory System, Memory Characteristics. | **A** |
| 3 | Thursday, Feb 07,2013 | Lab: Introduction to Verilog | **A** |
| 2 | Thursday, Feb 07,2013 | Lab: Intorduction to Verilog | **A** |
| 1 | Wednesday, Feb 06,2013 | Introduction, Difference between Computer Architecture and Computer Organization. | **A** |
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**Class Proceedings**

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| **Course:** | **Electronics - II** | **Faculty Member:** | **Masood Ahmed(EE)** |

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| **S.no** | **Date** | **Topics** | **Status** |
| 22 | Wednesday, Mar 13,2013 | Check sessional one paper to the class, Exercise problem 20, Design Problem of low frequency VDR bias amplifier. | **P** |
| 21 | Tuesday, Mar 12,2013 | sessional one... | **P** |
| 20 | Tuesday, Mar 12,2013 | Sessional one... | **P** |
| 19 | Monday, Mar 11,2013 | sessional 1 Exam | **A** |
| 18 | Wednesday, Mar 06,2013 | Low frequecncy Analysis, Example 9.8, Low frequency response of BJT amplifier, Example 9.9. | **P** |
| 17 | Tuesday, Mar 05,2013 | Lab#04... | **P** |
| 16 | Tuesday, Mar 05,2013 | Lab#04... | **P** |
| 15 | Monday, Mar 04,2013 | Itroduction to Frequecy response, Example, Amplitude and Phase distortion, Decibels,Example, Semilog andd log-log Plots,Example | **A** |
| 14 | Wednesday, Feb 27,2013 | Fet small signal model of JFET, Graphical and mathematical model of gm, Example, JFET fixed and self bias Configurtion, Example 8.7, VDR configuration. | **A** |
| 13 | Tuesday, Feb 26,2013 | Lab03... | **P** |
| 12 | Tuesday, Feb 26,2013 | Lab03... | **P** |
| 11 | Monday, Feb 25,2013 | Cascade systems, Darlington connection, Dc and Ac analysis,Example 5.20, Exercise prloblem 8,Exercise prloblem 69,70,Quiz # 01. | **P** |
| 10 | Wednesday, Feb 20,2013 | Emitter Follower Configuration,Example 5.10,Common Base configuration,Effect of RL and RS,Example 5.14,Exercise Question 30 | **P** |
| 9 | Tuesday, Feb 19,2013 | LAB02... | **P** |
| 8 | Tuesday, Feb 19,2013 | LAB02... | **P** |
| 7 | Monday, Feb 18,2013 | Example5.4, Example5.5, CE Emitter Bias Configuration Unbypassed, Example5.6, Example5.7, Example5.8, Example5.9 | **A** |
| 6 | Wednesday, Feb 13,2013 | Voltage Divider Bias(Derivation of all parameters), Example 5.5 | **P** |
| 5 | Tuesday, Feb 12,2013 | LAB01... | **P** |
| 4 | Tuesday, Feb 12,2013 | LAB01.. | **P** |
| 3 | Monday, Feb 11,2013 | Common Emitter Fixed Bias configuration(Derivation if Av,Zin,Zout,Ai), Example 5.4 | **P** |
| 2 | Wednesday, Feb 06,2013 | Amplifier,Amp.Properties(voltage current and power gain,input and output impedence), Example,Ac analysis of BJT,re model. | **A** |
| 1 | Monday, Feb 04,2013 | Introduction to Class, Introduction to Course, Discuss Course outline, Revise Electronics-I concepts | **A** |