Working Draft

X3T13 2008D

Revision 7b
27 January 1997

Information Technology - AT Attachment-3 Interface (ATA-3)

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X3T13 Technical Editor:

Peter T. McLean
Maxtor Corporation
2190 Miller Drive
Longmont, CO 80501-6744
USA

Tel: 303-678-2149
Fax: 303-682-4811
Email: pete_mclean@maxtor.com

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Other Points of Contact:

X3T13 Chair
Gene Milligan
Seagate Technology
OKM 251
10323 West Reno (West Dock)
P.O. Box 12313
Oklahoma City, OK 73157-2313
Tel: 405-324-3070
Fax: 405-324-3794
E-mail: gene_milligan@notes.seagate.com

X3T13 Vice-Chair
Pete McLean
Maxtor Corporation
2190 Miller Drive
Longmont, CO 80501
Tel: 303-678-2149
Fax: 303-682-4811
E-mail: pete_mclean@maxtor.com

X3 Secretariat
Lynn Barra
Administrator Standards Processing
X3 Secretariat
1250 Eye Street, NW Suite 200
Washington, DC 20005
Tel: 202-626-5738
Fax: 202-638-4922
Email: LBARRA@ITIC.NW.DC.US

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DOCUMENT STATUS

Revision 0 - 28 February 1995

Initial document. Created from X3T10/948D Revision 2k, the proposed AT Attachment Interface with Extensions (ATA-2) standard, and the following proposed additions:

X3T10/94-053r3	Reset Pulse Duration
X3T10/94-087r3	Security Mode
X3T10/94-154r1	Check Power Mode Enhancement
X3T10/95-144r0	Identify Device DMA
X3T10/95-145r0	Device 1 Only

It is the intent of the editor that any changes that may be made to X3T10/948D by the X3T10 be implemented in this document as well. In addition, the editor has taken the liberty to make improvements as deemed necessary, understanding that the entire document is subject to review and change.

Revision 1 - 21 April 1995

Added changes made to X3T10/948D Revision 3 as a result of letter ballot. Rewrote Abstract, Introduction and Scope. Added the proposals approved at the April 12-13, 1995 meeting as follows:

X3T10/95-125r2	Dynamic Power Selection
X3T10/95-155r0	Delete DASP timing clause 10.6
X3T10/95-198r0	DRDY max set time 30 sec
X3T10/95-198r0	Paragraph merge in READ MULTIPLE command
X3T10/95-199r0	Modify driver current

Revision 2 - 2 June 1995

Added proposal X3T10/95-154r1 and 10K pulldown to DD7 as approved at the 11 May 1995 meeting.

Revision 3 - 26 July 1995

Per the June 21-22 working group meeting:

Corrected reset timing figures
Added FFh not specified in revision word.
Removed word “non-shielded” from Clause 5.1.

Per the July 18-20 working group meeting:

Added ATAPI bit definition in word 1 of DEVICE ID response.
Removed DEVICE ID response word 71.
Moved DEVICE ID response words 72 and 73 to words 73 and 74.
Added SFF8035i S.M.A.R.T. into the standard.
Added X3T10/95-294r0, Set Features changes into document.
Reformatted protocol diagrams.
Added DD7 pull-down modification.
Deleted Annex A, reset considerations.
Moved 40-pin connector definition into new Annex A that includes other connector definitions previously in Annex B and C.
Deleted the IOCS16- signal.
Deleted WRITE SAME command.
Made numerous other minor changes requested during page-by-page review.

Revision 4 - 6 September 1995

Per the August 22-25 working group meeting:
- Changed capacitance values in table 4.
- Modified cable configuration in clause 4.1 and figure 2.
- Removed 8-bit transfer mode.
- Added bibliography.
- Made LBA mandatory.
- Made READ, WRITE, and SET MULTIPLE mandatory.
- Removed single word DMA.
- Made READ and WRITE DMA mandatory.
- Inserted tables into command code definitions.
- Made SET FEATURES mandatory.
- Made numerous other changes requested during page-by-page review.

Revision 5 - 6 October 1995

Per the September 19-22 working group meeting:
- Added text to clause 6.2.
- Changed security mode definition to X3T10/95-329r0
- Added text to READ/WRITE LONG
- Changed protocol flowcharts to X3T10/95-330r1.
- Added X3T10/95-331r0 to clause 7.4.
- Deleted ACKNOWLEDGE MEDIA CHANGE, POST BOOT AND PRE BOOT COMMANDS.
- Added signal integrity annex C, (modified SFF 8036I)
- Made numerous other changes requested during page-by-page review.
- Made editorial changes requested by the ANSI editor for ATA-2 document.

Revision 6 - 26 October 1995

Per the October 17-19 working group meeting:
- Added command set supported, words 82-83, to IDENTIFY DEVICE response.
- Deleted Bxh codes for security mode.
- Made numerous other changes requested during page-by-page review.

Revision 7 - 25 April 1996

Resolution of letter ballot comments added per X3T13/D96112r2.

Revision 7a - 18 September 1996

Added editorial changes recommended by ANSI pre-edit.
Added public review comment restoring register transfer timing.

Revision 7b - 27 January 1997

Added X3 letter ballot comment changing DMARQ to DMACK- in clauses 5.2.2, 5.2.3, 5.2.4, 5.2.5, 5.2.6, 5.2.7, 5.2.8, 5.2.10, 5.2.11 and 5.2.12.

ANSI®
X3.298-1997

American National Standard
for Information Systems —

AT Attachment-3 Interface — (ATA-3)

Secretariat
Information Technology Industry Council

Approved mm dd yy

American National Standards Institute, Inc.

Abstract

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

This standard maintains a high degree of compatibility with the AT Attachment Interface with Extensions standard (ATA-2), X3.279-1996, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

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Approval of an American National Standard requires verification by ANSI that the requirements for due process, consensus, and other criteria for approval have been met by the standards developer. Consensus is established when, in the judgment of the ANSI Board of Standards Review, substantial agreement has been reached by directly and materially affected interests. Substantial agreement means much more than a simple majority, but not necessarily unanimity. Consensus requires that all views and objections be considered, and that effort be made towards their resolution.

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Foreword

(This foreward is not part of American National Standard X3.298-1997.)

This AT Attachment-3 Interface (ATA-3) standard is designed to maintain a high degree of compatibility with the AT Attachment Interface with Extensions standard (ATA-2), while providing the advantages of additional features and functions.

This standard was developed by the ATA/ATAPI ad hoc working group of X3T10 during 1994-1995. The standards approval process started in 1995. This document was transferred to X3T13 in January 1996. This document includes five annexes. Annex A is normative, and Annexes B to E are informative and are not considered part of the standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the X3 Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, X3. Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, the X3 Committee had the following members:

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Jeffrey L. Williams (Alt.)
Devon Worrell (Alt.)
Anthony Yang (Alt.)
Danny Yeung (Alt.)
Ruben Yomtoubian (Alt.)

Subcommittee X3T13 on ATA interfaces, which reviewed this standard, had the following members:

G. E. Milligan, Chairman

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John Masiewicz (Alt.)
James McGrath (Alt.)
Patrick Mercer (Alt.)
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Devon Worrell (Alt.)

Other ad hoc participants were:

Michael Aarans
Lyle Adams
Michael Alexenko
Joe Bennett
John Brooks
Peter Brown
Ian Davies
Pat Edsall
David Evans
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Takayuk Fujioka
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Daniel Wu
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Charles Yang
Mike Yokoyama

Introduction

This standard encompasses the following:

Clause 1 describes the scope.

Clause 2 provides definitions, abbreviations, and conventions used within this document.

Clause 3 contains the electrical and mechanical characteristics; covering the interface cabling requirements of the interface and DC cables and connectors.

Clause 4 contains the signal descriptions of the AT Attachment Interface.

Clause 5 contains descriptions of the registers of the AT Attachment Interface.

Clause 6 describes the general operating requirements of the AT Attachment Interface.

Clause 7 contains descriptions of the commands of the AT Attachment Interface.

Clause 8 contains an overview of the protocol of the AT Attachment Interface.

Clause 9 contains the interface timing diagrams.

AMERICAN NATIONAL STANDARD **X3.298-1997**

American National Standard
for Information Systems —

Information Technology
AT Attachment-3 Interface — (ATA-3)

1 Scope

2 Definitions, abbreviations, and conventions

2.1 Definitions and abbreviations

For the purposes of this American National Standard, the following definitions apply:

2.1.1 ATA (AT Attachment): ATA defines the physical, electrical, transport, and command protocols for the internal attachment of block storage devices.

2.1.2 ATA-1 device: A device which complies with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives (see annex D).

2.1.3 ATA-2 device: A device which complies with ANSI X3.279-1996, the AT Attachment Interface with Extensions (see annex D).

2.1.4 AWG: American Wire Gauge.

2.1.5 command acceptance: A command is considered accepted whenever the host writes to the Command Register and the device currently selected has its BSY bit equal to zero. An exception exists for the EXECUTE DIAGNOSTIC command (see 7.5).

2.1.6 CHS (cylinder-head-sector): This term defines the addressing of the device as being by cylinder number, head number, and sector number.

2.1.7 data block: This term describes a unit of data words transferred using PIO data transfer. A data block is transferred between the host and the device as a complete unit. A data block is a sector, except for data blocks of a READ MULTIPLE, WRITE MULTIPLE, READ LONG, and WRITE LONG commands. In the cases of READ MULTIPLE and WRITE MULTIPLE commands, the size of the data block may be changed in multiples of sectors by the SET MULTIPLE MODE command. In the cases of READ LONG and WRITE LONG, the size of the data block is a sector plus a vendor specific number of bytes. The default length of the vendor specific bytes associated with the READ LONG and WRITE LONG commands is four bytes, but may be changed by use of the SET FEATURES command.

2.1.8 device: Device is a storage peripheral. Traditionally, a device on the ATA interface has been a hard disk drive, but any form of storage device may be placed on the ATA interface provided it adheres to this standard.

2.1.9 device selection: A device is selected when the DEV bit of the Drive/Head register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal.

2.1.10 DMA (direct memory access): A means of data transfer between device and host memory without processor intervention.

2.1.11 LBA (logical block address): This term defines the addressing of the device as being by the linear mapping of sectors.

2.1.12 master: In ATA-1, Device 0 has also been referred to as the master. Throughout this document the term Device 0 is used.

2.1.13 PIO (programmed input/output): A means of accessing device registers. PIO is also used to describe one form of data transfers. PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.

2.1.14 reserved: Reserved bits, bytes, words, fields, and code values are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be set to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as an error.

2.1.15 sector: A uniquely addressable set of 256 words (512 bytes).

2.1.16 slave: In ATA-1, Device 1 has also been referred to as the slave. Throughout this document the term Device 1 is used.

2.1.17 S.M.A.R.T.: Self-Monitoring, Analysis, and Reporting Technology for prediction of device degradation and/or faults. Throughout this document this is noted as SMART.

2.1.18 unrecoverable error: An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one and the BSY bit to zero in the Status register when processing a command.

2.1.19 VS (vendor specific): This term is used to describe bits, bytes, fields, and values which are reserved for vendor specific purposes. These bits, bytes, fields, and values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE – Industry practice could result in conversion of a Vendor Specific bit, byte, field, or value into a defined standard value in a future standard.

2.2 Conventions

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, then text.

2.2.1 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality, as follows:

expected – A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

may – A keyword that indicates flexibility of choice with no implied preference.

shall – A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other standard conformant products.

should – keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

obsolete – A keyword indicating items that were defined in ATA-1 or ATA-2 but have been removed from this standard.

mandatory – A keyword indicating items to be implemented as defined by this standard.

optional – This term describes features which are not required by this standard. However, if any optional feature defined by the standard is implemented, it shall be done in the way defined by the standard. Describing a feature as optional in the text is done to assist the reader.

Lowercase is used for words having the normal English meaning. Certain words and terms used in this American National Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 2 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 2.2.4 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., Cylinder Low register).

2.2.2 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

2.2.3 Signal conventions

Signal names are shown in all uppercase letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates it is a low active signal. A low active signal is true when it is below V_{iL}, and is false when it is above V_{iH}. No dash at the end of a signal name indicates it is a high active signal. A high active signal is true when it is above V_{iH}, and is false when it is below V_{iL}.

Asserted means that the signal is driven by an active circuit to its true state. Negated means that the signal is driven by an active circuit to its false state. Released means that the signal is not actively driven to any state. Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal. These cases are noted under the description of the signal, and their released state is stated.

Control signals that may be used for two mutually exclusive functions are identified with their two names separated by a colon.

2.2.4 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true, and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero the meaning of the bit is true and when nBIT is set to one the meaning of the bit is false.

2.2.5 Byte ordering for data transfers

Assuming a block of data contains "n" bytes of information, and the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block, and Byte(n-1) is the last byte of the block. Table 1 shows the order the bytes shall be presented in when such a block of data is transferred on the interface.

Table 1 – Byte order

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (n-1)								Byte (n-2)							

NOTE – The above description is for data on the ATA Interface. Host systems and/or host adapters may cause the order of data, as seen in the memory of the host, to be different.

3 Interface physical and electrical requirements

Connectors are documented in annex A.

3.1 Cable configuration

Cable total length shall not exceed 0.46 m (18 in).

Cable capacitance shall not exceed 35 pf.

3.3 Electrical characteristics

Table 2 defines the DC characteristics of the interface signals. Table 3 defines the AC characteristics.

Table 2 – DC characteristics

Description		Min	Max
I_{oL}	Driver sink current (see note 1)	4 mA	
I_{oH}	Driver source current (see note 2)	400 µA	
V_{iH}	Voltage input high	2.0 V D.C.	
V_{iL}	Voltage input low		0.8 V D.C.
V_{oH}	Voltage output high (I_{oH} = -400 µA)	2.4 V D.C.	
V_{oL}	Voltage output low (I_{oL} = 12 ma)		0.5 V D.C.
NOTES – 1 I_{oL} for DASP shall be 12 mA minimum to meet legacy timing and signal integrity. 2 I_{oH} value at 400 µA is insufficient in the case of DMARQ which is typically pulled low by a 5.6 kΩ resistor.			

Table 3 – AC characteristics

Description		Min	Max
tRISE	Rise time for any signal on AT interface (see note)	5 ns	
tFALL	Fall time for any signal on AT interface (see note)	5 ns	
Cin	Host input capacitance		25 pf
Cout	Host output capacitance		25 pf
Cin	Device input capacitance		20 pf
Cout	Device output capacitance		20 pf
NOTE – tRISE and tFALL are measured from 10-90% of full signal amplitude with a total capacitive load of 40 pf.			

3.3.1 Driver types and required termination

Table 4 defines driver types and required termination. Annex C provides informative guidelines for signal termination.

Table 4 – Driver types and required termination

Signal	Source	Driver type (see note 1)	Host (see note 2)	Device (see note 2)	Notes
Reset	Host	TP			
DD (15:0)	Bidir	TS			3
DMARQ	Device	TS	5.6 kΩ PD		4
DIOR- DIOW-	Host	TS			
IORDY	Device	TS	1.0 kΩ PU		5
CSEL	Host		Ground	10 kΩ PU	6
DMACK-	Host	TP			
INTRQ	Device	TS			7
DA (2:0)	Host	TP			
PDIAG-	Device	TS		10 kΩ PU	
CS0- CS1-	Host	TP			
DASP-	Device	OC		10 kΩ PU	

NOTES –
1 TS=Tri-state; OC=Open Collector; TP=Totem-pole; PU=Pull-up; PD=Pull-down; VS=Vendor specific
2 All resistor values are minimum (lowest) allowed.
3 Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in a future revision of this standard.
4 This line shall be tri-stated whenever the device is not selected or is not executing a DMA data transfer. When enabled by DMA transfer, it shall be driven high and low by the device.
5 This signal should only be enabled during DIOR/DIOW cycles to the selected device.
6 When used as CSEL, this line is grounded at the Host and a 10 kΩ pull-up is required at both devices.
7 If the host uses a level sensitive interrupt controller a 10k pull-down or pull-up, depending upon the level sensed, may be required at the host.

4 Interface signal assignments and descriptions

4.1 Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Table 5 defines the signal names. For connector descriptions see annex A.

Table 5 – Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select	(see note)			CSEL
Chip select 0	→			CS0-
Chip select 1	→			CS1-
Data bus bit 0	↔			DD0
Data bus bit 1	↔			DD1
Data bus bit 2	↔			DD2
Data bus bit 3	↔			DD3
Data bus bit 4	↔			DD4
Data bus bit 5	↔			DD5
Data bus bit 6	↔			DD6
Data bus bit 7	↔			DD7
Data bus bit 8	↔			DD8
Data bus bit 9	↔			DD9
Data bus bit 10	↔			DD10
Data bus bit 11	↔			DD11
Data bus bit 12	↔			DD12
Data bus bit 13	↔			DD13
Data bus bit 14	↔			DD14
Data bus bit 15	↔			DD15
Device active or slave (Device 1) present	(see note)			DASP-
Device address bit 0	→			DA0
Device address bit 1	→			DA1
Device address bit 2	→			DA2
DMA acknowledge	→			DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read	→			DIOR-
I/O ready	←			IORDY
I/O write	→			DIOW-
Passed diagnostics	(see note)			PDIAG-
Reset	→			RESET-
NOTE – See signal descriptions for information on source of these signals				

4.2 Signal descriptions

4.2.1 CS0- (CHIP SELECT 0)

This is the chip select signal from the host used to select the Command Block registers. Table 6 defines its use.

4.2.2 CS1- (CHIP SELECT 1)

This is the chip select signal from the host used to select the Control Block registers. Table 6 defines its use.

4.2.3 DA2, DA1, and DA0 (DEVICE ADDRESS)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device. Table 6 defines this address.

4.2.4 DASP- (Device active, device 1 present)

This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. This signal shall be an open collector output and each device shall have a 10 kΩ pull-up resistor.

If the host connects to the DASP- signal for the illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the ATA interface for DASP- shall maintain V_{oH} and V_{oL} compatibility, given the I_{oH} and I_{oL} requirements of the DASP- device drivers.

4.2.5 DD (15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers.

4.2.6 DIOR- (Device I/O read)

This is the read strobe signal from the host. The falling edge of DIOR- enables data from the device onto the signals, DD (7:0) or DD (15:0). The rising edge of DIOR- latches data at the host and the host shall not act on the data until it is latched.

4.2.7 DIOW- (Device I/O write)

This is the Write strobe signal from the host. The rising edge of DIOW- latches data from the signals, DD (7:0) or DD (15:0), into the device. The device shall not act on the data until it is latched.

4.2.8 DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

4.2.9 DMARQ (DMA request)

This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

4.2.10 INTRQ (Device interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the nIEN bit in the Device Control register. If the nIEN bit is equal to one, or the device is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

The pending interrupt condition shall be set by:

- the completion of a command; or
- at the beginning of each data block to be transferred for PIO transfers except for the first data block for FORMAT TRACK, WRITE SECTOR(S), WRITE BUFFER, and WRITE LONG commands.

The pending interrupt condition shall be cleared by:

- assertion of RESET-; or
- the setting of the SRST bit of the Device Control register; or
- the host writing the Command register; or
- the host reading the Status register.

4.2.11 IOCS16- (Device 16-bit I/O)

Obsolete.

4.2.12 IORDY (I/O channel ready)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

If actively asserted, this signal shall only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

The use of IORDY is required for PIO modes 3 and above and otherwise optional.

4.2.13 PDIAG- (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. A 10 kΩ pull-up resistor shall be used on this signal by each device.

The host shall not connect to the PDIAG- signal.

4.2.14 RESET- (Device reset)

This signal from the host system shall be asserted beginning with the application of power and held asserted until at least 25 μs after voltage levels have stabilized within tolerance during power on and negated thereafter unless some event requires that the device(s) be reset following power on.

ATA devices shall not recognize a signal assertion shorter than 20 ns as a valid reset signal. Devices may respond to any signal assertion greater than 20 ns, and shall recognize a signal equal to or greater than 25 μs.

4.2.15 CSEL (Cable select)

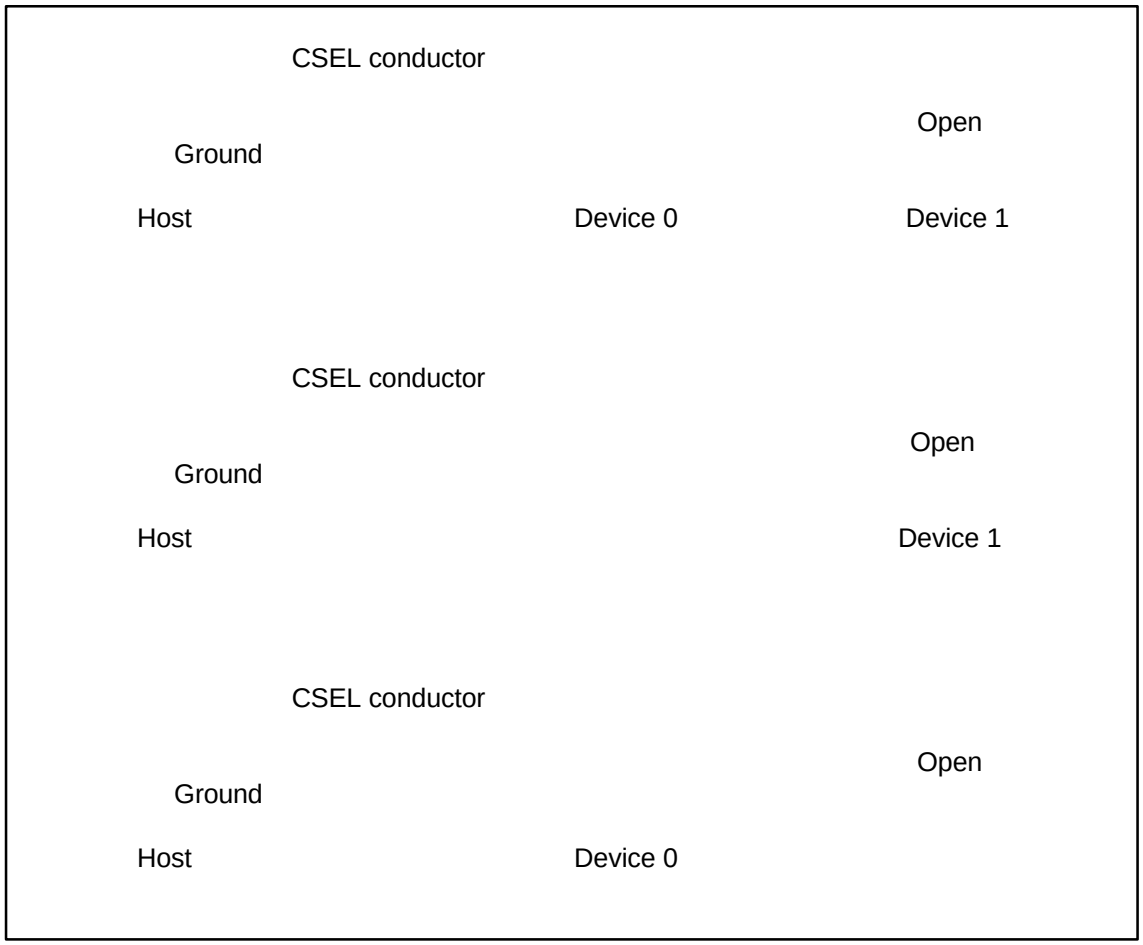
This signal shall have a 10 kΩ pull-up resistor at each device.

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL:

- If CSEL is negated then the device address is 0;
- If CSEL is asserted then the device address is 1.

CSEL shall be maintained at a steady level for at least 31 s after the negation of RESET-.

NOTE – Special cabling can be used by the system manufacturer to selectively ground CSEL e.g., CSEL of Device 0 is connected to the CSEL conductor in the cable, and is grounded, thus allowing the device to recognize itself as Device 0. CSEL of Device 1 is not connected to CSEL because the conductor is removed, thus the device can recognize itself as Device 1. Figure 2 shows possible configurations.



5 Interface register definitions and descriptions

5.1 Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers). The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisychained on the interface, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTICS command, only the selected device executes the command. On an EXECUTE DEVICE DIAGNOSTICS command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register (see 5.2.8). When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1.

5.2 I/O register descriptions

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR-, and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Anytime a command is in progress, that is, from the time the Command register is written until the device has completed the command and posted ending status, the device shall have either BSY or DRQ set to one. If the Command Block registers are read by the host when BSY or DRQ is set to one, the content of all register bits and fields except BSY and DRQ in the Status and Alternate Status registers is indeterminant. If the host writes to any Command Block register when BSY or DRQ is set to one, the results are indeterminant and may result in the command in progress ending with a command abort error.

When performing DMA transfers, BSY and DRQ shall both be cleared to zero within 400 ns of INTRQ assertion. This signals the completion of a DMA command.

When performing PIO transfers, BSY and DRQ shall both be cleared to zero within 400 ns of the transfer of the final byte of data. This assertion signals the completion of a PIO data transfer command.

Table 6 lists these registers and the addresses that select them.

Table 6 – I/O port functions and selection addresses

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	x	x	x	Data bus high impedence	Not used
					Control block registers	
N	A	0	x	x	Data bus high impedence	Not used
N	A	1	0	x	Data bus high impedence	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(see note 1)	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number LBA (7:0) (see note 2)	Sector Number LBA (7:0) (see note 2)
A	N	1	0	0	Cylinder Low LBA (15:8) (see note 2)	Cylinder Low LBA (15:8) (see note 2)
A	N	1	0	1	Cylinder High LBA (23:16) (see note 2)	Cylinder High LBA (23:16) (see note 2)
A	N	1	1	0	Device/Head LBA (27:24) (see note 2)	Device/Head LBA (27:24)(see note 2)
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, x = don't care
NOTES –
1 This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall not drive the DD7 signal to prevent possible conflict with floppy disk implementations.
2 Mapping of registers in LBA translation.

Each register description in the following clauses contain the following format:

ADDRESS - the CS and DA address of the register.

DIRECTION - indicates if the register is read/write, read only, or write only from the host.

ACCESS RESTRICTIONS - indicates when the register may be accessed.

EFFECT - indicates the effect of accessing the register.

FUNCTIONAL DESCRIPTION - describes the function of the register.

FIELD/BIT DESCRIPTION - describes the content of the register.

5.2.1 Alternate Status register

ADDRESS - CS(1:0)=1h, DA(2:0)=6h

5.2.2 Command register

ADDRESS - CS(1:0)=2h, DA(2:0)=7h

DIRECTION - This register is write-only. If this address is read by the host, the Status register is read.

ACCESS RESTRICTIONS - This register shall only be written when BSY and DRQ are both equal to zero and DMACK- is not asserted. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - Command processing begins when this register is written. The content of the Command Block registers become parameters of the command when this register is written. Writing this register clears any pending interrupt condition.

FUNCTIONAL DESCRIPTION - This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in clause 7.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Command Code							

5.2.3 Cylinder High register

ADDRESS - CS(1:0)=2h, DA(2:0)=5h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the high order bits of the starting cylinder address for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 23-16 of the LBA for any media access.

This register shall be updated to reflect the address of the first error when a media access command is unsuccessfully completed.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
Cylinder(15:8)							

LBA

7	6	5	4	3	2	1	0
LBA(23:16)							

5.2.4 Cylinder Low register

ADDRESS - CS(1:0)=2h, DA(2:0)=4h

DIRECTION - TQQQ‡

5.2.5 Data register

ADDRESS - CS(1:0)=2h, DA(2:0)=0h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written and the contents shall be valid on read only when DRQ is set to one and DMACK- is not asserted. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - PIO out data transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO in data transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a PIO in or a write during a PIO out are indeterminant.

FUNCTIONAL DESCRIPTION - The data register is 16-bits wide.

FIELD/BIT DESCRIPTION -

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

5.2.6 Data port

ADDRESS - None.

DIRECTION - This port is read/write.

ACCESS RESTRICTIONS - This port shall be written and the contents shall be valid on read only when DMACK- is asserted.

EFFECT - DMA out data transfers are processed by a series of reads to this port, each read transferring the data that follows the previous read. DMA in data transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a DMA in or a write during a DMA out are indeterminant.

FUNCTIONAL DESCRIPTION - The data port is 16-bits in width.

FIELD/BIT DESCRIPTION -

15	14	13	12	11	10	9	8
Data(15:8)							

5.2.7 Device Control register

ADDRESS - CS(1:0)=1h, DA(2:0)=6h

DIRECTION - This register is write only. If this address is read by the host, the Alternate Status register is read.

ACCESS RESTRICTIONS - This register shall only be written when DMACK- is not asserted.

EFFECTIVENESS - the content of this register shall take effect when written.

FUNCTIONAL DESCRIPTION - This register allows a host to software reset attached devices and enable/disable interrupts.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved;
- SRST is the host software reset bit (see 8.2);
- nIEN is the enable bit for the device interrupt to the host. When the nIEN bit is equal to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is equal to one, or the device is not selected, the INTRQ signal shall be in a high impedance state;
- Bit 0 shall be written with zero.

5.2.8 Device/Head register

ADDRESS - CS(1:0)=2h, DA(2:0)=6h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when BSY and DRQ equal zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - The DRV bit becomes becomes effective when this register is written. All other bits in this register become a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - This register selects the device, defines address translation as CHS or LBA, and provides the head address if CHS or LBA (27:24) if LBA.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
1	LBA	1	DEV	HS3	HS2	HS1	HS0

LBA

7	6	5	4	3	2	1	0
1	LBA	1	DEV	LBA(27:24)			

- Bit 7 shall be set to one for backward compatibility;

  NOTE – This bit may be reclaimed for use in a future ATA standard.

- LBA. When this bit is equal to zero, addressing is by CHS. When this bit is equal to one, addressing is by LBA;
- Bit 5 shall be set to one for backward compatibility;

  NOTE – This bit may be reclaimed for use in a future ATA standard.

- DEV is the device address. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected;
- Bit 3-0 If LBA is equal to zero (CHS), these contain the head address of the starting CHS address. The HS3 bit is the most significant bit. If LBA is equal to one (LBA), these bits contain bits 27 through 24 of the LBA. This field shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed (see 6.2).

5.2.9 Error register

ADDRESS - CS(1:0)=2h, DA(2:0)=1h

5.2.10 Features register

ADDRESS - CS(1:0)=2h, DA(2:0)=1h

DIRECTION - This register is write only. If this address is read by the host, the Error register is read.

ACCESS RESTRICTIONS - This register shall be written only when BSY and DRQ equal zero and DMACK- is not asserted. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - This register is command specific.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Command specific							

5.2.11 Sector Count register

ADDRESS - CS(1:0)=2h, DA(2:0)=2h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in this register is zero, a count of 256 sectors is specified.

For media access commands that complete with an error indication in the Status register, this register contains the number of sectors which need to be transferred in order to complete the request.

The contents of this register may be redefined on some commands.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Sector Count							

5.2.12 Sector Number register

ADDRESS - CS(1:0)=2h, DA(2:0)=3h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the starting sector number for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 7-0 of the LBA for any media access. This register is used by some non-media access commands to pass command specific information from the host to the device, or from the device to the host.

This register shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
Sector(7:0)							

LBA

7	6	5	4	3	2	1	0
LBA(7:0)							

5.2.13 Status register

ADDRESS - CS(1:0)=2h, DA(2:0)=7h

DIRECTION - This register is read only. If this address is written to by the host, the Command register is written.

ACCESS RESTRICTIONS - The contents of this register, except for BSY, shall be ignored when BSY is set equal to one. BSY is valid at all times. The contents of the this register and all other Command Block registers are not valid while a device is in the Sleep mode.

EFFECT - Reading this register when an interrupt is pending causes the interrupt to be cleared (see 4.2.10).

FUNCTIONAL DESCRIPTION - This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device. When the BSY bit is equal to zero, the other bits in this register are valid. When the BSY bit is equal to one, other bits in this register are not valid.

> NOTE – Although host systems might be capable of generating read cycles shorter than the 400 ns specified for status update following the last command or data cycle, host implementations should wait at least 400 ns before reading the Status register to insure that the BSY bit is valid.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

– BSY (Busy) is set whenever the device has control of the command Block Registers. When the BSY bit is equal to one, a write to a command block register by the host shall be ignored by the device.

The device shall not change the state of the DRQ bit unless the BSY bit is equal to one. When the last block of a PIO data in command has been transferred by the host, then the DRQ bit is cleared without the BSY bit being set.

When the BSY bit equals zero, the device may only change the IDX, DRDY, DF, DSC, and CORR bits in the Status register and the Data register. None of the other command block registers nor other bits within the Status register shall be changed by the device.

> NOTE – BIOSs and software device drivers that sample status as soon as the BSY bit is cleared to zero may not detect the assertion of the CORR bit by the device.

After the host has written the Command register either the BSY bit shall be set, or if the BSY bit is cleared, the DRQ bit shall be set, until command completion.

> NOTE – The BSY bit is set and then cleared so quickly, that host detection of the BSY bit being set is not certain.

The BSY bit shall be set by the device under the following circumstances:

> a) within 400 ns after either the negation of RESET- or the setting of the SRST bit in the Device Control register;

b) within 400 ns after writing the Command register if the DRQ bit is not set;

c) between blocks of a data transfer during PIO data in commands if the DRQ bit is not set;

d) after the transfer of a data block during PIO data out commands if the DRQ bit is not set;

e) during the data transfer of DMA commands if the DRQ bit is not set.

The device shall not set the BSY bit at any other time.

- DRDY (Device Ready) is set to indicate that the device is capable of accepting all command codes. This bit shall be cleared at power on. Devices that implement the power management features shall maintain the DRDY bit equal to one when they are in the Idle or Standby power modes. When the state of the DRDY bit changes, it shall not change again until after the host reads the Status register.

  When the DRDY bit is equal to zero, a device responds as follows:

  a) the device shall accept and attempt to execute the EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS commands;

  b) If a device accepts commands other than EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS during the time the DRDY bit is equal to zero, the results are vendor specific.

- DF (Device Fault) indicates a device fault error has been detected. The internal status or internal conditions that causes this error to be indicated is vendor specific.

- DSC (Device Seek Complete) indicates that the device heads are settled over a track. When an error occurs, this bit shall not be changed until the Status register is read by the host, at which time the bit again indicates the current Seek Complete status.

- DRQ (Data Request) indicates that the device is ready to transfer a word or byte of data between the host and the device.

- CORR (Corrected Data) is used to indicate a correctable data error. The definition of what constitutes a correctable error is vendor specific. This condition does not terminate a data transfer.

- IDX (Index) is vendor specific.

- ERR (Error) indicates that an error occurred during execution of the previous command. The bits in

6 General operational requirements

6.1 Reset response

There are three types of reset in ATA. The following is a suggested method of classifying reset actions:

- Power On Reset: the device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametrics, and sets default values (see 8.1);
- Hardware Reset: the device executes a series of electrical circuitry diagnostics, and resets to default values (see 8.1);
- Software Reset: the device resets the interface circuitry (see 8.2).

6.2 Sector addressing

All addressing of data sectors recorded on the device's media is by a logical sector address. The mapping of logical sector addresses to the actual physical location of the data sector on the media is vendor specific.

A device shall support at least one logical CHS translation known as the default translation if the device capacity is less than or equal to 16,515,072 sectors. The device shall enter this translation following a power-on reset. A device shall support LBA translation regardless of capacity. If the device capacity is equal to or greater than 16,515,072 sectors, the LBA translation shall be the default translation and the device shall enter this translation following a power-on reset. A device may support other logical translations if the device capacity is less than or equal to 16,515,072 sectors and the host may use the INITIALIZE DEVICE PARAMETERS command to select the translation. The default translation is described in the IDENTIFY DEVICE information. The current translation may also be described in the Identify Device information.

A CHS address is made up of three fields: the sector address, the head number and the cylinder number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation but can not exceed 255. Heads are numbered from 0 to the maximum value allowed by the current CHS translation but can not exceed 15. Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation but cannot exceed 65,535.

When the host selects a CHS translation using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested translation.

Sequential access to logical sectors shall be accomplished by treating the sector number as the least significant portion of the logical sector address, the head number as the middle portion of the logical sector address, and the cylinder number as the most significant portion of the logical sector address.

A device shall not change the addressing method and shall return status information utilizing the addressing method specified for the command.

The following LBA addressing methods shall be supported by the device:

a) The host may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the LBA bit in the Device/Head register;
b) The device shall support LBA addressing for all media access commands, except for the FORMAT TRACK command. Implementation of LBA addressing for the FORMAT TRACK command is vendor specific. The LBA bit of the Device/Head register shall be ignored for commands that do not access the media;
c) Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation currently in effect, the LBA address of a given logical sector does not change. The following is always true:

LBA = ((cylinder * heads_per_cylinder + heads) * sectors_per_track) + sector - 1

where heads_per_cylinder and sectors_per_track are the current translation values.

Annex B provides informative information for the implementation of devices with capacity below 8 GB.

6.3 Power management feature set

The optional Power Management Feature Set permits a host to modify the behavior of a device in a manner which reduces the power required to operate. The Power Management Feature Set provides a set of commands and a timer that enable a device to implement low power consumption modes. A device that implements the Power Management feature shall implement the following minimum set of functions:

a) A Standby timer;
b) IDLE command;
c) IDLE IMMEDIATE command;
d) SLEEP command;
e) STANDBY command;
f) STANDBY IMMEDIATE command.

Additional vendor specific commands and functions are allowed.

6.3.1 Power modes

In Active mode the device is capable of responding to commands. During the execution of a media access command a device shall be in Active mode. Power consumption is greatest in this mode.

In Idle mode the device is capable of responding to commands but the device may take longer to complete commands than when in the Active mode. Power consumption may be reduced from that of Active mode.

In Standby mode the device is capable of responding to commands but the device may take longer to complete commands than in the Idle mode. The time to respond could be as long as 30 s. Power consumption may be reduced from that of Idle mode.

In Sleep mode the device requires a reset to be activated. The time to respond could be as long as 30 s. Sleep provides the lowest power consumption of any mode.

6.3.2 Power management commands

The CHECK POWER MODE command allows a host to determine if a device is currently in, going to, or leaving Standby or Idle mode.

The IDLE and IDLE IMMEDIATE commands move a device to Idle mode immediately from the Active or Standby modes. The Idle command also sets the Standby Timer count and enables or disables the Standby Timer.

The SLEEP command moves a device to Sleep mode. The device's interface becomes inactive at the completion of the SLEEP command. A reset is required to move a device out of Sleep mode. When a device exits Sleep mode it may enter Active, Idle or Standby mode. The mode selected by the device is based on the type of reset received and on vendor specific implementation.

The STANDBY and STANDBY IMMEDIATE commands move a device to Standby mode immediately from the Active or Idle modes. The STANDBY command also sets the Standby Timer count and enables or disables the Standby Timer.

6.3.3 Standby timer

The Standby timer provides a method for the device to automatically enter Standby mode from either Active or Idle mode following a host programmed period of inactivity. If the Standby timer is enabled and if the device is in the Active or Idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the Standby mode.

If the Standby Timer is disabled, the device may not automatically enter Standby mode.

6.3.4 Idle mode transition

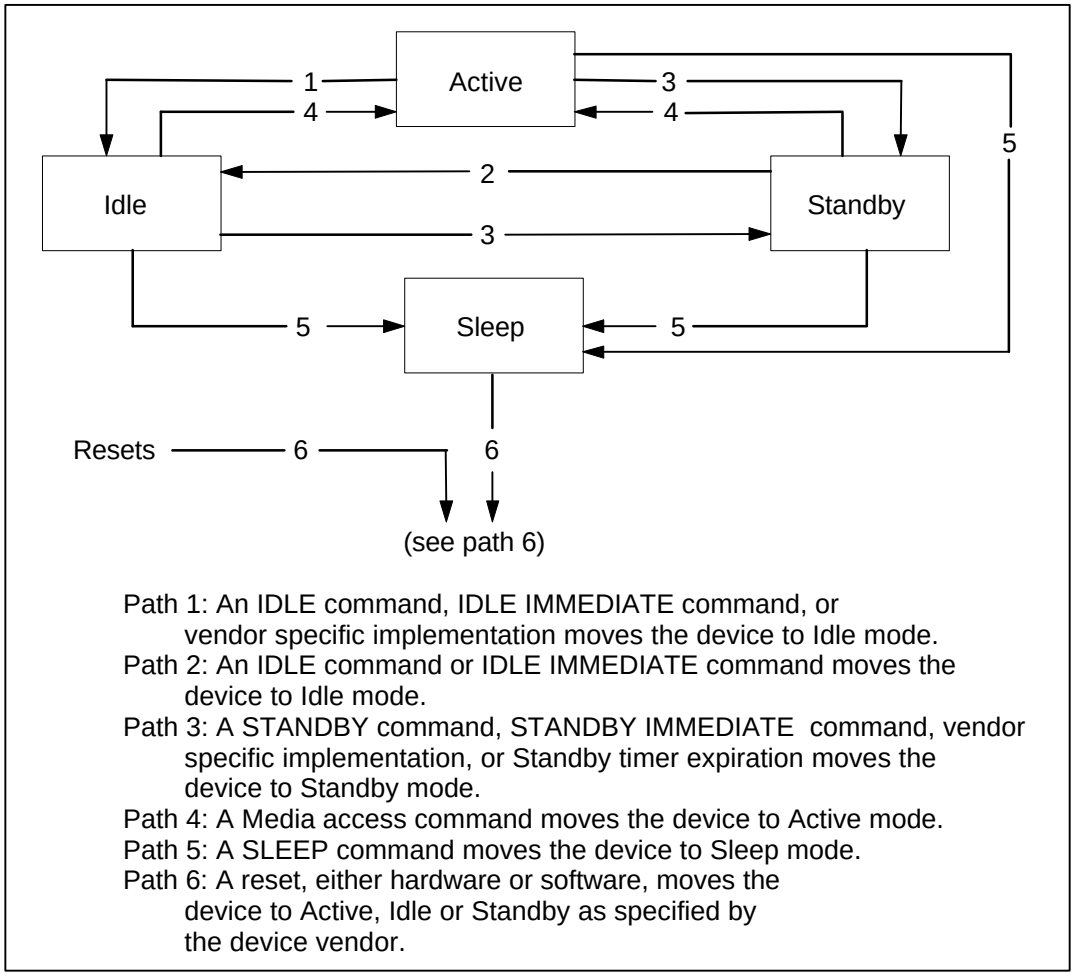
The transition to Idle mode is vendor specific, and may occur as a result of an IDLE or IDLE IMMEDIATE command, or in a vendor specific way.

6.3.5 Status

In Sleep mode, the device's interface is not active. The content of the Status register is invalid in this mode.

6.3.6 Power mode transitions

Figure 3 shows the minimum set of mode transitions that shall be implemented.

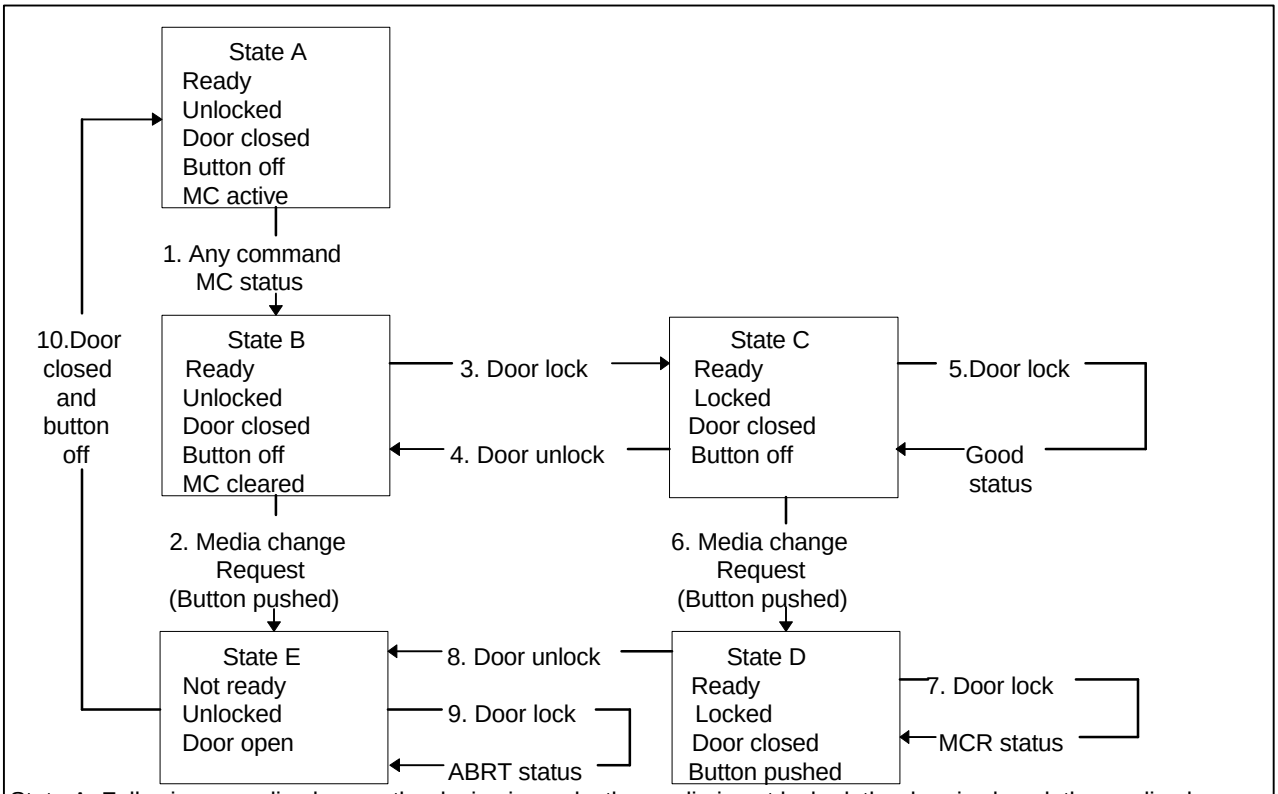


Path 1: An IDLE command, IDLE IMMEDIATE command, or vendor specific implementation moves the device to Idle mode.
Path 2: An IDLE command or IDLE IMMEDIATE command moves the device to Idle mode.
Path 3: A STANDBY command, STANDBY IMMEDIATE command, vendor specific implementation, or Standby timer expiration moves the device to Standby mode.
Path 4: A Media access command moves the device to Active mode.
Path 5: A SLEEP command moves the device to Sleep mode.
Path 6: A reset, either hardware or software, moves the device to Active, Idle or Standby as specified by the device vendor.

Figure 3 – Power management modes

6.4 Removable media mode transitions

Figure 4 shows the minimum set of mode transitions that shall be implemented by removable media devices which contain a media change request mechanism (button) and support the DOOR LOCK and DOOR UNLOCK commands, and the MC and MCR bits in the Error register.



State A: Following a media change, the device is ready, the media is not locked, the door is closed, the media change request button is not active and a media change has been detected.

Path 1: The first command following a media change shall be rejected with the MC bit set in the Error register and the ERR bit set in the Status register. The device shall then be moved to state B, the MC condition cleared and susequent commands accepted normally.

State B: In normal operation, the device is ready, the media is not locked, the door is closed, the media change request button is not active and the MC bit is off.

Path 2: Activating the media change request button shall cause the device to complete any pending operations, spin down the device, if needed, and move to state E, allowing media removal.

Path 3: A DOOR LOCK command shall lock the media and move the device to state C.

State C: In normal operation, the device is ready, the media is locked, the door is closed and the media change request button is not active.

Path 4: A DOOR UNLOCK command shall unlock the media and move the device to state B.

Path 5: A DOOR LOCK command shall return good status.

Path 6: Pushing the media change button shall move the device to state D.

State D: The device is ready, the media is locked, the door is closed and the media change button is active.

Path 7: A DOOR LOCK command shall return MCR status in the Error register and the ERR bit in the Status register. The device shall remain in state D..

Path 8: A DOOR UNLOCK command or a hard reset shall move the device to state E, allowing media removal.

State E: The device is not ready, the media is not locked and the door is open.

Path 9: A DOOR LOCK command shall return an ABRT error status.

Path 10: If the door is closed and the Media Change Button is inactive, the device shall move the device to state A (ready) and shall set the MC bit.

Note: A MEDIA EJECT command, while in states B, C, or D, will unlock the door or media , if locked, and cause the device to transition to state E (see 7.12).

Figure 4 – Removable modes

6.5 Security mode feature set

The Security mode features allow a host to implement a security password system to prevent unauthorized access to the internal disk drive.

The Commands supported by this feature set are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

Support of the Security mode feature set is indicated in IDENTIFY DEVICE response Word 128.

6.5.1 Security mode default setting

The Master Password shall be set to a vendor specific value during manufactuing and the lock function disabled.

The system manufacturer/dealer may set a new Master Password using the SECURITY SET PASSWORD command, without enabling or disabling the lock function.

6.5.2 Initial setting of the user password

When a user password is set, the device shall automatically enter lock mode the next time the device is powered-on or hardware reset.

6.5.3 Security mode operation from power-on or hardware reset

When lock is enabled, the device rejects media access commands until a SECURITY UNLOCK command is successfully completed. Figure 5 describes this behavior. Table 7 defines executable commands in each lock mode state.

6.5.4 User password lost

If the user password is lost and High level security is set, the device shall not allow the user to access data. The device shall be unlocked using the master password. Figure 6 describes this behavior.

If the user password is lost and Maximum security level is set, data access shall be impossible. However, the device shall be unlocked using the SECURITY ERASE UNIT command with the master password to unlock the device and shall erase all user data.

6.5.5 Attempt limit for SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit counter. The purpose of this counter is to defeat repeated trial attacks. After each failed user or master password SECURITY UNLOCK command, the counter is decremented. When the counter value reaches zero the EXPIRE bit (bit 4) of word 128 in the IDENTIFY DEVICE information is set, and the SECURITY UNLOCK and SECURITY UNIT ERASE commands are aborted until the device is powered off or hardware reset. The EXPIRE bit is cleared after power on or hardware reset. The counter is reset to five after a power on or hardware reset.

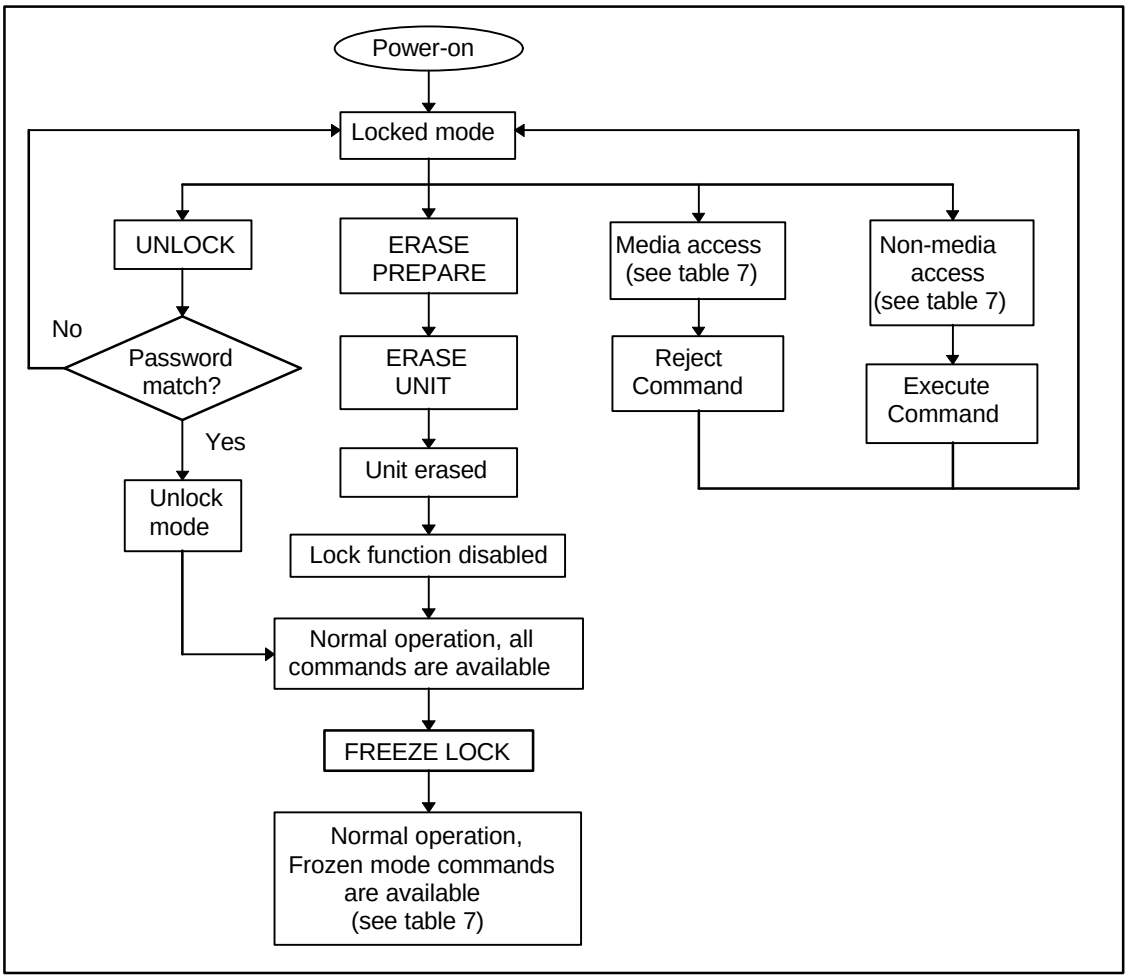


Figure 5 – Password set security mode power-on flow

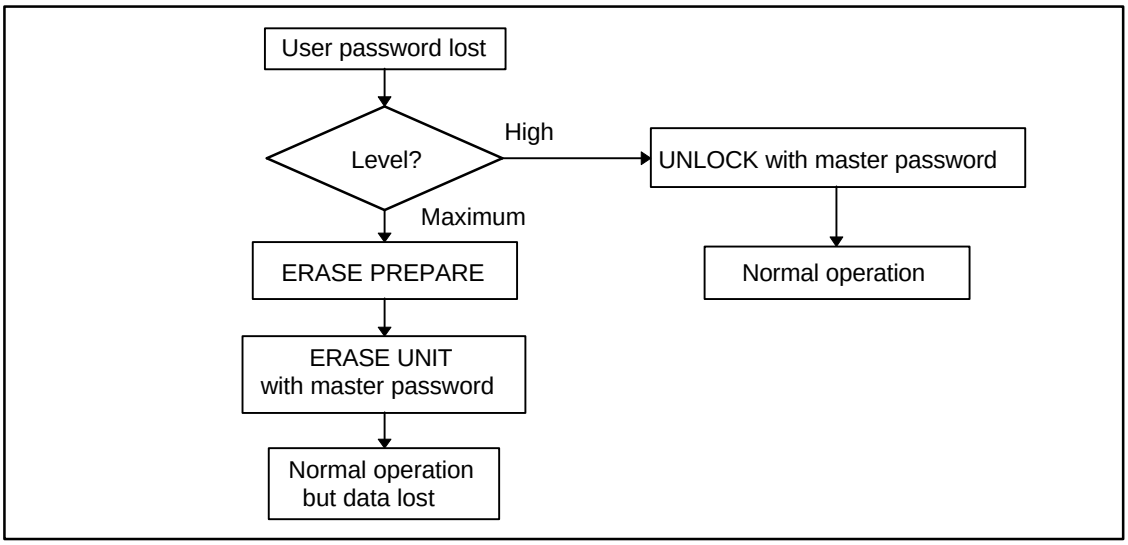


Figure 6 – User password lost

Table 7 – Security mode command actions

Command	Locked mode	Unlocked mode	Frozen mode
CHECK POWER MODE	Executable	Executable	Executable
DOOR LOCK	Executable	Executable	Executable
DOOR UNLOCK	Executable	Executable	Executable
DOWNLOAD MICROCODE	Executable	Executable	Executable
EXECUTE DEVICE DIAGNOSTICS	Executable	Executable	Executable
FORMAT TRACK	Aborted	Executable	Executable

6.6 Self-monitoring, analysis, and reporting technology

The intent of self-monitoring, analysis, and reporting technology (SMART) is to protect user data and minimize the liklihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition, allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in bit 0 of word 82 of the IDENTIFY DEVICE response.

6.6.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or fault conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

6.6.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or fault condition exisiting. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or fault condition existing.

6.6.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or fault condition. The numerical value of the attribute thresholds are determined by the device manufacturer tPhe sid

If the SMART feature set is implemented, the following commands may be implemented. These commands are not recommended and may be removed in a future ATA standard.

- SMART READ ATTRIBUTE THRESHOLDS
- SMART READ ATTRIBUTE VALUES
- SMART SAVE ATTRIBUTE VALUES

6.6.6 SMART operation with power management modes

It is recomended that, when used in a system that is utilizing the Power Management Feature set, a SMART enabled device automatically saves its attribute values upon receipt of an IDLE IMMEDIATE, STANDBY IMMEDIATE, or SLEEP command. If the device has been set to utilize the Standby timer, it is recommended that the device automatically perform a SMART SAVE ATTRIBUTE VALUES function prior to going from an Idle state to the Standby state.

7 Command descriptions

Commands are issued to the device by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command register.

Upon receipt of a command, the device sets the BSY bit or the DRQ bit within 400 ns. Following the setting of the BSY bit equal to one, or the BSY bit equal to zero and the DRQ bit equal to one, the status presented by the device depends on the type of command: PIO data in, PIO data out, non-data transfer, or DMA. See the individual command descriptions and clause 8 for the protocol followed by each command and command type.

NOTE – Some older host implementations may require the BSY bit being cleared to zero and the DRQ bit equal to one in the Status register within 700 ns of receiving some PIO data out commands.

NOTE – For the power mode related commands, it is recommended that the host utilize E0h through E3h, E5h, and E6h command values. While command values 94h through 99h command values are valid, they should be considered obsolete and may be removed in future versions of this standard.

Each command description in the following clauses contains the following subclauses:

COMMAND CODE - Indicates the command code for this command.

TYPE - Indicates if the command is:

- Mandatory - Required to be implemented by all devices as specified.
- Optional - Implementation is optional but if implemented shall be implemented as specified.
- Vendor specific - Implementation or certain implementation details are vendor specific.

If the command is a member of one or more feature sets, which feature sets it belongs to is noted.

PROTOCOL - Indicates which protocol is used by the command.

INPUTS - Describes the Command Block register data that the host shall supply.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Command	Command Code							

NOTE – No entry indicates register or bit not used by the device. If the register is written by the host, bits with no entry shall be written to zero.

NORMAL OUTPUTS - Describes the Command Block register data returned by the device at the end of a command. The Status register shall always be valid and, if the ERR bit in the Status register is set to one, then the Error register shall be valid.

ERROR OUTPUTS - Describes the Command Block register data that shall be returned by the device at the end of a command which completes with an unrecoverable error.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
NOTE – No entry indicates bit is not used. V indicates bit is valid.								

PREREQUISITES - Any prerequisite commands or conditions that shall be met before the command shall be issued.

DESCRIPTION - The description of the command function(s).

7.1 CHECK POWER MODE

COMMAND CODE - 98h or E5h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	98h or E5h							

NORMAL OUTPUTS - The Sector Count register shall be written with a value of 0 (00h) if the device is in Standby mode. The Sector Count register may be written with a value of 128 (80h) if the device is in Idle Mode. The Sector Count register may be written with a value of 255 (FFh) if the device is in Active mode.

ERROR OUTPUTS - Aborted Command if the device does not support the Power Management feature set.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - If the device is going to, in, or leaving the Standby Mode the device shall set the BSY bit, set the Sector Count register to 0 (00h), clear the BSY bit, and assert INTRQ.

If the device is in the Idle Mode, the device shall set BSY, shall set the Sector Count register to 128 (80h) or 255 (FFh), clear BSY, and assert INTRQ.

If the device is in Active Mode, the device shall set the BSY bit, may set the Sector Count register to 255 (FFh), clear the BSY bit, and assert INTRQ.

7.2 DOOR LOCK

COMMAND CODE - DEh

TYPE - Optional - Removable.

PROTOCOL - Non-data command.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	DEh							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device is not ready or is not capable of locking the media, the ABRT bit in the Error register and the ERR bit in the Status register shall be set to one.

If the device is already locked and the media change request button is active, then a Media Change Requested status shall be returned by setting the MCR bit to one in the Error register and the ERR bit in the Status register to one.

Status register				Error register					
DRDY	DF	CORR	ERR	UNC	IDNF	MCR	ABRT	TK0NF	AMNF
V	V		V			V	V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command either locks the device or media, or provides the status of the media change request button.

If the device is not locked, the device shall be set to the locked state and no error set.

If the device is locked, the status returned shall indicate the state of the media change request button. No error shall be set while the media change request button is not active, and the MCR bit in the Error register and the ERR bit in the Status register shall be set to one when the media change request button is active.

When a device is in a DOOR LOCKED state, the device shall not respond to the media change request button, except by setting the MCR bit to one, until the DOOR LOCKED condition is cleared. A DOOR LOCK condition shall be cleared by a DOOR UNLOCK or MEDIA EJECT command, or by a hardware device reset (see 6.4).

NOTE – Some caching controllers not reporting ATA-3 capability hang if issued this command.

7.3 DOOR UNLOCK

COMMAND CODE - DFh

TYPE - Optional - Removable.

PROTOCOL - Non-data command.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	DFh							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command or is not ready, the ABRT bit shall be set to one in the Error register and the ERR bit shall be set to one in the Status register.

Status register				Error register					
DRDY	DF	CORR	ERR	UNC	IDNF	MCR	ABRT	TK0NF	AMNF
V	V		V				V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command shall unlock the device, if it is locked, and shall allow the device to respond to the media change request button (see 6.4).

NOTE – Some caching controllers not reporting ATA-3 capability hang if issued this command.

7.4 DOWNLOAD MICROCODE

COMMAND CODE - 92h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The head bits of the Device/Head register shall always be set to zero. The Cylinder High and Low registers shall be set to zero. The Sector Number and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Sector count (low order)							
Sector Number	Sector count (high order)							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	1		1	D	0	0	0	0
Command	92h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support this command or did not accept the microcode data. Aborted error if subcommand code not a supported value.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number register and the Sector Count register. The Sector Number register shall be used to extend the Sector Count register, to create a sixteen bit sector count value. The Sector Number register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number register and the Sector Count register shall indicate no data is to be transferred. This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Feature Register are:

- 01h - download is for immediate, temporary use;
- 07h - save downloaded code for immediate and future use.

Either or both values may be supported. All other values are reserved.

7.5 EXECUTE DEVICE DIAGNOSTIC

COMMAND CODE - 90h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - None. The device selection bit in the Device/Head register is ignored.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Command	90h							

NORMAL OUTPUTS - The diagnostic code written into the Error register is an 8-bit code. Table 8 defines these values. The values are not as defined in 5.2.9.

Table 8 – Diagnostic codes

Code	Description
01h	Device 0 passed, Device 1 passed or not present
00h, 02h-7Fh	Device 0 failed, Device 1 passed or not present
81h	Device 0 passed, Device 1 failed
80h, 82h-FFh	Device 0 failed, Device 1 failed

c) Device 0 resets the Command Block registers to the following:

Cylinder Low	=	00h	Cylinder High	=	00h
Sector Count	=	01h	Device/Head	=	00h
Sector Number	=	01h			

d) Device 0 posts diagnostic results to bits 6-0 of the Error Register;

e) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 6 s from the time that the EXECUTE DEVICE DIAGNOSTIC command was received for Device 1 to assert PDIAG-. If PDIAG- is asserted within 6 s, Device 0 clears bit 7 to zero in the Error Register, or else Device 0 sets bit 7 equal to 1 in the Error Register.

If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 clears bit 7 to zero in the Error register;

f) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit within 6 s from the time that the EXECUTE DEVICE DIAGNOSTIC command was received;

g) Device 0 sets the DRDY bit when ready to accept any command.

NOTE – Steps (f) and (g) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one to occur, a host is advised to allow at least 30 s for the DRDY bit to be set to one. Figure 7 defines this timing.

Device 1 performs the following operations for this command:

a) Device 1 sets the BSY bit within 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;

b) Device 1 negates PDIAG- within 1 ms after the command is received;

c) Device 1 performs diagnostics;

d) Device 1 resets the Command Block registers to the following:

Cylinder Low	=	00h	Cylinder High	=	00h
Sector Count	=	01h	Device/Head	=	00h
Sector Number	=	01h			

e) Device 1 clears bit 7 of the Error register to zero and posts its diagnostic results to bits 6 through 0 of Error register;

f) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to one;

g) If Device 1 passed its diagnostics without error in step (c), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step;

NOTE – Device 1 shall clear the BSY bit and assert PDIAG- within 5 s of the time that the EXECUTE DEVICE DIAGNOSTIC command is received.

h) Device 1 sets the DRDY bit when ready to accept any command.

NOTE – Steps (f), (g), and (h) may occur at the same time. While no maximum time is specified for the DRDY bit to set to one, a host is advised to allow at least 30 s for the DRDY bit to be equal to one. Figure 7 defines this timing.

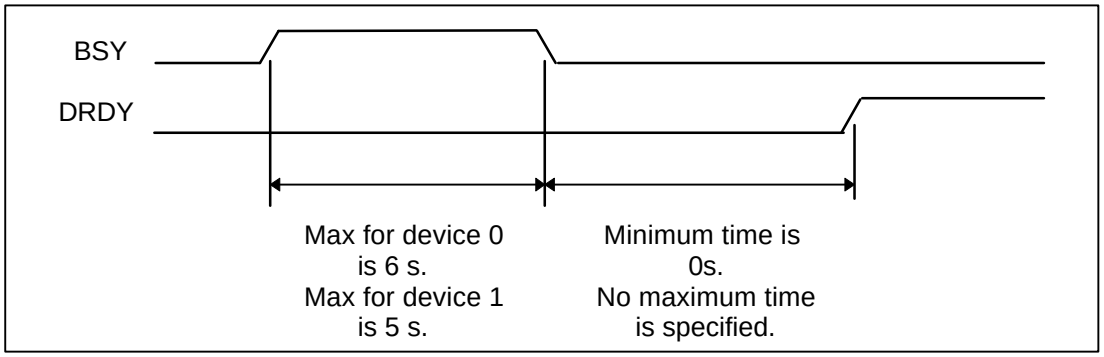


Figure 7 – BSY and DRDY timing for diagnostic command

7.6 FORMAT TRACK

COMMAND CODE - 50h

TYPE - Vendor specific.

PROTOCOL - Vendor specific.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features	Vendor specific							
Sector Count	Vendor specific							
Sector Number	Vendor specific							
Cylinder Low	Vendor specific							
Cylinder High	Vendor specific							
Device/Head	1		1	D				
Command	50h							

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Aborted Command if the device does not support this command. All other errors are vendor specific.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V	V	V	V	V	V

PREREQUISITES - DRDY set to one. Other prerequisites are vendor specific.

DESCRIPTION - The implementation of the FORMAT TRACK command is vendor specific. It is recommended that system implementations not utilize this command.

7.7 IDENTIFY DEVICE

COMMAND CODE - ECh

TYPE - Mandatory.

PROTOCOL - PIO data in.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	ECh							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - None.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V								

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host can then transfer the data by reading the Data register. Table 9 defines the arrangement and meanings of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a group of bits. A word which is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a sixteen bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32 bit values (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD (15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD (15:0) respectively.

Some parameters are defined as a string of ASCII characters. For the string “Copyright”, the character “C” is the first byte, “o” is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character (“C”) is on bits DD (15:8) of the first word;
the 2nd character (“o”) is on bits DD (7:0) of the first word;
the 3rd character (“p”) is on bits DD (15:8) of the second word;
the 4th character (“y”) is on bits DD (7:0) of the second word;
etc.

Table 9 – Identify device information

Word	F/V	
0		General configuration bit-significant information:
	F	15 0=ATA device
		1=ATAPI device
	F	14 Obsolete
	F	13 Obsolete
	F	12 Obsolete
	F	11 Obsolete
	F	10 Obsolete
	F	9 Obsolete
	F	8 Obsolete
	F	7 1=removable media device
	F	6 1=not removable controller and/or device
	F	5 Obsolete
	F	4 Obsolete
	F	3 Obsolete
	F	2 Obsolete
	F	1 Obsolete
	F	0 Reserved
1	F	Number of logical cylinders
2	R	Reserved
3	F	Number of logical heads
4	X	Obsolete
5	X	Obsolete
6	F	Number of logical sectors per logical track
7-9	X	Vendor specific
10-19	F	Serial number (20 ASCII characters)
20	X	Obsolete
21	X	Obsolete
22	F	Number of vendor specific bytes available on READ/WRITE LONG cmds
23-26	F	Firmware revision (8 ASCII characters)
27-46	F	Model number (40 ASCII characters)
47	X	15-8 Vendor specific
	R	7-0 00h =Reserved
	F	01h-FFh = Maximum number of sectors that can be transferred per interrupt on READ/WRITE MULTIPLE commands
48	R	Reserved

(continued)

Table 9 – Identify device information *(continued)*

Word	F/V		
49		Capabilities	
	R	15-14	Reserved
	F	13	1=Standby timer values as specified in this standard are supported
			0=Standby timer values are vendor specific
	R	12	Reserved (for advanced transfer mode)
	F	11	1=IORDY supported
			0=IORDY may be supported
	F	10	1=IORDY can be disabled
	R	9	Obsolete
	R	8	Obsolete
	X	7-0	Vendor specific
50	R	Reserved	
51	F	15-8	PIO data transfer cycle timing mode
	X	7-0	Vendor specific
52	R	15-8	Obsolete
	X	7-0	Vendor specific
53	R	15-2	Reserved
	F	1	1=the fields reported in words 64-70 are valid
	F		0=the fields reported in words 64-70 are not valid
	V	0	1=the fields reported in words 54-58 are valid
	V		0=the fields reported in words 54-58 may be valid
54	V	Number of current logical cylinders	
55	V	Number of current logical heads	
56	V	Number of current logical sectors per track	
57-58	V	Current capacity in sectors	
59	R	15-9	Reserved
	V	8	1=Multiple sector setting is valid
	V	7-0	xxh=Current setting for number of sectors that can be transferred per interrupt on R/W Multiple command
60-61	F	Total number of user addressable sectors (LBA mode only)	
62	R		Obsolete
63	V	15-8	Multiword DMA transfer mode active
	F	7-0	Multiword DMA transfer modes supported
64	R	15-8	Reserved
	F	7-0	Advanced PIO transfer modes supported
65		Minimum Multiword DMA transfer cycle time per word	
	F	15-0	Cycle time in nanoseconds
66		Manufacturer's recommended Multiword DMA transfer cycle time	
	F	15-0	Cycle time in nanoseconds
67		Minimum PIO transfer cycle time without flow control	
	F	15-0	Cycle time in nanoseconds
68		Minimum PIO transfer cycle time with IORDY flow control	
	F	15-0	Cycle time in nanoseconds
69-79	R	Reserved (for future command overlap and queuing)	

(continued)

Table 9 – Identify device information *(concluded)*

Word	F/V	
80	F	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA-14 13 Reserved for ATA-13 12 Reserved for ATA-12 11 Reserved for ATA-11 10 Reserved for ATA-10 9 Reserved for ATA-9 8 Reserved for ATA-8 7 Reserved for ATA-7 6 Reserved for ATA-6 5 Reserved for ATA-5 4 Reserved for ATA-4 3 1=supports ATA-3 2 1=supports ATA-2 1 1=supports ATA-1
81	F	Minor version number 0000h or FFFFh=device does not report version 0001h-FFFEh=see 7.7.37
82	F	Command set supported. If words 82 and 83 =0000h or FFFFh command set notification not supported. 15-4 Reserved 3 1=supports power management feature set 2 1=supports removeable feature set 1 1=supports security feature set 0 1=supports SMART feature set
83	F	Command sets supported. If words 82 and 83 =0000h or FFFFh command set notification not supported. 15 Shall be cleared to zero. 14 Shall be set to one 13-0 Reserved
84-127	R	Reserved
128	V	Security status 15-9 Reserved 8 Security level 0=High, 1=Maximum 7-5 Reserved 4 1=Security count expired 3 1=Security frozen 2 1=Security locked 1 1=Security enabled 0 1=Security supported
129-159	X	Vendor specific
160-255	R	Reserved

Key:
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word is vendor specific and may be fixed or variable.
R = the content of the word is reserved and shall be zero.

7.7.1 Word 0: General configuration

7.7.14 Words 27-46: Model number

7.7.21 Word 53: Field validity

If bit 0 of word 53 is set, then the values reported in words 54 through 58 are valid. If this bit is cleared, the values reported in words 54 through 58 may be valid. If bit 1 of word 53 is set, then the values reported in words 64 through 70 are valid. If this bit is cleared, the values reported in words 64-70 are not valid. Any device which supports PIO Mode 3 or above, or supports Multiword DMA Mode 1 or above, shall set bit 1 of word 53 and support the fields contained in words 64 through 70.

7.7.22 Word 54: Number of current logical cylinders

The number of user-addressable logical cylinders in the current translation mode.

NOTE – For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

7.7.23 Word 55: Number of current logical heads

The number of user-addressable logical heads per logical cylinder in the current translation mode.

NOTE – For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

7.7.24 Word 56: Number of current logical sectors per logical track

The number of user-addressable logical sectors per logical track in the current translation mode.

NOTE – For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

7.7.25 Word 57-58: Current capacity in sectors

The current capacity in sectors excludes all sectors used for device-specific purposes. The value reported in this field shall be the product of words 54, 55, and 56.

7.7.26 Word 59: Multiple sector setting

If bit 8 is set, then bits 7-0 reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. If word 47 bits 7-0 are zero then word 59 bits 8-0 shall also be zero. This field may be defaulted to the optimum value.

7.7.27 Word 60-61: Total number of user addressable sectors

These words reflect the total number of user addressable sectors in LBA translation. This value does not depend on the current device geometry

7.7.28 Word 62:Obsolete

7.7.29 Word 63: Multiword DMA transfer

The low order byte identifies by bit all of the Modes which are supported, e.g., if Mode 0 is supported, bit 0 is set to one. The high order byte contains a single bit set to indicate which mode is active supported, e.g., if Mode 0 is active, bit 0 is set to one.

7.7.30 Word 64: Flow control PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes it is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3. Bit 1, if set, indicates that the device supports PIO Mode 4.

> NOTE – For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

7.7.31 Word 65: Minimum multiword DMA transfer cycle time per word

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.7.32 Word 66: Device recommended multiword DMA cycle time

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the Device Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command over all locations on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.7.33 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer Without Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.7.34 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer With IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 68 shall not be less than the fastest PIO mode reported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

7.7.35 Words 69-79: Reserved

Words 69 through 79 are reserved for future command overlap and queuing.

7.7.36 Word 80: Major version number

If not 0000h or FFFFh, the device claims compliance with the major version(s) as indicated by bits 1 through 3 being equal to one. Values other than 0000h and FFFFh are bit significant. Since the ATA-3 and ATA-2 standards maintain downward compatibility with ATA-1 (published as ATA), it is allowed for an ATA-3 device to set all of bits 1 through 3 to one.

7.7.37 Word 81: Minor version number

If an implementor claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to this revision of the standard, Word 81 shall be 0000h or FFFFh.

Table 10 defines the value that may optionally be reported in Word 81 to indicate the revision of the standard which guided the implementation.

Table 10 – Minor version number

Value	Minor revision
0001h	ATA (ATA-1) X3T9.2 781D prior to revision 4
0002h	ATA-1 published, ANSI X3.221-1994
0003h	ATA (ATA-1) X3T9.2 781D revision 4
0004h	ATA-2 published, ANSI X3.279-1996
0005h	ATA-2 X3T10 948D prior to revision 2k
0006h	ATA-3 X3T10 2008D revision 1
0007h	ATA-2 X3T10 948D revision 2k
0008h	ATA-3 X3T10 2008D revision 0
0009h	ATA-2 X3T10 948D revision 3
000Ah	ATA-3 published, ANSI X3.298-1997
000Bh	ATA-3 X3T10 2008D revision 6
000Ch	ATA-3 X3T13 2008D revision 7
000Dh-FFFFh	Reserved

7.7.38 Words 82-83: Command sets supported

Words 82 and 83 indicate command sets supported. The values 0000h and FFFFh in these words indicate that command set support is not indicated. Bits 4 through 15 of Word 82 are reserved. Bits 0 through 13 of Word 83 are reserved. Bit 14 of Word 83 shall be set to one. Bit 15 of Word 83 shall be cleared to zero.

If bit 0 of Word 82 is set, the SMART feature set is supported.

If bit 1 of Word 82 is set, the security feature set is supported.

If bit 2 of Word 82 is set, the removable feature set is supported.

If bit 3 of Word 82 is set, the power management feature set is supported.

7.7.39 Words 84-127: Reserved.

7.7.40 Word 128: Security status

7.7.40.1 Security level

Bit 8 of Word 128 indicates the security level. If bit 8 is cleared to zero, the security level is high. If bit 8 is set to one, the security level is maximum. When security mode is disabled, bit 8 is cleared to zero.

7.7.40.2 Security count expired

Bit 4 of Word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are aborted until a power-on reset or hard reset.

7.7.40.3 Security frozen

Bit 3 of Word 128 indicates security frozen. If bit 3 is set to one, the security is frozen.

7.7.40.4 Security locked

Bit 2 of Word 128 indicates security locked. If bit 2 is set to one, the security is locked.

7.7.40.5 Security enabled

Bit 1 of Word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.

7.7.40.6 Security supported

Bit 0 of Word 128 indicates Security mode feature set is supported. If bit 0 is set to one, security is supported.

7.7.41 Words 129-159: Vendor specific.

7.7.42 Words 160-255: Reserved.

7.8 IDENTIFY DEVICE DMA

COMMAND CODE - EEh

TYPE - Optional.

PROTOCOL - DMA.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	EEh							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - None.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V								

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - The IDENTIFY DEVICE DMA command enables the host to receive parameter information from the device in DMA mode. The command transfers the same 256 words of device identification data as transferred by the IDENTIFY DEVICE command.

7.9 IDLE

COMMAND CODE - 97h or E3h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby Timer. Table 11 defines these values.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Timer period value							
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	97h or E3h							

7.10 IDLE IMMEDIATE

COMMAND CODE - 95h or E1h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	95h or E1h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management feature set.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Idle Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode (see 6.3).

7.11 INITIALIZE DEVICE PARAMETERS

COMMAND CODE - 91h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Sector Count register specifies the number of logical sectors per logical track, and the Device/Head register specifies the maximum head number.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Logical sectors per logical track							
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D	Max head			
Command	91h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support the requested CHS translation.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V							

PREREQUISITES - None.

DESCRIPTION - This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1 per logical cylinder for the current CHS translation mode.

Upon receipt of the command, the device sets the BSY bit, saves the parameters, clears the BSY bit, and generates an interrupt.

A device shall support the CHS translation described in words 1, 3, and 6 of the IDENTIFY DEVICE information. Support of other CHS translations is optional.

If the requested CHS translation is not supported, the device shall set the Error bit in the Status register and set the Aborted Command bit in the Error register before clearing the BSY bit in the Status register.

If the requested CHS translation is not supported, the device shall fail all media access commands with an ID Not Found error until a valid CHS translation is established.

7.12 MEDIA EJECT

COMMAND CODE - EDh

TYPE - Optional - Removable.

PROTOCOL - Non-data.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	EDh							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - If the device does not support this command, the device shall return a Command Abort error.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command completes any pending operations, spins down the device if needed, unlocks the door or media if locked, and initiates a media eject, if required.

7.13 NOP

COMMAND CODE - 00h

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	00h							

NORMAL OUTPUTS - The Command Block registers, other than the Error and Status registers, are not changed by this command. This command always fails with an Aborted Command error.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

ERROR OUTPUTS - None.

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command enables a host, which can only perform 16-bit register accesses, to check device status. The device shall respond, as it does to an unrecognized command, by setting Aborted Command in the Error register, Error in the Status register, clearing Busy in the Status register, and asserting INTRQ.

7.14 READ BUFFER

COMMAND CODE - E4h

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	E4h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one. A WRITE BUFFER command shall immediately precede a READ BUFFER command.

DESCRIPTION - The READ BUFFER command enables the host to read the current contents of the device's sector buffer. When this command is issued, the device sets the BSY bit, sets up the sector buffer for a read operation, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host then reads the data from the buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

7.15 READ DMA (with retries and without retries)

COMMAND CODE - C8h (with retries) or C9h (without retries)

TYPE - Mandatory.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number registers specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C8h or C9h							

ERROR OUTPUTS - An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V	V	V	V	V	V		V

PREREQUISITES - DRDY set equal to one. The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to the READ SECTOR(S) command except for the following:

- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a READ DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed.

Error recovery performed by the device either with or without retries is vendor specific.

7.16 READ LONG (with retries and without retries)

COMMAND CODE - 22h (with retries) or 23h (without retries)

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be read. The Sector Count register shall not specify a value other than one.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	01h							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	22h or 23h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V		V	V		V

PREREQUISITES - DRDY set equal to one. The SET FEATURES subcommand to enable more than 4 vendor specific bytes shall be executed prior to the READ LONG command if other than 4 vendor specific bytes are to be transferred. Additional prerequisites are vendor specific.

DESCRIPTION - The READ LONG command performs similarly to the READ SECTOR(S) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector. During a READ LONG command, the device does not check to determine if there has been a data error. Only single sector READ LONG operations are supported.

The transfer of the vendor specific bytes shall be 16 bit transfers with the vendor specific byte in bits 7 through 0. Bits 15 through 8 shall be ignored by the host. The host shall use PIO mode 0 when using this command.

Error recovery performed by the device either with or without retries is vendor specific.

> NOTE – The committee is considering removing READ LONG and WRITE LONG commands in a future ATA standard.

7.17 READ MULTIPLE

COMMAND CODE - C4h

TYPE - Mandatory.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C4h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V	V	V	V	V	V		V

PREREQUISITES - DRDY set equal to one. If bit 8 of Word 59 of the IDENTIFY DEVICE response is cleared to zero, a successful SET MULTIPLE MODE command shall precede a READ MULTIPLE command.

DESCRIPTION - The READ MULTIPLE command performs similarly to the READ SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command or the default if no intervening SET MULTIPLE command has been issued. Command execution is identical to the READ SECTOR(S) operation except that the number of sectors defined by a SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the READ MULTIPLE command. When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where n = remainder (sector count/ block count)

If the READ MULTIPLE command is attempted when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with an Aborted Command error.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error. Interrupts are generated when the DRQ bit is set at the beginning of each block or partial block.

7.18 READ SECTOR(S) (with retries and without retries)

COMMAND CODE - 20h (with retries) or 21h (without retries)

TYPE - Mandatory.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High								

7.19 READ VERIFY SECTOR(S) (with retries and without retries)

COMMAND CODE - 40h (with retries) or 41h (without retries)

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be verified. The Sector Count register specifies the number of sectors to be verified.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	40h or 41h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V	V	V	V	V	V		V

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command is identical to the READ SECTOR(S) command, except that the DRQ bit is never set, and no data is transferred to the host.

When the requested sectors have been verified, the device clears the BSY bit and generates an interrupt.

Error recovery performed by the device either with or without retries is vendor specific.

7.20 RECALIBRATE

COMMAND CODE - 10h

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	10h							

NORMAL OUTPUTS - If the command is executed in CHS addressing, Cylinder High, Cylinder Low, and the head portion of Device/Head shall be zero. The Sector Number register shall be 1. If the command is executed in LBA addressing, the Cylinder High, Cylinder Low, the head portion of the Device/Head, and the Sector Number register shall be zero.

ERROR OUTPUTS - If the device cannot reach cylinder 0, a Track 0 Not Found error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V	V	

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - The function performed by this command is vendor specific.

7.21 SECURITY DISABLE PASSWORD

COMMAND CODE - F6h

TYPE - Optional - Security mode feature set.

PROTOCOL - PIO data out.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	F6h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - Device returns Aborted command error if command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Status register	Error register

7.22 SECURITY ERASE PREPARE

COMMAND CODE - F3h

TYPE - Optional - Security mode feature set.

PROTOCOL - Non-data.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	F3h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - Device returns Aborted command error if command is not supported or the device is in Frozen mode.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - None.

DESCRIPTION - The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command is to prevent accidental erasure of the device.

7.23 SECURITY ERASE UNIT

COMMAND CODE - F4h

TYPE - Optional - Security mode feature set.

PROTOCOL - PIO data out.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	F4h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - Device returns Aborted command error if command is not supported or the device is in Frozen mode.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - This command must be immediately preceded by a SECURITY ERASE PREPARE command.

DESCRIPTION - This command requests to transfer a single sector of data from the host. Table 12 defines the content of this sector of information. If the password does not match then the device rejects the command with an Aborted error.

The SECURITY ERASE UNIT command erases all user data. The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device aborts the SECURITY ERASE UNIT command

This command disables the device lock function, however, the master password is still stored internally within the device and may be reactivated later when a new user password is set.

7.24 SECURITY FREEZE LOCK

COMMAND CODE - F5h

TYPE - Optional - Security mode feature set.

PROTOCOL - Non-data.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	F5h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - Device returns Aborted command error if command is not supported, or the device is in Locked mode.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - None

DESCRIPTION - The SECURITY FREEZE LOCK command sets the device to frozen mode. After this command is completed any other commands which update the device lock functions are rejected. Frozen mode is quit by power off or hardware reset. If SECURITY FREEZE LOCK is issued when the device is in frozen mode, the command executes and the device remains in frozen mode.

Commands disabled by SECURITY FREEZE LOCK are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT

7.25 SECURITY SET PASSWORD

COMMAND CODE - F1h

TYPE - Optional - Security mode feature set.

PROTOCOL - PIO data out.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	F1h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - Device returns Aborted command error if command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - None.

DESCRIPTION - This command requests a transfer of a single sector of data from the host. Table 13 defines the content of this sector of information. The data transferred controls the function of this command.

Table 13 – SECURITY SET PASSWORD data content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

Table 14 defines the interaction of the identifier and security level bits.

Table 14 – Identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new user password. The lock function shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by either the user password or the previously set master password.
User	Maximum	The password supplied with the command shall be saved as the new user password. The lock function shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the user password. The master password previously set is still stored in the device but shall not be used to unlock the device.
Master	High or Maximum	This combination shall set a master password but shall not enable or disable the lock function. The security level is not changed.

7.26 SECURITY UNLOCK

COMMAND CODE - F2h

TYPE - Optional - Security mode feature set.

PROTOCOL - PIO data out.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	F2h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - Device returns Aborted command error if command is not supported, or the device is in Frozen mode.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - None.

DESCRIPTION - This command requests to transfer a single sector of data from the host. Table 12 defines the content of this sector of information.

If the Identifier bit is set to master and the device is in high security level, then the password supplied shall be compared with the stored master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device compares the supplied password with the stored user password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT commands are aborted until a power-on reset or a hard reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

7.27 SEEK

COMMAND CODE - 70h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder High, Cylinder Low, head portion of the Device/Head register and the Sector Number register contain the sector address to which the device may move the read/write heads.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	70h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Error reporting is vendor specific.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V		V	V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - The function performed by this command is vendor specific, and may or may not affect the position of the read/write heads.

7.28 SET FEATURES

COMMAND CODE - EFh

TYPE - The command is mandatory.Each subcommand is optional.

PROTOCOL - Non-data.

INPUTS - Table 15 defines the value of the subcommand in the Feature register. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Subcommand specific							
Sector Number	Subcommand specific							
Cylinder Low	Subcommand specific							
Cylinder High	Subcommand specific							
Device/Head	1		1	D				
Command	EFh							

NORMAL OUTPUTS - See the subcommand descriptions.

ERROR OUTPUTS - If any subcommand input value is not supported or is invalid, the device posts an Aborted Command error.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - None.

DESCRIPTION - This command is used by the host to establish parameters which affect the execution of certain device features. Table 15 defines these features.

At power on, or after a hardware reset, the default setting of the functions specified by the subcommands are vendor specific.

Table 15 – SET FEATURES register definitions

Value (see note)	
01h	Obsolete
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register. Table 16 defines values.
04h	Enable all automatic defect reassignment
33h	Disable retry
44h	Length of vendor specific data appended on READ LONG/WRITE LONG commands
54h	Set cache segments to Sector Count register value
55h	Disable read look-ahead feature
66h	Disable reverting to power on defaults
77h	Disable ECC
81h	Obsolete
82h	Disable write cache
84h	Disable all automatic defect reassignment
88h	Enable ECC
99h	Enable retries
9Ah	Set device maximum average current
AAh	Enable read look-ahead feature
ABh	Set maximum prefetch using Sector Count register value
BBh	4 bytes of vendor specific data appended on READ LONG/WRITE LONG commands
CCh	Enable reverting to power on defaults
NOTE – All values not shown are reserved for future definition.	

7.28.1 Enable/disable write cache

Vendor specific subcommand codes 02h and 82h allow the host to enable or disable write cache in devices that implement write cache.

7.28.2 Set transfer mode

A host can choose the transfer mechanism by Set Transfer Mode, subcommand code 03h, and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. Table 16 defines these values.

Table 16 – Transfer/mode values

PIO default transfer mode	00000	000
PIO default transfer mode, disable IORDY	00000	001
PIO flow control transfer mode x	00001	nnn
Obsolete	00010	nnn
Multiword DMA mode x	00100	nnn
Reserved	01000	nnn
Reserved	10000	nnn
Key: nnn = a valid mode number in binary x = the mode number in decimal for the associated transfer type.		

If a device supports this standard, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000000b”, it shall set its default PIO transfer mode. If the value is “00000001b” and the device supports disabling of IORDY, then the device shall set its default PIO transfer mode and disable IORDY.

See vendor specification for the default mode of the commands which are vendor specific.

Devices reporting support for Multi Word DMA Transfer Mode 1 shall also support Multi Word DMA Transfer Mode 0. Support of IORDY is mandatory when PIO Mode 3 or above is the current mode of operation.

7.28.3 Enable/disable automatic defect reassignment

Vendor specific subcommand codes 04h and 84h allow the host to request the device to enable or disable automatic defect reassignment. Error recovery performed by the device with or without retries is vendor specific.

7.28.4 Enable/disable retries

Vendor specific subcommand codes 99h and 33h allow the host to request the device to enable or disable retries. Error recovery performed by the device with or without retries is vendor specific.

7.28.5 Vendor specific data appended

Subcommand code 44h allows the host to set the number of data bytes appended to the data transfer on READ LONG and WRITE LONG commands to the value set in the Sector Count register. Subcommand code BBh sets the number of data bytes appended to the data transfer on READ LONG and WRITE LONG commands to four bytes.

7.28.6 Set cache segments

Vendor specific subcommand code 54h allows the host to request the device to set the size of cache segments to the value in sectors placed in the Sector Count register. Error recovery performed by the device with or without retries is vendor specific.

7.28.7 Enable/disable read look-ahead

Subcommand codes AAh and 55h allow the host to request the device to enable or disable read look-ahead. Error recovery performed by the device with or without retries is vendor specific.

7.28.8 Enable/disable reverting to defaults

Subcommand codes CCh and 66h allow the host to enable or disable the device from reverting to power on default values. A setting of 66h allows settings of greater than 80h which may have been modified since power on to remain at the same setting after a software reset.

7.28.9 Enable/disable ECC

Vendor specific subcommand codes 77h and 88h allow the host to request the device to enable or disable ECC. Error recovery performed by the device with or without retries is vendor specific.

7.28.10 Set device current

To adjust the current the device draws, the host shall issue the Set Features command with the Features register set to 9Ah and the Sector Count register set to a current value which is equal to 4 mA times the value in the Sector Count register. If the device supports this feature, the device shall set its average operating current to the nearest supported current that does not exceed the specified current, where average operating current is defined as the maximum current required averaged over a period of one second. For example, if the Sector Count is set to 32 which is equivalent to 128 mA and the nearest possible current less than the selected current that the device can support is 100 mA, the device then shall set its average operating current to 100 mA.

A hard reset shall return the average operating current to the power default value which is vendor specific. A soft reset shall not return the average operating current to the power on default value.

However, if the selected current is less than the minimum value the device can support, the device shall switch to operate at its minimum current. For example, if the Sector count is set to 5 which is equivalent to 20 mA but the minimum device current is 50 mA, the device shall operate at its minimum value at 50 mA. If the host intends to operate at the device's lowest possible current, the Sector Count value shall be set to 1. Similarly, the device shall use its maximum operating current for any Sector Count value which is greater than the maximum current it can use.

At the completion of this command, the device shall update the Cylinder Low register with the minimum valid operating current of the device and the Cylinder High register with the maximum valid operating current. The host may use this minimum valid operating current returned in the Cylinder Low register to verify if the system can run that device.

Sector Count equal to zero is invalid. Therefore, this command allows the host to support a current range from 4 mA to 1020 mA.

If the device does not support this feature, it shall post an Aborted Command error.

7.28.11 Set maximum prefetch

Vendor specific subcommand code ABh allows the host to request the device to set the maximum prefetch to the value in sectors contained in the Sector Count register. Error recovery performed by the device with or without retries is vendor specific.

7.29 SET MULTIPLE MODE

COMMAND CODE - C6h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Sector Count register contains number of sectors per block to use on all following READ/WRITE MULTIPLE commands. The host shall set Sector Count values equal to 2, 4, 8, 16, 32, 64, or 128.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sectors per block							
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	C6h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - If a block count is not supported, a Aborted Command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set Equal to one.

DESCRIPTION - This command establishes the block count for READ MULTIPLE and WRITE MULTIPLE commands.

Devices shall support the block size specified in the IDENTIFY DRIVE parameter word 47, bits 7 through 0, and may also support smaller values.

Upon receipt of the command, the device sets the BSY bit equal to one and checks the Sector Count register. If the Sector Count register contains a valid value and the block count is supported, the value is used for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and their execution is enabled.

7.30 SLEEP

COMMAND CODE - 99h or E6h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	99h or E6h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management feature set.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command is the only way to cause the device to enter Sleep Mode.

This command causes the device to set the BSY bit, prepare to enter Sleep mode, clear the BSY bit, and assert INTRQ. The host shall read the Status register in order to clear the interrupt and allow the device to enter Sleep mode. In Sleep mode the interface becomes inactive without affecting the operation of the ATA interface. The host shall not attempt to access the Command Block registers while the device is in Sleep mode.

Because some host systems may not read the Status register and clear the interrupt, a device may automatically deassert INTRQ and enter Sleep mode after a vendor specific time period of not less than 2 s.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

A device shall not power on in Sleep Mode nor remain in Sleep Mode following a reset sequence.

7.31 SMART

7.31.1 SMART DISABLE OPERATIONS

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command shall be implemented.

PROTOCOL - Non-data command.

INPUTS - The Features register shall be set to D9h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command, if SMART is not enabled, or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V			V			V		

PREREQUISITES - DRDY set equal to one. SMART enabled.

DESCRIPTION - This command disables all SMART capabilities within the device including any and all timer functions related exclusively to this feature. After receipt of this command the device will disable all SMART operations. Attribute values will no longer be monitored or saved by the device. The state of SMART (either enabled or disabled) will be preserved by the device across power cycles.

Upon receipt of the SMART DISABLE OPERATIONS command from the host, the device sets BSY, disables SMART capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of this command by the device, all other SMART commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be aborted by the device (including SMART DISABLE OPERATIONS commands), returning the Aborted command error.

7.31.2 SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command shall be implemented.

PROTOCOL - Non-data command.

INPUTS - The Features register shall be set to D2h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h. The Sector Count register is set to 00h to disable attribute autosave and a value of F1h is set to enable attribute autosave.

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command, if SMART is disabled or if the values in

If this command is not supported by the device, the device shall abort the command upon receipt from the host, returning the Aborted command error.

During execution of the autosave routine the device shall not assert BSY nor deassert DRDY. If the device receives a command from the host while executing its autosave routine it must respond to the host within two seconds.

7.31.3 SMART ENABLE OPERATIONS

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command shall be implemented.

PROTOCOL - Non-data command.

INPUTS - The Features register shall be set to D8h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, an Aborted command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V			V			V		

PREREQUISITES -DRDY set equal to one.

DESCRIPTION - This command enables access to all SMART capabilities within the device. Prior to receipt of this command attribute values are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any of the attribute values.

Upon receipt of this command from the host, the device sets BSY, enables SMART capabilities and functions, clears BSY, and asserts INTRQ.

7.31.4 SMART READ ATTRIBUTE THRESHOLDS

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command is optional and not recommended.

PROTOCOL - PIO data in.

INPUTS - The Features register shall be set to D1h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D1h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command, if SMART disabled or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, an Aborted command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V			V			V		

PREREQUISITES - DRDY set equal to one. SMART enabled.

DESCRIPTION - This command returns the device's attribute thresholds to the host. Upon receipt of this command from the host, the device sets BSY, reads the attribute thresholds from non-volitile memory, sets DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of attribute threshold information from the device via the Data register.

Table 17 defines the 512 bytes that make up the attribute threshold information. All multi-byte fields shown in these data structures follow the byte ordering specified in 2.2.5.

The sequence of active attribute thresholds must appear in the same order as their corresponding attribute values (see 7.31.5).

The data structure revision number shall be the same value used in the device attribute values data structure.

Table 18 defines the 12 bytes that make up the information for each threshold entry in the device attribute thresholds data structure. Attribute entries in the individual threshold data structure must be in the same order and correspond to the entries in the individual attribute data structure.

The data structure checksum is the two's compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

Table 17 – Device attribute thresholds data structure

Description	Bytes	Format	Type
Data structure revision number = 0x0004h for this revision	2	binary	Rd only
1st attribute threshold	12	(Table 18)	Rd only
.....			
.....			
.....			
30th attribute threshold	12	(Table 18)	Rd only
reserved (0x00)	18		Rd only
Vendor specific	131		Rd only
Data structure checksum	1		Rd only
Total bytes	512		

Table 18 – Individual threshold data structure

Description	Bytes	Format	Type
Attribute ID number	1	binary	Rd only
Attribute threshold (for comparison with attribute values from 0x00 to 0xFFh)	1	binary	Rd only
0x00 "always passing" threshold value to be used for code test purposes			
0x01 minimum value for normal operation			
0xFD maximum value for normal operation			
0xFE invalid for threshold value - not to be used			
0xFF "always failing" threshold value to be used for code test purposes			
Reserved	10		Rd only
Total bytes	12		

7.31.5 SMART READ ATTRIBUTE VALUES

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command is optional and not recommended.

PROTOCOL - PIO data in.

INPUTS - The Features register shall be set to D0h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V			V			V		

PREREQUISITES - DRDY set equal to one. SMART enabled.

DESCRIPTION - This command returns the device's attribute values to the host. Upon receipt of this command from the host, the device sets BSY, saves any updated attribute values to non-volitile memory, sets DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of attribute value information from the device via the Data register.

Table 19 defines the 512 bytes that make up the attribute value information. All multi-byte fields shown in these data structures follow the byte ordering described in 2.2.5.

The number of active attributes and, therefore, the number of active attribute values is determined independently by the device manufacturer for each individual device. All active attribute entries should be concatenated together directly after the data structure revsion number. If there are fewer than thirty active attributes implemented on a device, the excess locations in the data structure are reserved for future attribute implementations and are designated as blanks containing the value 0x00h. Thus the first reserved byte following the attribute entries shall be the 363rd byte in the structure, the first SMART capability byte shall be the 369th byte in the structure, etc.

The data structure revision number identifies which version of this data structure is implemented by a device. Upon initial release of this specification, the revision number will be set to 0x0004h. Later revisions, if any, will increment the revision number by one for each new revision. The revision number will be the same for both the attribute value and attribute threshold structures.

Table 20 defines the 12 bytes that make up the information for each attribute entry in the device attibutes data stucture.

Table 19 – Device attributes data structure

Description	Bytes	Format	Type
Data structure revision number = 0x0004 for this specification revision	2	binary	Rd only
1st device attribute	12	Table 20	Rd/Wrt
...			
...			
...			
30th device attribute	12	Table 20	Rd/Wrt
reserved (0x00)	6		Rd only
SMART capability	2		Rd only
reserved (0x00)	16		Rd/Wrt
Vendor specific	125		Rd only
Data stucture checksum	1		Rd only
Total bytes	512		

Table 20 – Individual attribute data structure

Description	Bytes	Format	Type
Attribute ID number (0x01 to 0xFFh)	1	binary	Rd only
Status flags	2	bit flags	Rd only
Pre-failure/advisory bit			
Vendor specific (5 bits)			
reserved (10 bits)			
Attribute value (valid values from 0x01 to 0xFEh)	1	binary	Rd only
0x00 invalid for attribute value - not to be used			
0x01 minimum value			
0x64 initial value for all attributes prior to any data collection			
0xFD maximum value			
0xFE value is not valid			
0xFF invalid for attribute value - not to be used			
Vendor specific	8	binary	Rd only
Total bytes	12		

The attribute ID numbers and their definitions are vendor specific. Any non-zero value in the attribute ID number indicates an active attribute. Valid values for this byte are from 0x01 through 0xFFh.

Status flag

- Bit 0 -Pre-failure/advisory - If the value of this bit equals zero, an attribute value less than or equal to its corresponding attribute threshold indicates an advisory condition where the usage or age of the device has exceeded its intended design life period. If the value of this bit equals one, an atribute value less than or equal to its corresponding attribute threshold indicates a pre-failure condition where imminent loss of data is being predicted.

- Bit 1 Reserved for future use.

- Bits 3 - 6 - Vendor specific.
- Bits 7 - 15 - Reserved for future use.

Table 20 describes the range and meaning of the attribute values. Prior to the monitoring and saving of attribute values, all values are set to 0x64h. The attribute values of 0x00h and 0xFFh are reserved and should not be used by the device.

SMART capability

- Bit 0 - Pre-power mode attribute saving capability - If the value of this bit equals one, the device will save its attribute values prior to going into a power saving mode (Idle, Standby, or Sleep modes).

- Bit 1 - Attribute autosave after event capability - If the value of this bit is equal to one, the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE comand.

- Bits 2-15 - Reserved for future use.

The data structure checksum is the two’s compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

7.31.6 SMART RETURN STATUS

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command shall be implemented.

PROTOCOL -Non-data command.

INPUTS - The Features register shall be set to DAh. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	DAh							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - If the device has not detected a thrshold exceeded condition, the device sets the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If the device has detected a threshold exceeded condition, the device sets the Cylinder Low register to F4h and the Cylinder High register to 2Ch.

ERROR OUTPUTS - If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, an Aborted command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V			V			V		

PREREQUISITES - DRDY set equal to one. SMART enabled.

DESCRIPTION - This command is used to communicate the reliability status of the device to the host at the host's request. Upon receipt of this command the device sets BSY, saves any updated attribute values to non-volatile memory, and compares the updated attribute values to the attribute thresholds.

7.31.7 SMART SAVE ATTRIBUTE VALUES

COMMAND CODE - B0h

TYPE - Optional - SMART Feature set. If the SMART feature set is implemented, this command is optional and not recommended.

PROTOCOL -Non-data command.

INPUTS - The Features register shall be set to D3h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D3h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1		1	D				
Command	B0h							

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, an Aborted command error is posted.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V			V			V		

PREREQUISITES - DRDY set equal to one. SMART enabled.

DESCRIPTION - This command causes the device to immediately save any updated attribute values to the device's non-volatile memory regardless of the state of the attribute autosave timer. Upon receipt of this command from the host, the device sets BSY, writes any updated attribute values to non-volatile memory, clears BSY, and asserts INTRQ.

7.32 STANDBY

COMMAND CODE - 96h or E2h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby Timer. Table 11 defines these values.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Time period value							
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	96h or E2h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support the Power Management feature set.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Standby Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

7.33 STANDBY IMMEDIATE

COMMAND CODE - 94h or E0h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	94h or E0h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management feature set.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Standby Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

7.34 WRITE BUFFER

COMMAND CODE - E8h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS -

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head	1		1	D				
Command	E8h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V			V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command enables the host to overwrite the contents of one sector in the device's buffer. When this command is issued, the device sets the BSY bit, sets up the buffer for a write operation, sets the DRQ bit, clears the BSY bit, and waits for the host to write the data. Once the host has written the data, the device sets the BSY bit, clears the BSY bit, and generates an interrupt.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

7.35 WRITE DMA (with retries and without retries)

COMMAND CODE - CAh (with retries) or CBh (without retries).

TYPE - Mandatory.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	CAh or CBh							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V		V	V		

PREREQUISITES - DRDY set equal to one. The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to WRITE SECTOR(S) except for the following:

- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a WRITE DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed.

Error recovery performed by the device either with or without retries is vendor specific.

7.36 WRITE LONG (with retries and without retries)

COMMAND CODE - 32h (with retries) or 33h (without retries)

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register shall not specify a value other than one.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	01h							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	32h or 33h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V		V	V		

PREREQUISITES - The SET FEATURES subcommand to enable other than 4 vendor specific bytes shall be executed prior to the WRITE LONG command if other than 4 vendor specific bytes are to be transferred. Additional prerequisites are vendor specific.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command except that it writes the data and the vendor specific bytes as supplied by the host; the device does not generate the vendor specific bytes itself. Only single sector Write Long operations are supported.

The transfer of the vendor specific bytes shall be 16 bit transfers with the vendor specific byte in bits 7 through 0. Bits 15 through 8 shall be ignored by the host.. The host shall use PIO mode 0 when using this command.

Error recovery performed by the device either with or without retries is vendor specific.

NOTE – The committee is considering removing the READ LONG and WRITE LONG commands in a future ATA standard.

7.37 WRITE MULTIPLE

COMMAND CODE - C5h

TYPE - Mandatory.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C5h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminent.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V		V	V		

PREREQUISITES - DRDY set equal to one. If bit 8 of Word 59 in the IDENTIFY DEVICE response is equal to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block that contains the number of sectors defined by SET MULTIPLE MODE or the default if no intervening SET MULTIPLE command has been issued.

Command execution is identical to the WRITE SECTOR(S) operation except that the number of sectors defined by the SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is the default or programmed by the SET MULTIPLE MODE command, which shall be executed prior to the WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = Remainder (sector count/ block count).

If the WRITE MULTIPLE command is attempted when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with an Aborted Command error.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The Write command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupts are generated when the DRQ bit is set at the beginning of each block or partial block.

7.38 WRITE SECTOR(S) (with retries and without retries)

COMMAND CODE - 30h (with retries) or 31h (without retries)

TYPE - Mandatory.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	30h or 31h							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V		V		V	V		

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

7.39 WRITE VERIFY

COMMAND CODE - 3Ch

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head, and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	3Ch							

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Status register				Error register				
DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
V	V	V	V	V	V	V		V

PREREQUISITES - DRDY set equal to one.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

8 Protocol

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if the BSY bit is equal to one, and should proceed no further unless and until the BSY bit is equal to zero. For most commands, the host shall also wait for the DRDY bit to be equal to one before proceeding. The commands shown with DRDY=x can be executed when the DRDY bit is equal to zero.

Data transfers may be accomplished in more ways than are described below, but these sequences should work with all known implementations of ATA devices.

A device shall maintain either the BSY bit equal to one or the DRQ bit equal to one at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from one to zero during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while the BSY bit is equal to one or the DRQ bit is equal to one is unpredictable and may result in data corruption.

8.1 Power on and hardware resets

This clause describes the algorithm and timing relationships for Devices 0 and 1 during the processing of power on and hardware resets.

The timing assumes the following:

a) DASP- is asserted by Device 1 and received by Device 0 at power-on or hardware reset to indicate the presence of Device 1. At all other times it is asserted by Device 0 or Device 1 to indicate when a device is active;
b) PDIAG- is asserted by Device 1 and detected by Device 0. It is used by Device 1 to indicate to Device 0 that it has completed diagnostics without error and is ready to accept commands from the Host (BSY bit is cleared). This does not indicate that the device is ready, only that it can accept commands.

8.1.1 Power on and hardware resets – Device 0

a) Host asserts RESET- for a minimum of 25 μs;
b) Device 0 sets the BSY bit no later than 400 ns after RESET- is negated;
c) Device 0 negates DASP- no later than 1 ms after RESET- is negated;
d) Device 0 samples for at least 450 ms for DASP- to be asserted from Device 1. This sampling starts 1 ms after RESET- is negated;
e) Device 0 performs hardware initialization and diagnostics;
f) Device 0 may revert to its default condition;
g) If Device 0 detected that DASP- was asserted during step (d), then Device 0 waits up to 31 s for Device 1 to assert PDIAG-. Sampling of PDIAG- starts 1 ms after RESET is negated. If PDIAG- is asserted within 31 s, Device 0 clears bit 7 equal to zero in the Error Register, else Device 0 sets bit 7 equal to one in the Error Register. If DASP- assertion was not detected in step (d) Device 0 clears bit 7 equal to zero in the Error Register. In either case the device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h. Device 0 shall store whether or not Device 1 was detected in step (d) because this information is needed in order to process any Software reset or EXECUTE DEVICE DIAGNOSTIC command later;

h) Device 0 posts diagnostic results to bits 6-0 of the Error Register;
i) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit no later than 31 s from the time that RESET- is negated;
j) Device 0 sets the DRDY bit when ready to accept any command.

NOTE – Steps (i) and (j) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one, a host should allow up to 30 s for the DRDY bit to become 1. Figure 8 defines this timing.

8.1.2 Power on and hardware resets – Device 1

a) Host asserts RESET- for a minimum of 25 μs;
b) Device 1 sets the BSY bit no later than 400 ns after RESET- is negated;
c) Device 1 negates DASP- no later than 1 ms after RESET- is negated;
d) Device 1 negates PDIAG- before asserting DASP-;
e) Device 1 asserts DASP- no later than 400 ms after RESET- is negated;
f) Device 1 performs hardware initialization and diagnostics;
g) Device 1 may revert to its default condition;
h) Device 1 posts diagnostic results to the Error Register;
i) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1;
j) If Device 1 passed its diagnostics without error in step (f), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step. Device 1 shall clear the BSY bit, and optionally assert PDIAG-, no later than 30 s from the time RESET- is negated. The device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h;
k) Device 1 sets the DRDY bit when ready to accept any command;

NOTE – Steps (i), (j) and (k) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one, a host should allow up to 30 s for the DRDY bit to become 1. Figure 8 defines this timing.

l) Device 1 negates DASP- after the first command is received or negates DASP- if no command is received within 31 s after RESET- is asserted.

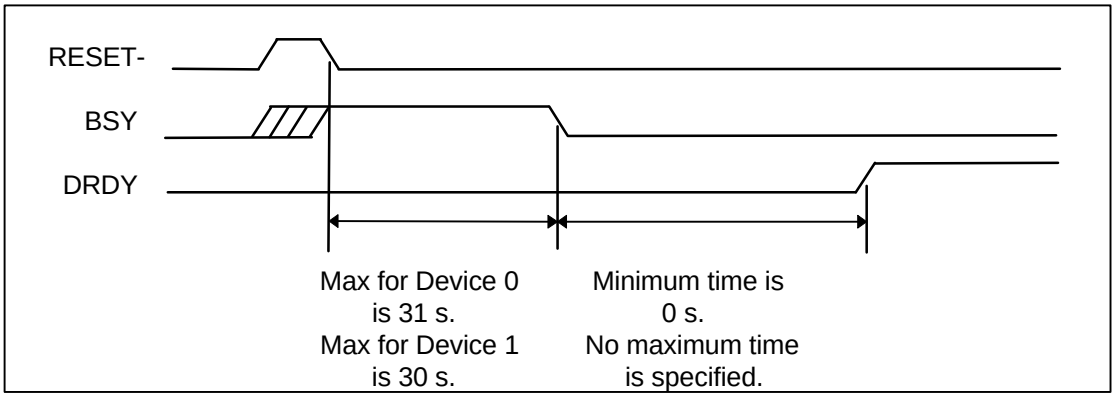


Figure 8 – BSY and DRDY timing for power on and hardware resets

8.2 Software reset

This clause describes the algorithm and timing relationships for Devices 0 and 1 during the processing of software resets.

NOTE – Some devices may require SRST be set for a minimum of 5 μs.

8.2.1 Software reset – Device 0

a) Host sets the SRST bit to one in the Device Control register;
b) Device 0 sets BSY bit no later than 400 ns after detecting that the SRST bit is equal to one;
c) Device 0 performs hardware initialization and diagnostics;
d) Device 0 may revert to its default condition;
e) Device 0 posts diagnostic results to the Error Register;
f) Device 0 waits for the host to clear the SRST bit to zero;
g) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 31 s from the time that the SRST bit to become zero for Device 1 to assert PDIAG-. Sampling of PDIAG- starts 1 ms after SRST is cleared to zero. If PDIAG- is asserted within 31 s, Device 0 clears bit 7 equal to zero in the Error Register, else Device 0 sets bit 7 equal to one in the Error Register. If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 clears bit 7 equal to zero in the Error register. In either case the device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h;
h) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit no later than 31 s from the time that the host clears the SRST bit equal to zero;

NOTE – Steps (g) and (h) may occur very rapidly.

i) Device 0 sets the DRDY bit when ready to accept any command.

NOTE – Steps (h) and (i) may occur at the same time. While no maximum time is specified for the DRDY bit to become equal to 1 to occur, a host should allow up to 30 s for the DRDY bit to be set to one. Figure 9 defines this timing.

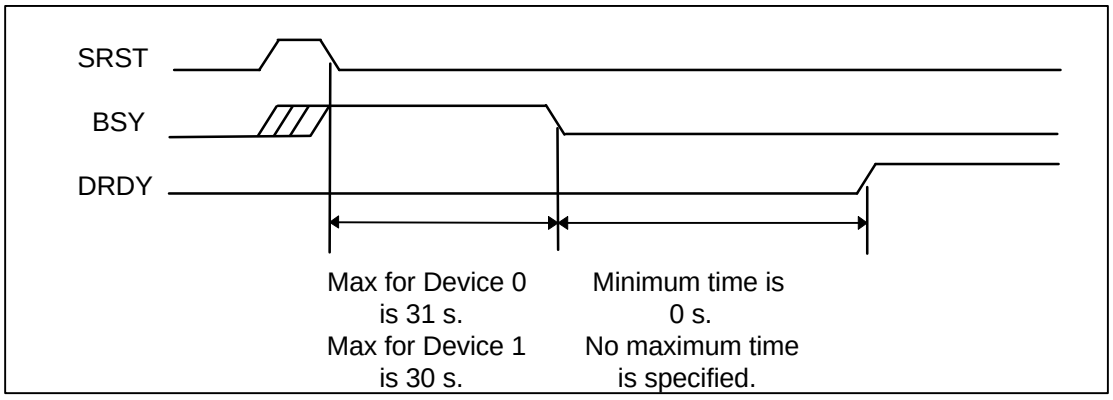


Figure 9 – BSY and DRDY timing for software reset

8.3 PIO data in commands

This class includes:

- IDENTIFY DEVICE
- READ BUFFER
- READ LONG (with and without retry)
- READ SECTOR(S) (with and without retry)
- READ MULTIPLE
- SMART READ ATTRIBUTE THRESHOLDS
- SMART READ ATTRIBUTE VALUES

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. Figure 10 describes the processing of a PIO data in command. This description does not include all possible error conditions.

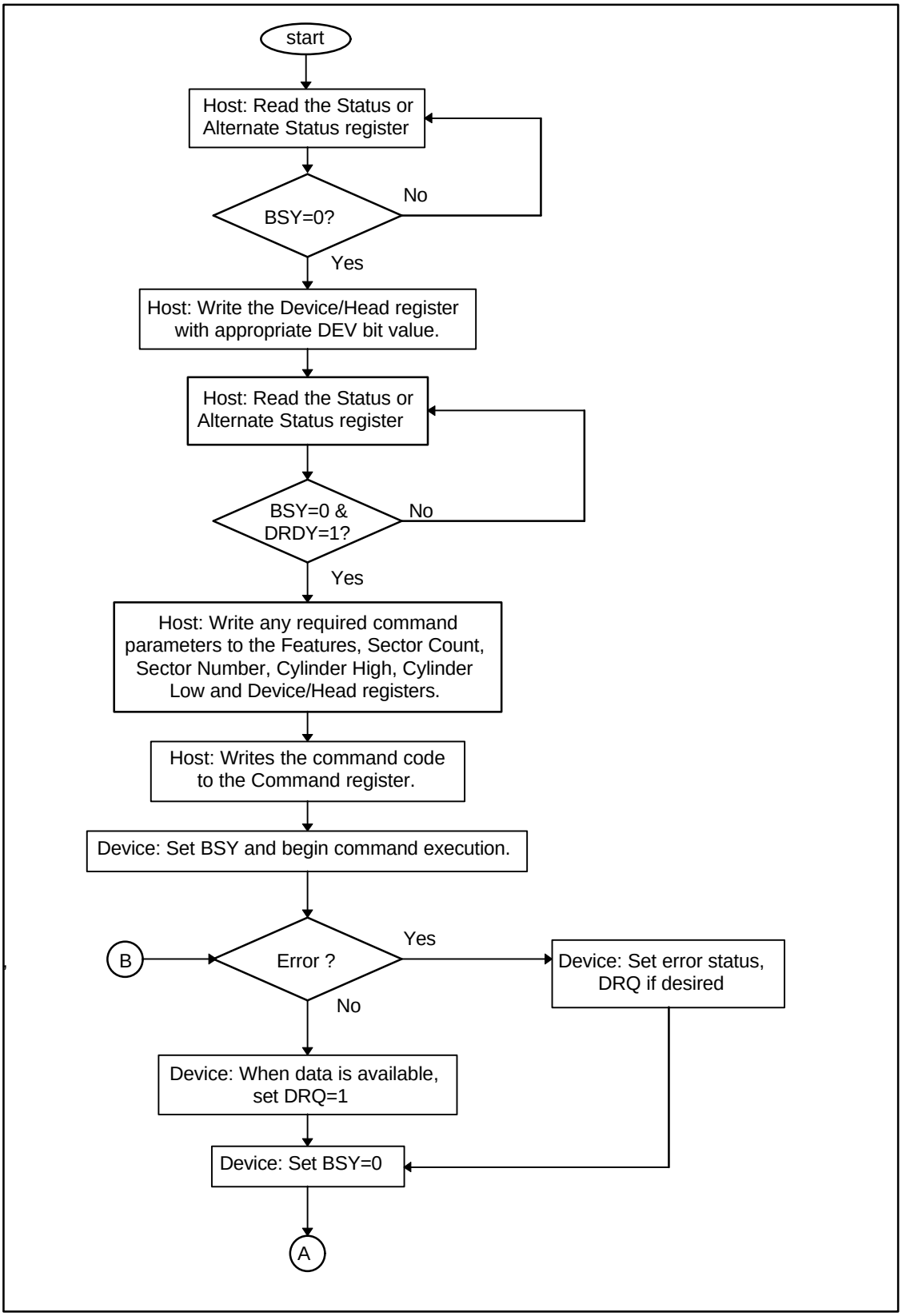


Figure 10 – **Example of PIO data transfer in diagram** *(continued)*

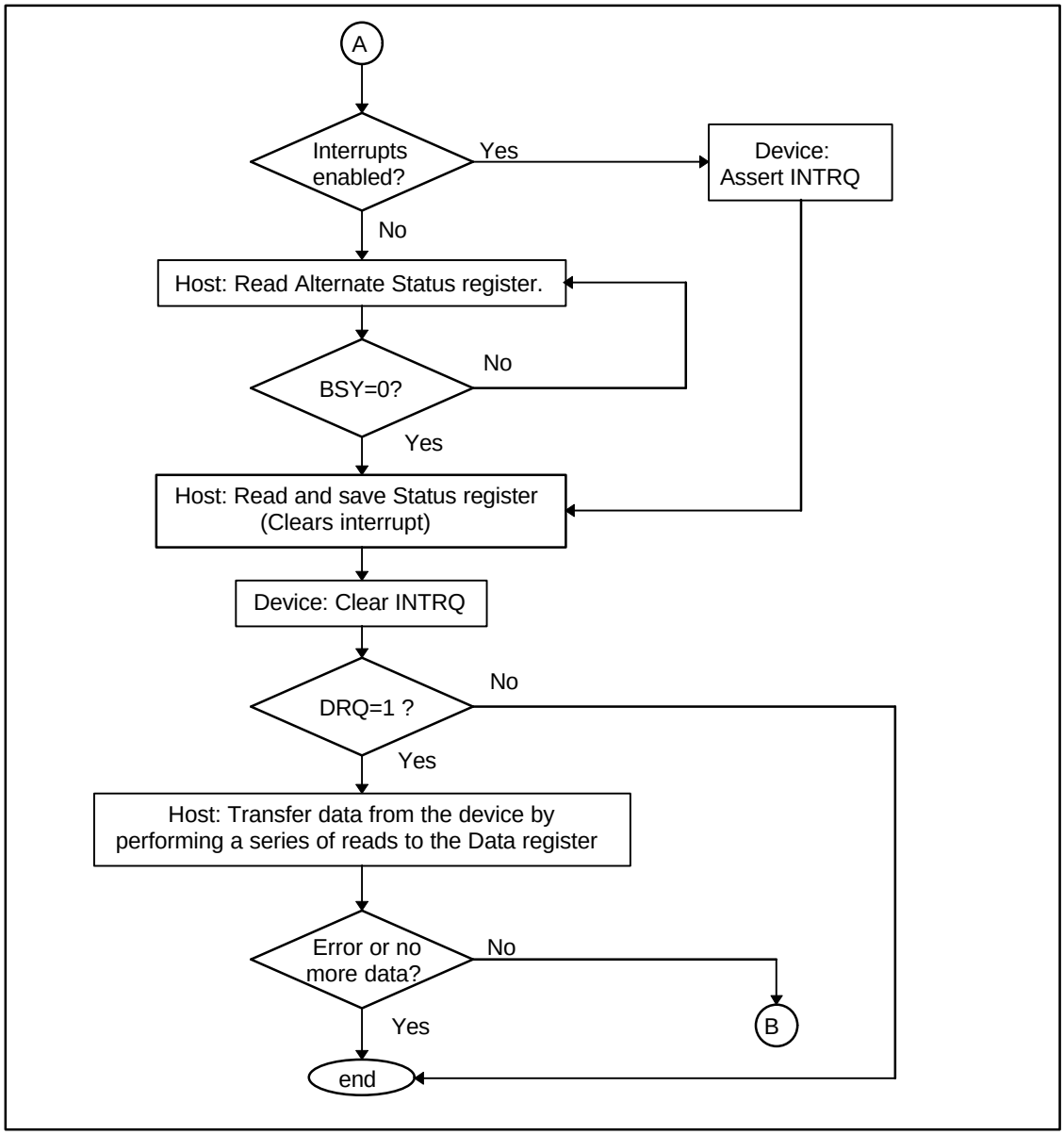


Figure 10 – **Example of PIO data transfer in diagram** *(concluded)*

8.4 PIO data out commands

This class includes:

- DOWNLOAD MICROCODE
- FORMAT TRACK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- WRITE BUFFER
- WRITE LONG (with and without retry)
- WRITE MULTIPLE
- WRITE SECTOR(S) (with and without retry)
- WRITE VERIFY

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 11 describes the processing of a PIO data out command.. This description does not include all possible error conditions.

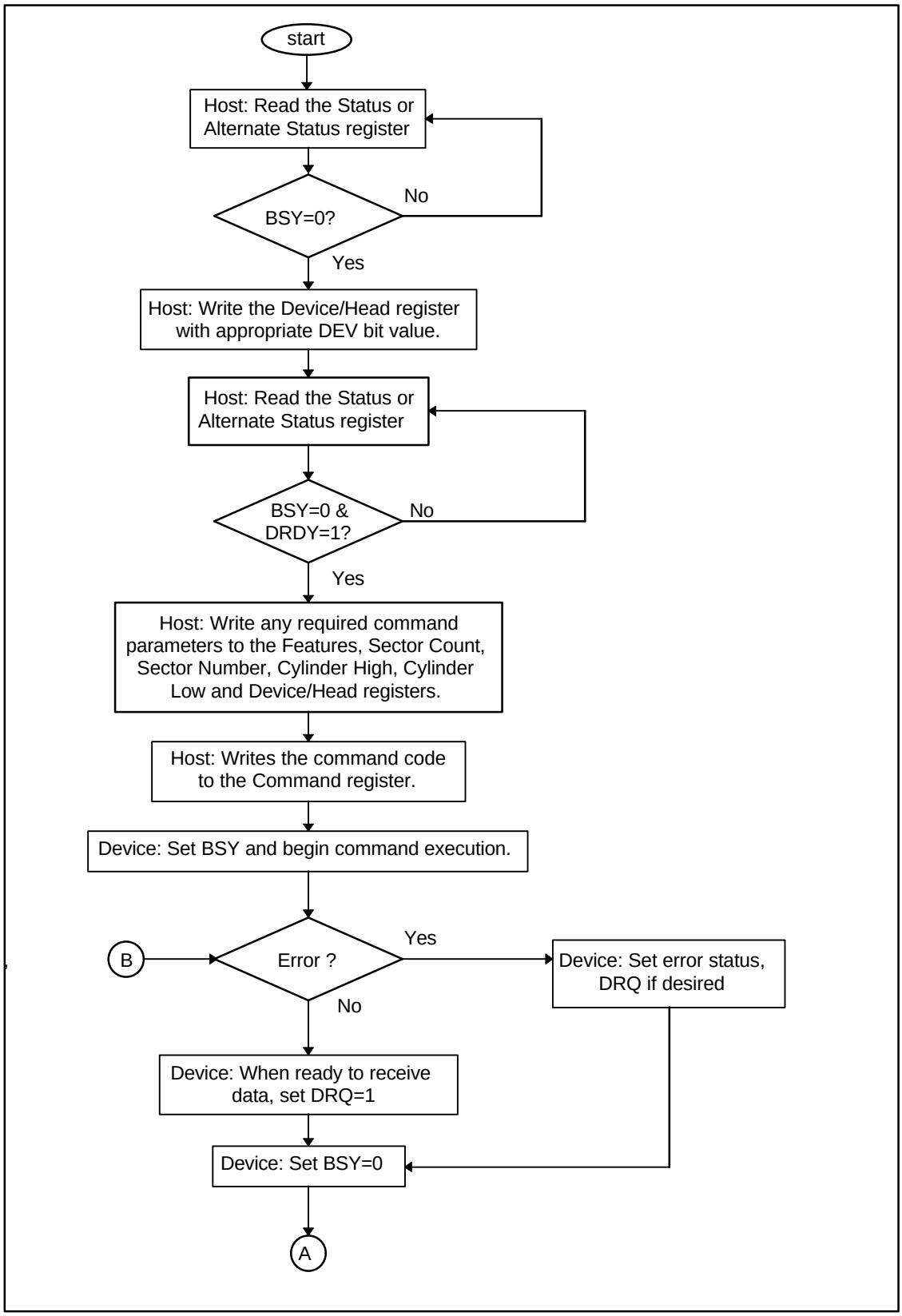


Figure 11 – **Example of PIO data transfer out diagram** *(continued)*

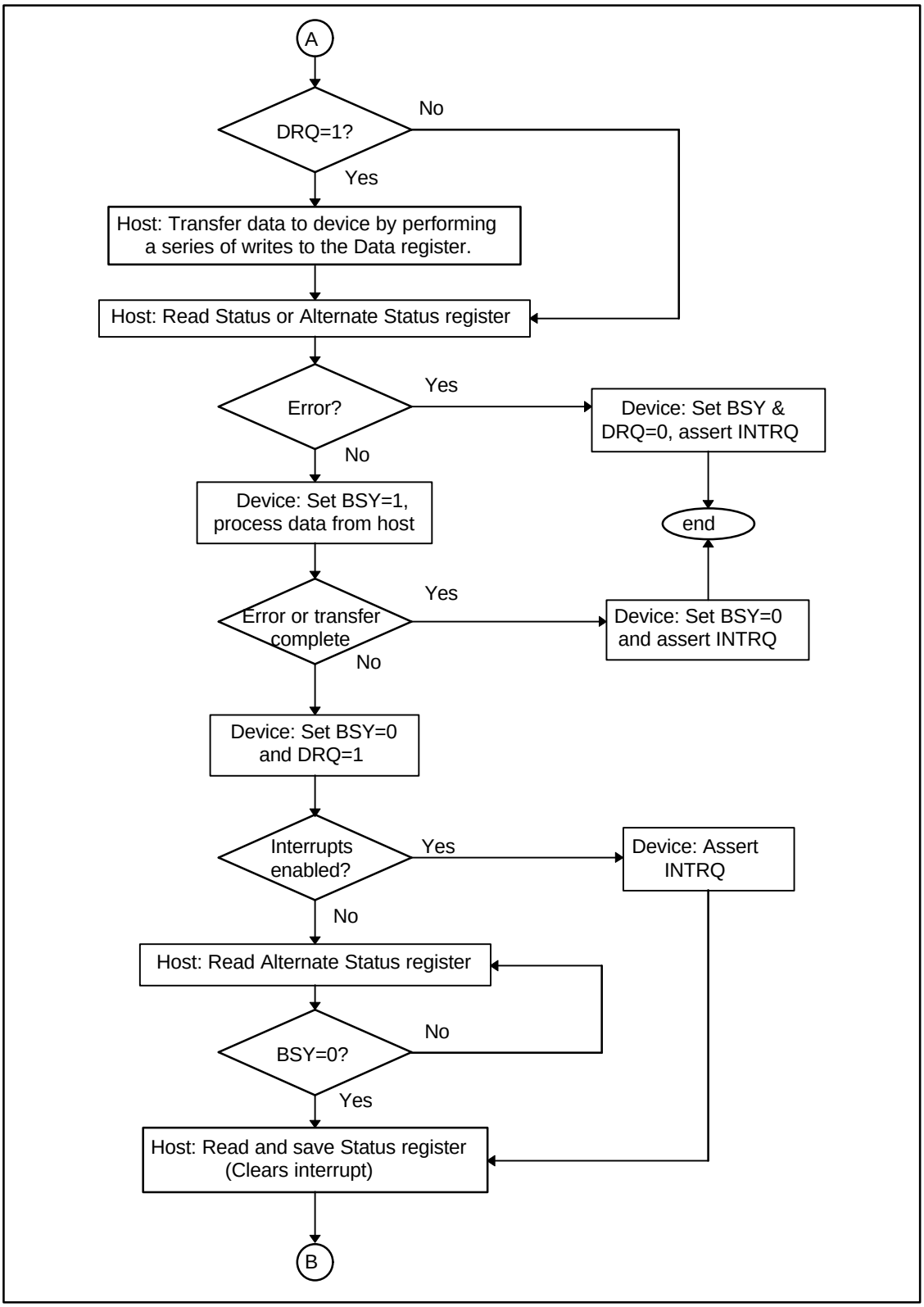


Figure 11 – **Example of PIO data transfer out diagram** *(concluded)*

8.5 Non-data commands

This class includes:

- CHECK POWER MODE
- DOOR LOCK
- DOOR UNLOCK
- EXECUTE DEVICE DIAGNOSTIC (DRDY=x)
- IDLE
- IDLE IMMEDIATE
- INITIALIZE DEVICE PARAMETERS (DRDY=x)
- MEDIA EJECT
- NOP
- READ VERIFY SECTOR(S)
- RECALIBRATE
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- SEEK
- SET FEATURES
- SET MULTIPLE MODE
- SLEEP
- SMART DISABLE OPERATION
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATION
- SMART RETURN STATUS
- SMART SAVE ATTRIBUTE VALUES
- STANDBY
- STANDBY IMMEDIATE

Execution of these commands involves no data transfer. Figure 12 describes the processing of a no data transfer command. This description does not include all possible error conditions.

See the EXECUTE DEVICE DIAGNOSTICS command description in 7.5, the NOP command description in 7.13 and the SLEEP command description in 7.30 for additional protocol requirements.

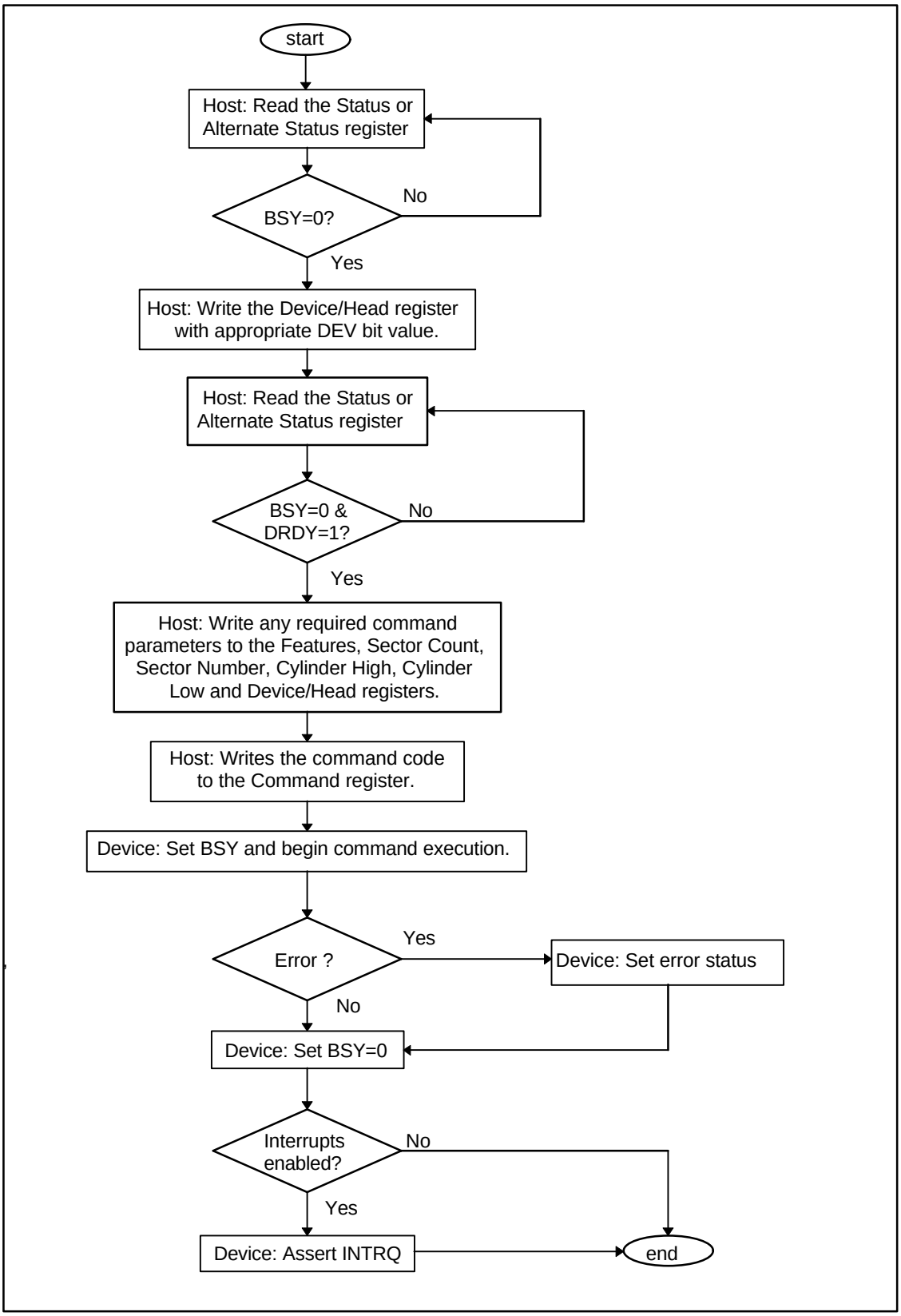


Figure 12 – Example of non-data transfer diagram

8.6 DMA data transfer commands

This class comprises:

- READ DMA (with and without retry)
- WRITE DMA (with and without retry)
- IDENTIFY DEVICE DMA

Data transfers using DMA commands differ in two ways from PIO transfers:

1) data transfers are performed using the DMA channel;

2) A Single interrupt is issued at the completion of the command.

Initiation of the DMA transfer commands is identical to the READ SECTOR(S) or WRITE SECTOR(S) commands except that the host initializes the DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that no intermediate sector interrupts are issued on multi-sector commands.

Figure 13 describes the execution of a DMA command.

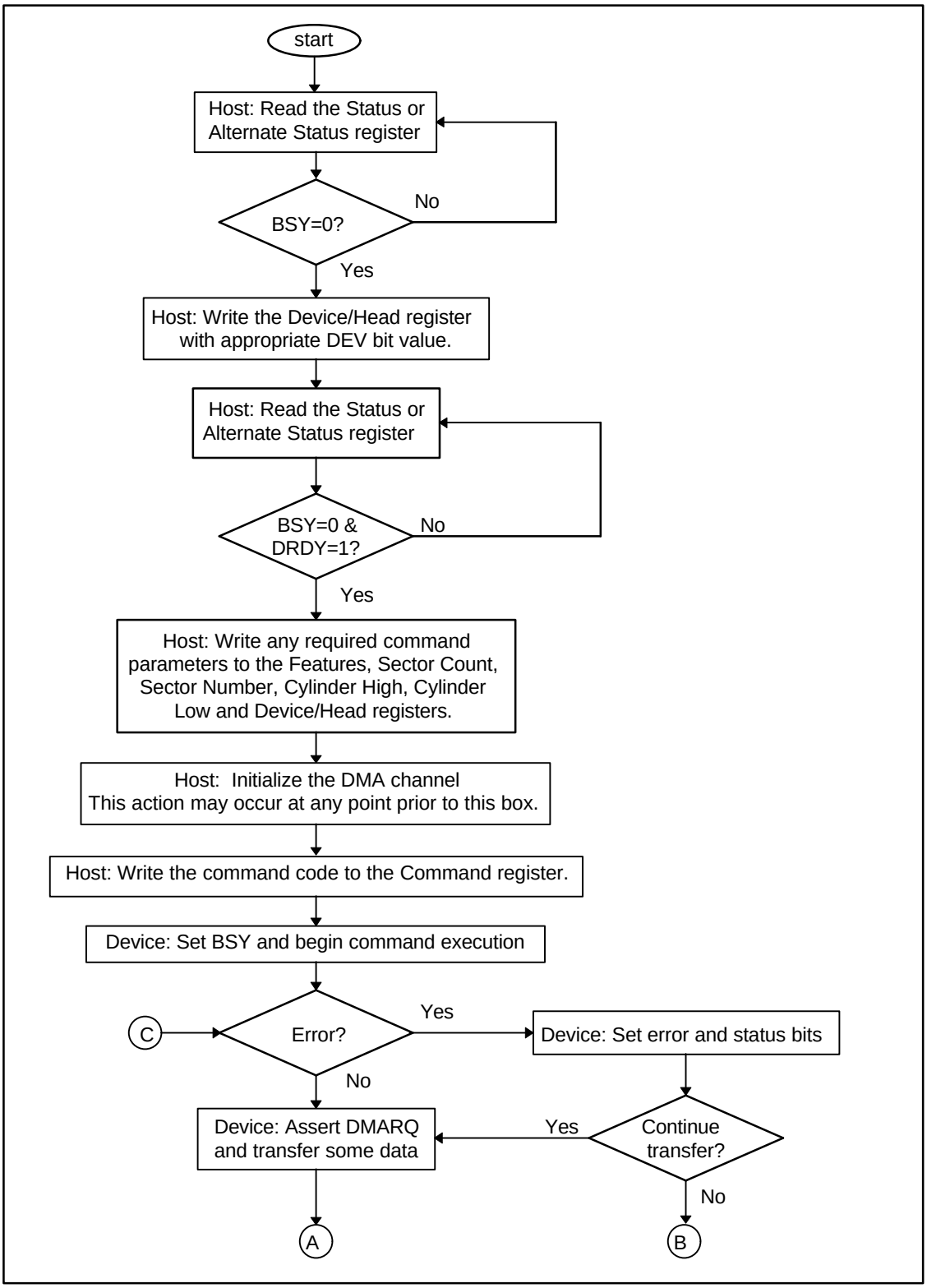


Figure 13 – **Example of DMA data transfer diagram** *(continued)*

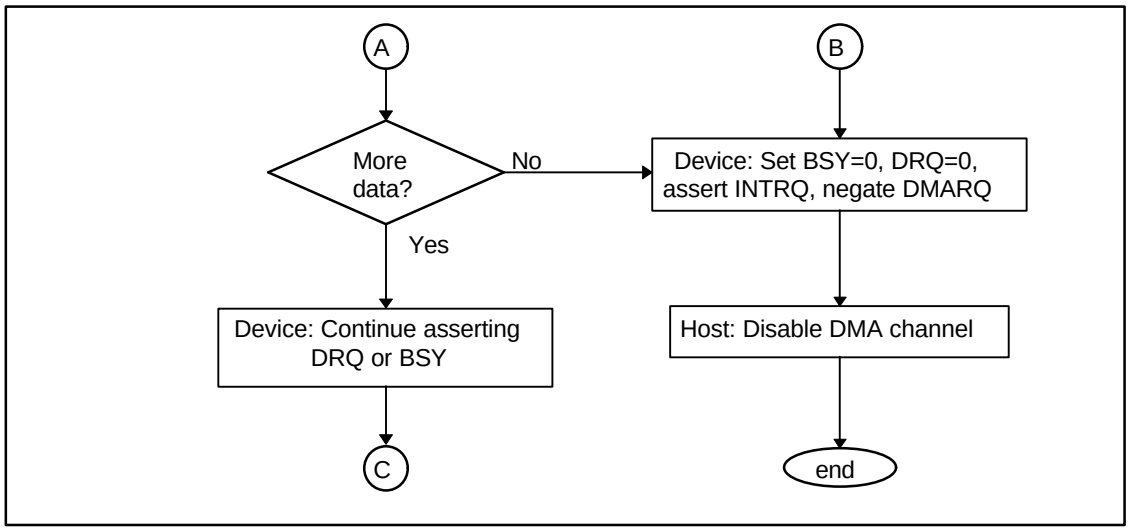


Figure 13 – **Example of DMA data transfer diagram** *(concluded)*

8.7 Single device configurations

8.7.1 Device 0 only configurations

In a single device configuration where Device 0 is the only device and the host selects Device 1, Device 0 may respond to accesses of the Command Block and Control Block registers in one of two methods. These two methods exist because previous versions of the ATA standard did not specify the required behavior for this configuration. The first method is the recommended implementation.

The first method is:

a) A write to the Device Control register shall complete as if Device 0 was the selected device;

b) A write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected;

c) A write to the Command register is ignored;

d) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected;

e) A read of the Status or Alternate status register returns the value 00h;

NOTE – IDX is vendor specific and might change following reset or power mode changes resulting in values for status other than 00h.

The second method requires that Device 0 implement an Error, Status, and Alternate Status register that is used whenever Device 1 is selected.

The second method is:

a) The Device 1 Error, Status, and Alternate status registers are set to 00h by a reset;

NOTE – IDX is vendor specific and might change following reset or power mode changes resulting in values for status other than 00h;

b) A write to the Device Control register shall complete as if Device 0 was the selected device;

c) A write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected;

d) A write to the Command register with a command code other than the INITIALIZE DEVICE PARAMETERS or EXECUTE DEVICE DIAGNOSTICS command causes the Device 1 Error, Status, and Alternate Status registers to be used as follows:

1) the BSY bit is set in the Device 1 Status register;

2) the ABRT bit is set in the Device 1 Error register;

3) the ERR bit is set in the Device 1 Status register;

4) the BSY bit is cleared in the Device 1 Status register;

5) if the nIEN bit in the Device Control Register is cleared, the INTRQ signal is asserted.

e) An EXECUTE DEVICE DIAGNOSTIC command is executed as if it addressed to Device 0;

f) An INITIALIZE DEVICE PARAMETERS command is executed as if Device 1 is present and is actually executing the command. The command shall have no effect of the device parameters of Device 0;

g) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected;

h) A read of the Error, Status or Alternate status register returns the value in the device 1 copy of these registers. The Device 1 status registers shall contain 00h following a reset and the value 01h following an attempt to execute a command, other than EXECUTE DEVICE DIAGNOSTICS or INITIALIZE DEVICE PARAMETERS, on Device 1.

8.7.2 Device 1 only configurations

Host support of Device 1 only configurations is host specific.

In a single device configuration where Device 1 is the only device and the host selects Device 0, Device 1 shall respond to accesses of the Command Block and Control Block registers in the same way it would if Device 0 was present. This is because Device 1 cannot determine if Device 0 is, or is not, present.

Host implementation of read and write operations to the Command and Control Block registers of non-existent Device 0 are host specific.

NOTE – The remainder of this section is a host implementation note.

The host implementor should be aware of the following when supporting Device 1 only configurations:

a) Following a hardware reset or software reset, Device 1 will not be selected. The following steps may be used to reselect Device 1:

1) Write to the Device/Head register with DRV bit set to one;

2) Using one or more of the Command Block registers that can be both written and read, such as the Sector Count or Sector Number, write a data pattern other than 00h or FFh to the register(s);

3) Read the register(s) written in step (2). If the data read is the same as the data written, proceed to step (5);

4) Repeat steps (1) to (3) until the data matches in step (3) or until 31 s has past. After 31 s it can probably be assumed that Device 1 is not functioning properly;

5) Read the Status register and Error registers. Check the Status and Error register contents for any error conditions that Device 1 may have posted.

b) Following the execution of an EXECUTE DEVICE DIAGNOSTICS command, Device 1 will not be selected. Also, no interrupt will be generated to signal the completion of the command. After writing the EXECUTE DEVICE DIAGNOSTIC command to the Command register, execute steps (1) to (3) as described in (a) above;

c) At all other times, do not write zero into the DRV bit of the Device/Head register. All other commands execute normally.

9 Timing

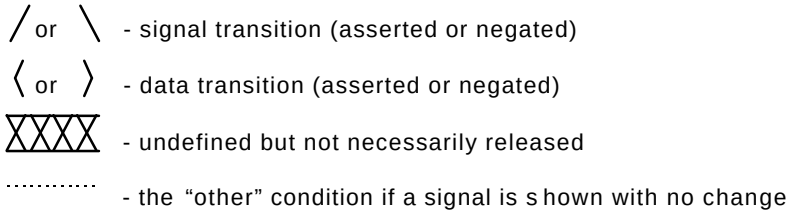
9.1 Deskewing

The host shall provide cable deskewing for all signals originating from the device. The device shall provide cable deskewing for all signals originating at the host.

All timing values and diagrams are shown and measured at the connector of either device connected to the ATA interface. No values are given for measurement at the host interface.

9.2 Symbols

Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.

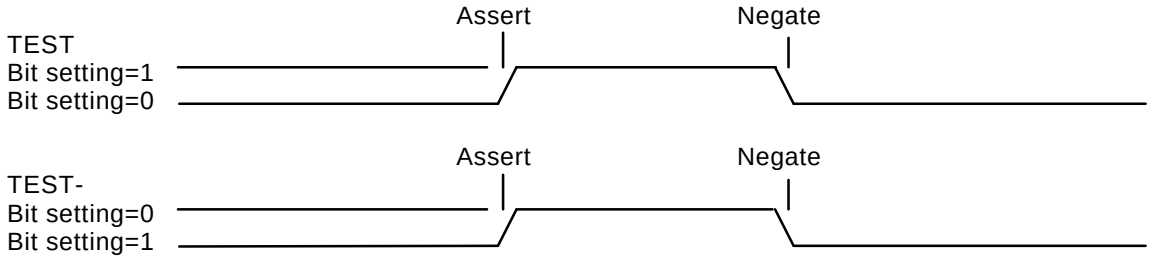


All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

9.3 Terms

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted e.g., the following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



9.4 Data transfers

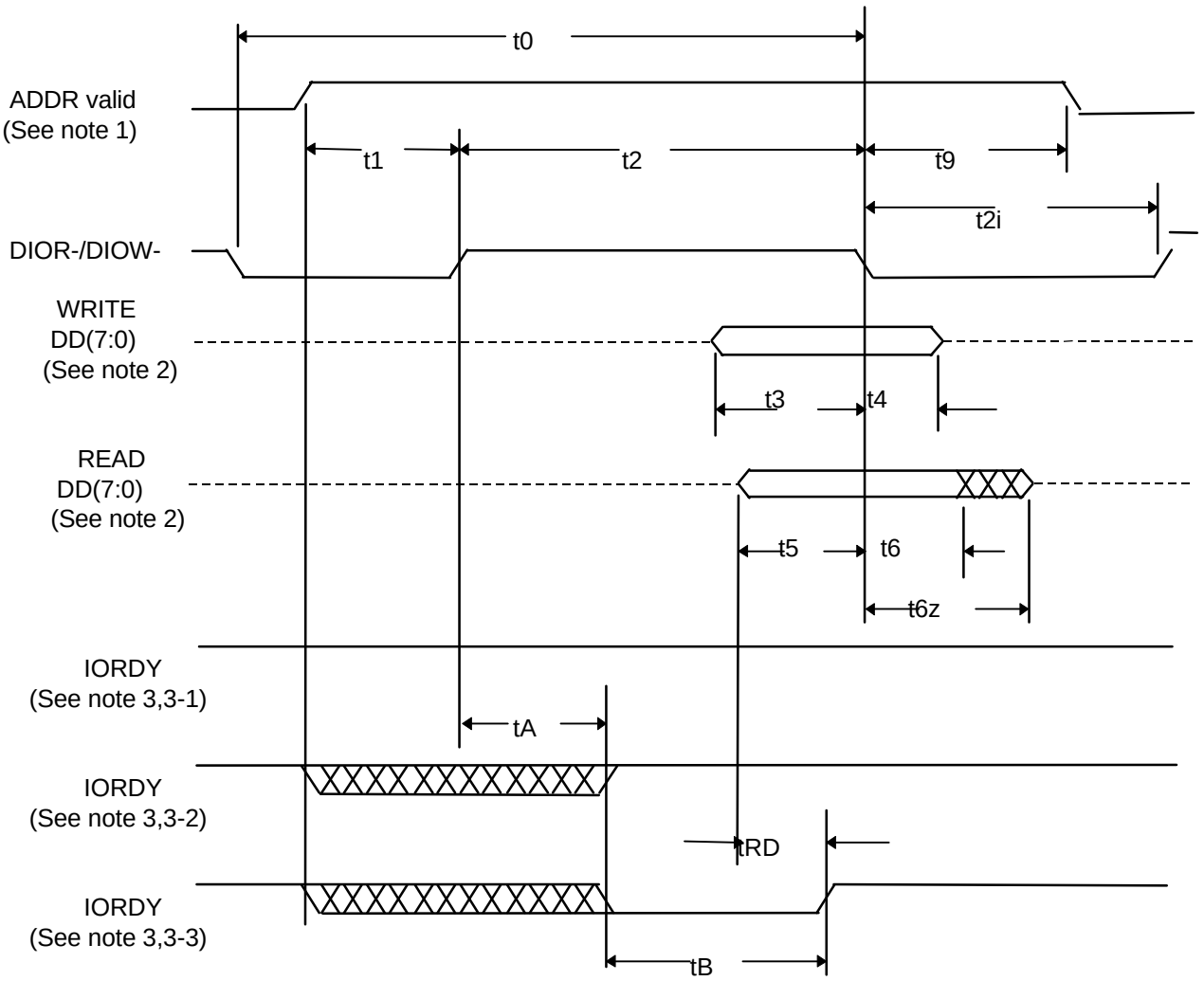
The minimum cycle time supported by the device in PIO Mode 3, 4 and Multiword DMA Mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated Mode e.g., a drive supporting PIO Mode 4 timing shall not report a value less than 120 ns, the minimum cycle time defined for Mode 4 PIO Timings.

9.4.1 Register transfers

Figure 14 defines the relationships between the interface signals for 8-bit PIO register transfers. This timing applies to all register accesses except accesses to the Data register. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1 or 2.

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the Identify Drive parameter list. Table 21 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.



NOTES –
1 Device address consists of signals CS0-, CS1- and DA(2:0)
2 Data consists of DD(7:0).
3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY: no wait is generated.
3-2 Device negates IORDY before tA, but causes IORDY to be asserted before tA: no wait generated.
3-3 Device negates IORDY before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for tRD before asserting IORDY.

Figure 14 – Register transfer to/from device

Table 21 – Register transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t0	Cycle time	(min)	600	383	240	180	120	1
t1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t2	DIOR-/DIOW- 8-bit	(min)	290	290	290	80	70	1
t2i	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t3	DIOW- data setup	(min)	60	45	30	30	20	
t4	DIOW- data hold	(min)	30	20	15	10	10	
t5	DIOR- data setup	(min)	50	35	20	20	20	
t6	DIOR- data hold	(min)	5	5	5	5	5	
t6Z	DIOR- data tristate	(max)	30	30	30	30	30	2
t9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
tRd	Read Data Valid to IORDY active (if IORDY initially low after tA)	(min)	0	0	0	0	0	
tA	IORDY Setup time		35	35	35	35	35	3
tB	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	

NOTES –

1 t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

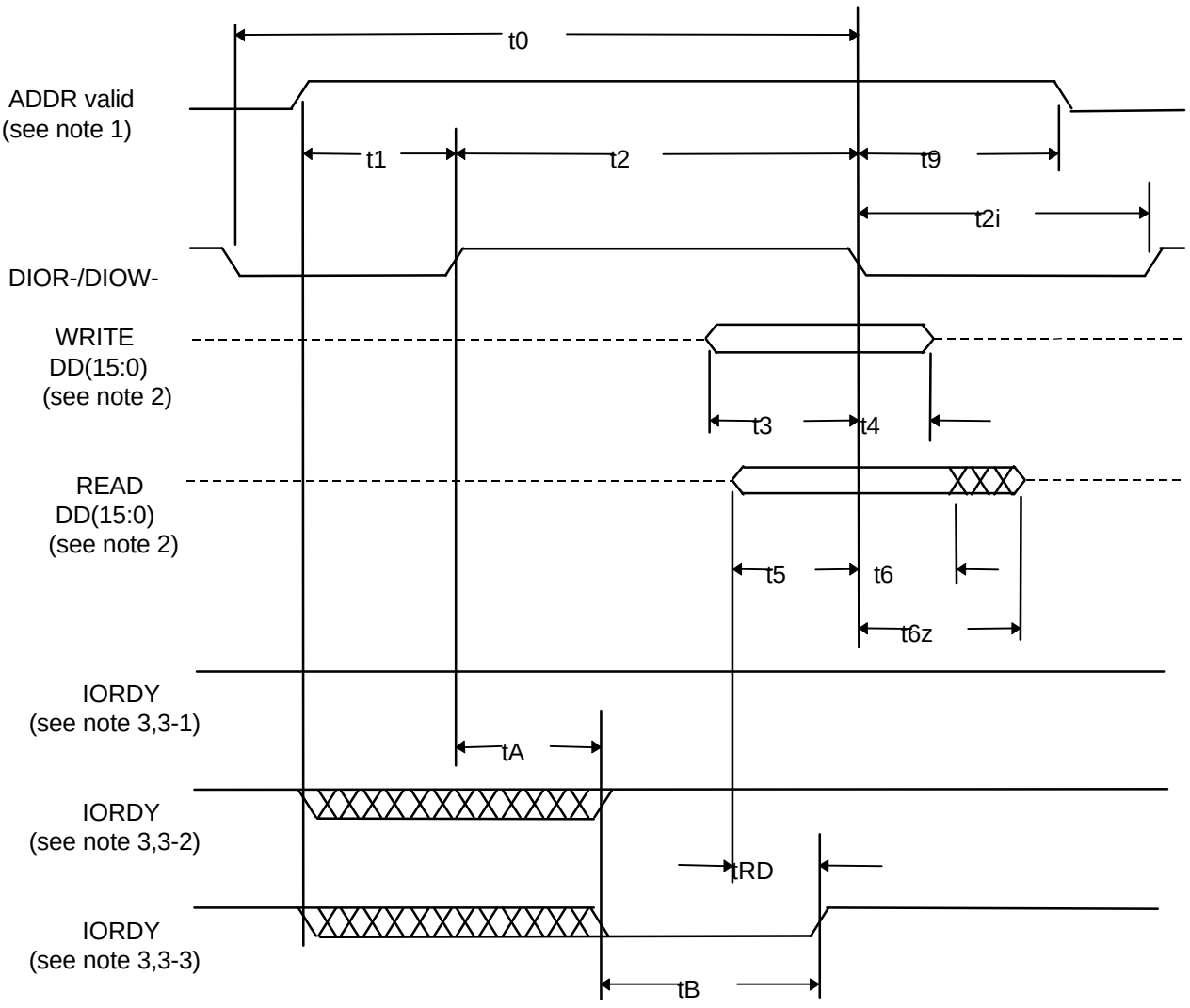
3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at the tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.

9.4.2 PIO data transfers

Figure 15 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 22 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.



NOTES

1 Device address consists of signals CS0-, CS1- and DA(2:0)

2 Data consists of DD(15:0). For READ LONG and WRITE LONG commands, the transfer of the vendor specific bytes shall be 16 bit transfers with the vendor specific byte in bits 7 through 0. Bits 15 through 8 shall be ingnored.

3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY: no wait is generated.

3-2 Device negates IORDY before tA, but causes IORDY to be asserted before tA: no wait generated.

3-3 Device negates IORDY before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for tRD before asserting IORDY.

Figure 15 – PIO data transfer to/from device

Table 22 – PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t0	Cycle time	(min)	600	383	240	180	120	1
t1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t2	DIOR-/DIOW- 16-bit	(min)	165	125	100	80	70	1
t2i	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t3	DIOW- data setup	(min)	60	45	30	30	20	
t4	DIOW- data hold	(min)	30	20	15	10	10	
t5	DIOR- data setup	(min)	50	35	20	20	20	
t6	DIOR- data hold	(min)	5	5	5	5	5	
t6Z	DIOR- data tristate	(max)	30	30	30	30	30	2
t9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
tRd	Read Data Valid to IORDY active (if IORDY initially low after tA)	(min)	0	0	0	0	0	
tA	IORDY Setup time		35	35	35	35	35	3
tB	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	

NOTES

1 t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

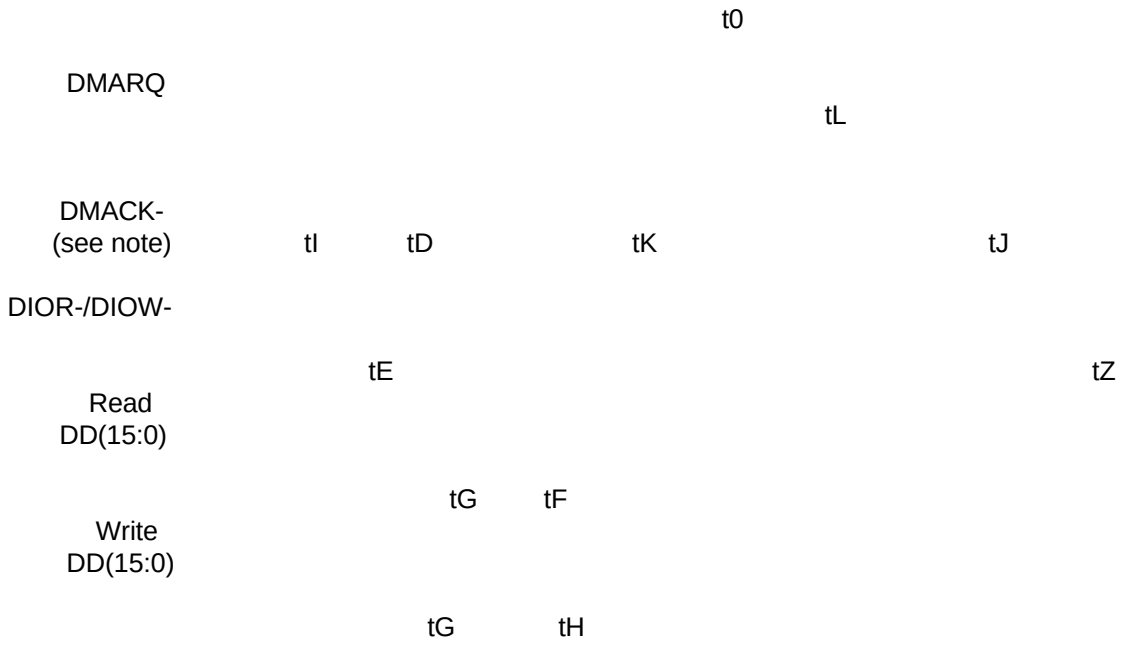
3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at the tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.

9.4.3 Multiword DMA data transfer

Figure 16 defines the timings associated with Multiword DMA transfers.

For Multiword DMA modes 1 and above, the minimum value of t0 is specified by word 65 in the IDENTIFY DEVICE parameter list. Table 23 defines the minimum value that shall be placed in word 65.

Devices reporting support for Multiword DMA Transfer Mode 2 shall also support Multiword DMA Transfer Mode 0 and 1 and shall power up with Mode 0 as the default Multiword DMA Mode.



NOTE – This signal may be negated by the Host to suspend the DMA transfer in process. For Multi-Word DMA transfers, the Device may negate DMARQ within the tL specified time once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert.

Table 23 – Multiword DMA data transfer

Multiword DMA timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
t0	Cycle time	(min)	480	150	120	see note
tC	DMACK to DMARQ delay					
tD	DIOR-/DIOW-	(min)	215	80	70	see note
tE	DIOR- data access	(max)	150	60		
tF	DIOR- data hold	(min)	5	5	5	
tG	DIOR-/DIOW- data setup	(min)	100	30	20	
tH	DIOW- data hold	(min)	20	15	10	
tI	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
tJ	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
tKr	DIOR- negated pulse width	(min)	50	50	25	see note
tKw	DIOW- negated pulse width	(min)	215	50	25	see note
tLr	DIOR- to DMARQ delay	(max)	120	40	35	
tLw	DIOW- to DMARQ delay	(max)	40	40	35	
tZ	DMACK- to tristate	(max)	20	25	25	

NOTE – t0 is the minimum total cycle time, tD is the minimum command active time, and tK (tKr or tKw, as appropriate) is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tK shall be met. The minimum total cycle time requirement, t0, is greater than the sum of tD and tK. This means a host implementation can lengthen either or both tD or tK to ensure that t0 is equal to the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

Annex A
(normative)
Connectors

A.1 40-pin connector

The I/O connector is a 40-pin connector as shown in figure A.1, with pin assignments as shown in table A.1. The connector shall be keyed to prevent the possibility of installing it upside down. A key is provided by the removal of pin 20. The corresponding pin on the cable connector shall be plugged.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle is not polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in figure A.1, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

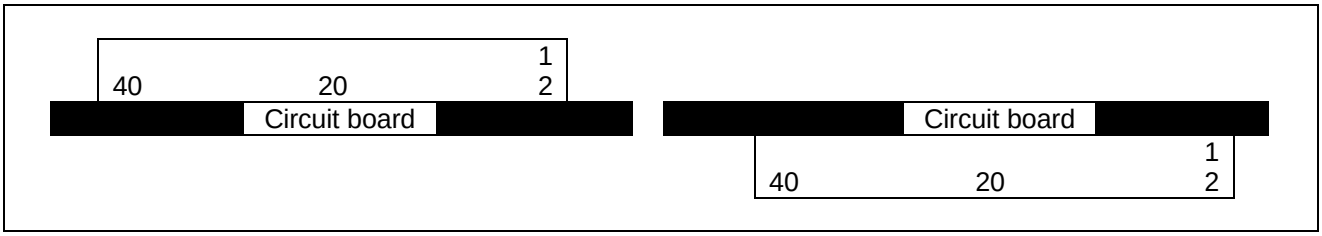


Figure A.1 – 40-pin connector mounting

Table A.1 – 40-pin connector interface signals

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

Recommended part numbers for the mating connector and cable are shown below, but equivalent parts may be used.

Connector (40 pin) :	3M 3417-7000 or equivalent
Strain relief :	3M 3448-2040 or equivalent

Flat cable (stranded 28 AWG) :	3M 3365-40 or equivalent
Flat cable (stranded 28 AWG) :	3M 3517-40 (shielded) or equivalent

A.1.1 4-pin power connector

When the device uses the 40-pin connector, the device receives DC power through a 4-pin connector. The pin assignments are shown in table A.2 and the connector pin locations are shown if figure A.2. Recommended part numbers for the mating connector to 18 AWG cable are shown below, but compatible parts may be used.

Connector (4 pin) :	AMP 1-480424-0 or compatible
Contacts (loose piece) :	AMP 60619-4 or compatible
Contacts (strip) :	AMP 61117-4 or compatible

Table A.2 – DC interface using 4-pin power connector

Power line designation	Pin Number
+12 Volts	1
+12 Volt return	2
+5 Volt return	3
+5 Volts	4

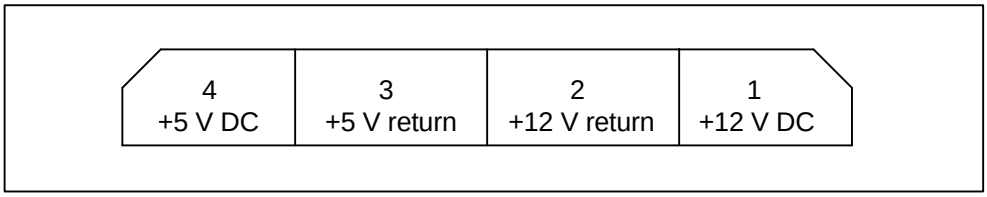


Figure A.2 – Drive side connector pin numbering

A.2 44-pin small form factor connector

This annex describes a connector alternative often used for 2 1/2 inch or smaller devices. This alternative was developed by the Small Form Factor (SFF) Committee, an industry ad hoc group.

In an effort to broaden the applications for small form factor devices, a group of companies representing system integrators, device suppliers, and component suppliers decided to address the issues involved.

A primary purpose of the SFF Committee was to define the external dimensions of small form factor devices so that products from different vendors could be used in the same mounting configurations.

The restricted area and the mating of devices directly to a motherboard required that the number of connectors be reduced, which caused the assignment of additional pins for power. Power is provided to the devices on the same connector as used for the signals, and addresses are set by the receptacle into which the devices are plugged.

The 50-pin connector that has been widely adopted across industry for SFF devices is a low density 2 mm connector which has no shroud on the plug which is mounted on the device. A number of suppliers provide

intermatable components. The following information has been provided to assist users in specifying components used in an implementation.

Signals Connector Plug :	DuPont 86451 or equivalent
Signals Connector Receptacle :	DuPont 86455 or equivalent

A.2.1 44-pin signal assignments

The signals assigned for 44-pin applications are described in table A.3. Although there are 50 pins in the plug, a 44-pin mating receptacle may be used (the removal of pins E and F provides room for the wall of the receptacle).

Some devices may utilize pins A, B, C, and D for option selection via physical jumpers. Such implementations may require use of the 44-pin receptacle.

The first four pins of the connector plug located on the device shall not to be connected to the host, as they are reserved for manufacturer's use. Pins E, F, and 20 are keys, and are removed (see figure A.3).

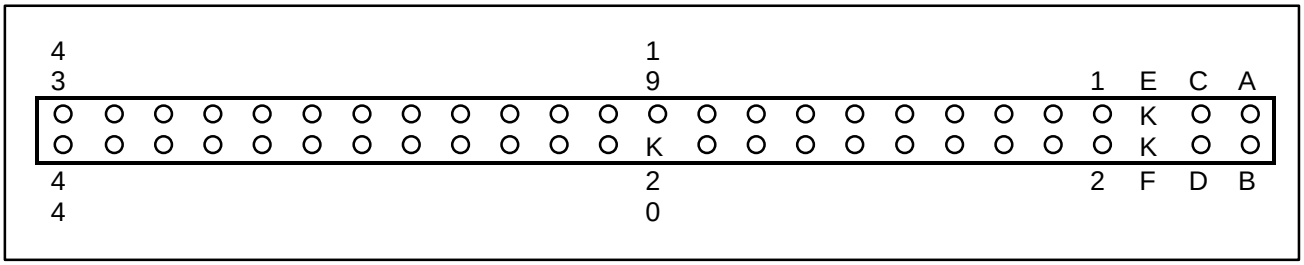


Figure A.3 – 44-pin connector

Table A.3 – Signal assignments for 44-pin ATA

Signal name	Connector contact	Conductor		Connector contact	Signal name
Vendor specific	A			B	Vendor specific
Vendor specific	C			D	Vendor specific
(keypin)	E			F	(keypin)
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic) (see note)	41	41	42	42	+5 V (Motor) (see note)
Ground(return) (see note)	43	43	44	44	TYPE- (0=ATA) (see note)

NOTE – Pins which are additional to those of the 40-pin cable.

A.3 68-pin small form factor connector

This clause defines the pinouts used for the 68-pin alternative connector for the AT Attachment Interface. This connector is the same as the one defined by PCMCIA. This clause defines a pinout alternative that allows a device to function as an AT Attachment Interface compliant device, while also allowing the device to be compliant with PC Card ATA mode defined by PCMCIA. The signal protocol allows the device to identify the host interface as being 68-pin ATA or PC Card ATA.

To simplify the implementation of dual-interface devices, the 68-pin AT Attachment Interface maintains commonality with as many PC Card ATA signals as possible, while supporting full command and signal compliance with the ATA standard.

The 68-pin ATA pinout shall not cause damage or loss of data if a PCMCIA card is accidentally plugged into a host slot supporting this interface. The inversion of the reset signal between the ATA and PCMCIA interfaces prevents loss of data if the device is unable to reconfigure itself to the appropriate host interface.

A.3.1 Signals

This specification relies upon the electrical and mechanical characteristics of PCMCIA and unless otherwise noted, all signals and registers with the same names as PCMCIA signals and registers have the same meaning as defined in PCMCIA.

The PC Card-ATA specification is used as a reference to identify the signal protocol used to identify the host interface protocol.

A.3.2 Signal descriptions

Any signals not defined below shall be as described in the ATA, PCMCIA, or the PC Card ATA documents.

Table A.4 shows the ATA signals and relationships such as direction, as well as providing the signal name of the PCMCIA equivalent.

Table A.4 – Signal assignments for 68-pin ATA

Pin	Signal	Hst	Dir	Dev	PCMCIA	Pin	Signal	Hst	Dir	Dev	PCMCIA
1	Ground	x	→	x	Ground	35	Ground	x	→	x	Ground
2	DD3	x	↔	x	D3	36	CD1-	x	←	x	CD1-
3	DD4	x	↔	x	D4	37	DD11	x	↔	x	D11
4	DD5	x	↔	x	D5	38	DD12	x	↔	x	D12
5	DD6	x	↔	x	D6	39	DD13	x	↔	x	D13
6	DD7	x	↔	x	D7	40	DD14	x	↔	x	D14
7	CS0-	x	→	x	CE1-	41	DD15	x	↔	x	D15
8			→	i	A10	42	CS1-	x	→	x(1)	CE2-
9	SELATA-	x	→	x	OE-	43			←	i	VS1-
10						44	DIOR-	x	→	x	IORD-
11	CS1-	x	→	x(1)	A9	45	DIOW-	x	→	x	IOWR-
12			→	i	A8	46					
13						47					
14						48					
15			→	i	WE-	49					
16	INTRQ	x	←	x	READY/ IREQ-	50					
17	Vcc	x	→	x	Vcc	51	Vcc	x	→	x	Vcc
18						52					
19						53					
20						54					
21						55	M/S-	x	→	x(2)	
22			→	i	A7	56	CSEL	x	→	x(2)	
23			→	i	A6	57			←	i	VS2-
24			→	i	A5	58	RESET-	x	→	x	RESET
25			→	i	A4	59	IORDY	o	←	x(3)	WAIT-
26			→	i	A3	60	DMARQ	o	←	x(3)	INPACK-
27	DA2	x	→	x	A2	61	DMACK-	o	→	o	REG-
28	DA1	x	→	x	A1	62	DASP-	x	↔	x	BVD2/ SPKR-
29	DA0	x	→	x	A0	63	PDIAG-	x	↔	x	BVD1/ STSCHG
30	DD0	x	↔	x	D0	64	DD8	x	↔	x	D8
31	DD1	x	↔	x	D1	65	DD9	x	↔	x	D9
32	DD2	x	↔	x	D2	66	DD10	x	↔	x	D10
33		x	←	x	WP/ IOIS16	67	CD2-	x	←	x	CD2-
34	Ground	x	→	x	Ground	68	Ground	x	→	x	Ground

Key:
Dir = the direction of the signal between host and device.
x in the Hst column = this signal shall be supported by the Host.
x in the Dev column = this signal shall be supported by the device.
i in the Dev column = this signal shall be ignored by the device while in 68-pin ATA mode.
o = this signal is Optional.
Nothing in Dev column = no connection should be made to that pin.

NOTES –
1 The device shall support only one CS1- signal pin.
2 The device shall support either M/S- or CSEL but not both.
3 The device shall hold this signal negated if it does not support the function.

A.3.2.1 CD1- (Card Detect 1)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

A.3.2.2 CD2- (Card Detect 2)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

A.3.2.3 CS1- (Device chip select 1)

Hosts shall provide CS1- on both the pins identified in table A.4.

Devices shall recognize only one of the two pins as CS1-.

A.3.2.4 DMACK- (DMA acknowledge)

This signal is optional for hosts and devices.

If this signal is supported by the host or the device, the function of DMARQ shall also be supported.

A.3.2.5 DMARQ (DMA request)

This signal is optional for hosts.

If this signal is supported by the host or the device, the function of DMACK- shall also be supported.

A.3.2.6 IORDY (I/O channel ready)

This signal is optional for hosts.

A.3.2.7 M/S- (Master/slave)

This signal is the inverted form of CSEL. Hosts shall support both M/S- and CSEL though devices need only support one or the other.

Hosts shall assert CSEL and M/S- prior to applying VCC to the connector.

A.3.2.8 SELATA- (Select 68-pin ATA)

This pin is used by the host to select which mode to use, PC Card-ATA mode or the 68-pin ATA mode. To select 68-pin ATA mode, the host shall assert SELATA- prior to applying power to the connector, and shall hold SELATA- asserted.

The device shall not re-sample SELATA- as a result of either a Hard or Soft Reset. The device shall ignore all interface signals for 19 ms after the host supplies Vcc within the device's voltage tolerance. If SELATA- is negated following this time, the device shall either configure itself for PC Card-ATA mode or not respond to further inputs from the host.

A.3.3 Removability considerations

This specification supports the removability of devices which use the ATA protocol. As removability is a new consideration for ATA devices, several issues need to be considered with regard to the insertion or removal of devices.

A.3.3.1 Device recommendations

The following are recommendations to device implementors:

- CS0-, CS1-, RESET-, and SELATA- signals be negated on the device to prevent false selection during hot insertion.

- Ignore all interface signals except SELATA- until 19 ms after the host supplies VCC within the device's voltage tolerance. This time is necessary to de-bounce the device's power on reset sequence. Once in the 68-pin ATA mode, if SELATA- is ever negated following the 19 ms de-bounce delay time, the device disables itself until VCC is removed.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register are used to prevent unexpected removal of the device or media.

A.3.3.2 Host recommendations

The following are recommendations to host implementors:

- Connector pin sequencing to protect the device by making contact to ground before any other signal in the system.

- SELATA- to be asserted at all times.

- All devices reset and reconfigured to the same base address each time a device at that address is inserted or removed.

- The removal or insertion of a device at the same address to be detected so as to prevent the corruption of a command.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register used to prevent unexpected removal of the device or media.

Annex B
(informative)
Identify device data for ATA devices below 8 GB

B.1 Definitions and background information

The following abbreviations are used in this annex:

- 528 MB is used to describe a device that has 1,032,192 sectors or 528,482,304 bytes.
- 8 GB is used to describe a device that has 16,515,072 sectors or 8,455,716,864 bytes.

The original IBM PC BIOS (Basic Input/Output System) imposed several restrictions on the support of devices, and these have been incorporated into many higher level software products. One such restriction limits the capacity of a device. Most BIOS software cannot support a device with more than 1,024 cylinders, 16 heads and 63 sectors per track. The maximum addressable capacity of a device under this scheme is 528 MB.

There is growing support of auto-configuration for devices on PC systems. The auto-configuration capability usually resides in the BIOS and uses the IDENTIFY DEVICE command data to configure a device.

This annex defines rules for the IDENTIFY DEVICE data of all capacity devices and allows BIOS support of devices up to 8 GB using Cylinder/Head/Sector (CHS) addressing.

This specification defines information that newer BIOSs and system software can use to determine the true size of a device and access the full capacity of the device.

B.2 Cylinder, head, and sector addressing

BIOSs and other software that operate a device in CHS (Cylinder, Head, and Sector) addressing mode use IDENTIFY DEVICE data words 1, 3, 6, and words 53-58 to ascertain the appropriate translation mode to use and determine the capacity of a device.

Maximum compatibility is achieved if the following rules are obeyed. These rules limit the values placed into words 1, 3, 6, and 53-58. The rules specified here for CHS addressing apply to devices up to 8 GB.

B.2.1 Word 1

For devices less than or equal to 528 MB, IDENTIFY DEVICE data word 1 (Default Cylinders) does not specify a value greater than 1,024.

If a device is greater than 528 MB but less than or equal to 8 GB, the maximum value that is placed into this word is determined by the value in Word 3 as shown in table B.1.

NOTE – This algorithm reserves a gap at cylinder address 16,384 to support the legacy of a maintenance cylinder.

Table B.1 – Word 1 value

Value in Word 3	Maximum value in Word 1
1 1h	65,535 FFFFh
2 2h	65,535 FFFFh
3 3h	65,535 FFFFh
4 4h	65,535 FFFFh
5 5h	32,767 7FFFh
6 6h	32,767 7FFFh
7 7h	32,767 7FFFh
8 8h	32,767 7FFFh
9 9h	16,383 3FFFh
10 Ah	16,383 3FFFh
11 Bh	16,383 3FFFh
12 Ch	16,383 3FFFh
13 Dh	16,383 3FFFh
14 Eh	16,383 3FFFh
15 Fh	16,383 3FFFh
16 10h	16,383 3FFFh

The value in this word does not change.

B.2.2 Word 3

IDENTIFY DEVICE data word 3 (Default Heads) does not specify a value greater than 16.

The value in this word does not change.

B.2.3 Word 6

For devices of 8 GB or less, IDENTIFY DEVICE data word 6 (Default Sectors) does not specify a value greater than 63.

The value in this word does not change.

B.2.4 Use of words 53 through 58

Devices that are over 528 MB implement words 53-58. Devices not over 528 MB may also implement these words. These words define the addressing for all sectors accessible in CHS mode.

B.2.5 Word 53

IDENTIFY DEVICE data word 53 bit 0 is set to one at all times that the device is in a valid translation mode. Some devices may have translation modes that cannot be supported. An attempt to put a device into one of these unsupported modes causes word 53 bit 0 to be cleared to zero with words 54-58 cleared to zero until a valid translation mode is established.

B.2.6 Word 54

IDENTIFY DEVICE data word 54 (Current Cylinders) specifies the number of full logical cylinders that can be accessed in the current translation mode. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word is the same as word 1. If an INITIALIZE DEVICE PARAMETERS command has been executed, this word is the integer result of dividing the total number of user sectors (this value may be in words 60-61) by the number of sectors per logical cylinder ([word55] x [word56]), but is not a value greater than 65,535.

B.2.7 Word 55

IDENTIFY DEVICE data word 55 (Current Heads) is the number of heads specified by the last INITIALIZE DEVICE PARAMETERS command. This word contains a value of between 1 and 16. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word are the same as word 3.

B.2.8 Word 56

IDENTIFY DEVICE data word 56 (Current Sectors) is the number of sectors specified by the last INITIALIZE DEVICE PARAMETERS command. This word may contain a value of between 1 and 255. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word are the same as word 6.

B.2.9 Words 57-58

IDENTIFY DEVICE data words 57-58 contain a 32-bit value that is equal to [word54] x [word55] x [word56]. Words 57-58 are less than or equal to the value in words 60-61 at all times.

B.3 Orphan sectors

The sectors, if any, between the last sector addressable in CHS mode and the last sector addressable in LBA mode are known as "orphan" sectors. A device may or may not allow access to these sectors in CHS addressing mode.

The values in words 1, 3, and 6 are selected such that the number of orphan sectors is minimized. Normally, the number of orphan sectors should not exceed ([word55] x [word56] - 1). However, the host system can create conditions where there are a larger number of orphans sectors by issuing the INITIALIZE DEVICE PARAMETERS command with values other than the values in words 3 and 6.

Annex C
(informative)
Signal integrity

C.1 Introduction

The ATA Bus (a.k.a. IDE bus) is a disk drive interface originally designed for the ISA Bus of the IBM PC/AT™. With the advent of faster disk drives the definition of the ATA Bus has been expanded to include new operating modes. Each of the PIO modes, numbered zero through four, is faster than the one before it (higher numbers translate to faster transfer rates). Modes 0, 1, and 2 correspond to the ATA interface as originally defined. PIO Mode 3 defines a maximum transfer rate of 11.1 MB/s and PIO Mode 4 defines a maximum rate of 16.7 MB/s. Additional DMA modes have also been defined, with Multiword DMA Mode 0 corresponding to the original interface, and DMA Modes 1 and 2 being faster transfer rates. Multiword DMA Mode 2 is the same speed as the new PIO Mode 4.

With this increased speed, the weaknesses of the original ATA cabling scheme have become apparent on desktop systems. System manufacturers, chipset designers, and disk drive manufacturers must all take measures to insure that signal integrity is maintained on the bus. The areas of concern are:

a) ringing due to improper termination;
b) crosstalk between signals;
c) bus timing.

The intended audience for this annex is digital and analog engineers who design circuits interfacing to the ATA bus. Familiarity with the ATA specification and a basic understanding of circuit theory is assumed.

C.1.1 The problems

Early implementations of the ATA bus used LS-TTL parts to drive an 18-inch cable. The slow edges of LS-TTL and the short cable length worked well at the time. PIO Modes 3 and 4 demand higher performance. In an effort to cut cycle times, edge rates have inadvertently been increased, causing ringing on the cable and increased crosstalk between adjacent signals.

When an ATA host adapter was little more than a few buffers and some gates there was no issue with host adapter timing. With the advent of local bus architectures and faster transfer rates, timing issues have become more important. Propagation delay with worst-case loads must now be taken into account when designing host adapters.

One of the frequently asked questions is why are problems with ringing on the ATA bus seen now when they were not seen before. The answer is in the edge speed of the logic. How the edge speed changed can be found by looking at the history of the IBM PC.

When the IBM PC/AT™ was introduced in 1983, the 8 MHz 80286 processor quickly became the dominant platform. The AT bus (now called the ISA bus) became standardized around an 8 MHz processor speed. When the first ATA disk drive was introduced a few years later, it was designed as a simple extension of the bus – hence the name “AT Attachment” interface (see figure C.1). The idea was to remove the disk drive controller electronics from the PC and place them on the drive instead. What remained on the PC was a pair of bidirectional data buffers and an address decoder. This simple interface was most often implemented with a pair of 74LS245 buffers and a programmable logic device such as a PAL. These TTL devices had rise and fall times in the 5 to 6 ns range. Although this was fast enough to cause some ringing on the ATA bus, it was not so severe as to prevent millions of successful system implementations.

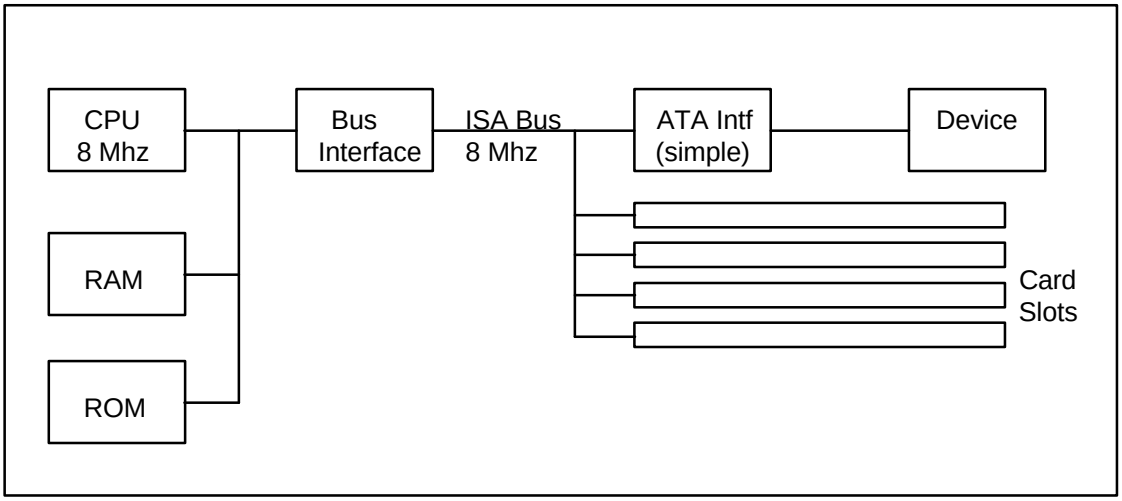


Figure C.1 – Original IBM PC/AT architecture

The architecture of modern PCs has changed somewhat from the original PC/AT™. As the processor speed increased it became necessary to separate the processor bus from the ISA bus (see figure C.2). To maintain compatibility the ISA bus continues to run at an 8 MHz rate. Processors, and their associated busses, have increased from 8 MHz to 12, 16, 25, and now 33 Mhz.

NOTE – Processors that run faster than 33 MHz, such as the 486DX2-66, still tend to keep the external processor bus at 33 MHz.

Disk drives have also increased in speed. The increase in rotational speed and linear bit density has increased the rate at which data comes off the heads, and the presence of cache on the drive makes data available at the access rates of RAM. This has created a data bottleneck at the ISA bus. The drive is faster, the processor is faster, but the data can't be moved from one to the other any faster.

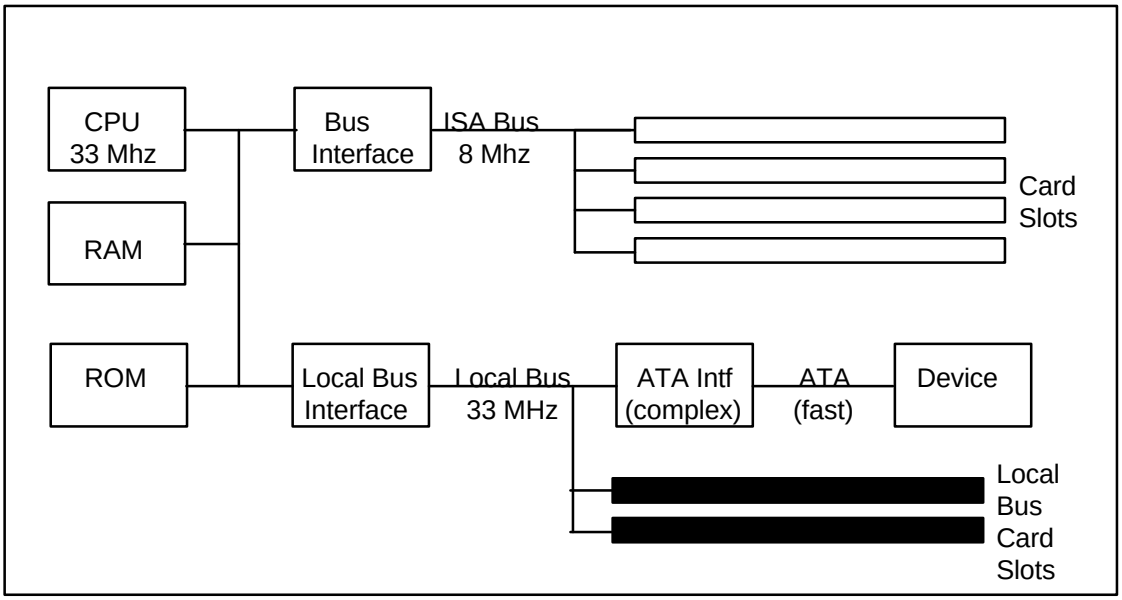


Figure C.2 – Modern PC architecture

This bottleneck inspired the invention of new, faster interfaces to the processor. Local busses are designed to run at the speed of the processor bus. Two local bus standards have emerged, the VESA Local Bus (VLB) and the Peripheral Component Interconnect bus (PCI). These local busses have the potential for faster data transfer from the disk drive to the processor.

To allow ATA disk drives to transfer data faster, the ATA standard had to be updated to allow faster transfer rates. These enhanced modes are still not as fast as a processor bus. To synchronize the data flow between 32-bit 33 MHz processor busses and slower 16-bit disk drives, a VLSI chip is required. Most of these bridge chips were implemented with fast CMOS processes to achieve the required bus speeds. As a result the edge rates on the ATA bus were often 1 to 2 ns, and sometimes less. These fast edges have aggravated the ringing on the bus to the point that system/drive combinations fail to work.

In summary, the reason for signal integrity problems appearing now, when they were absent before, is the advent of faster transfer rates on the ATA bus coupled with a change of IC process at the interface. The problems are not insurmountable, and in time it is likely that the ATA bus will be known as a robust, fast, and inexpensive interface.

C.1.2 The goals

The recommendations in this document make the following assumptions. The word “device” is used generically to describe disk drives and other peripheral devices on the ATA bus.

- Backward compatibility must be maintained. Old devices must work with new host adapters, and old host adapters must work with new devices.
- The ATA-3 standard must be followed as closely as possible. Without this, solutions implemented by different manufacturers will tend to diverge, creating incompatible systems.
- Solutions must be simple and inexpensive. The market for ATA products is very cost sensitive.

C.2 Termination

When analyzing the ATA bus, the standard 18-inch ribbon cable used to connect devices could be considered to be either a transmission line or a lumped LC circuit. Analog circuit designers generally use the rule of thumb that if the edge rate is less than four times the cable propagation delay, then it is a transmission line. Otherwise, it can be considered to be a lumped LC.

> NOTE – Different ratios are used by different designers. A survey of textbooks shows that values of three times, four times, six times, and even sqrt(2*pi) have been suggested.

The cable used almost exclusively is a PVC-coated 40-conductor ribbon cable with 0.05 inch spacing. This cable can be modeled as a transmission line with a typical characteristic impedance of 110 ohms and propagation velocity of 60% c. This gives a propagation delay of 2.5 ns. The edge rates from both hosts and devices are usually faster than 10 ns (4 x 2.5 ns), so a transmission line model applies.

> NOTE – Measurements taken on a sample cable gave an impedance of 107 ohms and a delay of 2.6 ns (59% c propagation velocity).

C.2.1 The problem

Many users have experienced problems with early implementations of PIO Mode 3 devices and hosts. Most failures in the systems observed can be attributed to signal integrity problems on the control lines that go from the host to the device. The problem appears most frequently as ringing on the DIOR- (read command) and DIOW- (write command) lines.

During a read cycle when DIOR- is asserted, it is possible for the ringing to create a short duration deassertion pulse (see figure C.3). This pulse occurs early in the read cycle. Inside the ATA interface portion of the datapath controller chip is a FIFO buffer that contains the data to be read. The extra pulse on the DIOR- line advances the FIFO pointer by one. This results in losing one word of data. The host system read operation therefore receives one word too few, and the remaining bytes are shifted. A typical data sequence might look like . . .W7, W8, W9, W11, W12 . . . Notice that word 10 is missing from the returned data. This

also means that the host tries to read one more word from the device than the device has remaining. Depending on the implementation of the BIOS, this locks-up the system or simply returns a byte of garbage at the end of the sector.

Pulse slivers due to ringing on the DIOW- line cause a similar problem during writes. The pulse sliver advances the FIFO pointer by one unexpectedly, writing an extra word of garbage into the FIFO. Subsequent data bytes are shifted by one word. A typical stored data sequence on the device might look like . . . W7, W8, W9, XX, W10, W11 . . . In this example an extra word was inserted during the write cycle for word 10. From the device's point of view, the host is trying to write 514 bytes rather than the expected 512 bytes. The device throws away the final word and should flag an error. A properly written BIOS detects this error and indicates a problem to the user.

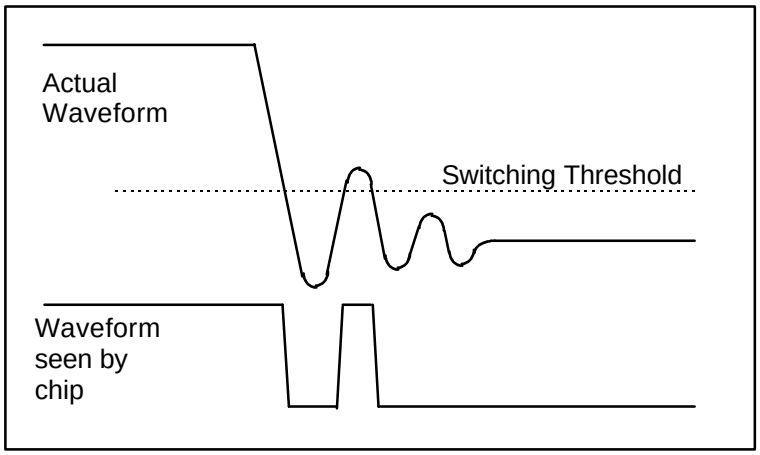


Figure C.3 – Typical ringing on ATA bus and its effect

These are only two examples of a systemic problem. Ringing on any control signal, and possibly on data lines, can cause system failures or data loss. To address this problem it is necessary to examine the circuit structure of the ATA bus.

Figure C.4 shows the seven basic driver/receiver structures that appear in ATA bus interfaces. The host circuitry appears on the left side of the diagram and the device circuitry appears on the right. The first circuit in figure C.4 shows the structure of the seven control lines that go from the host to the device. A SPICE model of the circuit is designed if some assumptions are made about the circuitry at the host and device. Virtually all devices today use a CMOS VLSI chip as part of the bus interface. This high-impedance input is modeled with clamp diodes to supply and ground and a typical input capacitance of 8 pF (see figure C.4). Since the ringing problem is worse with CMOS VLSI bridge chips at the source the host is modeled as a voltage source with 1 ns edges, a 12 ohm output impedance, and clamp diodes to supply and ground. The ribbon cable is modeled as a 110 ohm transmission line. The resulting SPICE model appears in figure C.5.

The simulation results in figure C.6 show the waveforms at both the host and device ends of the cable. The signal at the device end has ringing of sufficient amplitude to cause false triggering of the device. This is confirmed by transmission line theory which indicates that ringing will occur whenever the source impedance is lower than the characteristic impedance of the cable, and the termination is of higher impedance than the cable. The greater the mismatch, the greater the amplitude of the ringing. The oscilloscope trace shown in figure C.7 confirms the results of the simulations.

The latest trend in ATA interface chips has aggravated the ringing problem. In an effort to decrease propagation delay, some bridge chip manufacturers have increased the output drive current of the host in order to slew the output signal faster with the capacitive load of the cable. This has caused the edge rates and the output impedance to decrease, both of which increase the ringing at the device end of the cable. The oscilloscope trace in figure C.7 uses a generic driver and receiver – the problem of ringing is a fundamental characteristic of the ATA interface. This has not always been the case.

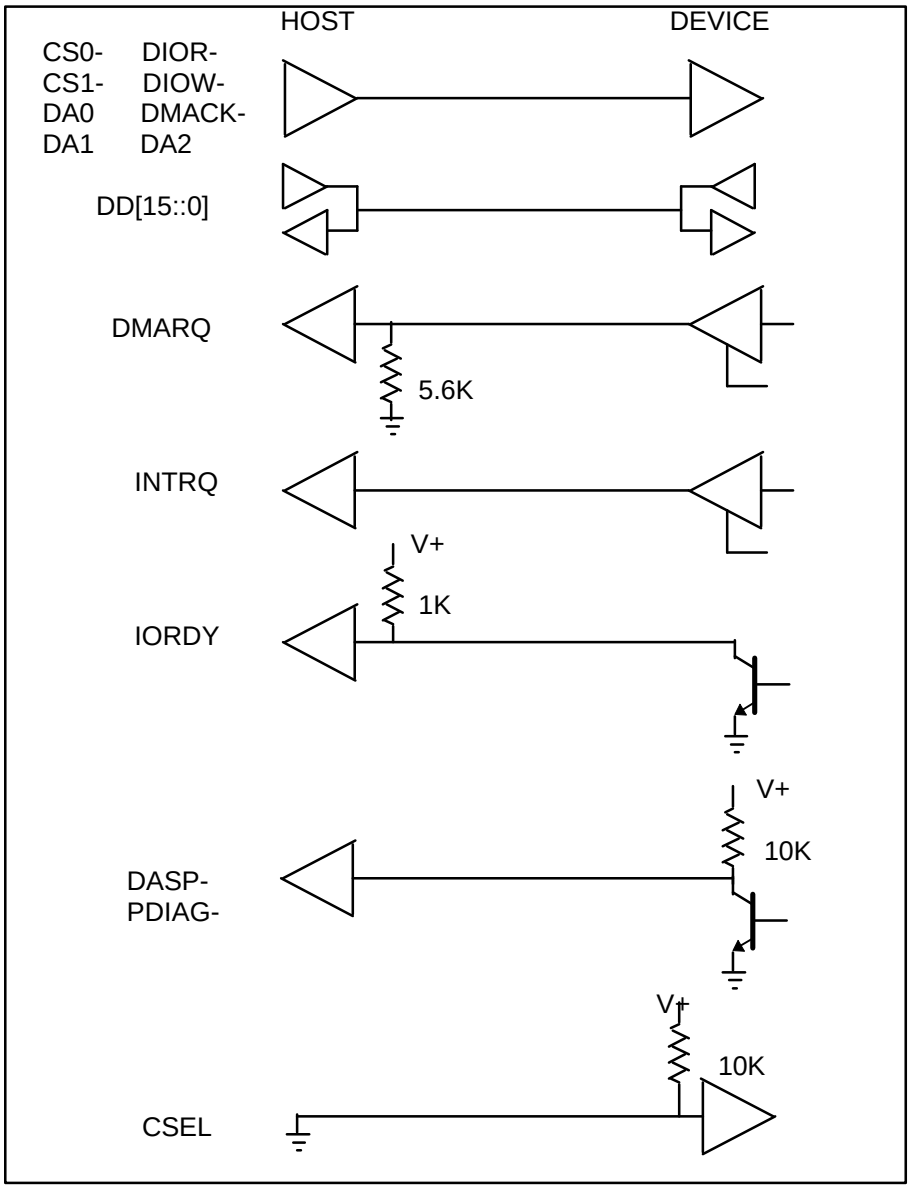


Figure C.4 – The seven basic ATA driver/receiver structures

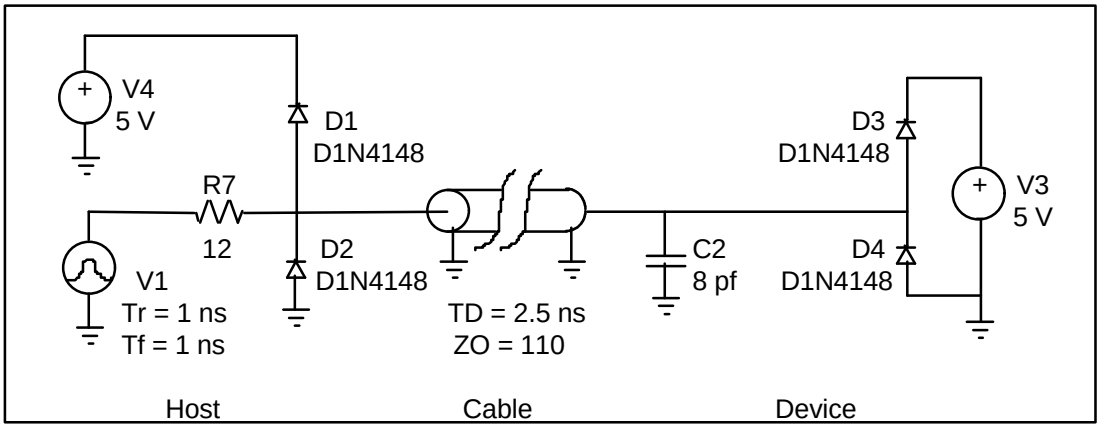


Figure C.5 – Schematic of SPICE simulation model

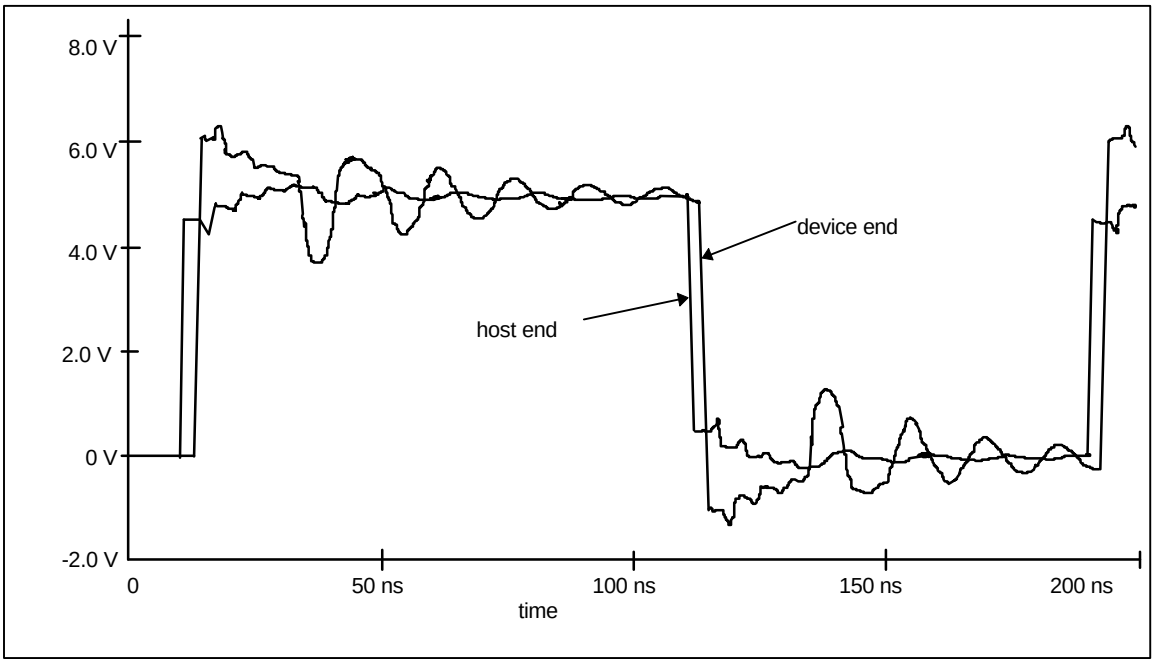


Figure C.6 – Simulation waveforms at host and device ends of cable

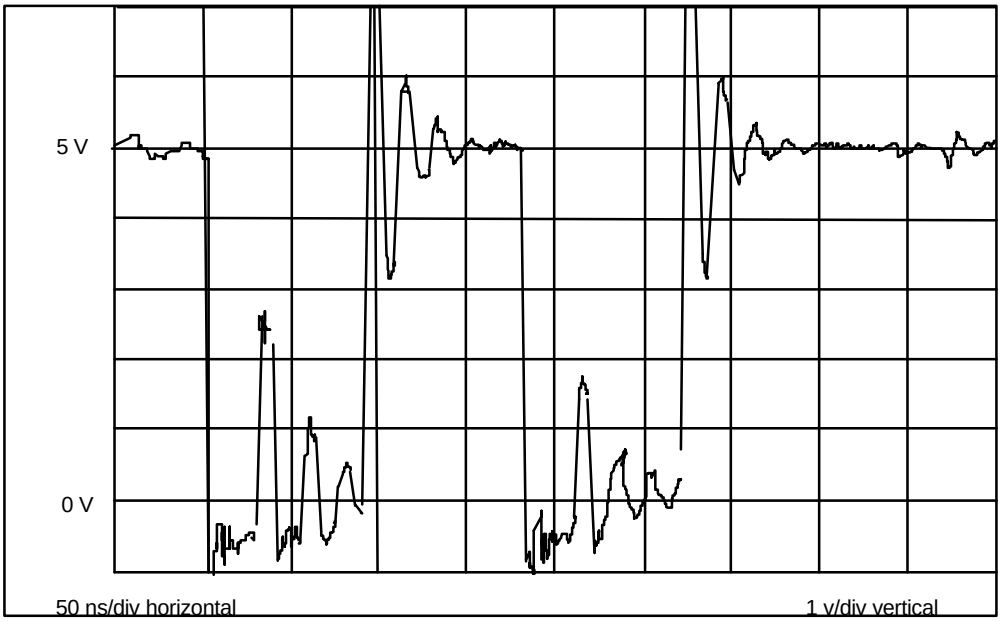


Figure C.7 – Oscilloscope trace at device end of DIOR- signal on a typical system

C.2.2 What are the options?

The proper solution is to terminate the transmission line. Either a series termination at the source or a parallel termination at the device is acceptable. Unfortunately, each of these solutions has problems of its own. A 110 ohm termination at the device end causes excessive DC loading. Having a termination on both devices in a two-device configuration results in too low of a load impedance, causing reflections on the cable again.

Matching the source impedance of the host to the cable has similar problems. The impedance required is different when the host is in the middle of the cable as opposed to being at the end. Even with the host at one end of the cable, ringing can occur with a two-device configuration. This is because the input impedance of the devices is not infinite: they appear as a reactive load due to their input stray capacitance.

The SCSI interface standard avoids ringing by requiring terminations at each end of the physical cable and having each device drive the cable with a current sink. However, real SCSI configurations often have too many, too few, or improperly located terminations. Changing the ATA standard to a user-installed termination scheme loses all backward compatibility and is therefore not considered to be a viable option.

One of the solutions used in the past to “fix” failing ATA configurations has been to place a capacitor at the input of the device. Since the ringing is the result of a resonant system, adding purely reactive elements (capacitors and inductors) which simply change the frequency of oscillation is not recommended. These elements may fix a given configuration of a device and cable, but they really just move the interfering resonance peaks to a different frequency, solving the problem only for that particular configuration. Proper solutions include resistive elements to dissipate the energy stored in the transmission line.

No single solution meets the dual criteria of solving the ringing problem and being backward compatible with current systems. The suggested approach uses partial solutions in three different areas: partial termination at the host, partial termination at the device, and edge rate control at both the host and the device.

C.2.3 Design goals

Before a solution can be designed the design goals must be explicitly stated. This leads to the question of “How much ringing is acceptable?” To answer this question the design and specification of the ATA bus is considered.

The ATA bus was originally designed to use standard TTL signals. TTL was designed with built-in noise margin. All drivers are required to have a “low” (zero) signal level of 0.5 V or less, and a “high” (one) signal level of 2.4 V or more. All receivers are specified to accept any signal below 0.8 V as a logical zero and any signal above 2.0 V as a logical one. This results in a low-side noise margin of 0.3 V (0.8 - 0.5) and a high-side margin of 0.4 V (2.4 - 2.0). Signals between 0.5 V and 2.0 V are in no man’s land, interpreted by the receiver as either a zero or a one. TTL compatible inputs typically use a switching threshold of 1.3 to 1.4 V.

Bus designers have long known that the noise margins of TTL are insufficient for signals passed on cables. To improve the noise margin inherent in TTL systems, hysteresis has been added to the receiver input. Hysteresis changes the input switching threshold depending on the present state of the logic output of the receiver. For example, if the receiver is currently in a zero state, it might require an input voltage of 1.7 V before changing to a one. Once in a one state, the receiver might require the input voltage to drop below 0.9 V before changing back to a zero. Modern design practice dictates that all signals passing across a bus be received with hysteresis.

It is desirable that, even with ringing, the input signal remain less than 0.5 V after a falling edge and remain above 2.4 V after a rising edge. With CMOS drivers only the falling edge is of concern. This is due to the input switching threshold of TTL (typically 1.4 V) being closer to ground than to the supply. It turns out that designing to the 0.5 V requirement is too restrictive, so the looser requirement of 0.8 V is used here. This relaxed requirement essentially removes the noise margin inherent in TTL and depends on receiver hysteresis for proper operation. As input hysteresis has been the norm in drive design for many years now, this limitation is not considered unreasonable.

Depending on system timing and other issues, a designer may elect to use a looser threshold of 0.9 V or a tighter one of 0.7 V. For these cases circuit simulation of the bus and receiver is done to verify the design. The resulting termination circuits have different values from those derived here.

C.2.4 Source termination

A series resistor at the source (host) acts as a termination to the transmission line. When the value of the resistor matches the characteristic impedance of the cable (110 ohms) then the ringing is reduced to zero. Resistor values less than 110 ohms will partially terminate the cable and reduce the ringing.

NOTE – This assumes that the output impedance of the driver is zero. In reality, an optimum match occurs when the output impedance and the series resistor together equal the cable impedance.

The ATA specification requires that a source sink 4 mA while maintaining a logical low output voltage of 0.5 V or less (see 4.3). Adding a series resistor in the output of the driver causes the output logical zero voltage to increase with greater resistance. For example, if the unterminated logical zero output of the driver is 0.4 V, then a maximum series resistance of 25 ohms is allowed ((0.5-0.4)/4 mA). This DC voltage drop requirement acts in opposition to the higher resistance values required for cable termination. A 5%, 22 ohm resistor meets the 25 ohm requirement. Note that this places an addition requirement on the host interface chip: timing measurements use a logical threshold of 0.4 V rather than 0.5 V as in the past.

Is a 22 ohm resistor adequate for reducing the ringing? The simulation was repeated using the same model as shown in figure C.5 with a 22 ohm series resistor added. The results of that simulation appear in figure C.8. The ringing is significantly reduced from the previous simulation in figure C.6.

For maximum ringing it is assumed that the device(s) have CMOS input stages that do not provide significant DC loading. Yet for the series termination resistor calculation it is assumed a logical low sink current of 4 mA. Both of these conditions cannot simultaneously occur in practice, but assuming the worst-case sink current gives the best compatibility with older devices.

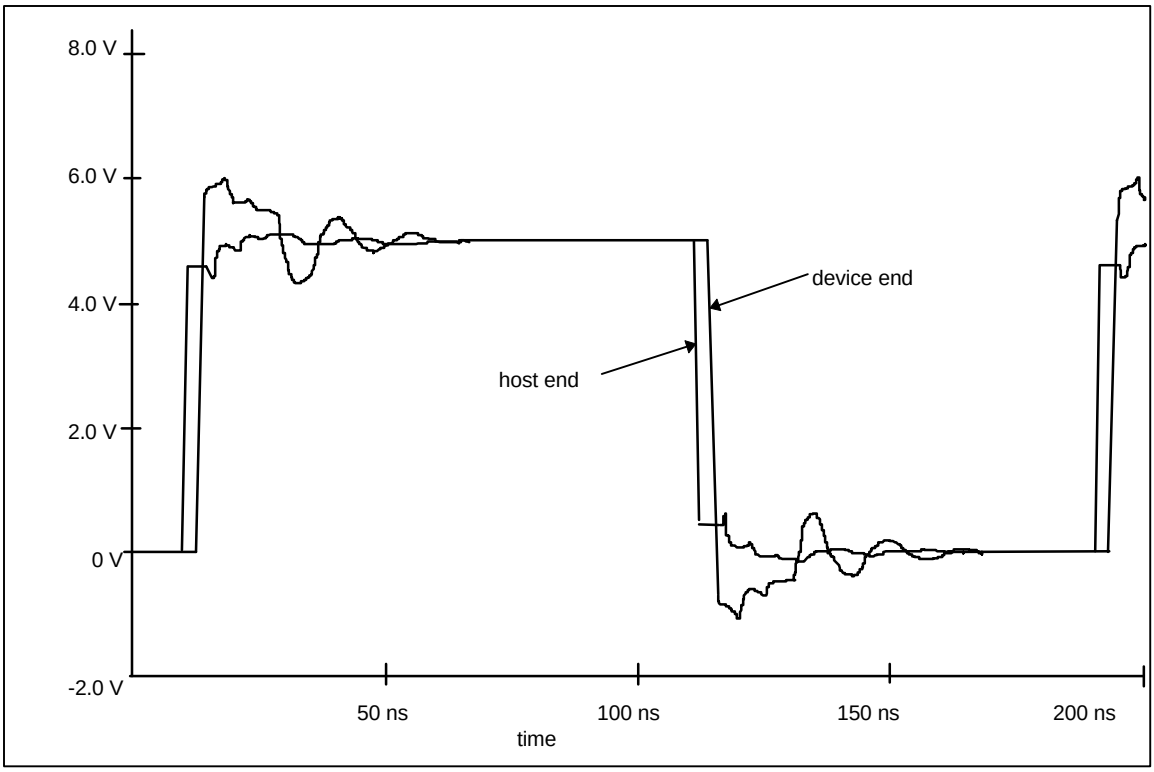


Figure C.8 – Waveforms with 22 ohm series resistor at source

C.2.5 Receiver termination

Receiver termination is more difficult than source termination. Viable solutions must work with one or two drives located anywhere along the cable. The host may be located at one end or in the middle of the cable. The host may or may not have termination. These and other considerations make drive termination a multifaceted problem.

The first constraint is the maximum DC loading allowed. The ATA specification requires that the host be capable of providing 400 µA of current while in a logical one state. Assuming each device is allowed to take half of that amount, the minimum DC resistance allowed is 25K ohms.

NOTE – This assumes a CMOS output with a high output voltage of 5.0 V : 5.0 V/200 µA = 25 KΩ

For a 110 ohm transmission line, 25K ohms is as good as infinity. This means that any practical termination solution must not have significant DC loading.

One way of terminating the cable is with an "AC termination." This is a simple RC network that provides termination for high-frequency signals but does not load the line at DC (see figure C.9). This circuit acts as both a cable termination and a filter for the ringing. The termination characteristics can be observed by looking at the ringing signal at the host when the circuit is connected or removed. When the circuit is in place, less energy is reflected back to the host, so the host waveform has less ringing. The lowpass filter characteristics of the circuit help decrease the amount of ringing presented to the interface circuitry of the device.

Although this may appear to be an unusual method of terminating the cable, it is not without precedent. The IEEE P996 committee recognized the problems inherent in the design of the IBM PC/AT™ bus and recommended a series RC termination for increased "data integrity and system reliability." They suggested that the termination circuit be added to each end of the backplane or motherboard. The recommended values are 40 to 60 ohms for the resistor and 30 to 70 pF for the capacitor.

Deriving the optimum values for an ATA bus AC termination circuit is difficult. The easiest way of determining the values is to perform a number of trial-and-error SPICE simulations for different host and device configurations. The recommended values are 82 ohms and 10 pF. Simulations show that capacitance values between 8 pF and 20 pF work well. Since the input capacitance of many interface chips is between 8 and 10 pF, a discrete capacitor is often unnecessary. This reduces the cost of implementation on the device. A conservative approach is to place pads so additional capacitance can be added if required.

Device manufacturers need to ensure that any partial termination circuits they implement present an effective capacitance of 20 pF or less. What is an effective capacitance? From a practical point of view, any circuit is valid provided it does not increase the propagation delay of a worst-case cable. This is because systems manufacturers are counting on a certain cable delay in their design. The easiest way to answer the question of acceptability is to run a SPICE simulation and measure the delay. The simulation should be run twice: once with a simple 20 pF load, and again with the proposed termination circuit. If the resulting delay of the proposed termination circuit is less than or equal to that obtained with a 20 pF load, then it meets the criterion for acceptance. The recommended termination of 82 ohms and 10 pF passes the test.

The major drawback of the RC termination circuit is that it adds delay to the signal. Since the ATA specification defines the timing at the input to the device (see clause 10), device manufacturers must ensure that their interface chip still works properly with the additional delay. The delay can be calculated for rising edges (2.0 V threshold) and falling edges (0.8 V threshold) with a fairly straightforward SPICE simulation. For the 82 ohm and 10 pF termination the delay is less than 1.5 ns.

NOTE – 0.7 ns for the rising edge, 1.2 ns for the falling edge, derived from simulations.

Will termination at both the host and the device "over-terminate" the transmission line? Figure C.10 shows the simulation results for device termination with no host termination, and figure C.11 shows the same simulation with a 22 ohm host termination added. It is clear that termination at both the host and the device results in the best signal integrity. To completely confirm the validity of the termination circuits more simulations must be performed with source termination and two devices with receiver termination; two devices, one with and one without termination; etc.

Another option for controlling ringing at the device is the use of a clamping circuit. Biased diodes have been shown to be excellent solutions, reducing the ringing to virtually zero. The advantage of clamp circuits is that they do not require any components in series with the signal, and therefore do not add any delay. This is particularly important for PIO Mode 4 operation. The disadvantage of clamping circuits is that they take considerably more space on the circuit board and cost much more than passive elements. Some implementations have used clamping circuits on sensitive edge-triggered lines (such as DIOR- and DIOW-) and used passive terminations on less sensitive lines (such as data). Clamping circuits work well both with and without host-end termination and are worthy of further investigation.

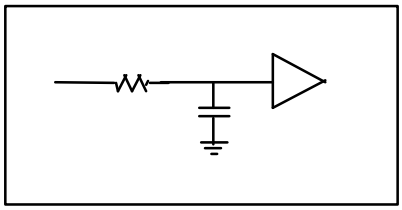


Figure C.9 – AC termination circuit at device end of cable

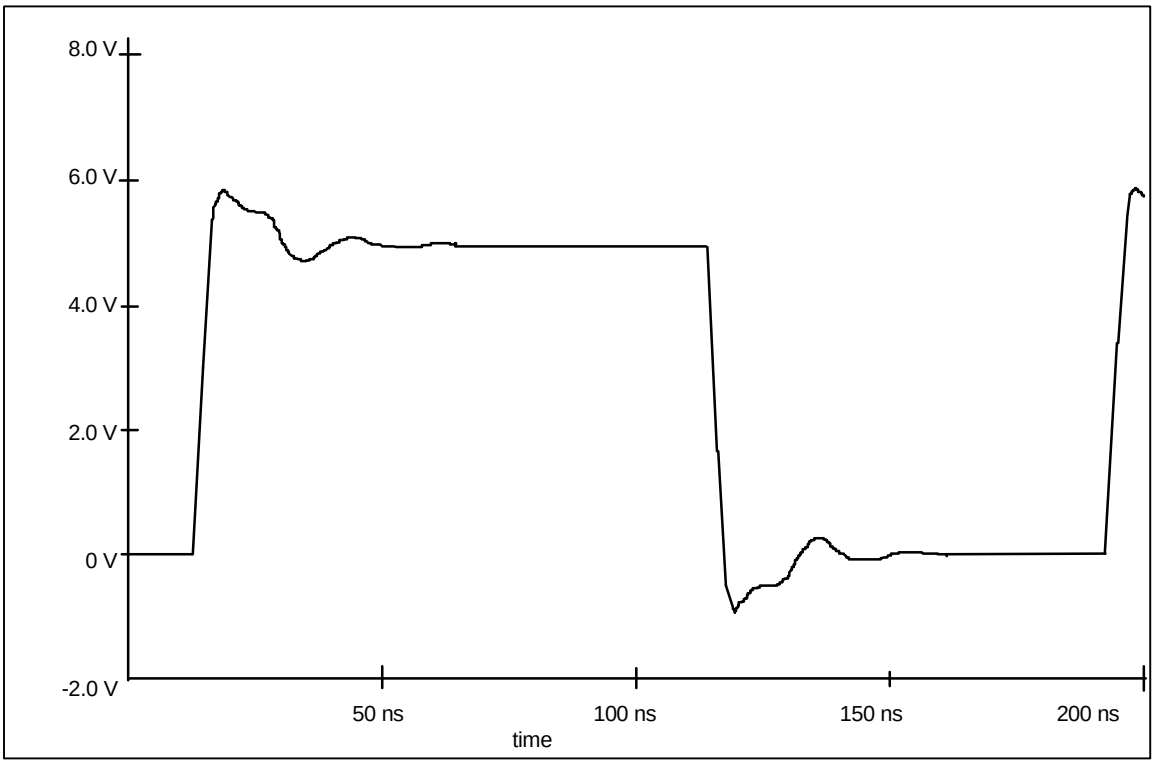


Figure C.10 – Device waveform with device termination and no host termination

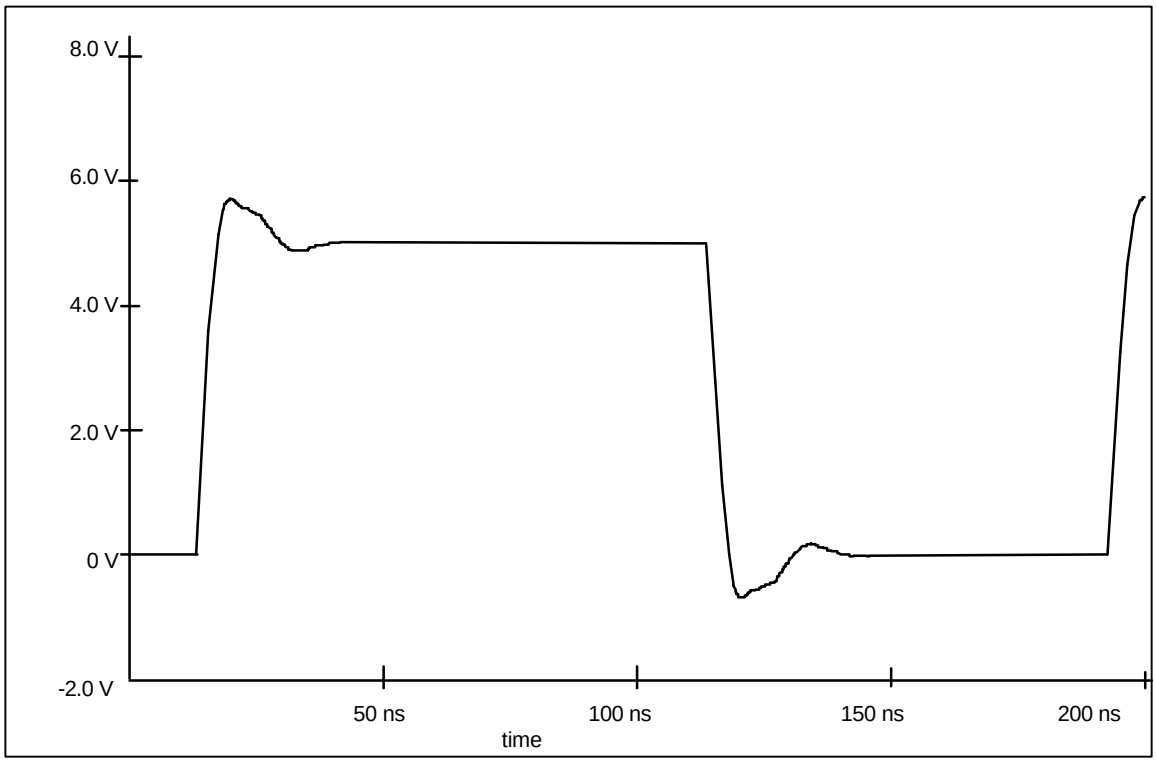


Figure C.11 – Device waveform with both device and host terminations

C.2.6 Edge rate control

The ATA specification requires that all sources have a rise time of not less than 5 ns (see 4.3). The original intent of this requirement was to avoid transmission line problems on the bus. One of the common misconceptions is that limiting the rise time of the source to 5 ns will fix the ringing problem.

A rule-of-thumb for analog designers is that when the propagation delay of the cable exceeds one-quarter of the signal rise time, cable termination be used.

> NOTE – In reality this rule-of-thumb varies considerably. Various books use values of one-half, one-third, one-fifth, and even one over the square root of two times pi.

In the case of the ATA bus, the worst case propagation delay of the cable is approximately 4 ns so by this rule rise times of less than 16 ns require termination. Many local bus to ATA bridge chips available today have rise times of 1 to 2 ns, in violation of the ATA requirement of 5 ns.

> NOTE – Assuming 18-inch cable, 60% c velocity factor; two drives, each drive having a maximum load of 25 pF.

The ATA document says that the rise time must be a minimum of 5 ns into a 40 pF load. The easiest way to implement this from a chip designer's point of view is to decrease the drive of the I/O cell until the timing requirement is met. Unfortunately, very few systems in the real world ever approach 40 pF. Although the cable and the devices have maximum capacitance specifications, these capacitance values are never seen by the host. At DC and low frequencies the cable looks like a capacitor. But at high frequencies (or fast edge rates) the cable appears as a transmission line.

One of the results from transmission line theory is that a properly terminated transmission line appears to be a resistor with no capacitance or inductance. From the driving end of the line the transmission line looks just like a resistor whose value is the characteristic impedance of the line. The distributed capacitance of the transmission line does not appear as a capacitive load: it interacts with the inductance of the line and the termination to appear resistive. As a result, real-world systems rarely see more than 30 pF of capacitive loading at the host. The reduced capacitance causes the I/O cell to slew faster, creating rise times less than 5 ns.

The best solution is to use special I/O cells that have slew rate feedback to keep the rise time at 5 ns regardless of load. These are more difficult to design than conventional I/O cells and consume more die area. This could be a problem for interface chip designs that are already pad ring limited. Another approach is to use a conventional I/O cell that is designed to have 5 ns rise times into a 10 pF or 20 pF load. The total delay of the cell is greater for heavier loads, but the maximum delay is determined with SPICE modeling of a worst-case cable and load.

Rise time control is still an important tool for controlling ringing. Although it is not the total solution, simulations show marked improvement between sources with 1 ns rise times and sources with 5 ns rise times. Slower rise times give the added benefit of reduced crosstalk.

C.2.7 The solution: A combination

No one element – source termination, receiver termination, nor rise time control – completely addresses the problem of ringing on the ATA bus. The recommended solution is a combination of all three. Each item must be enough to exert some control over the ringing problem in order to maintain backward compatibility. With the faster transfer rates of PIO Mode 4 (and DMA Mode 2) it is even more important to control undesired ringing on the bus.

The above discussion only addressed a particular group of signals driven by the host and received by the device. There are other signals driven by the device and received by the host that are equally susceptible to ringing. These signals need termination, but in the opposite manner. The device inserts 22 ohm resistors in series with signals it drives and the host has an RC (or just R) receiving end termination.

The data lines are different in that they are data bidirectional. Strictly speaking, the data lines are not edge sensitive and are unaffected by ringing. This is true as long as the data signals have sufficient setup time to allow for bus settling. The settling time is as long as 60 ns in severe cases. Excessive ringing on the data lines induces spurious signals on adjacent control lines (crosstalk). Good design dictates that some type of ringing control be used on data lines, but perhaps not as much as on edge-sensitive control lines. A good compromise is to insert 22 ohm series resistors on data lines at both the host and the device. The driving end sees the same source termination as before. The receiving end sees an RC network of 22 ohms combined with the input capacitance of the interface chip. This is enough to substantially reduce the ringing and minimize settling time.

The one remaining bus structure not discussed is the open collector output driven by the device (IORDY). This signal is driven by a current source rather than a voltage source. Usually the transistor driving this signal is relatively slow and does not cause an excessive amount of ringing. The nature of IORDY makes it relatively insensitive to ringing that might occur.

Table C.1 summarizes the recommended changes to the signal lines on the ATA bus.

Table C.1 – Recommended termination

Signal name	Host termination	Device termination
DIOR-, DIOW-	22 ohm series	82 ohm series
CS0-, CS1-	22 ohm series	82 ohm series
DA0, DA1, DA2	22 ohm series	82 ohm series
DMACK-	22 ohm series	82 ohm series
RESET-	no change	no change
DD0 through DD15	22 ohm series	22 ohm series
DMARQ	82 ohm series	22 ohm series
INTRQ	82 ohm series	22 ohm series
IORDY	no change	no change
DASP-, PDIAG-	no change	no change
CSEL	no change	no change
NOTE – For the 82 ohm series termination, an additional parallel capacitor may be needed if the interface chip and circuit board layout have less than 8 pF of capacitance.		

C.2.7.1 Example of device-end termination timing

Assume that 82 ohm series resistors are inserted on all receive signals and 22 ohm series resistors on all transmit and bidirectional signals. Also assume that the input capacitance of the interface chip is 10 pF. There are three different RC configurations that occur (see figure C.12). All receive signals will see an 82 ohm and 10 pF network. The data lines will see a 22 ohm and 10 pF network when the device is receiving data. Signals driven back to the host (including data lines during a read) will see 22 ohms and 50 pF. The 50 pF assumption is the worst-case condition of both the host and another device being located nearby (negligible cable length), and both of them having the maximum allowed input capacitance.

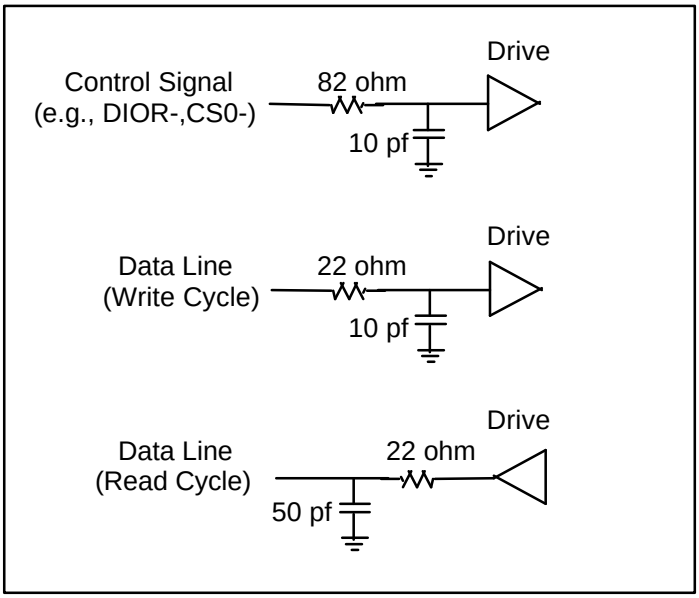


Figure C.12 – Signal models for device-end timing calculations

A simple SPICE simulation with a signal source and an RC load will show what the delays are through these three networks. Because the switching thresholds are not symmetrical with respect to the supply (0.8 V and 2.0 V) the delay for rising edges is different than that for falling edges. Since the input edge rate is unknown, both fast and slow edge inputs are simulated. The worst-case delay occurs with slow edges for rise times and fast edges for fall times. This mixture of slow rise time and fast fall time does not occur in real life, but since the edge speed is not known the worst case is planned for. The SPICE signal source is programmed for a rise time of 6.25 ns (same as 5 ns for 10% to 90%) and a fall time of 0.1 ns. The net result is six delay values. The results of the SPICE simulations are shown in table C.2.

Table C.2 – Typical device-end propagation delay times

Symbol	Description	Value
Tphlc	Propagation delay, high to low, control line	1.0 ns
Tplhc	Propagation delay, low to high, control line	0.9 ns
Tphldi	Propagation delay, high to low, data in	0.5 ns
Tplhdi	Propagation delay, low to high, data in	0.3 ns
Tphldo	Propagation delay, high to low, data out	2.5 ns
Tplhdo	Propagation delay, low to high, data out	1.1 ns

These delay values, combined with the interface chip timing specifications, will give the timing at the pins of the device. The trick is to figure out how each one of the ATA timing parameters is affected by the delays.

For example, consider the DIOW- Data Setup time (ATA value t3). This is the amount of time that the data must be stable before the rising edge of DIOW-. Assume that the interface chip has a value of 2.0 ns. It is known that DIOW- is a control signal and the rising edge of control signals are delayed by 0.9 ns. This means that the setup time at the chip is actually greater than expected. But the data is delayed too. It is not known what the data pattern is so it is assumed that the delay time is the maximum of Tphldi and Tplhdi. The actual setup time is 2.0 + 0.9 - MAX(0.3, 0.5) = 2.4 ns. This is less than the ATA requirement of 30 ns (for PIO Mode 3) and therefore within spec.

This careful thought process must be repeated for all 15 of the ATA PIO timing parameters (and for DMA also). The easiest way to do this is to make a spreadsheet and enter the six values for RC delay and the interface chip timing parameters. Spreadsheet formulas can then compute the timing at the pins of the device and highlight any that are not within specification. In this manner the difficult calculations need only be derived once and it becomes easier to verify results.

C.2.7.2 Example of host-end termination timing calculation

The host-end timing calculations are similar to the device-end calculations described above with a few more complicating factors added in. The four different signal configurations are shown in figure C.13. For this design 82 ohm series resistors are used on control lines received by the host and 22 ohm resistors on the data lines and control lines driven by the host. It is assumed that the host adapter chip input capacitance plus stray capacitance is 15 pF.

For these values, the control signal out and the data out models look the same. One simulation can be used to determine both values. The greatest uncertainty is the delay through the cable for received signals. The total cable delay depends on the source impedance of the device. This can be anything from zero to 82 ohms; the greater the impedance, the greater the delay. It is assumed for this example that the device vendor has read this document and has decided to use 22 ohms resistors. If it is desired later to make a worst-case assumption of 82 ohms, then approximately 2 ns are added to the numbers.

Using SPICE models similar to the one shown in figure C.14 the eight delay parameters required are derived. A second device appears in the model as a lumped capacitance of 25 pF which causes the maximum delay. The resulting values appear in table C.3. By examining the values in the table it should be clear why the cable propagation delay is often referred to as being about 5 ns.

The process of finding the ATA timing values is the same as for the device-end example. The propagation delay times are added to and subtracted from the host adapter chip timings to obtain the timings at the input to the device, in this case calculating the timing at the drive furthest from the host adapter. The resulting timing values are compared against the ATA values to determine what mode the device operates at.

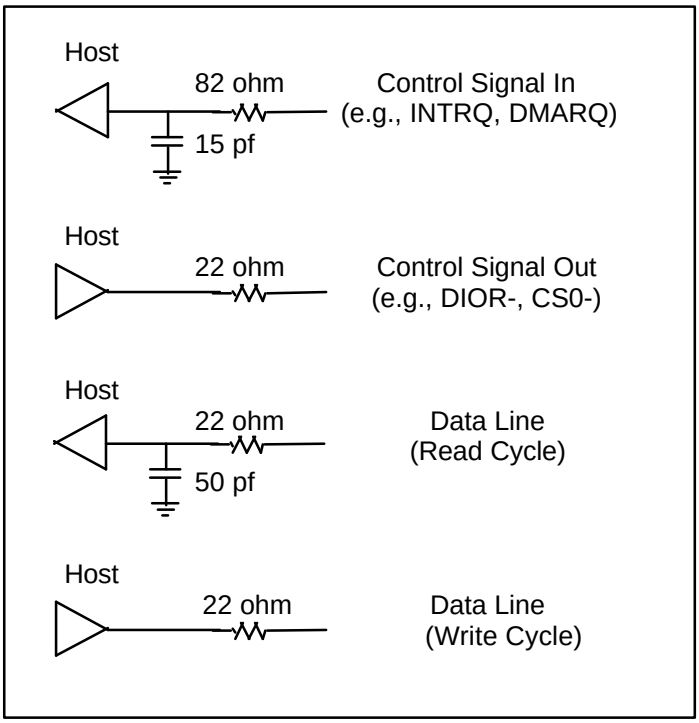


Figure C.13 – Host-end signal configurations with terminations

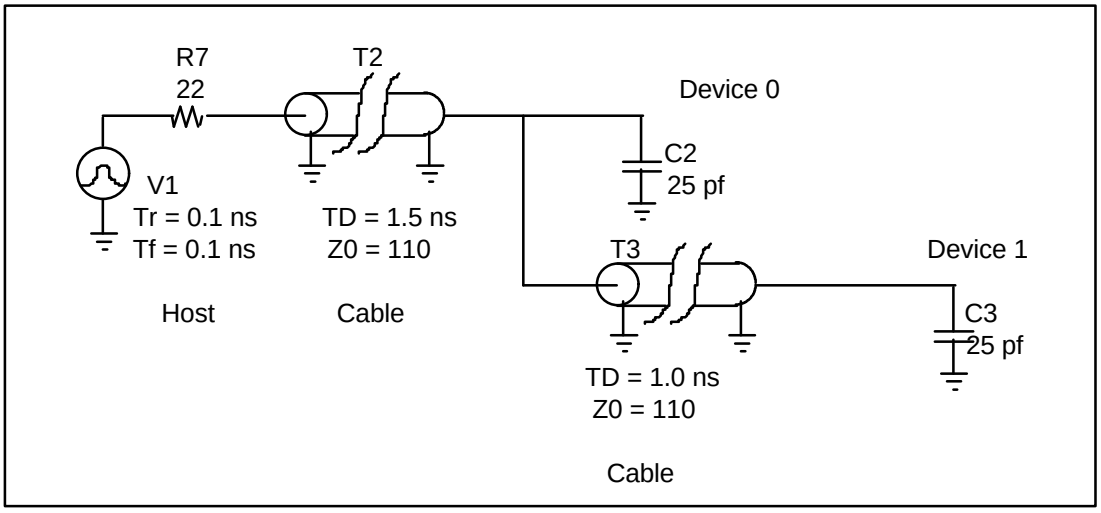


Figure C.14 – SPICE model for control signal out delay calculation

Table C.3 – Typical host-end propagation delay times

Symbol	Description	Value
Tphlci	Propagation delay, high to low, control in	6.4 ns
Tplhci	Propagation delay, low to high, control in	4.7 ns
Tphlco	Propagation delay, high to low, control out	5.9 ns
Tplhco	Propagation delay, low to high, control out	4.6 ns
Tphldi	Propagation delay, high to low, data in	5.7 ns
Tplhdi	Propagation delay, low to high, data in	4.3 ns
Tphldo	Propagation delay, high to low, data out	5.9 ns
Tplhdo	Propagation delay, low to high, data out	4.6 ns

C.2.8 Dual port cabling

One of the recent enhancements to the ATA bus has been the use of primary and secondary ports, allowing the user to attach up to four devices. The optimal way to implement dual ports is to have two completely separate interfaces that have no circuitry in common. This guarantees isolation between the ports and insures that no interference will occur.

> NOTE – At the 1995 Windows Hardware Engineering Conference (WinHEC), Microsoft recommended the use of fully independent primary and secondary ports.

The advent of local bus bridge chips has introduced new driving forces to the dual port cabling issue. Implementing two independent ATA ports on a single chip requires 66 I/O pins. Due to the cost of pins, some designs have combined the data lines of the two ports into one set of pins. Sharing the data lines (or any other lines) in this way without termination is asking for trouble. Simulations confirm that the ringing in such configurations is large and complex, particularly if the loads on the two cables are not balanced.

One alternative pin-saving solution would be to add a set of external buffers. This would require three new control lines but would save 16 data lines for a net improvement of 13 pins. This also would require additional packages on the circuit board.

An economical solution is to add independent series resistors for each line (see figure C.15). Energy reflected back from the first cable passes through one termination resistor before getting to the host. The reflected signal is further attenuated as it passes through the second resistor and into the second cable. This signal is reflected from the end of the second cable (with loss), and must pass through the termination resistor again before arriving at the host. This provides sufficient attenuation of reflected signals.

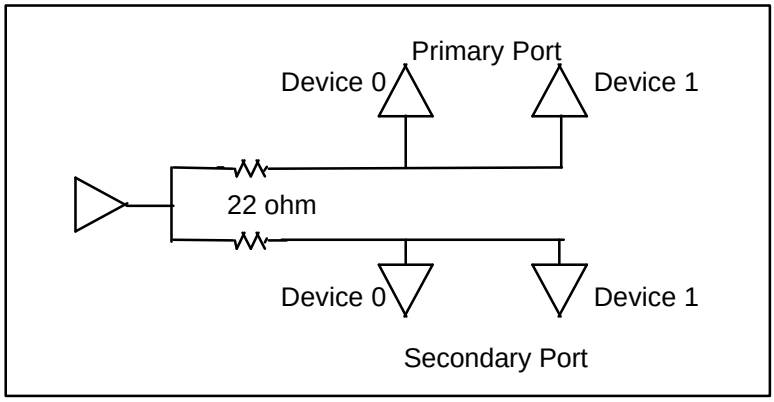


Figure C.15 – Preferred connection for shared lines in dual port systems

Not all of the signal lines in a shared dual port interface can be shared. If the chip selects (CS0-, CS1-) and the data strobes (DIOR-, DIOW-) are shared, then it is impossible to differentiate between the primary and secondary ports. A write to a device on one port causes the same action to occur on the other port, destroying the data on the other device. The data strobe lines are sensitive edge-triggered signals while the chip selects act more like level-sensitive address lines. It is recommended that designers share the less sensitive chip selects and not share the data strobes.

Table C.4 makes some assumptions about how the dual porting is being implemented. If the data lines are shared, there are not simultaneous accesses to the primary and secondary ports. This in theory allows the DMACK- and IORDY lines also to be shared. The INTRQ and DMARQ signals are driven by tristate buffers on the devices. Either Device 0 or Device 1 enables its tristate driver depending on the state of the DEV bit in the Device/Head Register. Therefore INTRQ and DMARQ cannot be shared because either Device 0 or Device 1 will be driving these lines at all times. The primary port devices do not know about the secondary port devices, so sharing these lines would create a conflict. In theory the DMACK- line could be shared since it is driven by the host. In practice this is not recommended. It is likely that some devices respond

unconditionally to the DMACK- signal, whether they ever requested a DMA cycle or not. This could lead to a conflict on a DMA cycle between a primary port device and a secondary port device during the data cycle. For these reasons the INTRQ, DMARQ, and DMACK- lines cannot be shared.

Table C.4 – Possible sharing of ATA signals in dual port configurations

Signal name	
DIOR-, DIOW-	Not shareable
CS0-, CS1-	Shareable
DA0, DA1, DA2	Shareable
DMACK-	Not shareable
RESET-	Shareable
DD0 – DD15	Shareable
DMARQ	Not shareable
INTRQ	Not shareable
IORDY	Shareable
DASP-, PDIAG-	Not shareable
CSEL	Not shareable

The DASP- lines cannot be shared. Assume there are two devices on the primary port, and one device on the secondary port. With the DASP- lines connected, the single device on the secondary port will incorrectly "see" Device 1 on the primary port. This would be a problem for all manufacturers who follow the ATA specifications. Similar problems can occur with the PDIAG- lines; they cannot be shared.

C.3 Crosstalk

Crosstalk is switching on one signal line causing induced signals in an adjacent line. Crosstalk has not been a significant issue in the past with slower edge rates; in newer systems the problem is often masked by ringing. Once the cable is terminated and the ringing is under control, then the presence of crosstalk becomes apparent.

C.3.1 Coupling mechanisms

There are two mechanisms by which a signal couples into an adjacent line. The first is coupling capacitance, and the second is mutual inductance. As a switching signal wavefront propagates down the cable it couples energy into the adjacent line. Once this energy is in the second transmission line, it propagates in both directions: forward toward the receiver and back toward the source (see figure C.16).

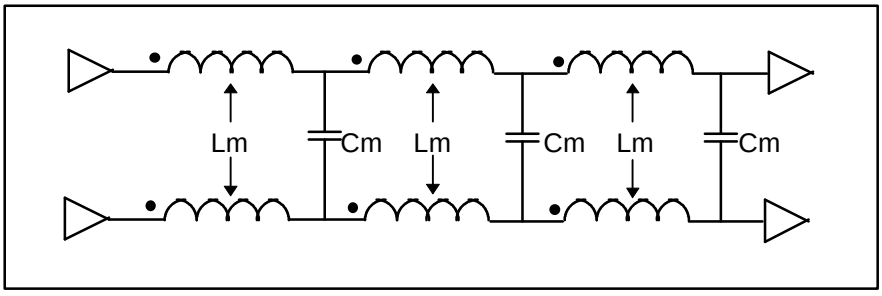


Figure C.16 – Crosstalk coupling mechanisms

First the forward coupling components are examined. The voltage induced in the second transmission line is proportional to the coupling coefficient, the inductance, and the rate of change of current in the primary side. This is a negative voltage: a positive current spike in the primary line results in a negative voltage spike in the secondary line.

The coupling capacitance between the two lines causes a current pulse in the secondary line proportional to the capacitance and the rate of change of voltage on the primary side. A positive voltage step on the primary line causes a positive voltage spike on the secondary line.

These two coupling mechanisms have some interesting characteristics. The polarity of the coupling is opposite for the mutual inductance and coupling capacitance. If the magnitudes of these effects are comparable, then they will cancel, resulting in no forward crosstalk. Unfortunately, accurately computing these values is difficult, and the easiest way to determine the actual amount of crosstalk is to measure it. The other noteworthy characteristic is that the magnitude of the coupled signal is proportional to the rate of change of the signal in the primary line. This is a major reason for controlling the slew rate on ATA bus drivers. Earlier it was said that ringing on the data lines is not necessarily a problem. Here it is seen that fast edge rates and ringing on the data lines can couple by crosstalk into adjacent control lines, causing control sequence errors through mistriggering. It is unlikely crosstalk from data lines causes observable failures in a laboratory environment. But the presence of crosstalk-induced voltage spikes on the control signals reduces the noise margin, and can increase the long-term error rate.

The amplitude of the coupled signal is proportional to the total amount of coupling capacitance and mutual inductance, and is therefore proportional to cable length. Once a line is terminated properly, ringing is no longer a function of length. This leaves crosstalk as the major factor limiting cable length.

Reducing crosstalk involves reducing the mutual inductance, reducing the coupling capacitance, or decreasing the source signal amplitude. Controlling the inductance and capacitance can be done by either keeping the length of the cable short or by increasing the distance between conductors. Placing a ground conductor between critical signals increases the separation of the signals and also adds a shielding effect from the intervening ground. In the ATA environment the only control that can be exercised over the cable is to keep the length at 18 inches or less. The amplitude of the source signal cannot be reduced and still maintain ATA compatibility, but there is control over some elements of the source signal. Slew rate limitation reduces the high-frequency components of the source signal and therefore reduces the coupling of these components into adjacent lines. Terminating the lines reduces ringing which also decreases the amount of energy coupled at the ringing frequency.

C.4 Bus timing

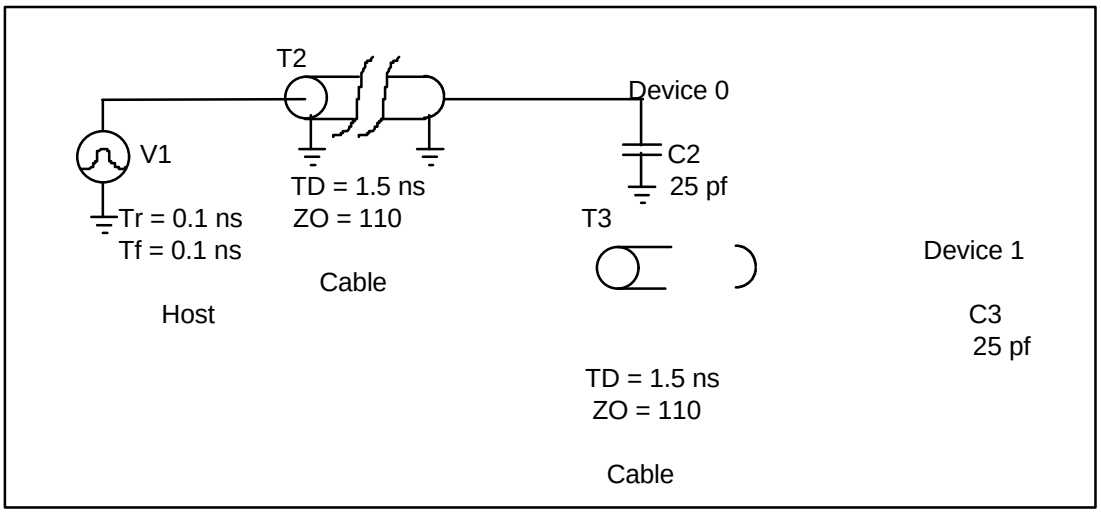
Terminating the ATA bus has its cost. Partial terminations at the host and the device increase propagation delays throughout the system. The ATA standard specifies that timing is referenced to the input pins of the device (see clause 10). This means that most of the timing issues must be addressed by systems manufacturers and bridge chip designers.

C.4.1 The issues

The most significant timing issue is the propagation delay of the cable. This needs to be added to the host-side timing. The SPICE model in figure C.17 shows an unterminated host with very fast rise times driving a cable with worst case loads. Two unterminated devices are assumed with the maximum allowed capacitive loading of 25 pF.

NOTE – 25 pf was specified in ATA-2.

The simulation results are shown in figure C.18. The period of the ringing is four times the propagation delay of the cable. This simulation shows a cable propagation delay of 5.6 ns. This is twice the value obtained by assuming an 18-inch cable with a propagation velocity of 60% c. The additional delay is due to the presence of the capacitive loads on the cable. This result is important to system designers who take into account worst-case cable delay when specifying the bridge chip timing.


T2
Device 0
V1
C2
25 pf
TD = 1.5 ns
ZO = 110
T3
Tr = 0.1 ns
Tf = 0.1 ns
Device 1
Cable
Host
C3
25 pf
TD = 1.5 ns
ZO = 110
Cable

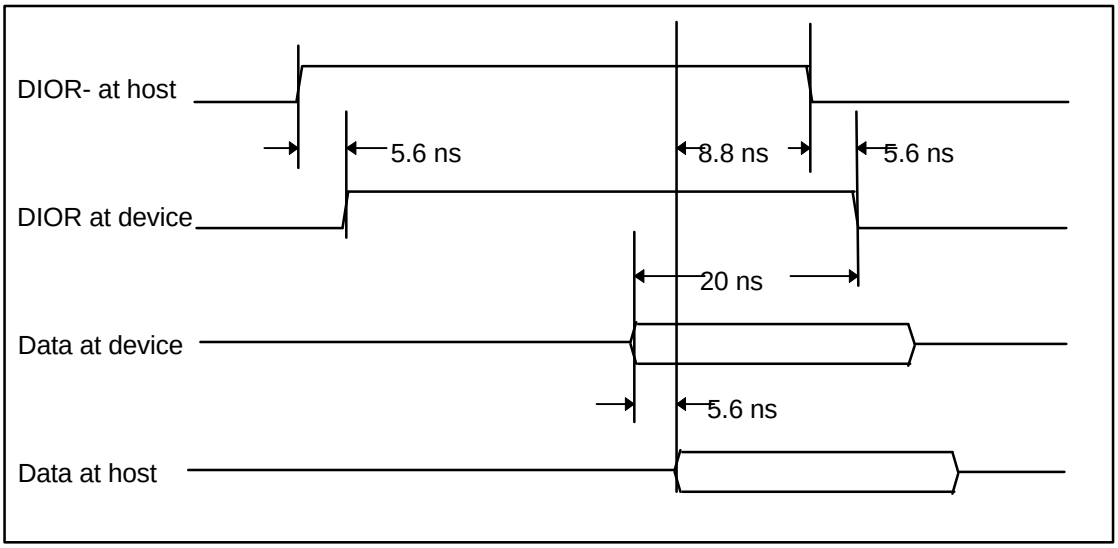


Figure C.19 – Host data setup time during a read cycle

The series resistor at the host is located as close as possible to the ATA connector. To see the importance of this, SPICE simulations are done with the stray capacitance on the driver side of the series resistor and again with the stray capacitance on the cable side. The ringing is reduced when the stray capacitance of the host is on the driver side of the series resistor. A related issue is the distance from the host adapter chip (or chipset) to the ATA connector. Some motherboards have the chip located up to 10 inches away from the connector. This effectively adds another 10 inches to the 18-inch ribbon cable, resulting in an equivalent cable length of 28 inches.

> NOTE – The traces on the circuit board are from 50 to 200 ohm impedance, so the electrical length of the trace cannot simply be added to the 110 ohm ribbon cable. A SPICE simulation can be used to find the actual delay.

This additional length is not necessarily a problem. If the system manufacturer takes the extra trace delay into account in the application of the host adapter chip, and the total capacitance is kept below the ATA host limit of 25 pF, then in theory there is no difference. Real-world experience indicates that this calculation is rarely done. The distance from the chip to the connector is not addressed in the ATA specification. Keeping the connector within 3 inches (by trace length) of the host adapter chip is recommended.

C.4.3 Calculating rise time

Chip designers often use a lumped capacitance model for simulating the delay of the output cell. For the simulations this sometimes consists of adding the maximum capacitance allowed for the host and the devices (3 x 25 pF) to an estimated capacitance value for the cable (25 pF). Simulation is then performed with 100 pF capacitance on the output. This does not give an accurate measurement of the timing. A better approximation is to use an output capacitance for the motherboard, a host end termination resistor, and a transmission line to the devices (see figure C.20).

To illustrate how these models are different, suppose that the propagation delay of the output cell simulation is 2 ns too slow. The chip designer (using a 100 pF model) increases the drive current of the output devices. With enough drive current into a purely capacitive load, the 2 ns is removed, bringing the output cell timing back into spec.

Increasing the drive of the output cell in the transmission line model, the length of the cable is not increased and nor increase the speed of signal propagation in the cable is not increased. The 2 ns required time

reduction is not achieved by increasing the output drive current. Increasing the output drive current only increases the edge speed, making the ringing worse at the device end (some time is gained with the faster edge speed, but not nearly as much as is predicted with a simple capacitive load model). It is not possible to decrease the overhead by increasing the drive current.

Most ASIC designers find that simulations using the recommended model of figure C.20 show their output cells to be faster than in models with a 100 pF load.

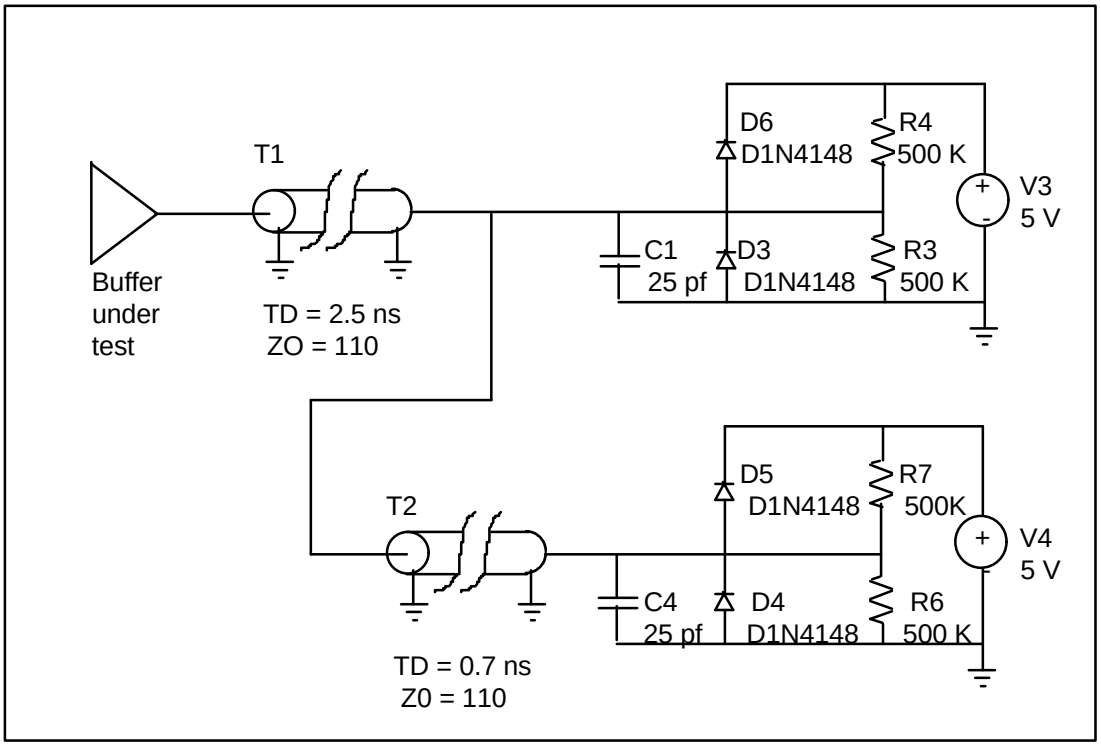


Figure C.20 – Recommended model for I/O cell propagation delay

C.4.4 Measuring propagation delay

Propagation delay times at the host (and at the device) are measured to the ATA standard of 0.8 V for high to low transitions and 2.0 V for low to high transitions. Many IC manufacturers measure propagation delay at the typical switch point for TTL of 1.4 V. This is not appropriate for the ATA interface since virtually every chip manufacturer (both host and device end) has included hysteresis for noise immunity. Since both the hysteresis window and hysteresis offset of a given receiver move with process, voltage, and temperature, the only guaranteed switch points are the TTL high and low values (0.8 V and 2.0 V).

C.5 Summary of guidelines

This summary is a collection of reminders for device, system, and chipset designers. They are separated into three groups by relevancy. The guidelines below are not intended to be a strict mandate, but a tool to help everyone build compatible, reliable, high-performance products.

C.5.1 Guidelines for device designers

- Terminate signals as shown in table C.1. Consider adding capacitors to ground on these lines if the input capacitance is less than 8 pF, or use active clamping circuits. Place these resistors as close to the ATA connector as possible.
- Verify that the termination circuit used on received signals has less than 20 pF of equivalent capacitance.
- Perform a timing analysis to verify that ATA timings are met at the input to the device. Include the time delay due to propagation and cable termination circuits.

C.5.2 Guidelines for system designers

- Do not use any value less than 1 Kohm for pull up resistors on ATA open-collector signals such as IORDY (as per the standard).
- The ATA host adapter chip should be located as close as possible to the ATA connector. Keep the trace length between them less than 3 inches.
- After circuit board fabrication, verify that the total input capacitance at the host is less than 25 pF.
- Terminate signals as shown in figure C.1. Place these resistors as close to the ATA connector as possible.
- Perform a system timing analysis to verify that ATA timings are met at the input to the device.
- For dual port implementations, terminate signals as shown in figure C.15. These resistors should be placed as close to the ATA connector of that port as possible.
- For dual port implementations, the signal lines CS0- and CS1- should be shared.
- For dual port implementations, the signal lines DIOR- and DIOW- should not be shared.
- For dual port implementations, do not share DASP- or PDIAG- signal lines.
- For dual port implementations, perform a system timing analysis to verify that ATA timings are met at the input of the device. In particular watch the assertion widths of DIOR- and DIOW- to insure that they meet the specification.
- Route ATA cable away from chassis, power supplies and high speed circuits.
- Use the shortest cable practical and never greater than 18 in.

C.5.3 Guidelines for chip designers

- Design I/O cells to have rise and fall times of 5 ns or more under both minimum and maximum load conditions.
- Perform timing simulations using a transmission line load model, not a 100 pF capacitor model.
- Take worst-case cable delay into account when designing the ATA interface. Ensure that ATA timing can be met at the device-end of the cable. Provide typical application data with timing for system manufacturers.

Annex D
(informative)
Bibliography

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AT Attachment Interface with Extensions, ANSI X3.279-199x
Suite of 2.5” Form Factor Specifications, SFF-8200, SFF-8201, SFF-8212[1)]
Suite of 3.5” Form Factor Specifications, SFF-8300, SFF-8301, SFF-8302
Information Specification for Phoenix EDD (Enhanced Disk Drive) Specification, SFF-8039
ATA Packet Interface for CD-ROMs, SFF-8020i
PC Card Standard, February 1995, PCMCIA[2)]

1) SFF documents are published by:
SFF
14426 Black Walnut Court, Saratoga, California 95070
FaxAccess: 408 741-1600

2) The PC Card Standard is published by:
Personal Computer Memory Card International Association
2635 North First Street, Suite 209, San Jose, California 95131

Annex E
(informative)
ATA command set summary

The following four tables are provided to facilitate the understanding of the ATA command set. Table E.1 provides information on which command codes are currently defined. Table E.2 provides a list of all of the ATA commands in order of command code. Table E.3 provides a summary of all commands with the protocol, required use, command code and registers used for each. Table E.4 shows the status and error bits used by each command.

Table E.1 – Command matrix

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	C	R	R	R	R	R	R	R	C	R	R	R	R	R	R	R
1x	C	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
2x	C	C	C	C	R	R	R	R	R	R	R	R	R	R	R	R
3x	C	C	C	C	R	R	R	R	R	R	R	R	C	R	R	R
4x	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R
5x	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
6x	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
7x	C	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
8x	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
9x	C	C	C	R	C	C	C	C	C	C	V	R	R	R	R	R
Ax	C	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R
Bx	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Cx	V	V	V	V	C	C	C	R	C	C	C	C	R	R	R	R
Dx	R	R	R	R	R	R	R	R	R	R	R	O	O	O	C	C
Ex	C	C	C	C	C	C	C	R	C	O	R	R	C	C	C	C
Fx	V	C	C	C	C	C	C	V	V	V	V	V	V	V	V	V

Key:
C = a unique command.
R = Reserved, undefined in current specifications.
V = Vender specific commands.
O = Obsolete.

Table E.2 – Commands sorted by command value

Command name	Command code
NOP	00h
ATAPI SOFT RESET	08h
RECALIBRATE	10h
READ SECTOR(S) (w/ retry)	20h
READ SECTOR(S) (w/o retry)	21h
READ LONG (w/ retry)	22h
READ LONG (w/o retry)	23h
WRITE SECTOR(S) (w/ retry)	30h
WRITE SECTOR(S) (w/o retry)	31h
WRITE LONG (w/ retry)	32h
WRITE LONG (w/o retry)	33h
WRITE VERIFY	3Ch
READ VERIFY SECTOR(S) (w/ retry)	40h
READ VERIFY SECTOR(S) (w/o retry)	41h
FORMAT TRACK	50h
SEEK	70h

(continued)

Table E.2 – Commands sorted by command value *(concluded)*

Command name	Command code
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
STANDBY IMMEDIATE (see note)	94h E0h
IDLE IMMEDIATE (see note)	95h E1h
STANDBY (see note)	96h E2h
IDLE (see note)	97h E3h
CHECK POWER MODE (see note)	98h E5h
SLEEP (see note)	99h E6h
ATAPI PACKET	A0h
ATAPI IDENTIFY DEVICE	A1h
ATAPI SERVICE	A2h
SMART	B0h
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
READ DMA (w/ retry)	C8h
READ DMA (w/o retry)	C9h
WRITE DMA (w/ retry)	CAh
WRITE DMA (w/o retry)	CBh
DOOR LOCK	DEh
DOOR UNLOCK	DFh
STANDBY IMMEDIATE (see note)	E0h 94h
IDLE IMMEDIATE (see note)	E1h 95h
STANDBY (see note)	E2h 96h
IDLE (see note)	E3h 97h
READ BUFFER	E4h
CHECK POWER MODE (see note)	E5h 98h
SLEEP (see note)	E6h 99h
WRITE BUFFER	E8h
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
IDENTIFY DEVICE DMA	EEh
SET FEATURES	EFh
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h
SECURITY FREEZE	F5h
SECURITY DISABLE PASSWORD	F6h

NOTE – These commands have two command codes and appear in this table twice, once for each command code.

Table E.3 – Command codes and parameters

proto	Command	typ	Command code	Parameters used				
				FR	SC	SN	CY	DH
ND	CHECK POWER MODE	O	98h E5h		y			D
ND	DOOR LOCK	O	DEh					D
ND	DOOR UNLOCK	O	DFh					D
PO	DOWNLOAD MICROCODE	O	92h	y	y	y	y	D
ND	EXECUTE DEVICE DIAGNOSTIC	M	90h					D*
VS	FORMAT TRACK	V	50h					d
PI	IDENTIFY DEVICE	M	ECh					D
DM	IDENTIFY DEVICE DMA	O	EEh					D
ND	IDLE	O	97h E3h		y			D
ND	IDLE IMMEDIATE	O	95h E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	91h		y			y
ND	MEDIA EJECT	O	EDh					D
ND	NOP	O	00h					D
PI	READ BUFFER	O	E4h					D
DM	READ DMA (w/ retry)	M	C8h		y	y	y	y
DM	READ DMA (w/o retry)	M	C9h		y	y	y	y
PI	READ LONG (w/ retry)	O	22h		y	y	y	y
PI	READ LONG (w/o retry)	O	23h		y	y	y	y
PI	READ MULTIPLE	M	C4h		y	y	y	y
PI	READ SECTOR(S) (w/ retry)	M	20h		y	y	y	y
PI	READ SECTOR(S) (w/o retry)	M	21h		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/ retry)	M	40h		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/o retry)	M	41h		y	y	y	y
ND	RECALIBRATE	O	10h					D
PO	SECURITY DISABLE PASSWORD	O	F6h					D
ND	SECURITY ERASE PREPARE	O	F3h					D
PO	SECURITY ERASE UNIT	O	F4h					D
ND	SECURITY FREEZE	O	F5					D
PO	SECURITY SET PASSWORD	O	F1H					D
PO	SECURITY UNLOCK	O	F2h					D
ND	SEEK	M	70h			y	y	y
ND	SET FEATURES	M	EFh	y				D
ND	SET MULTIPLE MODE	M	C6h		y			D
ND	SLEEP	O	99h E6h					D
ND	SMART DISABLE OPERATIONS	O	0B0h	y			y	D
ND	SMART ENABLE/DISABLE AUTOSAV	O	0B0h	y	y		y	D
ND	SMART ENABLE OPERATIONS	O	0B0h	y			y	D
PI	SMART READ THRESHOLDS	O	0B0h	y			y	D
PI	SMART READ VALUES	O	0B0h	y			y	D
ND	SMART RETURN STATUS	O	0B0h	y			y	D
ND	SMART SAVE VALUES	O	0B0h	y			y	D
ND	STANDBY	O	96h E2h		y			D
ND	STANDBY IMMEDIATE	O	94h E0h					D
PO	WRITE BUFFER	O	E8h					D
DM	WRITE DMA (w/ retry)	M	CAh		y	y	y	y
DM	WRITE DMA (w/o retry)	M	CBh		y	y	y	y
PO	WRITE LONG (w/ retry)	O	32h	*	y	y	y	y
PO	WRITE LONG (w/o retry)	O	33h	*	y	y	y	y

(continued)

Table E.3 – Command codes and parameters *(concluded)*

proto	Command	typ	Command code	Parameters used				
				FR	SC	SN	CY	DH
PO	WRITE MULTIPLE	M	C5h	*	y	y	y	y
PO	WRITE SECTOR(S) (w/ retry)	M	30h	*	y	y	y	y
PO	WRITE SECTOR(S) (w/o retry)	M	31h	*	y	y	y	y
PO	WRITE VERIFY	O	3Ch	*	y	y	y	y
VS	Vendor specific	V	9Ah,C0h-C3h,8xh, F0h-FFh					
-	Reserved: all remaining codes	R						

Key:
DM = DMA command ND = Non-data command PI = PIO data in command
PO = PIO data out command VS = Vendor specific command O = Optional
M = Mandatory R = Reserved V = Vendor specific implementation
CY = Cylinder registers SC = Sector Count register DH = Device/Head register
SN = Sector Number register FR = Features register (see command descriptions for use)
y = the register contains a valid parameter for this command. For the Device/Head register, y means both the device and head parameters are used.
D = only the device parameter is valid and not the head parameter.
d = the device parameter is valid, the usage of the head parameter vendor specific.
D* = Addressed to device 0 but both devices execute it.
* = Maintained for compatibility (see 5.2.10)

Table E.4 – Status and error usage

	Status register				Error register				
	DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
ACKNOWLEDGE MEDIA CHANGE	V	V		V			V		
BOOT - POST-BOOT	V	V		V			V		
BOOT - PRE-BOOT	V	V		V			V		
CHECK POWER MODE	V	V		V			V		
DOOR LOCK	V	V		V			V		
DOOR UNLOCK	V	V		V			V		
DOWNLOAD MICROCODE	V	V		V			V		
EXECUTE DEVICE DIAGNOSTIC	V	V		V	(see 7.5)				
FORMAT TRACK	V	V		V	V	V	V	V	V
IDENTIFY DEVICE	V								
IDENTIFY DEVICE DMA	V								
IDLE	V	V		V			V		
IDLE IMMEDIATE	V	V		V			V		
INITIALIZE DEVICE PARAMETERS	V	V							
MEDIA EJECT	V	V		V			V		
NOP	V	V		V			V		
READ BUFFER	V	V		V			V		
READ DMA (w/ retry)	V	V	V	V	V	V	V		V
READ DMA (w/o retry)	V	V	V	V	V	V	V		V
READ LONG (w/ retry)	V	V		V		V	V		V
READ LONG (w/o retry)	V	V		V		V	V		V
READ MULTIPLE	V	V	V	V	V	V	V		V
READ SECTOR(S) (w/ retry)	V	V	V	V	V	V	V		V
READ SECTOR(S) (w/o retry)	V	V	V	V	V	V	V		V

(continued)

Table E.4 – Status and error usage *(concluded)*

	Status register				Error register				
	DRDY	DF	CORR	ERR	UNC	IDNF	ABRT	TK0NF	AMNF
READ VERIFY SECTOR(S) (w/ retry)	V	V	V	V	V	V	V		V
READ VERIFY SECTOR(S) (w/o retry)	V	V	V	V	V	V	V		V
RECALIBRATE	V	V		V			V	V	
SECURITY DIS PASSWORD	V	V		V			V		
SECURITY ERASE PREP	V	V		V			V		
SECURITY ERASE UNIT	V	V		V			V		
SECURITY FREEZE	V	V		V			V		
SECURITY SET PASSWRD	V	V		V			V		
SECURITY UNLOCK	V	V		V			V		
SEEK	V	V		V		V	V		
SET FEATURES	V	V		V			V		
SET MULTIPLE MODE	V	V		V			V		
SLEEP	V	V		V			V		
SMART DISABLE OPS	V			V			V		
SMART EN/DIS AUTOSAVE	V			V			V		
SMART ENABLE OPS	V			V			V		
SMART READ THRSHOLDS	V			V		V	V		
SMART READ VALUES	V			V		V	V		
SMART RETURN STATUS	V			V			V		
SMART SAVE VALUES	V	V		V		V	V		V
STANDBY	V	V		V			V		
STANDBY IMMEDIATE	V	V		V			V		
WRITE BUFFER	V	V		V			V		
WRITE DMA (w/ retry)	V	V		V		V	V		
WRITE DMA (w/o retry)	V	V		V		V	V		
WRITE LONG (w/ retry)	V	V		V		V	V		
WRITE LONG (w/o retry)	V	V		V		V	V		
WRITE MULTIPLE	V	V		V		V	V		
WRITE SECTOR(S) (w/ retry)	V	V		V		V	V		
WRITE SECTOR(S) (w/o retry)	V	V		V		V	V		
WRITE VERIFY	V	V	V	V	V	V	V		V
Invalid command code	V	V		V			V		
Key: V = valid on this command									