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- MODULE SimpleStore_Regular
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The model represents the model of a simple storage system that provides \*regular\* register semantics. It works as follows: - It has a queue of incoming  $pending\_rd$  and a queue of incoming  $pending\_wr$  ( $pending\_rd$ , resp  $pending\_wr$ ). These queues are very flacky meaning that they may drop requests when they like. - It has a reliable store (oviously single-copy), which takes out  $pending\_rd$  and  $pending\_wr$  from the queues one at a time and executes them. Once a write is executed by the store, there's no turning back. The write cannot be dropped anymore. - Writes: are appended to the  $pending\_wr$  and are later dropped or executed by the store. - Reads: are appended to the  $pending\_rd$  and are later dropped or executed by the store in the following way. A read can return EITHER the content of the store (so the last committed value) OR the value of one of the  $pending\_wr$  that are still pending in  $pending\_wr$  (so value of some overlapping write).

Thus, the model corresponds to "regular registers" in Lamport terms [On Inter-Process Communication]. Reads that don't overlap any write return the last committed value and  $pending\_rd$  that overlap some  $pending\_wr$  return either the alst committed value or the value of any overlapping write.

EXTENDS  $simplestore\_quickrd$  extends the linearizable simple store

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SSR\_TypeInvariant \triangleq SS1\_TypeInvariant
SSR\_Init \triangleq SS1\_Init
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## STORE operations:

Reads: not serialized w/  $pending_wr$ . A read can return either the value of the last committed wr, or the value of one of the pending (overlapping)  $pending_wr$ .

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one of the pending (overlapping) pending_wr.
SSR\_HdlRead \triangleq handle one read requests
        EITHER get the store value (value of last committed write),
   \land \lor last\_read\_val' = store
        OR the value of one of the overlapping pending write requests
       \vee \exists idx \in 1 .. Len(pending\_wrreq) :
           \wedge last\_read\_val' = pending\_wrreq[idx]
       \vee \exists v \in Val:
           \land pending\_wrresp[v] > 0
                                           there is a write pending for this value
           \land last\_read\_val' = v
                                           read this value
       \vee \exists v \in Val:
          \wedge failed_wr[v] > 0 there's a failed write for this valve
          \wedge last\_read\_val' = v read this value
   ∧ UNCHANGED ⟨pending_rd⟩
SSR\_RunStore \triangleq
    \lor \land SSR\_HdlRead
       \land UNCHANGED \langle pending\_wrresp, pending\_wrreq, failed\_wr, store <math>\rangle
       \land SS_CommitWrite
       ∧ UNCHANGED ⟨pending_rd, last_read_val⟩
```

Full specification.

 $SSR\_Next \stackrel{\triangle}{=}$ 

 $\vee \, SS1\_Client$ a client submits a request (query or update)

 $\lor \mathit{SSR\_RunStore}$ the store deals w/ the updates

 $\lor \mathit{SS\_ChannelActions}$ the incoming channel for the store drops some requests

 $\begin{array}{ll} ssrvars & \triangleq ss1vars \\ SSR\_Spec & \triangleq SSR\_Init \land \Box [SSR\_Next]_{ssrvars} \end{array}$ 

Invariants

 $SSR\_AllInvariants \; \stackrel{\triangle}{=} \;$  $\land \mathit{SSR\_TypeInvariant}$ 

Theorem

THEOREM  $SSR\_Spec \Rightarrow \Box SSR\_AllInvariants$