Power Electronic Converter for Characterization of Hall-effect Current Sensors

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***Abstract*—Hall-effect current sensors are widely used in industrial applications. Characterization of their steady state, dynamic capabilities and thermal endurance verification is important to ensure the sensor performance. It is shown that an H-bridge inverter topology with an RCD snubber, packaged as proposed, can be used for large signal sinusoidal current characterization and step current characterization of the current sensor. Analytical expression of step current is derived and used to produce rising and falling step excitation with controlled peak value and transition time. A hybrid PWM technique with a frequency adaptive proportional-resonant current controller is used to produce large magnitude sinusoidal current with controlled frequency and magnitude. Using IGBT and MOSFET legs in the H-bridge reduces overall power consumption of the current source during sinusoidal current generation. The hardware is fabricated in the laboratory, and its performance is validated using high bandwidth current probe.**

***Index Terms*—Current sensor characterization, current source, step current, Hall-effect current sensor, frequency adaptive PR current controller, power converter**

I. Introduction

Hall-effect current sensors, used in power electronic applications, are typically specified in terms of rated current, rise time, settling time, reaction time, $\frac{\mathrm{d}i}{\mathrm{d}t}$ limitation and bandwidth [1]. A step current waveform contains more frequency components, and can be used to validate dynamic performance of a current sensor [2]. The steady state performance can be validated using dc and sinusoidal current excitation. Small signal bandwidth of these sensors can be measured using commercial frequency response analyzer, but excitation current of the order of 100mA can only be obtained, while the nominal current rating of Hall-effect sensors can be of the order of 100A.

Successful attempt was made in [3] to produce stable and accurate 100A dc current source in the frequency range from 0.1Hz to 1kHz using computer controlled commercial equipment in conjunction with software-controlled digitizing voltmeter. It was further used in [4] to validate the performance of the set-up developed in the laboratory. In [5] a test set-up was fabricated in laboratory, generating step current of 40ns rise time with 540A peak current to validate transient performance of Rogowski current transducer. Experimental results for characterization of current transformers and Hall-effect current transducers in presence of harmonic distortions are reported in [6], [8], [9] in the frequency range from 30Hz to 800Hz and 15A peak current. But, little is reported to date on the hardware configuration, which can be used to validate both transient as well as steady state performance of Hall-effect current sensors without significant modification.

This paper proposes the design of a current source capable of producing step current with controlled peak value and transition time, as well as sinusoidal current of adjustable magnitude and frequency. It is designed to produce step rise and step fall current of 100A peak having rise/fall time less than 200ns. In addition to step current the current source also produces sinusoidal current of magnitude 50A rms, and frequency in the range 1Hz - 1000Hz. This current source can be used to characterize step response, $\frac{\mathrm{d}i}{\mathrm{d}t}$ tracking limit and long term thermal endurance test of the current sensor at its rated current. The ability to characterize the sensor with rated current at harmonic frequencies facilitates the thermal endurance test of the sensor in an industrial environment. To minimize the effect of positional error these current sensors are manufactured with an aperture having through-hole area almost equal to the cross-sectional area of typical wire capable of carrying the rated current of the sensor. To test the thermal endurance the excitation sinusoidal signal should be the rated current of the sensor with single primary turn. This is because the use of multiple primary turns alters the sensor thermal envelope at rated condition required for the endurance tests. It is shown that such long term tests can be conducted with minimal power loading using the proposed test set-up.

II. Power Circuit Topology

The circuit, shown in Fig. 1(a), is used for step and sinusoidal current generation in two different branches P_1-P_2 and P_3-P_4 respectively. It resembles an H-bridge voltage source inverter with pure inductive load, consisting of a MOSFET leg and an IGBT leg. An RCD over-voltage snubber is connected across the IGBT leg, which is used to observe step current $i_{Ls}(t)$ in the branch $P_1 - P_2$. The MOSFET leg is protected with a de-coupling capacitive snubber C_s. Here, L_s represents total stray inductance as seen by the IGBT module. It includes the insertion inductance offered by the current sensor.

The positive dc bus plate is modified to accommodate the current sensor in the branch $P_1 - P_2$, as shown in Fig. 1(b). Insertion inductance of the current sensor becomes significant,

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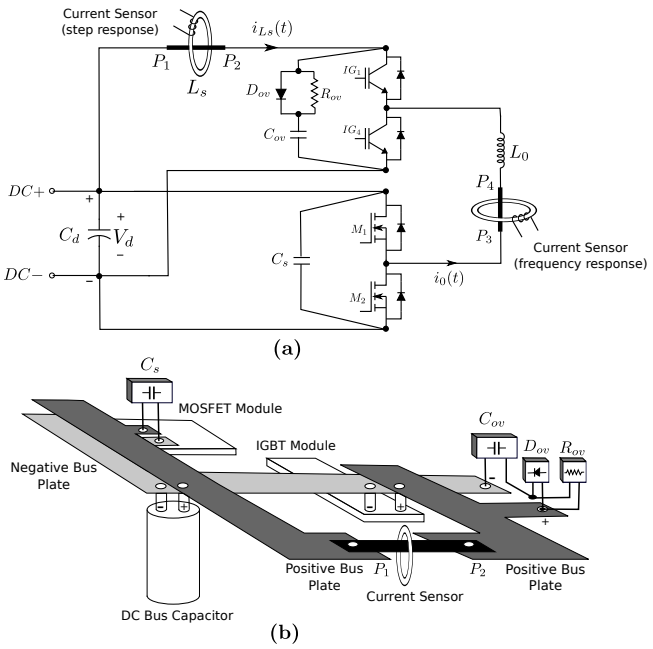

Fig. 1: Current sensor characterization set-up: (a) power circuit of the hardware set-up to produce reference step current $i_{Ls}(t)$ and sinusoidal current $i_0(t)$ in the branch P_1-P_2 and P_3-P_4 respectively, (b) modification in the positive dc bus plate to accommodate the current sensor under test to check step response.

when the sensor is inserted, and has direct impact on the total loop stray inductance of the dc bus. This causes voltage overshoot across the semiconductor devices during turn-off. The snubber elements are chosen to minimize the voltage overshoot across the devices. Moreover, the positive and the negative dc bus plates cannot be placed lateral to each other. An approach, as shown in Fig. 1(b), is required to design the layout of dc bus plates and placement of semiconductor devices. The layout of devices ensures that the additional stray inductance due to the branch $P_1 - P_2$ appears only across the IGBT leg, and not across the MOSFET leg.

III. Step Current Generation

Step electric current may be produced as either rising or falling current. To produce perfect step change in electric current is impossible due to inherent stray inductance associated with current carrying elements in the circuit. But, the duration of change can be kept minimal to emulate a step current, though it results in very high $\frac{\mathrm{d}i}{\mathrm{d}t}$ producing large voltage drop over the inductive path, which can damage the circuit elements. Use of multiple turns in the branch P_1-P_2 to increase the effective magnitude of the step current is not recommended, as the insertion induction increases rapidly with number of turns, causing large voltage overshoot.

In this section a non-destructive method is proposed to generate both rising and falling step current with rise/fall time less than 200ns, and adjustable step current value. Its transition time can be varied by selecting suitable RCD snubber capacitor C_{ov}.

The semiconductor switches are switched in a particular sequence to generate either falling or rising step current, as explained below.

A. Falling step current

A falling step current is produced in the branch P_1-P_2 using the over-voltage RCD snubber. The circuit operates in four modes, as shown in Fig. 2.

Mode-I: All the four switches are initially OFF, as shown in Fig. 2(a). The capacitor C_{ov} gets charged to dc bus voltage V_d.

Mode-II: The top IGBT IG_1 and the bottom MOSFET M_2 are switched ON, as shown in Fig. 2(b). The load inductor L_0 starts getting charged, and the current $i_0(t)$ increases linearly as expressed in (1).

$$I_{Ls0} = \frac{V_d}{L_0} T_{on}, \tag{1}$$

where T_{on} is the ON period of IG_1.

Mode-III: The load current $i_0(t)$ is sensed using a current sensor. When $i_0(t)$ attains a specified value I_{Ls0}, the IGBT IG_1 is turned OFF, as shown in Fig. 2(c). As soon as the voltage across IG_1 rises to dc bus voltage V_d, the diode D_4 starts free-wheeling the inductor current i_0, and the IGBT current i_{c1} starts falling. Owing to very small turn-off time of the IGBT used in the hardware, the dc bus current i_{Ls} can be assumed to stay constant at I_{Ls0} till i_{c1} falls to zero.

When IG_1 starts turning off, the snubber diode D_{ov} turns ON, and C_{ov} gets charged from its initial pre-charged voltage V_d till i_{Ls} comes down to zero. The voltage v_{ce1} across IG_1 is equal to the capacitor voltage v_{Cov} as long as D_{ov} is conducting. The free-wheeling diode D_4 along with L_0 appears as short circuit after IG_1 turns off.

Mode-IV: In this mode, shown in Fig. 2(d), the snubber diode D_{ov} stops conducting, and the capacitor C_{ov} starts getting discharged through the resistor R_{ov} till its voltage comes down to the dc bus voltage V_d. Due to ON-state voltage drop across M_2 and D_4, the free-wheeling current $i_0(t)$ also comes down to zero in a while.

The above four modes complete the sequence to generate the falling step current. It is a single pulse operation, and the modes are not repeated. The falling step current is observed in the Mode-III, and the response may be captured in a high bandwidth oscilloscope in single sequence capture mode. The components selected have pulse ratings compatible with that required during the transient excitation.

The factors governing the characteristics of the falling step current in the Mode-III are analyzed below. The equivalent circuit during the decay of $i_{Ls}(t)$ in this mode consists of a single loop containing series connection of V_d, L_s and C_{ov}. At the start of this mode the current $i_{Ls}(t)$ is I_{Ls0}, and IG_1 is turned off. The diode D_{ov} starts conducting, till $i_{Ls}(t)$ comes down to zero. The fall time of i_{c1} is neglected to simplify the analysis.

The switching transients of diodes and IGBTs are ignored during the analysis. Assuming that $i_{Ls}(t)$ starts falling at $t =$

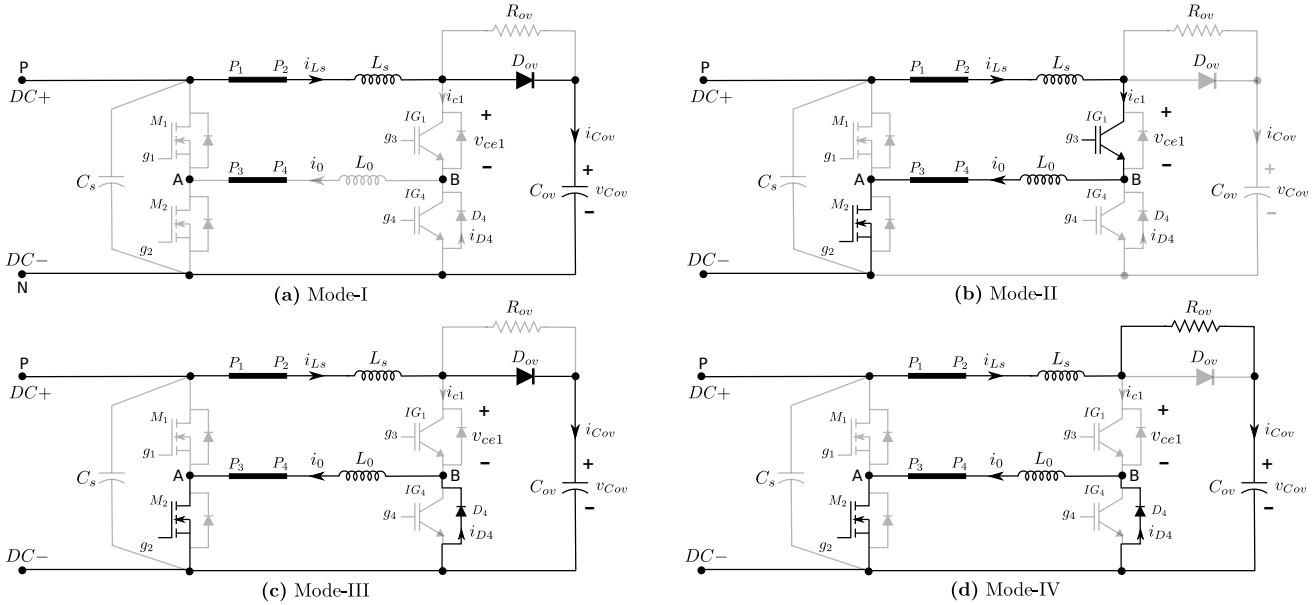

Fig. 2: Four modes of operation of the falling step current generation circuit. The step current $i_{Ls}(t)$ is observed in the Mode-III.

0, the equivalent circuit in Fig. 2(c) can be used to derive the expression of $i_{Ls}(t)$ and $v_{Cov}(t)$, valid for the conduction interval of D_{ov}.

At the start of Mode-III the capacitor C_{ov} is charged to V_d, and the initial value of $i_{Ls}(t)$ is I_{Ls0}. The expression of $i_{Ls}(t)$ and $v_{Cov}(t)$ are derived to be:

$$i_{Ls}(t) = I_{Ls0} \cos \omega_r t, \tag{2}$$

$$v_{Cov}(t) = V_d + \frac{I_{Ls0}}{\omega_r C_{ov}} \sin \omega_r t, \tag{3}$$

where

$$\omega_r = \frac{1}{\sqrt{L_s C_{ov}}}, . \tag{4}$$

The fall time t_f is calculated, when $i_{Ls}(t)$ comes down to zero from I_{Ls0}, and D_{ov} stops conducting.

$$t_f = \frac{\pi}{2\omega_r} = \frac{\pi}{2}\sqrt{L_s C_{ov}}, \tag{5}$$

This makes t_f independent of I_{Ls0}.

The gate pulses g_1-g_4 along with $i_{c1}(t)$, $i_{Ls}(t)$, $v_{ce1}(t)$ and $v_{Cov}(t)$ are shown in Fig. 3 during the four modes. The fall time t_f is exaggerated, though it is negligible compared to T_{on} in practice.

With proper choice of C_{ov} and using (1), (5) the current $i_{Ls}(t)$ flowing in the branch P_1-P_2 can be made fall to zero in a fixed duration t_f from a peak value I_{Ls0}.

The voltage $v_{ce1}(t)$ across the IGBT IG_1 attains maximum value at $t = t_f$, given by

$$V_{OV1} = V_d + \left(\frac{\pi L_s}{2}\right) \frac{I_{Ls0}}{t_f} \tag{6}$$

In practical implementation, the dc bus voltage V_d is fixed. The stray inductance L_s depends on the layout arrangement of the devices, the bus plates and sensor insertion inductance. The

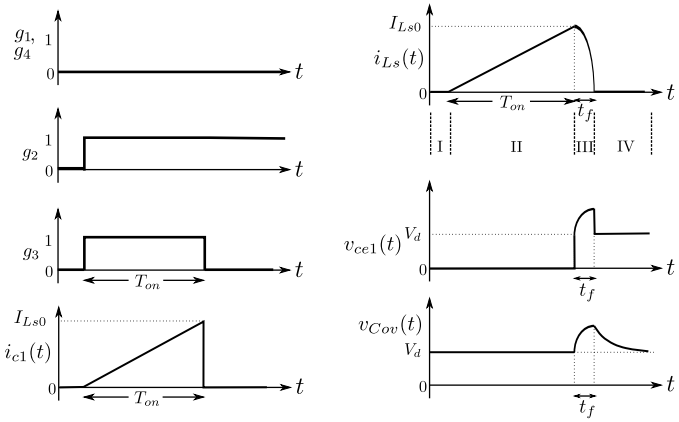

Fig. 3: Waveforms of the gate pulses g_1-g_4 along with $i_{c1}(t)$, $i_{Ls}(t)$, $v_{ce1}(t)$ and $v_{Cov}(t)$ during the four modes in generation of falling step current.

peak current I_{Ls0} is determined by the step current required to characterize the current sensor, and must be below the rated current of the IGBT. As shown in (5) C_{ov} remains to be decided to generate a current of peak I_{Ls0} with fall time t_f. Eq. (5) suggests that t_f can be reduced by using low capacitance C_{ov}, but reduction in t_f raises the peak voltage V_{OV1} across the IGBT as shown in (6). A proper value of C_{ov} must be chosen to keep V_{OV1} below the voltage rating of the IGBT. Fig. 4 shows the typical variation in V_{OV1} with t_f for different I_{Ls0} and a fixed V_d. The designer may, first, decide minimum feasible t_f corresponding to the permissible V_{OV1} with curve of the required I_{Ls0}. The snubber capacitor C_{ov} can be selected using (5) for a t_f greater than this minimum value.

The resistor R_{ov} of the RCD snubber comes into picture in the Mode-IV, when C_{ov} starts getting discharged. The RCD

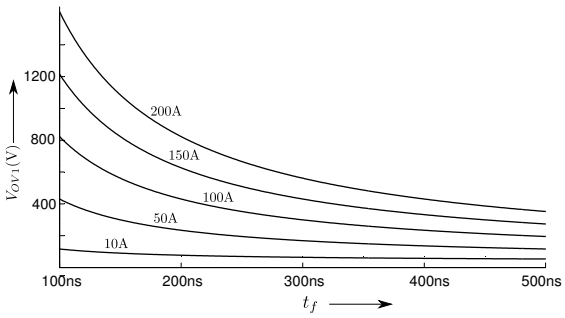

Fig. 4: Plot of the voltage overshoot across IG_1 during the turn-off vs. the fall time t_f of $i_{Ls}(t)$ for different values of peak current I_{Ls0}. The stray inductance L_s is 500nH, and V_d is fixed at 15V.

snubber is used in generation of reference sinusoidal current also. R_{ov} must be chosen sufficiently small to ensure that C_{ov} is fully discharged before next turn-off. At the same time the discharge transient should be overdamped to prevent undesired switch voltage oscillations, imposing a minimum value of R_{ov} [10].

B. Rising step current

The power circuit, shown in Fig. 1(a), is also used to generate rising step current in the branch P_1-P_2. The switches, in the Mode-II and the Mode-III, are modulated in a sequence by gating the MOSFET M_1 and the IGBT IG_4 in the Mode-II. The behaviour during these modes occurs in a similar manner. Similar to the falling step current generation, the peak value I_{Ls0} and the rise time t_r of this rising step current can be controlled independently.

IV. Sinusoidal Current Generation

The circuit shown in Fig. 1(a) is used to generate reference sinusoidal current $i_0(t)$ in the branch P_3-P_4. The power MOSFETs M_1 and M_2 along with IGBTs IG_1 and IG_4 constitute a hybrid structure to reduce overall switching loss in the devices based on a hybrid PWM strategy for full bridge inverter proposed in [11]. The hybrid PWM principle and its frequency spectrum are described in [11], and the spectrum is shown to be similar to unipolar PWM method with triangular carrier. The use of MOSFET and IGBT legs in the H-bridge configuration reduces the overall switching loss in the converter when switches are modulated with the hybrid PWM strategy. It can be illustrated with a theoretical calculation of total switching losses in the inverter operated at the experimental condition.

The switching loss of the H-bridge inverter, calculated for three cases are tabulated in Table I using the datasheets of the MOSFET [15] and the IGBT [16] used in the hardware set-up. It can be seen that total converter switching loss is the lowest, when the MOSFET is switched at 20kHz and the IGBT at 100Hz to produce 50A rms, 100Hz output current. Total conduction loss in the switches is 4.2W in all the three cases.

As the objective is to produce a current for measurement purpose only, an air core inductor [18] is chosen as the load

TABLE I: CALCULATED SWITCHING LOSS DISTRIBUTION IN THE CONVERTER AT 40V DC BUS AND 100Hz SINUSOIDAL OUTPUT CURRENT GENERATION WITH 50A RMS.

PWM	f_{sw} MOSFET	f_{sw} IGBT	P_{sw} per MOEFET	P_{sw} per IGBT	P_{sw} converter
Unipolar	10kHz	10kHz	2.05W	3.4W	10.9W
Hybrid	100Hz	20kHz	∼0W	6.8W	13.6W
Hybrid	20kHz	100Hz	4.1W	∼0W	8.2W

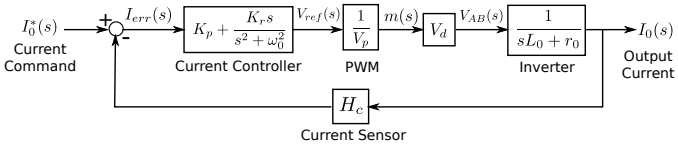

Fig. 5: Block diagram of closed loop PR current controlled inverter.

to avoid any active power consumption by load. In this way, the mains needs to supply active power required for losses in semiconductor devices and other parasitic losses. The reactive power required by the inductor gets delivered by the dc bus electrolytic capacitor bank.

A. System Modeling and Current Controller Design

Average model of the inverter modulated with the hybrid PWM method is similar to sine-triangle unipolar PWM method. The average output voltage, $v_{AB}(t)$ can be expressed in terms of modulation index $m(t)$ and dc bus voltage V_d as [11]:

$$v_{AB}(t) = m(t)V_d \tag{7}$$

The output current $i_0(t)$ is sensed and compared with the reference current command generated in a microprocessor. A proportional-resonant current controller, proposed in [12] is used in the closed loop structure, as shown in Fig. 5. K_p and K_r are gains of the current controller; H_c is gain of the current sensor in the feedback path; V_p is the peak of the triangular carrier; r_0 is the winding resistance of the load inductor L_0. The controlled output current $i_0(t)$ with fundamental frequency ω_0 (rad/s) matches the characteristics of the current sensor in the feedback path.

The semiconductor devices have a upper limit on switching frequency to avoid thermal failure. This, in turn, puts upper limit on the fundamental frequency of the closed loop controlled current. In the higher frequency range the controller gains, shown in Fig. 5, are selected to avoid instability due to low switching-to-fundamental frequency ratio. The design procedure, suggested in [13], is used to obtain optimal controller gains in this condition.

B. Scheme for Online Change in Frequency and Magnitude

The sinusoidal current command $i_0^*(t) = I_m^* \sin \omega_0 t$ is generated using a look-up table of sine-cosine function stored in an FPGA. Its operating frequency needs to be swept in the frequency range of interest. Varying the frequency ω_0 and the magnitude I_m^* online, preferably by changing a knob setting, will be convenient for the user to record the magnitude and

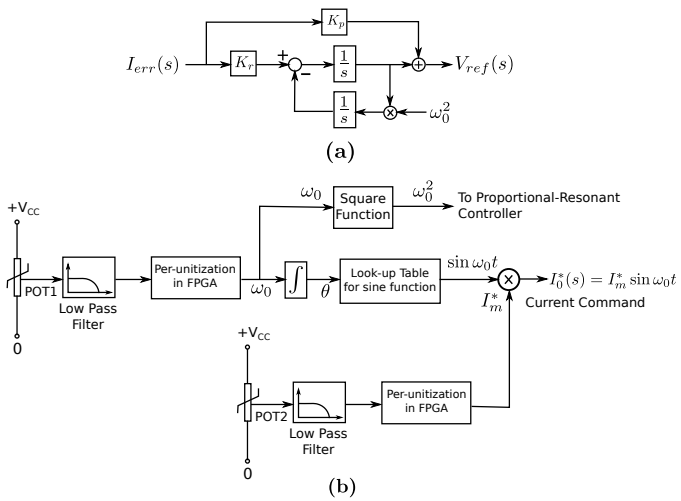

Fig. 6: Adaptive scheme for online change in frequency and magnitude of the output current (a) block diagram of frequency adaptive proportional-resonant controller based on two integrators in continuous time domain [14], (b) online change in frequency ω_0 and magnitude I_m^* of the current command generated in FPGA using external potentiometers POT1 and POT2.

phase shift with respect to the reference current at a particular frequency to get the current sensor frequency response.

A frequency adaptive continuous time structure of proportional-resonant controller is proposed in [14] to mitigate the sensitiveness to frequency variations of the signals to be controlled. It does not require the online computation of explicit cosine functions. The structure is shown in Fig. 6(a), and is used in implementing digital PR controller to track harmonics currents for an active power filter [14].

The above structure is included in a scheme proposed in this section, and shown in Fig. 6(b) to generate the sinusoidal current command of frequency ω_0. The output of the potentiometer POT1, filtered by a low pass filter, is per-unitized and integrated to produce $\theta = \omega_0 t$, which is fed as the memory address to the look-up table of sine function stored in the FPGA. The unit reference sinusoid $\sin\omega_0 t$ is further multiplied by the desired magnitude I_m^* to generate the current command $I_m^* \sin\omega_0 t$. Here, the current magnitude I_m^* is generated using another external potentiometer POT2. Square of the frequency of the current command, ω_o^2 is fed to the frequency adaptive PR controller block shown in Fig. 6(a). In this way, the resonance frequency of the PR current controller is equal to the frequency of the current command. It ensures that the output current $i_0(t)$ tracks the current command $i_0^*(t)$ while varying its frequency ω_0 online by changing the variable terminal of the external potentiometer.

V. Experimental results

The dc bus voltage V_d is fixed at 40V in sinusoidal current generation to reduce the overall losses in the converter. During step current generation V_d is fixed at 15V to lower the voltage overshoot across the IGBT during the turn-OFF in Mode-III. The control scheme is implemented on ALTERA cyclone FPGA platform.

TABLE II: SPECIFICATIONS OF THE COMPONENTS USED IN THE HARDWARE SET-UP.

Components	Specifications	Technology
C_d	33000μF, 100V	Electrolytic
C_s	2.2μF, 1000V	Snubber
IG_1, IG_4	100A, 600V	Field-stop Trench-gate [16]
MS_1, MS_4	80A, 100V	Trench-gate [15]
R_{ov}	50Ω, 10W	Metal Film
C_{ov}	1200V, 15nF	Metallized Film Polypropylene
D_{ov}	1200V, 20A	SiC Schottky Barrier Diode [17]
L_0	72μH, 70Arms	Air-core Toroidal-cage [18]

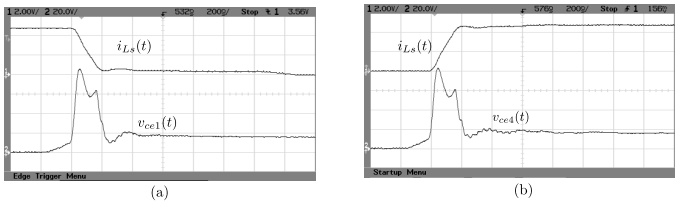

Fig. 7: Experimental waveforms of step current $i_{Ls}(t)$ produced in the branch P_1-P_2 and IGBT voltage overshoot for 15nF C_{ov}. The peak value I_{Ls0} is fixed at 48A for both falling and rising step current generation.
(a) $i_{Ls}(t)$ and corresponding IG_1 voltage $v_{ce1}(t)$, (b) rising step current $i_{Ls}(t)$ and corresponding IG_4 voltage $v_{ce4}(t)$.
$i_{Ls}(t)$: 20A/div, $v_{ce1}(t)$: 20V/div, $v_{ce4}(t)$: 20V/div, time: 200ns/div.

Components used in the hardware set-up are shown in Table II. A SiC Schottky barrier diode [17] is selected as D_{ov} to take advantage of its zero reverse recovery feature, when $i_{Ls}(t)$ crosses zero in step current generation. L_0 is an air-core toroidal cage inductor designed in laboratory using the guidelines in [18].

A. Measured Step Current Characteristics

Experimental waveforms of the falling and the rising step current $i_{Ls}(t)$, produced in the branch P_1-P_2 along with voltage drop across the corresponding switching IGBT, are depicted in Fig. 7. The peak current is fixed at 48A, as the measuring current probe [19] rating is limited to 50A. Estimated value of L_s is 500nH. Due to reverse recovery effect of D_{ov} the step current $i_{Ls}(t)$ can go below zero level and above I_{Ls0} level in falling and rising step current respectively. A SiC Schottky Barrier Diode having zero reverse recovery feature is used as D_{ov} to get smooth transition to the final level. The first peak in IGBT voltage waveforms, shown in Fig. 7, is due to forward recovery effect of D_{ov}.

B. Sinusoidal Current

A closed loop Hall-effect current sensor [1] is used as the sensor in the feedback path, shown in Fig. 5. Using the scheme described in the section IV-B, a sinusoidal reference current $i_0^*(t)$ of 50A rms and frequency f_0 from 1Hz to 1000Hz is

TABLE III: SYSTEM AND CONTROLLER PARAMETERS SHOWN IN FIG. 5.

V_d	L_0	r_0	V_p	H_c	I^*_{0rms}	K_p	K_r
40V	72μH	35mΩ	5V	0.11V/A	50A	0.6	$2240s^{-1}$

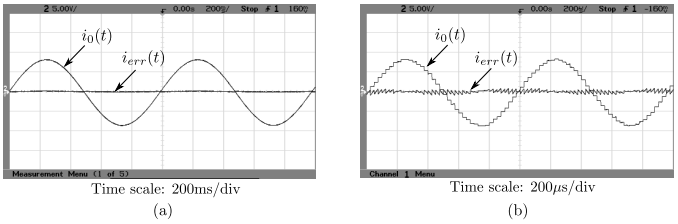

Fig. 8: Experimental waveforms of the controlled 50A rms output current $i_0(t)$ and the error $i_{err}(t)$ at fundamental frequency of (a) 1Hz and (b) 1000Hz. $i_0(t)$, $i_{err}(t)$ scale: 45A/div. The output current $i_0(t)$ contains 20kHz switching components.

generated in FPGA. Switching frequency f_{sw} of the MOSFET leg is fixed at 20kHz, while the IGBT leg is switched at the frequency f_0 of the reference current $i^*_0(t)$. The system and controller parameters of Fig. 5, used in the experimental set-up are given in Table III.

The experimental waveforms of 50A rms output current $i_0(t)$ along with the error $i_{err}(t)$ is shown in Fig.8 at fundamental frequency of 1Hz and 1000Hz. There is very little error at the fundamental frequency. The error consists of switching ripple, which is more obvious at 1000Hz due to proximity to the switching frequency (20kHz). The THD of $i_0(t)$ varies from 2% at 1Hz to 5.1% at 1000Hz.

The power converter consumes 315W active power during 50A rms sinusoidal current generation at 50Hz. The active power consumption goes upto 360W at 1kHz output current. This small power consumption leads to energy saving during long term thermal endurance test conducted on the current sensors during production and qualification.

VI. Conclusion

A novel application of the H-bridge inverter with RCD snubber is proposed for generation of step current and sinusoidal current with variable frequency and amplitude, without significant modification in the hardware configuration. The use of IGBT with higher voltage rating facilitates the rapid rise of the step current, even with the insertion impedance of the inserted sensor. The magnitude and the fall/rise time of the step current can be controlled independently to produce current with adjustable transition time. Analysis of trade-off between peak overshoot of the IGBT, C_{ov} and the transition time t_f is presented. Based on the analysis a guideline is suggested to select the circuit components. Experimental results related to production of the step current with peak value 48A and fall/rise time less than 200ns are shown.

The used hybrid PWM technique is suggested for the switching of the MOSFET leg and the IGBT leg, which results in reduction of total switching loss of the converter during sinusoidal current generation. A scheme is proposed for on-line change of magnitude and frequency of the controlled sinusoidal current. Experimental results are shown for sinusoidal current with 50A rms and fundamental frequency from 1Hz to 1000Hz. The THD of the controlled current in less than 5.1% in the above range. The converter consumes 315W active power from mains during 50A rms sinusoidal current generation at 50Hz. This is useful for conducting long term thermal endurance test on the current sensor with excitation current at grid frequency and its harmonics.

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