Week 1 – Syllabus & Outline

Logic Circuit Design Laboratory

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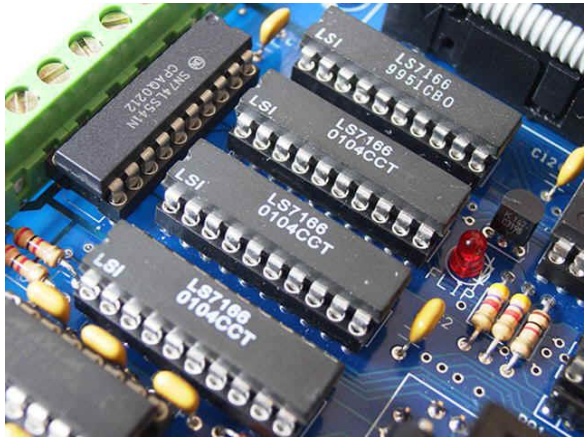
Course Information

- ICE 2005: Logic Circuit Design Lab.
  - Tuesday/Wednesday 6PM
  - 반도체관 400126호 (강의)
  - 반도체관 400325호 (실험)



- Staff
  - Instructor: 이윤명 (yoonmyung@skku.edu , #400416, Tel. x7979)
  - TA: 기형민 gudals6870@gmail.com
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  - Office: 반도체관 #400417
    Tel: x4689

Course Information

- What will I learn?
  - Basic theories of digital logic circuits
  - Hand-on experiments of digital logic design
  - Familiarize yourselves to simulation tools (Quartus, ModelSim)
  - Logic design and verification using Verilog
  - Implementation through field programmable gate array (FPGA)

- Experiments include…
  - Circuit implementation using logic IC
    - Combinational logic including AND, OR, NAND, XOR, and Adder.
    - Sequential logic including flip-flop, counter, encoder, and decoder.
  - Logic design and verification using Verilog
    - Quartus and ModelSim
    - FPGA kit: HBE-COMBO II
  - Final logic circuit system design project
    - HBE-COMBO II : 200k logic gates, LEDs, buttons, LCD, Motor, Buzzer, lights, etc…

Schedule

- No required textbook, following references could be useful
  - Digital Circuit Design using Altera and Xilinx, Hanbaek Electronics (in Korean)
  - Digital Logic Design - Tutorial and Laboratory Exercises, Passafiume and Douglas
  - Fundamentals of Logic Design, Roth (6/e)

Week	Lecture	Lab
01	Welcome, Syllabus and Policy	
02	Bread Board & Boolean equation and Karnaugh Map	Getting familiar with tools Basic gates & Boolean Equations
03	Adder and Subtractor	Adder, Subtractor
04	Multiplexer , Encoder, Decoder	Encoder, Multiplexer, MUX logic
05	Sequential logics	S-R, J-K, Flip-Flop
06	Quiz 1 / Verilog tutorial (금, 녹화?)	
07	Verilog Syntax, ModelSim and Verification	Verilog, ModelSim and Verification
08	Week of Mid-Term Exam (No lecture)	중간고사 주차 전체 휴강
09	LED and 7-Segments,Counter	LED and 7-Segments, Counter
10	Dot Matrix, Step Motor, Piezo, Keypad	Dot Matrix, Step Motor, Piezo, Keypad
11	Quiz 2	Project Assignment
12	Term Project	
13	Term Project	
14	Term Project	
15	Term Project Presentation	

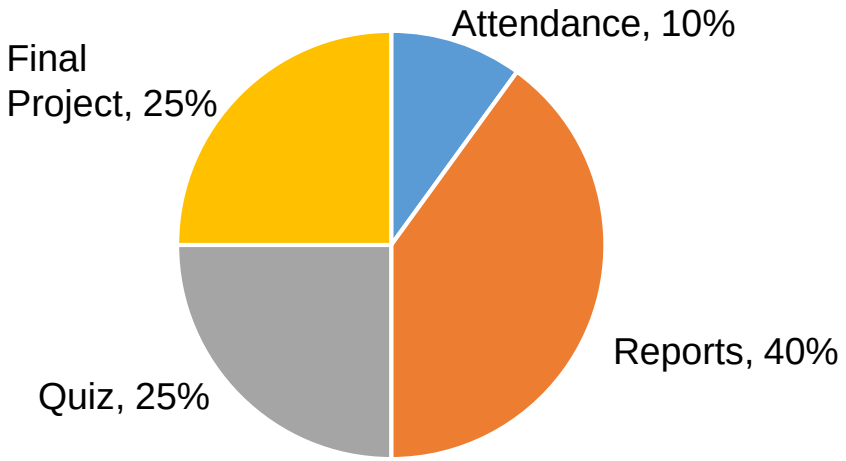
Weekly Routine

- Pre-lab (예비보고서)
  - Contents: 3-4 problems to be solved AND designs to be prepared for the next lab
  - Submit at the beginning of class (6:00 PM)
  - Only hand-written copies are accepted.
  - Late submission penalty: 20% per day for up to two days
- Lecture
  - 6:00pm – 6:30pm (Rm. 400126)
  - Background and fundamentals for laboratory
- Lab (Rm. #400325)
  - In-lab (실험보고서) should be printed in advance and filled out
  - You can submit in-lab report and leave the lab once all your assignment is done
  - You are not allowed to come back once you leave
- Post-lab (결과보고서)
  - Due at the beginning of the next lab (6PM)
  - Lab Report 80%, Discussion 20%
  - Use the template given. Template will be posted on i-Campus.
  - Late penalty: 20% per day for up to two days

Policies

- Communication
  - Class materials are posted on i-Campus (ICE2005-46/47)
  - Use email instructor/TA rather than messaging on i-Campus

- Grading policy
  - Reports: 40%
    - pre + inlab + post
    - Curved at the end of semester
  - Quizzes: 25%
    - Two ~1 hour long quizzes.
  - Final project: 25%
    - Last 3 weeks
    - Demo & report required



- 3 or more absences will result in course failure (SSE Dept. guideline)
- Attendance checked with report submission
- Miscellaneous
  - Don’t mess up your own seat. Please clean your seat after the lab
  - Don’t bring any food to the lab