디지털시스템설계 과제

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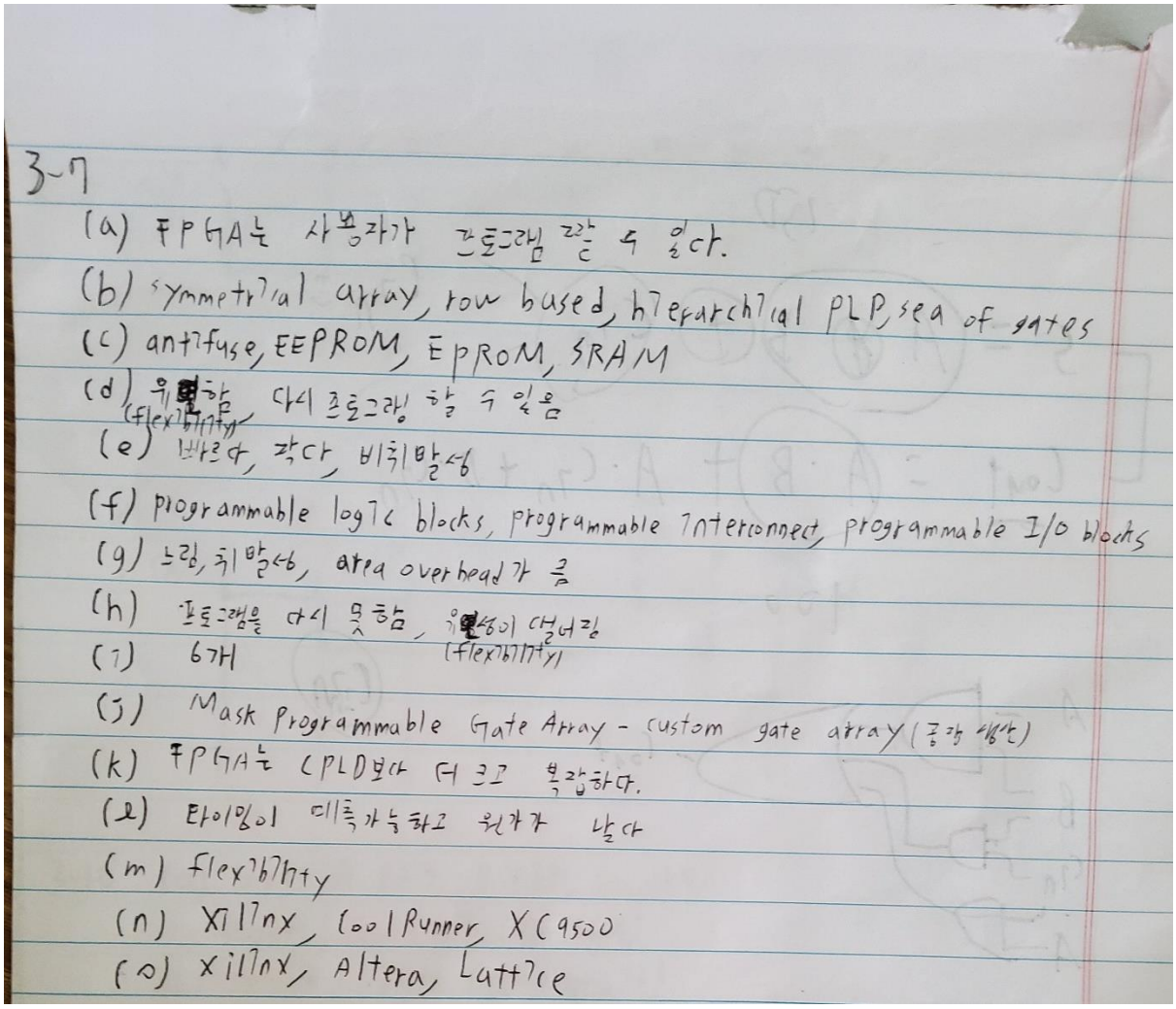


3-7

(a) FPGA는 사용자가 프로그램할 수 있다.

(b) Symmetrical array, row based, hierarchical PLP, sea of gates

(c) antifuse, EEPROM, EPROM, SRAM

(d) 휘발함, 다시 프로그램 할 수 있음 (flexibility)

(e) 빠르다, 작다, 비휘발성

(f) programmable logic blocks, programmable interconnect, programmable I/O blocks

(g) 느림, 휘발성, area overhead가 큼

(h) 프로그램을 다시 못함, 융통성이 떨어짐 (flexibility)

(i) 6개

(j) Mask Programmable Gate Array - custom gate array (공장 생산)

(k) FPGA는 CPLD보다 더 크고 복잡하다.

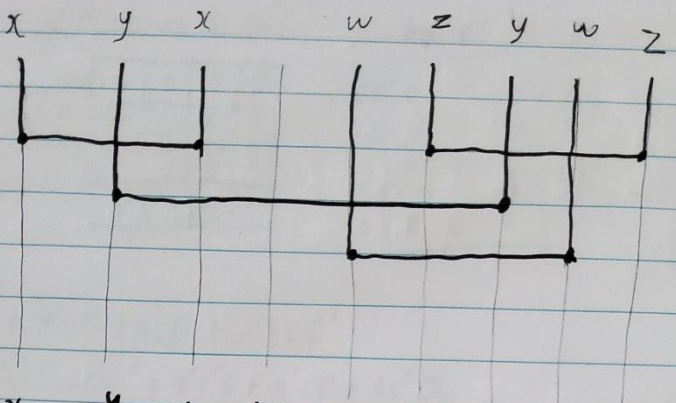
(l) 타이밍이 예측가능하고 원가가 낮다

(m) flexibility

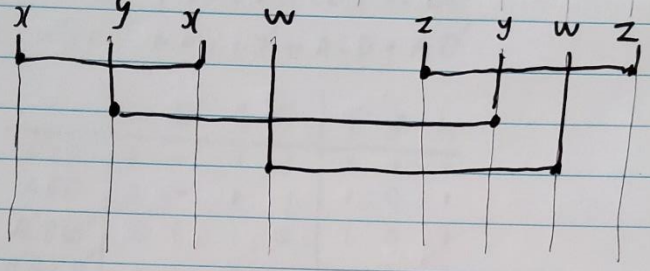
(n) Xilinx, CoolRunner, XC9500

(o) xilinx, Altera, Lattice

3-8 (a)



(b)



3-10 (a) Input (A 8bit, B 8bit, C_{in} 1bit)
Output (Sum 8bit, C_{out} 1bit) ∴ $2^{17} \times 9$

(b) Input (2digit BCD → 8bit)
Output (99까지대비 → 7bit) ∴ $2^8 \times 7$

(c) Input (Select 2bit, Input 4bit)
Output (1bit) ∴ $2^6 \times 1$

(d) Input (32bit x2)
output (33bit) ∴ $2^{64} \times 33$

(e) $2^3 \times 8$

(f) $2^{64} \times 32$

(g) $2^{16+16} \times (16+16) = 2^{32} \times 32$

(h) $2^{16+16+1} \times (16+1) = 2^{33} \times 17$

(i) $2^8 \times (3+1) = 2^8 \times 4$

(j) $2^{10} \times (4+1) = 2^{10} \times 5$

(k) $2^{2+8} \times 1 = 2^{11}$

3-11 (a)

f

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	1	0	0

g

CD \ AB	00	01	11	10
00	0	1	0	0
01	1	0	1	1
11	1	1	0	0
10	0	0	0	0

h

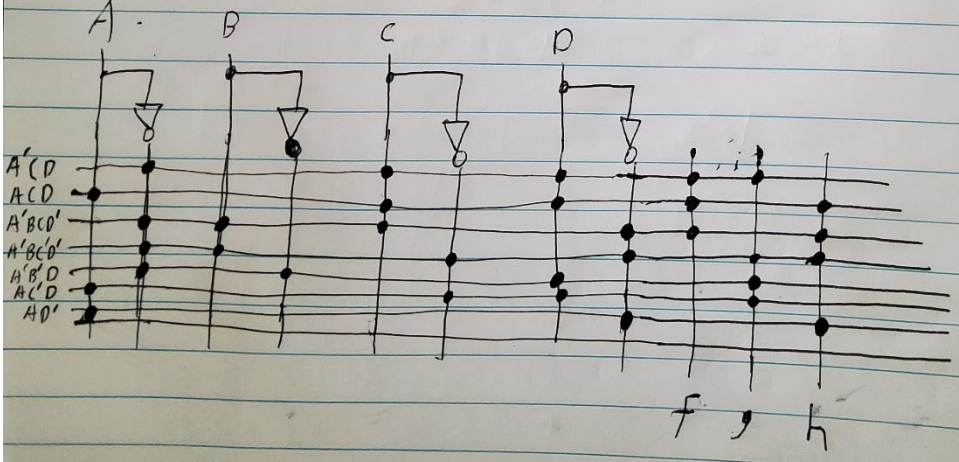
CD \ AB	00	01	11	10
00	0	1	1	1
01	0	0	0	0
11	0	0	1	1
10	0	1	1	1

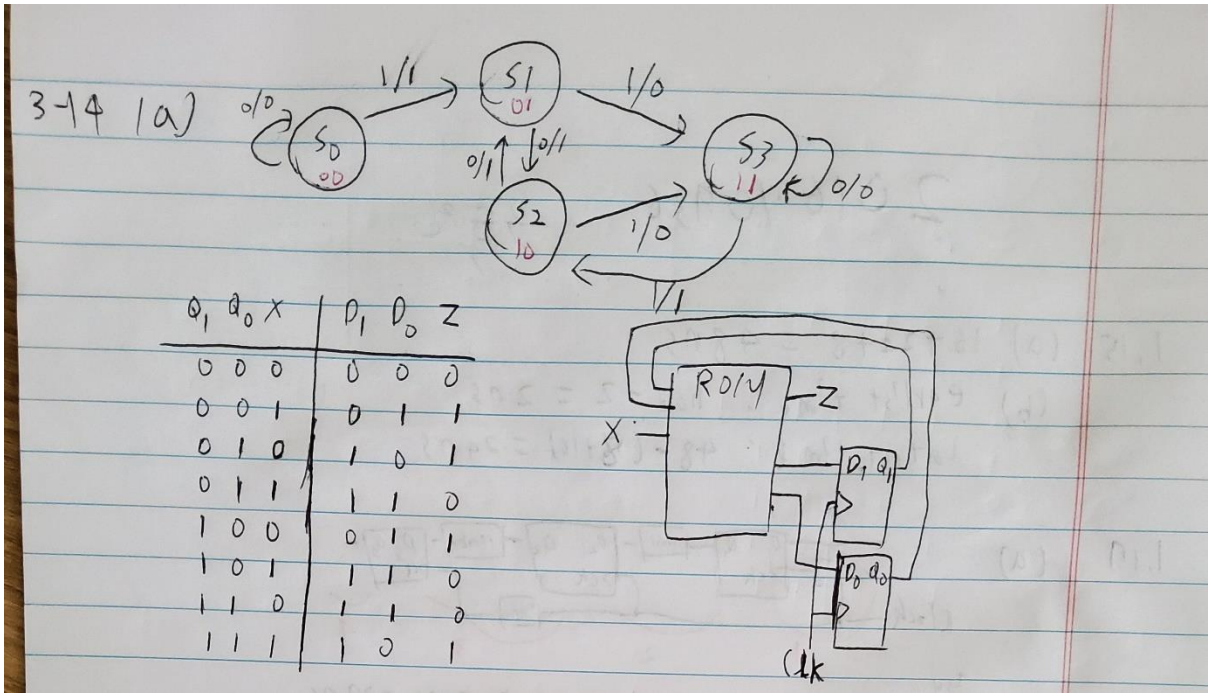
$f = A'CD + ACD + A'BCD'$

$g = A'BC'D' + A'B'D + A'CD + AC'D$

$h = A'BC'D' + A'BCD' + ACD + AD'$

	A	B	C	D	f	g	h
A'CD	0	-	1	1	1	1	0
ACD	1	-	1	1	1	0	1
A'BCD'	0	1	1	0	1	0	1
A'BC'D'	0	1	0	0	0	1	1
A'B'D	0	0	-	1	0	1	0
AC'D	1	-	0	1	0	1	0
AD'	1	-	-	0	0	0	1

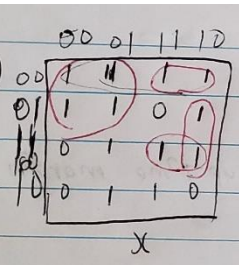


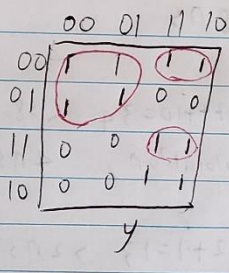


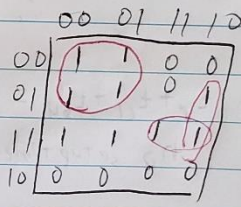
(b)

```
1   module HOM5(X, Clk, Z);
2     input X, Clk;
3     output reg Z;
4     reg [1:0] Q, Qplus;
5     reg [2:0] ROM;
6     reg [2:0] index;
7
8     initial begin
9       Q = 1'b0;
10      Qplus = 1'b0;
11    end
12
13    always @(Q, X)
14      begin
15      index = {Q, X};
16      case(index)
17        3'b000 : ROM = 3'b000;
18        3'b001 : ROM = 3'b011;
19        3'b010 : ROM = 3'b101;
20        3'b011 : ROM = 3'b110;
21        3'b100 : ROM = 3'b011;
22        3'b101 : ROM = 3'b110;
23        3'b110 : ROM = 3'b110;
24        3'b111 : ROM = 3'b101;
25      endcase
26      Qplus = ROM[2:1];
27      Z = ROM[0];
28      end
29
30    always @(negedge Clk)
31      begin
32      Q <= Qplus;
33      end
34  endmodule
```

3-15 (a)







$x = A'C' + C'D' + AB'D + BC$

$y = A'C' + C'D' + AC$

$z = A'C' + CD + AB'D$

	A	B	C	D	x	y	z
$A'C'$	0	-	0	-	1	1	1
$C'D'$	-	-	0	0	1	1	0
$AB'D$	1	0	-	1	1	0	1
BC	-	1	1	-	1	0	0
AC	1	-	1	-	0	1	0
CD	-	-	1	1	0	0	1

(b)