|  |  |
| --- | --- |
| Pre-lab (7주차) | 학번: 이름: |
| (7주차 강의자료 p.17 부터 참조할 것)  1. 다음 Verilog 코드를 설명하시오.   |  |  | | --- | --- | | Half Adder | Description | | module half\_adder(a,b,sum,carry);  input a;  input b;  output wire sum;  output wire carry;  assign sum = x ^ y;  assign carry = x & y;  endmodule |  |  |  |  | | --- | --- | | Half Adder Test Bench | Description | | Module tb\_half\_adder(sum,carry);  reg a;  reg b;  output wire sum;  output wire carry;  half\_adder u0(a,b,sum,carry);  initial  begin  a = 1’b0;  b = 1’b0;  #10;  a = 1’b0;  b = 1’b1;  #10;  a = 1’b1;  b = 1’b0;  #10;  a = 1’b1;  b = 1’b1;  #10;  end  endmodule |  |   2. 위 1번의 half\_adder를 이용하여 full adder 및 2bit full adder 코드를 완성하시오   |  | | --- | | Module full\_adder(a,b,cin,sum,cout);  Input a;  Input b;  Input cin;  Output wire sum;  Output wire cout;  Endmodule  Module Full\_adder\_2b(a,b,cin,sum,cout);  Input [1:0] a;  Input [1:0] b;  Input cin;  Output wire [1:0] sum;  Output wire cout  endmodule | | |