

Demonstration of Ge Nanowire CMOS Devices and Circuits for Ultimate Scaling

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Abstract—In this paper, Ge nanowire (NW) CMOS devices and circuits are analyzed in detail. Various experiment splits are studied, including device geometry parameters such as the channel lengths (L_{ch}) from 100 to 40 nm, a NW height (H_{NW}) of 10 nm, the NW widths (W_{NW}) from 40 to 10 nm, and the dielectric equivalent oxide thicknesses (EOTs) of 2 and 5 nm, and four types of device operation modes of accumulation mode (AM) and inversion mode (IM) n-type MOSFETs and p-type MOSFETs. Benefited from the NW structure with scaled EOT, subthreshold swing (SS) as low as 64 mV/dec and maximum transconductance (g_{max}) as high as 1057 μ S/ μ m are obtained on the Ge NW nMOSFETs. The NW pMOSFETs are also realized on the same common substrate. Furthermore, hybrid Ge NW CMOS with AM nMOSFET and IM pMOSFET is demonstrated for the first time on a Si substrate. The highest maximum voltage gain reaches 54 V/V in the Ge NW CMOS inverters.

Index Terms—CMOS, Ge, GeOI, MOSFET, nanowire (NW), operation mode, scalability.

I. INTRODUCTION

TO EXTEND Moore's law, tremendous efforts have been spent on non-Si materials with higher carrier mobility for the future low-power and high-speed device applications. As one of the most promising candidates for post-Si CMOS, Ge [1]–[3] is quite unique in its high and balanced mobilities for both electrons and holes, and much higher density of states than most of the III–V compounds at conduction band. Promising progresses in Ge MOSFETs research have been realized regarding interfaces [2], [4]–[8], contacts [4], [6], [9], [10], scaling [3], [7], [8], [11], [12], and 3-D channel structures [10]–[13]. On the other hand, in terms of circuit integration, the Ge planar and FinFET CMOS circuits have been realized on GeOI [13]–[16] or poly-Ge substrate [17]. However, to effectively suppress the short channel effects (SCEs) at a 7-nm node and beyond, 3-D nanowire (NW) channel might be needed [18]–[20], which provides the best gate electrostatic control.

In our previous conference report [16], suspended Ge NWs have been successfully demonstrated through a combination of dry etching and selective wet etching process. Recessed channel is also employed in the NW formation to reduce the

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cross-sectional area, hence, enhancing the gate controllability. The NWs are further integrated into the CMOS fabrication, realizing the first Ge 3-D NW CMOS circuits.

In this paper, we expand the previous results [13], [16] and further investigate them comprehensively in the realm of fabrication processes, NW MOSFETs' and circuits' characteristics, and their superiority over the planar channel devices. The fabrication processes of the channel structures from 2-D to 3-D are thoroughly described. Based on more than 1600 well-behaved devices obtained and measured, clear trends of the dependences on L_{ch} , W_{NW} , and operation mode of the NW CMOS devices are observed. The characteristics, such as ON-state drain current (I_{ON}), g_{max} , threshold voltage (V_{TH}), I_{ON}/I_{OFF} ratio, SS, and drain induced barrier lowering (DIBL), are statistically and systematically studied. Furthermore, the NW CMOS inverters with accumulation mode (AM) or inversion mode (IM) nMOSFETs and pMOSFETs are also studied in detail, in terms of their dependence on device geometry size and operation modes.

This paper is organized as follows. Section II describes the experimental processes of the Ge NW CMOS circuits. The device structure designs are explained in Section III. Section IV explains the NW nMOSFETs' characteristics. The NW pMOSFETs are studied in Section V. Section VI investigates the Ge NW CMOS circuits. Section VII compares the difference between the 3-D NW and planar devices. Finally, Section VIII concludes this paper.

II. EXPERIMENT

The fabrication process flow is given in Fig. 1(a). The experiment started with a 4-inch GeOI wafer with 90-nm i-type (100) Ge and 400-nm SiO_2 buried oxide (BOX) on Si from Soitec, made by the Smartcut technology. First, a standard clean (acetone, methanol, and isopropanol soaking in 5/5/5 min sequent order) was carried out, and alignment marks were then patterned and formed by dry etching. Next, the samples were selectively P ($5 \times 10^{15} \text{ cm}^{-2}$ at 15 keV) and BF_2 ($4 \times 10^{15} \text{ cm}^{-2}$ at 15 keV) implanted for nMOSFETs and pMOSFETs. The energy of both the n-type and p-type ion implantations is intentionally reduced to keep a low doping concentration in the recessed channel area for the AM MOSFETs, due to the thinner 90-nm Ge substrate used in this experiment, as compared to the 180-nm Ge substrate in our previous works [15], [21]. Note that a ZEP 520 A e-beam resist mask was used to cover the channel region of the IM MOSFETs to define the channel length.

Following the mesa isolation etching, an optimized common SF₆ dry etching process was applied to form the planar

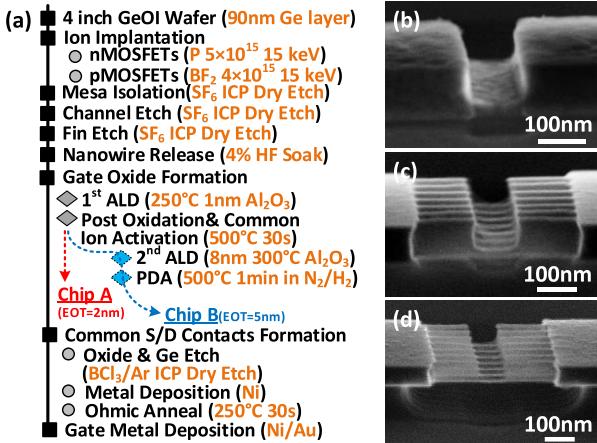


Fig. 1. (a) Fabrication process flow of the Ge NW CMOS. Devices with different gate oxide are fabricated in parallel. (b)–(d) Structure-wise evolution in the channel area: (b) Planar Ge recessed channel standing on the SiO₂ BOX layer. (c) 3-D Ge recessed fin channel standing on the SiO₂ BOX layer. (d) 3-D Ge freestanding recessed NW channel with the bottom SiO₂ removed.

recessed channel [as shown in Fig. 1(b)] for both nMOSFETs and pMOSFETs. Then, fin structures were placed into recessed channel by another common dry etching, shaping the recessed fin structure, as shown in Fig. 1(c). Note that both the recessed channel and the recessed fin structures are standing on the SiO₂ box layer. After that, the NW channel release process was carried out, and the sample was soaked in 4% HF solution and DI water for 30 s cyclically for 3 times, ending at the third HF soaking to keep a clean Ge surface without native oxide. The HF solution could selectively remove SiO₂ underneath the Ge NW channel, suspending the recessed NW [as shown in Fig. 1(d)]. At the same time, since DI water could slightly oxidize Ge and HF could fast remove the native oxide, the HF and DI water soaking would also reduce the surface damages of the NWs caused by the dry etching process and improve the surface roughness.

For the gate dielectric, the sample was transferred into an atomic layer deposition chamber immediately after the NW releasing. 1-nm Al₂O₃ was first grown at 250 °C, which is a relatively low growth temperature in order to suppress the growth of low quality native oxide. Then, a post-oxidation process was performed by rapid thermal oxidation at 500 °C in pure oxygen ambient to form ~2-nm GeO_x underneath Al₂O₃, which also activated the n- and p-dopant ions simultaneously. Due to the high diffusivity of P ions inside Ge at high temperature [4], [22], the processes with high thermal budget in this experiment were carefully calibrated and simplified. Therefore, the common ion activation process was merged with the post-oxidation. Next, 8-nm Al₂O₃ was deposited only for Chip B and no Al₂O₃ was deposited on Chip A. Post deposition annealing was also conducted only on Chip B at 500 °C for 30 s in forming gas ambient. The overall equivalent oxide thickness (EOT) is calculated to be 2 nm for Chip A and 5 nm for Chip B, considering a 2-nm GeO_x ($\kappa = 6$) interfacial layer and 1- or 9-nm Al₂O₃ ($\kappa = 8.5$) dielectrics. Note that the EOT is conservatively estimated here, since the thickness of GeO_x could be thinner in real case [7]. It is also worth mentioning that for the whole experiment, the thermal

budget was conservatively limited to 500 °C, and only one high temperature thermal process was conducted on Chip A, to handle the fast P diffusion issue in Ge.

Recessed S/D dry etching was conducted afterward by first stripping the oxide, and then partially removing the top Ge layer in the source/drain region, based on BC_l₃/Ar as the etchants. The S/D contact metal was formed by 100-nm Ni deposition and ohmic annealing at 250 °C in pure N₂ ambient. Eventually, the gate and interconnection metal were formed by 100/40 nm Ni/Au.

All the lithography was carried out by a Vistec EBPG 5200 electron-beam lithography system using pure ZEP 520A of 500 nm or diluted ZEP 520A of 100 nm as the e-beam resists. In total, nine steps of lithography process were employed in the device fabrication.

III. STRUCTURE DESIGNS

Fig. 2(a) shows the schematic of a Ge 3-D NW CMOS inverter, and lists the experiment splits and cartoons of the four types of MOSFETs fabricated on the same chip. The recessed NWs are adopted to reduce the channel cross-sectional area to enhance the gate electrostatic control. Note that both the IM and AM devices have the NW recessed for better comparison. The cross-sectional cartoon in perpendicular to NW direction is also given in Fig. 2(a) (inset). The top, left, and right side of the NW are covered by the gate metal. Therefore, the channel width (W_{ch}) is calculated from $W_{ch} = (2 \cdot H_{NW} + W_{NW}) \times (\text{number of NWs})$.

Thanks to the well-engineered dry etching process, the smallest fin width (W_{Fin}) of 10 nm with a high aspect ratio of 18 is achievable, as shown in Fig. 2(b). Similarly, the smallest W_{NW} is 10 nm, as shown in Fig. 2(c). In terms of channel length, Fig. 2(d) shows the ZEP 520A e-beam resist mask in channel region of the IM MOSFETs to define the channel length with the smallest L_{ch} of 40 nm. Fig. 2(e) shows the top-down SEM image of a 40 nm W_{NW} NW, clearly indicating that the NW is precisely recessed to have an L_{ch} of 40 nm as reflected by the darker color of the recessed region in the NW.

The NW array in device gate area is shown in Fig. 2(f) with 40-nm long channel marked. To better illustrate the structure, the gate region is zoomed-out in Fig. 2(g). The whole Ge layer is sitting on the SiO₂ BOX layer. As determined by the isotropic nature of SiO₂ wet etching, the SiO₂ beneath the source/drain region is partially etched, but only in the channel area, the SiO₂ is fully removed. The recessed NW is precisely engineered to have a NW height of only 10 nm, as shown in Fig. 2(g) (inset). The numbers of NWs in the channels of pMOSFETs to nMOSFETs are designed to be 11 and 7 for balanced performance, and can be adjusted during the mask layout accordingly, as shown in Fig. 2(h) and (i).

In terms of the substrate, thinner Ge layer of 90 nm used here is preferred, because smaller Ge layer thickness would have smaller series resistance and parasitic capacitance for the recessed channels benefited from the reduced area of the overlap region between gate and source/drain, thus improving the MOSFET performance. For the layout, each chip

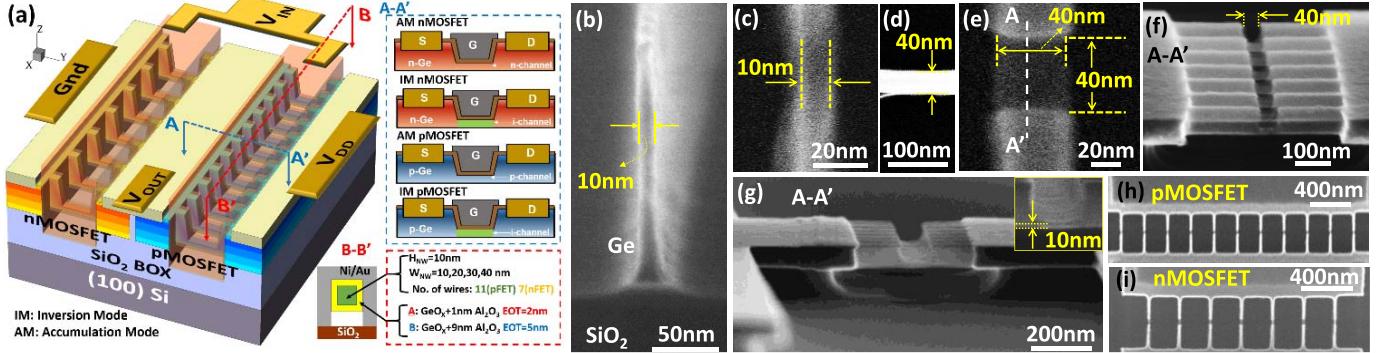


Fig. 2. (a) Device 3-D schematic and key geometry parameters of the Ge NW CMOS. Cross-sectional schematics of the NW CMOS in parallel (A-A') and perpendicular (B-B') to the NW direction with four types of operation modes (AM and IM nMOSFETs, AM and IM pMOSFETs) are listed. (b)–(i) SEM images of various structures on Ge: (b) Titled image of one of the narrowest fin structures with $W_{\text{Fin}} = 10 \text{ nm}$ and an aspect ratio of 18. (c) Top-down image of the narrowest NW with 10-nm W_{NW} . (d) ZEP e-beam resist mask to define the smallest channel length of 40 nm in the IM devices. (e) NW with 40-nm W_{NW} and 40-nm L_{ch} . The darker area on the NW is the recessed region with reduced NW height. (f) Freestanding NWs with 40-nm L_{ch} . (g) Zoomed-out of the Ge NWs (inset: H_{NW} of 10 nm). (h) and (i) NWs in the channel areas of p- and nMOSFETs for CMOS integration.

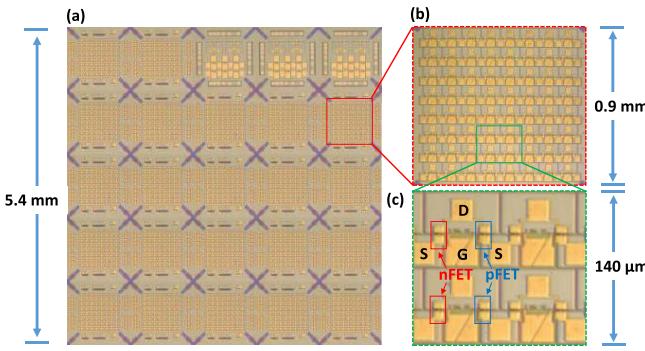


Fig. 3. (a) Top-down view of a fabricated chip under the optic microscope. The size parameters of the chip are marked. (b) Enlargement of one die inside the chip [red square in (a)]. (c) Zoomed-in view of Ge CMOS devices array [green square in (b)].

has ~ 2000 devices patterned on a 5.4 mm^2 substrate, as shown in Fig. 3(a) (optical image). There are 5×5 duplicated dies on each chip, and the three dies on top right corner of the chip are mainly used for testing, such as TLM for contact resistance and large planar devices to extract mobility. Fig. 3(b) shows the image of a single die on the chip, which has nMOSFETs, pMOSFETs, and CMOS circuits included. The MOSFET region is further enlarged in Fig. 3(c) with source, drain, and gate marked. The pMOSFETs and nMOSFETs have the common gate and drain, for the CMOS inverters.

The electrical characterization was carried out using a Keithley 4200 system at room temperature and ~ 1600 devices are measured in total, on both chip A and chip B. The error bars in all figures in this paper are based on ~ 20 measured different devices with the same geometry and fabrication conditions for each data point.

IV. Ge NANOWIRE nMOSFETs

Fig. 4(a) shows the transfer curves of a 100-nm L_{ch} and 20-nm W_{NW} AM NW nMOSFET with an EOT of 2 nm, showing a record low SS of 64.1 mV/dec and $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 1×10^6 at $V_{\text{ds}} = 0.05 \text{ V}$. Another device with smaller W_{NW} of 10 nm is giving in Fig. 4(b), showing positively

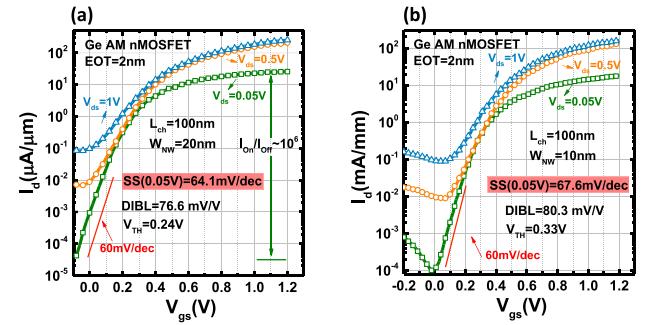


Fig. 4. (a) Transfer curves of a 100-nm L_{ch} and 20-nm W_{NW} Ge AM NW nMOSFET with SS = 64.1 mV/dec at V_{ds} of 0.05 V . (b) $I_{\text{d}} - V_{\text{gs}}$ curves of another device with sub-70 mV/dec SS at V_{ds} of 0.05 V .

shifted V_{TH} and an excellent SS of 67.6 mV/dec . In total, 11 out of 800 measured devices in the same chip have $SS < 70 \text{ mV/dec}$. It proves the excellent gate control enabled by the NW structure, delivering more than 30% and 40% reduced SS over FinFETs and planar MOSFETs, respectively. The reduced $I_{\text{ON}}/I_{\text{OFF}}$ at high V_{ds} is related to the gate induced drain leakage (GIDL) in the device OFF-state, since the gate leakage current is very low (10 times smaller than the lowest OFF-state current). In narrow bandgap materials, such as Ge, the band-to-band tunneling (BTBT), the dominant mechanism in GIDL current, is much severer than that in Si, resulting in more challenging OFF-state leakage control. Band-gap engineering, such as increasing the bandgap in source/drain by using SiGe, can be a potential way to suppress the BTBT near the drain side to improve the $I_{\text{ON}}/I_{\text{OFF}}$ ratio and reduce the power consumption at OFF-state.

Fig. 5(a) shows the V_{TH} versus L_{ch} in the 2-nm EOT NW nMOSFETs with a W_{NW} of 40 nm, and V_{TH} is linearly extrapolated from the transfer curves at V_{ds} of 0.05 V. A small V_{TH} roll-off of only 0.1 V is obtained, indicating the excellent scaling capability of the NW structures. The AM devices are majority carrier devices with n-type dopants in the channel, which make the devices easier to turn ON. Thus, V_{TH} of the AM devices is smaller than that of the IM ones. In terms of the W_{NW} dependence of V_{TH} , as shown in Fig. 5(b), V_{TH} increases

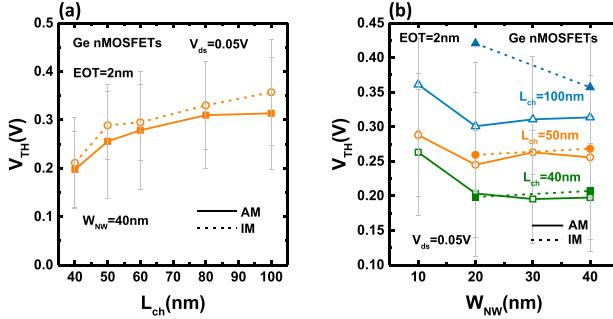


Fig. 5. (a) V_{TH} scaling metrics of the Ge NW nMOSFETs with an EOT of 2 nm and 40-nm W_{NW} . IM and longer L_{ch} nMOSFETs have larger V_{TH} . (b) W_{NW} dependence of the V_{TH} of the AM and IM Ge NW nMOSFETs with an EOT of 2 nm. Smaller W_{NW} devices have larger V_{TH} .

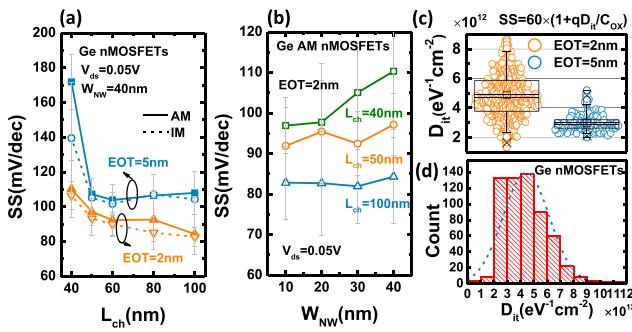


Fig. 6. (a) SS scaling metrics of the AM and IM Ge NW nMOSFETs with an EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and smaller EOT devices have better SS. (b) W_{NW} dependence of the SS of the AM Ge NW nMOSFETs with an EOT of 2 nm. Smaller W_{NW} devices have better SS. (c) BOX plot for mid-gap D_{it} of Ge NW nMOSFETs with 2- and 5-nm EOT, extracted from SS based on more than 800 measured data points. (d) Histogram for mid-gap D_{it} .

with smaller NW width, due to better SCEs immunity. Similar to that shown in Fig. 5(a), the IM devices have higher V_{TH} . Meanwhile, with reduced NW size, quantum effects would be more prominent, which could also shift the V_{TH} .

The excellent gate control in the NW devices can also be reflected in the SS dependence, as shown in Fig. 6(a). It gives the SS scaling metrics of the 40-nm W_{NW} NW nMOSFETs with an EOT of 5 and 2 nm at V_{ds} of 0.05 V. Thanks to the NW structure, SS is well controlled to be ~ 100 mV/dec for $L_{ch} > 60$ nm, but with decreasing L_{ch} , SS degrades significantly, due to SCEs. Meanwhile, according to capacitance model [23], larger gate capacitance compared with the source/drain capacitances could effectively enhance the gate modulation. Hence, the devices with 2-nm EOT deliver 20% reduced SS, as compared with the 5-nm EOT ones. The IM devices show better SS, mainly attributed to the undoped channel. As well accepted, higher vertical gate electrical field is expected in the undoped channel [24], delivering better controllability of gate over the channel, in competition with the horizontal electrical field from the source/drain bias. Similarly, smaller NW size could also provide higher gate electrical field. Therefore, SS would be reduced with smaller W_{NW} , as demonstrated by the SS dependence on W_{NW} shown in Fig. 6(b).

The mid-gap D_{it} is also extracted from the equation $SS = 60 \times (1 + qD_{it}/C_{ox})$, based on more than

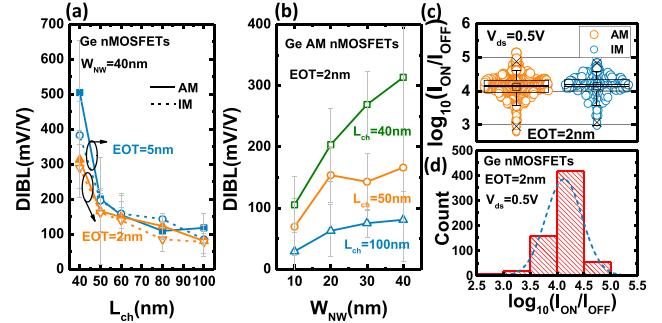


Fig. 7. (a) DIBL scaling metrics of the AM and IM Ge NW nMOSFETs with an EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and smaller EOT devices have better DIBL. (b) W_{NW} dependence of the DIBL of the AM Ge NW nMOSFETs with an EOT of 2 nm. Smaller W_{NW} devices have better DIBL. (c) and (d) BOX plot and histogram of the I_{ON}/I_{OFF} of the Ge NW nMOSFETs with the EOTs of 2 nm at V_{ds} of 0.5 V based on more than 800 measured data points.

800 devices with $L_{ch} = 50\text{--}100$ nm and different EOTs. The BOX plot and histogram of mid-gap D_{it} are presented in Fig. 6(c) and (d), and the median is almost the same as the average, indicating a near symmetrical data distribution. The lowest D_{it} is $7 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$, and the mean value is $\sim 4 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, indicating a good interface realized by the post oxidation technique [7]. Meanwhile, it is found that the 5-nm EOT devices have better interface, which could be related with the experiment processes. Since 2-nm EOT devices only have 1-nm Al_2O_3 thin capping layer, rather than the 9-nm Al_2O_3 in the thicker 5-nm ones, the 2-nm EOT devices would be more vulnerable and sensitive to the processes in following and their interface quality could be more affected and degraded.

As another key figure of merit in the MOSFET's OFF-state, DIBL is also analyzed. Fig. 7(a) shows the DIBL dependences on L_{ch} of the nMOSFETs with different EOTs and operation modes. Similar to the case of SS, smaller EOT and IM devices have smaller DIBLs, owing to better SCE immunity. The DIBL relation with W_{NW} is given in Fig. 7(b), and smaller NW size reduces DIBL.

Thanks to the BOX SiO_2 blocking the junction leakage from drain to substrate and the 3-D NW channel effectively suppressing the subthreshold leakage, the Ge NW nMOSFETs in this paper have high I_{ON}/I_{OFF} ratio. Fig. 7(c) and (d) provides the BOX plot and histogram of I_{ON}/I_{OFF} of the Ge NW nMOSFETs with an EOT of 2 nm at high V_{ds} of 0.5 V. The IM devices show slightly higher I_{ON}/I_{OFF} ratio due to better gate control. The mean value is $\sim 3 \times 10^4$, and the highest value is 5×10^5 . For V_{ds} of 0.05 V, the mean and highest I_{ON}/I_{OFF} values are 2×10^5 and 1.5×10^6 .

By further scaling down the channel length, together with reduced EOT, the devices' ON-state performance can be further enhanced. Fig. 8(a) shows the transfer characteristics of a high-performance AM NW nMOSFET with L_{ch} of 40 nm, W_{NW} of 30 nm and an EOT of 2 nm. It is an enhancement mode device with a positive V_{TH} of 0.25 V, and the ON-state drain current reaches a record high value of $662 \mu\text{A}/\mu\text{m}$ [10]–[12] at $V_{gs} - V_{TH} = V_{ds} = V_{DD} = 1$ V. In addition, the SS still keeps at a low value of 93 mV/dec, and I_{ON}/I_{OFF} ratio is $\sim 10^5$ at such scaled channel length, proving the excellent scalability of the

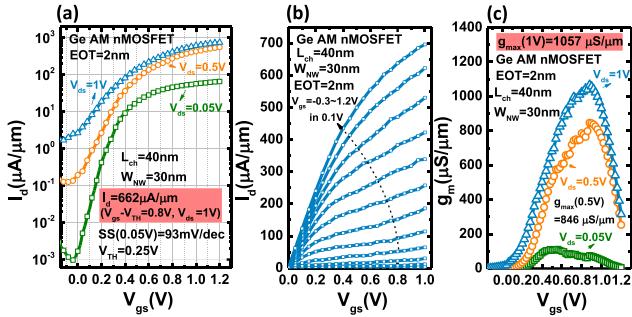


Fig. 8. (a) Transfer curves of a 40-nm L_{ch} , 30-nm W_{NW} , and 2-nm EOT Ge AM NW nMOSFET with I_{ON} of $662 \mu\text{A}/\mu\text{m}$ at V_{ds} of 1 V and $V_{gs} - V_{TH} = 0.8\text{ V}$. (b) Output curves of the same device in (a). The I_{max} is $\sim 700 \mu\text{A}/\mu\text{m}$. (c) g_m versus V_{gs} curves of the same device given in (a). Record high g_{max} of $1057 \mu\text{S}/\mu\text{m}$ is obtained.

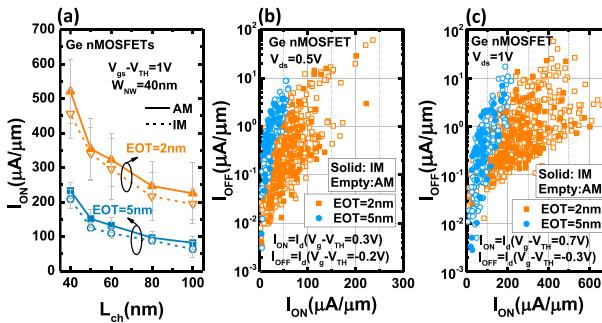


Fig. 9. (a) I_{ON} scaling metrics of the AM and IM Ge NW nMOSFETs with the EOTs of 2 and 5 nm. AM and smaller EOT devices have larger I_{ON} . (b) I_{OFF} versus I_{ON} of the AM and IM Ge nMOSFETs with L_{ch} from 100 to 40 nm and different EOTs at low V_{DD} of 0.5 V. (c) I_{OFF} versus I_{ON} of the Ge AM and IM nMOSFETs with L_{ch} from 100 to 40 nm and different EOTs at high V_{DD} of 1 V.

NW structures. The output curves are presented in Fig. 8(b) with V_{gs} sweeping from -0.3 to 1.2 V in 0.1 V step and maximum current is $\sim 700 \mu\text{A}/\mu\text{m}$.

Fig. 8(c) presents the $g_m - V_{gs}$ curves of the same device in Fig. 8(a), and a record high g_{max} of $1057 \mu\text{S}/\mu\text{m}$ is obtained at $V_{ds} = 1\text{ V}$, benefited from the scaled EOT of 2 nm and NW channel structure. Meanwhile, the quality factor of this device is calculated to be $g_{max}/SS_{sat} = 5.42$ at $V_{ds} = 0.5\text{ V}$, which is almost twice of the best value reported earlier on Ge [10].

Fig. 9(a) gives the I_{ON} scaling metrics of the 40-nm W_{NW} devices. Smaller EOT significantly enhances the I_{ON} by 120% at the same $V_{gs} - V_{TH} = 1\text{ V}$, due to more carriers induced by the more than twice higher gate capacitance. As determined by Fermi-level alignment to the trap neutral level near the valence band edge (E_V) inside Ge [25], [27], AM nMOSFET would get much higher carrier density compared with IM nMOSFET, as proved by the 25% drain current improvement. Meanwhile, it is also reported [26] that the AM devices would have higher mobility than the IM ones, which could also be attributed to higher drain current.

The I_{OFF} versus I_{ON} relationships at low V_{DD} of 0.5 V for all the Ge nMOSFETs (including different EOTs, L_{ch} s, W_{NW} s, and operation modes) are further shown in Fig. 9(b). The I_{OFF} is determined as the drain current at $V_{gs} - V_{TH} = -0.2\text{ V}$, and I_{ON} is defined at $V_{gs} - V_{TH} = 0.3\text{ V}$. The statistical plot

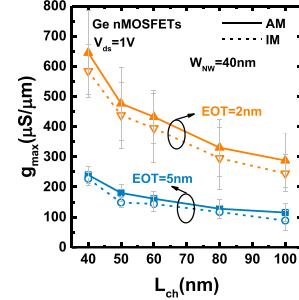


Fig. 10. g_{max} scaling metrics of the AM and IM Ge NW nMOSFETs with an EOT of 2 and 5 nm. AM and smaller EOT devices have larger g_{max} .

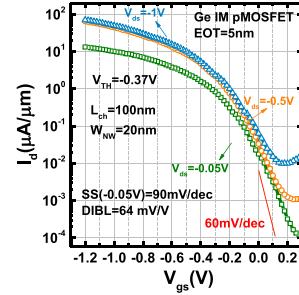


Fig. 11. Transfer curves of a 100-nm L_{ch} and 20-nm W_{NW} Ge IM NW pMOSFET with an EOT of 5 nm.

clearly indicates that smaller EOT could remarkably improve the drive current, as proved by the different slopes of the devices with 2- and 5-nm EOT. The data points of the IM and AM devices overlap and show the same trend. In addition, the I_{ON} is $\sim 100 \mu\text{A}/\mu\text{m}$ at fixed I_{OFF} of $100 \text{nA}/\mu\text{m}$ at low V_{DD} of 0.5 V. By increasing the drive voltage to 1 V, as shown in Fig. 9(c), the drive current is further enhanced to $\sim 200 \mu\text{A}/\mu\text{m}$ at the same fixed I_{OFF} , with the penalty of increased OFF-state current. Note that the I_{OFF} is defined at $V_{gs} - V_{TH} = -0.3\text{ V}$ and $V_{gs} - V_{TH} = 0.7\text{ V}$ for I_{ON} here, in case of $V_{DD} = 1\text{ V}$.

Maximum transconductance can also be used to reflect the ON-state performance, as shown by the g_{max} versus L_{ch} curves at V_{ds} of 1 V in Fig. 10. Similar to that of I_{ON} , g_{max} is improved in smaller L_{ch} and the smaller EOT and AM devices.

V. Ge NANOWIRE pMOSFETS

A typical Ge NW pMOSFET is given in Fig. 11. This IM device has an EOT of 5 nm, W_{NW} of 20 nm, and L_{ch} of 100 nm. Benefitted from NW structure, the device still maintains a good SS of 90 mV/dec and a high I_{ON}/I_{OFF} ratio of 10^5 although the gate dielectric is fairly thick. Resulted from the Fermi-level alignment near E_V in Ge, IM pMOSFET is preferred for better OFF-state performance, since it is harder to move E_F to the conduction band edge (E_C) to turn the device OFF in AM pMOSFET with a p-type channel [21].

Fig. 12(a) shows the V_{TH} scaling metrics of the 40-nm W_{NW} pMOSFETs, pointing out that the smaller EOT devices have more negative V_{TH} , due to better SCEs immunity when scaling the EOT. Similar to that of the AM nMOSFETs, the p-type dopants in the AM pMOSFETs would need extra

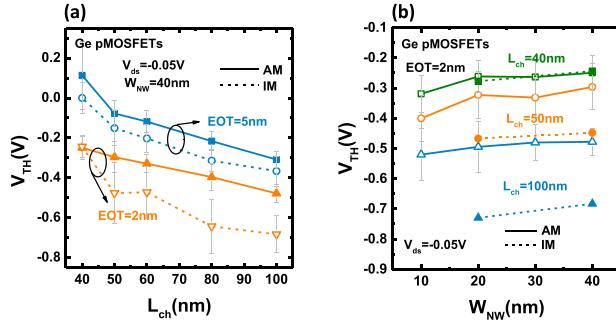


Fig. 12. (a) V_{TH} scaling metrics of the AM and IM Ge NW pMOSFETs with an EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and thinner EOT pMOSFETs have larger V_{TH} . (b) W_{NW} dependence of the V_{TH} of the AM and IM Ge NW pMOSFETs with an EOT of 2 nm. Smaller W_{NW} devices have larger V_{TH} .

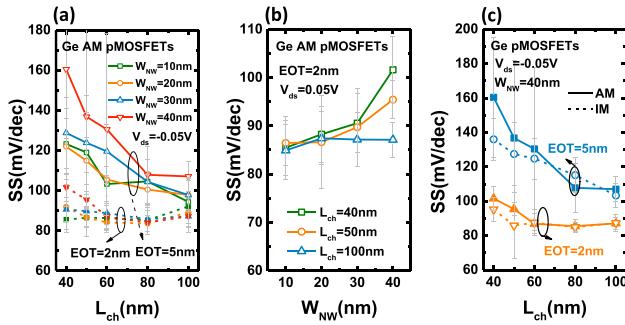


Fig. 13. (a) SS scaling metrics of the Ge AM NW pMOSFETs with an EOT of 2 and 5 nm and W_{NW} of 20, 30, or 40 nm. (b) W_{NW} dependence of the SS of the AM Ge NW pMOSFETs with an EOT of 5 nm. Smaller W_{NW} devices have better SS. (c) SS scaling metrics of the AM and IM Ge NW pMOSFETs with an EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and smaller EOT devices have better SS.

positive gate bias to fully deplete the channel, and thus shift the V_{TH} positively, making the V_{TH} of the AM pMOSFETs smaller. Fig. 12(b) shows V_{TH} versus W_{NW} of the AM and IM pMOSFETs, indicating that smaller W_{NW} increases V_{TH} , and inversion operation mode shifts the V_{TH} negatively in pMOSFETs.

In accordance with that of the nMOSFETs, smaller EOT could improve SS significantly for the pMOSFETs as well, as shown in Fig. 13(a). The SS of 2-nm EOT devices is well controlled to be ~ 90 mV/dec, and shows weak dependence on L_{ch} . Whereas, the 5-nm EOT devices have 30% larger SS values, and the SS almost linearly increases with decreasing L_{ch} . This distinction clearly points out that smaller EOT provides better scalability. The W_{NW} dependence of SS is given in Fig. 13(b), taking 2-nm EOT devices as the example. SS is suppressed with reducing W_{NW} . Especially, SS is almost independent on L_{ch} for devices with 10-nm W_{NW} , indicating the excellent gate control in smaller NWs.

As mentioned before, IM pMOSFET is theoretically predicted to have better OFF-state performance due to E_F alignment close to E_V in Ge [21]. It has been experimentally confirmed in Fig. 13(c). For both the 2- and 5-nm EOT devices, the IM pMOSFETs have smaller SS, which is even more prominent in shorter channel case ($L_{ch} < 60$ nm).

By using the AM devices, together with smaller EOT and L_{ch} , the ON-state performance can be improved

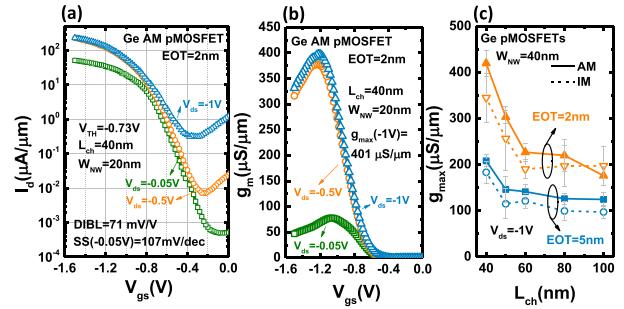


Fig. 14. (a) Transfer curves of a 40-nm L_{ch} and 30-nm W_{NW} Ge AM NW pMOSFETs. (b) g_m versus V_{gs} curves of the same Ge AM NW pMOSFETs given in (a). (c) g_{max} scaling metrics of the AM and IM Ge NW pMOSFETs with an EOT of 2 and 5 nm. AM and smaller EOT devices have larger transconductance.

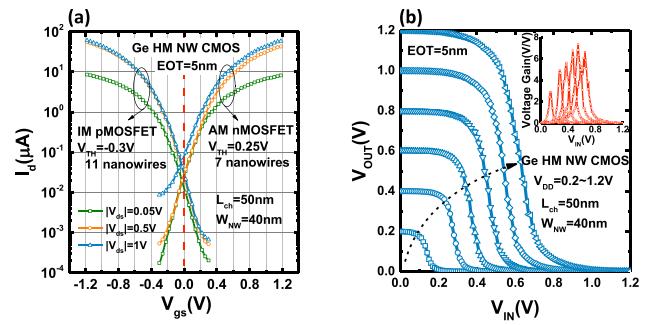


Fig. 15. (a) $I_d - V_{gs}$ of the AM nMOSFET and the IM pMOSFET inside a 50-nm L_{ch} and 40-nm W_{NW} hybrid Ge NW CMOS inverter with a 5-nm EOT. The two show symmetrical performance. (b) V_{out} versus V_{in} of the same CMOS inverter shown in (a). Inset: voltage gain.

significantly, as shown in Fig. 14(a). The I_{ON} is $135 \mu\text{A}/\mu\text{m}$ at $V_{gs} - V_{TH} = V_{ds} = V_{DD} = -0.5$ V. However, as the penalty, the OFF-state performance is deteriorated, as proved by the degraded SS of 107 mV/dec and reduced I_{ON}/I_{OFF} of 10^3 at high V_{ds} of -1 V. The g_m versus V_{gs} curves of the same device are presented in Fig. 14(b), showing a g_{max} of $401 \mu\text{S}/\mu\text{m}$ at $V_{ds} = -1$ V.

The g_{max} dependence on L_{ch} of the Ge NW pMOSFETs is shown in Fig. 14(c). Similar to that of the nMOSFETs, g_{max} is enhanced in smaller EOT, AM, and shorter channel devices.

VI. Ge NANOWIRE CMOS

In the condition of four types of MOSFETs studied here, three combinations of pMOSFETs and nMOSFETs are used for CMOS inverter interconnection: hybrid mode (HM) CMOS composed of AM nMOSFET and IM pMOSFET, IM CMOS composed of IM nMOSFET and IM pMOSFET, and AM CMOS composed of AM nMOSFET and AM pMOSFET.

Resulted from that E_F tends to align near E_V in Ge [21], [25], [27] for nonideal Ge-oxide interface, it is hard to turn ON the IM nMOSFETs and turn OFF the AM pMOSFETs [21], [25]. Therefore, HM CMOS with AM nMOSFET and IM pMOSFET is preferred for Ge, as a tradeoff between ON- and OFF-state performance.

Fig. 15(a) shows the transfer curves of IM pMOSFET and AM nMOSFET inside a 50-nm L_{ch} and 40-nm W_{NW} Ge HM NW CMOS inverter with an EOT of 5 nm. As carefully

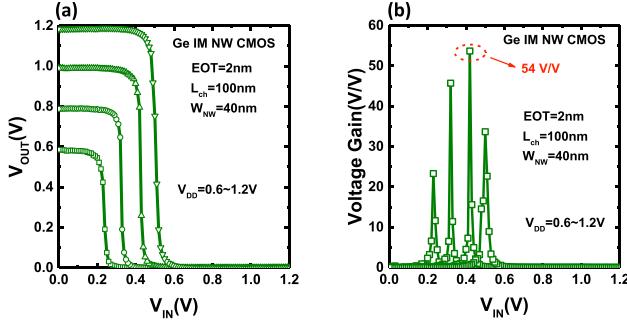


Fig. 16. (a) V_{OUT} versus V_{IN} of a 100-nm L_{ch} , 40-nm W_{NW} , and 2-nm EOT Ge IM NW CMOS inverter with (b) highest voltage gain of 54 V/V.

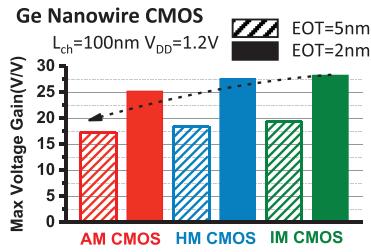


Fig. 17. Maximum voltage of the Ge NW CMOS inverters with different operation modes and EOTs.

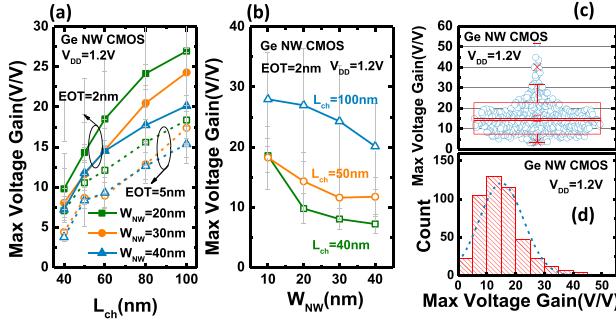


Fig. 18. (a) Maximum voltage gain scaling metrics of all the three types of Ge NW CMOS inverters with an EOT of 2 and 5 nm and W_{NW} of 20, 30, and 40 nm. Thinner EOT devices have larger voltage gain. (b) W_{NW} dependence of the maximum voltage gain of all the three types of Ge NW CMOS inverters with an EOT of 2 nm. Smaller W_{NW} devices have better values. (c) and (d) BOX plot and histogram for the maximum voltage gain of all the three types of Ge NW CMOS inverters at V_{DD} of 1.2 V based on more than 400 measured devices.

designed. The two devices show symmetrical performance in terms of $|V_{\text{TH}}|$ of $\sim 0.3\text{V}$, the SS of $\sim 100\text{mV/dec}$, DIBL close to 100mV/V , $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 10^5 and balanced drain current, which are crucial for well-behaved CMOS applications with low power and high speed. The $V_{\text{IN}} - V_{\text{OUT}}$ curves of this inverter are given in Fig. 15(b) with V_{DD} from 0.2 to 1.2 V. As shown in Fig. 15(b) (inset), the maximum voltage gain is $\sim 7\text{V/V}$, which is about 2 times higher than that of the planar CMOS inverters we have demonstrated before [15] at the same L_{ch} . By further reducing the EOT to 2 nm, increasing L_{ch} to 100 nm, and using IM CMOS, much steeper $V_{\text{IN}} - V_{\text{OUT}}$ curves were achieved, as shown in Fig. 16(a). Given in Fig. 16(b), the maximum voltage gain is 54 V/V at a low V_{DD} of 1 V, which is comparable with the result of the state of the art Si NW CMOS inverters [20], [28]–[30].

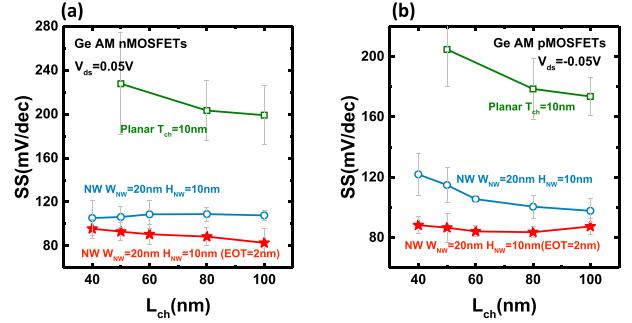


Fig. 19. SS versus L_{ch} of the Ge NW MOSFETs with different EOTs and planar MOSFETs at low V_{ds} of $\pm 0.05\text{V}$. (a) AM nMOSFETs. (b) AM pMOSFETs.

The maximum voltage gain is a critical parameter in the CMOS inverters, reflecting how fast an inverter could switch in responding to an input signal. It is defined as $\Delta V_{\text{OUT}}/\Delta V_{\text{IN}}$ and is directly related to the output conductance (g_d) of its MOSFET components and smaller g_d gives higher voltage gain. Meanwhile, in MOSFETs, g_d in the saturation region is mainly determined by DIBL. In other words, better SCEs immunity reduces DIBL, thus improves the maximum voltage gain of the CMOS inverters. Fig. 17 compares the maximum voltage at V_{DD} of 1.2 V of various CMOS inverters with different operation modes and the EOTs we fabricated. As discussed before, better gate control has been confirmed in the IM or smaller EOT MOSFETs. Therefore, smaller EOT and IM inverters have highest maximum voltage gains, and the AM inverters with 5-nm EOT deliver the lowest value. Meanwhile, an HM device, as a compromise between SCEs immunity and current drivability, is in the middle of the three.

The maximum voltage gain is further compared in Fig. 18(a) and (b) in terms of L_{ch} and W_{NW} . All the three types (HM, IM, and AM) of the CMOS inverters with different EOTs, L_{ch} s and W_{NW} s are included. Longer channel devices have higher maximum voltage gains. In agreement with the EOT dependence, it is also improved with smaller W_{NW} due to better gate control over channel with smaller NW size. Note that the noise margin, another key inverter parameter, is not used here for comparison due to the noncalibrated V_{TH} in the AM and IM CMOS devices. Fig. 18(c) and (d) provide the box plot and histogram of the maximum voltage gain based on more than 400 measured Ge NW CMOS inverters. It has an average maximum voltage gain of 15 V/V, delivering more than 200% enhancement over the planar ones [15].

VII. SUPERIORITY OF NANOWIRE STRUCTURE

A comparison between the NW devices and the planar devices is also conducted. Fig. 19(a) and (b) benchmark the SS versus L_{ch} relationship of the Ge NW devices over the planar ones, for nMOSFETs and pMOSFETs, respectively. For accuracy, extremely thin body (ETB) MOSFETs [14] having a channel thickness (T_{ch}) of 10 nm, same as the H_{NW} of NW devices, are taken as the matched group. Surprisingly, NW device shows remarkably small SS than the planar ones with the ETB channels. Especially, the SS of the 2-nm EOT NW devices is even smaller than half of that of the planar devices.

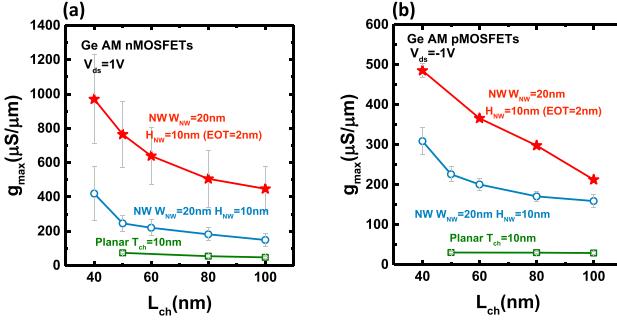


Fig. 20. Maximum transconductance relationships with L_{ch} SS of the Ge NW MOSFETs with different EOTs and planar MOSFETs at low V_{ds} of ± 0.05 V. (a) AM nMOSFETs. (b) AM pMOSFETs.

It clearly points out that 3-D gate control is of great advance for the short channel devices, and scaling EOT is also needed when applying the 3-D channel structures.

Besides using SS to represent the OFF-state performance, the ON-state performance is also benchmarked, by comparing g_{max} . The g_{max} versus L_{ch} curves of the same sets of devices in Fig. 19 are presented in Fig. 20(a) and (b). As reported earlier [14], [31], the Ge ETB device has severe mobility degradation due to the surface roughness scattering and high interface trap density existing in the nonoptimized interface between Ge and SiO_2 BOX layer. Therefore, their g_{max} are fairly small, which are ~ 100 and $50 \mu\text{S}/\mu\text{m}$ for nMOSFETs and pMOSFETs, respectively. However, the surface roughness scattering and the large D_{it} in the back interface could be effectively suppressed or eliminated by etching away the SiO_2 beneath the channel region in NW devices. Therefore, NW devices without the defective back interface show much better g_{max} , which are 3–7 times higher than those of the planar ones.

VIII. CONCLUSION

We present a systematical and statistical study on the Ge NW CMOS devices and circuits with H_{NW} of 10 nm, W_{NW} of 40 to 10 nm, L_{ch} of 100 to 40 nm, EOT of 2 and 5 nm, and different operation modes of AM and IM. Various device performance dependences on L_{ch} , W_{NW} , EOT, and operation modes are studied in great detail. The NW CMOS shows superior performance in both the OFF- and ON-states, as compared with the planar CMOS. A Record low SS of 64 mV/dec and record high g_{max} of $1057 \mu\text{S}/\mu\text{m}$ are obtained. This paper shows the promise of applying Ge as the high mobility channel material for the future post-Si CMOS technology.

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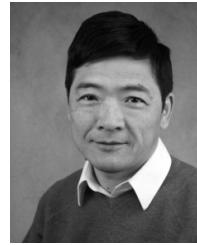
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