Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

Table 1-1 Platform Feature Overview

Feature		TC38x
CPUs	Type	TC1.6.2
	Cores / Checker Cores	4 / 2
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB
	DSPR	240 KB for CPU0,1 / 96 KB else
	DLMU	64 KB
SRAM global	LMU	128 KB
	DAM	64 KB
Extension Memory	TCM	- MB
	XCM	- MB
	XTM	- KB
Program Flash	Size	10 MB
	Banks	3 x 3 MB, 1 x 1 MB
Data Flash	Size (single-ended)	512 KB (DF0) + 128 KB (DF1)
DMA	Channels	128
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	8 / 64
	Secondary Groups/Channels	4 / 64
	Fast Compare Channels	4
EDSADC	Channels	10

Table 1-1 Platform Feature Overview (cont'd)

Feature		TC38x
GTM	Clusters	9 (5 @ 200MHz, 4 @ 100MHz)
	TIM (8 ch)	7
	TOM (16 ch)	5
	ATOM (8 ch)	9
	MCS (8 ch)	7
	CMU / ICM	1 / 1
	PSM	2
	TBU channels[1)]	4 (TBU0-3)
	SPE	4
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
	CDTM modules	6
	DTM modules	20 (8 on TOM, 12 on ATOM)
Timer	GPT12	1
	CCU6	1
STM	Modules	4
FlexRay	Modules	2
	Channels	2
CAN	Modules	3
	Nodes	3 x 4
	of which support TT-CAN	1
QSPI	Modules	5
	HSCI Channels	-
ASCLIN	Modules	24
I2C	Interfaces	2
SENT	Channels	25
PSI5	Modules	4
PSI5-S	Modules	1
HSSL	Channels	1
MSC	Channels	3
SDMMC	eMMC/SD Interface	0
Ethernet (10/100Mbit/1Gbit)	Modules	1
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
SPU	Modules	-
RIF	Modules	-
HSPDM	Modules	-

Table 1-1 Platform Feature Overview (cont'd)

Feature		TC38x
Security	HSM+	1
Debug	OCDS	yes
	MCDS	no
	miniMCDS	yes
	miniMCDS TRAM	8 KB
	AGBT	No
Low Power Features	Standby RAM	2
	SCR	yes
Packages	Type	FBGA-516 / LFBGA-292
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
$T_{ambient}$	Range	−40 … +150°C

1) TBU3 has special purpose as angle clock.