# TC397XA B-step BMHD

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# Four sets of BMHD_x

### 2.6.3.1 UCB_BMHDx_ORIG and UCB_BMHDx_COPY (x = 0 - 3)

**Table 2-6 UCB_BMHDx_ORIG and UCB_BMHDx_COPY**

| Offset | Content | Range | Description |
|---|---|---|---|
| $000_H$ | BMI | 2 Byte | Boot Mode Index (BMI). |
| $002_H$ | BMHDID | 2 Byte | Boot Mode Header ID (CODE) = $B359_H$. |
| $004_H$ | STAD | 4 Byte | ABHMDx start address (in case BMI.HWCFG = ABM = $110_H$).<br>User Code start address (in case BMI.HWCFG = Flash start = $111_H$). |
| $008_H$ | CRCBMHD | 4 Byte | Check Result for the BMI Header (offset $000_H$ - $007_H$). |
| $00C_H$ | CRCBMHD_N | 4 Byte | Inverted Check Result for the BMI Header (offset $000_H$ - $007_H$). |
| $1F0_H$ | Confirmation | 4 Byte | 32-bit CODE. |
| $1F4_H$ | Reserved | 4 Byte | Reserved. |
| $1F8_H$ | Reserved | 4 Byte | Reserved. |
| $1FC_H$ | Reserved | 4 Byte | Reserved. |

| Address Range | Size | Unit |
|---|---|---|
| AF40 $0000_H$ - AF40 $01FF_H$ | 512 Byte | UCB00 (UCB_BMHD0_ORIG) |
| AF40 $0200_H$ - AF40 $03FF_H$ | 512 Byte | UCB01 (UCB_BMHD1_ORIG) |
| AF40 $0400_H$ - AF40 $05FF_H$ | 512 Byte | UCB02 (UCB_BMHD2_ORIG) |
| AF40 $0600_H$ - AF40 $07FF_H$ | 512 Byte | UCB03 (UCB_BMHD3_ORIG) |

| | | |
|---|---|---|
| AF40 $1000_H$ - AF40 $11FF_H$ | 512 Byte | UCB08 (UCB_BMHD0_COPY) |
| AF40 $1200_H$ - AF40 $13FF_H$ | 512 Byte | UCB09 (UCB_BMHD1_COPY) |
| AF40 $1400_H$ - AF40 $15FF_H$ | 512 Byte | UCB10 (UCB_BMHD2_COPY) |
| AF40 $1600_H$ - AF40 $17FF_H$ | 512 Byte | UCB11 (UCB_BMHD3_COPY) |

/0_Src/AppSw/Tricore/Cfg_Ssw/Ifx_Cfg_SswBmhd.c

```
49 const Ifx_Ssw_Bmhd bmhd_0_orig=
50 {
51   0x00FE,      /**< \brief 0x000: .bmi: Boot
52   0xB359,      /**< \brief 0x002: .bmhdid: B
53   0xA0000000,    /**< \brief 0x004: .stad: U
54   0x31795570,    /**< \brief 0x008: .crc: Ch
55   0xCE86AA8F,    /**< \brief 0x00C: .crcInv:
56   {
57     0x00000000, 0x00000000, 0x00000000, 0x0
58     0x00000000, 0x00000000, 0x00000000, 0x0
```

## Generated Hex file

```
AF400000    B359000E A0000000 794D052D 86B2FAD2
AF400010    00000000 00000000 00000000 00000000
AF400020    00000000 00000000 00000000 00000000
AF4001B0    00000000 00000000 00000000 00000000
AF4001C0    00000000 00000000 00000000 00000000
AF4001D0    00000000 00000000 00000000 00000000
AF4001E0    00000000 00000000 00000000 00000000
AF4001F0    43211234
```

# BMI configuration

| Field Name | Subfield | Description |
|---|---|---|
| BMI | Boot Mode Index - 16 bit | |
| | PINDIS<br>bit [0] | Mode selection by configuration pins:<br>0B Mode selection by HWCFG pins is enabled<br>1BMode selection by HWCFG pins is disabled |
| | HWCFG<br>bits [3:1] | Start-up mode selection:<br>111B Internal start from Flash<br>110BAlternate Boot Mode (ABM)<br>100B Generic Bootstrap Loader Mode (ASC/CAN BSL)<br>011BASC Bootstrap Loader Mode (ASC BSL)<br>elseinvalid |
| | LSENA0<br>bit [4] | Lockstep monitoring control by SSW for CPU0:<br>0B Lockstep monitoring for CPU0 is disabled<br>1BLockstep monitoring for CPU0 is enabled |
| | LSENA1<br>bit [5] | Lockstep monitoring control by SSW for CPU1: 1)<br>0B Lockstep monitoring for CPU1 is disabled<br>1BLockstep monitoring for CPU1 is enabled |
| | LSENA2<br>bit [6] | Lockstep monitoring control by SSW for CPU2: 1)<br>0B Lockstep monitoring for CPU2 is disabled<br>1BLockstep monitoring for CPU2 is enabled |
| | LSENA3<br>bit [7] | Lockstep monitoring control by SSW for CPU3: 1)<br>0B Lockstep monitoring for CPU3 is disabled<br>1BLockstep monitoring for CPU3 is enabled |
| | LBISTENA<br>bit [8] | LBIST execution start by SSW:<br>0B LBIST execution start by SSW is disabled<br>1BLBIST execution start by SSW is enabled |
| | CHSWENA<br>bits [11:9] | Checker Software (CHSW) execution after SSW: 2)<br>$101_B$ CHSW execution after SSW is disabled<br>else CHSW execution after SSW is enabled |
| | reserved<br>bits [15:12] | Reserved for future extensions, must be configured to 0 in UCB_BMHDx |

## Examples:

- Internal start from Flash (HWCFG enabled)

```
const Ifx_Ssw_Bmhd bmhd_0_orig=
{
    0x00FE,          /**< \brief
    0xB359,          /**< \brief
    0xA0000000,      /**< \brief
    0x31795570,      /**< \brief
    0xCE86AA8F,      /**< \brief
```

- Generic bootloader (HWCFG disabled)

```
    0x0009,      /**<
    0xB359,      /**<
    0xA0000000,
    0xCB6DD93D,
    0x349226c2,
```

# Special Notes - 1

- The BMHD installation is dependent on the confirmation states of UCB_BMHDx_ORIG and UCB_BMHDx_COPY. If the confirmation code of both ORIG and COPY is **ERRORED**, SSW does not evaluate the UCB!

**Table 183 UCB States**

| State | Value | Description |
|---|---|---|
| UNLOCKED | $4321\ 1234_H$ | **Delivery State**<br>The UCB confirmation code is programmed with the UNLOCKED value. |
| CONFIRMED | $57B5\ 327F_H$ | **Operational State**<br>The UCB confirmation code is programmed with the CONFIRMED value.<br>*Note: The UNLOCKED value can be over programmed with the CONFIRMED value.* |
| ERASED | $0000\ 0000_H$ | **Erased State**<br>Behavior as for the ERRORED state. |
| ERRORED | Others | **Errored State**<br>The UCB confirmation code stored is not the CONFIRMED or UNLOCKED value. |

# Special Notes - 2

- The following table shows the evaluation sequence of ORIG & COPY. In order to make BMHD_1_ORIG to be evaluated, user application must take care both BMHD_0_ORIG & BMHD_0_COPY.

**Table 184 Boot Mode Header 0 Installation**

| UCB_BMHD0_ORIG Confirmation State | UCB_BMHD0_COPY Confirmation State | Boot Mode Header Installation |
|---|---|---|
| UNREAD | Don't Care | No evaluation. |
| **UNLOCKED** | Don't Care | SSW evaluates UCB_BMHD0_ORIG.<br>Password installed from UCB_BMHD0_ORIG. |
| **CONFIRMED** | Don't Care | SSW evaluates UCB_BMHD0_ORIG.<br>Password installed from UCB_BMHD0_ORIG. |
| **ERRORED** | **UNLOCKED** | SSW evaluates UCB_BMHD0_COPY.<br>Password installed from UCB_BMHD0_COPY. |
| **ERRORED** | **CONFIRMED** | SSW evaluates UCB_BMHD0_COPY.<br>Password installed from UCB_BMHD0_COPY. |
| **ERRORED** | **ERRORED** | No evaluation.<br>No Password installed. |

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