|  |  |  |  |
| --- | --- | --- | --- |
| Clk | In | 1 |  |
| Reset | In | 1 |  |
| Coef\_valid | Out | 1 | The valid signal of the output coef |
| Coef | Out | Radius\*depth\*DW\*freq |  |
| Axi4\_bus | Slave |  | Transmit the coef data into the internal memory; |

Memory model: 6个频率对应6个bank。每个bank输出coef到RsdKernelGen。

F6

F5

F4

F1

F2

F3

(6是虚指)，bank、row、col的设置应该是2的幂次。32 bit地址的低 （log2(bank)+log2(row)+log2(col)）位代表了内部寄存器组的地址。

地址为32’bffff\_ffff时，coef\_valid有效。