Review Notes for Computer Architecture

Yi Gu

December 25, 2019

- $\text{CPI} = \dfrac{\text{CPU Time} \times \text{Clock Rate}}{\text{Instrution Count}} = \dfrac{\text{Cycles}}{\text{Instrution Count}}$
- $\text{CPI} = \text{Cycle Time} \times \sum_{j=1}^{n} \text{CPI}_j \times I_j$
- $\text{CPI} = \sum_{j=1}^{n} \text{CPI}_j \times F_j$, where $F_j = \dfrac{I_j}{\text{Instrution Count}}$
- $\text{CPI}_{\text{Pipelined}} = \text{Ideal CPI} + \text{Average Stall cycles per Inst}$
- $\text{Speedup} = \dfrac{\text{Ideal CPI} \times \text{Pipeline depth}}{\text{Ideal CPI} + \text{Pipeline stall CPI}} \times \dfrac{\text{Cycle Time}_{\text{unpipelined}}}{\text{Cycle Time}_{\text{pipelined}}}$
- If ideal CPI is 1, then $\text{Speedup} = \dfrac{\text{Pipeline depth}}{1 + \text{Pipeline stall CPI}} \times \dfrac{\text{Cycle Time}_{\text{unpipelined}}}{\text{Cycle Time}_{\text{pipelined}}}$
- Temporal Locality (time), Spatial Locality (space)
- Compulsory Misses (cold start), Capacity Misses, Conflict Misses
- Write Through, Write back
- synonym/alias (two va, same pa)
- $\text{CPU time} = \text{IC} \times \left(\text{CPI}_{\text{Execution}} + \dfrac{\text{Mem Access}}{\text{Inst}} \times \text{Miss Rate} \times \text{Miss Penalty} \right) \text{Cycle Time}$
- $\text{CPU time} = \text{IC} \times \left(\dfrac{\text{AluOps}}{\text{Inst}} \times \text{CPI}_{\text{AluOps}} + \dfrac{\text{Mem Access}}{\text{Inst}} \times \text{AMAT} \right) \times \text{Cycle Time}$
- $\text{AMAT} = \text{Hit Time} + \text{Miss Rate} \times \text{Miss Penalty}$
- Reduce Miss Rate: larger block size, higher associativity, victim cache, pseudo-associativity, hardware prefetching, softerware prefetching, compiler optimizations
- Reduce Miss Penalty: read priority over write, early restart and critical word first, non-blocking cache, second-level cache
- Reduce Hit Time: small and simple cache, avoid address translation, pipeline cache
- Structural hazard, Data hazard (RAW, WAR, WAW), Control hazard
- HW (Tomasulo) vs. SW (VLIW) Speculation -> P115