Hi3137 V100

Data Sheet

Issue 01

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Contents

About This Document

Purpose

This document describes the main features, logic architecture, and hardware design of the terrestrial digital TV channel processor chip Hi3137 V100 to facilitate use and design.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3137	V100

Intended Audience

This document is intended for:

- Design and maintenance personnel
- Sales personnel

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Alerts you to a high risk hazard that could, if not avoided, result in serious injury or death.
 WARNING	Alerts you to a medium or low risk hazard that could, if not avoided, result in moderate or minor injury.

Symbol	Description
CAUTION	Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results.
TIP	Provides a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points in the main text.

Register Attributes

The register attributions that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000

Type	Symbol	Value
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Others

Frequencies in this document all comply with the SDH standard. The shortened frequency names and the corresponding nominal frequencies are as follows.

Shortened Frequency Name	Nominal Frequency
19 M	19.44 MHz
38 M	38.88 MHz
77 M	77.76 MHz
622 M	622.08 MHz

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 01 (2014-09-26)

This issue is the first official release, which incorporates the following changes:

Modifications are made in section 1.2.1 to support DVB-T 1.6.1.

The name of section 1.2.2 is changed.

Issue 00B01 (2014-01-30)

This issue is the first draft release.

Contents

Figures

1 Overview

1.1 Introduction

Hi3137 V100 is a terrestrial digital TV channel receiver chip that supports the DVB-T and DVB-T2 modes. Complying with the DVB-T2 (ETS 302 755) and DVB-T (ETS 300 744) standards, it provides the high-performance multi-carrier demodulation capability and forward error correction function to implement full processing from baseband sampling on terrestrial digital signals to MPEG TS output. Hi3137 V100 ensures signal sampling precision by using the integrated 12-bit high-performance analog-to-digital converter (ADC). After baseband sampling, all the signals are processed in the digital domain. The chip provides all required functions based on the complex channel situations, such as demodulation, channel estimation and equalization, Viterbi, Reed-Solomon (RS), low-density parity check (LDPC), and Bose-Chaudhuri-Hocquenghem (BCH) forward error correction (FEC). It also monitors the signal strength and quality to facilitate program searching and storage.

1.2 Main Features

1.2.1 Modulation

- DVB-T and DVB-T2 modes, automatic recognition
- Standard DVB-T2 V1.3.1 and DVB-T V1.6.1
- DVB-T2 Base and Lite modes
- 5 MHz, 6 MHz, 7 MHz, 8 MHz, and 1.7 MHz input bandwidth
- Single physical layer pipe (PLP) and Multi PLP services and SISO and MISO transmission support for DVB-T2
- Automatic combination of common PLP and data PLP in DVB-T2 mode
- TSs and general streams (GSs) support for DVB-T2, adapting to data services
- All parameter modes support for DVB-T, including layered transmission and non-layered transmission

1.2.1 RX Performance

- Compliant with various test standards, including DTG7.0, NorDig-Unified Test Specification V2.2.1, and Digital Europe Ebook
- Low intermediate frequency (IF) and high IF (36 MHz) signal inputs

- Rapid signal capturing capability (less than 250 ms for DVB-T signals and less than 500 ms for DVB-T2 signals), reducing the wait time for switching the channel
- Superior Gaussian, multipath, and mobile reception performance
- Superior anti-interference (from the same frequency) performance
- Adaptive spectrum reverse recognition
- Frequency error detecting range broader than [–700 kHz, +700 kHz]

1.2.2 System

- Integrated 12-bit high-performance ADC for supporting highly precise sampling
- Integrated phase-locked loop (PLL), external passive crystal oscillator, 10−30 MHz (24 MHz typically), ±100 ppm frequency error
- Real-time monitoring of the signal strength, signal quality, and bit error rate
- Simple external circuits, 2-layer PCB routing, low BOM costs

1.2.3 Interfaces

- I^2C bus protocol support for flexibly controlling chipsets
- Tuner I^2C bus trunk
- TS outputs in configurable serial or parallel mode to work with the decoding chipset
- Configurable TS output pin for facilitating PCB routing

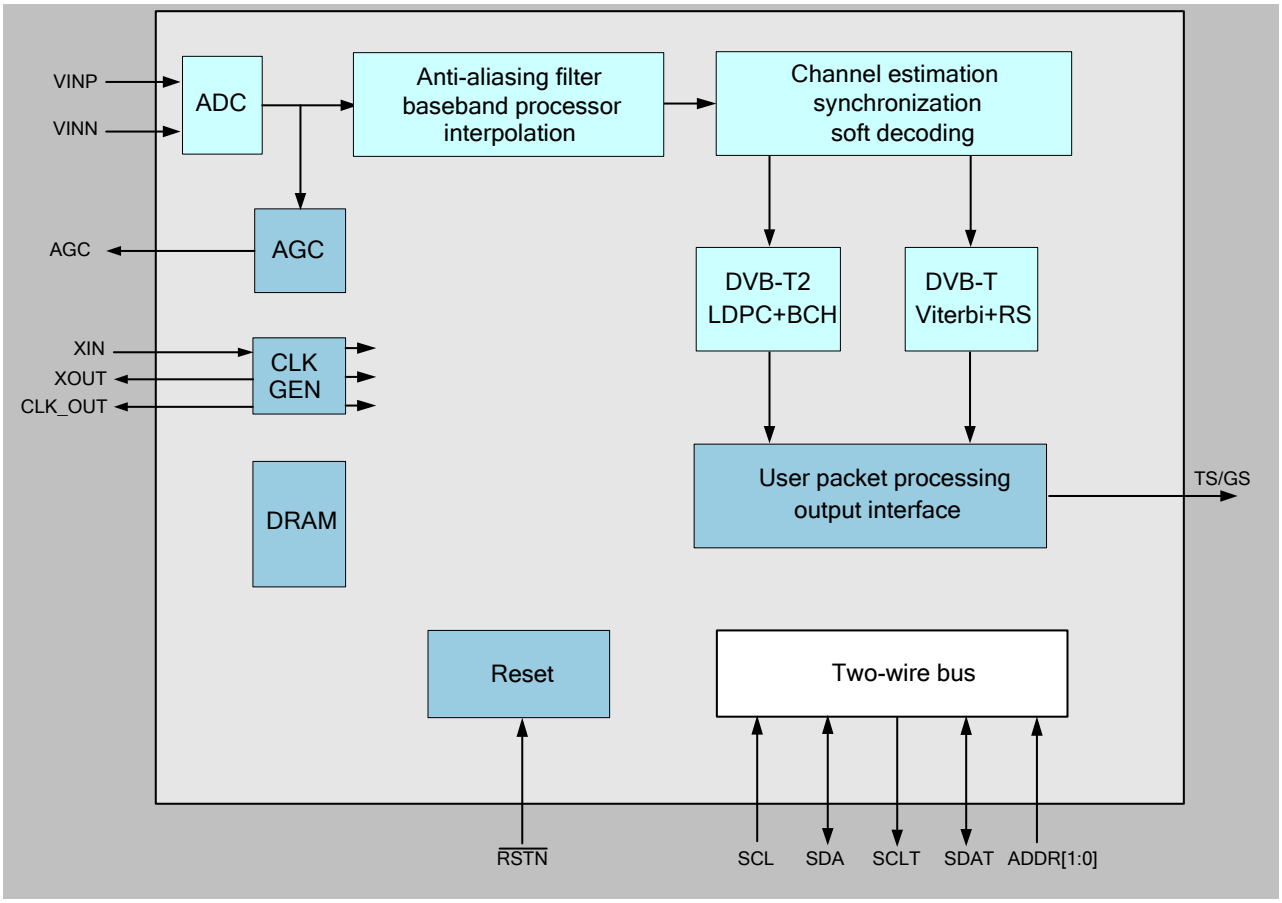
1.2.4 Process

- 1.1 V core power supply, 3.3 V I/O power supply, and maximum power consumption of 490 mW
- Micro-coax quad-flat no-leads 48 (MQFN48), body size of 6 mm x 6 mm (0.24 in. x 0.24 in.), RoHS compliance

1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of Hi3137 V100.

Figure 1-1 Functional block diagram of Hi3137 V100



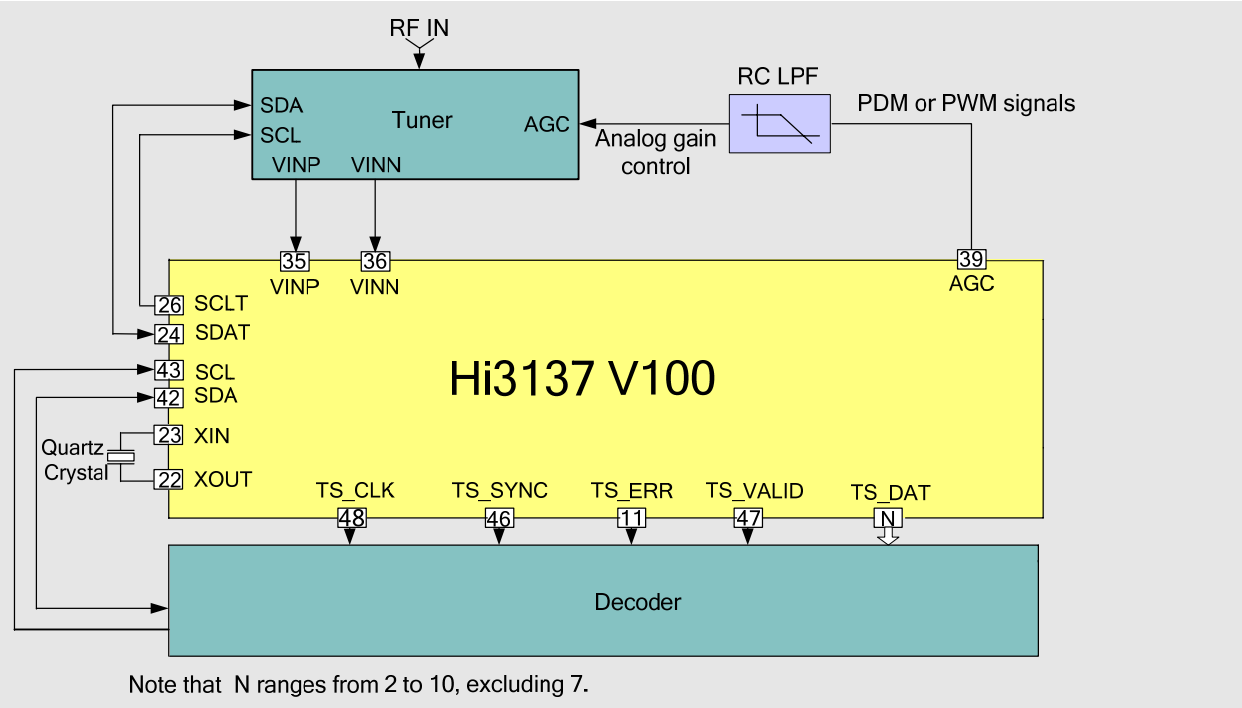
1.4 Application Scope

- Terrestrial digital signal tuner
- Terrestrial digital STB and integrated digital TV
- Modem and digital TV card

1.5 Typical Application

Figure 1-2 shows the typical front-end receiving application.

Figure 1-2 Typical front-end receiving application



Contents

Figures

Tables

2 Demod

2.1 Clock

The Demod input clock is derived from an external crystal oscillator or external clock. After being processed by the internal PLL, the working clock frequency for the Demod is obtained. The Demod has four internal clock domains. The ADC works at the CLK_ADC clock domain, the demodulation part works at the CLK_DEMO clock domain, the DRAM controller works at the CLK_SDC clock domain, and the channel decoding and TS output part works at the CLK_FEC clock domain. Figure 2-1 shows the internal clock domains of the Demod.

Figure 2-1 Internal clock domains of the Demod

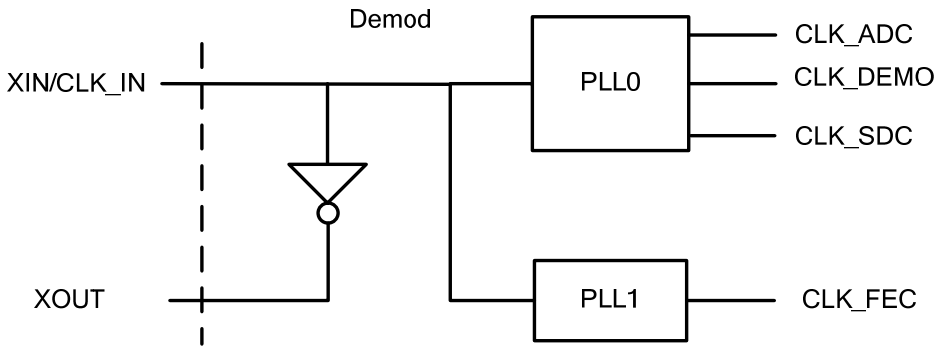


Table 2-1 describes the clock domain of other main modules.

Table 2-1 Clock domain of other main modules

Module	Clock Domain
I^2C	After power-on, the I^2C module works under a crystal oscillator clock or an external clock. After the internal PLLs are stable, the clock domain can be switched to CLK_DEMO to accelerate I^2C communication. The I^2C communication rate can be 100 kbit/s or 400 kbit/s.

The PLL0 output frequency can be set by performing the following I²C operations:

Step 1 Set ADC_CTRL1[i2c_xo_clk] to **0** to switch the I²C clock to the crystal oscillator clock or external clock. (If Hi3137 V100 starts to work after power-on reset, the I²C module works under a crystal oscillator clock or an external clock by default.)

Step 2 Set PLL0_PD[pll0_pd] to **1** to disable PLL0.

Step 3 Set parameters of PLL0.

```
FVCO0= FREF/refdiv[5:0]* (fbdiv[7:0]+frac[11:0]/2^12)
FOUT0= FVCO0/postdiv1[2:0]/postdiv2[2:0]
CLK_DEMO = FOUT0/6
CLK_ADC = FOUT0/12
CLK_SDC = FOUT0/4
```

where

- **FREF** is the frequency of the external crystal oscillator or clock. It ranges from 10 MHz to 30 MHz, and its default value is 24 MHz.
- **refdiv** is set by configuring PLL0_REFDIV[pll0_refdiv] and **fbdiv** is set by configuring PLL0_FBDIV[pll0_fbdiv].
- **frac** is set by configuring PLL0_FRAC_L[pll0_frac_l] and PLL0_PD[pll0_frac_h].
- **postdiv1** must be greater than or equal to **postdiv2**. For PLL0, **postdiv1** is **2** and is set by configuring PLL0_POSTDIV[pll0_postdiv1]; **postdiv2** is **1** and is set by configuring PLL0_POSTDIV[pll0_postdiv2].
- **FVCO0** is the VCO frequency of PLL0. It is recommended that **FVCO0** be greater than 600 MHz.
- **FOUT0** is the output frequency of PLL0.
- For details about other parameters, see the descriptions of PLL0 registers.

With the typical 24 MHz crystal oscillator input, the working frequencies of CLK_DEMO, CLK_ADC, and CLK_SDC are 64 MHz, 32 MHz, and 96 MHz respectively based on the default configuration.

Step 4 Set PLL0_PD[pll0_pd] to **0** to enable PLL0.

Step 5 Wait for the PLL_LOCK [pll0_lock] indicator. The value **1** indicates that PLL0 is locked. The wait time is less than 1 ms.

Step 6 Set ADC_CTRL1[i2c_xo_clk] to 1 to switch the I²C clock to CLK_DEMO.

Step 7 Write 0 and then 1 to RSTN_CTRL[hot_rst_n] to perform a hot reset on Hi3137 V100.

----End

The PLL1 output frequency can be set by performing the following I²C operations:

Step 1 Set PLL1_PD[pll1_pd] to **1** to disable PLL1.

Step 2 Set parameters of PLL1.

```
FVCO1=FREF /refdiv[5:0]* (fbdiv[7:0]+frac[11:0]/2^12)
FOUT1= FVCO1/postdiv1[2:0]/postdiv2[2:0]
CLK_FEC = FOUT1
```

where

- **FREF** is the frequency of the external crystal oscillator clock. It ranges from 10 MHz to 30 MHz, and its default value is 24 MHz.
- **refdiv** is set by configuring PLL1_REFDIV[pll1_refdiv] and **fbdiv** is set by configuring PLL1_FBDIV[pll1_fbdiv].
- **frac** is set by configuring PLL1_FRAC_L[pll1_frac_l] and PLL1_PD[pll1_frac_h].
- **postdiv1** must be greater than or equal to **postdiv2**. For PLL1, **postdiv1** is **2** and is set by configuring PLL1_POSTDIV[pll1_postdiv1]; **postdiv2** is **2** and is set by configuring PLL1_POSTDIV[pll1_postdiv2].
- **FVCO1** is the VCO frequency of PLL1. It is recommended that **FVCO1** be greater than 600 MHz.
- **FOUT1** is the output frequency of PLL1.
- For details about other parameters, see the descriptions of PLL1 registers.

With the typical 24 MHz crystal oscillator input, the working frequency of CLK_FEC is 153 MHz based on the default configuration.

Step 3 Set PLL1_PD[pll1_pd] to **0** to enable PLL1.

Step 4 Wait for the PLL_LOCK [pll1_lock] indicator. The value **1** indicates that PLL1 is locked. The wait time is less than 1 ms.

Step 5 Write 0 and then 1 to RSTN_CTRL[hot_rst_n] to perform a hot reset on Hi3137 V100.

----End

NOTE

You can set the CLK_DEMO and CLK_FEC frequencies after switching the I^2C clock to the crystal oscillator clock. The frequencies of PLLx input and output clocks and internal clocks must fall within the value ranges described in Table 2-3. The value of *x* in PLL*x* or FVOC*x* is 0 or 1.

Table 2-2 Frequency ranges of PLL input and output clocks and internal clocks

Clock	Frequency Range (MHz)
FREF	10–30
FVCOx	> 600
CLK_DEMO	≤ 65
CLK_FEC	≤ 160

The Demod also provides the loopback clock CLK_OUT (PIN_19) of the crystal oscillator clock or external clock for other chips such as the MPEG decoding chip. In this case, IO_CTRL4[clkout_sel] must be set to **0**.

2.2 Reset

Reset operations are classified into hard reset and soft reset.

- The external RSTN pin is used for power-on reset or hard reset on the Demod by the master chip. When a hard reset is performed, all registers are reset.
- By using the I^{2}C module, internal registers can be reset by a cold reset (cool_rst_n) or hot reset (hot_rst_n) as follows:
  - Cold reset: Write **0** and then **1** to RSTN_CTRL[cool_rst_n]. When a cold reset is performed, all registers are reset, which is the same as a hard reset.
  - Hot reset: Write **0** and then **1** to RSTN_CTRL[hot_rst_n]. When a hot reset is performed, only the logic is reset and register values are retained.

2.3 I^{2}C Controller

The I^{2}C controller on the Demod acts as an I^{2}C slave. The I^{2}C controller reads or writes to the internal configuration register of the Demod over I^{2}C communication and forwards I^{2}C communication for the tuner.

As a slave component, the Demod supports all I^{2}C operations initiated by the master chip. The Demod component address is expressed by an 8-bit binary number 10110XXY. XX is specified by setting ADDR bit[1:0] and Y is used to specify the operation type. The value 1 indicates read and the value 0 indicates write. Figure 2-2 shows the I^{2}C read timing, and Figure 2-3 shows the I^{2}C write timing.

Figure 2-2 I^{2}C read timing

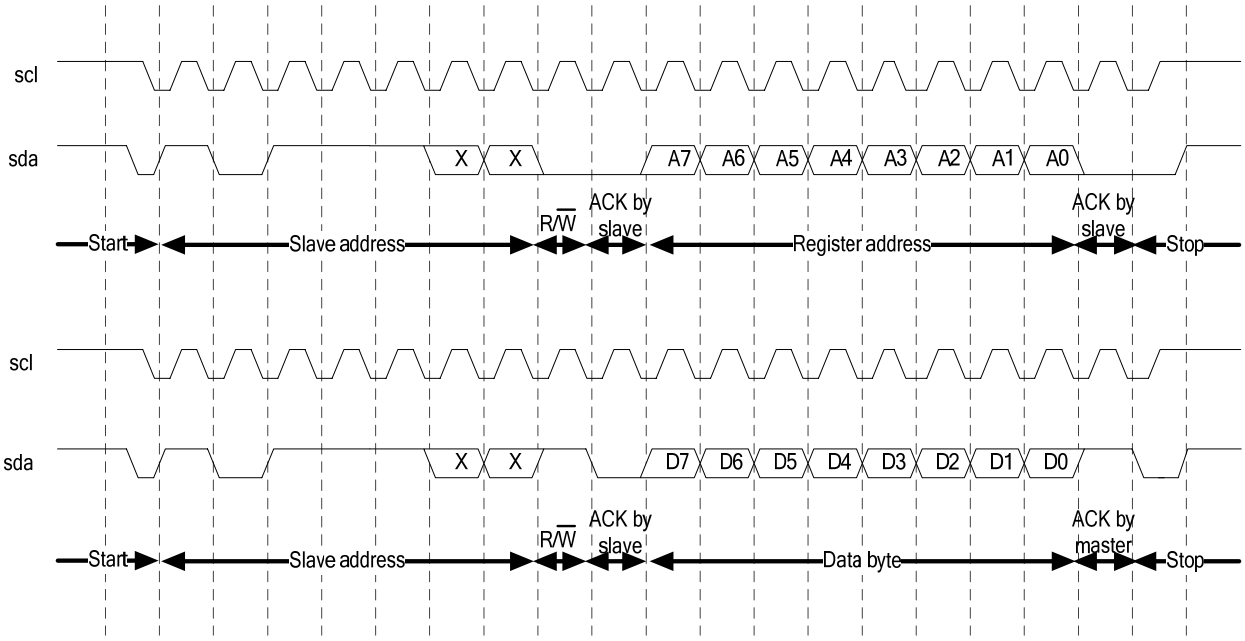
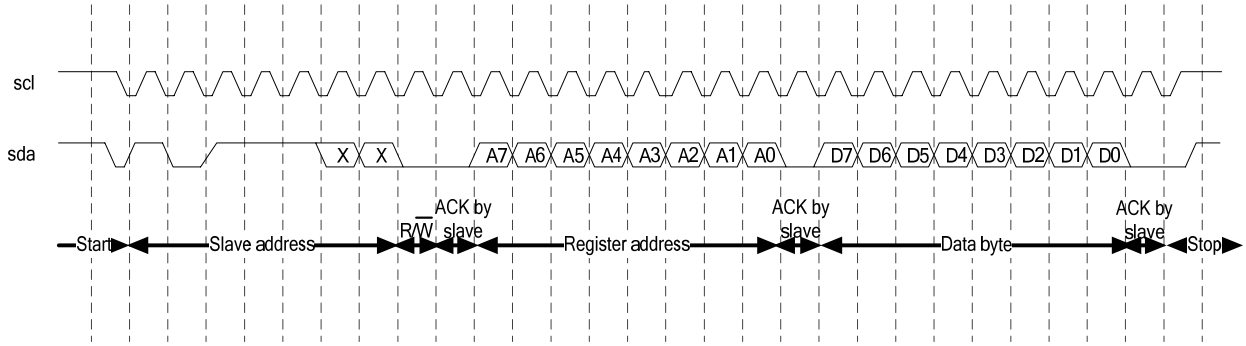


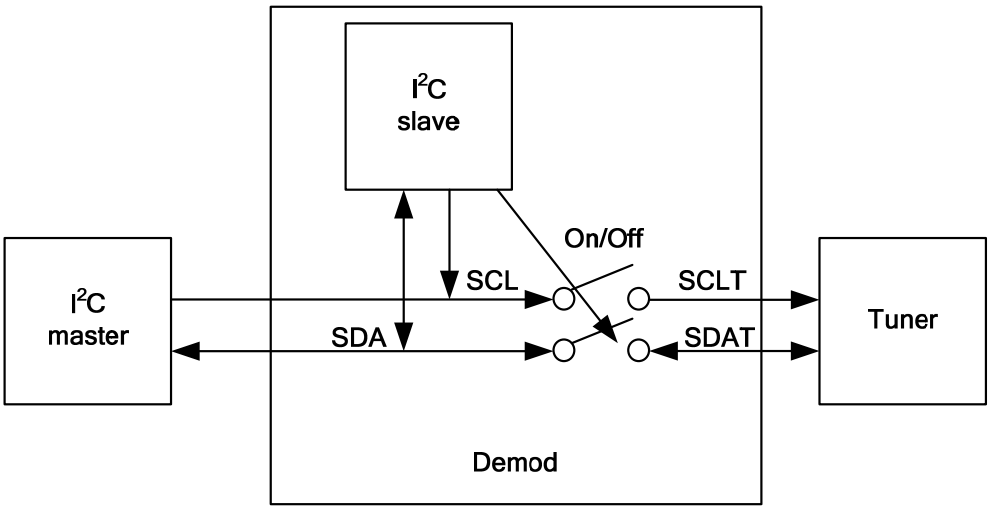
Figure 2-3 I²C write timing



The I²C controller can consecutively read or write to multiple registers by working with software. For the tuner, the Demod can forward I²C communication. That is, the master chip can access the tuner in the same way that it accesses the Demod when the I²C path between the master chip and the tuner is enabled. Each time after an I²C read or write operation is complete, the Demod automatically disables forwarding to prevent interference to the tuner from the I²C module. For details about I²C addresses for the tuner, see the corresponding tuner user manuals.

Figure 2-4 shows the I²C forwarding schematic diagram.

Figure 2-4 I²C forwarding schematic diagram



For details about how to enable I²C forwarding, see the description of TUNER_SEL[tuner_sel].

2.4 ADC

The Demod integrates a high-performance 12-bit ADC on-chip for sampling the low IF or IF (36 MHz) signals output by the front-end tuner. The actual sampling clock frequency can be changed by setting the CLK_ADC frequency, which is 65 MHz at the maximum. The ADC

supports differential or single-end inputs, and the peak-to-peak voltage at full scale is 1 V. The sampling clock edge is selected by configuring the most significant bit (MSB) of ADC_CTRL0[adc_clk_sel].

After the Demod is powered on and PLLs are configured, the ADC can be initialized by performing the following I^2C operations:

Step 1 Set the sampling rate based on the CLK_ADC frequency. Divide the CLK_ADC working frequency (Hz) by 1000 and write the value to CLK_ADC_L[clk_adc_l], CLK_ADC_M[clk_adc_m], and CLK_ADC_H[clk_adc_h]. For example, if the CLK_ADC frequency is 32 MHz, write **0x00** to CLK_ADC_L[clk_adc_l] and CLK_ADC_H[clk_adc_h], and write **0x7D** to CLK_ADC_M [clk_adc_m].

Step 2 Write **0** and then **1** to ADC_CTRL1[adi2c_resetz] to initialize the ADC.

Step 3 Set ADC_CTRL3[adc_opm] to **3** to enter the working mode.

Step 4 Wait until PLL0_REFDIV[adc_rdy] changes from low to high. The wait time is less than 1 ms. Then the ADC is initialized.

----End

2.5 AGC

The automatic gain control (AGC) module receives outputs from the ADC and generates AGC control signals based on the difference between the expected power and actual power. The AGC control signal can be the pulse-duration modulation (PDM) or pulse-width modulation (PWM) wave, which is set by configuring USE_PWM[use_pwm]. The PDM output is used by default. After resistor-capacitor (RC) filtering externally, the AGC control signal is transmitted to the tuner to adjust the tuner output amplitude to the expected value. The clock frequency of the AGC control signal is adjusted by configuring AGC_CTRL[pdm_div], and the output polarity is set by configuring AGC_CTRL[agc_inverse].

- The expected AGC power can be set by configuring AGC_GOAL[agc_goal].
- The AGC adjustment speed can be set by configuring AGC_SPEED_BOUND[agc_speed].

Table 2-3 describes AGC signal clock frequencies.

Table 2-3 AGC signal clock frequencies

pdm_div[2:0]	AGC Signal Clock Frequency
b'000	CLK_ADC
b'001	CLK_ADC/2
b'010	CLK_ADC/4
b'011	CLK_ADC/8
b'100	CLK_ADC/16
b'101	CLK_ADC/32
b'110	CLK_ADC/64

pdm_div[2:0]	AGC Signal Clock Frequency
b'111	CLK_ADC/128

2.6 Clock Recovery

The clock recovery module recovers a clock with the same symbol rate as that at the TX end and sampling data in the accurate clock phase.

To ensure that the clock recovery module works properly, the Demod needs to write the CLK_DEMO frequency value f_{clk_demo} over the I^2C. f_{clk_demo} is an 18-bit unsigned number. Its least significant bit (LSB) indicates 1 kHz. For details, see the descriptions of the CLK_DEMO_L, CLK_DEMO_M, and RSTN_CTRL[clk_dem_h] registers. The Demod also needs to configure the input signal bandwidth over the I^2C. For details, see the description of BAND_WIDTH[bw].

Table 2-4 bw[2:0], input signal bandwidth, and symbol rate

bw[2:0]	Input Signal Bandwidth	Symbol Rate fs (kHz)
b'000	1700	1845
b'001	5000	5714
b'010	6000	6857
b'011	7000	8000
b'100	8000	9143

2.7 Carrier Recovery

The carrier recovery module traces and compensates the frequency offset and phase offset of the carrier.

To ensure that the carrier recovery module works properly, the Demod needs to write the center frequency value of the tuner output signal (f_{IF}) over the I^2C. f_{IF} is a 16-bit unsigned number. Its LSB indicates 1 kHz. For details, see the descriptions of the IF_FREQ_L and IF_FREQ_H registers.

2.8 Frame Synchronization

DVB-T2/DVB-T signals are arranged by frame. Therefore, the start position of frames must be accurately defined and the optimal position must be traced in real time. The frame synchronization module implements this function and supports rapid synchronization in an

environment with an extremely low signal-to-noise ratio (SNR), multipath channels, or analog interference from the same frequency.

2.9 Channel Estimation and Equalization

The channel estimation and equalization module estimates channel features and equalizes modulation data by using the pilot frequency inserted in the DVBT/T2 signal frequency domain data. The Demod uses the high-performance channel estimation algorithm, which increases the estimation accuracy.

2.10 DVB-T2 FEC

This module performs the following operations:

Step 1 Deinterleave and demap symbols and transmit the generated software information to the bit deinterleaver.

Step 2 Store the deinterleaved data to the RAM and implement LDPC decoding. The LDPC decoder supports the long frame and short frame modes, as well as all bit rates in the DVB-T2 standard.

Step 3 Transmit the decoded data to the BCH module for BCH decoding.

----End

2.11 DVB-T FEC

This module performs the following operations:

Step 1 Deinterleave symbols.

Step 2 Perform depuncturing, demapping, and bit deinterleaving operations.

Step 3 Perform Viterbi decoding. The supported code rates include 1/2, 2/3, 3/4, 5/6, and 7/8.

Step 4 Perform DVB-T convolutional deinterleaving.

Step 5 Transmit deinterleaved data to the RS decoder for channel error correction. The DVB-T output packet length is 188 bytes.

----End

2.12 TS Output

The Demod supports three TS output modes: parallel mode, 1-bit serial mode, and 2-bit serial mode.

The signals from the TS output interface include the data signal TS_OUT[7:0], clock signal TS_CLK, data validity signal TS_VLD, sync header signal TS_SYNC, and packet error signal TS_ERR.

- TS_OUT: TS frame data. This signal is 8 bits in parallel mode, 1 bit in 1-bit serial mode, and 2 bits in 2-bit serial mode.
- TS_CLK: data clock. The clock edge is configurable. The clock frequency output varies according to the TS speed.
- TS_VLD: TS packet data validity indicator (byte valid in parallel mode or bit valid in serial mode).
- TS_SYNC: TS packet sync header indicator (byte valid in parallel mode or bit valid in serial mode).
- TS_ERR: TS packet error indicator. It is set to **1** if an error occurs in the current TS packet.

The TS output mode is set by configuring OUTP_TS_MODE[paral] and OUTP_TS_MODE[serl2]. See Table 2-5.

Table 2-5 TS output modes

para l	serl2	TS Output Mode	Maximum TS_CLK Frequency (MHz)	Maximum TS Bit Rate (Mbit/s)
1	0	Parallel	9	72
0	1	2-bit serial	36	72
0	0	1-bit serial	76.5	72

Figure 2-5 shows the timing in TS parallel output mode.

Figure 2-5 Timing in TS parallel output mode

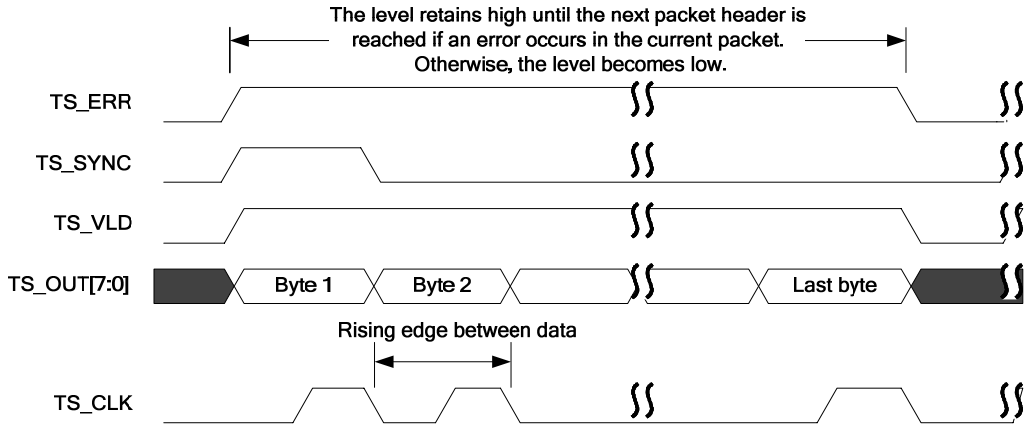
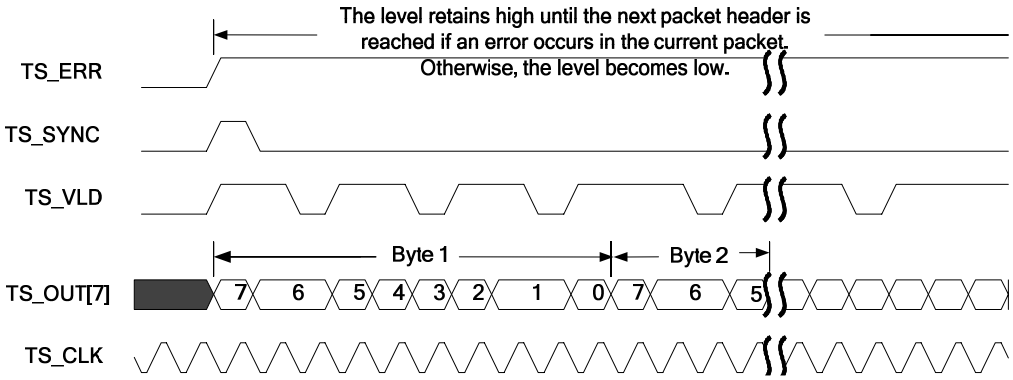


Figure 2-6 shows the timing in 1-bit TS serial output mode.

Figure 2-6 Timing in 1-bit TS serial output mode

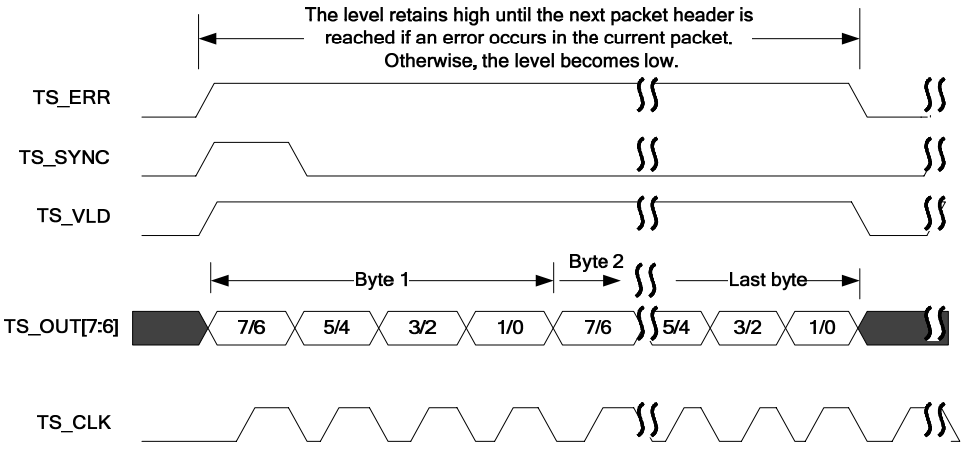


NOTE

In 1-bit serial output mode, TS_CLK works at the CLK_FEC frequency divided by 2. You can mask invalid bits by setting the TS_VLD level to low, or mask TS-CLK when the TS_VLD level is low by setting OUTP_TS_MODE[mask_clk] to **1**. In Figure 2-6, upper bits are output first. You can enable lower bits to output first by writing **0** to OUTP_TS_MODE[msb_first]. TS_OUT can be mapped to any pin of TS_OUT[7:0]. For details, see the following sections.

Figure 2-7 shows the timing in 2-bit TS serial output mode.

Figure 2-7 Timing in 2-bit TS serial output mode



NOTE

In 2-bit serial output mode, TS_OUT can be mapped to any two pins of TS_OUT[7:0].

In parallel output mode or 2-bit serial output mode, the TS_CLK clock edge is selected by configuring OUTP_TS_MODE[clk_inv]. If OUTP_TS_MODE[clk_inv] is **0**, the rising edge is between TS data. If OUTP_TS_MODE[clk_inv] is **1**, the falling edge is between data.

In 1-bit serial output mode, the TS_CLK clock edge is selected by configuring OUTP_TS_MODE[clk_inv]. If OUTP_TS_MODE[clk_inv] is **0**, the rising edge is selected. If OUTP_TS_MODE[clk_inv] is **1**, the falling edge is selected.

In parallel mode or 2-bit serial mode, the Demod automatically generates even TS_CLK signals based on the CLK_FEC frequency, bandwidth, bit rate, and modulation mode. You can also specify a fixed frequency-division signal of CLK_FEC as the TS_CLK signal as follows:

Step 1 Set OUTP_CLK_SET[clk_div], OUTP_CLK_SETH[clk_div_fh], and OUTP_CLK_SETL[clk_div_fl] to determine the frequency divider for the system clock. clk_div[5:0] is the integral part of the frequency divider and ranges from 1 to 63. clk_div_f[15:0] is the decimal part of the frequency divider. It is calculated as follows: clk_div_f = clk_div_fh x 256 + clk_div_fl. The actual frequency divider is calculated as follows: Frequency divider = clk_div[5:0] + clk_div_f[15:0]/65536.

Step 2 Set OUTP_MODE_SET[out_mode] and OUTP_CLK_SET[clk_mode] to 1 to switch TS_CLK to the configured frequency.

CAUTION

Ensure that the maximum TS rate (72 Mbit/s) is supported at the configured TS_CLK frequency.

The TS pin outputs are selected by using the following control signals. In Table 2-6, the value of *x* in ts_*x*_sel is a or 0–9.

Table 2-6 Mapping between the control signal ts_*x*_sel and the controlled external pin

Control Signal	Register	Controlled External Pin
ts_0_ sel	TS_0_SEL	TS_OUT0
ts_1_ sel	TS_21_SEL	TS_OUT1
ts_2_ sel	TS_21_SEL	TS_OUT2
ts_3_sel	TS_43_SEL	TS_OUT3
ts_4_ sel	TS_43_SEL	TS_OUT4
ts_5_ sel	TS_65_SEL	TS_OUT5
ts_ 6_sel	TS_65_SEL	TS_OUT6
ts_7_ sel	TS_87_SEL	TS_OUT7
ts_8_ sel	TS_87_SEL	TS_SYNC
ts_9_ sel	TS_A9_SEL	TS_VLD
ts_ a_sel	TS_A9_SEL	TS_ERR

Table 2-7 describes the mapping between the ts_*x*_sel value and the internal TS signal. The value of *x* in ts_*x*_sel is a or 0–9.

Table 2-7 Mapping between the ts_*x*_sel value and the internal TS signal

ts_x_sel	Internal TS signal
b'0000	ts_out[0]
b'0001	ts_out[1]
b'0010	ts_out[2]
b'0011	ts_out[3]
b'0100	ts_out[4]
b'0101	ts_out[5]
b'0110	ts_out[6]
b'0111	ts_out[7]
b'1000	ts_sync
b'1001	ts_vld
Others	ts_err

NOTE

- In 1-bit serial output mode, if the upper bits are output first, select the internal TS data signal ts_out[7]. If the lower bits are output first, select the internal TS data signal ts_out[0].
- In 2-bit serial output mode, if the upper bits are output first, select the internal TS data signal ts_out[7:6]. If the lower bits are output first, select the internal TS data signal ts_out[1:0].

----End

2.13 Signal Monitoring

Signal Strength

The Demod supports signal power statistics. The signal strength identifier can be obtained by reading AGC_CTRL_L[agc_ctrl_l] and then AGC_CTRL_H[agc_ctrl_h].

```
sig_strength = agc_ctrl_h[7:0]*16 + agc_ctrl_l[3:0]
```

A larger sig_strength value indicates weaker signal strength. The curve that shows the relationship between sig_strength and signal power varies according to the radio frequency (RF) chip.

Transmission Standard and Spectrum Inversion Recognition

The transmission standard is read as follows:

Step 1 Wait until LOCK_FLAG[fec_ok] is 1. The read information is correct only when LOCK_FLAG[fec_ok] is 1.

Step 2 Read CHN_FFT_GI[is_dvbt]. The value 1 indicates the DVB-T mode, and the value 0 indicates the DVB-T2 mode.

- DVB-T2

  Read CHN_FFT_GI[fft_size] in DVB-T2 mode to obtain the FFT mode. Read TPS[bw_ext] in DVB-T2 mode. The value 1 indicates that the bandwidth is extended, and the value 0 indicates that the bandwidth is not extended.

Table 2-8 Relationship between fft_size and the FFT mode

fft_size[2:0]	bw_ext	FFT and Bandwidth Mode
b'000	-	1K
b'001	-	2K
b'010	-	4K
b'011	0	8K, normal carrier mode
b'011	1	8K, extend carrier mode
b'100	0	16K, normal carrier mode
b'100	1	16K, extend carrier mode
b'101	0	32K, normal carrier mode
b'101	1	32K, extend carrier mode
b'110– b'111	-	Reserved

Read TPS[gi_mode] in DVB-T2 mode to obtain the guard interval mode.

Table 2-9 Relationship between gi_mode and the guard interval mode

gi_mode[2:0]	Guard Interval Mode
b'000	1/32
b'001	1/16
b'010	1/8
b'011	1/4
b'100	1/128
b'101	19/128
b'110	19/256
b'111	Reserved

Read P1_SIGNAL[p1_signal_s1] in DVB-T2 mode to obtain the S1 part of the P1 signaling.

Table 2-10 p1_signal_s1 description

p1_signal_s1[2:0]	Description
b'000	T2_SISO
b'001	T2_MISO
b'010	Non-T2 signal
b'011	T2_LITE_SISO
b'100	T2_LITE_MISO
b'101– b'111	Reserved

Read PP_VERSION[pilotpattern] in DVB-T2 mode to obtain the pilot pattern mode.

Table 2-11 Relationship between pilotpattern and pilot pattern mode

pilotpattern[3:0]	Pilot Pattern Mode
b'0000	PP1
b'0001	PP2
b'0010	PP3
b'0011	PP4
b'0100	PP5
b'0101	PP6
b'0110	PP7
b'0111	PP8
b'1000– b'1111	Reserved

Read CHN_FFT_GI[spectrum] in DVB-T2 mode. The value 1 indicates that the spectrum is inverted; the value 0 indicates that the spectrum is not inverted.

Read PLP_PARAM[plp_cod] and PLP_PARAM[plp_mod] in DVB-T2 mode to obtain the current PLP modulation mode and LDPC bit rate.

Read PLP_PARAM[plp_fec_type] in DVB-T2 mode to obtain the FEC frame mode of the current PLP. The value 1 indicates long frames (64K LDPC), and the value 0 indicates short frames (16K LDPC).

Table 2-12 Relationship between plp_mode and the modulation mode

plp_mod[2:0]	Modulation Mode
b'000	QPSK

b'001	16QAM
b'010	64QAM
b'011	256QAM
B'100– b'111	Reserved

Table 2-13 Relationship between plp_cod and the bit rate

plp_cod[2:0]	Bit Rate (T2_base)	Bit Rate (T2_lite)
b'000	1/2	1/2
b'001	3/5	3/5
b'010	2/3	2/3
b'011	3/4	3/4
b'100	4/5	Reserved
b'101	5/6	Reserved
b'110	Reserved	1/3
b'111	Reserved	2/5

NOTE

The relationship between plp_cod and the bit rate in Base mode is different from that in Lite mode. Therefore, you need to confirm whether the Base or Lite mode is used by reading P1_SIGNAL[p1_signal_s1] before determining the bit rate.

- DVB-T

  Read CHN_FFT_GI[fft_size] to obtain the FFT mode, and read TPS [gi_mode] to obtain the guard interval mode.

  Read CHN_FFT_GI[spectrum] in DVB-T mode. The value 1 indicates that the spectrum is inverted, and the value 0 indicates that the spectrum is not inverted.

  Read TPS_DVBT[mod], TPS_DVBT[hier], and TPS_DVBT[cod_rate_H] in DVB-T mode to obtain the modulation mode, hierarchical mode, and the internal bit rate of high-priority streams in hierarchical or non-hierarchical mode. Read CODE_RATE_DVBT[code_rate_L] to obtain the internal bit rate of low-priority streams in hierarchical mode.

Table 2-14 Relationship between mod and the modulation mode

mod[1:0]	Modulation Mode
b'00	QPSK
b'01	16QAM
b'10	64QAM

b'11	reserved

Table 2-15 Relationship between hier and the hierarchical mode

hier[1:0]	Hierarchical Mode
b'00	Non-hierarchical
b'01	Hierarchical, α = 1
b'10	Hierarchical, α = 2
b'11	Hierarchical, α = 4

Table 2-16 Relationship between cod_rate_H/code_rate_L and the bit rate

cod_rate_H or code_rate_L	Bit Rate
b'000	1/2
b'001	2/3
b'010	3/4
b'011	5/6
b'100	7/8
b'101~ b'111	reserved

----End

Symbol Rate Offset

The input signal bandwidth must be set before timing recovery. After the timing loop is stable, read TIM_OFFSET[tim_offset] from the Demod, and then read TIM_LOOP_L[tim_loop_l] and TIM_LOOP_H[tim_loop_h]. tim_offset and tim_loop_h are signed numbers, and the MSB is a signed bit. The offset between the actual symbol rate and fs is calculated as follows:

fs_offset = (tim_offset x 4 – (tim_loop_h x 256 + tim_loop_l)/16)/2^10 x fs

If the value of fs_offset is a positive signed number, the actual symbol rate is greater than the configured symbol rate. If the value of fs_offset is a negative signed number, the actual symbol rate is less than the configured symbol rate. For details about the value of fs, see Table 2-4. The fs_offset unit is kHz.

Note that the symbol rate offset is valid only when the offset is read after LOCK_FLAG[fec_ok] is 1.

Carrier Offset

After the carrier loop is stable, read CAR_OFFSET_L and then CAR_OFFSET_H from the Demod. The offset between the actual signal center frequency and the tuner center frequency can be calculated as follows:

freq_offset = (CAR_OFFSET_H x 256 + CAR_OFFSET_L)/2^8 x fs

If the value of freq_offset is a positive signed number, the actual carrier frequency is greater than the configured tuner frequency. If the value of freq_offset is a negative signed number, the actual carrier frequency is less than the configured tuner frequency. For details about the value of fs, see Table 2-4. The freq_offset unit is kHz.

Note that the carrier offset is valid only when the offset is read after LOCK_FLAG[fec_ok] is 1.

Signal Quality

Read the noise power statistics registers SNR_L[snr_l] and SNR_H[snr_h] from the Demod and convert the values into the SNR (ranges from 0 dB to 36 dB) as follows (The SNR is used to evaluate the signal quality):

SNR = 10.0 x log10(snr_h[7:0] x 256 + snr_l) – 11.7

CAUTION

The estimated SNR is accurate only when LOCK_FLAG [tps_ok_t] (for DVB-T) or LOCK_FLAG [sig_ok_t2] (for DVB-T2) is 1.

BER Statistics

The bit error rate (BER) before RS (for DVB-T) or BCH (for DVB-T2) correction can be calculated by using the Demod error bit count registers FEC_BER_L and FEC_BER_H.

Read FEC_BER_L and then FEC_BER_H, and calculate the error count error_cnt as follows: error_cnt = FEC_BER_H x 256 + FEC_BER_L. If the BER is high, the actual error bit count may be greater than the maximum value of the error bit count registers. In this case, the maximum value is retained, which results in a BER that is less than the actual error bit count.

In DVB-T mode, the BER before RS decoding is calculated as follows:

$$\text{BER} = \frac{error\_cnt}{8 \times 204 \times frams}$$

frams is the total frame count, which is set by configuring BER_CTRL[frame_num].

In DVB-T2 mode, the BER before BCH decoding is calculated as follows:

$$\text{BER} = \frac{error\_cnt}{N \times frams}$$

- *N* is the statistics reference length. The code length varies according to the frame length mode and code rate. For details, see Table 2-17.
- **frams** is the total frame count, which is set by configuring BER_CTRL[frame_num]. For details, see Table 2-18.

Table 2-17 Values of *N* in DVB-T2 mode

LDPC Bit Rate	Value of *N* for 64K LDPC	Value of *N* for 16K LDPC
1/3	N/A	5400
2/5	N/A	6480
1/2	32400	7200
3/5	38880	9720
2/3	43200	10800
3/4	48600	11880
4/5	51840	12600
5/6	54000	13320

Table 2-18 Relationship between BER_CTRL[frame_num] and frams

BER_CTRL [frame_num]	frams in DVB-T Mode	frams in DVB-T2 Mode	
		plp_fec_type = 1 Long FEC Frame	plp_fec_type = 0 Short FEC Frame
b'000	d'16	d'32	d'128
b'001	d'64	d'64	d'256
b'010	d'256	d'128	d'512
b'011	d'1024	d'256	d'1024
b'100	d'4096	d'512	d'2048
b'101	d'16384	d'1024	d'4096
b'110	d'65536	d'2048	d'8192
b'111	d'262144	d'4096	d'16384

In DVB-T mode, the BER after RS decoding is calculated as follows: BER = 32 x FER

For details about the frame error rate (FER), see the following section. The BER after RS decoding is an approximate value.

In DVB-T2 mode, the BER after BCH decoding is calculated as follows: BER = 27 x FER

For details about the FER, see the following section. The BER after BCH decoding is an approximate value.

FER Statistics

In FER statistics, the frame indicates an RS packet in DVB-T mode or a BCH packet in DVB-T2 mode.

Read FEC_FER_L and then FEC_FER_H. error_fram is calculated as follows: error_fram = FEC_FER_H x 256 + FEC_FER_L. For details about the relationship between the total frame count **frams** and BER_CTRL bit[6:4] in DVB-T/DVB-T2 mode, see the description in the BER statistics.

The FER is calculated as follows:

FER = error_fram/frams

2.14 Signal Search

After the frequency is determined, required parameters need to be configured for searching for and locking the signals and outputting TSs. This process is signal search.

The signal search process is as follows:

Step 1 Check whether the chip communication is normal by reading CHIP_ID_L and then CHIP_ID_H. If the read data is not 0x31 and 0x37, verify that the I^2C component address of the chip and the circuit connection are correct.

Step 2 Initialize the chip, and initialize the PLL, ADC, clock recovery, and carrier recovery modules by configuring registers.

Step 3 Set the search mode. Set the mode for searching DVB-T/T2 signals by configuring MAN_RST_CTRL1[cfg_scan], or set the mode for searching DVB-T2 signals in Base/Lite mode by configuring T2_CHK_CTRL[t2_lite].

Step 4 Set the output priority. Set the TS output priority for DVB-T signals during hierarchical transmission by configuring AUTO_DLY[prior_low] (the default value is 0, indicating that streams with a higher priority are output); set the ID of the PLP to be output for DVB-T2 signals in Multi PLP mode by configuring PLP_CTRL[common_plp], PLP_ID0, and PLP_ID1.

Step 5 Configure the tuner RF frequency, wait 5 ms to 20 ms, and perform a hot reset. The wait time depends on the tuner.

Step 6 Wait about 20 ms and then query LOCK_FLAG[tps_ok_t] or LOCK_FLAG [sig_ok_t2]. If tps_ok_t is 1, DVB-T signals are captured successfully; if sig_ok_t2 is 1, DVB-T2 signals are captured successfully. In this case, go to step 7; otherwise, wait and query until the maximum wait time (300 ms for DVB-T or 500 ms for DVB-T2) is reached. If tps_ok_t and sig_ok_t2 are still 0 when the maximum wait time is reached, the frequency fails to be locked, indicating that there is no signal at this frequency or the signal quality is too low.

Step 7 Query LOCK_FLAG[fec_ok]. If fec_ok is 1, the signals are successfully captured, and TSs start to be output.

NOTE

For the DVB-T2 Multi PLP mode, before the first signal search, you need to confirm the number of PLPs and PLP_GROUP_ID and PLP_TYPE of each PLP so that the Demod can be correctly configured to output expected TSs.

----End

2.15 Summary of Demod Registers

When you write to only some bits of a register, read the register, change the values of the bits to be written, and retain the values of other bits.

If a state to be read is specified by multiple registers, read the low register and then high register unless otherwise specified. For example, to obtain car_offset specified by the registers CAR_OFFSET_L and CAR_OFFSET_H, read CAR_OFFSET_L and then CAR_OFFSET_H.

Table 2-19 describes Demod registers.

Table 2-19 Summary of Demod registers (base address: 0x00)

Offset Address	Name	Description	Page
0x20	MAN_RST_CTRL0	Reset control register	2-26
0x21	MAN_RST_CTRL1	Reset control enable register	2-27
0x22	STATE_WAITS	Timeout reset register	2-27
0x23	CLK_DEMO_L	Demodulation clock low register	2-28
0x24	CLK_DEMO_M	Demodulation clock middle register	2-28
0x25	CHIP_ID_L	Chip ID low register	2-29
0x26	CLK_FEC_L	FEC clock low register	2-29
0x27	CLK_FEC_M	FEC clock middle register	2-29
0x28	CHIP_ID_H	Chip ID high register	2-30
0x29	CLK_SDC_L	Synopsys design constraint (SDC) clock low register	2-30
0x2A	CLK_SDC_M	SDC clock middle register	2-31
0x2B	SDC_CTRL	SDC control register	2-31
0x2C	LOCK_FLAG	Lock flag register	2-32
0x2D	TUNER_SEL	Tuner control register	2-32
0x2E	RSTN_CTRL	Logic reset register	2-33
0x2F	ILA_SEL	Test vector select register	2-34
0x30	AGC_SPEED_BOUND	AGC step register	2-34

Offset Address	Name	Description	Page
0x31	AGC_GOAL	AGC power register	2-34
0x32	AGCOK_WAIT	AGC wait register	2-35
0x33	AGC_CTRL	AGC control register	2-35
0x34	AGC_DC_I	Channel I direct current (DC) register	2-36
0x35	AGC_DC_Q	Channel Q DC register	2-36
0x36	DAGC_CTRL	Digital AGC (DAGC) control register	2-36
0x37	AGC_CTRL_L	AGC power high register	2-37
0x38	AGC_CTRL_H	AGC power low register	2-37
0x39	AMP_ERR_IIR	Amplitude error register	2-38
0x3A	PDM_CTRL_L	Manual AGC control word low register	2-38
0x3B	PDM_CTRL_H	Manual AGC control word high register	2-39
0x3C	USE_PWM	AGC output wave select register	2-39
0x40	MF_SEL	Matched filter select register	2-39
0x41	SF_RMV	Narrowband interference suppression control register	2-40
0x42	DAGC_REF	DAGC amplitude reference register	2-41
0x43	DAGC_SPEED	DAGC step select register	2-41
0x4A	IF_FREQ_L	Input signal IF low register	2-41
0x4B	IF_FREQ_H	Input signal IF high register	2-42
0x4E	BAND_WIDTH	Input signal bandwidth register	2-42
0x50	SYN_CTRL0	Sync control register	2-42
0x51	CORR_HIGH_TH	P2-related detection upper threshold register	2-43
0x52	CORR_LOW_TH	P2-related detection lower threshold register	2-43
0x53	P2_POS_MOD	P2 sync position modification register	2-44
0x54	P1_THRES	P1 sync control register	2-44
0x55	CHN_FFT_GI	Sync detection parameter register	2-44
0x56	P1_SIGNAL	P1 detection signaling register	2-45
0x57	TIM_OFFSET	Timing offset register	2-46

Offset Address	Name	Description	Page
0x58	CAR_OFFSET_L	Carrier offset low register	2-46
0x59	CAR_OFFSET_H	Carrier offset high register	2-47
0x5D	T2_CHK_CTRL	DVB-T2 detection configuration register	2-47
0x5E	SOAC_TH	P1 signaling detection threshold register	2-47
0x5F	OUTP_RAND	Output TS scrambling register	2-48
0x60	LOOP_BW	Loop bandwidth select register	2-48
0x61	FD_GRP	Time domain interpolation control register	2-49
0x64	NP_IIR_SFT	Channel state information (CSI) calculation control register	2-49
0x67	ECHO_THRES	Multipath detection threshold register	2-50
0x69	MIN_THRES	Multipath detection minimum threshold register	2-50
0x6A	NP_GRP	Time domain interpolation control register	2-51
0x6B	TS_A9_SEL	TS output control register	2-51
0x6C	TS_87_SEL	TS output control register	2-52
0x6D	TS_65_SEL	TS output control register	2-52
0x6E	TS_43_SEL	TS output control register	2-53
0x6F	TS_21_SEL	TS output control register	2-53
0x70	TIM_LOOP_L	Timing offset low register	2-54
0x71	TIM_LOOP_H	Timing offset high register	2-54
0x75	TS_0_SEL	TS output control register	2-55
0x76	CIR_DIST_0	Multipath distribution register	2-55
0x77	CIR_DIST_1	Multipath distribution register	2-55
0x78	CIR_DIST_2	Multipath distribution register	2-56
0x79	CIR_DIST_3	Multipath distribution register	2-56
0x7A	SNR_L	SNR low register	2-57
0x7B	SNR_H	SNR high register	2-57
0x7C	DOPPLER	Doppler indicator register	2-57

Offset Address	Name	Description	Page
0x80	CW_FREQ_L	Single-frequency interference frequency low register	2-58
0x81	CW_FREQ_H	Single-frequency interference frequency high register	2-58
0x85	CLK_ADC_L	ADC clock low register	2-59
0x86	CLK_ADC_M	ADC clock middle register	2-59
0x87	CLK_ADC_H	ADC clock high register	2-60
0x88	ATV_STATE	Same-frequency interference flag register	2-60
0x91	ITER_CTRL	Iteration control register	2-60
0x92	BER_CTRL	BER control register	2-61
0x93	AUTO_DLY	Iteration switch register	2-61
0x94	ITER_NUM	PRE signaling iteration times register	2-62
0x95	ITER_NUM_POST	POST signaling iteration times register	2-62
0x96	FEC_BER_L	BER low register	2-63
0x97	FEC_BER_H	BER high register	2-63
0x98	FEC_FER_L	FER low register	2-64
0x99	FEC_FER_H	FER high register	2-64
0x9C	SWITCH_DLY	Signaling code word switch delay register	2-64
0x9E	T2_SUCCESS	T2 decoding success register	2-65
0xA0	OUTP_ISSY	Input stream synchronizer (ISSY) control register	2-65
0xA1	OUTP_DCAP_SET	Data PLP capacity configuration register	2-66
0xA2	OUTP_CCAP_SET	Common PLP capacity configuration register	2-66
0xA3	OUTP_PLL0	PLL control register	2-66
0xA4	OUTP_PLL1	PLL control register	2-67
0xA5	OUTP_PLL2	PLL control register	2-67
0xA6	OUTP_PLL3	PLL control register	2-68
0xA7	OUTP_PLL4	PLL control register	2-68

Offset Address	Name	Description	Page
0xA8	OUTP_CLK_SET	Output clock configuration register	2-69
0xA9	OUTP_CLK_SETH	I^2C clock configuration register	2-69
0xAA	OUTP_CLK_SETL	I^2C clock configuration register	2-70
0xAB	OUTP_MODE_SET	Output mode configuration register	2-70
0xAC	OUTP_TS_MODE	TS output mode configuration register	2-71
0xAE	OUTP_PKT_STA	TS packet count configuration register	2-72
0xAF	OUTP_LIMIT_EN	Limit and enable register	2-72
0xB0	PLP_CTRL	PLP control register	2-73
0xB1	PLP_ID0	Data PLP ID register	2-74
0xB2	PLP_ID1	Common PLP ID register	2-74
0xB3	TPS	Signal parameter register	2-75
0xB4	STREAM_TYPE	Transfer data stream type indicator register	2-76
0xB4	CODE_RATE_DVBT	DVB-T internal code rate register	2-76
0xB5	TPS_DVBT	DVB-T signal parameter register	2-77
0xB6	PAPR_L1MOD	DVB-T2 PRE signaling register	2-78
0xB8	PP_VERSION	DVB-T2 PRE signaling register	2-79
0xB9	NUM_T2_FRM	DVB-T2 PRE signaling register	2-79
0xBA	LDATA_L	DVB-T2 PRE signaling register	2-80
0xBB	LDATA_H	DVB-T2 PRE signaling register	2-80
0xBF	NUM_PLP	DVB-T2 PRE signaling register	2-80
0xC6	PLP_ID	DVB-T2 POST signaling register	2-81
0xC7	PLP_TYPE	DVB-T2 POST signaling register	2-81
0xC8	PLP_GRP_ID	DVB-T2 POST signaling register	2-82
0xC9	PLP_PARAM	DVB-T2 POST signaling register	2-82
0x00	ADC_CTRL0	ADC IP control register	2-84
0x01	ADC_CTRL1	ADC IP control register	2-84
0x02	ADC_CTRL2	ADC IP control register	2-85
0x03	ADC_CTRL3	ADC IP control register	2-86
0x04	ADC_FSCTRL	ADC IP control register	2-87

Offset Address	Name	Description	Page
0x05	PLL_LOCK	PLL lock indicator register	2-87
0x06	PLL0_FRAC_L	PLL0 frequency divider decimal part low register	2-88
0x07	PLL0_PD	PLL0 power-down control register	2-88
0x08	PLL0_POSTDIV	PLL0 post divider configuration register	2-89
0x09	PLL0_FBDIV	PLL0 feedback divider register	2-90
0x0A	PLL0_REFDIV	PLL0 reference divider register	2-90
0x0B	PLL0_SPREAD	PLL0 spread spectrum mode configuration register	2-91
0x0C	PLL_DIVVAL	PLL spread spectrum mode output divider control register	2-91
0x0D	PLL1_FRAC_L	PLL1 frequency divider decimal part low register	2-92
0x0E	PLL1_PD	PLL1 power-down control register	2-92
0x0F	PLL1_POSTDIV	PLL1 post divider configuration register	2-93
0x10	PLL1_FBDIV	PLL1 feedback divider register	2-93
0x11	PLL1_REFDIV	PLL1 reference divider register	2-93
0x12	PLL1_SPREAD	PLL1 spread spectrum mode configuration register	2-94
0x13	IO_CTRL0	I/O control register	2-95
0x14	IO_CTRL1	I/O control register	2-95
0x15	IO_CTRL2	I/O control register	2-96
0x16	IO_CTRL3	I/O control register	2-97
0x17	IO_CTRL4	I/O control register	2-98
0x18	SDR_CTRL	SDRAM control register	2-99

2.16 Description of Demod Registers

MAN_RST_CTRL0

MAN_RST_CTRL0 is a reset control register.

Offset Address	Register Name	Total Reset Value
0x20	MAN_RST_CTRL0	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rstn_sig	rstn_tdp	rstn_fec	rstn_tps	rstn_fbl	rstn_ceq	rstn_sync	rstn_agc
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RW	rstn_sig	SIG reset control 1: deassert reset 0: reset
[6]	RW	rstn_tdp	TDP reset control 1: deassert reset 0: reset
[5]	RW	rstn_fec	FEC reset control 1: deassert reset 0: reset
[4]	RW	rstn_tps	TPS reset control 1: deassert reset 0: reset
[3]	RW	rstn_fbl	FBL reset control 1: deassert reset 0: reset
[2]	RW	rstn_ceq	CEQ reset control 1: deassert reset 0: reset
[1]	RW	rstn_sync	Sync reset control 1: deassert reset 0: reset
[0]	RW	rstn_agc	AGC reset control 1: deassert reset 0: reset

MAN_RST_CTRL1

MAN_RST_CTRL1 is a reset control enable register.

Offset Address	Register Name	Total Reset Value
0x21	MAN_RST_CTRL1	0x5F

Bit	7	6	5	4	3	2	1	0
Name	cfg_tcl	cfg_scan		outp_rst_ena	auto_rst_ena	rstn_catch	rstn_sdc	rstn_outp
Reset	0	1	0	1	1	1	1	1

Bits	Access	Name	Description
[7]	RW	cfg_tcl	SDRAM TCL 1: TCL = 3 0: TCL = 2
[6:5]	RW	cfg_scan	Channel scan select 00: DVB-T2 signals only 00: DVB-T signals only 10: DVB-T2/DVB-T signals adaptively 11: reserved
[4]	RW	outp_rst_ena	OUTP auto reset enable 1: enabled 0: disabled
[3]	RW	auto_rst_ena	FEC auto reset enable 1: enabled 0: disabled
[2]	RW	rstn_catch	Catch reset control 1: deassert reset 0: reset
[1]	RW	rstn_sdc	SDC reset control 1: deassert reset 0: reset
[0]	RW	rstn_outp	OUTP reset control 1: deassert reset 0: reset

STATE_WAITS

STATE_WAITS is a timeout reset register.

Offset Address	Register Name	Total Reset Value
0x22	STATE_WAITS	0x16

Bit	7	6	5	4	3	2	1	0
Name	state_wait							
Reset	0	0	0	1	0	1	1	0

Bits	Access	Name	Description
[7:0]	RW	state_wait	OK signal wait timeout reset When bit[28:21] of the counter are greater than or equal to the state_wait field, the system is reset. When state_wait is 0xFF, timeout reset is disabled.

CLK_DEMO_L

CLK_DEMO_L is a demodulation clock low register.

Offset Address	Register Name	Total Reset Value
0x23	CLK_DEMO_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	clk_demo_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	clk_demo_l	Lower bits of the frequency of the demodulation clock CLK_DEMO. The LSB indicates 1 kHz.

CLK_DEMO_M

CLK_DEMO_M is a demodulation clock middle register.

Offset Address	Register Name	Total Reset Value
0x24	CLK_DEMO_M	0xFA

Bit	7	6	5	4	3	2	1	0
Name	clk_demo_m							
Reset	1	1	1	1	1	0	1	0

Bits	Access	Name	Description
[7:0]	RW	clk_demo_m	Middle bits of the frequency of the demodulation clock CLK_DEMO

CHIP_ID_L

CHIP_ID_L is a chip ID low register.

Offset Address	Register Name	Total Reset Value
0x25	CHIP_ID_L	0x37

Bit	7	6	5	4	3	2	1	0
Name	chip_id_l							
Reset	0	0	1	1	0	1	1	1

Bits	Access	Name	Description
[7:0]	RO	chip_id_l	Lower eight bits of the chip ID (0x3137)

CLK_FEC_L

CLK_FEC_L is an FEC clock low register.

Offset Address	Register Name	Total Reset Value
0x26	CLK_FEC_L	0xA8

Bit	7	6	5	4	3	2	1	0
Name	clk_fec_l							
Reset	1	0	1	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	clk_fec_l	Lower bits of the frequency of the decoding clock CLK_FEC. The LSB indicates 1 kHz.

CLK_FEC_M

CLK_FEC_M is an FEC clock middle register.

Offset Address	Register Name	Total Reset Value
0x27	CLK_FEC_M	0x55

Bit	7	6	5	4	3	2	1	0
Name	clk_fec_m							
Reset	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	clk_fec_m	Middle bits of the frequency of the decoding clock CLK_FEC

CHIP_ID_H

CHIP_ID_H is a chip ID high register.

Offset Address	Register Name	Total Reset Value
0x28	CHIP_ID_H	0x31

Bit	7	6	5	4	3	2	1	0
Name	chip_id_h							
Reset	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[7:0]	RW	chip_id_h	Upper eight bits of the chip ID (0x3137)

CLK_SDC_L

CLK_SDC_L is an SDC clock low register.

Offset Address	Register Name	Total Reset Value
0x29	CLK_SDC_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	clk_sdc_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	clk_sdc_l	Lower bits of the frequency of the SDC clock CLK_SDC. The LSB indicates 3 kHz.

CLK_SDC_M

CLK_SDC_M is an SDC clock middle register.

Offset Address	Register Name	Total Reset Value
0x2A	CLK_SDC_M	0x7D

Bit	7	6	5	4	3	2	1	0
Name	clk_sdc_m							
Reset	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	clk_sdc_m	Middle bits of the frequency of the SDC clock CLK_SDC

SDC_CTRL

SDC_CTRL is an SDC control register.

Offset Address	Register Name	Total Reset Value
0x2B	SDC_CTRL	0x18

Bit	7	6	5	4	3	2	1	0
Name	sdr_slfchk_ok	sdr_slfchk_ena	sdr_fix_num			stop_addrinc	reserved	clk_sdc_h
Reset	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[7]	RO	sdr_slfchk_ok	SDRAM self check result 0: correct 1: incorrect
[6]	RW	sdr_slfchk_ena	SDRAM self check enable 0: enabled 1: disabled
[5:3]	RW	sdr_fix_num	Number of SDC fixed time slices
[2]	RW	stop_addrinc	Address auto increase enable for the data capture module 1: disabled 0: enabled
[1]	-	reserved	Reserved
[0]	RW	clk_sdc_h	MSB of the frequency of the SDC clock CLK_SDC

LOCK_FLAG

LOCK_FLAG is a lock flag register.

Offset Address	Register Name	Total Reset Value
0x2C	LOCK_FLAG	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		fec_ok	tps_ok_t	sig_ok_t2	syn_pre_ok_t	syn_ok	agc_ok
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved
[5]	RO	fec_ok	FEC lock flag 1: locked 0: unlocked
[4]	RO	tps_ok_t	DVB-T transmission parameter lock flag 1: locked 0: unlocked
[3]	RO	sig_ok_t2	DVB-T2 signaling lock flag 1: locked 0: unlocked
[2]	RO	syn_pre_ok_t	DVB-T sync lock flag 1: locked 0: unlocked
[1]	RO	syn_ok	Sync lock flag 1: locked 0: unlocked
[0]	RO	agc_ok	AGC lock flag 1: locked 0: unlocked

TUNER_SEL

TUNER_SEL is a tuner control register.

Offset Address	Register Name	Total Reset Value
0x2D	TUNER_SEL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			man_state				tuner_sel
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	-	reserved	Reserved
[4:1]	RO	man_state	Status of the main control state machine
[0]	RW	tuner_sel	Tuner signal selected by configuring the I^2C This field must be set to 1 before the tuner is configured. Each time after the tuner is read or written, this field is automatically cleared. If you need to continue to configure the tuner, set this field to 1 again.

RSTN_CTRL

RSTN_CTRL is a logic reset register.

Offset Address	Register Name	Total Reset Value
0x2E	RSTN_CTRL	0x83

Bit	7	6	5	4	3	2	1	0
Name	clk_fec_h		clk_dem_h		reserved		hot_rstn	cool_rstn
Reset	1	0	0	0	0	0	1	1

Bits	Access	Name	Description
[7:6]	RW	clk_fec_h	Upper bits of the frequency of the decoding clock CLK_FEC
[5:4]	RW	clk_dem_h	Upper bits of the frequency of the demodulation clock CLK_DEMO
[3:2]	-	reserved	Reserved
[1]	RW	hot_rstn	Logic reset signal. Only the logic but not the system registers is reset. 1: not reset 0: reset
[0]	RW	cool_rstn	Reset signal. The logic and system registers are reset. 1: not reset 0: reset

ILA_SEL

ILA_SEL is a test vector select register.

Offset Address	Register Name	Total Reset Value
0x2F	ILA_SEL	0x00

Bit	7	6	5	4	3	2	1	0
Name	ila_sel							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	ila_sel	Test vector select for the ILA and Catch modules

AGC_SPEED_BOUND

AGC_SPEED_BOUND is an AGC step register.

Offset Address	Register Name	Total Reset Value
0x30	AGC_SPEED_BOUND	0x67

Bit	7	6	5	4	3	2	1	0
Name	agc_speed			err_bound				
Reset	0	1	1	0	0	1	1	1

Bits	Access	Name	Description
[7:5]	RW	agc_speed	AGC step. The actual value is the configured value plus 2 and the maximum value is 7.
[4:0]	RW	err_bound	Amplitude error boundary

AGC_GOAL

AGC_GOAL is an AGC power register.

Offset Address	Register Name	Total Reset Value
0x31	AGC_GOAL	0x0D

Bit	7	6	5	4	3	2	1	0
Name	agc_goal							
Reset	0	0	0	0	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	agc_goal	Target AGC power

AGCOK_WAIT

AGCOK_WAIT is an AGC wait register.

Offset Address	Register Name	Total Reset Value
0x32	AGCOK_WAIT	0x0C

Bit	7	6	5	4	3	2	1	0
Name	agcok_wait							
Reset	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[7:0]	RW	agcok_wait	AGC amplitude exception wait period

AGC_CTRL

AGC_CTRL is an AGC control register.

Offset Address	Register Name	Total Reset Value
0x33	AGC_CTRL	0x11

Bit	7	6	5	4	3	2	1	0
Name	pdm_div			adc_twos	iq_swap	agc_hold	agc_inverse	dagc_on
Reset	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[7:5]	RW	pdm_div	Pulse width of the AGC PDM output The actual value is the configured value plus 1.
[4]	RW	adc_twos	Input data type 1: two's complement 0: sign-and-magnitude
[3]	RW	iq_swap	I/Q data switch control 1: switched 0: not switched
[2]	RW	agc_hold	AGC working type 1: The AGC holds and the output PDM is a fixed value. 0: The AGC works in normal mode.
[1]	RW	agc_inverse	PDM signal output 1: inverted 0: not inverted (normal output)

[0]	RW	dagc_on	DAGC enable 1: enabled 0: disabled

AGC_DC_I

AGC_DC_I is a channel I DC register.

Offset Address	Register Name	Total Reset Value
0x34	AGC_DC_I	0x00

Bit	7	6	5	4	3	2	1	0
Name	agc_dc_i							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	agc_dc_i	DC value of channel I data

AGC_DC_Q

AGC_DC_Q is a channel Q DC register.

Offset Address	Register Name	Total Reset Value
0x35	AGC_DC_Q	0x00

Bit	7	6	5	4	3	2	1	0
Name	agc_dc_q							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	agc_dc_q	DC value of channel Q data

DAGC_CTRL

DAGC_CTRL is a DAGC control register.

Offset Address	Register Name	Total Reset Value
0x36	DAGC_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	dagc_ctrl							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	dagc_ctrl	Control word of the DAGC

AGC_CTRL_L

AGC_CTRL_L is an AGC power low register.

Offset Address	Register Name	Total Reset Value
0x37	AGC_CTRL_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	agc_ok	reserved			agc_ctrl_l			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	agc_ok	AGC lock flag 1: locked 0: unlocked
[6:4]	-	reserved	Reserved
[3:0]	RO	agc_ctrl_l	Lower four bits of the AGC control word, indicating the current signal power

AGC_CTRL_H

AGC_CTRL_H is an AGC power high register.

Offset Address	Register Name	Total Reset Value
0x38	AGC_CTRL_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	agc_ctrl_H							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	agc_ctrl_H	Upper eight bits of the AGC control word, indicating the current signal power

AMP_ERR_IIR

AMP_ERR_IIR is an amplitude error register.

Offset Address	Register Name	Total Reset Value
0x39	AMP_ERR_IIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	amp_err_iir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	amp_err_iir	ADC input signal amplitude error relative to the target value

PDM_CTRL_L

PDM_CTRL_L is a manual AGC control word low register.

Offset Address	Register Name	Total Reset Value
0x3A	PDM_CTRL_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			pdm_ctrl_sel	pdm_ctrl_h			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	-	reserved	Reserved
[4]	RW	pdm_ctrl_sel	Manual AGC control 1: manual mode (pdm_ctrl_sel acts as the control word) 0: automatic AGC mode

[3:0]	RW	pdm_ctrl_l	Lower four bits of the configurable AGC control word in manual AGC mode

PDM_CTRL_H

PDM_CTRL_H is a manual AGC control word high register.

Offset Address	Register Name	Total Reset Value
0x3B	PDM_CTRL_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	pdm_ctrl_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	pdm_ctrl_h	Upper eight bits of the configurable AGC control word in manual AGC mode

USE_PWM

USE_PWM is an AGC output wave select register.

Offset Address	Register Name	Total Reset Value
0x3C	USE_PWM	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							use_pwm
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Reserved
[0]	RW	use_pwm	AGC output wave 0: PDM 1: PWM

MF_SEL

MF_SEL is a matched filter select register.

Offset Address	Register Name	Total Reset Value
0x40	MF_SEL	0xC9

Bit	7	6	5	4	3	2	1	0
Name	dagc_ena	auto_atvfreq	reserved		mf_sel			
Reset	1	1	0	0	1	0	0	1

Bits	Access	Name	Description
[7]	RW	dagc_ena	Internal DAGC enable 1: enabled 0: disabled
[6]	RW	auto_atvfreq	Internal ATV frequency 1: auto 0: configured input
[5:4]	-	reserved	Reserved
[3:0]	RW	mf_sel	Matched filter (the default value is 9 for DVB-T/T2)

SF_RMV

SF_RMV is a narrowband interference suppression control register.

Offset Address	Register Name	Total Reset Value
0x41	SF_RMV	0xCC

Bit	7	6	5	4	3	2	1	0
Name	sf_rmv	atv_on	pll_thres					
Reset	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[7]	RW	sf_rmv	Internal single-frequency interference suppression module enable 1: enabled 0: disabled
[6]	RW	atv_on	Internal same-frequency interference suppression module enable 1: enabled 0: disabled
[5:0]	RW	pll_thres	Single-frequency detection threshold

DAGC_REF

DAGC_REF is a DAGC amplitude reference register.

Offset Address	Register Name	Total Reset Value
0x42	DAGC_REF	0x5A

Bit	7	6	5	4	3	2	1	0
Name	dagc_ref							
Reset	0	1	0	1	1	0	1	0

Bits	Access	Name	Description
[7:0]	RW	dagc_ref	DGAC amplitude reference

DAGC_SPEED

DAGC_SPEED is a DAGC step select register.

Offset Address	Register Name	Total Reset Value
0x43	DAGC_SPEED	0x20

Bit	7	6	5	4	3	2	1	0
Name	dagc_speed							
Reset	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	dagc_speed	DGAC step

IF_FREQ_L

IF_FREQ_L is an input signal IF low register.

Offset Address	Register Name	Total Reset Value
0x4A	IF_FREQ_L	0x04

Bit	7	6	5	4	3	2	1	0
Name	if_freq_l							
Reset	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	if_freq_l	Lower eight bits of the input signal IF. The LSB indicates 1 kHz.

IF_FREQ_H

IF_FREQ_H is an input signal IF high register.

Offset Address	Register Name	Total Reset Value
0x4B	IF_FREQ_H	0x15

Bit	7	6	5	4	3	2	1	0
Name	if_freq_h							
Reset	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RW	if_freq_h	Upper eight bits of the input signal IF

BAND_WIDTH

BAND_WIDTH is an input signal bandwidth register.

Offset Address	Register Name	Total Reset Value
0x4E	BAND_WIDTH	0x40

Bit	7	6	5	4	3	2	1	0
Name	bw				reserved			
Reset	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RW	bw	Signal bandwidth 000: 1.7 MHz 001: 5 MHz 010: 6 MHz 011: 7 MHz 100: 8 MHz Other values: reserved
[3:0]	-	reserved	Reserved

SYN_CTRL0

SYN_CTRL0 is a sync control register.

Offset Address	Register Name	Total Reset Value
0x50	SYN_CTRL0	0x89

Bit	7	6	5	4	3	2	1	0
Name	rgn_scope				thr_t		reserved	p1_frac_sel
Reset	1	0	0	0	1	0	0	1

Bits	Access	Name	Description
[7:4]	RW	rgn_scope	P2-related scan scope
[3:2]	RW	thr_t	DVB-T related detection threshold
[1]	-	reserved	Reserved
[0]	RW	p1_frac_sel	P1 carrier detection mode

CORR_HIGH_TH

CORR_HIGH_TH is a P2-related detection upper threshold register.

Offset Address	Register Name	Total Reset Value
0x51	CORR_HIGH_TH	0x40

Bit	7	6	5	4	3	2	1	0
Name	corr_high_th							
Reset	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	corr_high_th	P2-related detection upper threshold

CORR_LOW_TH

CORR_LOW_TH is a P2-related detection lower threshold register.

Offset Address	Register Name	Total Reset Value
0x52	CORR_LOW_TH	0x18

Bit	7	6	5	4	3	2	1	0
Name	corr_low_th							
Reset	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	corr_low_th	P2-related detection lower threshold

P2_POS_MOD

P2_POS_MOD is a P2 sync position modification register.

Offset Address	Register Name	Total Reset Value
0x53	P2_POS_MOD	0x64

Bit	7	6	5	4	3	2	1	0
Name	p2_pos_mod							
Reset	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	p2_pos_mod	Modification on the detected P2 sync position

P1_THRES

P1_THRES is a P1 sync control register.

Offset Address	Register Name	Total Reset Value
0x54	P1_THRES	0xD0

Bit	7	6	5	4	3	2	1	0
Name	fscan_th	p1th_sel		p1_min_th				
Reset	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[7]	RW	fscan_th	P1 carrier scan validity decree threshold
[6:5]	RW	p1th_sel	P1 frequency domain data limit threshold
[4:0]	RW	p1_min_th	P1 time-domain detection minimum threshold

CHN_FFT_GI

CHN_FFT_GI is a sync detection parameter register.

Offset Address	Register Name	Total Reset Value
0x55	CHN_FFT_GI	0x00

Bit	7	6	5	4	3	2	1	0
Name	is_dvbt	spectrum	fft_size			gi_mode		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	is_dvbt	Signal indicator 1: DVB-T signals 0: DVB-T2 signals
[6]	RO	spectrum	Spectrum indicator 1: The input signal spectrum is inverted. 0: The input signal spectrum is normal.
[5:3]	RO	fft_size	FFT mode 000: 1K 001: 2K 010: 4K 011: 8K 100: 16K 101: 32K Other values: reserved
[2:0]	RO	gi_mode	Guard interval 000: 1/32 001: 1/16 010: 1/8 011: 1/4 100: 1/128 101: 19/128 110: 19/256 Other values: reserved When the FFT mode is 100 or 101, the guard interval indicator is invalid.

P1_SIGNAL

P1_SIGNAL is a P1 detection signaling register.

Offset Address	Register Name	Total Reset Value
0x56	P1_SIGNAL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	p1_signal_s1			p1_signal_s2			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	-	reserved	Reserved
[6:4]	RO	p1_signal_s1	S1 part of the P1 signaling
[3:0]	RO	p1_signal_s2	S2 part of the P1 signaling

TIM_OFFSET

TIM_OFFSET is a timing offset register.

Offset Address	Register Name	Total Reset Value
0x57	TIM_OFFSET	0x00

Bit	7	6	5	4	3	2	1	0
Name	tim_offset							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	tim_offset	Timing offset. The LSB indicates 4 ppm.

CAR_OFFSET_L

CAR_OFFSET_L is a carrier offset low register.

Offset Address	Register Name	Total Reset Value
0x58	CAR_OFFSET_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	car_offset_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	car_offset_l	Carrier offset low register. The LSB indicates 32 Hz.

CAR_OFFSET_H

CAR_OFFSET_H is a carrier offset high register.

Offset Address	Register Name	Total Reset Value
0x59	CAR_OFFSET_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	car_offset_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	car_offset_h	Carrier offset high register

T2_CHK_CTRL

T2_CHK_CTRL is a DVB-T2 detection configuration register.

Offset Address	Register Name	Total Reset Value
0x5D	T2_CHK_CTRL	0x02

Bit	7	6	5	4	3	2	1	0
Name	reserved		t2_lite		reserved		thr_t2	
Reset	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved
[5:4]	RW	t2_lite	T2 mode support 0: support only t2_base 1: support only t2_lite 2: support both t2_base and t2_lite. However, if the T2 signals contain T2 frames in both t2_base and t2_lite modes, the system randomly captures frames in only one mode, and frames in the other mode are detected based on the captured P1 signaling during signal search.
[3:2]	-	reserved	Reserved
[1:0]	RW	thr_t2	T2 signal detection threshold

SOAC_TH

SOAC_TH is a P1 signaling detection threshold register.

Offset Address	Register Name	Total Reset Value
0x5E	SOAC_TH	0x34

Bit	7	6	5	4	3	2	1	0
Name	reserved	fequ_param			soac_th			
Reset	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[7]	-	reserved	Reserved
[6:4]	RW	fequ_param	Internally reserved
[3:0]	RW	soac_th	P1 signaling detection threshold

OUTP_RAND

OUTP_RAND is an output TS scrambling register.

Offset Address	Register Name	Total Reset Value
0x5F	OUTP_RAND	0x08

Bit	7	6	5	4	3	2	1	0
Name	reserved		rand_no_hold	clk_min_wid			clk_rand	
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved
[5]	RW	rand_no_hold	1: The clock width and cycle are always scrambled. 0: The clock width and cycle are not scrambled under certain conditions.
[4:2]	RW	clk_min_wid	Minimum width of the high level and low level of the TS clock
[1:0]	RW	clk_rand	00: disable the scrambling module 01: enable the scrambling module with the maximum delay of 6 10: enable the scrambling module with the maximum delay of 9 11: enable the scrambling module with the maximum delay of 15

LOOP_BW

LOOP_BW is a loop bandwidth select register.

Offset Address	Register Name	Total Reset Value
0x60	LOOP_BW	0xA3

Bit	7	6	5	4	3	2	1	0
Name	cpe_on	tim_loop			car_loop			
Reset	1	0	1	0	0	0	1	1

Bits	Access	Name	Description
[7]	RW	cpe_on	CPE calibration enable 1: enabled 0: disabled
[6:4]	RW	tim_loop	Timing loop bandwidth (A larger value indicates narrower bandwidth.)
[3:0]	RW	car_loop	Carrier loop bandwidth (A larger value indicates narrower bandwidth.)

FD_GRP

FD_GRP is a time domain interpolation control register.

Offset Address	Register Name	Total Reset Value
0x61	FD_GRP	0x81

Bit	7	6	5	4	3	2	1	0
Name	div_p2				man_fd_grp	fd_grp		
Reset	1	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:4]	RW	div_p2	Multipath boundary of selected P2 symbols
[3]	RW	man_fd_grp	Whether the input bandwidth is adaptive during the calculation of the time domain interpolation coefficient 1: no 0: yes
[2:0]	RW	fd_grp	Interpolation bandwidth value configured by the system when man_fd_grp is 1. A larger value indicates broader bandwidth.

NP_IIR_SFT

NP_IIR_SFT is a CSI calculation control register.

Offset Address	Register Name	Total Reset Value
0x64	NP_IIR_SFT	0x65

Bit	7	6	5	4	3	2	1	0
Name	dop_th		sp_cell_on	np_para_sft			np_iir_sft	
Reset	0	1	1	0	0	1	0	1

Bits	Access	Name	Description
[7:6]	RW	dop_th	Doppler detection sensitivity. A larger value indicates greater sensitivity and higher probability of detecting false alarms.
[5]	RW	sp_cell_on	CSI narrowband interference suppression manual enable 1: enabled 0: disabled
[4:2]	RW	np_para_sft	Smoothing filter bandwidth during the calculation of the noise coefficient
[1:0]	RW	np_iir_sft	Smoothing filter bandwidth during the calculation of the narrowband interference

ECHO_THRES

ECHO_THRES is a multipath detection threshold register.

Offset Address	Register Name	Total Reset Value
0x67	ECHO_THRES	0x10

Bit	7	6	5	4	3	2	1	0
Name	th_mid				th_high			
Reset	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[7:4]	RW	th_mid	Middle threshold for multipath detection. A larger value indicates greater sensitivity.
[3:0]	RW	th_high	Upper threshold for multipath detection. A larger value indicates greater sensitivity.

MIN_THRES

MIN_THRES is a multipath detection minimum threshold register.

Offset Address	Register Name	Total Reset Value
0x69	MIN_THRES	0x08

Bit	7	6	5	4	3	2	1	0
Name	th_min							
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	th_min	Minimum threshold for multipath detection

NP_GRP

NP_GRP is a time domain interpolation control register.

Offset Address	Register Name	Total Reset Value
0x6A	NP_GRP	0x00

Bit	7	6	5	4	3	2	1	0
Name	isi_ena	fd_max			man_np_grp	np_grp		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	isi_ena	Elimination enable for interference between symbols 1: enabled 0: disabled
[6:4]	RW	fd_max	Maximum time domain interpolation bandwidth
[3]	RW	man_np_grp	Whether the noise coefficient is adaptive during the calculation of the time domain interpolation coefficient 1: no 0: yes
[2:0]	RW	np_grp	Noise coefficient configured by the system when man_np_grp is 1. A larger value indicates greater noise power.

TS_A9_SEL

TS_A9_SEL is a TS output control register.

Offset Address	Register Name	Total Reset Value
0x6B	TS_A9_SEL	0xA9

Bit	7	6	5	4	3	2	1	0
Name	ts_a_sel				ts_9_sel			
Reset	1	0	1	0	1	0	0	1

Bits	Access	Name	Description
[7:4]	RW	ts_a_sel	TS_ERR pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.
[3:0]	RW	ts_9_sel	TS_VLD pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.

TS_87_SEL

TS_87_SEL is a TS output control register.

Offset Address	Register Name	Total Reset Value
0x6C	TS_87_SEL	0x87

Bit	7	6	5	4	3	2	1	0
Name	ts_8_sel				ts_7_sel			
Reset	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[7:4]	RW	ts_8_sel	TS_SYNC pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.
[3:0]	RW	ts_7_sel	TS_OUT7 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.

TS_65_SEL

TS_65_SEL is a TS output control register.

Offset Address	Register Name	Total Reset Value
0x6D	TS_65_SEL	0x65

Bit	7	6	5	4	3	2	1	0
Name	ts_6_sel				ts_5_sel			
Reset	0	1	1	0	0	1	0	1

Bits	Access	Name	Description
[7:4]	RW	ts_6_sel	TS_OUT6 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.
[3:0]	RW	ts_5_sel	TS_OUT5 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.

TS_43_SEL

TS_43_SEL is a TS output control register.

Offset Address	Register Name	Total Reset Value
0x6E	TS_43_SEL	0x43

Bit	7	6	5	4	3	2	1	0
Name	ts_4_sel				ts_3_sel			
Reset	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[7:4]	RW	ts_4_sel	TS_OUT4 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.
[3:0]	RW	ts_3_sel	TS_OUT3 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.

TS_21_SEL

TS_21_SEL is a TS output control register.

Offset Address	Register Name	Total Reset Value
0x6F	TS_21_SEL	0x21

Bit	7	6	5	4	3	2	1	0
Name	ts_2_sel				ts_1_sel			
Reset	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[7:4]	RW	ts_2_sel	TS_OUT2 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.
[3:0]	RW	ts_1_sel	TS_OUT1 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.

TIM_LOOP_L

TIM_LOOP_L is a timing offset low register.

Offset Address	Register Name	Total Reset Value
0x70	TIM_LOOP_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	tim_loop_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	tim_loop_l	Lower bits of the timing offset output from the timing loop. The LSB indicates 1/16 ppm.

TIM_LOOP_H

TIM_LOOP_H is a timing offset high register.

Offset Address	Register Name	Total Reset Value
0x71	TIM_LOOP_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		tim_loop_h					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
5:0]	RO	tim_loop_h	Upper bits of the timing offset output from the timing loop

TS_0_SEL

TS_0_SEL is a TS output control register.

Offset Address	Register Name	Total Reset Value
0x75	TS_0_SEL	0x50

Bit	7	6	5	4	3	2	1	0
Name	cpadd_ena				ts_0_sel			
Reset	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[7:4]	RW	cpadd_ena	Internal key technology register for enabling the module for improving the performance in big guard interval mode
[3:0]	RW	ts_0_sel	TS_OUT0 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_dat[7:0]} are selected for signal output.

CIR_DIST_0

CIR_DIST_0 is a multipath distribution register.

Offset Address	Register Name	Total Reset Value
0x76	CIR_DIST_0	0x00

Bit	7	6	5	4	3	2	1	0
Name	cir_dist_0							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	cir_dist_0	Multipath distribution register for characterizing the distribution feature of the current channel impulse response (CIR). The CIR is represented by 32 bits. This register indicates bits 7 to 0.

CIR_DIST_1

CIR_DIST_1 is a multipath distribution register.

Offset Address	Register Name	Total Reset Value
0x77	CIR_DIST_1	0x00

Bit	7	6	5	4	3	2	1	0
Name	cir_dist_1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	cir_dist_1	Multipath distribution register for characterizing the distribution feature of the current CIR. The CIR is represented by 32 bits. This register indicates bits 15 to 8.

CIR_DIST_2

CIR_DIST_2 is a multipath distribution register.

Offset Address	Register Name	Total Reset Value
0x78	CIR_DIST_2	0x00

Bit	7	6	5	4	3	2	1	0
Name	cir_dist_2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	cir_dist_2	Multipath distribution register for characterizing the distribution feature of the current CIR. The CIR is represented by 32 bits. This register indicates bits 23 to 16.

CIR_DIST_3

CIR_DIST_3 is a multipath distribution register.

Offset Address	Register Name	Total Reset Value
0x79	CIR_DIST_3	0x00

Bit	7	6	5	4	3	2	1	0
Name	cir_dist_3							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	cir_dist_3	Multipath distribution register for characterizing the distribution feature of the current CIR. The CIR is represented by 32 bits. This register indicates bits 31 to 24.

SNR_L

SNR_L is an SNR low register.

Offset Address	Register Name	Total Reset Value
0x7A	SNR_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	snr_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	snr_l	Lower bits of the SNR register for calculating the SNR (dB) of the current input signal SNR = 10 x log10 (snr_h x 256 + snr_l) – 12

SNR_H

SNR_H is an SNR high register.

Offset Address	Register Name	Total Reset Value
0x7B	SNR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	snr_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	snr_h	Upper bits of the SNR register

DOPPLER

DOPPLER is a Doppler indicator register.

Offset Address	Register Name	Total Reset Value
0x7C	DOPPLER	0x00

Bit	7	6	5	4	3	2	1	0
Name	doppler					rela_fd_grp		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	doppler	Doppler value calculated by the demo
[2:0]	RO	rela_fd_grp	Bandwidth for the time domain interpolation coefficient calculation

CW_FREQ_L

CW_FREQ_L is a single-frequency interference frequency low register.

Offset Address	Register Name	Total Reset Value
0x80	CW_FREQ_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	cw_freq_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	cw_freq_l	Lower bits of the single-frequency interference frequency. The LSB indicates 9 kHz.

CW_FREQ_H

CW_FREQ_H is a single-frequency interference frequency high register.

Offset Address	Register Name	Total Reset Value
0x81	CW_FREQ_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	cw_lock	reserved					cw_freq_H	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	cw_lock	Whether single-frequency interference exists 1: yes 0: no

[6:2]	-	reserved	Reserved
[1:0]	RW	cw_freq_H	Upper bits of the single-frequency interference frequency

CLK_ADC_L

CLK_ADC_L is an ADC clock low register.

Offset Address	Register Name	Total Reset Value
0x85	CLK_ADC_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	clk_adc_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	clk_adc_l	Lower bits of the frequency of the ADC clock CLK_ADC. The LSB indicates 1 kHz.

CLK_ADC_M

CLK_ADC_M is an ADC clock middle register.

Offset Address	Register Name	Total Reset Value
0x86	CLK_ADC_M	0x7D

Bit	7	6	5	4	3	2	1	0
Name	clk_adc_m							
Reset	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[7:0]	RW	clk_adc_m	Middle bits of the frequency of the ADC clock CLK_ADC

CLK_ADC_H

CLK_ADC_H is an ADC clock high register.

Offset Address	Register Name	Total Reset Value
0x87	CLK_ADC_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						clk_adc_h	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	-	reserved	Reserved
[1:0]	RW	clk_adc_h	Upper bits of the frequency of the ADC clock CLK_ADC

ATV_STATE

ATV_STATE is a same-frequency interference flag register.

Offset Address	Register Name	Total Reset Value
0x88	ATV_STATE	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							atv_state
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	-	reserved	Description information
[0]	RO	atv_state	Whether same-frequency interference exists 1: yes 0: no

ITER_CTRL

ITER_CTRL is an iteration control register.

Offset Address	Register Name	Total Reset Value
0x91	ITER_CTRL	0xA4

Bit	7	6	5	4	3	2	1	0
Name	fix_iter	fix_iter_man	fix_iter_num					
Reset	1	0	1	0	0	1	0	0

Bits	Access	Name	Description
[7]	RW	fix_iter	Fixed or selected maximum iteration times 1: fixed 0: automatically selected
[6]	RW	fix_iter_man	Manually or automatically configured maximum iteration times 1: manually 0: automatically
[5:0]	RW	fix_iter_num	Manually configured maximum iteration times

BER_CTRL

BER_CTRL is a BER control register.

Offset Address	Register Name	Total Reset Value
0x92	BER_CTRL	0xB4

Bit	7	6	5	4	3	2	1	0
Name	stop_sel	frame_num			high_err			
Reset	1	0	1	1	0	1	0	0

Bits	Access	Name	Description
[7]	RW	stop_sel	Iteration check stop 1: Automatic iteration check stops. 0: Iteration stops when the maximum iteration times are reached.
[6:4]	RW	frame_num	BER statistics period
[3:0]	RW	high_err	Threshold for high BER reset

AUTO_DLY

AUTO_DLY is an iteration switch register.

Offset Address	Register Name	Total Reset Value
0x93	AUTO_DLY	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved						prior_low	auto_dly
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:2]	-	reserved	Reserved
[1]	RW	prior_low	Stream output select in DVB-T hierarchical mode 1: output streams with a low priority 0: output streams with a high priority
[0]	RW	auto_dly	Signaling code word switch wait time 1: automatically selected 0: configured

ITER_NUM

ITER_NUM is a PRE signaling iteration times register.

Offset Address	Register Name	Total Reset Value
0x94	ITER_NUM	0x18

Bit	7	6	5	4	3	2	1	0
Name	gate_off	reserved	iter_num_pre					
Reset	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[7]	RW	gate_off	Gating enable 1: disabled 0: enabled
[6]	-	reserved	Reserved
[5:0]	RW	iter_num_pre	Maximum iteration times for L1 PRE decoding

ITER_NUM_POST

ITER_NUM_POST is a POST signaling iteration times register.

Offset Address	Register Name	Total Reset Value
0x95	ITER_NUM_POST	0x18

Bit	7	6	5	4	3	2	1	0
Name	reserved			iter_num_post				
Reset	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[7:6]	-	reserved	Reserved
[5:0]	RW	iter_num_post	Maximum iteration times for L1 POST decoding

FEC_BER_L

FEC_BER_L is a BER low register.

Offset Address	Register Name	Total Reset Value
0x96	FEC_BER_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	fec_ber_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	fec_ber_l	Lower eight bits of BER statistics

FEC_BER_H

FEC_BER_H is a BER high register.

Offset Address	Register Name	Total Reset Value
0x97	FEC_BER_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	fec_ber_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	fec_ber_h	Upper eight bits of BER statistics

FEC_FER_L

FEC_FER_L is an FER low register.

Offset Address	Register Name	Total Reset Value
0x98	FEC_FER_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	fec_fer_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	fec_fer_l	Lower eight bits of the error frame count

FEC_FER_H

FEC_FER_H is an FER high register.

Offset Address	Register Name	Total Reset Value
0x99	FEC_FER_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	fec_fer_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	fec_fer_h	Upper eight bits of the error frame count

SWITCH_DLY

SWITCH_DLY is a signaling code word switch delay register.

Offset Address	Register Name	Total Reset Value
0x9C	SWITCH_DLY	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	man_switch_dly						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	-	reserved	Reserved
[6:0]	RW	man_switch_dly	Manually configured delay for signaling code word switching

T2_SUCCESS

T2_SUCCESS is a T2 decoding success register.

Offset Address	Register Name	Total Reset Value
0x9E	T2_SUCCESS	0x00

Bit	7	6	5	4	3	2	1	0
Name	iter_num						bch_cancorr	ldpc_badly
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	iter_num	LDPC decoding iteration times
[1]	RO	bch_cancorr	BCH decoding success flag 1: success 0: failure
[0]	RO	ldpc_badly	LDPC decoding success/failure 1: failure 0: success

OUTP_ISSY

OUTP_ISSY is an ISSY control register.

Offset Address	Register Name	Total Reset Value
0xA0	OUTP_ISSY	0x10

Bit	7	6	5	4	3	2	1	0
Name	issy_long	issy_rmv	tto_adjust					
Reset	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[7]	RW	issy_long	ISSY length 1: 3 bytes for ISSY of GCS and GSE streams 0: 2 bytes for ISSY of GCS and GSE streams
[6]	RW	issy_rmv	ISSY removal select 1: GCS and GSE stream packet length contains the ISSY. 0: GCS and GSE stream packet length does not contain the ISSY.
[5:0]	RW	tto_adjust	TTO adjustment

OUTP_DCAP_SET

OUTP_DCAP_SET is a data PLP capacity configuration register.

Offset Address	Register Name	Total Reset Value
0xA1	OUTP_DCAP_SET	0xC9

Bit	7	6	5	4	3	2	1	0
Name	vol_dset							
Reset	1	1	0	0	1	0	0	1

Bits	Access	Name	Description
[7:0]	RW	vol_dset	Data PLP capacity. OUTP_DCAP_SET[7:4] << OUTP_DCAP_SET[3:0] kbit, OUTP_DCAP_SET[7:4] ≥ 8

OUTP_CCAP_SET

OUTP_CCAP_SET is a common PLP capacity configuration register.

Offset Address	Register Name	Total Reset Value
0xA2	OUTP_CCAP_SET	0x88

Bit	7	6	5	4	3	2	1	0
Name	vol_cset							
Reset	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:0]	RW	vol_cset	Common PLP capacity. OUTP_CCAP_SET[7:4] << OUTP_CCAP_SET[3:0] kbit, OUTP_CCAP_SET[7:4] ≥ 8

OUTP_PLL0

OUTP_PLL0 is a PLL control register.

Offset Address	Register Name	Total Reset Value
0xA3	OUTP_PLL0	0x83

Bit	7	6	5	4	3	2	1	0
Name	cent_point					cent_speed		
Reset	1	0	0	0	0	0	1	1

Bits	Access	Name	Description
[7:3]	RW	cent_point	Position of the OUTP RAM central area
[2:0]	RW	cent_speed	Feedback coefficient for the central area

OUTP_PLL1

OUTP_PLL1 is a PLL control register.

Offset Address	Register Name	Total Reset Value
0xA4	OUTP_PLL1	0x9B

Bit	7	6	5	4	3	2	1	0
Name	slow_high					fast_speed		
Reset	1	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:3]	RW	slow_high	Upper threshold for the OUTP RAM slow adjustment area
[2:0]	RW	fast_speed	Feedback coefficient for the fast adjustment area

OUTP_PLL2

OUTP_PLL2 is a PLL control register.

Offset Address	Register Name	Total Reset Value
0xA5	OUTP_PLL2	0x40

Bit	7	6	5	4	3	2	1	0
Name	slow_slow					iscr_ted_gain	pll_speed_i	
Reset	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RW	slow_slow	Lower threshold for the OUTP RAM slow adjustment area
[2]	RW	iscr_ted_gain	Input stream time reference (ISCR) feedback coefficient

[1:0]	RW	pll_speed_i	ISCR feedback gain

OUTP_PLL3

OUTP_PLL3 is a PLL control register.

Offset Address	Register Name	Total Reset Value
0xA6	OUTP_PLL3	0xBF

Bit	7	6	5	4	3	2	1	0
Name	fast_high					auto_vol	pll_speed_r	
Reset	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:3]	RW	fast_high	Upper threshold for the OUTP RAM fast adjustment area
[2]	RW	auto_vol	De-jitter buffer (DJB) capacity configuration 1: The data PLP and common PLP capacities in the OUTP RAM are automatically configured. 0: The capacity is configured base on OUTP_DCAP_SET and OUTP_CCAP_SET.
[1:0]	RW	pll_speed_r	PLL speed when the ISCR is not active

OUTP_PLL4

OUTP_PLL4 is a PLL control register.

Offset Address	Register Name	Total Reset Value
0xA7	OUTP_PLL4	0x23

Bit	7	6	5	4	3	2	1	0
Name	fast_low					out_mode_auto	ted_shift	
Reset	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[7:3]	RW	fast_low	Lower threshold for the OUTP RAM fast adjustment area
[2]	RW	out_mode_auto	TS output mode auto select enable 1: enabled 0: disabled (The output mode is selected based on clk_mode and out_mode.)
[1:0]	RW	ted_shift	PLL feedback coefficient

OUTP_CLK_SET

OUTP_CLK_SET is an output clock configuration register.

Offset Address	Register Name	Total Reset Value
0xA8	OUTP_CLK_SET	0x00

Bit	7	6	5	4	3	2	1	0
Name	clk_div						clk_mode	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RW	clk_div	Integral part of the ratio of the system clock frequency to the I^2C configuration clock frequency
[1:0]	RW	clk_mode	TS output clock 00: PLL even clock 01: I^2C configuration clock 10: basic unit clock 11: reserved

OUTP_CLK_SETH

OUTP_CLK_SETH is an I^2C clock configuration register.

Offset Address	Register Name	Total Reset Value
0xA9	OUTP_CLK_SETH	0x00

Bit	7	6	5	4	3	2	1	0
Name	clk_div_fh							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	clk_div_fh	Upper eight bits of the decimal part of the ratio of the system clock frequency to the I^2C configuration clock frequency

OUTP_CLK_SETL

OUTP_CLK_SETL is an I^2C clock configuration register.

Offset Address	Register Name	Total Reset Value
0xAA	OUTP_CLK_SETL	0x00

Bit	7	6	5	4	3	2	1	0
Name	clk_div_fl							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	clk_div_fl	Lower eight bits of the decimal part of the ratio of the system clock frequency to the I^2C configuration clock frequency

OUTP_MODE_SET

OUTP_MODE_SET is an output mode configuration register.

Offset Address	Register Name	Total Reset Value
0xAB	OUTP_MODE_SET	0x10

Bit	7	6	5	4	3	2	1	0
Name	out_mode		ram_thres					serl_sync8
Reset	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	out_mode	TS output mode 00: TSs are output evenly. 01: TSs are output based on the I^2C configuration clock. 10: TSs are output based on the basic unit clock. 11: TSs are output if there is a complete packet.
[5:1]	RW	ram_thres	OUTP RAM output start threshold
[0]	RW	serl_sync8	TS sync header time length 1: The sync word occupies 8 bits in serial mode. 0: The sync word occupies 1 bit in 1-bit serial mode and 2 bits in 2-bit serial mode.

OUTP_TS_MODE

OUTP_TS_MODE is a TS output mode configuration register.

Offset Address	Register Name	Total Reset Value
0xAC	OUTP_TS_MODE	0x05

Bit	7	6	5	4	3	2	1	0
Name	wait_time			mask_clk	clk_inv	msb_1st	serl2	paral
Reset	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[7:5]	RW	wait_time	TS output wait time 000: 10 ms 001: 20 ms 010: 40 ms 011: 80 ms 100: 160 ms 101: 320 ms 110: 640 ms 111: 1000 ms
[4]	RW	mask_clk	TS output clock mask 1: masked when there is no TS 0: not masked
[3]	RW	clk_inv	TS clock edge select 1: The falling edge of the TS clock is between data. 0: The rising edge of the TS clock is between data.
[2]	RW	msb_1st	Serial output sequence 1: upper bits first 0: lower bits first
[1]	RW	serl2	Serial mode select (valid only when paral is 0) 1: 2-bit serial TS output 0: 1-bit serial TS output
[0]	RW	paral	Serial or parallel TS output 1: 8-bit parallel TS output 0: serial output

OUTP_PKT_STA

OUTP_PKT_STA is a TS packet count configuration register.

Offset Address	Register Name	Total Reset Value
0xAE	OUTP_PKT_STA	0x20

Bit	7	6	5	4	3	2	1	0
Name	sta_pkt_set							
Reset	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	sta_pkt_set	Number of packets to be counted when the initial TS rate is calculated

OUTP_LIMIT_EN

OUTP_LIMIT_EN is a limit and enable register.

Offset Address	Register Name	Total Reset Value
0xAF	OUTP_LIMIT_EN	0x64

Bit	7	6	5	4	3	2	1	0
Name	tei_en	ctrl_limit	iscr_limit	discard_num				
Reset	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[7]	RW	tei_en	Reset signal generation enable for the TS error flag bit 1: enabled 0: disabled
[6]	RW	ctrl_limit	PLL control word limit enable 1: limited to 32767 0: not limited
[5]	RW	iscr_limit	ISCR feedback processing 1: The ISCR feedback value is limited. 0: The ISCR feedback value is not limited.
[4:0]	RW	discard_num	Count reset threshold. The count restarts when error bits exist in the input baseband frames and the number of counted packets is less than this threshold.

PLP_CTRL

PLP_CTRL is a PLP control register.

Offset Address	Register Name	Total Reset Value
0xB0	PLP_CTRL	0x10

Bit	7	6	5	4	3	2	1	0
Name	reserved			post_static		reserved	common_plp	plp_read
Reset	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[7:5]	-	reserved	Reserved
[4:3]	RW	post_static	POST signaling track mode 0: The signaling changes in single PLP mode are dynamically traced. 1: The signaling changes are dynamically traced in single PLP mode when the static parameter in the L1 post signaling is 0. 2: The signaling changes are not traced in single PLP mode. 3: reserved
[2]	-	reserved	Reserved
[1]	RW	common_plp	Common PLP enable (valid only when common PLP exists). If the signals do not contain common PLP, this bit is fixed at 0.
[0]	RW	plp_read	PLP parameter read enable (valid only in Multi PLP mode) 1: Only difference PLP parameters are read. The PLP is not switched during demodulation. 0: PLPs are switched during demodulation.

PLP_ID0

PLP_ID0 is a data PLP ID register.

Offset Address	Register Name	Total Reset Value
0xB1	PLP_ID0	0x00

Bit	7	6	5	4	3	2	1	0
Name	data_plp_idx							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	data_plp_idx	Data PLP ID

PLP_ID1

PLP_ID1 is a common PLP ID register.

Offset Address	Register Name	Total Reset Value
0xB2	PLP_ID1	0x04

Bit	7	6	5	4	3	2	1	0
Name	common_plp_idx							
Reset	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[7:0]	RW	common_plp_idx	Common PLP ID

TPS

TPS is a signal parameter register.

Offset Address	Register Name	Total Reset Value
0xB3	TPS	0x00

Bit	7	6	5	4	3	2	1	0
Name	t_tps_ok	l1_pre_ok	bw_ext	gi_mode			t2_base_lite	l1_post_scr
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	t_tps_ok	Channel parameter check completion indicator for DVB-T signals
[6]	RO	l1_pre_ok	PRE signaling check completion indicator for DVB-T2 signals
[5]	RO	bw_ext	Bandwidth mode 1: extended bandwidth 0: common bandwidth
[4:2]	RO	gi_mode	Guard interval 000: 1/32 001: 1/16 010: 1/8 011: 1/4 100: 1/128 101: 19/128 110: 19/256 Other values: reserved
[1]	RO	t2_base_lite	T2_base_lite indicator (valid only when the standard V1.3.1 is used and the current signals are in Lite mode)

[0]	RO	l1_post_scr	Whether POST signaling is scrambled 1: scrambled 0: not scrambled

STREAM_TYPE

STREAM_TYPE is a data stream type indicator register.

Offset Address	Register Name	Total Reset Value
0xB4	STREAM_TYPE	0x00

Bit	7	6	5	4	3	2	1	0
Name	stream_type							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	stream_type	Type of DVB-T2 input data streams 0x00: TS 0x01: GS 0x02: TS and GS 0x03–0xFF: reserved

CODE_RATE_DVBT

CODE_RATE_DVBT is a DVB-T internal code rate register.

Offset Address	Register Name	Total Reset Value
0xB4	CODE_RATE_DVBT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					code_rate_l		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	-	reserved	Reserved

[2:0]	RO	code_rate_l	Code rate of streams with a low priority in DVB-T hierarchical mode or internal code in non-hierarchical mode 000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 Other values: reserved

TPS_DVBT

TPS_DVBT is a DVB-T signal parameter register.

Offset Address	Register Name	Total Reset Value
0xB5	TPS_DVBT	0x00

Bit	7	6	5	4	3	2	1	0
Name	mod		hier		indepth	code_rate		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	mod	Constellation 00: QPSK 01: 16QAM 10: 64QAM Other values: reserved
[5:4]	RO	hier	Hierarchical mode 00: non-hierarchical 01: alpha = 1 10: alpha = 2 11: alpha = 4
[3]	RO	indepth	Interleaving mode 1: indepth interleaving 0: normal interleaving

[2:0]	RO	code_rate_H	Code rate of streams with a high priority in DVB-T hierarchical mode or internal code in non-hierarchical mode 000: 1/2 001: 2/3 010: 3/4 011: 5/6 100: 7/8 Other values: reserved

PAPR_L1MOD

PAPR_L1MOD is a DVB-T2 PRE signaling register.

Offset Address	Register Name	Total Reset Value
0xB5	PAPR_L1MOD	0x00

Bit	7	6	5	4	3	2	1	0
Name	papr				l1_mod			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	papr	PAPR parameter
[3:0]	RO	l1_mod	POST signaling constellation 0000: BPSK 0001: QPSK 0010: 16QAM 0011: 64QAM Other values: reserved

PP_VERSION

PP_VERSION is a DVB-T2 PRE signaling register.

Offset Address	Register Name	Total Reset Value
0xB8	PP_VERSION	0x00

Bit	7	6	5	4	3	2	1	0
Name	pilotpattern				t2_version			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	pilotpattern	Pilot pattern 0000: PP1 0001: PP2 0010: PP3 0011: PP4 0100: PP5 0101: PP6 0110: PP7 0111: PP8 Other values: reserved
[3:0]	RO	t2_version	T2 standard version 0000: 1.1.1 0001: 1.2.1 0010: 1.3.1 Other values: reserved

NUM_T2_FRM

NUM_T2_FRM is a DVB-T2 PRE signaling register.

Offset Address	Register Name	Total Reset Value
0xB9	NUM_T2_FRM	0x00

Bit	7	6	5	4	3	2	1	0
Name	num_t2_frm							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	num_t2_frm	Number of T2 frames in each super frame of T2 signals

LDATA_L

LDATA_L is a DVB-T2 PRE signaling register.

Offset Address	Register Name	Total Reset Value
0xBA	LDATA_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	num_dat_sym_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	num_dat_sym_l	Lower bits of the signed number in each T2 frame

LDATA_H

LDATA_H is a DVB-T2 PRE signaling register.

Offset Address	Register Name	Total Reset Value
0xBB	LDATA_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				num_dat_sym_h			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3:0]	RO	num_dat_sym_h	Upper bits of the signed number in each T2 frame

NUM_PLP

NUM_PLP is a DVB-T2 PRE signaling register.

Offset Address	Register Name	Total Reset Value
0xBF	NUM_PLP	0x00

Bit	7	6	5	4	3	2	1	0
Name	num_plp							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	num_plp	Number of PLPs in T2 signals

PLP_ID

PLP_ID is a DVB-T2 POST signaling register.

Offset Address	Register Name	Total Reset Value
0xC6	PLP_ID	0x00

Bit	7	6	5	4	3	2	1	0
Name	plp_id							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	plp_id	ID of the currently selected PLP (specified by 0xB1)

PLP_TYPE

PLP_TYPE is a DVB-T2 POST signaling register.

Offset Address	Register Name	Total Reset Value
0xC7	PLP_TYPE	0x00

Bit	7	6	5	4	3	2	1	0
Name	plp_type			plp_pay_load				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	plp_type	Type of the currently selected PLP 000: common PLP 001: type 1 PLP 010: type 2 PLP Other values: reserved
[4:0]	RO	plp_pay_load	Payload of the currently selected PLP 00000: GFPS 00001: GCS 00010: GSE 00011: TS Other values: reserved

PLP_GRP_ID

PLP_GRP_ID is a DVB-T2 POST signaling register.

Offset Address	Register Name	Total Reset Value
0xC8	PLP_GRP_ID	0x00

Bit	7	6	5	4	3	2	1	0
Name	plp_grp_id							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	plp_grp_id	Group ID of the currently selected PLP

PLP_PARAM

PLP_PARAM is a DVB-T2 POST signaling register.

Offset Address	Register Name	Total Reset Value
0xC9	PLP_PARAM	0x00

Bit	7	6	5	4	3	2	1	0
Name	plp_cod			plp_mod			plp_rotation	plp_fec_type
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	plp_cod	LDPC code rate of the currently selected PLP Base mode 000: 1/2 001: 3/5 010: 2/3 011: 3/4 100: 4/5 101: 5/6 Other values: reserved Lite mode 000: 1/2 001: 3/5 010: 2/3 011: 3/4 110: 1/3 111: 2/5 Other values: reserved
[4:2]	RO	plp_mod	Constellation of the currently selected PLP 000: QPSK 001: 16QAM 010: 64QAM 011: 256QAM Other values: reserved
[1]	RO	plp_rotation	Constellation rotation mode of the currently selected PLP 0: standard constellation 1: rotated constellation
[0]	RO	plp_fec_type	FEC frame type of the currently selected PLP 0: 16K LDPC 1: 64K LDPC

ADC_CTRL0

ADC_CTRL0 is an ADC IP control register.

Offset Address	Register Name	Total Reset Value
0x00	ADC_CTRL0	0x41

Bit	7	6	5	4	3	2	1	0
Name	adi2c_en	adc_clk_on	adc_clk_sel					
Reset	0	1	0	0	0	0	0	1

Bits	Access	Name	Description
[7]	RW	adi2c_en	I^2C enable of the ADC (The I^2C of both the ADC and the tuner are mounted on the repeater.) When c_adi2c_en is 1, the repeater communicates with the ADC; when c_adi2c_en is 0, the repeater communicates with the tuner.
[6]	RW	adc_clk_on	ADC clock input enable 1: enabled 0: disabled
[5:0]	RW	adc_clk_sel	ADC clock select

ADC_CTRL1

ADC_CTRL1 is an ADC IP control register.

Offset Address	Register Name	Total Reset Value
0x01	ADC_CTRL1	0xC0

Bit	7	6	5	4	3	2	1	0
Name	adc_enavcmin	adi2c_resetz	adi2c_addr1	adi2c_addr0	pllout_sel	ts_testout	test_clk_en	i2c_xo_clk
Reset	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	adc_enavcmin	ADC common-mode voltage module enable 1: enabled 0: bypassed
[6]	RW	adi2c_resetz	0: reset the ADC module 1: deassert reset
[5]	RW	adi2c_addr1	I^2C address of the ADC
[4]	RW	adi2c_addr0	I^2C address of the ADC

[3]	RW	pllout_sel	0: normal mode 1: The fec_err/ts_err pin outputs frequency division signals of PLLs.
[2]	RW	ts_testout	0: normal mode 1: output test data
[1]	RW	test_clk_en	0: normal mode 1: internal PLL frequency division enable (fec_err/ts_err output can be selected by configuring c_pllout_sel)
[0]	RW	i2c_xo_clk	0: The I^2C works at the crystal oscillator clock. 1: The I^2C works at the clk_dem clock.

ADC_CTRL2

ADC_CTRL2 is an ADC IP control register.

Offset Address	Register Name	Total Reset Value
0x02	ADC_CTRL2	0x29

Bit	7	6	5	4	3	2	1	0
Name	adc_bctrl					adc_endoutz	adc_endcr	adc_chsel
Reset	0	0	1	0	1	0	0	1

Bits	Access	Name	Description
[7:3]	RW	adc_bctrl	Bias current control of the ADC. The default value is 0x05.
[2]	RW	adc_endoutz	0: output normal I/Q data 1: output 0
[1]	RW	adc_endcr	Duty cycle restorer enable 1: enabled (used only when the sampling rate fs is greater than or equal to 40 MHz) 0: disabled
[0]	RW	adc_chsel	Working mode of the ADC channel (by working with adc_ppsel) {adc_ppsel,adc_chsel} 00: single channel I 00: single channel Q 10: dual-channel I/Q interleaving 11: dual-channel independent In dual-channel mode, the frequency of the ADC input clock must be twice the sampling rate.

ADC_CTRL3

ADC_CTRL3 is an ADC IP control register.

Offset Address	Register Name	Total Reset Value
0x03	ADC_CTRL3	0x01

Bit	7	6	5	4	3	2	1	0
Name	adc_ppsel	adc_prevf	adc_opm		adc_bcal		adc_startcal	adc_selof
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7]	RW	adc_ppsel	See the description of adc_chsel.
[6]	RW	adc_prevf	ADC auto calibration module enable 0: enabled 1: disabled
[5:4]	RW	adc_opm	ADC operating mode 00: power down 01/10: standby 11: normal
[3:2]	RW	adc_bcal	ADC background calibration control
[1]	RW	adc_startcal	ADC start calibration
[0]	RW	adc_selof	0: ADC sign-and-magnitude output 1: ADC two's complement output

ADC_FSCTRL

ADC_FSCTRL is an ADC IP control register.

Offset Address	Register Name	Total Reset Value
0x04	ADC_FSCTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	adc_fsctrl							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	adc_fsctrl	ADC output digital gain Gain = 1 + adc_fsctrl/256

PLL_LOCK

PLL_LOCK is a PLL lock indicator register.

Offset Address	Register Name	Total Reset Value
0x05	PLL_LOCK	0x00

Bit	7	6	5	4	3	2	1	0
Name	pll1_lock	pll0_lock	adc_rflagi			adc_rflagq		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	pll1_lock	PLL1 lock indicator 1: locked 0: unlocked
[6]	RO	pll0_lock	PLL0 lock indicator 1: locked 0: unlocked
[5:3]	RO	adc_rflagi	Overflow flag of channel I input signals of the ADC
[2:0]	RO	adc_rflagq	Overflow flag of channel Q input signals of the ADC

PLL0_FRAC_L

PLL0_FRAC_L is a PLL0 frequency divider decimal part low register.

Offset Address	Register Name	Total Reset Value
0x06	PLL0_FRAC_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	pll0_frac_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	pll0_frac_l	LSB of the decimal part of the PLL0 feedback divider

PLL0_PD

PLL0_PD is a PLL0 power down control register.

Offset Address	Register Name	Total Reset Value
0x07	PLL0_PD	0x40

Bit	7	6	5	4	3	2	1	0
Name	pll0_foutpostdivpd	pll0_fout4phasepd	pll0_foutvcopd	pll0_pd	pll0_frac_h			
Reset	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	pll0_foutpostdivpd	PLL0 foutpostdiv power down 1: power down 0: power on
[6]	RW	pll0_fout4phasepd	PLL0 fout4phase power down 1: power down 0: power on
[5]	RW	pll0_foutvcopd	PLL0 foutvco power down 1: power down 0: power on
[4]	RW	pll0_pd	PLL0 power down 1: power down 0: power on
[3:0]	RW	pll0_frac_h	MSB of the decimal part of the PLL0 feedback divider

PLL0_POSTDIV

PLL0_POSTDIV is a PLL0 post divider configuration register.

Offset Address	Register Name	Total Reset Value
0x08	PLL0_POSTDIV	0x11

Bit	7	6	5	4	3	2	1	0
Name	pll0_dsmpd	pll0_dacpd	pll0_postdiv2			pll0_postdiv1		
Reset	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[7]	RW	pll0_dsmpd	PLL0 down Delta-Sigma modulator power down 1: power down 0: power on

[6]	RW	pll0_dacpd	PLL0 noise cancellation DAC power down 1: power down 0: power on
[5:3]	RW	pll0_postdiv2	PLL0 post divider 2
[2:0]	RW	pll0_postdiv1	PLL0 post divider 1

PLL0_FBDIV

PLL0_FBDIV is a PLL0 feedback divider register.

Offset Address	Register Name	Total Reset Value
0x09	PLL0_FBDIV	0x20

Bit	7	6	5	4	3	2	1	0
Name	pll0_fbdiv							
Reset	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	pll0_fbdiv	PLL0 feedback divider

PLL0_REFDIV

PLL0_REFDIV is a PLL0 reference divider register.

Offset Address	Register Name	Total Reset Value
0x0A	PLL0_REFDIV	0x01

Bit	7	6	5	4	3	2	1	0
Name	adc_rdy	pll0_bypass	pll0_refdiv					
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7]	RO	adc_rdy	Indication of the ADC working state 1: ready 0: not ready
[6]	RW	pll0_bypass	PLL0 bypass 1: bypassed 0: normal mode
[5:0]	RW	pll0_refdiv	PLL0 reference divider

PLL0_SPREAD

PLL0_SPREAD is a PLL0 spread spectrum mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0B	PLL0_SPREAD	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved	pll0_spread			pll0_downspread	pll0_disable_sscg	pll0_rst_req	pll0_cken
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7]	-	reserved	Reserved
[6:4]	RW	pll0_spread	PLL0 spectrum spread mode select
[3]	RW	pll0_downspread	PLL0 downspread mode select
[2]	RW	pll0_disable_sscg	PLL0 synchronization clock gate enable
[1]	RW	pll0_rst_req	PLL0 spectrum spread mode reset 1: reset 0: deassert reset
[0]	RW	pll0_cken	PLL0 spectrum spread mode clock enable 1: enabled 0: disabled

PLL_DIVVAL

PLL_DIVVAL is a PLL spread spectrum mode output divider control register.

Offset Address	Register Name	Total Reset Value
0x0C	PLL_DIVVAL	0x00

Bit	7	6	5	4	3	2	1	0
Name	pll1_divval				pll0_divval			
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RW	pll1_divval	VCO output divider of the PLL1 spectrum spread mode
[3:0]	RW	pll0_divval	VCO output divider of the PLL0 spectrum spread mode

PLL1_FRAC_L

PLL1_FRAC_L is a PLL1 frequency divider decimal part low register.

Offset Address	Register Name	Total Reset Value
0x0D	PLL1_FRAC_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	pll1_frac_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	pll1_frac_l	LSB of the decimal part of the PLL1 feedback divider

PLL1_PD

PLL1_PD is a PLL1 power down control register.

Offset Address	Register Name	Total Reset Value
0x0E	PLL1_PD	0x48

Bit	7	6	5	4	3	2	1	0
Name	pll1_foutpostdivpd	pll1_fout4phasepd	pll1_foutvcopd	pll1_pd	pll1_frac_h			
Reset	0	1	0	0	1	0	0	0

Bits	Access	Name	Description
[7]	RW	pll1_foutpostdivpd	PLL1 foutpostdiv power down 1: power down 0: power on
[6]	RW	pll1_fout4phasepd	PLL1 fout4phase power down 1: power down 0: power on
[5]	RW	pll1_foutvcopd	PLL1 foutvco power down 1: power down 0: power on
[4]	RW	pll1_pd	PLL1 power down 1: power down 0: power on
[3:0]	RW	pll1_frac_h	MSB of the decimal part of the PLL1 feedback divider

PLL1_POSTDIV

PLL1_POSTDIV is a PLL1 post divider configuration register.

Offset Address	Register Name	Total Reset Value
0x0F	PLL1_POSTDIV	0x12

Bit	7	6	5	4	3	2	1	0
Name	pll1_dsmpd	pll1_dacpd	pll1_postdiv2			pll1_postdiv1		
Reset	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[7]	RW	pll1_dsmpd	PLL1 down Delta-Sigma modulator power down 1: power down 0: power on
[6]	RW	pll1_dacpd	PLL1 noise cancellation DAC power down 1: power down 0: power on
[5:3]	RW	pll1_postdiv2	PLL1 post divider 2
[2:0]	RW	pll1_postdiv1	PLL1 post divider 1

PLL1_FBDIV

PLL1_FBDIV is a PLL1 feedback divider register.

Offset Address	Register Name	Total Reset Value
0x10	PLL1_FBDIV	0x19

Bit	7	6	5	4	3	2	1	0
Name	pll1_fbdiv							
Reset	0	0	0	1	1	0	0	1

Bits	Access	Name	Description
[7:0]	RW	pll1_fbdiv	PLL1 feedback divider

PLL1_REFDIV

PLL1_REFDIV is a PLL1 reference divider register.

Offset Address	Register Name	Total Reset Value
0x11	PLL1_REFDIV	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved	pll1_bypass	pll1_refdiv					
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7]	-	reserved	Reserved
[6]	RW	pll1_bypass	PLL1 bypass 1: bypassed 0: normal mode
[5:0]	RW	pll1_refdiv	PLL1 reference divider

PLL1_SPREAD

PLL1_SPREAD is a PLL1 spread spectrum mode configuration register.

Offset Address	Register Name	Total Reset Value
0x12	PLL1_SPREAD	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved	pll1_spread			pll1_downspread	pll1_disable_sscg	pll1_rst_req	pll1_cken
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7]	-	reserved	Reserved
[6:4]	RW	pll1_spread	PLL1 spectrum spread mode select
[3]	RW	pll1_downspread	PLL1 downspread mode select
[2]	RW	pll1_disable_sscg	PLL1 synchronization clock gate enable
[1]	RW	pll1_rst_req	PLL1 spectrum spread mode reset 1: reset 0: deassert reset
[0]	RW	pll1_cken	PLL1 spectrum spread mode clock enable 1: enabled 0: disabled

IO_CTRL0

IO_CTRL0 is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x13	IO_CTRL0	0x00

Bit	7	6	5	4	3	2	1	0
Name	ts_sync_sl	ts_sync_ds			ts_data_sl	ts_data_ds		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	ts_sync_sl	ts_sync I/O speed control 1: high speed 0: low speed
[6:4]	RW	ts_sync_ds	ts_sync I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA
[3]	RW	ts_data_sl	ts_data I/O speed 1: high speed 0: low speed
[2:0]	RW	ts_data_ds	ts_data I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA

IO_CTRL1

IO_CTRL1 is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x14	IO_CTRL1	0x00

Bit	7	6	5	4	3	2	1	0
Name	ts_err_sl	ts_err_ds			ts_vld_sl			ts_vld_ds
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	ts_err_sl	ts_err I/O speed 1: high speed 0: low speed
[6:4]	RW	ts_err_ds	ts_err I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA
[3:1]	RW	ts_vld_sl	ts_vld I/O speed 1: high speed 0: low speed
[0]	RW	ts_vld_ds	ts_vld I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA

IO_CTRL2

IO_CTRL2 is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x15	IO_CTRL2	0x00

Bit	7	6	5	4	3	2	1	0
Name	clkout_sl	clkout_ds			ts_clk_sl	ts_clk_ds		
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RW	clkout_sl	clkout I/O speed 1: high speed 0: low speed
[6:4]	RW	clkout_ds	clkout I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA
[3]	RW	ts_clk_sl	ts_clk I/O speed 1: high speed 0: low speed
[2:0]	RW	ts_clk_ds	ts_clk I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA

IO_CTRL3

IO_CTRL3 is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x16	IO_CTRL3	0xC0

Bit	7	6	5	4	3	2	1	0
Name	sdc_clk_sel			fec_err_hiz	fec_err_sl	fec_err_ds		
Reset	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RW	sdc_clk_sel	SDC clock phase
[4]	RW	fec_err_hiz	fec_err I/O output mode 1: high impedance 0: normal mode
[3]	RW	fec_err_sl	fec_err I/O speed 1: high speed 0: low speed
[2:0]	RW	fec_err_ds	fec_err I/O driving current 000: 4 mA 001: 7 mA 010: 10 mA 011: 12 mA 100: 14 mA 101: 16 mA 110: 18 mA 111: 20 mA

IO_CTRL4

IO_CTRL4 is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x17	IO_CTRL4	0x00

Bit	7	6	5	4	3	2	1	0
Name	lock_sel		lock_val	clkout_sel		clkout_hiz	lock_hiz	ts_hiz
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	lock_sel	Lock pin output signal select 00: Demod lock indicator 01: TXD 10: future extension frame (FEF) part indicator 11: lock_val value
[5]	RW	lock_val	Lock pin output signal
[4:3]	RW	clkout_sel	clkout I/O output signal 00: crystal oscillator clock 01: FEF part indicator 10: Demod lock indicator 11: gpio_val value
[2]	RW	clkout_hiz	clkout I/O output mode 1: high impedance 0: normal mode
[1]	RW	lock_hiz	Lock I/O output mode 1: high impedance 0: normal mode
[0]	RW	ts_hiz	TS I/O output mode 1: high impedance 0: normal mode

SDR_CTRL

SDR_CTRL is an SDR control register.

Offset Address	Register Name	Total Reset Value
0x18	SDR_CTRL	0x24

Bit	7	6	5	4	3	2	1	0
Name	sdr_dq_sl	sdr_dq_ds		sdr_addr_sl	sdr_addr_ds		sdr_etron	gpio_val
Reset	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[7]	RW	sdr_dq_sl	sdr_dq I/O speed 1: high speed 0: low speed
[6:5]	RW	sdr_dq_ds	sdr_dq I/O driving current 00: 4 mA 01: 7 mA 10: 10 mA 11: 12 mA
[4]	RW	sdr_addr_sl	sdr_addr I/O speed 1: high speed 0: low speed
[3:2]	RW	sdr_addr_ds	sdr_addr I/O driving current 00: 4 mA 01: 7 mA 10: 10 mA 11: 12 mA
[1]	RW	sdr_etron	Packaged SDRAM select 1: Etron 0: Winbond
[0]	RW	gpio_val	GPIO output signal control

Contents

Figures

Tables

3 Hardware Design

3.1 Package and Pins

3.1.1 Package and Pinout

Package

Hi3137 V100 uses the mapped quad flat non-leaded (MQFN) package. It has 48 pins, its body size is 6 mm x 6 mm (0.24 in. x 0.24 in.), and its lead pitch is 0.4 mm (0.02 in.). Figure 3-1 shows the package views. Figure 3-2 shows package dimensions.

Figure 3-1 Package views

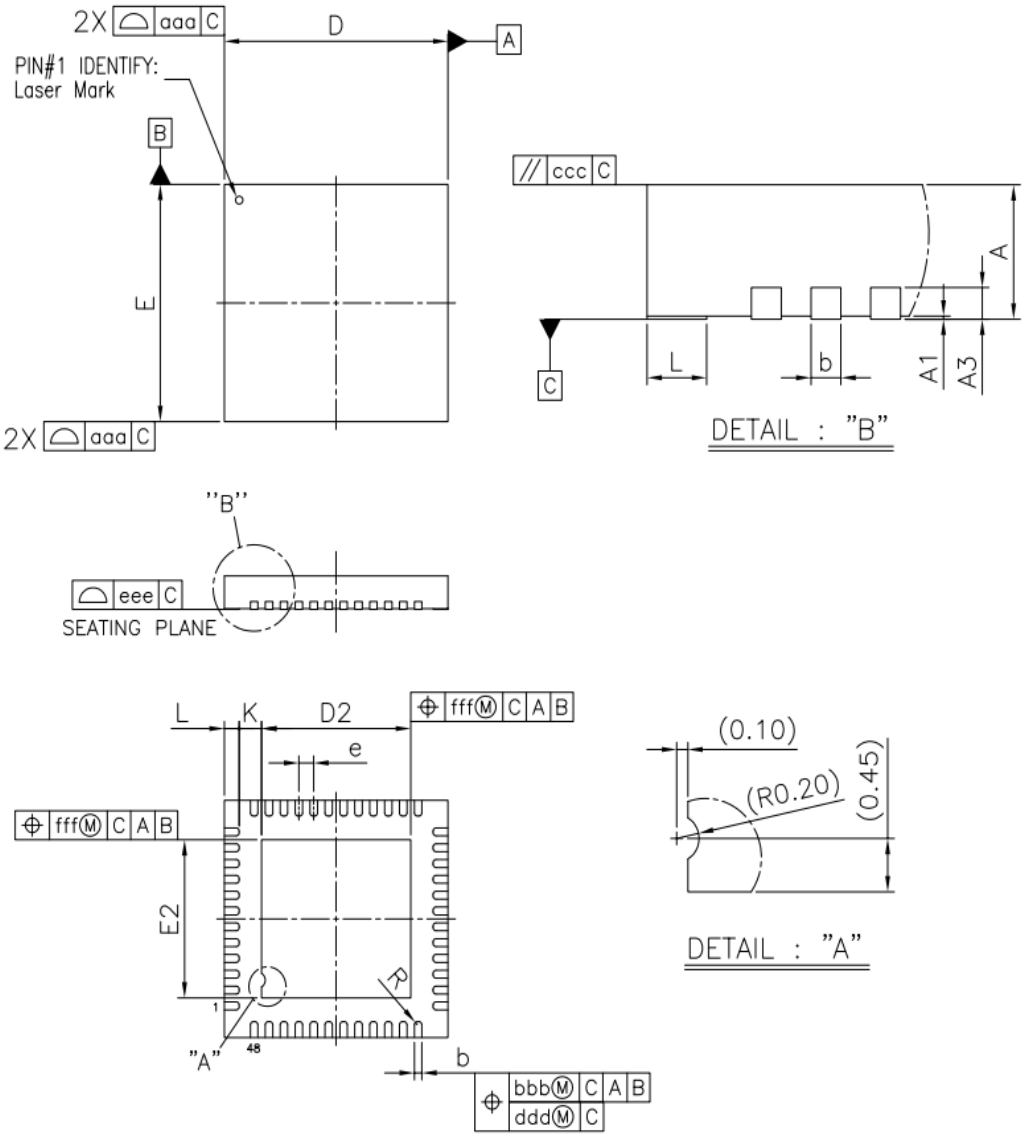


Figure 3-2 Package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	3.85	4.00	4.15	0.152	0.157	0.163
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

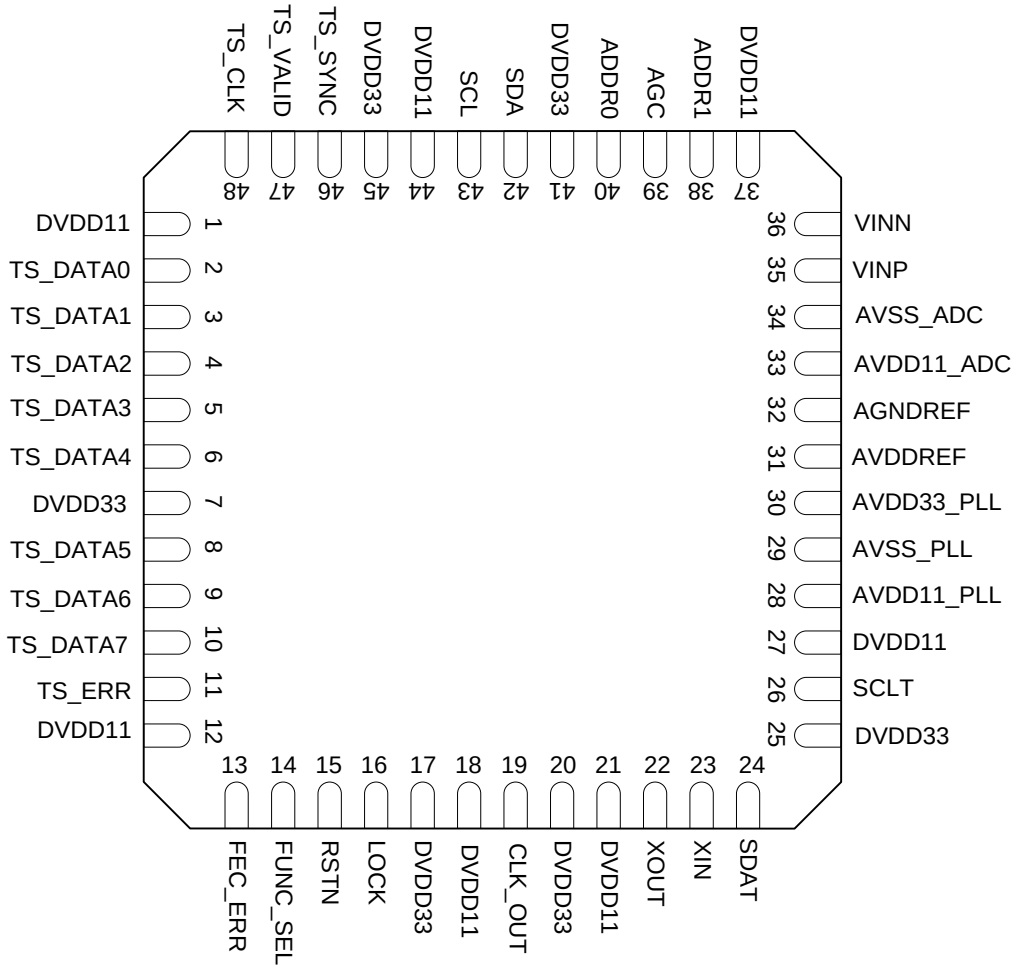
NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Pin Map

Figure 3-3 shows the pin map.

Figure 3-3 Pin map



3.1.2 Pin Descriptions

Pin Arrangement

Table 3-1 lists the pins of Hi3137 V100 in order.

Table 3-1 Pin arrangement

Position	Pin Name	Position	Pin Name
1	DVDD11	25	DVDD33
2	TS_DATA0	26	SCLT
3	TS_DATA1	27	DVDD11
4	TS_DATA2	28	AVDD11_PLL

Position	Pin Name	Position	Pin Name
5	TS_DATA3	29	AVSS_PLL
6	TS_DATA4	30	AVDD33_PLL
7	DVDD33	31	AVDDREF
8	TS_DATA5	32	AGNDREF
9	TS_DATA6	33	AVDD11_ADC
10	TS_DATA7	34	AVSS_ADC
11	TS_ERR	35	VINP
12	DVDD11	36	VINN
13	FEC_ERR	37	DVDD11
14	FUNC_SEL	38	ADDR1
15	RSTN	39	AGC
16	LOCK	40	ADDR0
17	DVDD33	41	DVDD33
18	DVDD11	42	SDA
19	CLK_OUT	43	SCL
20	DVDD33	44	DVDD11
21	DVDD11	45	DVDD33
22	XOUT	46	TS_SYNC
23	XIN	47	TS_VALID
24	SDAT	48	TS_CLK

Pin Types

Table 3-2 describes the I/O pin types.

Table 3-2 I/O pin types

I/O	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with a Schmitt trigger
I_{SPD}	Input signal with a Schmitt trigger, internal pull-down

I/O	Description
I_{SPU}	Input signal with a Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with a Schmitt trigger, input pull-up
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with a Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with a Schmitt trigger and output OD
XIN	Crystal oscillator input
XOUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

ADC Pins

Table 3-3 describes ADC pins.

Table 3-3 ADC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
34	AVSS_ADC	G	-	-	ADC GND
33	AVDD11_ADC	P	-	1.1	1.1 V ADC power
35	VINP	I	-	1.1	ADC differential input. The peak voltage in both differential input and single-end input modes is 1 Vpp.
36	VINN	I	-	1.1	ADC differential input. The peak voltage in both differential input and single-end input modes is 1 Vpp.

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
32	AGNDREF	I	-	-	ADC negative reference signal, which connects to a 22 Ω resistor in serial and then to GND
31	AVDDREF	I	-	1.1	ADC positive reference signal, which connects to the 1.1 V analog power

I²C Pins

Table 3-4 lists the I²C pins.

Table 3-4 I²C pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
40	ADDR0	I	3	3.3	Hi3137 V100 device address 0
38	ADDR1	I	3	3.3	Hi3137 V100 device address 1
26	SCLT	O_{OD}	3	3.3/5	I²C bus clock output, OD. This pin controls the tuner communication interface. It must connect to a pull-up resistor and then to the 3.3 V or 5 V power. The power voltage depends on the I²C level of the tuner.
24	SDAT	I_S/O_{OD}	3	3.3/5	I²C bus data output, OD. This pin controls the tuner communication interface. It must connect to an external pull-up resistor and then to the 3.3 V or 5 V power. The power voltage depends on the I²C level of the tuner.
43	SCL	I_S	3	3.3	Clock input bus of the I²C bus. This pin must connect to an external pull-up resistor and then to the 3.3 V power.
42	SDA	I_S/O_{OD}	3	3.3	Data bus of the I²C bus, OD output. This pin must connect to an external pull-up resistor and then to the 3.3 V power.

AGC and TS Pins

Table 3-5 describes TS pins.

Table 3-5 TS pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
39	AGC	O_{OD}	8	3.3/5	AGC output, OD. This pin is used to control the tuner gain and can connect to a pull-up resistor and then to the 3.3 V or 5 V power.
48	TS_CLK	O	4	3.3	TS clock of the Demod output
2	TS_DATA0	O	4	3.3	TS_DATA0 Demod data output
3	TS_DATA1	O	4	3.3	TS_DATA1 Demod data output
4	TS_DATA2	O	4	3.3	TS_DATA2 Demod data output
5	TS_DATA3	O	4	3.3	TS_DATA3 Demod data output
6	TS_DATA4	O	4	3.3	TS_DATA4 Demod data output
8	TS_DATA5	O	4	3.3	TS_DATA5 Demod data output
9	TS_DATA6	O	4	3.3	TS_DATA6 Demod data output
10	TS_DATA7	O	4	3.3	TS_DATA7 Demod data output
11	TS_ERR	O	4	3.3	TS_ERR TS error indicator
46	TS_SYNC	O	4	3.3	TS_SYNC Demod sync signal output
47	TS_VALID	O	4	3.3	TS_VALID Demod output data validity indicator, active high

PLL Pins

Table 3-6 describes PLL pins.

Table 3-6 PLL pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
28	AVDD11_PLL	P	-	1.1	1.1 V PLL analog power
30	AVDD33_PLL	P	-	3.3	3.3 V PLL analog power
29	AVSS_PLL	G	-	-	PLL analog GND

OSC Pins

Table 3-7 describes oscillator (OSC) pins.

Table 3-7 OSC pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
19	CLK_OUT	O	4	3.3	Loop-through output of the crystal oscillator clock
23	XIN	I	-	3.3	Crystal oscillator input
24	XOUT	O	-	3.3	Crystal oscillator output

PG Pins

Table 3-8 describes power/ground (PG) pins.

Table 3-8 PG pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
7, 17, 20, 25, 41, 45	DVDD33	P	-	3.3	3.3 V I/O power
1, 12, 18, 21, 27, 37, 44	DVDD11	P	-	1.1	1.1 V core power

SYS Pins

Table 3-9 describes system (SYS) pins.

Table 3-9 SYS pins

Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
14	FUNC_SEL	I_{SPD}	8	3.3	Mode select 0: functional mode 1: reserved
15	RSTN	I_{SPU}	8	3.3	System reset signal input, active low
16	LOCK	O	4	3.3	System lock indicator
13	FEC_ERR	O	4	3.3	System bit error indicator

3.1.3 Summary of I/O Function Configuration Registers

Table 3-10 describes the I/O function configuration registers.

Table 3-10 I/O function configuration registers (base address: 0x00)

Register	Offset Address	Description	Page
IO_CTRL4	0x17	I/O control register	3-10
SDR_CTRL	0x18	I/O control register	3-11

3.1.4 Description of I/O Function Configuration Registers

IO_CTRL4

IO_CTRL4 is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x17	IO_CTRL4	0x00

Bit	7	6	5	4	3	2	1	0
Name	lock_sel		lock_val	clkout_sel		clkout_hiz	lock_hiz	ts_hiz
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RW	lock_sel	Lock pin output signal select 00: Demod lock indicator 01: TXD 10: FEF part indicator 11: lock_val value
[5]	RW	lock_val	Programmable output level of the lock pin
[4:3]	RW	clkout_sel	CLK_OUT pin output signal select 00: crystal oscillator clock 01: FEF part indicator 10: Demod lock indicator 11: gpio_val value
[2]	RW	clkout_hiz	CLK_OUT I/O output mode 1: high impedance 0: normal mode
[1]	RW	lock_hiz	LOCK I/O output mode 1: high impedance 0: normal mode
[0]	RW	ts_hiz	TS I/O output mode 1: high impedance 0: normal mode

SDR_CTRL

SDR_CTRL is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x18	SDR_CTRL	0x24

Bit	7	6	5	4	3	2	1	0
Name	reserved							gpio_val
Reset	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[0]	RW	gpio_val	Programmable output level of the CLK_OUT pin. The output high level V_{OH} ranges from 2.7 V to 3.3 V, and the output low level V_{OL} is less than or equal to 0 V.

3.1.5 Software Multiplexed Pins

Table 3-11 describes the software multiplexed pins LOCK and CLK_OUT.

Table 3-11 Software multiplexed pins LOCK and CLK_OUT

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3
16	LOCK	IO_CTRL4	LOCK	TXD	FEF	GPO
19	CLK_OUT	SDR_CTRL	XO	FEF	LOCK	GPO

Table 3-12 describes the pin multiplexing signals.

Table 3-12 Pin multiplexing signals

Signal	Direction	Description
LOCK	O	Channel lock indicator
TXD	O	Serial output
FEF	O	FEF indicator
GPO	O	Programmable output
XO	O	Crystal oscillator clock
FEF	O	FEF indicator
LOCK	O	Channel lock indicator
GPO	O	Programmable output

3.2 Electrical Specifications

3.2.1 Power Consumption Specifications

Table 3-13 describes the power consumption specifications.

Table 3-13 Power consumption specifications

Symbol	Description	Min	Typ	Max	Unit
DVDD33	3.3 V (I/O) power	-	50	60	mA
AVDD33_PLL	3.3 V PLL analog power	-	3	5	mA
DVDD11	1.1 V core voltage	-	150	300	mA
AVDD11_ADC	1.1 V ADC power	-	7	15	mA
AVDD11_PLL	1.1 V PLL analog power	-	1	3	mA
AVDDREF	1.1 V ADC reference power		1	3	mA

3.2.2 Rated Working Conditions

WARNING

Hi3137 V100 may be unstable or damaged when working beyond the rated working conditions listed in Table 3-14.

Table 3-14 describes rated working conditions.

Table 3-14 Rated working conditions

Symbol	Description	Min	Max	Unit
T_{OPT}	Operating temperature	–40	125	ºC
T_{STG}	Storage temperature	–65	150	ºC
VI	Input voltage	–0.5	4.6	V
VO	Output voltage	–0.5	4.6	V
DVDD11	Internal core voltage	–0.5	1.8	V
DVDD33	I/O power	–0.5	4.6	V

3.2.3 Recommended Working Conditions

Table 3-15 describes the recommended working conditions.

Table 3-15 Recommended working conditions

Symbol	Description	Min	Typ	Max	Unit
T_{OPT}	Operating temperature	0	25	70	ºC
DVDD11	Internal core voltage	1.045	1.1	1.155	V
DVDD33	I/O power	2.97	3.3	3.63	V
AVDD33_PLL	PLL power	2.97	3.3	3.63	V
AVDD11_PLL	PLL power	1.045	1.1	1.155	V
AVDD11_ADC	ADC power	1.045	1.1	1.155	V
AVDDREF	1.1 V ADC reference power	1.045	1.1	1.155	V

3.2.4 Power-On and Power-Off Sequences

The power-on and power-off sequences are not restricted for the 3.3 V and 1.1 V power supplies.

3.2.5 DC Electrical Specifications

Table 3-16 describes the DC electrical specifications.

Table 3-16 DC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{IH}	Input high voltage	2.0	-	DVDD33 + 0.3	V	The 5 V tol is not supported.
V_{IL}	Input low voltage	–0.3	-	0.8	V	-
I_L	Input leakage current	-	-	±10	µA	-
I_{OZ}	Tri-state output leakage current	-	-	±10	µA	-
V_{OH}	Output high voltage	2.4	-	-	V	-
V_{OL}	Output low voltage	-	-	0.4	V	-
R_{PU}	Internal pull-up resistor	27	40	64	kΩ	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
R_{PD}	Internal pull-down resistor	31	46	78	kΩ	-

3.3 Design Recommendations for Schematic Diagrams

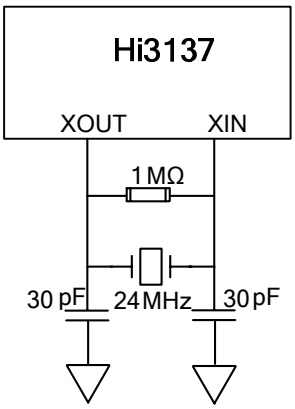
3.3.1 Design Recommendations for the Small System

3.3.1.1 Clocking Circuit

The system clock can be generated by combining the internal feedback circuit of Hi3137 V100 with an external 24 MHz (recommended) crystal oscillator circuit. ESR_{max} is 40 Ω and C_L is 20 pF.

Figure 3-4 shows the recommended connection mode of the crystal oscillator and the component specifications.

Figure 3-4 Recommended connection mode of the crystal oscillator



The following formula is used to calculate the capacitance of the internal load capacitor in the crystal oscillator and external capacitors:

$C_L = C1 \times C2/(C1 + C2) + C$

- C indicates the internal capacitor in the IC. Its capacitance is 5−7 pF.
- C1 and C2 each are 30 pF each in Figure 3-4.
- C_L is the load capacitor in the crystal oscillator. Its capacitance is 20−22 pF. The specific value provided by the vendor prevails.

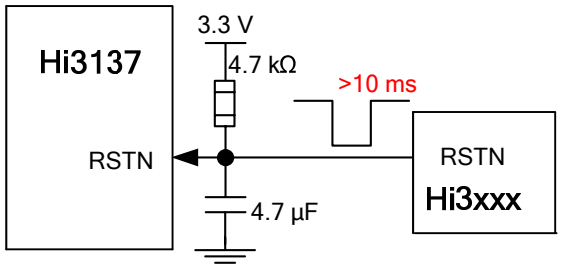
3.3.1.2 Reset Circuit

The Hi3137 V100 RSTN pin is a reset signal input pin. The valid reset signal must have low-level ($V_{IL} \leq 0.8$ V) pulse and the pulse width must be greater than 12 cycles of the clock input from the XIN pin. The pulse width of the reset signal ranges from 10 ms to 100 ms in general.

During the board design, the RC power-on reset circuit is recommended for the RSTN pin. That is, the RSTN pin connects to a 4.7 kΩ pull-up resistor and then to the 3.3 V power. In addition, the RSTN pin connects to a 4.7 µF capacitor and then to GND. This connection mode implements power-on reset. The RSTN pin can also connect to an STB decoder master chip. The master chip generates a reset signal complying with protocols in normal mode. If an exception occurs, the GPIO pin of the master chip generates a low-level pulse to trigger a soft reset.

Figure 3-5 shows the typical reset circuit.

Figure 3-5 Typical reset circuit



3.3.1.3 System Configuration Circuit for Hardware Initialization

The system configuration circuit for hardware initialization initializes internal registers over the I^2C bus. The I^2C addresses for Hi3137 V100 are set by configuring the external ADDR0 and ADDR1.

Table 3-17 and Table 3-18 describe address configurations.

Table 3-17 Address configurations 1

ADDR1	ADDR0	7-bit Address							R/W Bit	Write Address (in Hex)
		MSB						LSB		
Low	Low	1	0	1	1	1	0	0	0	0xB8
Low	High	1	0	1	1	1	0	1	0	0xBA
High	Low	1	0	1	1	1	1	0	0	0xBC
High	High	1	0	1	1	1	1	1	0	0xBE

Table 3-18 Address configurations 2

ADDR1	ADDR0	7-bit Address							R/W Bit	Read Address (in Hex)
		MSB						LSB		
Low	Low	1	0	1	1	1	0	0	1	0xB9
Low	High	1	0	1	1	1	0	1	1	0xBB
High	Low	1	0	1	1	1	1	0	1	0xBD

High	High	1	0	1	1	1	1	1	1	0xBF

3.3.1.4 Circuits for Digital/Analog Signal Interfaces

Introduction

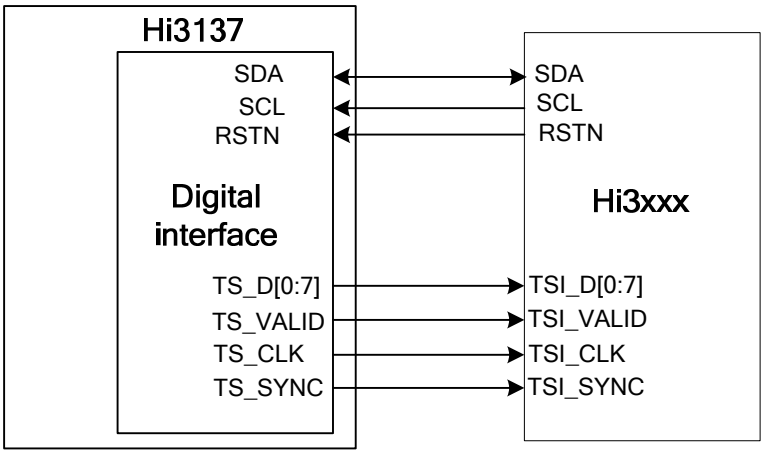
The level standard of digital interfaces is LVCMOS33. Hi3137 V100 provides the following digital interfaces:

- One TS serial/parallel interface (configurable serial/parallel working mode)
  - In 1-bit serial mode, the maximum clock frequency is 76.5 MHz, and the bit width is 1 bit.
  - In 2-bit serial mode, the maximum clock frequency is 36 MHz, and the bit width is 2 bits.
  - In parallel mode, the maximum clock frequency is 9 MHz, and the bit width is 8 bits.
- One I^2C interface with the maximum I^2C working frequency of 400 kHz. This interface is used to access the internal registers of Hi3137 V100 and the I^2C forwarding control tuner.
- One AGC output interface. This interface is used to control the gain of the front-end tuner in PWM or PDM (default) modulation mode by using an RC low-pass filtering circuit.
- One RSTN. A reset can be performed by using a hardware RC circuit or an STB decoder chip. The RSTN signal is active low.

TS Topologies

Figure 3-6 shows the typical topology when Hi3137 V100 connects to an external STB decoder chip in parallel. Figure 3-7 shows the typical topology when Hi3137 V100 connects to an external STB decoder chip in serial.

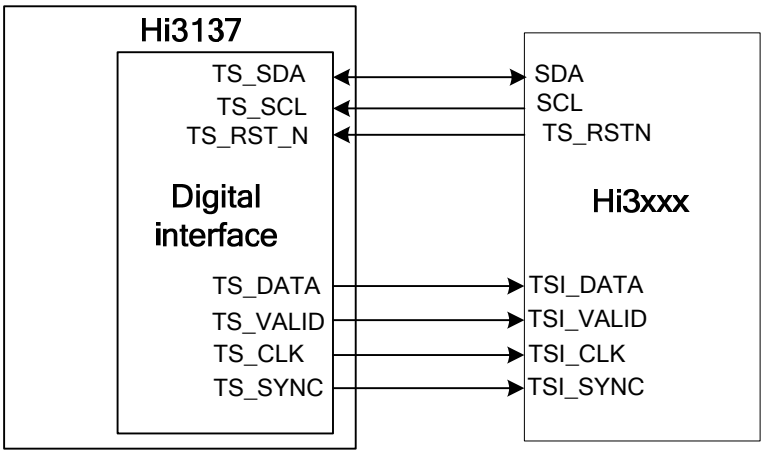
Figure 3-6 Topology when Hi3137 V100 connects to an STB decoder chip in parallel



NOTE

All TS output pins except TS_CLK in the TS parallel interface can be configured based on the actual layout.

Figure 3-7 Topology when Hi3137 V100 connects to an STB decoder chip in serial



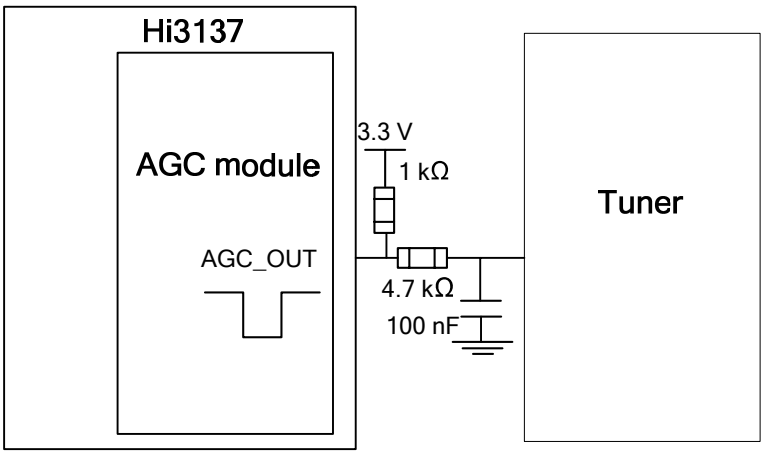
NOTE

All TS output pins except TS_CLK in the TS serial interface can be configured based on the actual layout.

AGC Topology

The AGC module converts digital signals into analog signals in PDM output mode (or PWM output mode by configuring internal registers) by using an external RC low-pass filter and automatically controls the gain of the front-end tuner when the external environment changes. This ensures signal quality. During the PCB layout design, the RC filtering circuit needs to be placed close to the AGC output pin of Hi3137 V100, preventing interference to analog RF from the high-frequency component of the AGC. Figure 3-8 shows the topology when the AGC interface connects to a tuner.

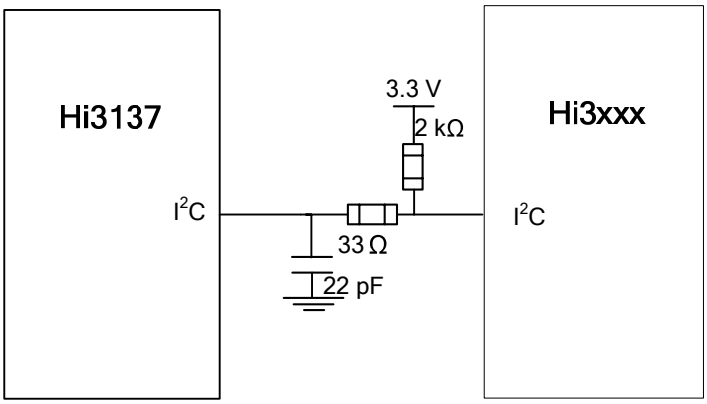
Figure 3-8 Topology when the AGC interface connects to a tuner



I²C Bus

The I²C bus between Hi3137 V100 and an STB decoder chip must connect to a 2 kΩ pull-up resistor and then to the 3.3 V power. In addition, bypass filtering capacitors (less than or equal to 100 pF) must be connected on the I²C bus close to the Hi3137 I²C pin. See Figure 3-9.

Figure 3-9 Topology when the I²C interface of Hi3137 V100 connects to an STB decoder chip



TS Matching Design

The TS matching design is provided based on the number of PCB layers:

- If more than two PCB layers are designed, the trace characteristic impedance is 50 Ω.
  - TS_OUT[0:7] connect to a 33 Ω resistor in serial. For details about the topology, see Figure 3-10.
  - TS_CLK, TS_SYNC, and TS_VALID connect to a 33 Ω resistor in serial. For details about the topology, see Figure 3-11.
- If two PCB layers are designed, the trace characteristic impedance is 140 Ω.
  - TS_OUT[0:7] connect to a 75 Ω resistor in serial. For details about the topology, see Figure 3-12.
  - TS_CLK, TS_VALID, and TS_SYNC connect to a 75 Ω resistor in serial. For details about the topology, see Figure 3-13.

NOTE

The maximum trace length is 4500 mils.

Figure 3-10 Interconnection topology of TS_OUT[0:7] and an STB decoder chip when the number of PCB layers is greater than 2

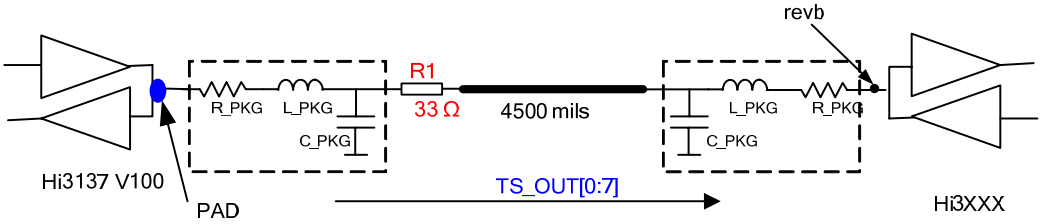


Figure 3-11 Interconnection topology of TS_CLK/TS_SYNC/TS_VALID and an STB decoder chip when the number of PCB layers is greater than 2

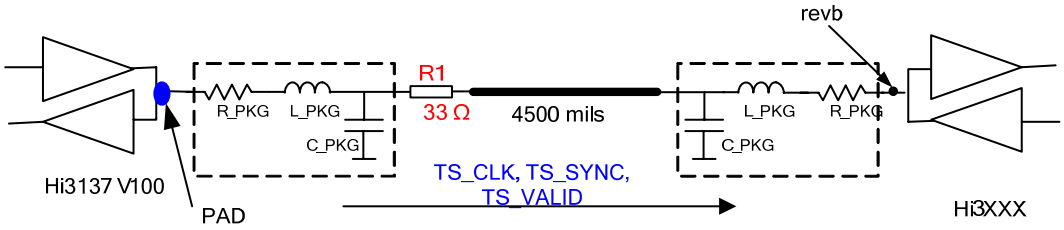


Figure 3-12 Interconnection topology of TS_OUT[0:7] and an STB decoder chip when the number of PCB layers is 2

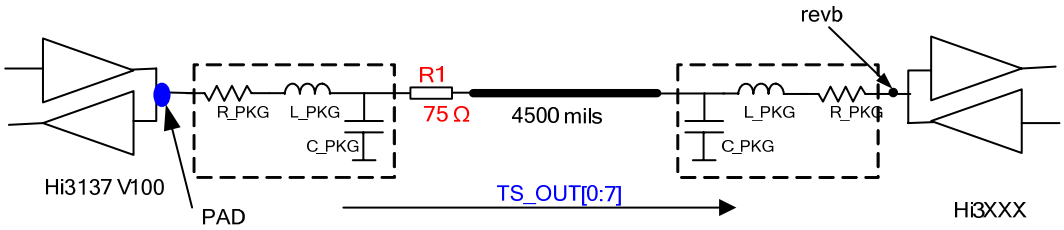
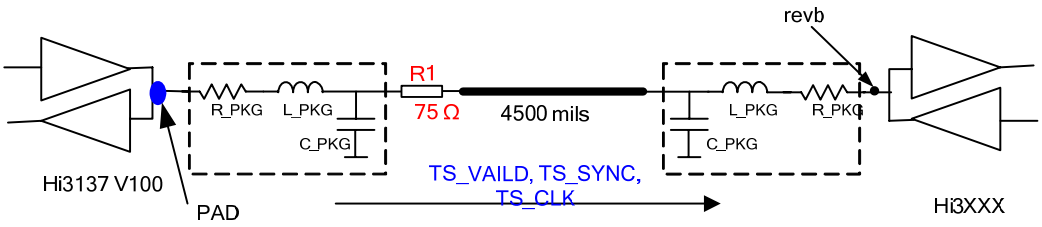


Figure 3-13 Interconnection topology of TS_VAILD/TS_SYNC/TS_CLK and an STB decoder chip when the number of PCB layers is 2



AGC Circuit

After the low-pass filter processes PDM modulation signals, the AC components in analog signals are significantly alleviated. On the RC filtering network, a larger RC value indicates less AC components but slow response. Therefore, an appropriate RC value is required to balance the quantity of AC analog signals and response speed in actual application scenarios. A 4.7 kΩ resistor and a 100 nF capacitor are recommended on the AGC circuit.

3.3.2 Power Supplies

NOTE

For details about system power supply design, see the schematic diagram of the Hi3137 V100 board.

3.3.2.1 Core Power

The core power pin DVDD11 connects to the 1.1 V digital power. The design recommendations are as follows:

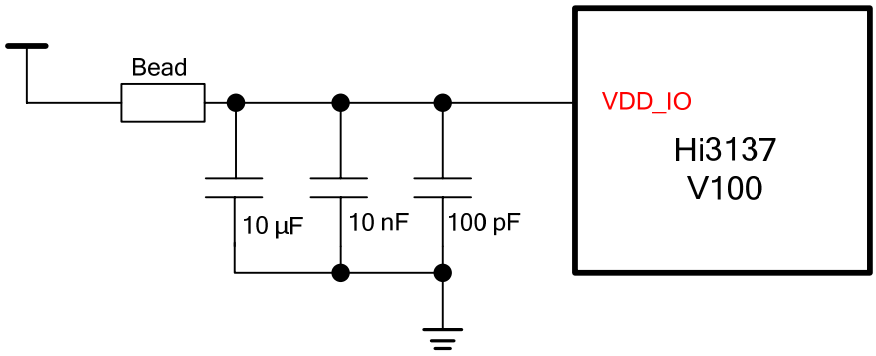
- If there is no 1.1 V power on the board, the low dropout regulator (LDO) is preferred when you select the power chip and the current of power chip must be greater than or equal to 500 mA.
- The typical current of the core power is 150 mA and the maximum current is 300 mA.
- Each core power pin connects to a 10 µF filtering bypass capacitor and then to GND. In addition, each core power pin connects to a group of 10 nF and 100 pF decoupling capacitors, which are placed close to power pins.

3.3.2.2 I/O Power

The I/O power pin DVDD33 is connected to the 3.3 V digital power.

- The maximum current of VDD_IO is 60 mA. The LDO is preferred.
- Each I/O power pin connects to a group of 10 nF and 100 pF decoupling capacitors, which are placed close to power pins.
- The inputs of I/O power pins are isolated by using electromagnetic interference (EMI) beads. See Figure 3-14.

Figure 3-14 VDD33_IO topology

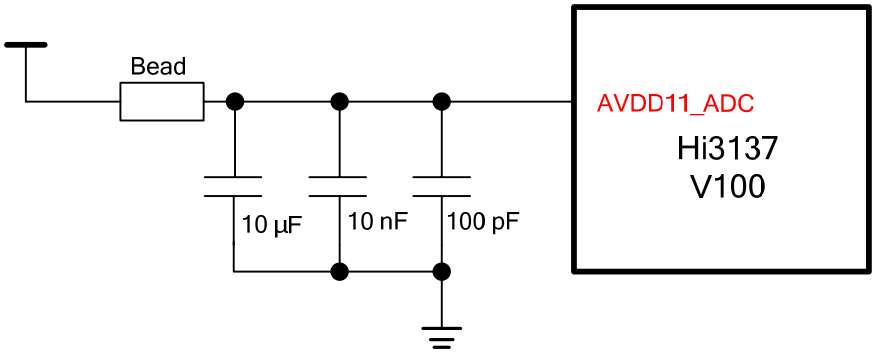


3.3.2.3 ADC Power

The ADC power pin AVDD11_ADC connects to the 1.1 V analog power. Note the following:

- The maximum current of the ADC power is 15 mA. By using the EMI beads, the ADC power and core power share the 1.1 V power.
- The ADC power is isolated from the 1.1 V power by using an EMI bead and connects to a 10 µF filtering bypass capacitor and then to GND.
- Each ADC power pin connects to a group of 10 nF and 100 pF decoupling capacitors, which are placed close to power pins.
- The level deviation of the 1.1 V power is within ±5%. See Figure 3-15.

Figure 3-15 AVDD11_ADC topology



3.3.2.4 Others

The other precautions for power supply design are as follows:

- The LDO is preferred when you select the power chip. The digital and analog power supplies are isolated by using EMI beads and groups of 10 nF and 100 pF decoupling capacitors are required.
- Ensure that the output voltage of each power supply meets the requirements even when ripples and noises occur. For details about the power supply requirements of each module, see section 3.2 "Electrical Specifications."

3.3.3 Unused Pins

If some pins are not used, do not connect them and disable the corresponding circuits by configuring registers.

3.4 PCB Design Recommendations

3.4.1 Stack and Layout

3.4.1.1 Stack

The package of Hi3137 V100 is mapped quad flat non-leaded 48 (MQFN48). The lead pitch is 0.4 mm (0.02 in.). You are advised to design a 4-layer PCB with the following stack:

- Top layer: signal traces
- Internal layer 1: GND plane
- Internal layer 2: power plane
- Bottom layer: signal traces

To reduce the cost, you can also design a 2-layer PCB with the following stack:

- Top layer: signal traces and part of power traces
- Bottom layer: GND plane and part of power traces

Take the following precautions during PCB design:

- Components are placed at the top layer. Routing signal traces at the top layer is preferred.

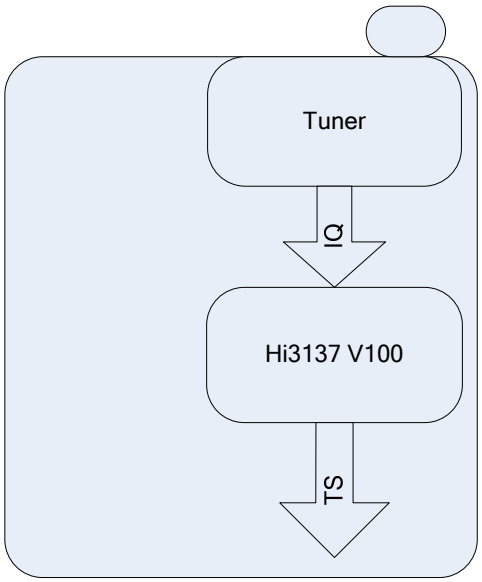
- Power pins are connected by using wide traces.
- Ensure that the bottom layer is a complete GND plane.
- The vias with 8-mil diameter are recommended for master chip fanout.
- The impedance of special signal traces must meet requirements.

The PCB material is FR-4, the PCB thickness is 1.6 mm, and the thickness of the copper foil on the surface is 1 oz.

3.4.1.2 Board Layout

Figure 3-16 shows the board layout of the Hi3137 V100 reference design.

Figure 3-16 Board layout



During the Demod reference design of Hi3137 V100, pay attention to the layout of RF, analog, and digital signals and ESD protective components such as the RF interface female connector, crystal resonator, and RF loop filter.

Isolate the 3.3 V and 1.1 V power pins from digital parts by using EMI beads and select the components with small-sized package.

3.4.2 PCB Design Recommendations for the Small System

3.4.2.1 Power Supplies of the Small System

Digital Power

The digital power supplies of Hi3137 V100 include DVDD33 (3.3 V) and DVDD11 (1.1 V). It is recommended that the DVDD33 and DVDD11 be isolated from the 3.3 V and 1.1 V digital power supplies of the board by using EMI beads. All power supplies use the exposed pad of Hi3137 V100 as the reference GND. The traces should be as wide as possible when the through-flow capacity is ensured. The minimum trace width is 15 mils for DVDD33 or 25 mils for DVDD11. Ensure that digital power and analog power planes do not overlap and decoupling capacitors are placed close to Hi3137 V100.

RF/Analog Power

The RF and analog power supplies must be isolated from other power supplies by using EMI beads. The RF and analog power supplies use the exposed pad of Hi3137 V100 as the reference GND.

- Never route digital signal traces especially high-speed digital signal traces in the analog power area.
- Connect a decoupling capacitor to each power pin and ensure that traces are as wide as possible and decoupling capacitors are placed close to Hi3137 V100.

3.4.2.2 Clock and Reset Circuits

Clock

The power supplies of the Hi3137 V100 PLL unit are AVDD11_PLL (1.1 V) and AVDD33_PLL. The GND of the Hi3137 V100 PLL unit is AVSS_PLL. Design the PCB based on the following guidelines:

- AVDD11_PLL is the 1.1 V PLL power. Ensure that the width of the AVDD11_PLL trace is 12 mils when the through-flow capacity is ensured.
- Ensure that the width of the AVDD33_PLL trace is 12 mils when the through-flow capacity is ensured.
- AVSS_PLL is the reference GND of the PLL unit. It is recommended that GND traces connect to the exposed pad and the GND vias are connected by ensuring a complete GND plane.
- The traces of the system clock crystal oscillator circuit must be as short as possible and be surrounded by GND traces. The crystal GND part must be separately processed and isolated from the large-sized GND area to prevent coupling.
- The matching capacitors for the crystal oscillator must be placed close to the crystal oscillator and the crystal oscillator must be placed close to Hi3137 V100. Ensure that the spacing between the crystal oscillator and the board edge is at least 1000 mils. Never route critical traces such as high-speed clock traces under the crystal oscillator and ensure the integrity of the signals under the crystal oscillator.

Reset

Pin 15 is a reset pin. The reset signal trace is a critical trace and is susceptible to interference. The following are design recommendations:

- If the number of PCB layers is greater than 2, route the reset signal trace at an inner layer close to the GND plane and ensure that the trace width is greater than 8 mils. If a 2-layer PCB is used, ensure that the reset signal trace is surrounded by GND traces.
- Route the reset signal trace at least 30 mils away from interfaces and power inputs.

3.4.3 PCB Design Recommendations for Digital and Analog Interfaces

3.4.3.1 Digital Interfaces

TS Signals

The following are TS signal requirements:

- The maximum signal trace length is 5000 mils.
- The length of all TS signal traces is determined based on the TS_CLK traces. The allowed length deviation is ±250 mils.
- The serial matching resistors are connected close to Hi3137 V100.
- For the 2-layer PCB, the characteristic impedance of the TS signal trace should be 140 Ω. It is recommended that TS_OUT[0:7] connect to a 75 Ω matching resistor in serial and TS_CLK, TS_SYNC, and TS_VALID connect to a 75 Ω matching resistor in serial.
- If more than two PCB layers are designed, the characteristic impedance of the TS signal trace should be 50 Ω. A 33 Ω matching resistor is recommended.

AGC Signals

The following are requirements on AGC signal traces:

- The maximum trace length is 5000 mils and the minimum trace width is 12 mils. Route GND traces around AGC signal traces to prevent interference to external signal traces from AGC signals and interference to AGC signal traces from external noises.
- The RC low-pass filter to which AGC outputs are transmitted must be placed close to the AGC output pin of Hi3137 V100. This prevents AGC high-frequency noises from being transmitted to the board, which may result in deterioration in channel performance.

The following are recommendations for the I^2C traces:

- The maximum serial clock (SCL) trace length is 5000 mils.
- The serial data (SDA) traces are routed based on SCL traces. The allowed length deviation is ±250 mils.

PCB Routing Recommendations

Route traces on a PCB based on the following guidelines:

CAUTION

Never cross the reference GND plane of TS signal traces when routing other signal traces, and ensure that GND traces are routed around signal traces. Place serial resistors close to Hi3137 V100. For details, see the PCB design documents of the Hi3137EVA board.

- Route all the TS signal traces on the planes adjacent to the GND plane. Never route the signal traces across the power and GND plane splits. Ensure that signal traces have a complete reference GND plane.
- To ensure a good signal return path, punch vias around signal traces and changed layers and connect the punched vias to GND.
- Ensure that signal traces are as short as possible. Minimize the use of vias to ensure the impedance continuity of traces. If the number of PCB layers is greater than 2, the characteristic impedance of the single-end PCB signal trace is 50 Ω ±10%. If a 2-layer PCB is used, the characteristic impedance of the single-end PCB signal trace is 140 Ω ±10%. The serial matching resistors are connected close to Hi3137 V100.
- If resistor networks are used, ensure that the TS_CLK trace and TS traces are not routed on the same resistor network.

- Ensure that the spacing between adjacent signal traces is 2–3 times of the trace width according to the 3W rule. The 3W rule indicates that the trace spacing is three times of the trace width.
- Route signal traces far away from data and address buses and route GND traces around the TS_CLK trace.

3.4.3.2 Others

Integrity Simulation Design Recommendations for PCB Signals

By using board-level simulation tools, PCB designers can simulate and analyze signal integrity based on the input/output buffer information specification (IBIS) models of the Hi3137 V100 interfaces and interconnected components, transmission line models, and board topologies. Based on the simulation results, PCB designers can adjust the typologies to meet the signal quality requirements in overshoot, undershoot, ringing, monotonicity, and others.

Note

If a clock signal trace connects to multiple loads, ensure good signal quality, especially signal edge monotonicity regardless of the frequency.

3.5 Heat Design Recommendations

3.5.1 Package Thermal Resistance

CAUTION

The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.

Table 3-19 describes the thermal resistance of the package.

Table 3-19 Thermal resistance of the package

Parameter	Symbol	Value	Unit
Junction-to-ambient thermal resistance	θ_{JA}	37	°C/W
Junction-to-case thermal resistance	θ_{JC}	20.684	°C/W
Junction-to-top center of case thermal resistance	Ψ_{JT}	-	°C/W
Junction-to-board thermal resistance	θ_{JB}	17.41	°C/W

3.5.2 Recommended Thermally Conductive Materials

Table 3-20 describes recommended thermally conductive materials.

Table 3-20 Recommended thermally conductive materials

Mode of Fixing Heat Sinks	Model	Thermal Conductivity Coefficient (W/m x k)	Ambient Temperature (°C)	Colloid Type	Insulation Strength (V/Mil)	Flame Retardance	Bearing Capacity (g)
Mechanical fixing	GF2000	2	−60 to +200	Silicone rubber	500	UL9V0	None
Non-mechanical fixing	Locotite 315	0.808	None	Acrylic resin	6000	UL9V2	None

3.5.3 Schematic Diagram Design

3.5.3.1 Power Supply

Ensure that the efficiency of the board power tree is the highest on the basis that the power supply is stable. That is, the board power load is designed optimally and fewer LDO components with large voltage difference are used. This reduces the heat produced during the conversion of the power supply. An exposed pad is designed at the bottom of the chip and solder mask opening is designed for the GND plane of the PCB, which is good for heat conduction.

3.5.4 PCB Design

3.5.4.1 Component Layout

Lay out components based on the product architecture and heat dissipation design:

- Do not lay out the components that consume a large amount of power and produce much heat on the same ventilation path.
- Place the components that consume a large amount of power and produce much heat evenly, and pour copper sheets under and around these components as large as possible to dissipate heat.

3.5.4.2 PCB Heat Dissipation

The recommendations are as follows:

- For the connect style of the vias under Hi3137 V100, select the full connect style but not the thermal connect style, In addition, use an opening copper plane at the PCB bottom layer on which the exposed pad of Hi3137 V100 is soldered to improve the dissipation efficiency of the board.
- The 1.1 V power traces, 3.3 V power traces, and GND traces should be as wide as possible on the basis that the maximum current capability is ensured.
- Never place components that produce much heat around Hi3137 V100.

3.6 Soldering Process Recommendations

3.6.1 Overview

The appropriate reflow soldering temperatures must be determined based on the reflow profiles supported by all the components, ICs, and PCB, and the reflow profile recommended by the solder paste vendor. This chapter describes only the reflow soldering temperature range supported by Hi3137 V100.

3.6.1.1 Coating Material

The elelectrotinning coating is used on the MQFN package.

3.6.1.2 Component Package and Storage

The following describes the component package and storage:

- Package of surface-mount components: tray
- Allowed storage duration (below 60% RH): 12 months at 40ºC (104ºF)
- Packaging material: electrostatic discharge (ESD) material

3.6.1.3 Soldering Process

Reflow soldering can be used.

Figure 3-17 shows the reflow profiles supported by Hi3137 V100 but not the reflow profiles recommended during soldering. Determine the soldering temperatures based on the reflow profiles of the solder paste, PCB, and all ICs and components. For details, see the JEDEC020D standard.

Figure 3-17 Soldering temperatures

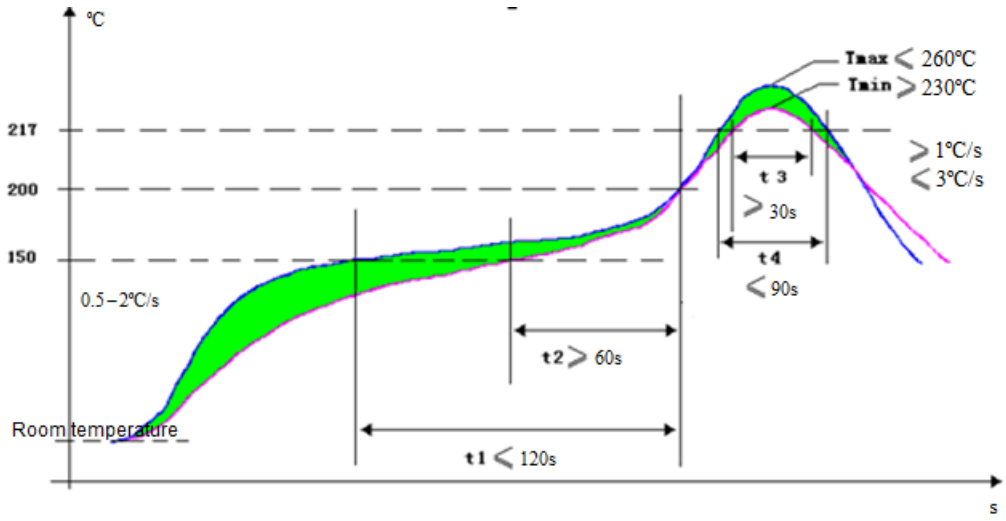


Table 3-21 Reflow soldering specifications

Zone	Duration	Heating Up Slope	Peak Temperature	Cooling Down Slope
Preheat zone (40–150°C or 104–302°F)	60−150s	≤ 2.0ºC/s (≤ 35.6ºF/s)	None	None
Soak zone (150–200°C or 302–392°F)	60−120s	< 1.0ºC/s (≤ 33.8ºF/s)	None	None
Reflow zone (> 217°C or 423°F)	30−90s	None	230−260ºC (446−500ºF)	None
Cooling zone (Tmax to 180°C or 356°F)	None	None	None	1.0ºC/s ≤ Slope ≤ 4.0ºC/s (33.8ºF/s ≤ Slope ≤ 39.2ºF/s)

3.6.2 Process Preparations

Confirm that all products are dry and materials have not expired.

Test the first sample (for example, check the solder paste thickness) before mass production. Start mass production only when the first sample passes all tests.

3.7 Moisture-Sensitive Specifications

3.7.1 Storage and Usage

[Application Scope]

The specifications apply to the storage and usage of all moisture-sensitive ICs of HiSilicon.

[Storage Environment]

You are advised to store products in vacuum packages at 30°C (86°F) or lower and at most 60% relative humidity (RH).

[Shelf Life]

At 30°C (86°F) or lower and at most 60% RH, the shelf life is greater than or equal to 12 months for the vacuum package.

[Floor Life]

Table 3-22 describes the floor life at 30°C (86°F) or lower and at most 60% RH.

Table 3-22 Floor life

Level	Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated
1	Unlimited at 30°C (86°F) or lower and at most 85% RH
2	1 year

2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. The product must be reflowed within the time limit specified on the label.

[Usage of Moisture-Sensitive Products]

- If a chip has been exposed to air for 2 hours at 30°C (86°F) or lower and at most 60% RH, rebake it and pack it into a vacuum bag.
- If a chip has been exposed to air for less than 2 hours at 30°C (86°F) or lower and at most 60% RH, replace the desiccant and pack the chip into a vacuum bag.

For details about other storage modes and usage rules, see the JEDEC J-STD-033A standard.

3.7.2 Rebaking

[Applicable Products]

All moisture-sensitive ICs of HiSilicon

[Application Scope]

All ICs that need to be rebaked

[Rebaking Reference]

Table 3-23 Rebaking reference

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
≤ 1.4 mm (0.06 in.)	2a	3 hours	11 hours	5 days
	3	7 hours	23 hours	9 days
	4	7 hours	23 hours	9 days
	5	7 hours	24 hours	10 days
	5a	10 hours	24 hours	10 days
≤ 2.0 mm (0.08 in.)	2a	16 hours	2 days	22 days
	3	17 hours	2 days	23 days
	4	20 hours	3 days	28 days
	5	25 hours	4 days	35 days

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
	5a	40 hours	6 days	56 days
≤ 4.5 mm (0.18 in.)	2a	48 hours	7 days	67 days
	3	48 hours	8 days	67 days
	4	48 hours	10 days	67 days
	5	48 hours	10 days	67 days
	5a	48 hours	10 days	67 days

Note:

- Table 3-23 lists the minimum rebaking time for moist chips.
- Low-temperature rebaking is recommended.
- For details, see the JEDEC standard.

3.8 Interface Timings

3.8.1 Output Interface Timings

Hi3137 V100 supports three TS output modes: parallel mode, 1-bit serial mode, and 2-bit serial mode.

The signals from the TS output interface include the data signals TS_OUT[7:0], clock signal TS_CLK, data validity signal TS_VLD, sync header signal TS_SYNC, and packet error signal TS_ERR.

- TS_OUT: TS frame data. This signal is 8 bits in parallel mode, 1 bit in 1-bit serial mode, and 2 bits in 2-bit serial mode.
- TS_CLK: data clock. The clock edge is configurable. The adaptive clock output is used by default in various output modes.
- TS_VLD: TS packet data validity indicator (byte valid in parallel mode or bit valid in 1-bit serial mode).
- TS_SYNC: TS packet sync header indicator (byte valid in parallel mode or bit valid in serial mode).
- TS_ERR: TS packet error indicator. Set it to 1 if an error occurs in the current TS packet.

Figure 3-18 Timing in TS parallel output mode

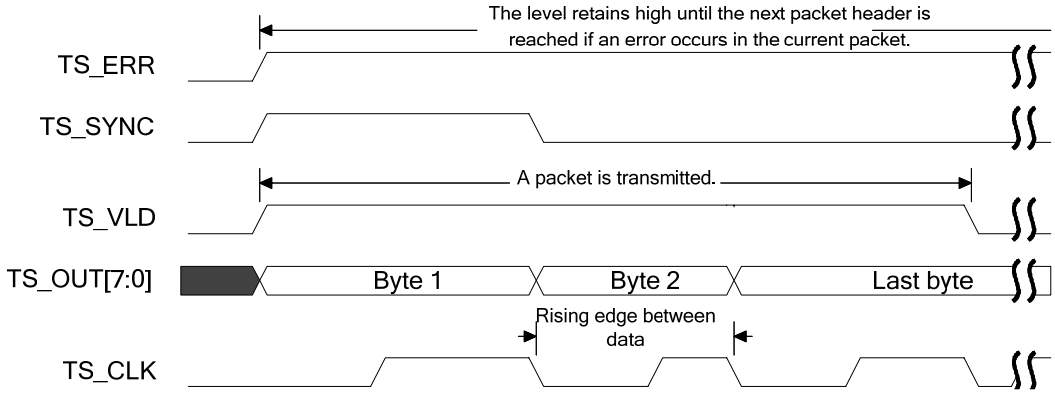


Figure 3-19 Timing in 1-bit TS serial output mode

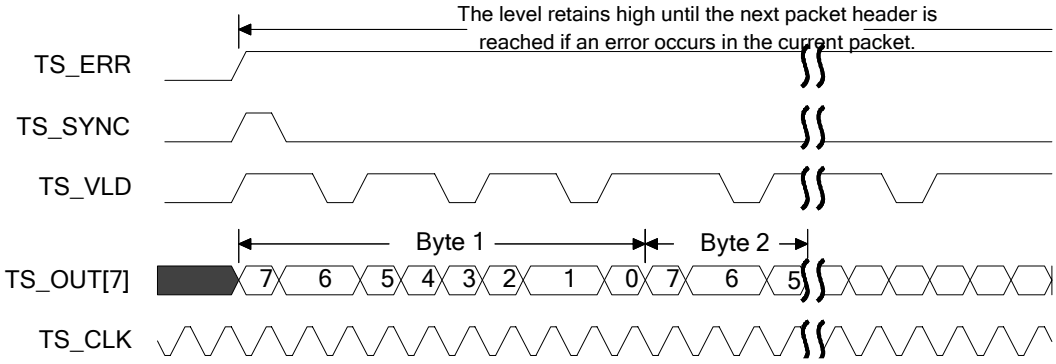
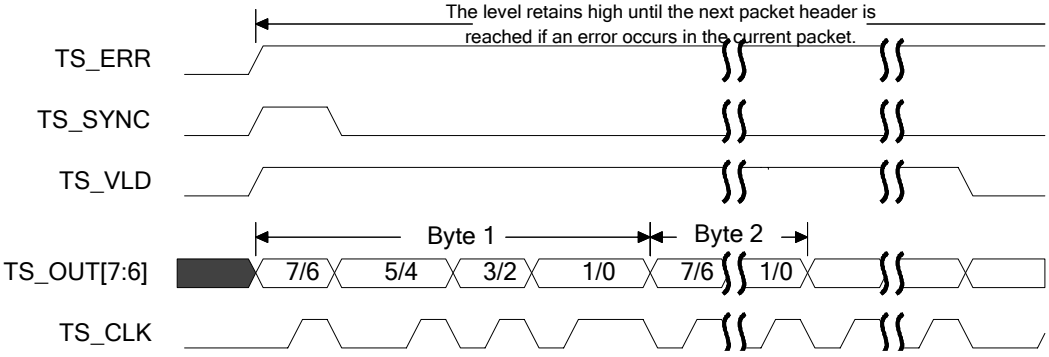


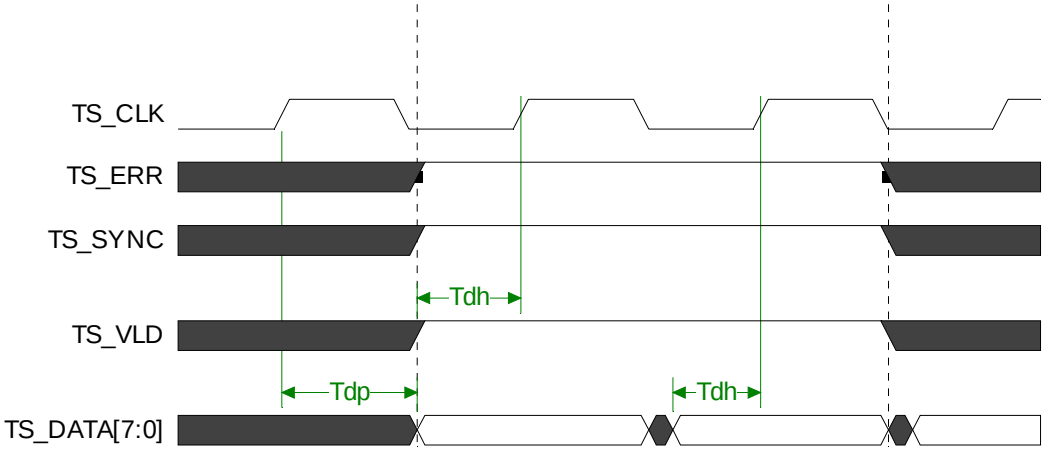
Figure 3-20 Timing in 2-bit TS serial output mode



3.8.2 Output Timing Parameters

Figure 3-21 shows the TS output timing.

Figure 3-21 TS_CLK output timing



Note that the TS_CLK output in the preceding figure is the rising edge mode.

Table 3-24 describes the TS output timing parameters.

Table 3-24 TS output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
TS_CLK duty cycle	-		50		%
TS_CLK clock frequency	TS_Freq			80	MHz
Output data signal setup time	Tdp		(1/TS_Freq)/2	(1/TS_Freq)/2 + 1.7	ns
Output data signal hold time	Tdh	(1/TS_Freq)/2 – 1.8	(1/TS_Freq)/2		ns

Contents

A Acronyms and Abbreviations

A

AAF	anti-aliasing filter
ADC	analog-to-digital converter
AGC	automatic gain control

B

BB	base band
BCH	bose-chaudhuri-hocquenghem multiple error correction binary block code
BER	bit error rate

C

CIR	channel impulse response
CLK	clock
CR	carrier recovery
CSI	channel state information

D

DAGC	digital automatic gain control
DNP	deleted null packets

E

EQU	equalizer
ERR	error
F	
FEC	forward error correction
FEF	future extension frame
FER	frame error rate
FFT	fast fourier transform
G	
GFPS	generic fixed-length packetized stream
GS	generic stream
GSE	generic stream encapsulation
I	
ISCR	input stream time reference
ISSY	input stream synchronizer
L	
LDPC	low density parity check code
LSB	least significant byte
M	
MISO	multiple input single output
MPLP	multiple physical layer pipe
P	
PER	packet error rate
PLL	phase-locked loop
PLP	physical layer pipe

PDM	pulse density modulation
PWM	pulse width modulation
PP	pilot pattern
Q	
Q	quadrant
QPSK	quaternary phase shift keying
QAM	quadrature amplitude modulation
R	
RF	radio frequency
RS	reed solomon
S	
SNR	signal-to-noise ratio
SYNC	synchronization
SISO	single input single output
T	
TR	timing recovery
TS	transport stream
V	
VLD	valid