



Hi3796M V100 Hardware Design

FAQs

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About This Document

Purpose

This document describes the solutions to frequently asked questions (FAQs) for the hardware design of Hi3796M V100.

Related Version

The following table lists the product version related to this document.

| Product Name | Version |
|--------------|---------|
| Hi3796M | V1XX |

Intended Audience

This document is intended for:

- Technical support personnel
- Hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B02 (2015-05-15)

This issue is the second draft release, which incorporates the following change:

Chapter 2 "Small System" is added.

Issue 00B01 (2015-01-20)

This issue is the first draft release.



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1 Peripherals

1.1 How Do I Optimize the Electrical Specifications of the SCI Circuit?

Problem Description

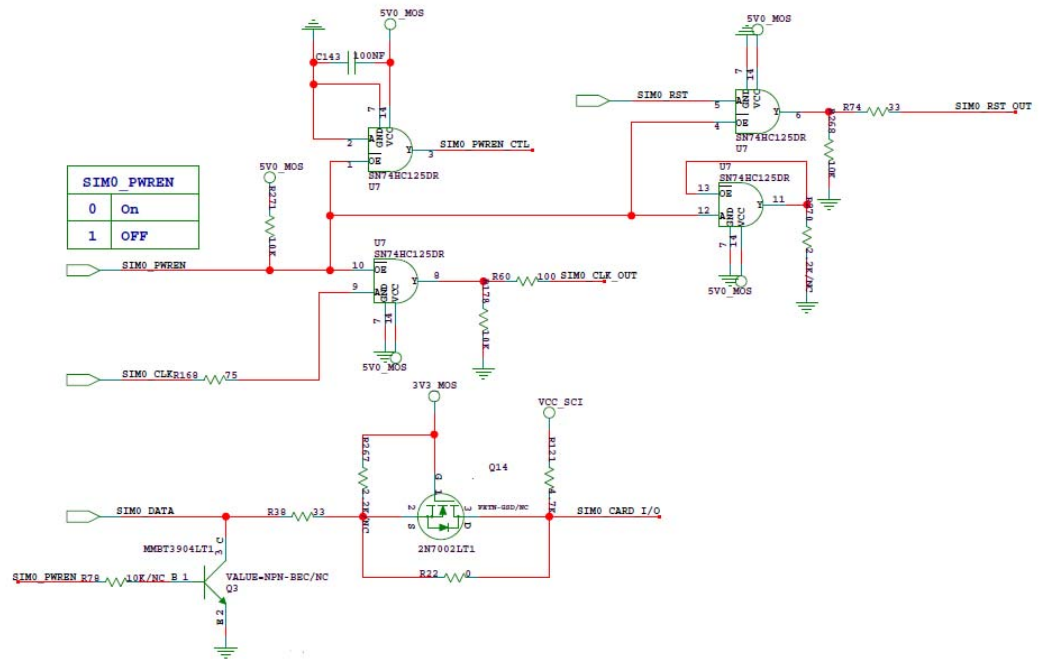
The SCI circuit of the Hi3716C V200 CA solution for a customer fails the electrical specifications certification test. The SCI circuit of Hi3796MDMO1A is the same, and the issue persists.

Solution

- Connect SIM_PWREN to a 10 k Ω (instead of 2.2 k Ω) pull-up resistor and then to 5V_MOS (instead of 3V3_MOS).
- Change the pull-down resistor for SIM0_CLK_OUT from 2.2 k Ω to 10 k Ω , and connect SIM0_CLK_OUT to a 100 Ω resistor in series.
- Modify the SIM0_DATA circuit, as shown in [Figure 1-1](#).



Figure 1-1 SCI circuit with optimized electrical performance





2 Small System

2.1 How Do I Design the 2-Layer PCB with Two 16-Bit DDR SDRAMs?

Problem Description

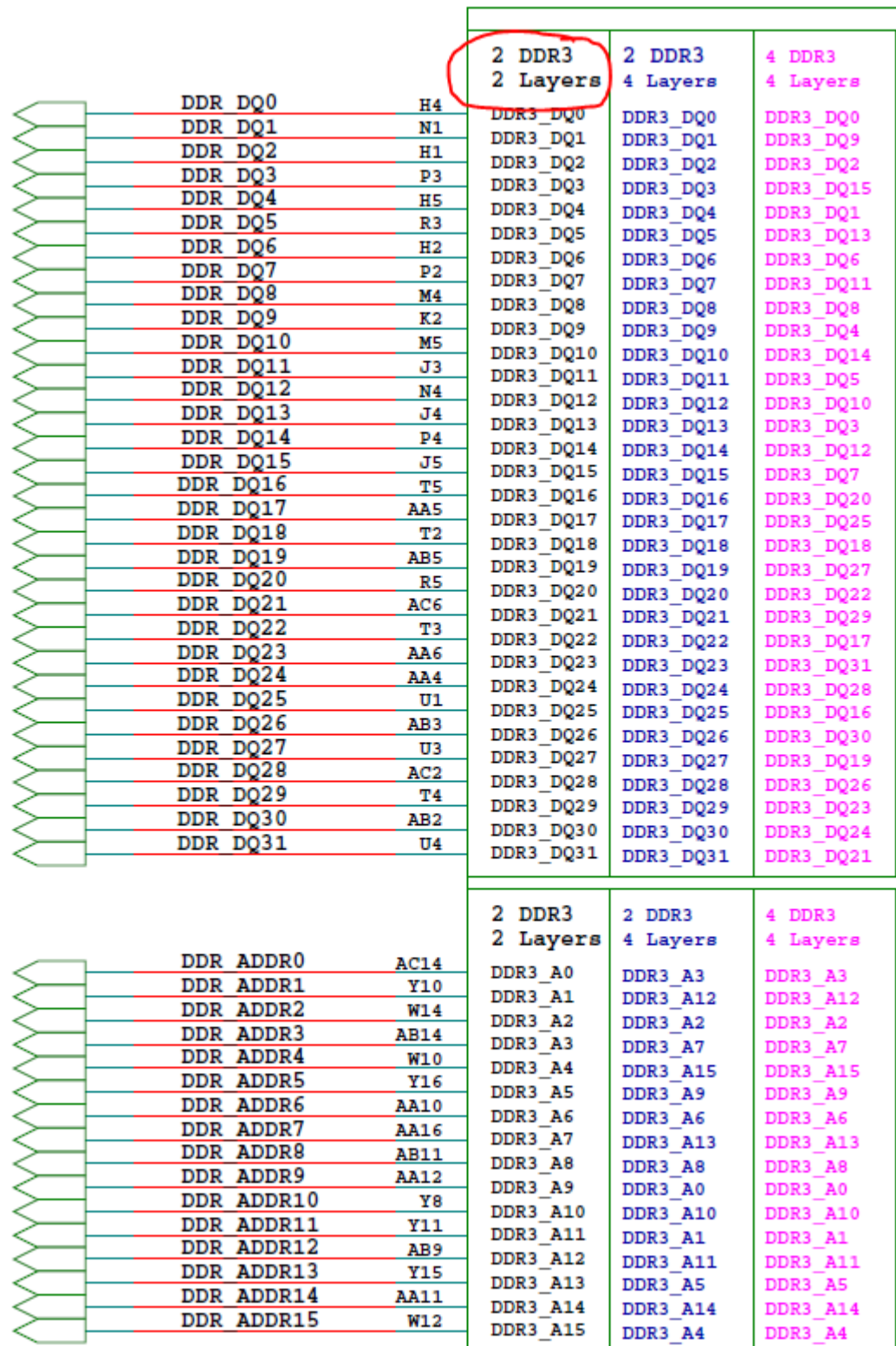
HiSilicon provides reference design only for the 4-layer PCB with two 16-bit DDR SDRAMs. How do I design the 2-layer PCB with two 16-bit DDR SDRAMs?

Solution

- Reference design for the schematic diagram and PCB
For details about the schematic diagram, see the Hi3798MDMO1B hardware release package. Ensure that the signal names are consistent with those of the Hi3798MDMO1B. For the DQ and ADDR pins, select the names in the **2 DDR3 2 Layers** column, as shown in [Figure 2-1](#).



Figure 2-1 Schematic diagram for the 2-layer PCB with two DDRs



Compared with the Hi3798M V100 BGA package, Hi3796M V100 has two more GND pins (AH2 and AG2) in the lower left corner of the DDR pin map, and the DDR pin map

is shifted rightwards by one ball on the bottom side. You can copy the PCB design of the Hi3798MDMO1B DDR part for Hi3796M V100 and modify the copper plane in the positions of the two additional GND pins.

The modifications are described as follows, as shown in [Figure 2-2](#) and [Figure 2-3](#):

- Copy the trace routing design for Hi3798MDMO1B, including the trace width, air gap between traces, and air gap between traces and GND, power trace routing, and trace length.
- Shift the ADDR signal trace under the master chip rightwards by one ball (compared with the Hi3798MDMO1B DDR) and fine-tune the ADDR trace length. Adjust the surrounding copper plane of the signal (except the area under the BGA chip) to ensure that the width of the copper plane is greater than or equal to the via outer diameter.
- Ensure that the surrounding GND of signals connects to the master chip end and the GND under the BGA chip. See the ellipses and rectangle in yellow in [Figure 2-2](#) and [Figure 2-3](#).

Figure 2-2 Top side of the 2-layer PCB (DDR layout)

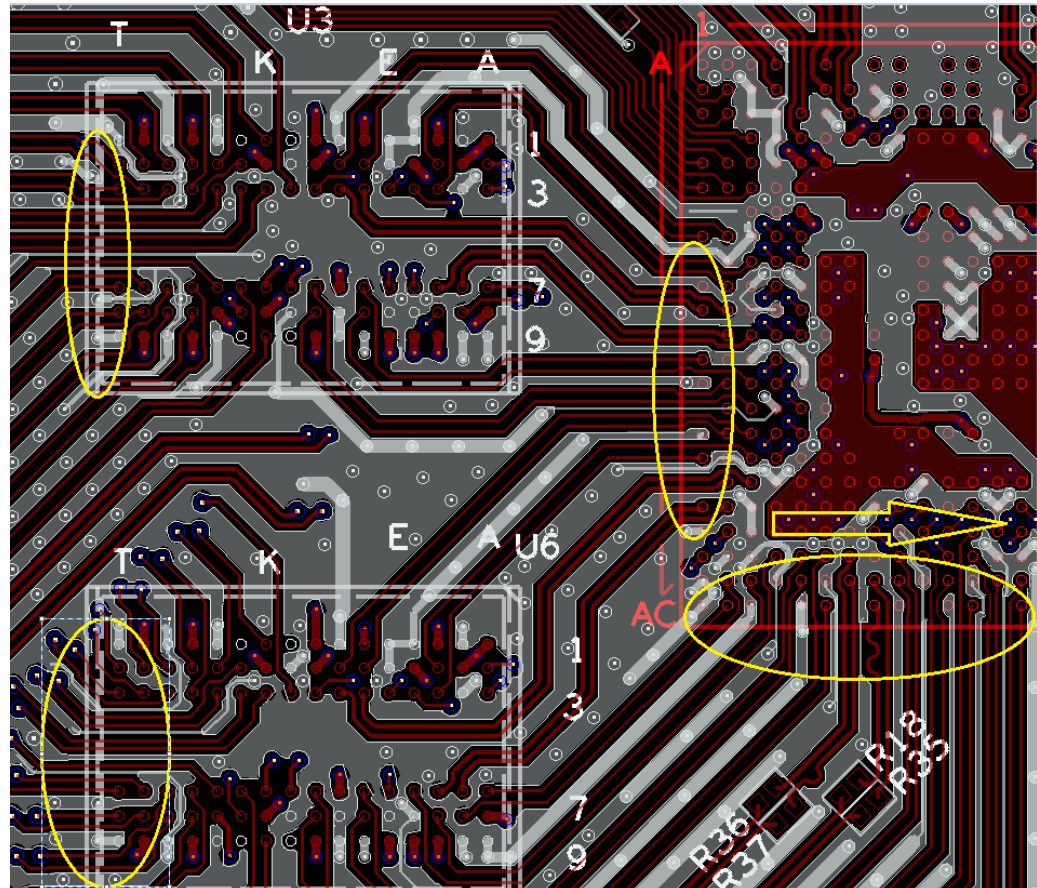
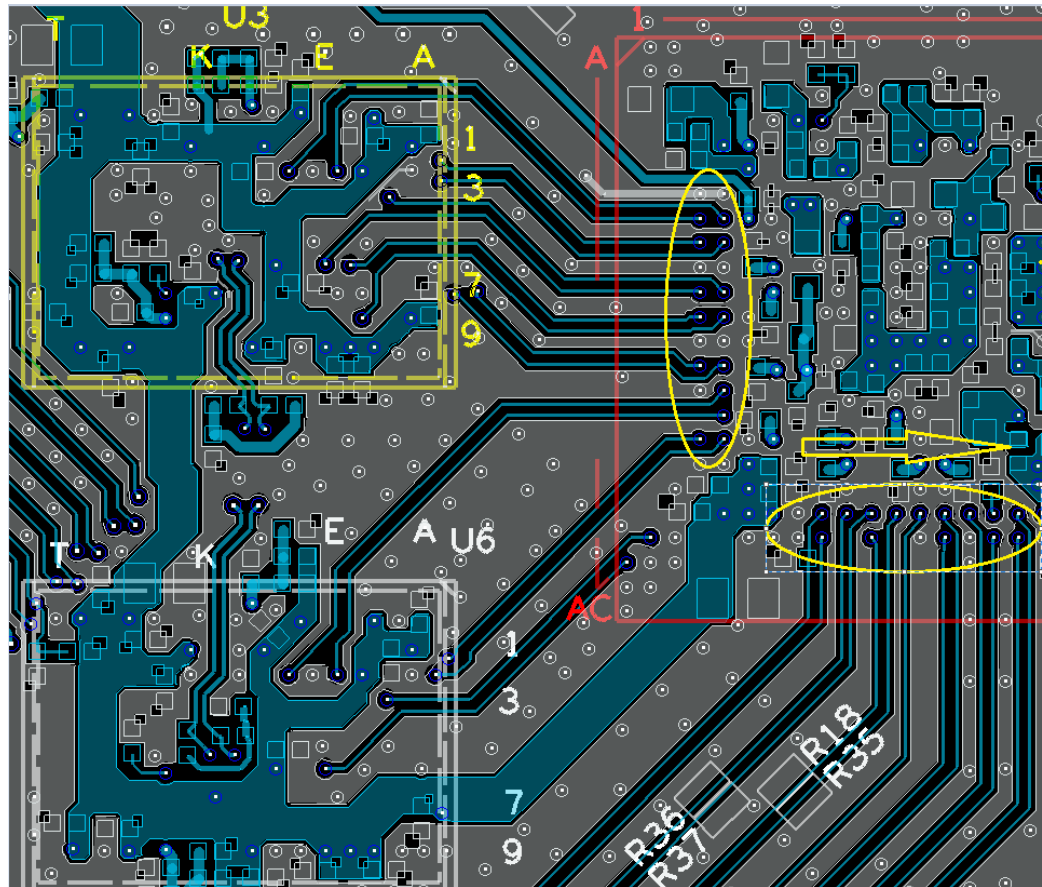


Figure 2-3 Bottom side of the 2-layer PCB (DDR layout)



- Fastboot configuration table

The fastboot configuration table is **hi3796mv100_ddr3_1gbyte_16bitx2_2layers.xlsm** in the SDK.

Configure the pin multiplexing relationship in the table based on actual application and set unused I/O pins to GPIO mode.



CAUTION

- Verify the DDR stability carefully if the board uses a new DDR solution.
- Ensure that the schematic diagram and PCB are reviewed by HiSilicon FAEs before populating the PCB.



2.2 How Do I Design the 4-Layer PCB with Four 8-Bit DDR SDRAMs?

Problem Description

HiSilicon provides reference design only for the 4-layer PCB with two 16-bit DDR SDRAMs. How do I design the 4-layer PCB with four 8-bit DDR SDRAMs?

Solution

- Reference design for the schematic diagram and PCB
For details about the schematic diagram, see the Hi3798MDMO1D hardware release package. Ensure that the signal names are consistent with those of the Hi3798MDMO1D. For the DQ and ADDR pins, select the names in the **4 DDR3 4 Layers** column, as shown in [Figure 2-4](#).



Figure 2-4 Schematic diagram for the 4-layer PCB with four DDRs

| | | | 2 DDR3 2 Layers | 2 DDR3 4 Layers | 4 DDR3 4 Layers |
|--|------------|------|--------------------|--------------------|--------------------|
| | DDR DQ0 | H4 | DDR3_DQ0 | DDR3_DQ0 | DDR3_DQ0 |
| | DDR DQ1 | N1 | DDR3_DQ1 | DDR3_DQ1 | DDR3_DQ9 |
| | DDR DQ2 | H1 | DDR3_DQ2 | DDR3_DQ2 | DDR3_DQ2 |
| | DDR DQ3 | P3 | DDR3_DQ3 | DDR3_DQ3 | DDR3_DQ15 |
| | DDR DQ4 | H5 | DDR3_DQ4 | DDR3_DQ4 | DDR3_DQ1 |
| | DDR DQ5 | R3 | DDR3_DQ5 | DDR3_DQ5 | DDR3_DQ13 |
| | DDR DQ6 | H2 | DDR3_DQ6 | DDR3_DQ6 | DDR3_DQ6 |
| | DDR DQ7 | P2 | DDR3_DQ7 | DDR3_DQ7 | DDR3_DQ11 |
| | DDR DQ8 | M4 | DDR3_DQ8 | DDR3_DQ8 | DDR3_DQ8 |
| | DDR DQ9 | K2 | DDR3_DQ9 | DDR3_DQ9 | DDR3_DQ4 |
| | DDR DQ10 | M5 | DDR3_DQ10 | DDR3_DQ10 | DDR3_DQ14 |
| | DDR DQ11 | J3 | DDR3_DQ11 | DDR3_DQ11 | DDR3_DQ5 |
| | DDR DQ12 | N4 | DDR3_DQ12 | DDR3_DQ12 | DDR3_DQ10 |
| | DDR DQ13 | J4 | DDR3_DQ13 | DDR3_DQ13 | DDR3_DQ3 |
| | DDR DQ14 | P4 | DDR3_DQ14 | DDR3_DQ14 | DDR3_DQ12 |
| | DDR DQ15 | J5 | DDR3_DQ15 | DDR3_DQ15 | DDR3_DQ7 |
| | DDR DQ16 | T5 | DDR3_DQ16 | DDR3_DQ16 | DDR3_DQ20 |
| | DDR DQ17 | AA5 | DDR3_DQ17 | DDR3_DQ17 | DDR3_DQ25 |
| | DDR DQ18 | T2 | DDR3_DQ18 | DDR3_DQ18 | DDR3_DQ18 |
| | DDR DQ19 | AB5 | DDR3_DQ19 | DDR3_DQ19 | DDR3_DQ27 |
| | DDR DQ20 | R5 | DDR3_DQ20 | DDR3_DQ20 | DDR3_DQ22 |
| | DDR DQ21 | AC6 | DDR3_DQ21 | DDR3_DQ21 | DDR3_DQ29 |
| | DDR DQ22 | T3 | DDR3_DQ22 | DDR3_DQ22 | DDR3_DQ17 |
| | DDR DQ23 | AA6 | DDR3_DQ23 | DDR3_DQ23 | DDR3_DQ31 |
| | DDR DQ24 | AA4 | DDR3_DQ24 | DDR3_DQ24 | DDR3_DQ28 |
| | DDR DQ25 | U1 | DDR3_DQ25 | DDR3_DQ25 | DDR3_DQ16 |
| | DDR DQ26 | AB3 | DDR3_DQ26 | DDR3_DQ26 | DDR3_DQ30 |
| | DDR DQ27 | U3 | DDR3_DQ27 | DDR3_DQ27 | DDR3_DQ19 |
| | DDR DQ28 | AC2 | DDR3_DQ28 | DDR3_DQ28 | DDR3_DQ26 |
| | DDR DQ29 | T4 | DDR3_DQ29 | DDR3_DQ29 | DDR3_DQ23 |
| | DDR DQ30 | AB2 | DDR3_DQ30 | DDR3_DQ30 | DDR3_DQ24 |
| | DDR DQ31 | U4 | DDR3_DQ31 | DDR3_DQ31 | DDR3_DQ21 |
| | | | 2 DDR3 2 Layers | 2 DDR3 4 Layers | 4 DDR3 4 Layers |
| | DDR ADDR0 | AC14 | DDR3_A0 | DDR3_A3 | DDR3_A3 |
| | DDR ADDR1 | Y10 | DDR3_A1 | DDR3_A12 | DDR3_A12 |
| | DDR ADDR2 | W14 | DDR3_A2 | DDR3_A2 | DDR3_A2 |
| | DDR ADDR3 | AB14 | DDR3_A3 | DDR3_A7 | DDR3_A7 |
| | DDR ADDR4 | W10 | DDR3_A4 | DDR3_A15 | DDR3_A15 |
| | DDR ADDR5 | Y16 | DDR3_A5 | DDR3_A9 | DDR3_A9 |
| | DDR ADDR6 | AA10 | DDR3_A6 | DDR3_A6 | DDR3_A6 |
| | DDR ADDR7 | AA16 | DDR3_A7 | DDR3_A13 | DDR3_A13 |
| | DDR ADDR8 | AB11 | DDR3_A8 | DDR3_A8 | DDR3_A8 |
| | DDR ADDR9 | AA12 | DDR3_A9 | DDR3_A0 | DDR3_A0 |
| | DDR ADDR10 | Y8 | DDR3_A10 | DDR3_A10 | DDR3_A10 |
| | DDR ADDR11 | Y11 | DDR3_A11 | DDR3_A1 | DDR3_A1 |
| | DDR ADDR12 | AB9 | DDR3_A12 | DDR3_A11 | DDR3_A11 |
| | DDR ADDR13 | Y15 | DDR3_A13 | DDR3_A5 | DDR3_A5 |
| | DDR ADDR14 | AA11 | DDR3_A14 | DDR3_A14 | DDR3_A14 |
| | DDR ADDR15 | W12 | DDR3_A15 | DDR3_A4 | DDR3_A4 |

The modifications are described as follows, as shown in [Figure 2-5](#) and [Figure 2-6](#):

- Copy the trace routing design for Hi3798MDMO1D, including the trace width, air gap between traces, air gap between traces and GND, power trace routing, and trace length.
- Shift the ADDR signal trace at the master chip end rightwards by one ball (compared with the Hi3798MDMO1D DDR) and fine-tune the ADDR trace length. Ensure that the air gap between traces is greater than 10 mils.

Figure 2-5 Top side of the 4-layer PCB (DDR layout)

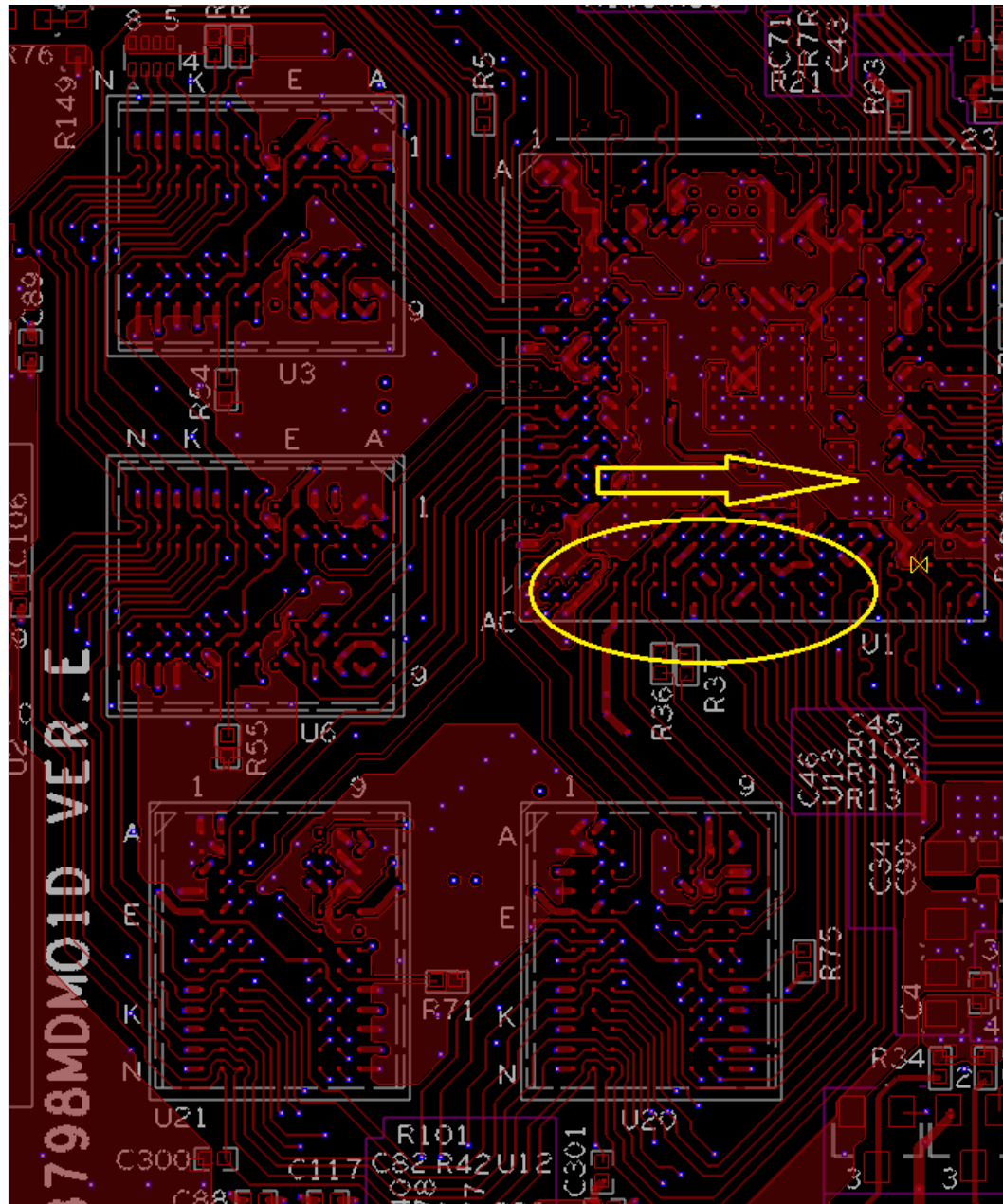
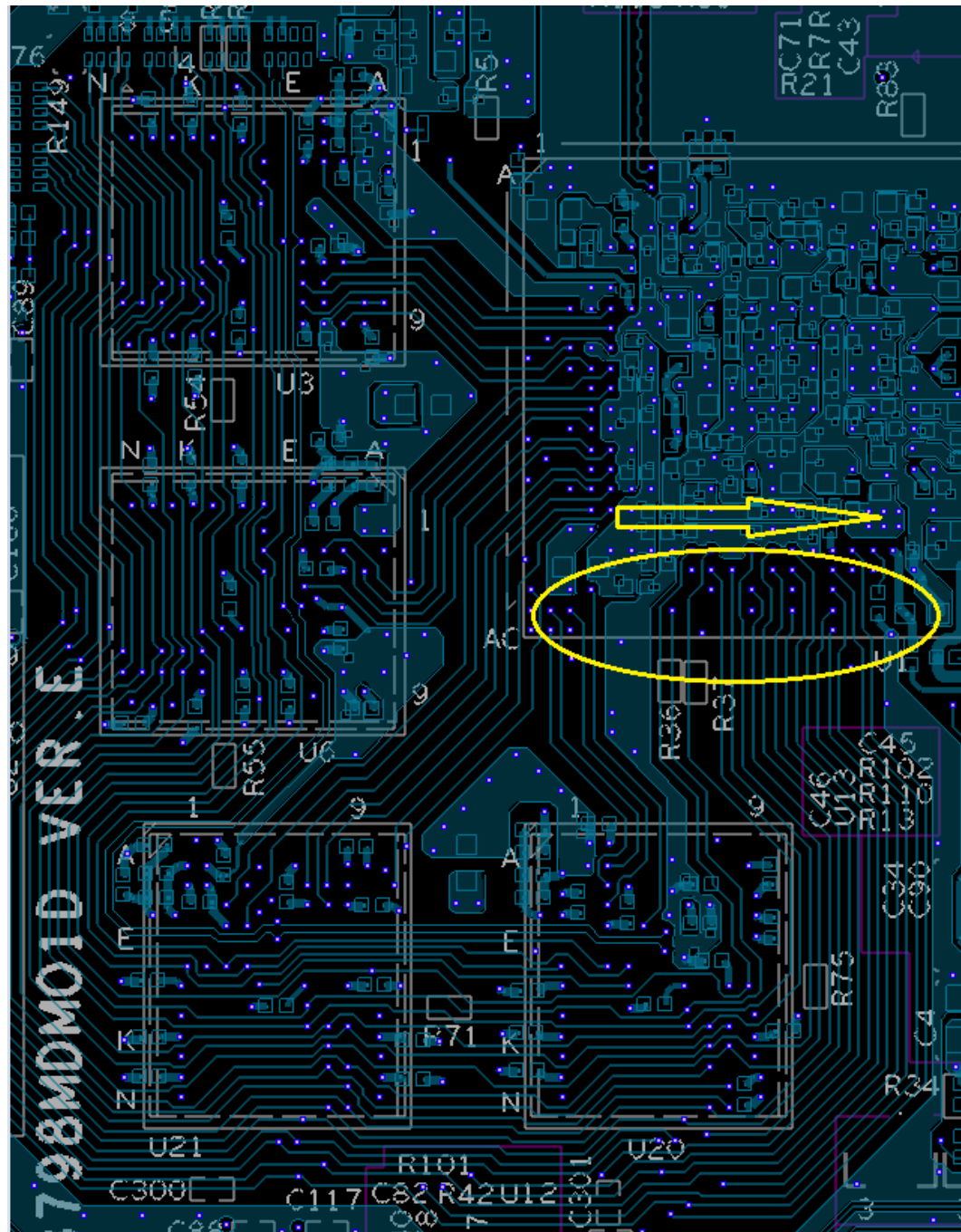


Figure 2-6 Bottom side of the 4-layer PCB (DDR layout)



- Fastboot configuration table

The fastboot configuration table is **hi3796mv100_ddr3_2gbyte_8bitx4_4layers.xlsm** in the SDK.

Configure the pin multiplexing relationship in the table based on actual application and set unused I/O pins to GPIO mode.



CAUTION

- Verify the DDR stability carefully if the board uses a new DDR solution.
 - Ensure that the schematic diagram and PCB are reviewed by HiSilicon FAEs before populating the PCB.
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