Hi3796M V100 Hardware Design

FAQs

Issue **00B02**

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About This Document

Purpose

This document describes the solutions to frequently asked questions (FAQs) for the hardware design of Hi3796M V100.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3796M	V1*XX*

Intended Audience

This document is intended for:

- Technical support personnel
- Hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B02 (2015-05-15)

This issue is the second draft release, which incorporates the following change:

Chapter 2 "Small System" is added.

Issue 00B01 (2015-01-20)

This issue is the first draft release.

Contents

Figures

1 Peripherals

1.1 How Do I Optimize the Electrical Specifications of the SCI Circuit?

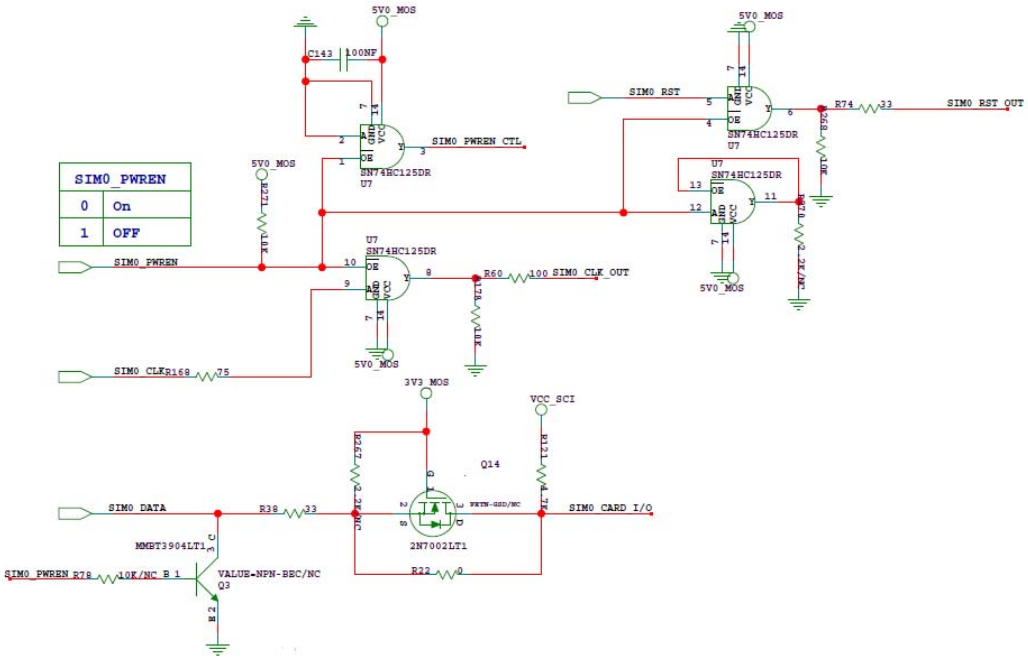
Problem Description

The SCI circuit of the Hi3716C V200 CA solution for a customer fails the electrical specifications certification test. The SCI circuit of Hi3796MDMO1A is the same, and the issue persists.

Solution

- Connect SIM_PWREN to a 10 kΩ (instead of 2.2 kΩ) pull-up resistor and then to 5V_MOS (instead of 3V3_MOS).
- Change the pull-down resistor for SIM0_CLK_OUT from 2.2 kΩ to 10 kΩ, and connect SIM0_CLK_OUT to a 100 Ω resistor in series.
- Modify the SIM0_DATA circuit, as shown in Figure 1-1.

Figure 1-1 SCI circuit with optimized electrical performance



2 Small System

2.1 How Do I Design the 2-Layer PCB with Two 16-Bit DDR SDRAMs?

Problem Description

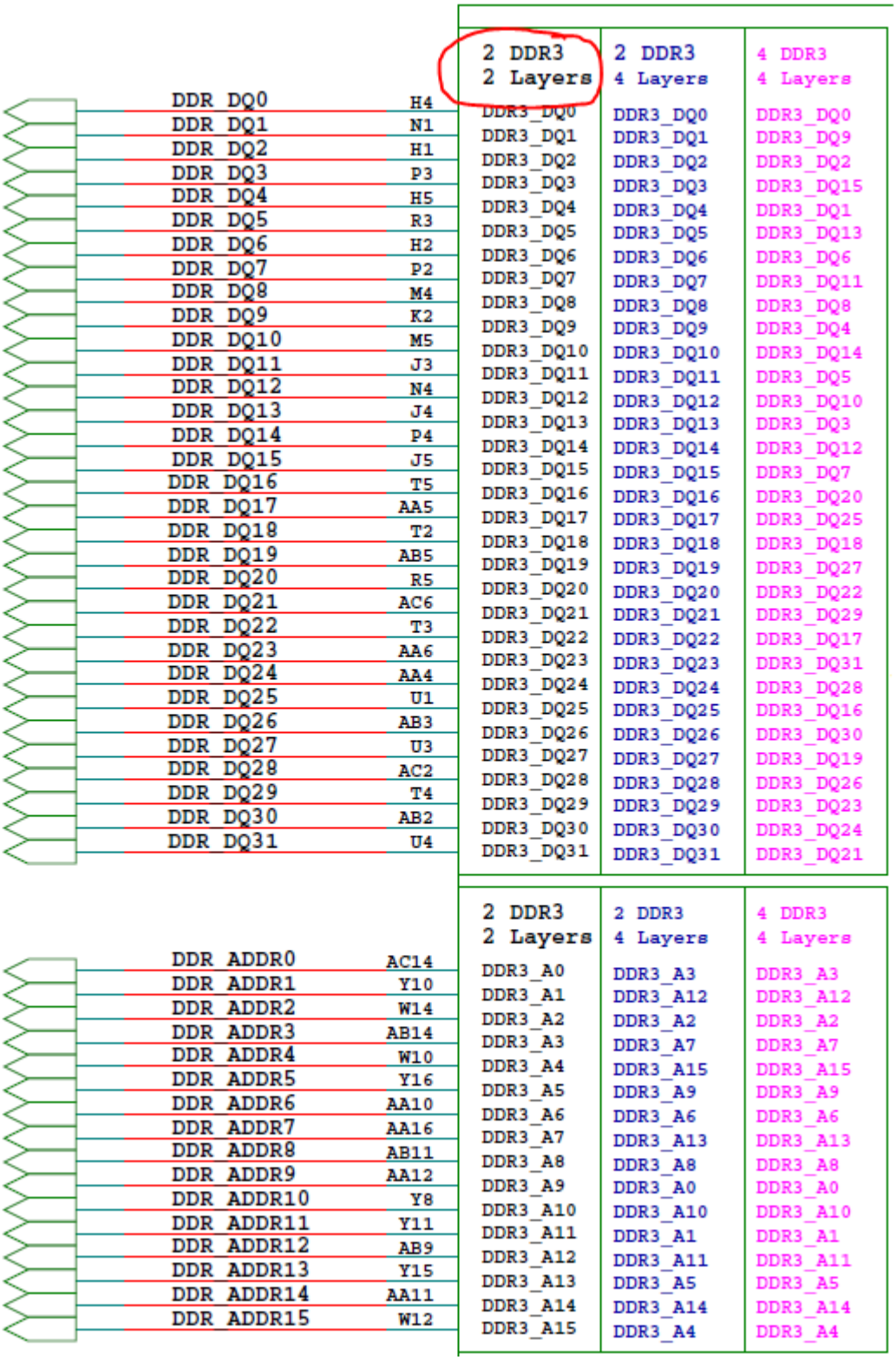
HiSilicon provides reference design only for the 4-layer PCB with two 16-bit DDR SDRAMs. How do I design the 2-layer PCB with two 16-bit DDR SDRAMs?

Solution

- Reference design for the schematic diagram and PCB

  For details about the schematic diagram, see the Hi3798MDMO1B hardware release package. Ensure that the signal names are consistent with those of the Hi3798MDMO1B. For the DQ and ADDR pins, select the names in the **2 DDR3 2 Layers** column, as shown in Figure 2-1.

Figure 2-1 Schematic diagram for the 2-layer PCB with two DDRs



Compared with the Hi3798M V100 BGA package, Hi3796M V100 has two more GND pins (AH2 and AG2) in the lower left corner of the DDR pin map, and the DDR pin map

is shifted rightwards by one ball on the bottom side. You can copy the PCB design of the Hi3798MDMO1B DDR part for Hi3796M V100 and modify the copper plane in the positions of the two additional GND pins.

The modifications are described as follows, as shown in Figure 2-2 and Figure 2-3:

- Copy the trace routing design for Hi3798MDMO1B, including the trace width, air gap between traces, and air gap between traces and GND, power trace routing, and trace length.
- Shift the ADDR signal trace under the master chip rightwards by one ball (compared with the Hi3798MDMO1B DDR) and fine-tune the ADDR trace length. Adjust the surrounding copper plane of the signal (except the area under the BGA chip) to ensure that the width of the copper plane is greater than or equal to the via outer diameter.
- Ensure that the surrounding GND of signals connects to the master chip end and the GND under the BGA chip. See the ellipses and rectangle in yellow in Figure 2-2 and Figure 2-3.

Figure 2-2 Top side of the 2-layer PCB (DDR layout)

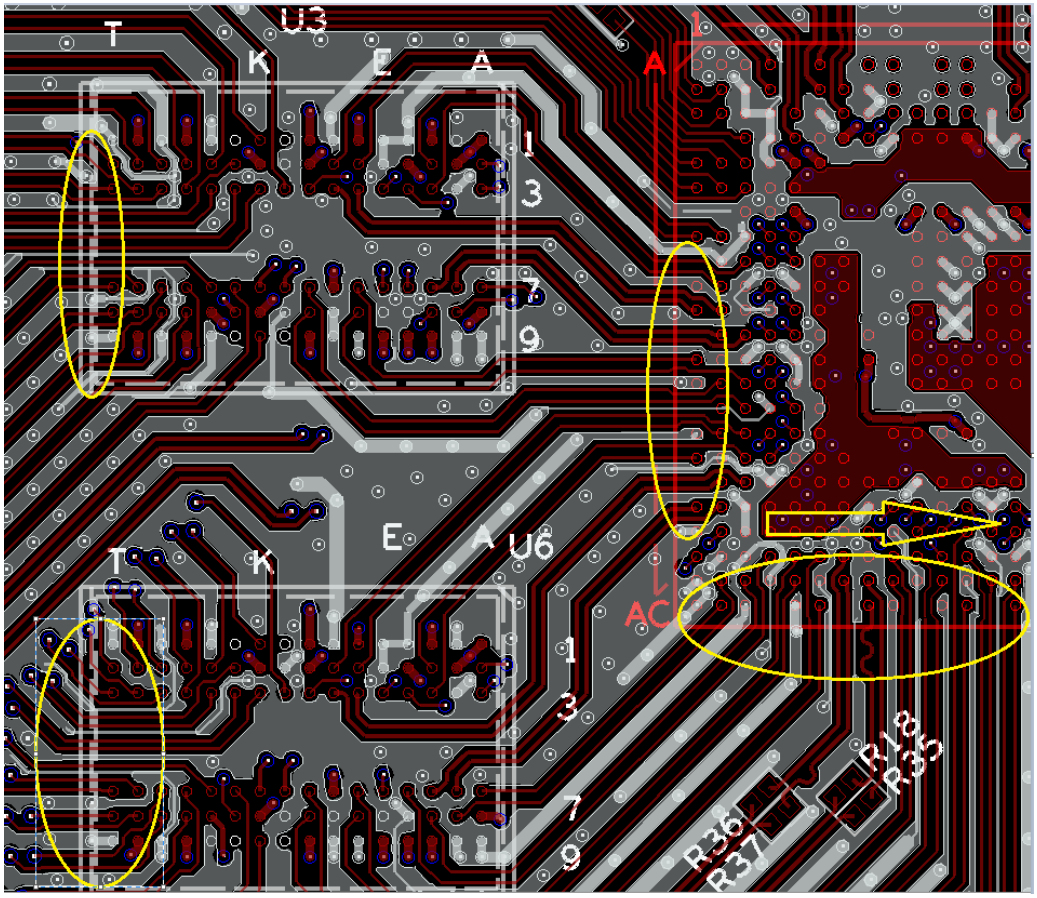
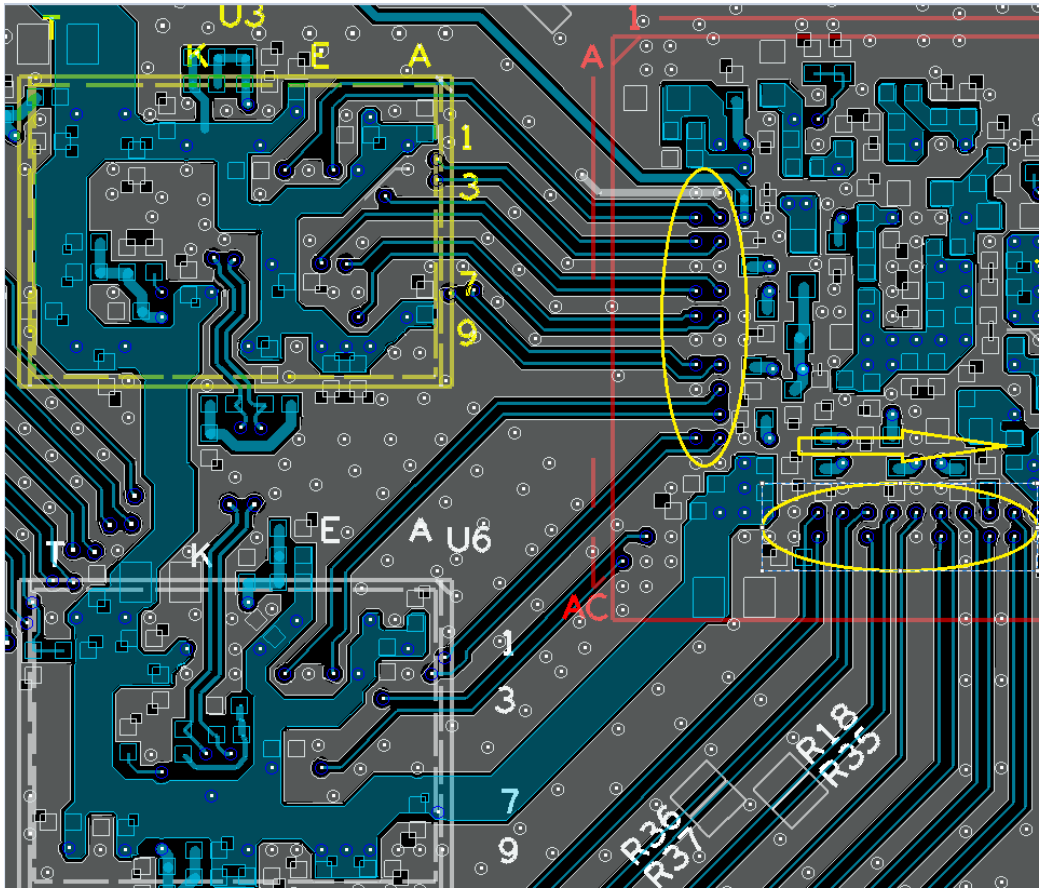


Figure 2-3 Bottom side of the 2-layer PCB (DDR layout)



- Fastboot configuration table

  The fastboot configuration table is **hi3796mv100_ddr3_1gbyte_16bitx2_2layers.xlsm** in the SDK.

  Configure the pin multiplexing relationship in the table based on actual application and set unused I/O pins to GPIO mode.

CAUTION

- Verify the DDR stability carefully if the board uses a new DDR solution.
- Ensure that the schematic diagram and PCB are reviewed by HiSilicon FAEs before populating the PCB.

2.2 How Do I Design the 4-Layer PCB with Four 8-Bit DDR SDRAMs?

Problem Description

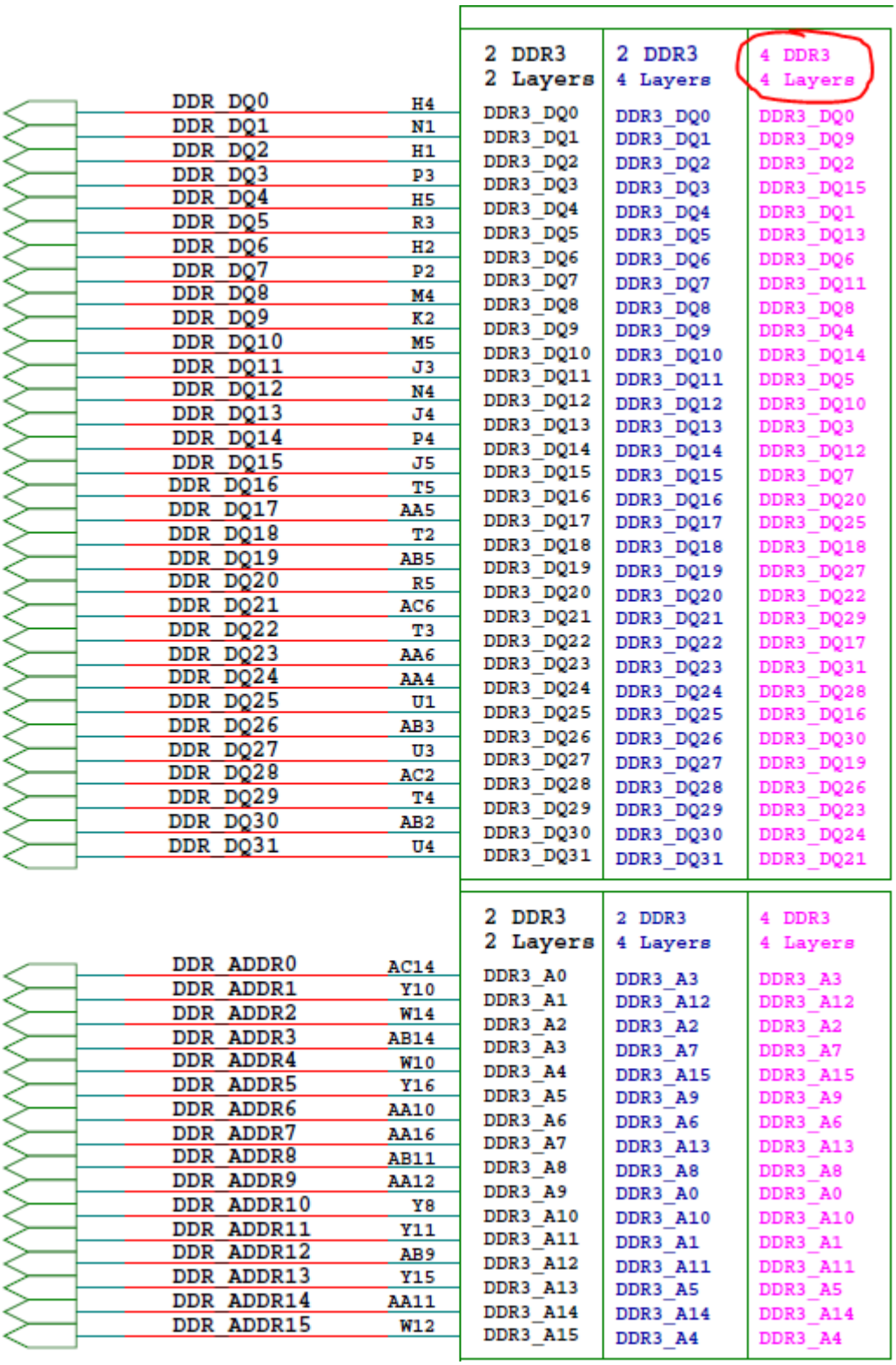
HiSilicon provides reference design only for the 4-layer PCB with two 16-bit DDR SDRAMs. How do I design the 4-layer PCB with four 8-bit DDR SDRAMs?

Solution

- Reference design for the schematic diagram and PCB

  For details about the schematic diagram, see the Hi3798MDMO1D hardware release package. Ensure that the signal names are consistent with those of the Hi3798MDMO1D. For the DQ and ADDR pins, select the names in the **4 DDR3 4 Layers** column, as shown in Figure 2-4.

Figure 2-4 Schematic diagram for the 4-layer PCB with four DDRs



The modifications are described as follows, as shown in Figure 2-5 and Figure 2-6:

- Copy the trace routing design for Hi3798MDMO1D, including the trace width, air gap between traces, air gap between traces and GND, power trace routing, and trace length.
- Shift the ADDR signal trace at the master chip end rightwards by one ball (compared with the Hi3798MDMO1D DDR) and fine-tune the ADDR trace length. Ensure that the air gap between traces is greater than 10 mils.

Figure 2-5 Top side of the 4-layer PCB (DDR layout)

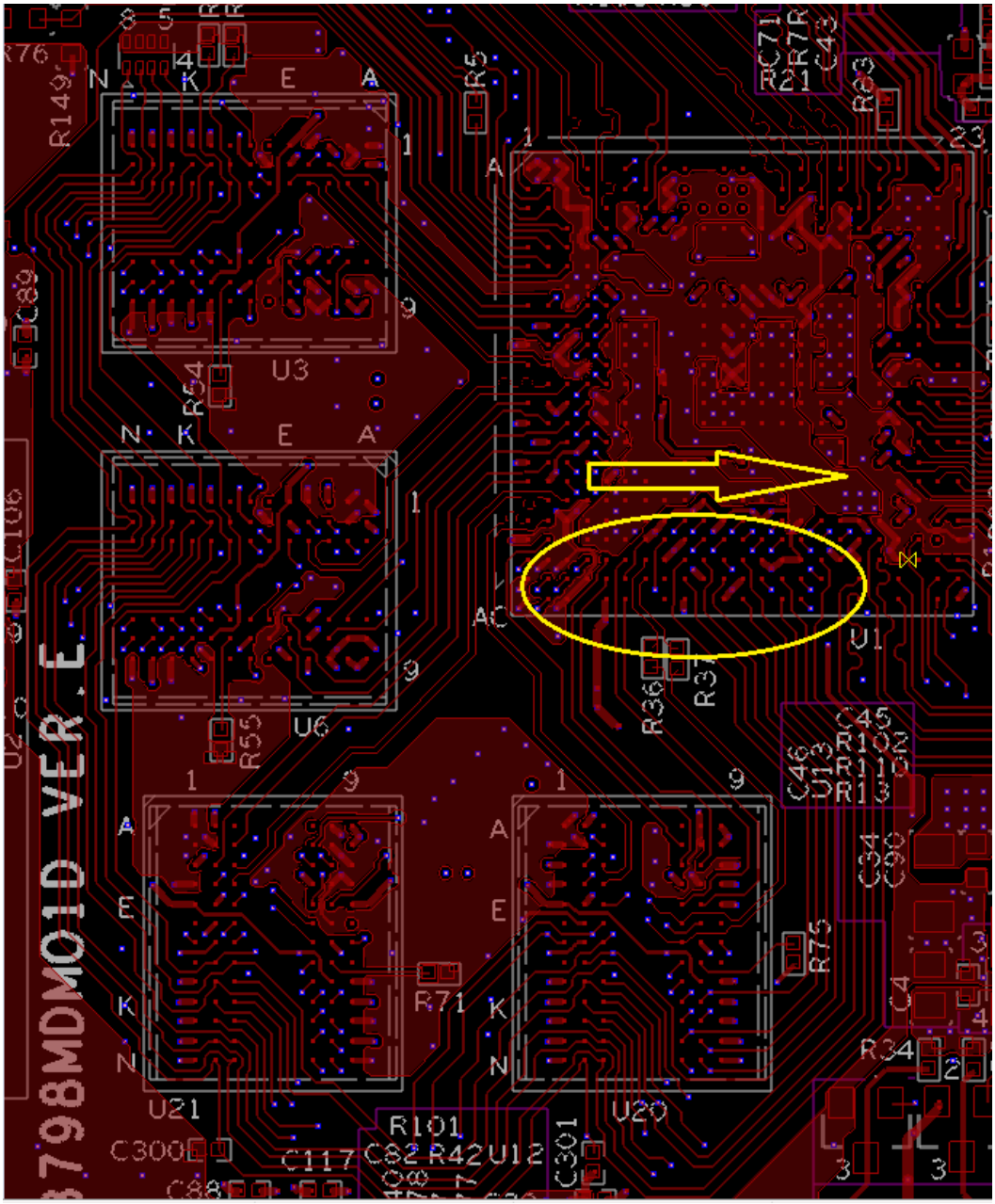
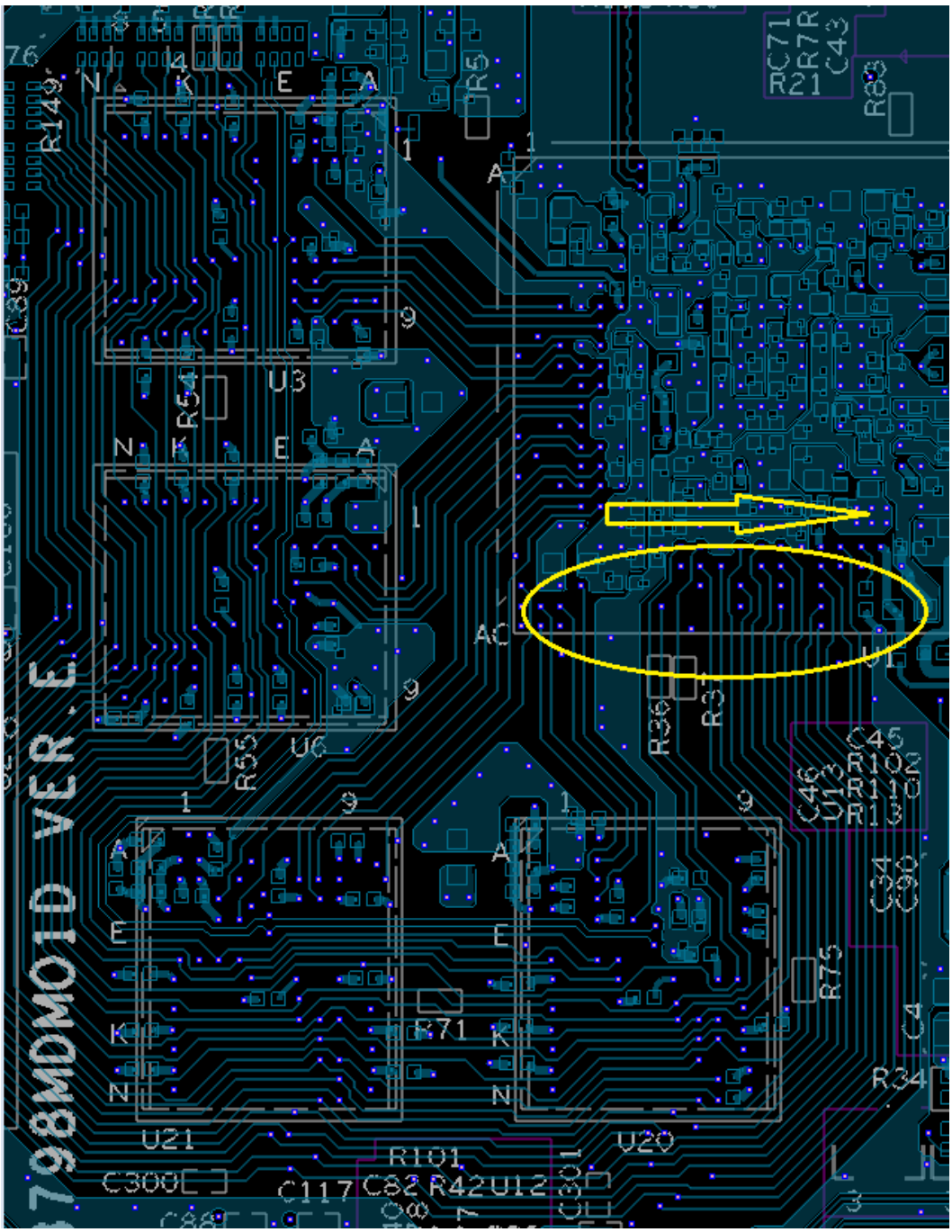


Figure 2-6 Bottom side of the 4-layer PCB (DDR layout)



- Fastboot configuration table

  The fastboot configuration table is **hi3796mv100_ddr3_2gbyte_8bitx4_4layers.xlsm** in the SDK.

  Configure the pin multiplexing relationship in the table based on actual application and set unused I/O pins to GPIO mode.

CAUTION

- Verify the DDR stability carefully if the board uses a new DDR solution.
- Ensure that the schematic diagram and PCB are reviewed by HiSilicon FAEs before populating the PCB.