Hi3137 V100 Hardware Design

User Guide

Issue 00B01

Date 2014-03-31

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About This Document

Purpose

This document describes the schematic diagram design and PCB design of the Hi3137 in the application solution design. It provides guidance for the hardware solution design.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3137	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Alerts you to a high risk hazard that could, if not avoided, result in serious injury or death.
 WARNING	Alerts you to a medium or low risk hazard that could, if not avoided, result in moderate or minor injury.

Symbol	Description
CAUTION	Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results.
TIP	Provides a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points in the main text.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B01 (2014-03-31)

This issue is the first draft release.

Contents

Figures

1 Schematic Diagram Design

1.1 RF Circuit Design

NOTE

This section takes Maxlinear MxL603 as an example.

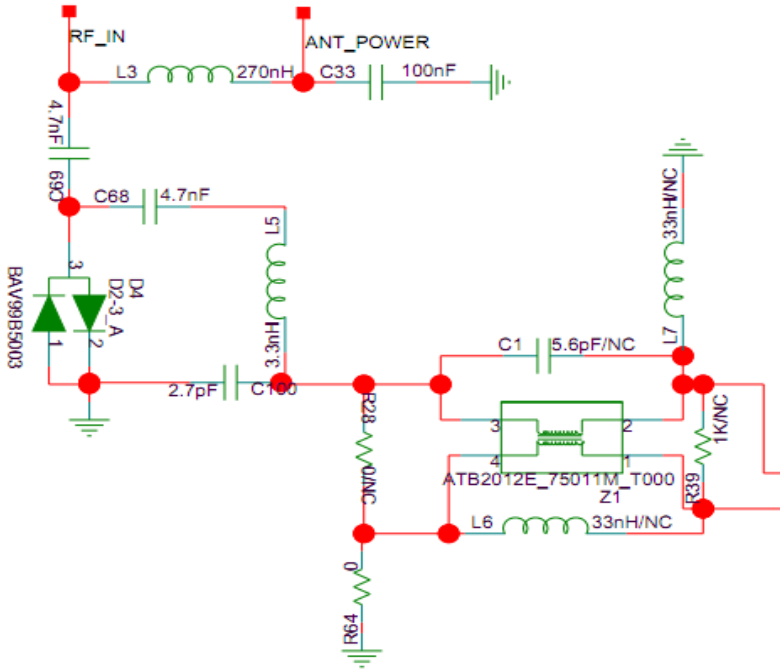
1.1.1 Input Signal Design

The front-end RF signal input design recommendations are as follows:

- Never change the front-end impedance of C68 and C69. Ensure that the capacitance precision of C68, C69, and C100 is within ±5%.
- L3 and L5 are high-frequency inductors. The self resonant frequency of L3 and L5 must be greater than or equal to 3 GHz. L3 is used for filtering ANT_POWER, and its rated current must be 150 mA.
- The LC circuit composed of L5 and C100 improves the anti Wi-Fi interference capability, and D4 improves the electrostatic discharge (ESD) capability externally, enhancing protection of the RF chip.
- Other optional NC components in the schematic diagram do not need to be soldered in normal cases.
- The Z1 technical specifications are as follows:
  - Amplitude imbalance: 0.2 dB (Typ)
  - Phase imbalance: 1 degree (Typ)
  - Insertion loss: 0.5 dB (Typ)

Figure 1-1 shows the RF input design.

Figure 1-1 RF input design



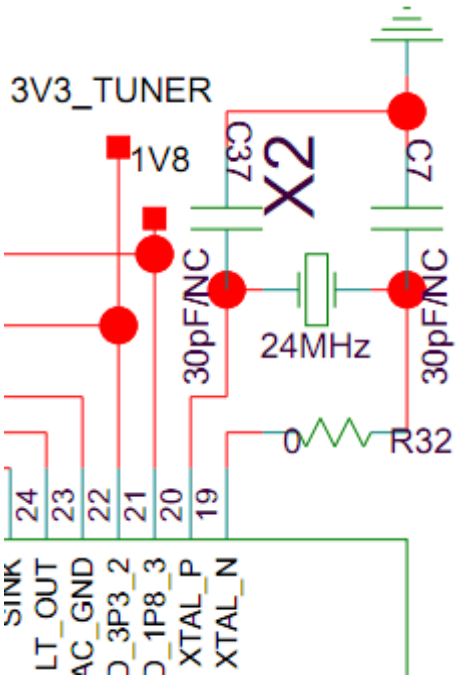
1.1.2 Load Capacitors of the Crystal Oscillator

Design recommendations for load capacitors of the crystal oscillator are as follows:

- The MxL603 supports the 24 MHz or 16 MHz crystal oscillator, and the 24 MHz clock is used currently.
- External load capacitors C7 and C37 are reserved and do not need to be soldered in normal cases because the MxL603 allows 1–31 pF capacitance to be adjusted internally.
- The adjustment step of the adjustable load capacitor in the MxL603 is 1 pF. If the external loads require more than 31 pF, C7 and C37 are used.

Figure 1-2 shows the RF crystal oscillator circuit.

Figure 1-2 RF crystal oscillator circuit



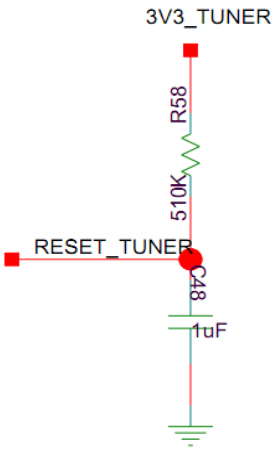
1.1.3 Reset Circuit

The RF chip has no special requirements on the power-on and power-off sequences. However, it imposes the following requirements on the reset circuit:

- The low level of the reset circuit must be retained longer than or equal to 10 μs after the power supplies are turned on.
- It is recommended that R58 be 510 kΩ and C48 be 1 μF.

Figure 1-3 shows the reset circuit.

Figure 1-3 Reset circuit



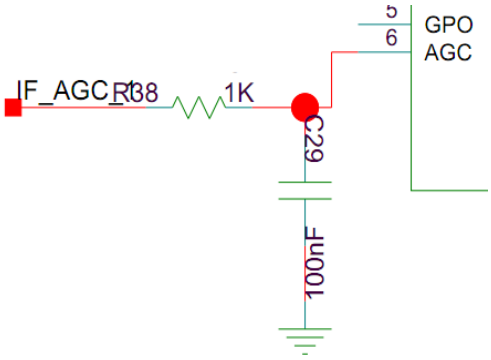
1.1.4 AGC Circuit

The automatic gain control (AGC) circuits include the AGC circuit at the Demod end and that at the RF end. You need to confirm with the RF chip vendor whether the provided AGC circuit is for the RF end or the Demod end. The following describes requirements on the AGC circuit at the RF end:

- R38 is 1 kΩ and C29 is 100 nF.
- The RC filtering circuit must be designed close to the MxL603 on the PCB to protect IF_AGC against noise interference.

See Figure 1-4.

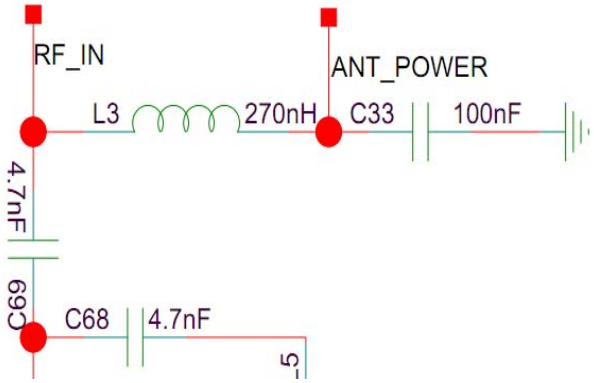
Figure 1-4 RF AGC circuit



1.1.5 Feedback Circuit

The RF signal input end and the antenna power belong to the same network. Pay attention to the matched impedance at the antenna power end during design. Do not place the filtering capacitor of the antenna power at the signal input end; otherwise, the RF input signal integrity may be affected. See Figure 1-5. Note that C33 needs to be placed in the antenna power branch during PCB design.

Figure 1-5 RF feedback circuit



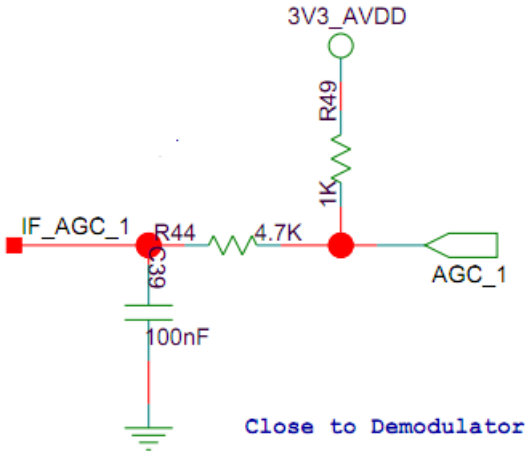
1.2 Hi3137 Circuit Design

1.2.1 AGC Circuit

The following describes requirements on the AGC circuit at the Demod end (see Figure 1-6):

- R49 is a 1 kΩ pull-up resistor. It must be connected; otherwise, the RF chip sensitivity is affected.
- R44 (4.7 kΩ) and C39 (100 nF) must be placed close to the Demod to prevent the AGC circuit from interfering with the board.

Figure 1-6 Hi3137 AGC circuit

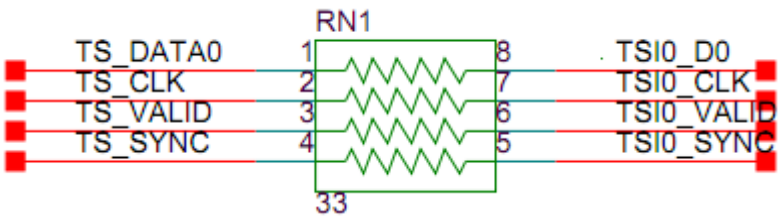


1.2.2 TS Circuit

Figure 1-7 shows some circuits for parallel TS outputs.

- The current serial resistor is 33 Ω in the parallel design.
- In the serial design, small capacitors cannot be connected to the serial TS output interface in parallel. Otherwise:
  - The TS clock edge becomes gentle, which affects sampling.
  - The Vpp decreases, which results in data loss and then mosaics during video output.
- You can reserve some space for capacitors or the T-shape filtering circuit for the concern of electromagnetic compatibility (EMC).

Figure 1-7 TS circuit



2 PCB Design

2.1 RF Circuit Design

Note the following during PCB layout:

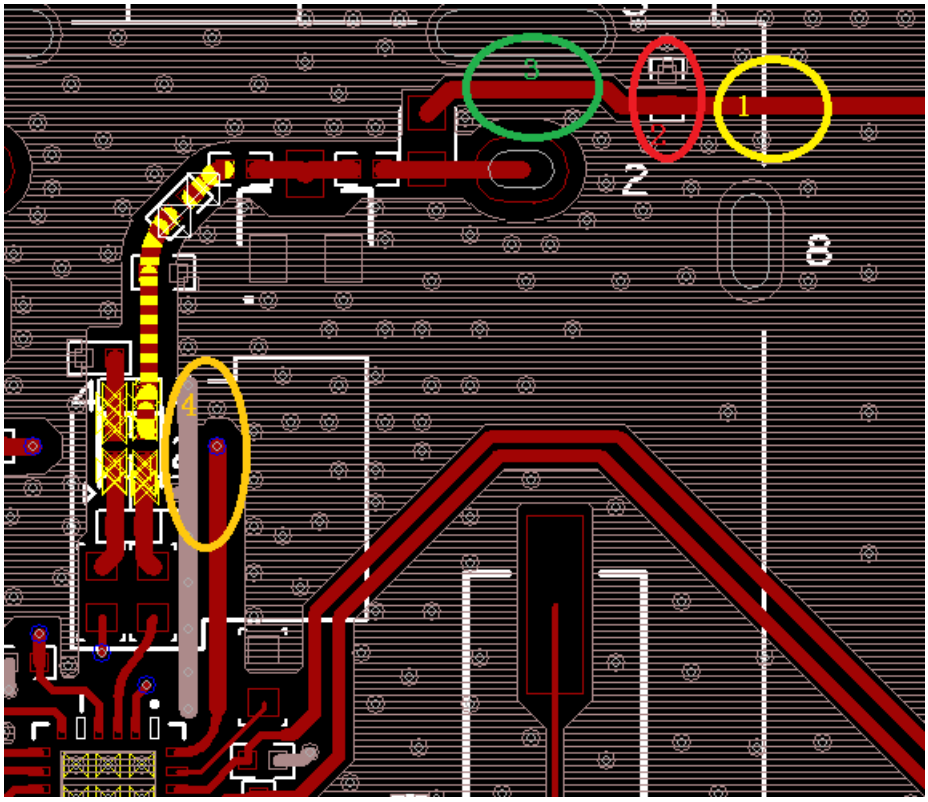
- Width of major signal traces
- Impedance
- Anti-interference capability
- Through-current capability

2.1.1 Input Signal Design

Requirements on the RF input-end signals are as follows:

- The signal matched impedance is 75 Ω.
- Do not route signal traces through vias or across the bottom layer, and ensure signal integrity of the GND layer.
- Surround RF signal traces with GND traces and connect the traces to GND vias to ensure relatively continuous low impedance, facilitate the release of high-frequency energy, and avoid the spur.
- The RF input signal traces should be straight if possible.
- Never route traces at an angle of 90 degrees to reduce signal loss.

Figure 2-1 RF input signal PCB design



2.1.2 Signal Traces of the Antenna Feedback Circuit

Requirements on signal traces of the antenna feedback circuit are as follows:

- The trace width is 15 mils to ensure the through-current capability of the feedback circuit traces.
- Place the matched capacitor (see the red ellipse 2 in Figure 2-1) at the feedback circuit end but not the RF signal input end to avoid signal attenuation due to mismatched impedance for RF signals.
- Isolate the feedback circuit from the RF input end by using the GND plane (see the green ellipse 3 in Figure 2-1). The GND plane width must be 2–3 times the trace width.
- The feedback circuit trace in the green ellipse 3 is routed along the board edge. Surround the circuit in this area with GND traces (with 2–3 times the trace width) to avoid radiation and interference with the RF chip.

2.1.3 Filtering Capacitors of the RF Power

- Connect each capacitor to the GND separately close to the RF chip through vias.
- Provides a smooth signal reflow path and reduce the parasitic inductance.

2.1.4 RF LT Signals

The RF loopthrough (LT) signals (see the golden ellipse 4 in Figure 2-1) are on the right of the RF signal input end. Isolate the LT traces from the RF input signal end by using the GND plane (with the width greater than or equal to 20 mils) to avoid mutual interference.

2.1.5 Shielding Case of the RF Input Signals

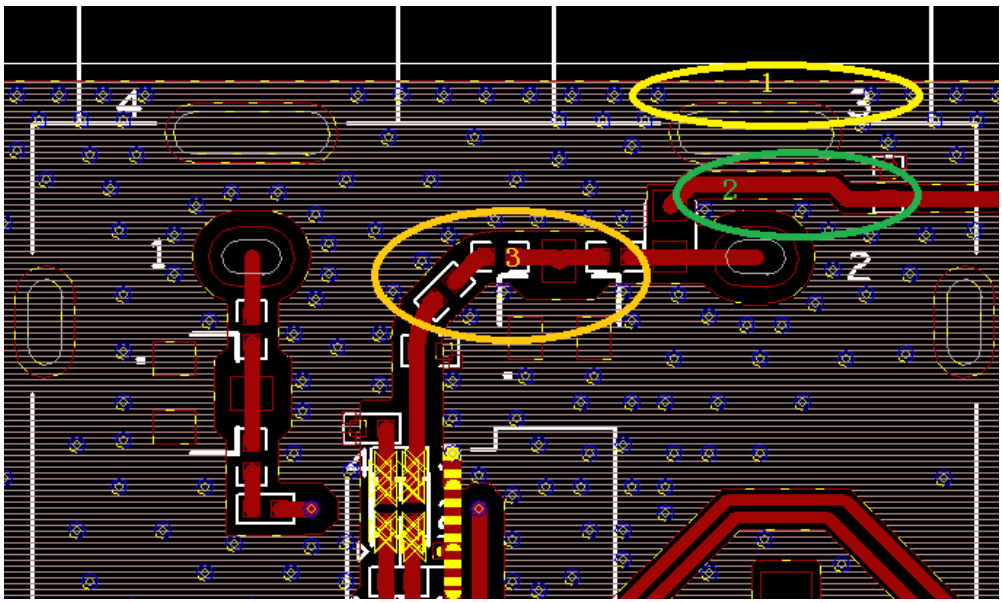
The yellow ellipse 1 in Figure 2-2 shows the layout of the shielding case for RF input signals.

- The board edge and mounting holes of the shielding case must be protected by using the GND plane (with the width greater than or equal to 35 mils).
- The length of the mounting holes of the shielding case must be less than or equal to (1/20) x λ. λ indicates the wave length of the RF input signal frequency. The length of the mounting holes of the shielding case cannot be greater than 0.7 cm. The shorter, the better. This avoids high-frequency radiation.

CAUTION

If you need to route the signal traces across the RF signal input end (below the green ellipse) due to the layout space limit, you cannot route the traces across the top or bottom layer in the golden ellipse. You can route the traces between the yellow ellipse and the green ellipse. However, you need to isolate the signal traces by using the GND plane, and the GND plane width must be 2–3 times the signal trace with.

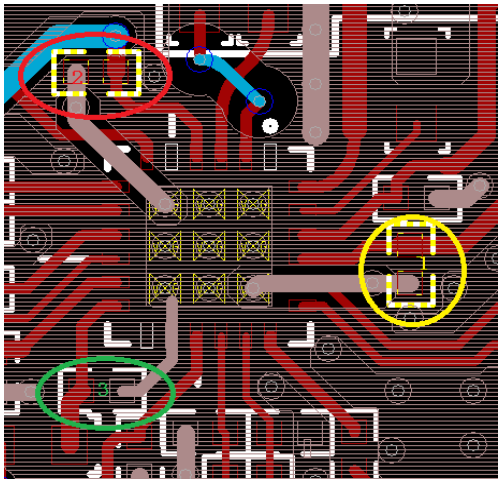
Figure 2-2 RF front-end shielding design



2.1.6 Key Decoupling Capacitors

The power decoupling capacitors need to be placed close to the IC pins and connect to the GND through separate vias. In the MxL603 design, C32 (see the yellow circle area 1 in Figure 2-3) is placed close to the corresponding IC pin, and the GND is connected to the exposed pad (EPAD) at the bottom of the RF chip. The layout design for C40 (see the red ellipse 2 in Figure 2-3) and C35 (see the green ellipse 3 in Figure 2-3) is similar to that for C32.

Figure 2-3 Decoupling capacitors on the PCB



2.1.7 AGC Signal Traces

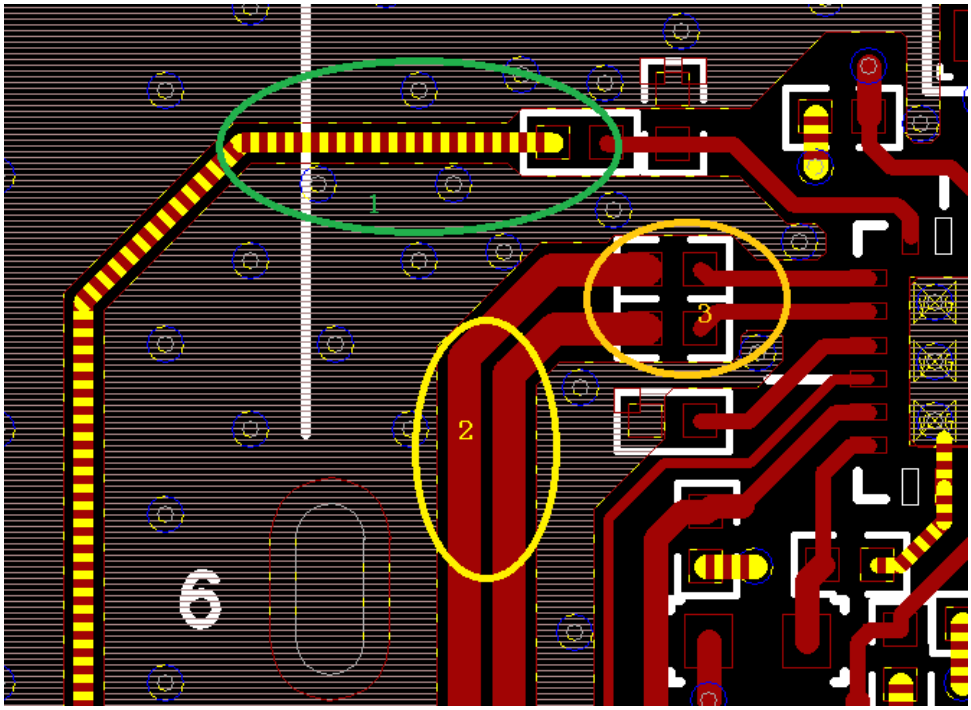
The green ellipse 1 in Figure 2-4 shows the layout of AGC signal traces. The trace width must be greater than or equal to 10 mils. The AGC signal traces must be surrounded by GND traces. You can route the AGC traces across the bottom layer. However, note that the reference GND layer for key signal traces such as the IQ signal traces cannot be affected.

2.1.8 IQ Signal Traces

Requirements on the IQ signal traces are as follows:

- The width of IQ signal traces must be greater than or equal to 8 mils. IFOUTP and IFOUTN are routed as differential traces and isolated by using GND traces. Signal traces cannot be routed on the bottom layer GND. See the yellow ellipse 2 in Figure 2-4.
- The matched capacitors for IQ signals must be placed close to the RF chip to avoid interference. See the golden ellipse 3 in Figure 2-4.

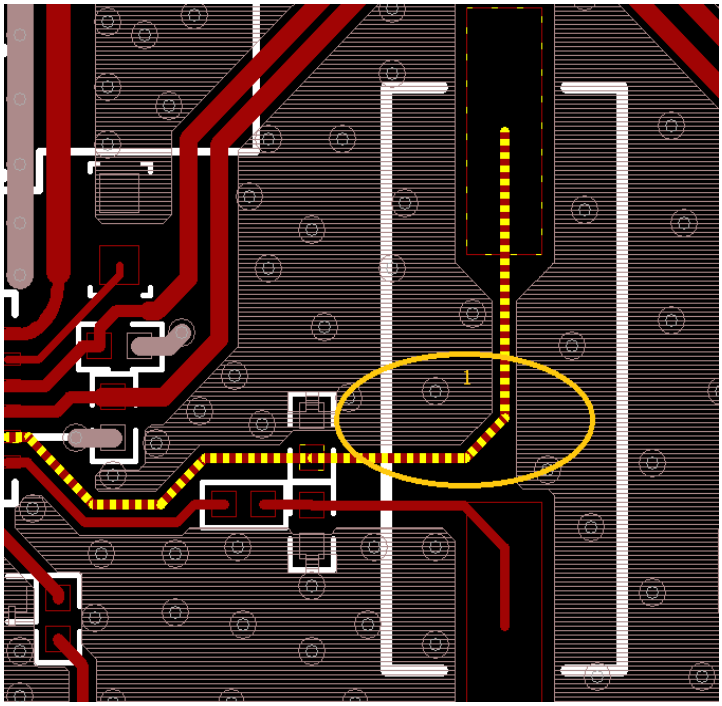
Figure 2-4 IQ signals on the PCB



2.1.9 Crystal Oscillator Circuit

The golden ellipse 1 in Figure 2-5 shows the layout of traces for the crystal oscillator circuit. The trace width must be greater than or equal to 10 mils. The crystal oscillator area (top and bottom layers) must have complete GND and many GND vias (for releasing noises of the crystal oscillator).

Figure 2-5 RF crystal oscillator circuit on the PCB

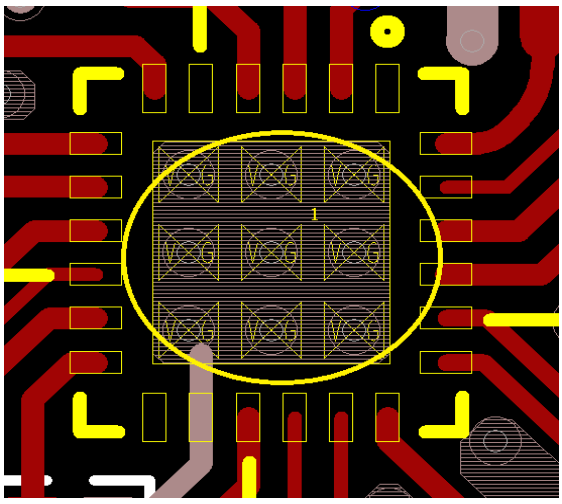


2.1.10 EPAD

In the PCB layout design, typically a GND pad is located on the rear side of the RF chip. An EPAD needs to be designed at the solder mask top layer and the solder mask bottom layer. Nine vias need to be punched and the recommended via diameter is 0.3 mm. These vias have the following functions:

- Facilitate heat dissipation of the RF chip.
- Ensure integrity of the top and bottom layer GND and facilitate the release of high-frequency energy. See Figure 2-6.

Figure 2-6 EPAD design

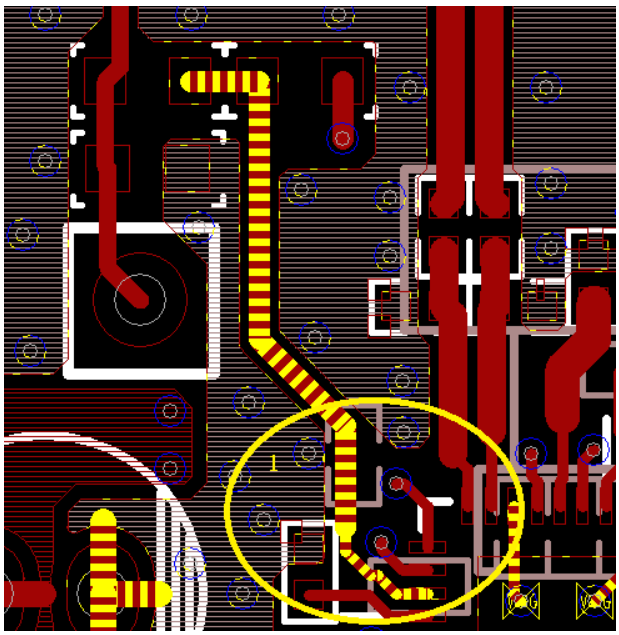


2.2 Hi3137 PCB Design

2.2.1 AGC Traces

- The AGC traces must be surrounded by GND traces and the trace width must be greater than or equal to 10 mils. See the yellow ellipse in Figure 2-7.
- The pull-up resistor and RC filtering circuit must be placed close to the AGC output interface to prevent the AGC high-frequency component from interfering with the board and affecting the performance.

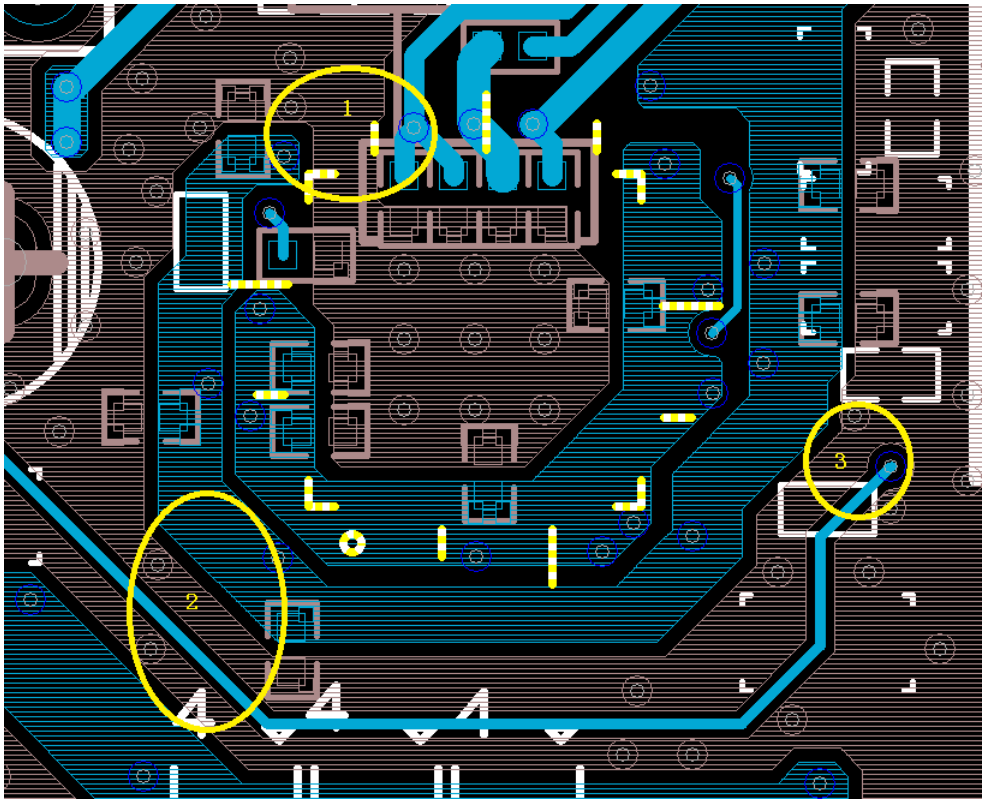
Figure 2-7 AGC PCB design



2.2.2 Bottom Layer

The yellow ellipses in Figure 2-8 show the Hi3137 bottom layer design. The 1.1 V and 3.3 V power traces are routed at the bottom layer of the Demod chip to ensure the GND integrity.

Figure 2-8 Hi3137 bottom layer design



2.2.3 TS Output Traces

Requirements on the matched impedance of the TS output traces vary according to the 2-layer and 4-layer PCBs. For details, see chapter 3 "Hardware Design" in the *Hi3137 Data Sheet*.

The TS_CLK trace must be surrounded by GND traces in serial mode. The width of GND traces must be 2–3 times the trace width, and the bottom layer GND must be complete.

2.2.4 EPAD

The Hi3137 has a GND pad at the bottom. In the PCB design, an EPAD needs to be designed at the solder mask top layer, as shown in the yellow ellipse in Figure 2-9.

Figure 2-9 EPAD design