Hi3130 V200 Brief Data Sheet

Key Specifications

- DVB-C and ITU J83-A/B/C standards
- 16-/32-/64-/128-/256-QAM demodulation
- Integrated high-performance 12-bit IF ADC to provide IF solutions and low- and intermediate-frequency solutions
- Adaptive digital down sampling and anti-aliasing filtering, symbol rate ranging from 0.87 Mbaud/s to 7.19 Mbaud/s
- Adaptive digital carrier recovery and maximum ±800 kHz frequency offset
- Adaptive digital timing recovery and maximum ±1% symbol rate deviation
- Automatic selection of the matched filter based on the bandwidth and support for the raised cosine roll-off factor ranging from 0.12 to 0.18
- Adaptive blind equalization and decree feedback equalization to correct micro-reflection and typical distortion in the cable channel
- Integrated FEC decoding, complying with the ITU J83-A/B/C standard.
- Dual AGC
- Internal register control and monitoring over a two-wire bus
- Signal quality monitoring in real time
- Chip working status indicator
- Compatibility with DVB common interface standards
- TS output in serial or parallel mode
- Automatic spectrum inversion recognition and correction
- Integrated PLLs, requiring only an external low-frequency passive crystal or sharing the same clock source with the decoder chip and demodulator
- An integrated crystal oscillator circuit with the system clock generated internally by using the external passive crystal
- Low-power design with typical power consumption at 200 mW when the symbol rate is 6.875 Msps
- Software-controlled power-saving mode.
- QFN40 package
- 1.2/3.3 V operating voltage

Application Fields and Typical Application Diagram

- Cable tuner
- Cable STB and integrated digital TV
- Cable modem and digital TV card

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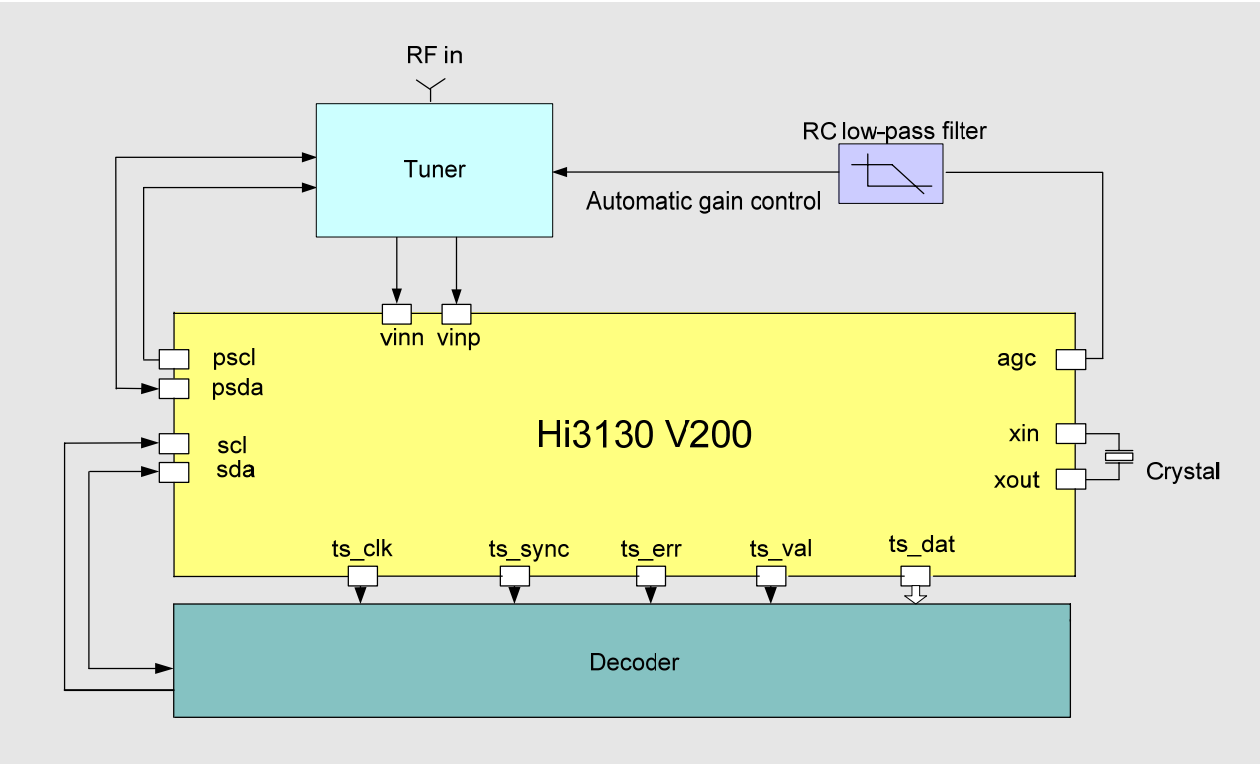
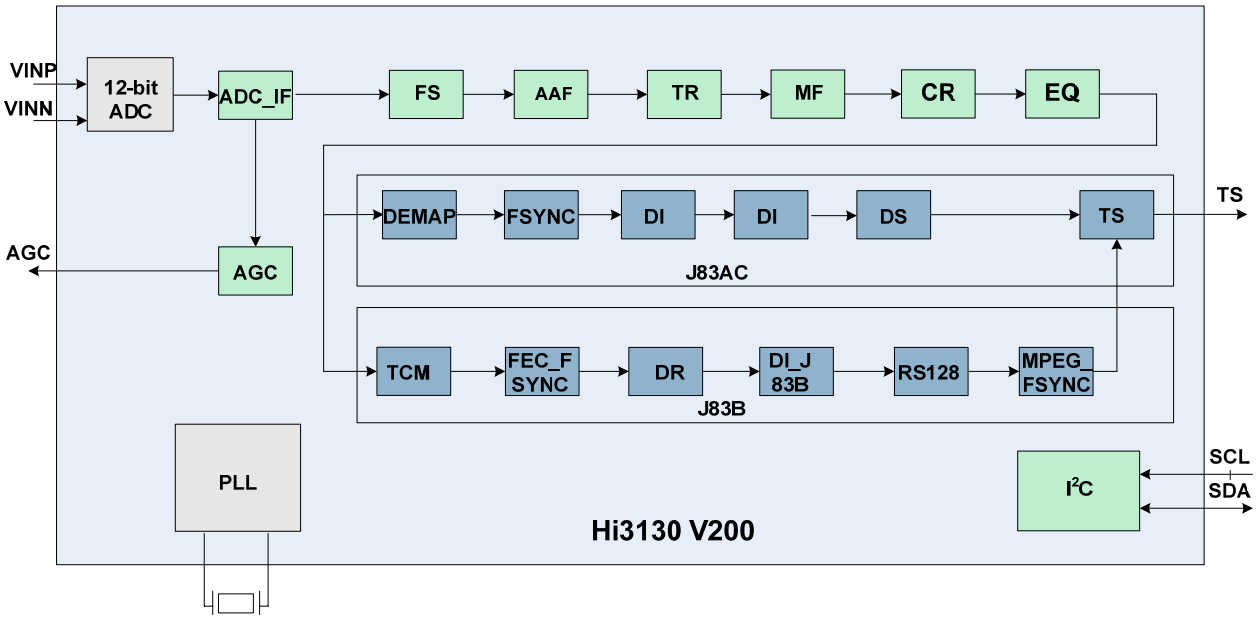
Issue: 00B01
Date: 2015-06-08



Functional Block Diagram



Hi3130 V200 is a cable digital TV channel receiver chip complying with the DVB-C (ETS 300 429) and ITU J83-A/B/C standards. It supports high-performance 16-/32-/64-/128-/256-QAM demodulation and FEC, implementing complete digital cable signal processing from sampling at the intermediate frequency to outputting MPEG-TSs, and provides solutions for receiving TV signals and other data signals sent through a coaxial cable.

Hi3130 V200 uses the integrated 12-bit and 40 Msps high-performance ADC, which ensures precise sampling of up to 256-QAM signals from the IF. After sampling, all the signals are processed in the digital domain. It provides all required functions based on the complex channel situations, such as demodulation, micro-reflection cancellation, and RS FEC. The chip monitors chip status and signal quality to work with the decoder chip, and provides dual AGC and two-wire buses for tuner control to simplify the board design.
The MPEG-TSs output by Hi3130 V200 comply with standard DVB interfaces and can seamlessly connect to the MPEG decoder.

Acronyms and Abbreviations

DVB-C	digital video broadcasting-cable
ITU	International Telecommunication Union
QAM	quadrature amplitude modulation
ADC	analog-to-digital converter
IF	intermediate frequency
AGC	automatic gain control
DVB	digital video broadcasting
TS	transport stream
PLL	phase-locked loop
QFN	quad flat no-lead package
STB	Set top box
FEC	forwarding equivalence class
MPEG-TS	moving picture experts group-transport stream
RS	Reed Solomon
I^2C	inter-integrated circuit