NAND
User Guide

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About This Document

Purpose

This document describes the precautions and usage of the NAND flash in the HD network media solution.

Intended Audience

This document is intended for:

- Technical support personnel
- Software development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 01 (2015-07-03)

This issue is the first official release.

Issue 00B01 (2013-03-30)

This issue is the first draft release.

Contents

Tables

1 Risks

1.1 Data Reliability

The common data reliability issues of the NAND flash are bit errors caused by bit inversion. Storage cell bit inversion of the NAND flash may occur in the following scenarios:

- During programming. Caused by programming interference, bit inversion occurs in both programming by using factory burners and programming after the NAND flash is soldered to the board. Programming interference indicates that when a zone of the NAND flash is being programmed, the threshold voltages of some programmed storage cells deviate. Bit inversion is more likely to occur in the multi-level cell (MLC) NAND flash rather than the single-level cell (SLC) NAND flash, because the MLC NAND flash has poor programming anti-interference capability. In addition, data errors also occur if the number of program or erase operations exceed the program/erase (P/E) cycle specified on the NAND flash.
- In read-only mode. Bit inversion still occurs even if you perform only read operations after programming without changing the data, because the threshold voltages of some storage cells deviate during the power-on process.
- During sudden change in temperature, such as board soldering. The NAND flash has low reliability at a high temperature, under which data errors may occur when the NAND flash is read, written, or even left idle.
- During long-term storage. The NAND flash is susceptible to various stresses due to the high-density feature of its circuit. For the MLC NAND flash that has a narrow threshold voltage range, the interference is highly likely to result in bit errors.
- During manufacturing process improvement. Driven by the demand for large-capacity NAND flash memories and pursuit of low cost, NAND flash vendors continuously develop technological innovations to improve their manufacturing process, which is improved from 90 nm to 65 nm, 55 nm, 3X nm, 2X nm, and maybe 1X nm. More cell circuits are implemented on the wafer with the same size, and each cell circuit stores more bits. However, the manufacturing process upgrade brings about more data reliability issues as well as lower costs and larger capacity. The data reliability issues are especially obvious for the MLC NAND flash. Due to its higher circuit density, the NAND flash has a narrower threshold voltage range, resulting in more bit inversion errors.

1.2 Short Lifecycle

The lifecycle of the NAND flash is the number of times that the NAND flash can be programmed and erased. Data errors indicate the end of the NAND flash lifecycle.

The lifecycle of the NAND flash determines its service life and repair rate. For example, assume that the program switchover information is stored to a fixed NAND block. If you switch programs for 20 times a day, and the NAND flash lifecycle is 3000, you can use the NAND flash for at most 150 days (3000/20). After the 150 days, the error occurrence and repair rate both increase.

CAUTION

It is recommended that MLC NAND flash memories be not used in STBs. If MLC NAND flash memories are used, you must estimate the memory lifecycle and repair rate in advance.

Table 1-1 compares the lifecycle of SLC and MLC NAND flash memories with different processes.

Table 1-1 Lifecycle of SLC/MLC NAND flash memories with different processes

NAND	P/E Cycle
34 nm SLC NAND	100000
25 nm SLC NAND	60000
25 nm MLC NAND	3000
20 nm SLC NAND	3000

1.3 Short Data Storage Time

Errors may occur in the data saved in the NAND flash after a period of time, which is usually about ten years.

The program and erase operations affect the data storage time. Table 1-2 lists the data storage time of SLC and MLC NAND flash memories with different P/E cycles.

Table 1-2 Data storage time of SLC/MLC NAND memories with different P/E cycles

NAND	P/E Cycle	Data Storage Time (Year)
25 nm SLC NAND	60000	1
25 nm SLC NAND	6000	5
25 nm MLC NAND	3000	1
25 nm MLC NAND	300	5

The preceding table indicates that data can be stored in the 25 nm MLC NAND flash for only one year after 3000 erase operations. The data is lost after a year even if the MLC NAND flash is no longer used.

2 Precautions

2.1 Randomization

Each cell of the MLC NAND flash uses various voltage levels to represent different data. If the voltage difference between two adjacent cells is large, the bit inversion probability is high. Data randomization indicates that data is randomly stored on the MLC NAND flash with 0 and 1 more evenly distributed, reducing the probability of bit inversion. Note that not all MLC NAND flash memories support the randomization function. For details, consult the memory vendor.

It is tested that randomization increases the MLC NAND flash reliability. This function is supported by the NAND flash controllers and drivers for HiSilicon Hi3716M V300 or later. (For details, consult the logic and hardware personnel.)

You can check whether randomization is supported and enabled by viewing the information displayed during system startup. Take Hi3716M V300 as an example. After randomization is enabled, the following information is displayed:

```
Nand: Hynix H27UBG8T2C Randomizer  //This indicates that randomization is supported by the controller and is enabled.
```

2.2 Read/Write Leveling

It is recommended that the data to be frequently written be saved as files and stored in the YAFFS2 file system. The YAFFS2 file system supports the read/write leveling function to equalize the erase operations of each block on the NAND flash, prolonging the service life of the NAND flash.

For example, if a partition has ten blocks, the read/write leveling function enables data to be evenly written to each block. That is, if the read/write leveling function is used, ten write operations are evenly distributed to ten blocks, with one operation for each block. If the function is not used, the ten write operations may be performed on a single block, which greatly shortens the service life of the block.

The YAFFS2 file system is tailored for the NAND flash. It uses the class log structure and provides loss equalization and power-off protection mechanisms based on NAND flash features to reduce the impact on the consistency and integrity of the file system due to power failures. You are advised to save data to be frequently written to the file system instead of the blocks of the NAND flash.

During upgrading, the write operations are directly performed on the NAND flash. However, the number of upgrade times is far less than the NAND flash lifecycle.

2.3 Read Retry

Some MLC NAND flash memories have low reliability due to manufacturing process issues. Therefore, the read retry function is required to ensure that the read or written data is correct. (Not all MLC NAND flash memories require the read retry function. For details, consult the memory vendor.)

The basic principles of the read retry function are as follows: The memory vendor provides a group of read retry levels for a specific NAND flash memory. When data read by the driver is incorrect, the driver retries by using different levels until the read data is correct or the maximum retry attempts are reached. The read retry function increases the reliability of the MLC NAND flash, but slows down the read operations. This function is supported by the NAND flash controllers and drivers for HiSilicon Hi3716M V300 or later. (For details, consult the hardware personnel.)

You can check whether the read retry function is supported by viewing the information displayed during system startup. Take Hi3716M V300 as an example. If the read retry function is supported, the following information is displayed:

```
Nand: Hynix H27UBG8T2C Randomizer Read-Retry // This indicates that the
read retry function is supported
```

2.4 Reserving Sufficient Space for the YAFFS

It is recommended that the rate of available space in a single YAFFS2 partition be above 25%. The more, the better. Smaller available space indicates more average erase operations on each block when the file is being written or deleted. The lifecycle of the NAND flash can be prolonged if the erase operations on each block are reduced.

Table 2-1 lists the statistics of the YAFFS2 file system. It is concluded that larger available space indicates less erase operations on each block and longer NAND flash lifecycle.

Table 2-1 YAFFS2 file system statistics

YAFFS2 File System Usage	Number of Erase Operations on Each Block	Lifecycle (Assuming that the Lifecycle is 3000)
100%	10–11	300 times
92%	3–4	1000 times
75%	1–2	3000 times

2.5 Erasing Before Writing

The MLC NAND flash can be written only once after it is erased. If you want to write data to the NAND flash again, you need to erase it again. The data in the NAND flash is 0xFF after it is erased. If you write 0xFF to the NAND flash, and then write other data to it, an error may occur because data is written to the NAND flash several times after it is erased.

For the non-read-only file systems, even if you do not write data to the NAND flash, write operations are also performed by the file systems, such as regular trash recycling and data synchronization.

CAUTION

- The read-only file systems such as Cramfs and Squahsf do not have the preceding problem.
- As the kernel and U-boot data is not modified, the preceding problem does not happen.

2.6 Booting from the NAND Flash

For all master chips of HiSilicon, if the first block on the NAND flash is a bad block, the master chip can identify and skip it when booting from the NAND flash.

2.7 Others

2.7.1 Combining Write Operations

Data does not need to be saved for each operation. For example, data of channel switchover and volume adjustment can be saved later when operations are stopped for a period of time.

2.7.2 Saving Data That Does Not Require Power-off Protection to the Memory

Data that does not require power-off protection can be saved to the memory. For example, buffer data of online video streams can be stored to the memory.

3 Hynix Read Retry Usage

3.1 Obtaining Read Retry Levels

For many vendors, such as Micron, Toshiba, and Samsung, the read retry levels can be directly obtained in the NAND flash data sheets. However, for the latest Hynix NAND flash, the read retry levels are obtained differently.

Take H27UBG8T2CTR and H27UCG8T2ATR of Hynix as examples. The NAND flash contains a one-time programmable (OTP) table, which stores the read retry levels. The read retry levels vary according to NAND flash models. The OTP table cannot be frequently accessed to ensure reliability. Therefore, data in the OTP table must be read and saved to another reliable storage medium, the SPI Flash. This indicates that if the Hynix NAND flash is used, the system must boot from the SPI flash. For details about the mapping between the SPI flash and the OTP table of the NAND flash, see the HiSilicon component compatibility list.

3.2 Setting the Offset Address for OTP Data in the SPI Flash

You can specify the offset address for the OTP table in the SPI flash. The reference code is as follows (**fastboot3.0/include/configs/godbox.h**):

```
# define NAND_RR_PARAM_OFFSET   0x80000ULL //0x80000 is the address on the SPI flash for the OTP table.
After fastboot is started, if no data is in the address, fastboot automatically reads the OTP table from the NAND flash and stores it to the address. You must erase the address space in advance.
```

4 Solution and Component Selection

Despite its data reliability issues, the NAND flash is still favored in embedded systems by many electronic vendors because of its low cost, low power consumption, large capacity, and easy-to-use features. In this case, you must consider the solution and component selection to ensure data reliability of embedded systems.

Solution Selection

During memory solution selection, you must take factors such as costs, performance, application scenarios, and lifecycle into consideration.

If the required capacity is 256 Mbits or less, the SPI flash is recommended.

If the required capacity is greater than 256 Mbits but equal to or less than 4 Gbits, the SLC NAND flash is recommended. If the required capacity is 16 Gbits or more, SPI flash+MLC NAND flash or managed NAND flash is recommended (for details, see the A Appendix.)

Component Selection

The NAND flash with the data storage time of ten years is recommended.

When selecting the flash memory, you must consider the lifecycle of the product. For example, the required lifecycle is two to three years for smartphones, three to five years for STBs, and five to eight years for TV sets. The data storage time for the SLC NAND flash is ten years or more, but that for the MLC NAND flash is at most ten years, or even five or three years. In addition, the data storage time is even shortened under the influence of the ambient temperature and erase operations. For example, the liquid crystal display (LCD) of TV sets produces much heat, which increases the internal temperature to 50°C to 70°C (323ºK to 343.15ºK). Therefore, it is highly risky if key programs and data for TV sets are stored on the MLC NAND flash. Also, if the lifecycle of a NAND flash is 3000, you switch channels for 20 times a day, and the channel switchover data is stored on a fixed area, then the NAND flash can be used for 150 days (3000/20). The specified lifecycle of the NAND flash is 150 days. After 150 days, the repair rate increases.

A Appendix

A.1 Raw NAND and Managed NAND

The NAND flash memories can be classified into the raw NAND flash memory and managed NAND flash memory.

Raw NAND

The raw NAND flash consists of a flash memory array and a simple E/P/R controller that performs erase, program, and read operations. It has low cost. The raw NAND flash can be classified into the following two types:

- SLC NAND flash: Each storage unit stores one bit data.
- MLC NAND: Each storage unit stores two or more bit data.

Managed NAND

The managed NAND flash is the raw NAND flash plus a managing controller. The managing controller has many functions, such as bad block management, error correcting code (ECC) algorithm, and randomization. The managed NAND flash can be classified into the following types:

- Storage card
  - SD card
  - CF card
  - MMC
- Embedded managed NAND
  - Clear NAND
  - eMMC NAND
  - iNAND

The complexity of the managing controller causes extra cost, which is too much for small capacity NAND flash memories. Therefore, most managed NAND flash memories have large capacity, which is at least 2 GB. The managed NAND flash is 10% to 20% more expensive (no more than $2) than the raw NAND flash with the same capacity.

With functions such as the bad block management, ECC, and read and write leveling algorithm, the managed NAND flash is more reliable and endurable than the raw NAND flash.

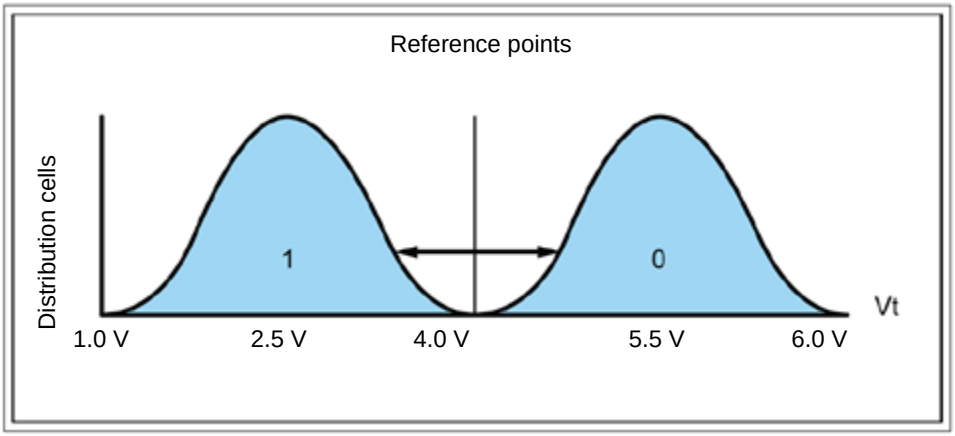
A.2 SLC NAND and MLC NAND

The NAND flash stores data by charging storage cells. The threshold voltage of a cell corresponds to the data stored in the cell. During the read operation, the data in a cell is obtained by comparing the threshold voltage and reference points.

SLC NAND

The SLC NAND flash has two level states and one reference point, as shown in Figure A-1.

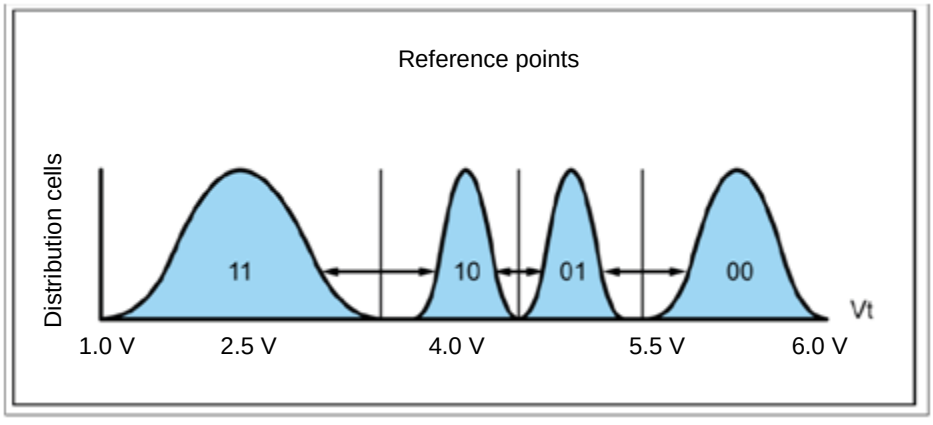
Figure A-1 SLC NAND flash threshold voltage and reference voltage



MLC NAND

The 2-bit MLC NAND flash has four level states and three reference points, as shown in Figure A-2.

Figure A-2 MLC NAND flash threshold voltage and reference voltage



TLC NAND

The 3-bit triple-level cell (TLC) NAND flash is more complex and less reliable.

Each cell of the MLC NAND flash can store more bits at sacrifice of the flash performance and reliability compared with the SLC NAND flash. As more level states and reference points are used, the error rate significantly increases. The threshold voltage of each storage cell of the NAND flash is subject to many factors which lead to changes during usage. Due to higher error rate, error occurrence of the MLC NAND flash is much more than that of the SLC NAND flash.

When the read data does not match the threshold voltage corresponding to the data during programming, bit inversion occurs, which is a threat to data reliability of the NAND flash. Bit inversion occurs more in the MLC NAND flash than the SLC NAND flash.