Hi3136

# Data Sheet

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|---|---|
| **Issue** | **00B10** |
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# About This Document

## Purpose

Hi3136 V100 is a satellite digital TV channel receiver chipset. This document describes the features, logic architecture, and hardware design of Hi3136 V100 for guiding user design.

## Related Version

The following table lists the product version related to this document.

| Product Name | Version |
|---|---|
| Hi3136 | V100 |

## Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronics

## Conventions

### Register Attributes

The register attributes that may be found in this document are defined as follows.

| Symbol | Description | Symbol | Description |
|---|---|---|---|
| RO | The register is read-only. | RW | The register is read/write. |

| Symbol | Description | Symbol | Description |
|---|---|---|---|
| RC | The register is cleared on a read. | WC | The register can be read.<br>The register is cleared when 1 is written.<br>The register keeps unchanged when 0 is written. |

## Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

## Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

| Type | Symbol | Value |
|---|---|---|
| Data capacity (such as the RAM capacity) | K | 1024 |
| | M | 1,048,576 |
| | G | 1,073,741,824 |
| Frequency, data rate | k | 1000 |
| | M | 1,000,000 |
| | G | 1,000,000,000 |

The expressions of addresses and data are described as follows.

| Symbol | Example | Description |
|---|---|---|
| 0x | 0xFE04, 0x18 | Address or data in hexadecimal |
| 0b | 0b000, 0b00 00000000 | Data or sequence in binary (register description is excluded.) |
| X | 00X, 1XX | In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111. |

# Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

## Issue 00B10 (2013-05-17)

This issue is the first official release, which incorporates the following changes:

**Chapter 3 Hardware**

The section 3.8.2 Output Timing Parameters is modified.

## Issue 00B01 (2012-12-06)

This issue is first draft release.

# Contents

# Figures

# 1 Product Description

## 1.1 Introduction to Hi3136 V100

Hi3136 V100 is a satellite digital TV channel receiver chipset that supports digital video broadcasting-satellite (DVB-S), DVB-S2, and DirecTV modes. The chipset uses all-digital processing technologies from baseband sampling on satellite digital signals to MPEG TS output. Hi3136 V100 supports quaternary phase shift keying (QPSK), 8 phase shift keying (8PSK), 16 absolute phase shift keying (16APSK), 32APSK, adaptive coding and modulation (ACM), and variable coding and modulation (VCM). These features make Hi3136 V100 the most comprehensive chipset in the industry. Hi3136 V100 supports a maximum of 60 Msps symbol rate and provides rapid and reliable blind scanning to search programs at full frequency bands and to obtain system information such as the carrier frequency, symbol rate, and code rate. Hi3136 V100 also supports phase noise suppression, anti-multipath, and anti-interference. Rapid channel synchronization enables Hi3136 V100 to reduce channel switching time. All these features enable Hi3136 V100 to work in various environments.

## 1.2 Key Specifications

### 1.2.1 Demodulation

Hi3136 V100 supports DVB-S2, DVB-S, and DirecTV (ITU-R BO.1516-System B) standards and automatic standard recognition. In the DVB-S2 standard, Hi3136 V100 provides the following demodulation functions:

- QPSK, 8PSK, 16APSK, and 32APSK
- 11 code rates
- Short and long frames
- CCM, VCM, and ACM modes
- TSs and generic streams (GSs), data services support

### 1.2.2 Features

Hi3136 V100 has the following features:

- Rapid and reliable blind scanning at full frequency bands to automatically obtain system information such as the carrier frequency, symbol rate, and code rate
- Superior phase noise suppression

- Superior anti-multipath for reducing reflections from high buildings and impedance mismatch
- Superior anti-interference for improving environment adaptation
- Rapid channel synchronization for reducing channel switching time
- Wide carrier and symbol rate acquisition ranges for improving applications
- Adaptive spectrum inversion recognition
- A maximum bit rate of 187.5 Mbit/s
- A minimum symbol rate of 1 Msps and the following maximum symbol rates:
  - 60 Msps in QPSK or 8PSK mode
  - 47 Msps in 16APSK mode
  - 37.5 Msps in 32APSK mode

### 1.2.3 System

Hi3136 V100 has the following system features:

- Integrated 125 MHz and 10-bit ADC with dual channels for supporting highly accurate sampling
- Integrated PLL, external passive crystal oscillator, 10−30 MHz (24 MHz typically)
- Real-time monitoring of the signal strength, signal-to-noise ratio, and bit error rate
- Simple external circuits, 2-layer PCB routing, low BOM costs

### 1.2.4 Interfaces

Hi3136 V100 has the following interface features:

- $I^2C$ bus protocol support for flexibly controlling chipsets
- Tuner $I^2C$ bus trunk
- Digital satellite equipment control (DiSEqC) V2.*x* and frequency shift keying (FSK) protocol support for controlling satellite equipment
- TS outputs in configurable serial or parallel mode to work with decoding chipsets
- Configurable TS output pin for facilitating PCB routing

### 1.2.5 Process

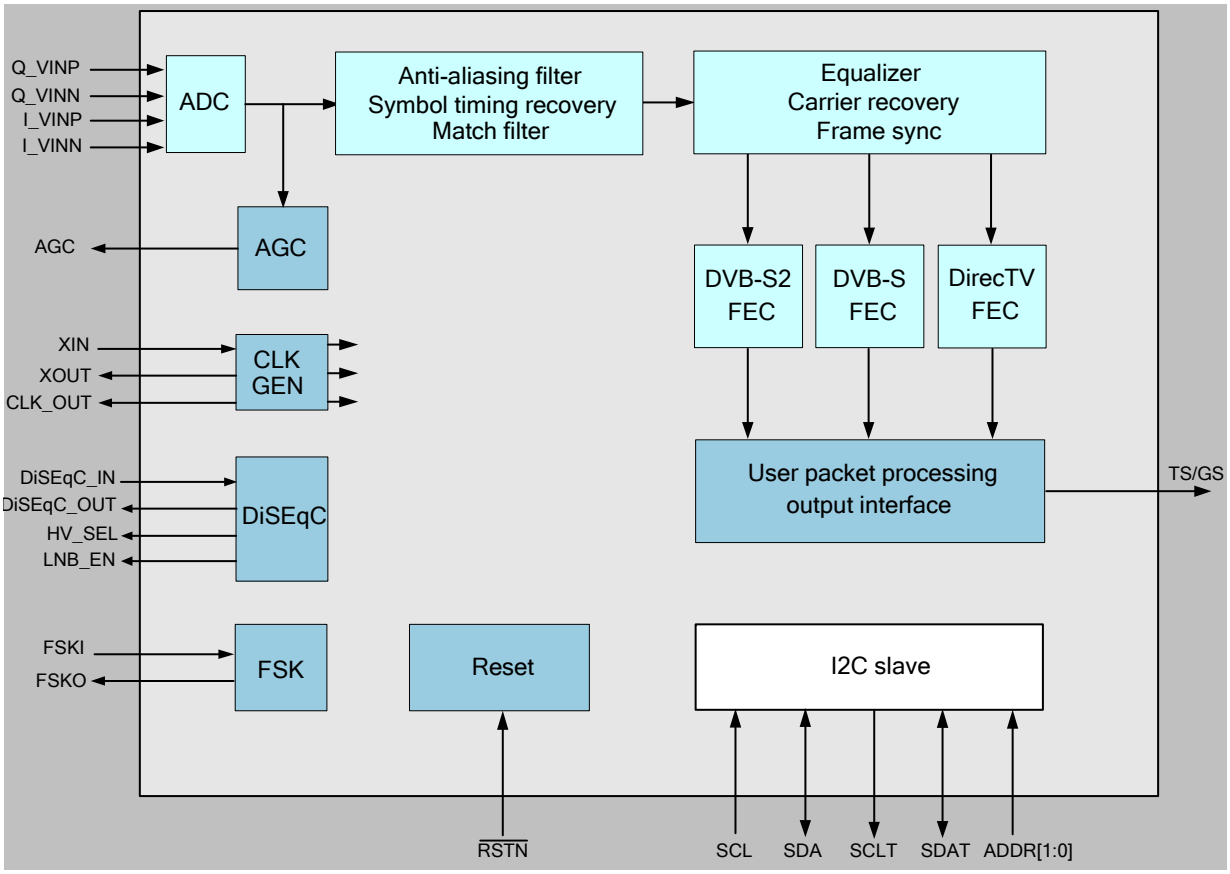
Hi3136 V100 uses the following power supplies and package:

- 1.2 V core power, 3.3 V I/O power, and the maximum power consumption of 540 mW
- Mapped quad flat non-leaded 48 (MQFN48), body size of 6 mm x 6 mm (0.24 in. x 0.24 in.), in compliance with the restriction of the use of certain hazardous substances (RoHS) directive

## 1.3 Functional Block Diagram

Figure 1-1 provides the functional block diagram.

**Figure 1-1** Functional block diagram




# 1.4 Application Fields

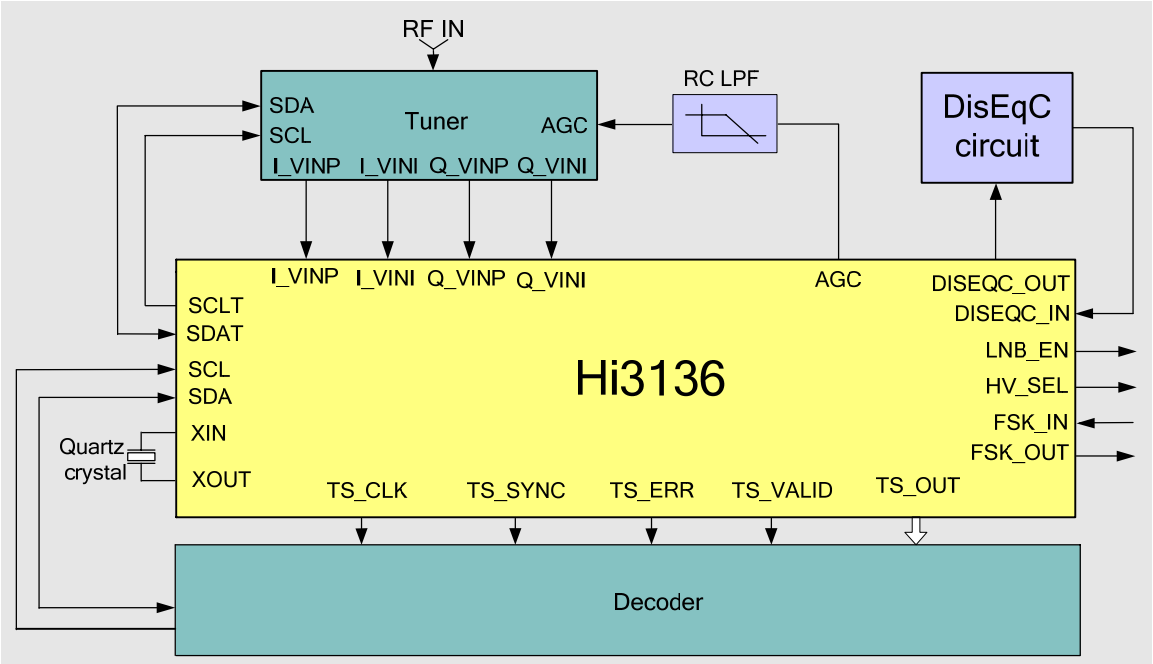
Hi3136 V100 applies to:

- Satellite tuner
- Satellite STB and integrated digital TV
- Satellite modem and digital TV card

# 1.5 Typical Application

Figure 1-2 demonstrates the typical front-end receiving application.

**Figure 1-2** Typical front-end receiving application



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# 2 Demod

## 2.1 Introduction

The Demod completes all-digital processing from baseband sampling on satellite digital TV signals, demodulation, and forward error correction (FEC) decoding to MPEG TS output. The Demod supports the DVB-S2 (ETS 302 307), DVB-S (ETS 300 421), and DirecTV (ITU-R BO.1294 System B) standards.

## 2.2 Clock

The Demod input clock is derived from an external crystal oscillator clock or external clock. After the internal PLLs process the input clock, the working clock frequency for the Demod is obtained. The Demod has two internal clock domains: CLK_DEMO and CLK_FEC. The CLK_DEMO clock domain is used for ADC and demodulation, and the CLK_FEC clock domain is used for FEC decoding and TS output. Figure 2-1 shows the internal clock domains of the Demod.

**Figure 2-1** Internal clock domains of the Demod

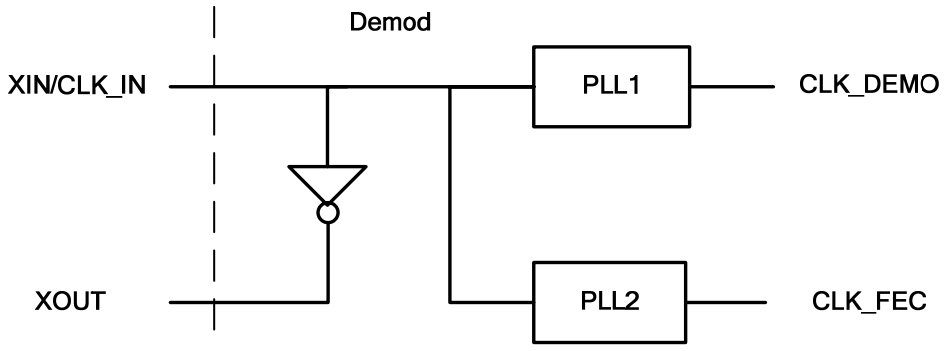



Table 2-1 describes the clock domains of other main modules.

**Table 2-1** Clock domains of other main modules

| Module | Clock Domain |
|---|---|
| $I^2C$ | After power-on, the $I^2C$ module works under a crystal oscillator clock or an external clock. After the internal PLLs are stable, the clock domain can be switched to CLK_DEMO to accelerate $I^2C$ communication. |
| DISEQC | CLK_DEMO (demodulation clock) |
| FSK | CLK_FEC (FEC decoding clock) |

Perform the following steps to set the CLK_DEMO frequency:

**Step 1** Set ADC_CTRL2[i2c_xo_clk] to 0 to switch the $I^2C$ clock to crystal oscillator clock or external clock. If Hi3136 V100 starts to work after power-on reset, the $I^2C$ module works under a crystal oscillator clock or an external clock by default.

**Step 2** Set PLL1_CTRL1[pll1_pd] to 1 to disable PLL1.

**Step 3** Set PLL1 parameters.

```
FVCO1 = FREF/pll1_refdiv[5:0] x (pll1_fbdiv[7:0] + pll1_frac[11:0]/2^12)
FOUT1 = FVCO1/pll1_postdiv1[2:0]/pll1_postdiv2[2:0]
```

where

- FREF is the frequency of a crystal oscillator clock or an external clock.
- FVCO1 is the PLL1 VCO frequency.
- FOUT1 is the CLK_DEMO output frequency.
- For details about other parameters, see the descriptions of PLL1 registers.

The working frequency of CLK_DEMO is 125 MHz when the typical 24 MHz crystal oscillator clock or external clock and default configurations are used.

**Step 4** Set PLL1_CTRL1[pll1_pd] to 0 to enable PLL1.

**Step 5** Wait until TS_CTRL2[pll1_lock] is 1, which indicating that PLL1 is locked.

**Step 6** Set PLL1_CTRL5[pll1_vcopd] to 0 to enable the PLL1 output.

**Step 7** Set ADC_CTRL2[i2c_xo_clk] to 0 to switch the $I^2C$ clock to CLK_DEMO.

**Step 8** Write 0 and then 1 to RSTN_CTRL[hot_rst_n] to perform a hot reset on Hi3136 V100.

**----End**

The procedure for setting the CLK_FEC frequency is similar. The only difference is to replace PLL1/pll1/FVCO1/FOUT1 with PLL2/pll2/FVCO2/FOUT2. For details, see PLL2 registers. The working frequency of CLK_FEC is 187.5 MHz when the typical 24 MHz crystal oscillator clock or external clock and default configurations are used.

**NOTE**

You can set the CLK_DEMO and CLK_FEC frequencies after switching the $I^2C$ clock to the crystal oscillator clock or external clock. The frequencies of PLLx input and output clocks and internal clocks must fall within the value ranges described in Table 2-2. The value of *x* in PLLx or FVOCx is 1 or 2.

**Table 2-2** Frequency ranges of PLL input and output clocks and internal clocks

| Clock | Frequency Range (MHz) |
|---|---|
| FREF | 10−30 |
| FREF/pllx_refdiv | 10−40 |
| FVCOx | ≤ 1600 |
| CLK_DEMO (FOUT1) | ≤ 125 |
| CLK_FEC (FOUT2) | ≤ 187.5 |

The maximum symbol rate supported by the Demod is CLK_DEMO/2 to ensure that the demodulation function is normal. Table 2-3 describes the relationship between the maximum symbol rate and the CLK_FEC frequency. The FEC decoding function is normal only when the maximum symbol rate is not exceeded.

**Table 2-3** Maximum symbol rates in various demodulation modes

| Modulation Mode | Maximum Symbol Rate |
|---|---|
| QPSK | CLK_FEC/2 |
| 8PSK | CLK_FEC/3 |
| 16APSK | CLK_FEC/4 |
| 32APSK | CLK_FEC/5 |

After power-on reset, PLL1 and PLL2 outputs are disabled. Set PLL1_CTRL5[pll1_vcopd] and PLL2_CTRL5[pll2_vcopd] to 0 to enable clock outputs.

To ensure that Hi3136 V100 works properly, do as follows after changing PLL frequencies:

- Set CLK_DEMO_L[clk_demo_l], CLK_DEMO_M[clk_demo_m], and CLK_DEMO_H[clk_demo_h] based on the current CLK_DEMO frequency. The CLK_DEMO frequency unit is kHz and the CLK_DEMO frequency is calculated as follows:

  CLK_DEMO frequency = clk_demo_h x 65536 + clk_demo_m x 256 + clk_demo_l
- Set CLK_FEC_L[clk_fec_l], CLK_FEC_M[clk_fec_m], and CLK_FEC_H[clk_fec_h] based on the current CLK_FEC frequency. The CLK_FEC frequency unit is kHz and the CLK_FEC frequency is calculated as follows:

  CLK_FEC frequency = clk_fec_h x 65536 + clk_fec_m x 256 + clk_fec_l

The Demod provides the loopback clock CLK_OUT (PIN_24) for other chips such as the MPEG decoding chip. The CLK_OUT frequency is equal to the frequency of the crystal oscillator clock or external clock.

# 2.3 Reset

Reset operations are classified into hard reset and soft reset.

- The external RSTN pin is used for power-on reset or used by the main control chip for resetting the Demod. When a hard reset is performed, all registers are reset.
- By using the $I^2C$ module, internal registers can be reset by a cold reset (cool_rst_n) or hot reset (hot_rst_n) as follows:
  - Cold reset: Write 0 and then 1 to RSTN_CTRL[cool_rst_n]. When a cold reset is performed, all registers are reset, which is the same as a hard reset.
  - Hot reset: Write 0 and then 1 to RSTN_CTRL[hot_rst_n]. When a hot reset is performed, only the logic is reset and register values are retained.

# 2.4 I²C Controller

The $I^2C$ controller on the Demod acts as an $I^2C$ slave. The $I^2C$ controller reads or writes to the internal configuration register of the Demod over $I^2C$ communication and forwards $I^2C$ communication for the tuner.

When the $I^2C$ controller acts as the slave, it supports all $I^2C$ operations initiated by the main control chip. The Demod component address is expressed by 10110XXY. XX is specified by setting ADDR bit[1:0] and Y is used to specify the operation type. The value 1 indicates read and the value 0 indicates write. Figure 2-2 shows the $I^2C$ read timing, and Figure 2-3 shows the $I^2C$ write timing.

**Figure 2-2** $I^2C$ read timing

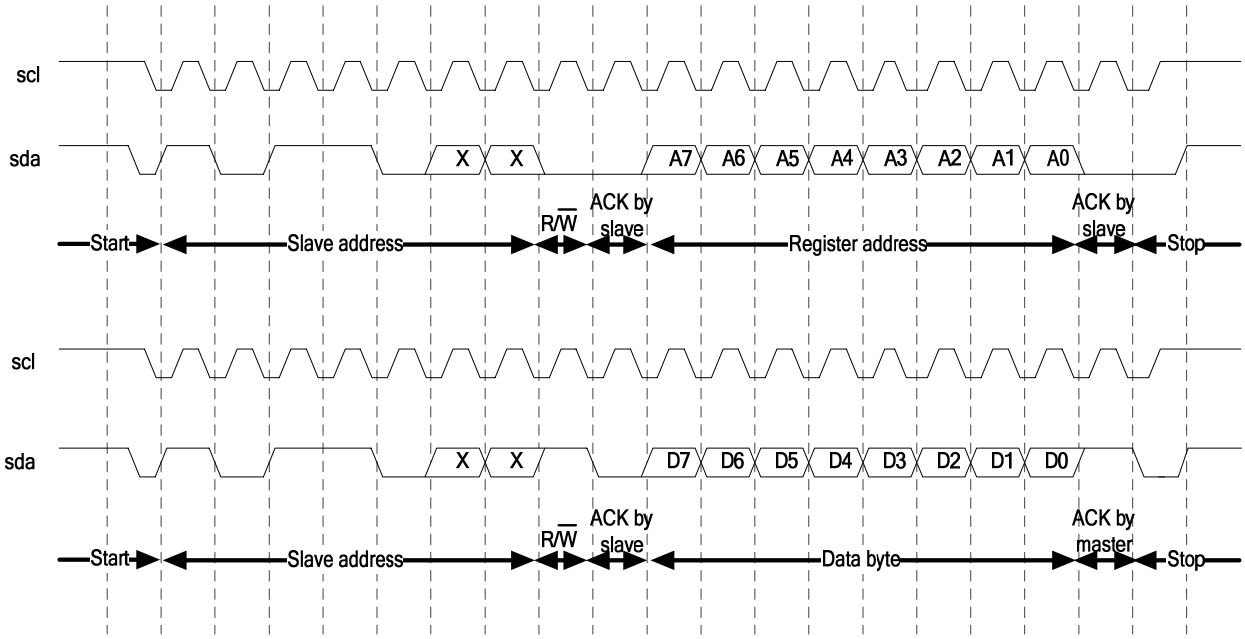
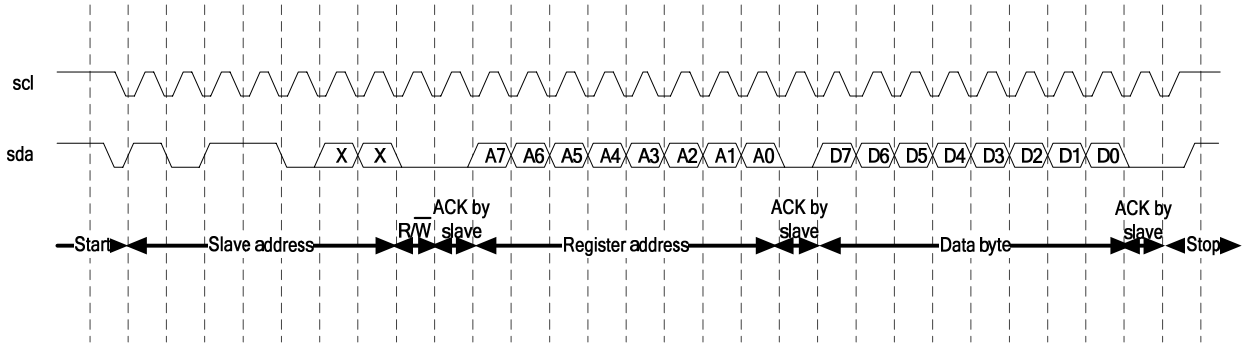


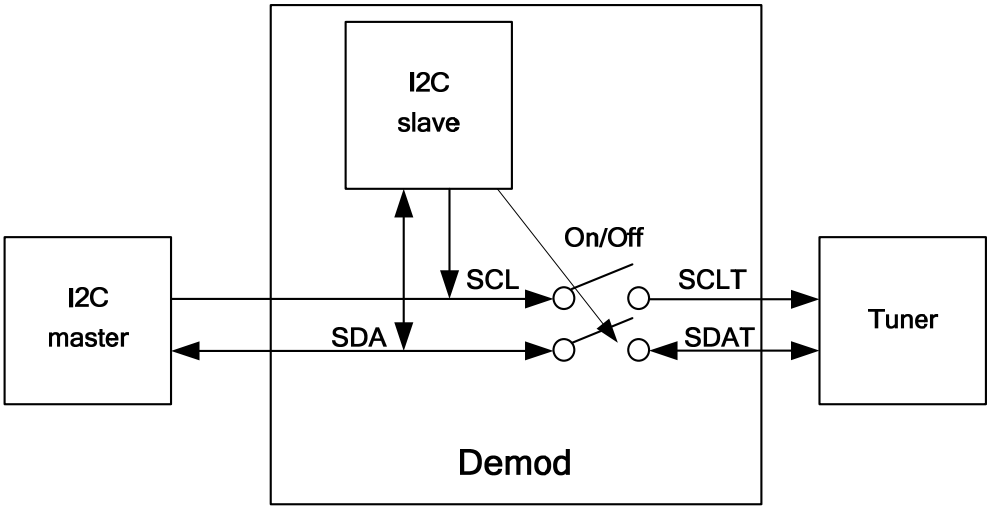
**Figure 2-3** I²C write timing




The I²C controller consecutively reads or writes to multiple registers by working with software. For the tuner, the Demod can forward I²C communication. That is, the main control chip can access the tuner in the same way that the main control chip accesses the Demod when the I²C path between the main control chip and the tuner is enabled. Each time after an I²C read or write operation is complete, the Demod automatically disables forwarding to prevent interference to the tuner from the I²C module. For details about I²C addresses for the tuner, see tuner user manuals.

Figure 2-4 shows the I²C forwarding schematic diagram.

**Figure 2-4** I²C forwarding schematic diagram




For details about how to enable I²C forwarding, see the descriptions of the TUNER_SEL register.

# 2.5 ADC

The Demod integrates a 10-bit ADC with dual channels. The ADC samples the baseband analog in-phase (I)/quadrant (Q) signals output from the front-end tuner. The CLK_DEMO frequency is set by changing the actual sampling clock frequency. The maximum CLK_DEMO frequency is 125 MHz. The ADC supports differential or single-ended inputs.

The default input mode is differential input. The peak voltage at full scale is 1 V. The sampling clock edge is selected by configuring ADC_CTRL2[adc_clk_inv].

Typically, the ADC I/Q traces and tuner I/Q traces are connected respectively. In some cases, the ADC I/Q traces and tuner Q/I traces are connected respectively to facilitate PCB routing, which can also be automatically identified by the Demod.

After powering on the Demod, write 3 and then 0 to ADC_CTRL1[adc_om] to initialize the Demod.

# 2.6 AGC

The automatic gain control (AGC) module receives I/O outputs from the ADC and generates an AGC control signal (PDM wave) based on the difference between the expected and the actual power consumption. After resistor-capacitor (RC) filtering externally, the AGC control signal is transmitted to the tuner to adjust the tuner output amplitude to the expected value.

Set the following items:

- Set the clock frequency of the AGC control signal by configuring AGC_CTRL[pdm_div].
- Set the output polarity by configuring AGC_CTRL[agc_inverse].
- Set the expected AGC power consumption by configuring AGC_GOAL[agc_goal].
- Set the AGC adjustment speed by configuring AGC_SPEED_BOUND[agc_speed].

Table 2-4 describes AGC signal clock frequencies.

**Table 2-4** AGC signal clock frequencies

| pdm_div[2:0] | AGC Signal Clock Frequency |
|---|---|
| 0 | CLK_DEMO |
| 1 | CLK_DEMO/2 |
| 2 | CLK_DEMO/4 |
| 3 | CLK_DEMO/8 |
| 4 | CLK_DEMO/16 |
| 5 | CLK_DEMO/32 |
| 6 | CLK_DEMO/64 |
| 7 | CLK_DEMO/128 |

# 2.7 AAF

The anti-aliasing filter (AAF) suppresses out-of-band interference based on the configured symbol rate, preventing interference to valid signals.

# 2.8 TR

The timing recovery (TR) module recovers a clock with the same symbol rate as that at the TX end and sampling data with accurate clock phase.

The Demod uses the $I^2C$ module to write the initial symbol rate fs, ensuring that the TR module works properly. fs is a 16-bit unsigned number. The LSB indicates 1 kHz, and the maximum fs value is about 65 MHz. For details, see the descriptions of the FS_H and FS_L registers.

When channel blind scanning is enabled, the initial symbol rate can be provided by the blind scanning module. For details, see section 2.17 "Channel Blind Scanning."

# 2.9 MF

The matched filter (MF) is a root raised cosine filter. Its roll-off factor is 0.2, 0.25, or 0.35, which can be automatically identified.

# 2.10 EQU

The equalizer (EQU) eliminates the influences caused by echoes and linear channel distortion by using the blind equalization algorithm and decree feedback equalization algorithm. Set the blind equalization step by configuring EQU_CTRL[blind_step]. Set the decree feedback equalization step by configuring LMS_STEP[lms_step_4_8] or RD_WR_TAP[lms_step_16_32]. LMS_STEP[lms_step_4_8] corresponds to the QPSK or 8PSK mode, and RD_WR_TAP[lms_step_16_32] corresponds to the 16APSK or 32APSK mode.

# 2.11 CR

The carrier recovery (CR) module traces and compensates the frequency offset and phase offset of the carrier. By using an innovative algorithm, Hi3136 V100 optimizes the phase noise suppression, synchronization speed, and carrier and symbol rate acquisition range.

In some cases (for example, when the symbol rate is low), demodulation performance is improved by offsetting the tuner center frequency. The offset must be compensated in Hi3136 V100. Set the offset by configuring CENT_FREQ_L[cent_freq_l] and CENT_FREQ_H[cent_freq_h]. The value of cent_freq[15:0] is the difference between the actual center frequency and the configured center frequency of tuner input signals. The value is a signed number. The LSB indicates 1 kHz, and the value range is −32 MHz to +32 MHz.

# 2.12 Frame Synchronization

Because DVB-S2 signals are organized by frame, the frame start position must be accurate. The frame synchronization function is used to locate the frame start position. Rapid synchronization is supported at an extremely low signal-to-noise ratio (SNR). In addition, reliable synchronization is supported when the frame length changes by frame in VCM or ACM mode.

# 2.13 DVB-S2 FEC Module

This module performs the following operations:

**Step 1** Demap symbols and transmit the generated software information to the deinterleaver.

**Step 2** After deinterleaving, store the information in the random access memory (RAM) for low-density parity check code (LDPC) decoding. The short frame mode, long frame modes, and all standard code rates are supported during LDPC decoding.

**Step 3** Transmit the decoded data to the Bose-Chaudhuri-Hocquenghem (BCH) module for BCH decoding.

**----End**

# 2.14 DVB-S&DirecTV FEC Module

This module performs the following operations:

**Step 1** Identify and synchronize Viterbi code rates.

**Step 2** Perform depuncturing and demapping.

**Step 3** Perform Viterbi decoding. The supported code rates include 1/2, 2/3, 3/4, 5/6, 7/8, and 6/7.

**Step 4** Perform DVB-S/DirecTV deinterleaving.

**Step 5** Transmit deinterleaved data to the Reed-Solomon (RS) decoder for channel correction. The DVB-S output packet length is 188 bytes, and the DirecTV output packet length is 130 bytes.

**----End**

# 2.15 TS Output

The Demod supports three TS output modes: parallel mode, 1-bit serial mode, and 2-bit serial mode.

The signals from the TS output interface include the data signal TS_OUT[7:0], clock signal TS_CLK, data validity signal TS_VLD, sync header signal TS_SYNC, and packet error signal TS_ERR.

- TS_OUT: TS frame data. This signal is 8 bits in parallel mode, 1 bit in 1-bit serial mode, and 2 bits in 2-bit serial mode.
- TS_CLK: data clock. The clock edge is configurable. The clock output varies according to the output mode.
- TS_VLD: TS packet data validity indicator. It is byte valid in parallel mode or bit valid in 1-bit serial mode.
- TS_SYNC: TS packet sync header indicator. It is byte valid in parallel mode or bit valid in 1-bit serial mode.
- TS_ERR: TS packet error indicator. Set it to 1 if an error occurs in the current TS packet.

Select the TS output mode by configuring TS_PARALL_CTRL[ts_parall] and TS_PARALL_CTRL[ts_serial2]. See Table 2-5.

**Table 2-5** TS output modes

| ts_parall | ts_serial2 | TS Output Mode | Maximum TS_CLK Frequency (MHz) | Maximum TS Bit Rate (Mbit/s) |
|---|---|---|---|---|
| 1 | 0 | Parallel mode | 23.5 | 187.5 |
| 1 | 1 | 2-bit serial mode | 94 | 187.5 |
| 0 | x | 1-bit serial mode | 187.5 | 187.5 |

Figure 2-5 shows the timing in TS parallel output mode.

**Figure 2-5** Timing in TS parallel output mode

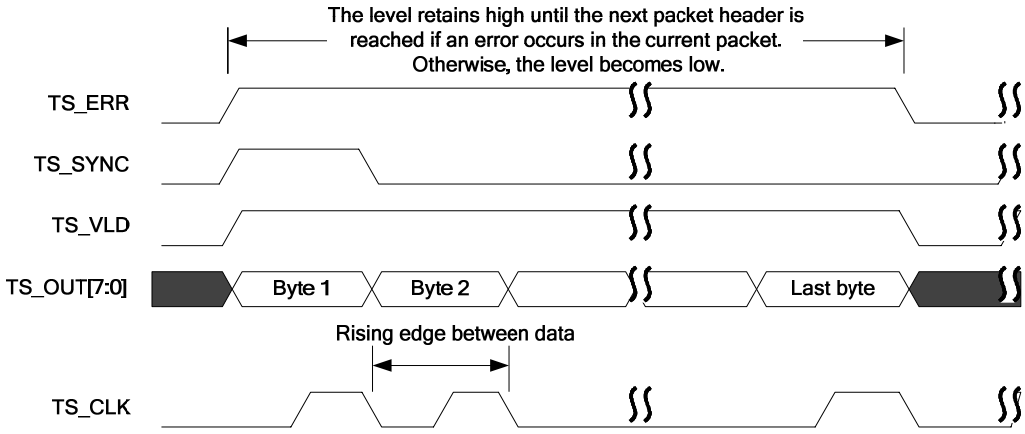
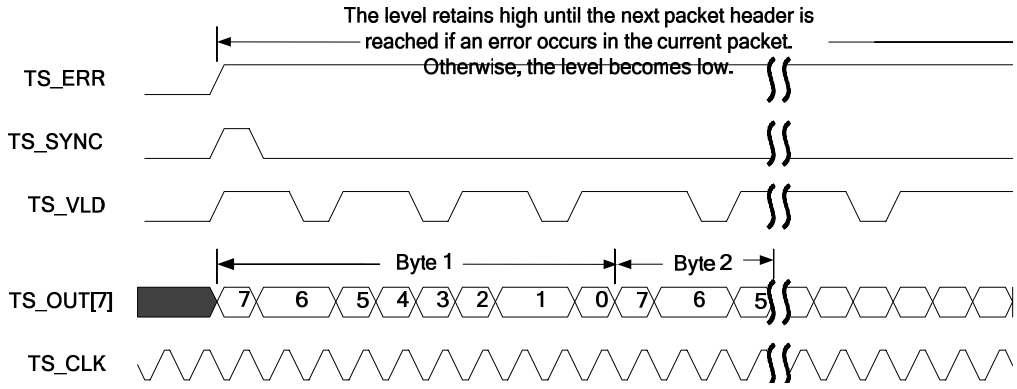



Figure 2-6 shows the timing in 1-bit TS serial output mode.

**Figure 2-6** Timing in 1-bit TS serial output mode

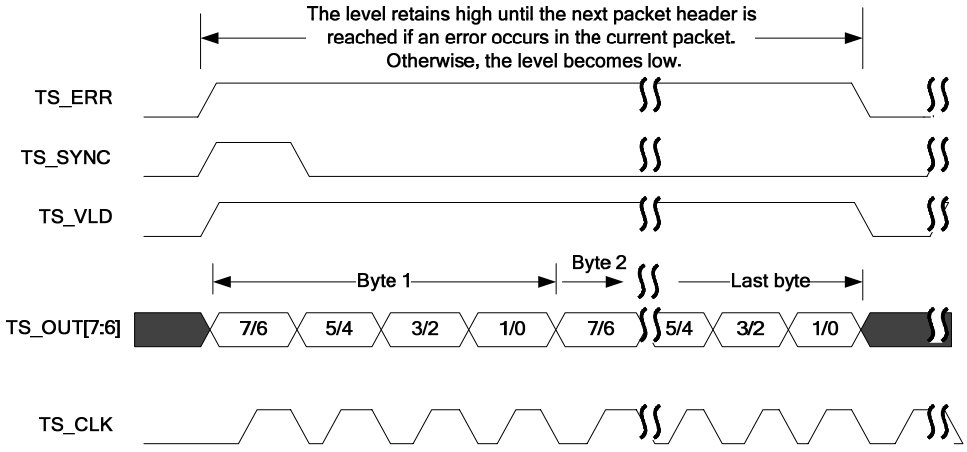


**NOTE**

In 1-bit serial output mode, the TS_CLK frequency is fixed at the CLK_FEC frequency. Invalid bits are masked by setting the TS_VLD level to low. In Figure 2-6, upper bits are output first. You can enable lower bits to output first by configuring TS_CTRL0[ts_lsb_first]. TS_OUT can be mapped to any pin in TS_OUT[7:0]. For details, see the following sections.

Figure 2-7 shows the timing in 2-bit TS serial output mode.

**Figure 2-7** Timing in 2-bit TS serial output mode




**NOTE**

In 2-bit serial output mode, TS_OUT can be mapped to any two pins in TS_OUT[7:0].

In parallel output mode or 2-bit serial output mode, select the TS_CLK clock edge by configuring TS_CTRL0[ts_clk_inv]. If TS_CTRL0[ts_clk_inv] is 0, the rising edge is between TS data. If TS_CTRL0[ts_clk_inv] is 1, the falling edge is between data.

In 1-bit serial output mode, select the TS_CLK clock edge by configuring ADC_CTRL2[clk_inv]. If ADC_CTRL2[clk_inv] is 0, the rising edge is selected. If ADC_CTRL2[clk_inv] is 1, the falling edge is selected.

In parallel mode or 2-bit serial mode, the Demod automatically generates an even TS_CLK signal based on the CLK_FEC frequency, transmission standard, symbol rate, and modulation mode. You can also specify a fixed frequency-division signal of CLK_FEC as the TS_CLK signal. This method is recommended, because TS outputs including VCM and multi-TS are supported in most cases. Perform the following steps:

**Step 1** Set TS_CTRL4[ts_clk_div], TS_CLK_DIV_F_L[ts_clk_div_f_l], and TS_CLK_DIV_F_H[ts_clk_div_f_h] to determine the frequency divider for the system clock. ts_clk_div[5:0] is the integral part of the frequency divider and ranges from 8 to 63. ts_clk_div_f[15:0] is the decimal part of the frequency divider. The actual frequency divider is calculated as follows: Frequency divider = ts_clk_div[5:0] + ts_clk_div_f[15:0]/65536

**Step 2** Set TS_CTRL4[clk_auto] to 0 to switch TS_CLK to the configured frequency.

**Step 3** Determine whether to mask the TS_CLK output by configuring TS_CTRL0[mask_ts_clk] when TS_VLD is low.

**CAUTION**

Ensure that the maximum TS rate is supported at the TS_CLK frequency.

In 1-bit serial output mode, the TS_CLK output frequency is fixed at the CLK_FEC frequency. Mask invalid bits by setting TS_VLD to low.

The TS pin outputs are selected by using control signals. In Table 2-6, the value of *x* in ts_x_sel is a or 0−9.

**Table 2-6** Mapping between the control signal ts_x_sel and the controlled external pin

| Control Signal | Register | Controlled External Pin |
|---|---|---|
| ts_0_ sel | TS_10_SEL | TS_OUT0 |
| ts_1_ sel | TS_10_SEL | TS_OUT1 |
| ts_2_ sel | TS_32_SEL | TS_OUT2 |
| ts_3_sel | TS_32_SEL | TS_OUT3 |
| ts_4_ sel | TS_54_SEL | TS_OUT4 |
| ts_5_ sel | TS_54_SEL | TS_OUT5 |
| ts_ 6_sel | TS_76_SEL | TS_OUT6 |
| ts_7_ sel | TS_76_SEL | TS_OUT7 |
| ts_8_ sel | TS_98_SEL | TS_SYNC |
| ts_9_ sel | TS_98_SEL | TS_VLD |
| ts_ a_sel | TS_PARALL_CTRL | TS_ERR |

Table 2-7 describes the mapping between the ts_x_sel value and the internal TS signal. The value of *x* in ts_x_sel is a or 0−9.

**Table 2-7** Mapping between the ts_x_sel value and the internal TS signal

| ts_x_sel Value | Internal TS Signal |
|---|---|
| 0000 | ts_out[0] |
| 0001 | ts_out[1] |
| 0010 | ts_out[2] |
| 0011 | ts_out[3] |
| 0100 | ts_out[4] |

| ts_x_sel Value | Internal TS Signal |
|---|---|
| 0101 | ts_out[5] |
| 0110 | ts_out[6] |
| 0111 | ts_out[7] |
| 1000 | ts_sync |
| 1001 | ts_vld |
| Others | ts_err |

**NOTE**

- In 1-bit serial output mode, if the upper bit output takes priority, select the internal TS data signal ts_out[7]. If the lower bit output takes priority, select the internal TS data signal ts_out[0].
- In 2-bit serial output mode, if the upper bit output takes priority, select the internal TS data signal ts_out[7:6]. If the lower bit output takes priority, select the internal TS data signal ts_out[1:0].

**----End**

# 2.16 Signal Monitoring

## Signal Strength

The Demod supports signal power statistics. Read AGC_CTRL_L[agc_ctrl_l] and then AGC_CTRL_H[agc_ctrl_h] to obtain the signal strength identifier.

```
sig_strength = agc_ctrl_h x 256 + agc_ctrl_l
```

A larger sig_strength value indicates weaker signal strength.

## Transmission Standard and Spectrum Inversion Recognition

To read the transmission standard, perform the following steps:

**Step 1** Wait until LOCK_FLAG[fec_ok] is 1. The read information is correct only when LOCK_FLAG[fec_ok] is 1.

**Step 2** Read LOCK_FLAG[sync_ok]. If LOCK_FLAG[sync_ok] is 1, the mode is DVB-S2. If LOCK_FLAG[sync_ok] is 0, the mode is DVB-S/DirecTV.

- DVB-S2 mode

  Read PLS_CODE bit[6:0]. PLS_CODE bit[6:2] indicate the modulation mode and code rate. PLS_CODE bit[1] indicates the frame length. If PLS_CODE bit[1] is 0, the frame is a normal frame (the frame length is 64800 bits). If PLS_CODE bit[1] is 1, the frame is a short frame (the frame length is 16200 bits). PLS_CODE bit[0] indicates whether there is pilot. If PLS_CODE bit[0] is 0, there is no pilot. If PLS_CODE bit[0] is 1, there is a pilot. Table 2-8 describes the mapping between PLS_CODE bit[6:2] and the modulation modes and code rates.

**Table 2-8** Mapping between PLS_CODE bit[6:2] and the modulation modes and code rates

| PLS_CODE Bit[6:2] | Modulation Mode and Code Rate | PLS_CODE Bit[6:2] | Modulation Mode and Code Rate |
|---|---|---|---|
| 00000 | Dummy (QPSK) | 10000 | 8PSK 8/9 |
| 00001 | QPSK 1/4 | 10001 | 8PSK 9/10 |
| 00010 | QPSK 1/3 | 10010 | 16APSK 2/3 |
| 00011 | QPSK 2/5 | 10011 | 16APSK 3/4 |
| 00100 | QPSK 1/2 | 10100 | 16APSK 4/5 |
| 00101 | QPSK 3/5 | 10101 | 16APSK 5/6 |
| 00110 | QPSK 2/3 | 10110 | 16APSK 8/9 |
| 00111 | QPSK 3/4 | 10111 | 16APSK 9/10 |
| 01000 | QPSK 4/5 | 11000 | 32APSK 3/4 |
| 01001 | QPSK 5/6 | 11001 | 32APSK 4/5 |
| 01010 | QPSK 8/9 | 11010 | 32APSK 5/6 |
| 01011 | QPSK 9/10 | 11011 | 32APSK 8/9 |
| 01100 | 8PSK 3/5 | 11100 | 32APSK 9/10 |
| 01101 | 8PSK 2/3 | 11101 | Reserved |
| 01110 | 8PSK 3/4 | 11110 | Reserved |
| 01111 | 8PSK 5/6 | 11111 | Reserved |

Read TS_CTRL3[is_ccm] in DVB-S2 mode. If TS_CTRL3[is_ccm] is 0, the current transmission mode is VCM or ACM. If TS_CTRL3[is_ccm] is 1, the current transmission mode is CCM.

Read ROLL_OFF[roll_off] to obtain the roll-off factors in DVB-S2 mode. Table 2-9 describes the mapping between the values of ROLL_OFF bit[1:0] and roll-off factors.

**Table 2-9** Mapping between the values of ROLL_OFF bit[1:0] and roll-off factors

| ROLL_OFF Bit[1:0] | Roll-Off Factor |
|---|---|
| 00 | 0.35 |
| 01 | 0.25 |
| 10 | 0.2 |
| 11 | Reserved |

Read FREQ_INV[freq_inverse] in DVB-S2 mode. If FREQ_INV[freq_inverse] is 1, the spectrum is inverted. If FREQ_INV[freq_inverse] is 0, the spectrum is not inverted.

- DVB-S/DirecTV

  Read SEAR_RESULT bit[0]. If SEAR_RESULT bit[0] is 1, the mode is DirecTV. If SEAR_RESULT bit[0] is 0, the mode is DVB-S. Read SEAR_RESULT bit[3:1] to obtain the code rates in DVB-S and DirecTV modes.

**Table 2-10** Code rates in DVB-S and DirecTV modes

| SEAR_RESULT Bit[3:1] | Code Rate in DVB-S Mode | Code Rate in DirecTV Mode |
|---|---|---|
| 000 | 1/2 | 1/2 |
| 001 | 2/3 | 2/3 |
| 010 | 3/4 | N/A |
| 011 | 5/6 | N/A |
| 100 | 7/8 | N/A |
| 101 | N/A | 6/7 |
| 110 | N/A | N/A |
| 111 | N/A | N/A |

Note the following:

- The modulation mode for DVB-S/DirecTV is fixed at QPSK.
- The roll-off factor is fixed at 0.35 for DVB-S or 0.2 for DirecTV.
- Read DEC_RESULT[iq_swap] in DVB-S/DirecTV mode.
  - 1: The spectrum is inverted.
  - 0: The spectrum is not inverted.

**----End**

## Symbol Rate Offset

The initial symbol rate fs must be loaded before timing recovery. After the timing loop is stable, read [fs_offset_fc_l] and then FS_OFFSET_FC_H[fs_offset_fc_h] from the Demod. Calculate the offset between the actual symbol rate and fs as follows:

```
fs_offset_tmp = (fs_offset_fc_h*256+fs_offset_fc_l)
if(fs_offset_tmp>=32768)
fs_offset = (fs_offset_tmp-65536)/2^22*CLK_DEMO
else
fs_offset  = fs_offset_tmp/2^22*CLK_DEMO
```

If the value of fs_offset is a positive number, the actual symbol rate is greater than the configured symbol rate. If the value of fs_offset is a negative number, the actual symbol rate is less than the configured symbol rate. The units of CLK_DEMO and fs_offset are kHz.

Note that the symbol rate offset is valid only when the offset is read after LOCK_FLAG[fec_ok] is 1.

## Carrier Offset

After the carrier loop is stable, read [freq_offset_fc_l] and then FREQ_OFFSET_FC_H[freq_offset_fc_h] from the Demod. Calculate the offset between the actual signal center frequency and the tuner center frequency as follows:

```
freq_offset_tmp=(freq_offset_fc_h*256+freq_offset_fc_l)
if(freq_offset_tmp>=32768)
freq_offset = (freq_offset_tmp – 65536)/2^17*CLK_DEMO
else
freq_offset = freq_offset_tmp/2^17*CLK_DEMO
```

If the value of freq_offset is a positive number, the actual center frequency is greater than the tuner center frequency. If the value of freq_offset is a negative number, the actual center frequency is less than the tuner center frequency. The units of CLK_DEMO and freq_offset are kHz.

Note that the carrier offset is valid only when the offset is read after LOCK_FLAG[fec_ok] is 1.

## Signal Quality

The Demod provides the noise power statistics registers NOISE_POW_H[noise_pow_h] and NOISE_POW_L[noise_pow_l]. Read the register values and convert the values into the SNR as follows (The SNR is used to evaluate the signal quality and its unit is dB):

SNR = 10.0 x log10(8192.0/(noise_pow_h [6:0] x 256 + noise_pow_l))

**CAUTION**

Read NOISE_POW_H and then NOISE_POW_L. Read NOISE_POW_H[cnr_est_ok] to obtain the signal quality indicator. The estimated SNR is reliable only when NOISE_POW_H[cnr_est_ok] is 1.

## BER Statistics

Calculate the bit error rate (BER) before RS (for DVB-S/DirecTV) or BCH (for DVB-S2) correction by using the Demod error bit count registers FEC_BER_H and FEC_BER_L.

Read FEC_BER_L and then FEC_BER_H, and calculate the error bit count error_cnt as follows:

error_cnt = FEC_BER_H x 256 + FEC_BER_L

If the BER is high, the actual error bit count may be greater than the maximum value of the error bit count registers. The registers will retain the maximum value, which results in a BER that is less than the actual value.

In DVB-S/DirecTV mode, calculate the BER before RS decoding as follows:

$$BER = \frac{error\_cnt}{8 \times N \times frams}$$

where

- *error_cnt* is the error bit count.
- *N* is 204 in DVB-S mode or 146 in DirecTV mode.
- *frams* is the total frame count, which is set by configuring BER_CTRL bit[6:4]. For details, see Table 2-12.

In DVB-S2 mode, calculate the BER before BCH decoding as follows:

$$BER = \frac{error\_cnt}{N \times frams}$$

where

- *error_cnt* is the error bit count.
- *N* is the BCH code length. The BCH code length varies according to the frame length mode and code rate. For details, see Table 2-11.
- *frams* is the total frame count, which is set by configuring BER_CTRL bit[6:4]. For details, see Table 2-12.

**Table 2-11** Values of *N* in DVB-S2 mode

| LDPC Code Rate | N Value for a Normal Frame | N Value for a Short Frame |
|---|---|---|
| 1/4 | 16200 | 3240 |
| 1/3 | 21600 | 5400 |
| 2/5 | 25920 | 6480 |
| 1/2 | 32400 | 7200 |
| 3/5 | 38880 | 9720 |
| 2/3 | 43200 | 10800 |
| 3/4 | 48600 | 11880 |
| 4/5 | 51840 | 12600 |
| 5/6 | 54000 | 13320 |
| 8/9 | 57600 | 14400 |
| 9/10 | 58320 | N/A |

**Table 2-12** Mapping between the values of BER_CTRL bit[6:4] and frams

| BER_CTRL bit [6:4] | frams Value in DVB-S/DirecTV Mode | frams Value in DVB-S2 Mode |
|---|---|---|
| b'000 | d'16 | d'4 |
| b'001 | d'64 | d'16 |
| b'010 | d'256 | d'128 |
| b'011 | d'1024 | d'256 |
| b'100 | d'4096 | d'2048 |
| b'101 | d'16384 | d'4096 |
| b'110 | d'65536 | d'32768 |
| b'111 | d'262144 | d'65535 |

- In DVB-S/DirecTV mode, calculate the BER after RS decoding as follows: BER = 32 x FER

  For details about the frame error rate (FER), see section "FER Statistics." The BER after RS decoding is an approximate value.
- In DVB-S mode, calculate the BER after BCH decoding as follows: BER = 27 x FER

  For details about the FER, see section "FER Statistics." The BER after BCH decoding is an approximate value.

**NOTE**

The BER statistics enable register is FS_CTRL2 bit[1]. It is active high and is high by default.

## FER Statistics

The frame is an RS frame for DVB-S/DirecTV signals or a BCH frame for DVB-S2 signals. The statistics enable register FS_CTRL2 bit[1] controls both FER statistics and BER statistics.

Read FEC_FER_L and then FEC_FER_H, and calculate the error frame count error_fram as follows:

error_fram = FEC_FER_H x 256 + FEC_FER_L

Calculate the FER as follows:

FER = error_fram/frams

where

- *error_fram* is the error frame count.
- *frams* is the total frame count in DVB-S, DirecTV, and DVB-S2 modes, which is set by configuring BER_CTRL bit[6:4]. For details, see section "BER Statistics."

### PER Statistics

In DVB-S2 mode, a BCH frame contains several TS and generic stream (GS) packets that can be used to calculate the packet error rate (PER). To calculate the PER, perform the following steps:

**Step 1** For multi-TS transmission, set TS_CTRL4[isi_sel_vld] to 1 and ISI_SEL[isi_sel] to the stream ID to select streams. For single-TS transmission, skip this step.

**Step 2** Set RST_WAIT[crc_pkt_cnt] to specify the total packet count for PER statistics.

Calculate the total packet count as follows:

Total packet count = crc_pkt_cnt x 1024

If crc_pkt_cnt is 0, the total packet count is 1024.

**Step 3** Read CRC_ERR[crc_err] and calculate the PER as follows: PER = crc_err/1024

**CAUTION**

- If consecutive streams are selected, PER statistics is invalid.
- If the PER is not 0 but less than 1/1024, the value 1/1024 is used.
- If the PER is greater than 255/1024, the value 255/1024 is used.

## 2.17 Channel Blind Scanning

Channel blind scanning enables you to obtain the accurate channel center frequency and symbol rate when they are unknown.

Typically, the accurate transponder (TP) carrier frequency and symbol rate are obtained after channel blind scanning is performed when the TP carrier frequency and symbol rate are unknown. If channel blind scanning is performed when the carrier frequency and symbol rate are known, system synchronization performance is improved.

Three operating states are provided:

- Blind scanning disabled: set CBS_CTRL_RDADDR[use_cbs] to 0.
- Blind scanning when the carrier frequency and symbol rate are known: set CBS_CTRL_RDADDR[use_cbs] and CBS_CTRL_RDADDR[know_fs_fc] to 1 and CBS_CTRL_RDADDR[cbs_rd_addr] to 0. Other operations are the same as non-blind scanning operations.
- Blind scanning at full frequency bands: set CBS_CTRL_RDADDR[use_cbs] to 1 and CBS_CTRL_RDADDR[know_fs_fc] to 0. Multiple TPs may be found during blind scanning. After the TP specified in CBS_CTRL_RDADDR[cbs_rd_addr] is automatically selected, demodulation and FEC decoding are performed.

To perform blind scanning at full frequency bands, perform the following steps:

**Step 1** Initialize Hi3136 V100.

**Step 2** Configure the blind scanning mode by setting CBS_CTRL_RDADDR[use_cbs] to 1 and CBS_CTRL_RDADDR[know_fs_fc] to 0.

**Step 3** Configure the tuner RF frequency, wait 5 to 20 ms, and perform a hot reset. The wait time depends on the tuner.

**Step 4** Wait 2 to 5 ms and query CBS_FINISH[cbs_finish].

- If CBS_FINISH[cbs_finish] is 1, go to Step 5.
- If CBS_FINISH[cbs_finish] is not 1, continue to wait and query.

**Step 5** Read CBS_R2_NUM[sig_num] to obtain the number of valid signals. If CBS_R2_NUM[sig_num] is not 0, set CBS_CTRL_RDADDR[cbs_rd_addr] to 0 and read the symbol rate offset and carrier offset of the first TP. The actual carrier frequency of the first TP is the RF frequency plus or minus the carrier offset, which depends on the hardware.

**Step 6** Set CBS_CTRL_RDADDR[cbs_rd_addr] to 1 and read the information about the second TP by following the descriptions in Step 5. Repeat Step 6 until CBS_CTRL_RDADDR[cbs_rd_addr] is CBS_R2_NUM[vld_sig_num] minus 1. For details about the TP symbol rate offset and carrier offset, see the descriptions of the registers CBS_FS_L, CBS_FS_H, CBS_FC_L, and CBS_FC_H.

**Step 7** Go to Step 2 and change the tuner RF frequency until blind scanning is complete in the specified frequency band range. Note that the frequency increment must be less than or equal to 13.5 MHz.

**Step 8** Process blind scanning results by using software. The processing operations include deleting duplicated TPs, sorting TPs by carrier, and checking TP validity. The operations depend on the software scheme.

**----End**

**CAUTION**

- CBS_RELIABILITY1 and CBS_R2_NUM provide blind scanning reliability measurements for each TP. The measurements can be used in software schemes to form more complicated software control policies, accelerating the blind scanning speed and improving reliability.
- When blind scanning is performed when the carrier frequency and symbol rate are known (CBS_CTRL_RDADDR[know_fs_fc] = 1), the carrier offset in blind scanning results is a relative value based on the known carrier frequency. When blind scanning is performed at full frequency bands, the carrier offset is an absolute value. The blind scanning carrier offset does not contain the carrier offset provided by the CR module.

# 2.18 DiSEqC

The DiSEqc transmits and receives data in compliance with the DiSEqc V2.x standard and controls the working status of satellite front-end devices such as the low noise block (LNB) and multi-switch.

Set DSEC_EN [dsec_en] to enable or disable the DiSEqc peripheral circuit.

- 1: The LNB_EN pin outputs a high level.
- 0: The LNB_EN pin outputs a low level.

Set TX_CTRL1[hv_sel] to select 13 V or 18 V level.

- 1: The HV_SEL pin outputs a high level.
- 0: The HV_SEL pin outputs a low level.

Before using the DiSEqc function, obtain a 22 kHz carrier by setting the frequency divider of CLK_DEMO based on the values of DSEC_RATIO_L (lower eight bits of diseqc_ratio) and DSEC_RATIO_H (upper eight bits of diseqc_ratio). See the following formula:

diseqc_ratio[15:0] = round (CLK_DEMO/22)

Note that the unit of CLK_DEMO is kHz and round indicates a rounding-up operation.

## TX

Set TX_CTRL1[dsec_mode] to select the working mode on the DiSEqc TX end. See Table 2-13.

**Table 2-13** Working modes on the DiSEqc TX end

| dsec_mode Bit[2:0] | TX Mode |
|---|---|
| 000 | Idle. |
| 001 | Consecutive 22 kHz square waves are transmitted. The duty ratio is 50%. |
| 010 | A 0 tone burst is transmitted. |
| 011 | A 1 data burst is transmitted. |
| 100 | DiSEqc messages are transmitted. |
| Others | Reserved. |

Figure 2-8 shows the schematic diagram for the 0 tone burst output.

**Figure 2-8** Schematic diagram for the 0 tone burst output

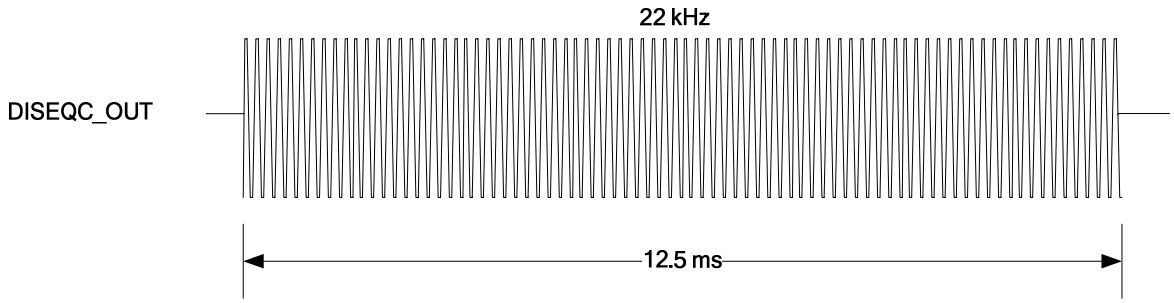



Figure 2-9 shows the schematic diagram for the 1 data burst output.

**Figure 2-9** Schematic diagram for the 1 data burst output

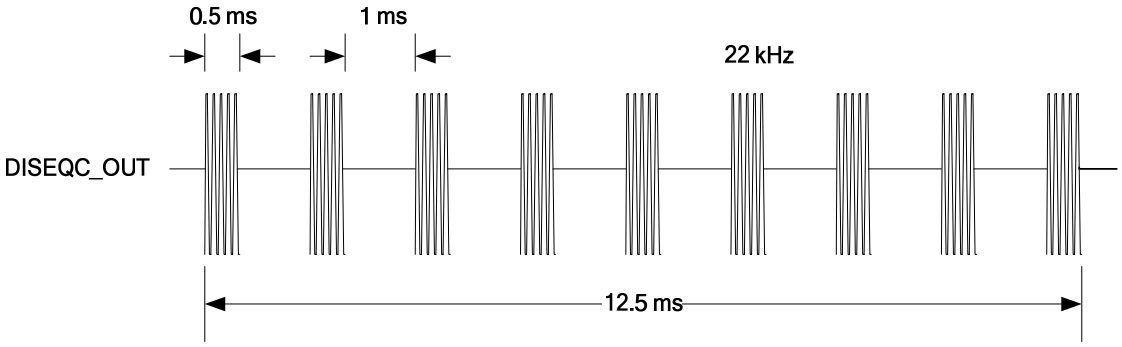
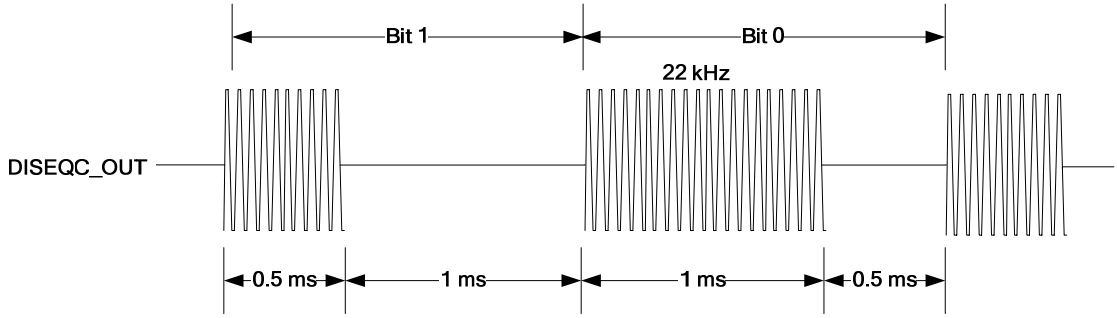



Figure 2-10 shows the schematic diagram for the DiSEqc message output.

**Figure 2-10** Schematic diagram for the DiSEqc message output




The TX procedure is as follows:

**Step 1** Set TX_CTRL1[dsec_mode] to 0. To transmit messages, go to Step 2. To transmit other data, go to Step 6.

**Step 2** Write to DSEC_DATA[dsec_data].

**Step 3** Write the storage address to DSEC_ADDR bit[2:0] and set DSEC_ADDR bit[7] and DSEC_ADDR bit[3] to 0.

**Step 4** Repeat Step 2 and Step 3 until all user data is stored.

**Step 5** Configure TX_CTRL1[num_byte].

**Step 6** Configure TX_CTRL1[dsec_mode] to start transmission.

**Step 7** If TX_CTRL1[dsec_mode] is 001, manually set TX_CTRL1[dsec_mode] to 0. In other modes, TX_CTRL1[dsec_mode] is automatically cleared.

**----End**

**NOTE**

DiSEqc messages are stored in the internal RAM to reduce $I^2C$ addresses. To store data, write data to DSEC_DATA and then write the storage address to DSEC_ADDR. To read data, write the read address to DSEC_ADDR and then read data from DSEC_DATA. The following describes address allocation rules:

- When DSEC_ADDR bit[7] is 1, the current operation is a read operation. When DSEC_ADDR bit[3] is 0, DSEC_ADDR bit[2:0] specify the address for storing the transmitted data.
  When DSEC_ADDR bit[3] is 1, DSEC_ADDR bit[2:0] specify the address for storing the received data.
- When DSEC_ADDR bit[7] is 1, the current operation is a write operation. When DSEC_ADDR bit[3] is 0, DSEC_ADDR bit[2:0] specify the address for storing the transmitted data.
  When DSEC_ADDR bit[3] is 1, the address specified in DSEC_ADDR bit[2:0] is invalid.

### RX

If bit 1 in the first byte of the message to be transmitted is 1, the state machine in the DiSEqc automatically enters the RX status after transmission is complete. The RX procedure is as follows:

**Step 1** Read INT_STATE to obtain the RX status.

**Step 2** Read RX_STATE[rx_recv_bytes] to obtain the number of bytes to be received.

**Step 3** Write the address to be read to DSEC_ADDR bit[2:0] and set DSEC_ADDR bit[7] and DSEC_ADDR bit[3] to 1.

**Step 4** Read DSEC_DATA.

**Step 5** Repeat Step 3 and Step 4 until all data is read.

**----End**

## 2.19 Register Summary

When you write to some bits of a register, you are required to read the register, change the values of the bits to be written, and retain the values of other bits.

If a quantity of state to be read is specified by multiple registers, you need to read the low register and then high register unless otherwise specified. For example, to obtain freq_offset_fc specified by the registers FREQ_OFFSET_FC_L and FREQ_OFFSET_FC_H, read FREQ_OFFSET_FC_L and then FREQ_OFFSET_FC_H.

**CAUTION**

For the registers related to the signal quality, read the high register and then low register.

Table 2-14 describes Demod registers.

**Table 2-14** Summary of Demod registers (base address: 0x00)

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x00 | PLL1_CTRL1 | PLL1 control register 1 | 2-29 |
| 0x01 | PLL1_CTRL2 | PLL1 control register 2 | 2-29 |
| 0x02 | PLL1_CTRL3 | PLL1 control register 3 | 2-30 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x03 | PLL1_CTRL4 | PLL1 control register 4 | 2-30 |
| 0x04 | PLL1_CTRL5 | PLL1 control register 5 | 2-30 |
| 0x05 | PLL2_CTRL1 | PLL2 control register 1 | 2-31 |
| 0x06 | PLL2_CTRL2 | PLL2 control register 2 | 2-31 |
| 0x07 | PLL2_CTRL3 | PLL2 control register 3 | 2-32 |
| 0x08 | PLL2_CTRL4 | PLL2 control register 4 | 2-32 |
| 0x09 | PLL2_CTRL5 | PLL2 control register 5 | 2-32 |
| 0x0A | ADC_CTRL1 | ADC control register 1 | 2-33 |
| 0x0B | TS_CTRL1 | TS control register 1 | 2-34 |
| 0x0C | ADC_CTRL2 | ADC control register 2 | 2-35 |
| 0x0D | IO_CTRL1 | I/O control register 1 | 2-36 |
| 0x0E | IO_CTRL2 | I/O control register 2 | 2-37 |
| 0x0F | TS_CTRL2 | TS control register 2 | 2-37 |
| 0x20 | MAN_RST_CTRL0 | Reset control register | 2-38 |
| 0x21 | MAN_RST_CTRL1 | Reset control enable register | 2-39 |
| 0x22 | STATE_WAITS | Timeout reset register | 2-40 |
| 0x23 | CLK_DEMO_L | Demodulation clock low register | 2-40 |
| 0x24 | CLK_DEMO_M | Demodulation clock middle register | 2-41 |
| 0x25 | CLK_DEMO_H | Demodulation clock high register | 2-41 |
| 0x26 | CLK_FEC_L | FEC decoding clock low register | 2-42 |
| 0x27 | CLK_FEC_M | FEC decoding clock middle register | 2-42 |
| 0x28 | CLK_FEC_H | FEC decoding clock high register | 2-42 |
| 0x29 | LOCK_TIME_L | Lock time low register | 2-43 |
| 0x2A | LOCK_TIME_M | Lock time middle register | 2-43 |
| 0x2B | LOCK_TIME_H | Lock time high register | 2-43 |
| 0x2C | LOCK_FLAG | Lock flag register | 2-44 |
| 0x2D | TUNER_SEL | Tuner control register | 2-44 |
| 0x2E | RSTN_CTRL | Logic reset register | 2-45 |
| 0x2F | ILA_SEL | Test vector select register | 2-45 |
| 0x30 | AGC_SPEED_BOUND | AGC step register | 2-46 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x31 | AGC_GOAL | AGC power register | 2-46 |
| 0x32 | AGCOK_WAIT | AGC wait register | 2-47 |
| 0x33 | AGC_CTRL | AGC control register | 2-47 |
| 0x34 | AGC_DC_I | Channel I direct current (DC) register | 2-48 |
| 0x35 | AGC_DC_Q | Channel Q DC register | 2-48 |
| 0x36 | DAGC_CTRL | Digital AGC (DAGC) control register | 2-48 |
| 0x37 | AGC_CTRL_L | AGC power low register | 2-49 |
| 0x38 | AGC_CTRL_H | AGC power high register | 2-49 |
| 0x39 | AMP_ERR_IIR | Power error register | 2-50 |
| 0x3A | PDM_CTRL_L | Manual AGC control word low register | 2-50 |
| 0x3B | PDM_CTRL_H | Manual AGC control word high register | 2-50 |
| 0x40 | TR_CTRL1 | TR control register | 2-51 |
| 0x41 | DAGC_STD | DAGC control register | 2-51 |
| 0x43 | TR_MONITOR | TR monitor register | 2-52 |
| 0x44 | CNT_THRESH | TR wait time register | 2-52 |
| 0x46 | FS_L | Symbol rate low register | 2-53 |
| 0x47 | FS_H | Symbol rate high register | 2-53 |
| 0x48 | CENT_FREQ_L | Carrier frequency low register | 2-53 |
| 0x49 | CENT_FREQ_H | Carrier frequency high register | 2-54 |
| 0x4C | FS_OFFSET_FC_L | Symbol rate offset low register | 2-54 |
| 0x4D | FS_OFFSET_FC_H | Symbol rate offset high register | 2-55 |
| 0x4E | FREQ_OFFSET_FC_L | Frequency offset low register | 2-55 |
| 0x4F | FREQ_OFFSET_FC_H | Frequency offset high register | 2-55 |
| 0x50 | PLH_SYNC_1 | Frame synchronization control register 1 | 2-56 |
| 0x51 | PLH_SYNC_2 | Frame synchronization control register 2 | 2-56 |
| 0x52 | CR_CTRL_SW | CR control register | 2-57 |
| 0x53 | SCAN_STEP_L | Frequency scanning speed register | 2-58 |
| 0x54 | SCAN_STEP_FB | Frequency scanning control register | 2-58 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x55 | SCAN_ADJUST | Automatic frequency scanning speed register | 2-59 |
| 0x56 | CR_ZUNI_WAIT | Carrier control register | 2-59 |
| 0x57 | CR_BW_ADJUST | Carrier bandwidth control register | 2-59 |
| 0x58 | CR_BW_MAX | Carrier maximum bandwidth control register | 2-60 |
| 0x59 | CR_BW_SET | Carrier bandwidth control register | 2-60 |
| 0x5A | CR_CN | Carrier noise (CN) ratio register | 2-61 |
| 0x5B | CR_STATE | Carrier status register | 2-61 |
| 0x5C | PLS_CODE | PLS_CODE register | 2-61 |
| 0x5D | FREQ_INV | Spectrum inversion register | 2-62 |
| 0x5E | CR_ZUNI_BW_L | Carrier bandwidth low register | 2-62 |
| 0x5F | CR_ZUNI_BW_H | Carrier bandwidth high register | 2-63 |
| 0x60 | SYNC_FREQ_L | Frame synchronization frequency low register. | 2-63 |
| 0x61 | SYNC_FREQ_H | Frame synchronization frequency high register | 2-63 |
| 0x62 | SCAN_FREQ_L | Scanning frequency low register. | 2-64 |
| 0x63 | SCAN_FREQ_H | Scanning frequency high register. | 2-64 |
| 0x64 | FREQ_ACC_L | Carrier frequency offset slow feedback low register | 2-65 |
| 0x65 | FREQ_ACC_H | Carrier frequency offset slow feedback high register | 2-65 |
| 0x66 | TR_FREQ_FB_L | Carrier frequency offset TR feedback low register | 2-65 |
| 0x67 | TR_FREQ_FB_H | Carrier frequency offset TR feedback high register | 2-66 |
| 0x68 | CR_LOOP_DC_L | Carrier PLL control word low register | 2-66 |
| 0x69 | CR_LOOP_DC_H | Carrier PLL control word high register | 2-66 |
| 0x6C | CHIP_ID_0 | Chip ID register 0 | 2-67 |
| 0x6D | CHIP_ID_1 | Chip ID register 1 | 2-67 |
| 0x6E | CHIP_ID_2 | Chip ID register 2 | 2-67 |
| 0x6F | CHIP_ID_3 | Chip ID register 3 | 2-68 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x70 | EQU_CTRL | Equalization control register | 2-68 |
| 0x71 | LMS_STEP | Equalization step control register | 2-69 |
| 0x75 | CN_CTRL | Noise power statistics control register | 2-69 |
| 0x76 | EQU_TAP_REAL | Equalization tap real part register | 2-70 |
| 0x77 | EQU_TAP_IMAG | Equalization tap imaginary part register | 2-70 |
| 0x78 | EQU_TAP_SEL | Tap select register | 2-70 |
| 0x7A | XREG_INIT_LOW | Equalization control low register | 2-71 |
| 0x7B | XREG_INIT_MID | Equalization control middle register | 2-71 |
| 0x7C | XREG_INIT_HI | Equalization control high register | 2-72 |
| 0x7D | RD_WR_TAP | Tap control register | 2-72 |
| 0x7E | NOISE_POW_L | Noise power low register | 2-73 |
| 0x7F | NOISE_POW_H | Noise power high register | 2-73 |
| 0x82 | LDPC_ITER | LDPC iteration control register | 2-73 |
| 0x83 | BER_CTRL | BER control register | 2-74 |
| 0x84 | FEC_BER_L | BER low register | 2-74 |
| 0x85 | FEC_BER_H | BER high register | 2-75 |
| 0x86 | FEC_FER_L | FER low register | 2-75 |
| 0x87 | FEC_FER_H | FER high register | 2-75 |
| 0x88 | S2_SUCCESS | S2 decoding success register | 2-76 |
| 0x89 | VTB_CTRL1 | VTB control register 1 | 2-76 |
| 0x8A | VTB_THRES | VTB search control register | 2-77 |
| 0x8B | VTB_CTRL2 | VTB control register 2 | 2-78 |
| 0x8C | FS_CTRL1 | S frame synchronization control register 1 | 2-78 |
| 0x8D | FS_CTRL2 | S frame synchronization control register 2 | 2-79 |
| 0x8E | SEAR_RESULT | S search result register | 2-79 |
| 0x8F | DEC_RESULT | S decoding result register | 2-80 |
| 0x90 | TS_PARALL_CTRL | TS output select register | 2-81 |
| 0x91 | TS_10_SEL | TS output control register | 2-82 |
| 0x92 | TS_32_SEL | TS output control register | 2-82 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x93 | TS_54_SEL | TS output control register | 2-82 |
| 0x94 | TS_76_SEL | TS output control register | 2-83 |
| 0x95 | TS_98_SEL | TS output control register | 2-83 |
| 0x96 | TS_CTRL0 | TS control register 0 | 2-84 |
| 0x97 | TS_CTRL3 | TS control register 3 | 2-85 |
| 0x98 | TS_CTRL4 | TS control register 4 | 2-85 |
| 0x99 | TS_CLK_DIV_F_L | TS clock low register | 2-86 |
| 0x9A | TS_CLK_DIV_F_H | TS clock high register | 2-86 |
| 0x9B | ISI_SEL | Input stream identifier (ISI) select register | 2-87 |
| 0x9C | MATTYPE | Stream ID register | 2-87 |
| 0x9D | ROLL_OFF | Roll-off register | 2-87 |
| 0x9E | CRC_ERR | CRC check register | 2-88 |
| 0x9F | RST_WAIT | Reset wait register | 2-88 |
| 0xA0 | FC_MAX_RELIABLE | Blind scanning carrier control register | 2-89 |
| 0xA1 | FS_SPAN | Blind scanning symbol rate range register | 2-89 |
| 0xA7 | AMP_MIN_FS | Blind scanning minimum symbol rate register | 2-90 |
| 0xA8 | CBS_CTRL_RDADDR | Blind scanning control register | 2-90 |
| 0xA9 | CBS_FS_L | Bind scanning symbol rate low register | 2-91 |
| 0xAA | CBS_FS_H | Bind scanning symbol rate high register | 2-91 |
| 0xAB | CBS_FC_L | Blind scanning frequency offset low register | 2-92 |
| 0xAC | CBS_FC_H | Blind scanning frequency offset high register | 2-92 |
| 0xAD | CBS_FINISH | Blind scanning completion register | 2-93 |
| 0xAE | CBS_RELIABILITY1 | Blind scanning reliability register | 2-93 |
| 0xAF | CBS_R2_NUM | Blind scanning signal count register | 2-93 |
| 0xB0 | DSEC_ADDR | DSEC address register | 2-94 |
| 0xB1 | DSEC_DATA | DSEC data register | 2-94 |
| 0xB2 | DSEC_RATIO_L | DSEC frequency low register | 2-95 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0xB3 | DSEC_RATIO_H | DSEC frequency high register | 2-95 |
| 0xB4 | TX_CTRL1 | DSEC TX control register | 2-96 |
| 0xB5 | RX_CTRL1 | DSEC RX control register | 2-96 |
| 0xB7 | DSEC_EN | DSEC enable register | 2-97 |
| 0xB8 | RX_STATE | DSEC RX status register | 2-97 |
| 0xB9 | INT_STATE | DSEC status register | 2-98 |
| 0xC0 | DF_FC_L | FSK frequency offset low register | 2-98 |
| 0xC1 | DF_FC_H | FSK frequency offset high register | 2-99 |
| 0xC2 | FS_FC_L | FSK symbol rate low register | 2-99 |
| 0xC3 | FS_FC_M | FSK symbol rate middle register | 2-100 |
| 0xC4 | FS_FC_H | FSK symbol rate high register | 2-100 |
| 0xC5 | HEAD_L | Frame header low register | 2-100 |
| 0xC6 | HEAD_M | Frame header middle register | 2-101 |
| 0xC7 | HEAD_H | Frame header high register | 2-101 |
| 0xC8 | NBIT_HEAD | FSK control register | 2-101 |
| 0xC9 | CRC_POLY_L | CRC low register | 2-102 |
| 0xCA | CRC_POLY_M | CRC middle register | 2-102 |
| 0xCB | CRC_POLY_H | CRC high register | 2-102 |
| 0xCC | NBIT_CRC | CRC control register | 2-103 |
| 0xCD | TCF_FC_L | TX frequency low register | 2-103 |
| 0xCE | TCF_FC_H | TX frequency high register | 2-104 |
| 0xCF | RCF_FC_L | RX frequency low register | 2-104 |
| 0xD0 | RCF_FC_H | RX frequency high register | 2-104 |
| 0xD1 | TX_NBIT_L | TX control register | 2-105 |
| 0xD2 | TX_CTRL2 | TX control register | 2-105 |
| 0xD3 | RX_NBIT_L | RX control register | 2-106 |
| 0xD4 | RX_CTRL2 | RX control register | 2-106 |
| 0xD5 | FSK_ADDR | FSK address register | 2-107 |
| 0xD6 | FSK_DATA | FSK data register | 2-107 |
| 0xD7 | FSK_RX_LEN | FSK control register | 2-108 |

# 2.20 Demod Register Descriptions

## PLL1_CTRL1

PLL1_CTRL1 is PLL1 control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x00 | PLL1_CTRL1 | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll1_pd | pll1_bypass | pll1_refdiv | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | pll1_pd | Global power-down signal of PLL1, active high. |
| [6] | RW | pll1_bypass | PLL1 bypass signal, active high. |
| [5:0] | RW | pll1_refdiv | PLL1 frequency divider. The frequency-division clock ranges from 1 MHz to 40 MHz. |

## PLL1_CTRL2

PLL1_CTRL2 is PLL1 control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x01 | PLL1_CTRL2 | 0x61 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll1_dsmpd | pll1_postdiv2 | | | pll1_dacpd | pll1_postdiv1 | | |
| Reset | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | pll1_dsmpd | Delta sigma power-down signal of PLL1.<br>1: integral frequency division<br>0: decimal frequency division |
| [6:4] | RW | Pll1_postdiv2 | Value of frequency divider 2 after PLL1 VCO.<br>FOUT = FVCO/postdiv1/postdiv2 |
| [3] | RW | pll1_dacpd | DAC pd signal of PLL1. The signal is low in normal cases. |
| [2:0] | RW | pll1_postdiv1 | Value of frequency divider 1 after PLL2 VCO.<br>FOUT = FVCO/postdiv1/postdiv2 |

## PLL1_CTRL3

PLL1_CTRL3 is PLL1 control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x02 | PLL1_CTRL3 | 0x1F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll1_fbdiv | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | pll1_fbdiv | Lower eight bits of the integral frequency divider of PLL1. The upper four bits are not used and are fixed at 0. |

## PLL1_CTRL4

PLL1_CTRL4 is PLL1 control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x03 | PLL1_CTRL4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll1_frac_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | pll1_frac_l | Bits 19−12 of the decimal frequency divider of PLL1. The lower 12 bits are not used and are fixed at 0. |

## PLL1_CTRL5

PLL1_CTRL5 is PLL1 control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x04 | PLL1_CTRL5 | 0x14 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | pll1_postdivpd | pll1_vcopd | pll1_frac_h | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [5] | RW | pll1_postdivpd | Power-down signal of the frequency divider after PLL1 VCO. The value 1 indicates valid. |
| [4] | RW | pll1_vcopd | Power-down signal of PLL1 VCO buffer. The VCO still works but the output buffer is disabled. |
| [3:0] | RW | pll1_frac_h | Bits 23−20 of the decimal frequency divider of PLL1. The lower 12 bits are not used and are fixed at 0. |

## PLL2_CTRL1

PLL2_CTRL1 is PLL2 control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x05 | PLL2_CTRL1 | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll2_pd | pll2_bypass | pll2_refdiv | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | pll2_pd | Global power-down signal of PLL2, active high. |
| [6] | RW | pll2_bypass | PLL2 bypass signal, active high. |
| [5:0] | RW | pll2_refdiv | PLL2 frequency divider. The frequency-division clock ranges from 1 MHz to 40 MHz. |

## PLL2_CTRL2

PLL2_CTRL2 is PLL2 control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x06 | PLL2_CTRL2 | 0x61 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll2_dsmpd | pll2_postdiv2 | | | pll2_dacpd | pll2_postdiv1 | | |
| Reset | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | pll2_dsmpd | Delta sigma power-down signal of PLL2. The value 1 indicates integral frequency division and the value 0 indicates decimal frequency division. |
| [6:4] | RW | pll2_postdiv2 | Value of frequency divider 2 after PLL2 VCO.<br>FOUT = FVCO/postdiv1/postdiv2 |

| | | | |
|---|---|---|---|
| [3] | RW | pll2_dacpd | DAC pd signal of PLL2. The signal is low in normal cases. |
| [2:0] | RW | pll2_postdiv1 | Value of frequency divider 1 after PLL2 VCO.<br>FOUT = FVCO/postdiv1/postdiv2 |

## PLL2_CTRL3

PLL2_CTRL3 is PLL2 control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x07 | PLL2_CTRL3 | 0x2E |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll2_fbdiv | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | pll2_fbdiv | Lower eight bits of the integral frequency divider of PLL2. The upper four bits are not used and are fixed at 0. |

## PLL2_CTRL4

PLL2_CTRL4 is PLL2 control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x08 | PLL2_CTRL4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll2_frac_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | pll2_frac_l | Bits 19−12 of the decimal frequency divider of PLL2. The lower 12 bits are not used and are fixed at 0. |

## PLL2_CTRL5

PLL2_CTRL5 is PLL2 control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x09 | PLL2_CTRL5 | 0x1E |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | pll2_postdivpd | pll2_vcopd | pll2_frac_h | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5] | RW | pll2_postdivpd | Power-down signal of the frequency divider after PLL2 VCO. The value 1 indicates valid. |
| [4] | RW | pll2_vcopd | Power-down signal of PLL2 VCO buffer. The VCO still works but the output buffer is disabled. |
| [3:0] | RW | pll2_frac_h | Bits 23−20 of the decimal frequency divider of PLL2. The lower 12 bits are not used and are fixed at 0. |

## ADC_CTRL1

ADC_CTRL1 is ADC control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0A | ADC_CTRL1 | 0x4A |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | adc_odf | adc_pdclamp | adc_om | | adc_cs | | adc_is | |
| Reset | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | adc_odf | Output format.<br>1: complement<br>0: sign-and-magnitude |
| [6] | RW | adc_pdclamp | ADC mode.<br>1: AC mode<br>0: DC mode |
| [5:4] | RW | adc_om | Mode select.<br>00: normal mode<br>01: standby mode (minimum startup time)<br>10: minimum power consumption mode<br>11: power-down mode |

| | | | |
|---|---|---|---|
| [3:2] | RW | adc_cs | Channel signal.<br>00: channel I<br>11: channel Q<br>10: channel I and channel Q<br>11: reserved |
| [1:0] | RW | adc_is | Bias control.<br>00: reduced by 50% based on the current value<br>01: reduced by 25% based on the current value<br>10: no offset<br>11: increased by 25% based on the current value |

## TS_CTRL1

TS_CTRL1 is TS control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0B | TS_CTRL1 | 0x6C |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_vld_ds | | | ts_err_ds | | | reserved | |
| Reset | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | ts_vld_ds | Drive current of the TS_VLD pin.<br>000: 0 mA<br>001: 4 mA<br>010: 8 mA<br>011: 12 mA<br>100: 12 mA<br>101: 16 mA<br>110: 20 mA<br>111: 24 mA |

| | | | |
|---|---|---|---|
| [4:2] | RW | ts_err_ds | Drive current of the TS_ERR pin.<br>000: 0 mA<br>001: 4 mA<br>010: 8 mA<br>011: 12 mA<br>100: 12 mA<br>101: 16 mA<br>110: 20 mA<br>111: 24 mA |
| [1:0] | - | reserved | Reserved. |

## ADC_CTRL2

ADC_CTRL2 is ADC control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0C | ADC_CTRL2 | 0x52 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | adc_clk_sel | adc_clk_on | adc_clk_inv | i2c_xo_clk | reserved | clk_inv | lock_fsko | ts_testout |
| Reset | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | adc_clk_sel | ADC I/O clock.<br>1: TS_SYNC is the input port of adc_clk.<br>0: TS_SYNC is the output port of the ts_sync signal. |
| [6] | RW | adc_clk_on | ADC clock enable.<br>1: normal clock<br>0: no clock |
| [5] | RW | adc_clk_inv | ADC clock invert.<br>1: inverse clock<br>0: forward clock |
| [4] | RW | i2c_xo_clk | Crystal oscillator clock.<br>1: The crystal oscillator input clock acts as the clk_i2c clock.<br>0: The PLL output clock acts as the clk_i2c clock. |
| [3] | - | reserved | Reserved. |
| [2] | RW | clk_inv | TS serial clock invert.<br>1: inverse output<br>0: forward output |

| | | | |
|---|---|---|---|
| [1] | RW | lock_fsko | Lock output.<br>1: FSK output<br>0: channel OK output |
| [0] | RW | ts_testout | Test mode.<br>0: TSs are output in normal mode.<br>1: The TS pin is multiplexed for test signal output. |

## IO_CTRL1

IO_CTRL1 is I/O control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0D | IO_CTRL1 | 0x1B |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | adc_im | adc_clk_sel | ts_out_ds | | | ts_sync_ds | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | adc_im | Input mode.<br>1: single-end input<br>0: differential input |
| [6] | RW | adc_clk_sel | ADC clock.<br>1: I/O clock<br>0: PLL output clock |
| [5:3] | RW | ts_out_ds | Drive current of the TS_OUT pin.<br>000: 0 mA<br>001: 4 mA<br>010: 8 mA<br>011: 12 mA<br>100: 12 mA<br>101: 16 mA<br>110: 20 mA<br>111: 24 mA |

| | | | |
|---|---|---|---|
| [2:0] | RW | ts_sync_ds | Drive current of the TS_SYNC pin.<br>000: 0 mA<br>001: 4 mA<br>010: 8 mA<br>011: 12 mA<br>100: 12 mA<br>101: 16 mA<br>110: 20 mA<br>111: 24 mA |

## IO_CTRL2

IO_CTRL2 is I/O control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0E | IO_CTRL2 | 0x1B |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | test_clk_en | clkout_sel | fsko_ds | | | ts_clk_ds | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | test_clk_en | Test clock enable.<br>1: test clock output<br>0: normal mode |
| [6] | RW | clkout_sel | Clock output control.<br>1: The diseqc_in and diseqc_out are multiplexed to output clocks of PLL0 and PLL1.<br>0: The normal pin function is used. |
| [5:3] | RW | fsko_ds | Drive current of the FSK_OUT pin. |
| [2:0] | RW | ts_clk_ds | Drive current of the TS_CLK pin. |

## TS_CTRL2

TS_CTRL2 is TS control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0F | TS_CTRL2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pll2_lock | pll1_lock | ts_out_sl | ts_sync_sl | ts_vld_sl | ts_err_sl | ts_clk_sl | fsko_sl |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | pll2_lock | PLL2 clock flag.<br>1: locked<br>0: unlocked |
| [6] | RO | pll1_lock | PLL1 clock flag.<br>1: locked<br>0: unlocked |
| [5] | RW | ts_out_sl | TS_OUT pin speed adjustment.<br>1: slow edge<br>0: fast edge |
| [4] | RW | ts_sync_sl | TS_SYNC pin speed adjustment.<br>1: slow edge<br>0: fast edge |
| [3] | RW | ts_vld_sl | TS_VLD pin speed adjustment.<br>1: slow edge<br>0: fast edge |
| [2] | RW | ts_err_sl | TS_ERR pin speed adjustment.<br>1: slow edge<br>0: fast edge |
| [1] | RW | ts_clk_sl | TS_CLK pin speed adjustment.<br>1: slow edge<br>0: fast edge |
| [0] | RW | fsko_sl | FSK_OUT pin speed adjustment.<br>1: slow edge<br>0: fast edge |

## MAN_RST_CTRL0

MAN_RST_CTRL0 is a reset control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x20 | MAN_RST_CTRL0 | 0xFF |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rstn_fsk | rstn_outp | rstn_fec | rstn_equ | rstn_cr | rstn_tr | rstn_cbs | rstn_agc |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | rstn_fsk | FSK reset.<br>1: deassert reset<br>0: reset |
| [6] | RW | rstn_outp | OUTP reset.<br>1: deassert reset<br>0: reset |
| [5] | RW | rstn_fec | FEC reset.<br>1: deassert reset<br>0: reset |
| [4] | RW | rstn_equ | EQU reset.<br>1: deassert reset<br>0: reset |
| [3] | RW | rstn_cr | CR reset.<br>1: deassert reset<br>0: reset |
| [2] | RW | rstn_tr | TR reset.<br>1: deassert reset<br>0: reset |
| [1] | RW | rstn_cbs | CBS reset.<br>1: deassert reset<br>0: reset |
| [0] | RW | rstn_agc | AGC reset.<br>1: deassert reset<br>0: reset |

## MAN_RST_CTRL1

MAN_RST_CTRL1 is a reset control enable register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x21 | MAN_RST_CTRL1 | 0x07 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | auto_rst_ena | rstn_diseqc | rstn_catch |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |
| [2] | RW | auto_rst_ena | FEC auto reset enable.<br>1: enabled<br>0: disabled |
| [1] | RW | rstn_diseqc | DiSEqC reset.<br>1: deassert reset<br>0: reset |
| [0] | RW | rstn_catch | Catch reset.<br>1: deassert reset<br>0: reset |

## STATE_WAITS

STATE_WAITS is a timeout reset register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x22 | STATE_WAITS | 0x1B |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | state_wait | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | state_wait | OK signal wait timeout reset.<br>When bit[28:21] of the counter are greater than the state_wait field, the system is reset. |

## CLK_DEMO_L

CLK_DEMO_L is a demodulation clock low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x23 | CLK_DEMO_L | 0x48 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | clk_demo_l | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | clk_demo_l | Lower bits of the frequency of the demodulation clock CLK_DEMO. The LSB indicates 1 kHz. |

## CLK_DEMO_M

CLK_DEMO_M is a demodulation clock middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x24 | CLK_DEMO_M | 0xE8 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | clk_demo_m | | | | | | | |
| Reset | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | clk_demo_m | Middle bits of the frequency of the demodulation clock CLK_DEMO. |

## CLK_DEMO_H

CLK_DEMO_H is a demodulation clock high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x25 | CLK_DEMO_H | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | clk_demo_h | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | - | reserved | Reserved. |
| [1:0] | RW | clk_demo_h | Upper bits of the frequency of the demodulation clock CLK_DEMO. |

## CLK_FEC_L

CLK_FEC_L is an FEC decoding clock low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x26 | CLK_FEC_L | 0x6C |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | clk_fec_l | | | | | | | |
| Reset | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | clk_fec_l | Lower bits of the frequency of the FEC decoding clock CLK_FEC. The LSB indicates 1 kHz. |

## CLK_FEC_M

CLK_FEC_M is an FEC decoding clock middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x27 | CLK_FEC_M | 0xDC |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | clk_fec_m | | | | | | | |
| Reset | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | clk_fec_m | Middle bits of the frequency of the FEC decoding clock CLK_FEC. |

## CLK_FEC_H

CLK_FEC_H is an FEC decoding clock high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x28 | CLK_FEC_H | 0x02 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | clk_fec_h | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | - | reserved | Reserved. |
| [1:0] | RW | clk_fec_h | Upper bits of the frequency of the FEC decoding clock CLK_FEC. |

## LOCK_TIME_L

LOCK_TIME_L is a lock time low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x29 | LOCK_TIME_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tr_time | | | | cbs_time | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RO | tr_time | TR lock time. Its unit is 10 ms. |
| [3:0] | RO | cbs_time | CBS lock time. Its unit is 10 ms. |

## LOCK_TIME_M

LOCK_TIME_M is a lock time middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x2A | LOCK_TIME_M | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_time_l | | | | sync_time | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RO | cr_time_l | Lower four bits of the CR lock time. Its unit is 10 ms. |
| [3:0] | RO | sync_time | Sync lock time. Its unit is 10 ms. |

## LOCK_TIME_H

LOCK_TIME_H is a lock time high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x2B | LOCK_TIME_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fec_time | | | | | | cr_time_h | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | RO | fec_time | FEC lock time. Its unit is 10 ms. |

| | | | |
|---|---|---|---|
| [1:0] | RO | cr_time_h | Upper two bits of the CR lock time. |

## LOCK_FLAG

LOCK_FLAG is a lock flag register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x2C | LOCK_FLAG | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | fec_ok | cr_ok | sync_ok | tr_ok | cbs_ok | agc_ok |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5] | RO | fec_ok | FEC lock flag.<br>1: locked<br>0: unlocked |
| [4] | RO | cr_ok | CR lock flag.<br>1: locked<br>0: unlocked |
| [3] | RO | sync_ok | Sync lock flag.<br>1: locked<br>0: unlocked |
| [2] | RO | tr_ok | TR lock flag.<br>1: locked<br>0: unlocked |
| [1] | RO | cbs_ok | CBS lock flag.<br>1: locked<br>0: unlocked |
| [0] | RO | agc_ok | AGC lock flag.<br>1: locked<br>0: unlocked |

## TUNER_SEL

TUNER_SEL is a tuner control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x2D | TUNER_SEL | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | man_state | | | tuner_sel |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:1] | RO | man_state | Status of the main control state machine. |
| [0] | RW | tuner_sel | Tuner signal selected by configuring the $I^2C$.<br>This field must be set to 1 before the tuner is configured. Each time after the tuner is read or written, this field is automatically cleared. If you need to continue to configure the tuner, set this field to 1 again. |

## RSTN_CTRL

RSTN_CTRL is a logic reset register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x2E | RSTN_CTRL | 0x03 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | hot_rstn | cool_rstn |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | - | reserved | Reserved. |
| [1] | RW | hot_rstn | Logic reset signal. Only the logic but not the system registers are reset.<br>1: not reset<br>0: reset |
| [0] | RW | cool_rstn | Reset signal. The logic and system registers are reset.<br>1: not reset<br>0: reset |

## ILA_SEL

ILA_SEL is test vector select register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x2F | ILA_SEL | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ila_sel | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ila_sel | Test vector select for the ILA and Catch modules. |

## AGC_SPEED_BOUND

AGC_SPEED_BOUND is an AGC step register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x30 | AGC_SPEED_BOUND | 0x67 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_speed | | | err_bound | | | | |
| Reset | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | agc_speed | AGC step. The actual value is the configured value plus 2 and the maximum value is 7. |
| [4:0] | RW | err_bound | Amplitude error boundary. |

## AGC_GOAL

AGC_GOAL is an AGC power register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x31 | AGC_GOAL | 0x22 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_goal | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agc_goal | Target AGC power. |

## AGCOK_WAIT

AGCOK_WAIT is an AGC wait register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x32 | AGCOK_WAIT | 0x0F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agcok_wait | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agcok_wait | AGC amplitude abnormal wait period. |

## AGC_CTRL

AGC_CTRL is an AGC control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x33 | AGC_CTRL | 0x71 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pdm_div | | | adc_twos | iq_swap | agc_hold | agc_inverse | dagc_on |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | pdm_div | Pulse width of the AGC PDM output.<br>The actual value is the configured value plus 1. |
| [4] | RW | adc_twos | Input data format.<br>1: complement<br>0: sign-and-magnitude |
| [3] | RW | iq_swap | I/Q data switch.<br>1: switched<br>0: not switched |
| [2] | RW | agc_hold | AGC working type.<br>1: The AGC holds and the output PDM is a fixed value.<br>0: The AGC works in normal mode. |
| [1] | RW | agc_inverse | PDM signal output.<br>1: inverted<br>0: not inverted (normal output) |

| | | | |
|---|---|---|---|
| [0] | RW | dagc_on | DAGC enable.<br>1: enabled<br>0: disabled |

## AGC_DC_I

AGC_DC_I is a channel I DC register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x34 | AGC_DC_I | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_dc_i | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | agc_dc_i | DC value of channel I data. |

## AGC_DC_Q

AGC_DC_Q is a channel Q DC register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x35 | AGC_DC_Q | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_dc_q | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | agc_dc_q | DC value of channel Q data. |

## DAGC_CTRL

DAGC_CTRL is a DAGC control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x36 | DAGC_CTRL | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dagc_ctrl | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | dagc_ctrl | Control word of the DAGC. |

## AGC_CTRL_L

AGC_CTRL_L is an AGC power low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x37 | AGC_CTRL_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_ctrl_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | agc_ctrl_l | Lower eight bits of the AGC control word, indicating the current signal power. |

## AGC_CTRL_H

AGC_CTRL_H is an AGC power high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x38 | AGC_CTRL_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_ok | reserved | | | agc_ctrl_h | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | agc_ok | AGC lock.<br>1: locked<br>0: unlock |
| [6:4] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [3:0] | RO | agc_ctrl_h | Upper four bits of the AGC control word, indicating the current signal power. |

## AMP_ERR_IIR

AMP_ERR_IIR is a power error register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x39 | AMP_ERR_IIR | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | amp_err_iir | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | amp_err_iir | Error between the data power and the reference power. |

## PDM_CTRL_L

PDM_CTRL_L is manual AGC control word low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3A | PDM_CTRL_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pdm_ctrl_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | pdm_ctrl_l | Lower eight bits of the configurable AGC control word in manual AGC mode. |

## PDM_CTRL_H

PDM_CTRL_H is manual AGC control word high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3B | PDM_CTRL_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | pdm_ctrl_sel | pdm_ctrl_h | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4] | RW | pdm_ctrl_sel | Manual AGC control.<br>1: manual mode (pdm_ctrl_sel acts as the control word)<br>0: automatic AGC mode |
| [3:0] | RW | pdm_ctrl_h | Upper four bits of the configurable AGC control word in manual AGC mode. |

## TR_CTRL1

TR_CTRL1 is a TR control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x40 | TR_CTRL1 | 0x21 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | dagc_bypass | dagc_speed | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3] | RW | dagc_bypass | DAGC bypass.<br>1: bypass<br>0: not bypass |
| [2:0] | RW | dagc_speed | DAGC adjustment speed.<br>A larger value indicates a faster AGC adjustment speed. |

## DAGC_STD

DAGC_STD is a DAGC control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x41 | DAGC_STD | 0x20 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dagc_std | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | dagc_std | Average amplitude after DAGC adjustment.<br>A larger value indicates a larger amplitude. |

## TR_MONITOR

TR_MONITOR is a TR monitor register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x43 | TR_MONITOR | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tr_ok | reserved | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | tr_ok | Timing lock flag.<br>1: locked<br>0: unlocked |
| [6:0] | - | reserved | Reserved. |

## CNT_THRESH

CNT_THRESH is a TR wait time register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x44 | CNT_THRESH | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cnt_thresh | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | cnt_thresh | Lock detection wait time.<br>A larger value indicates longer wait time. |

## FS_L

FS_L is a symbol rate low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x46 | FS_L | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_l | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fs_l | Lower bits of the symbol rate. The symbol rate is an unsigned number. The LSB indicates 1 kHz. |

## FS_H

FS_H is a symbol rate high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x47 | FS_H | 0x27 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_h | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fs_h | Upper bits of the symbol rate. The symbol rate is an unsigned number. The LSB indicates 1 kHz. |

## CENT_FREQ_L

CENT_FREQ_L is a carrier frequency low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x48 | CENT_FREQ_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cent_freq_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | cent_freq_l | Lower bits of the carrier center frequency. The center frequency is a signed number. The LSB indicates 1 kHz. |

## CENT_FREQ_H

CENT_FREQ_H is a carrier frequency high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x49 | CENT_FREQ_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cent_freq_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | cent_freq_h | Upper bits of the carrier center frequency. The center frequency is a signed number. The LSB indicates 1 kHz. |

## FS_OFFSET_FC_L

FS_OFFSET_FC_L is a symbol rate offset low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x4C | FS_OFFSET_FC_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_offset_fc_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | fs_offset_fc_l | Lower bits of the symbol rate offset normalized to the system clock. The symbol rate offset is a signed number. The actual normalized offset is fs_offset_fc/2^22. |

## FS_OFFSET_FC_H

FS_OFFSET_FC_H is a symbol rate offset high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x4D | FS_OFFSET_FC_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_offset_fc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | fs_offset_fc_h | Upper bits of the symbol rate offset normalized to the system clock. The symbol rate offset is a signed number. The actual normalized offset is fs_offset_fc/2^22. |

## FREQ_OFFSET_FC_L

FREQ_OFFSET_FC_L is a frequency offset low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x4E | FREQ_OFFSET_FC_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | freq_offset_fc_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | freq_offset_fc_l | Lower bits of the carrier frequency offset normalized to the system clock. The carrier frequency offset is a signed number. The actual normalized offset is freq_offset_fc/2^17. |

## FREQ_OFFSET_FC_H

FREQ_OFFSET_FC_H is a frequency offset high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x4F | FREQ_OFFSET_FC_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | freq_offset_fc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | freq_offset_fc_h | Upper bits of the carrier frequency offset normalized to the system clock. The carrier frequency offset is a signed number. The actual normalized offset is freq_offset_fc/2^17. |

## PLH_SYNC_1

PLH_SYNC_1 is frame synchronization control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x50 | PLH_SYNC_1 | 0x4F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | plh_sync_th | | | | reserved | | | |
| Reset | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | plh_sync_th | Confidence count threshold for determining whether frame synchronization enters the synchronization state. A smaller value indicates a faster synchronization speed but easier false synchronization. |
| [3:0] | - | reserved | Reserved. |

## PLH_SYNC_2

PLH_SYNC_2 is frame synchronization control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x51 | PLH_SYNC_2 | 0x49 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | plh_lost_th | | | | plh_am_th | | | |
| Reset | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | plh_lost_th | Number of lost frames when lock loss is checked during frame synchronization. A smaller value indicates a faster check speed but easier false lock loss. |
| [3:0] | RW | plh_am_th | Amplitude threshold for frame synchronization. A smaller value indicates higher synchronization performance but slower synchronization speed. |

## CR_CTRL_SW

CR_CTRL_SW is a CR control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x52 | CR_CTRL_SW | 0x3F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_crfb_bypass | ccm_dummy | denbi_bypass | use_intp | reserved | use_pulse_det | scan_auto | cr_bw_auto |
| Reset | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | cr_crfb_bypass | Carrier frequency offset slow feedback bypass.<br>1: bypass<br>0: not bypass |
| [6] | RW | ccm_dummy | Blank frame allowed in the CCM.<br>1: allowed<br>0: not allowed |
| [5] | RW | denbi_bypass | Narrowband interference suppression module bypass.<br>1: bypass<br>0: not bypass |
| [4] | RW | use_intp | Carrier phase interpolation using pilot.<br>1: yes<br>0: no |
| [3] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [2] | RW | use_pulse_det | Pulse interference detection.<br>1: yes<br>0: no |
| [1] | RW | scan_auto | Mode for setting the carrier frequency scanning step.<br>1: automatic mode<br>0: manual mode |
| [0] | RW | cr_bw_auto | Mode for setting the CR bandwidth.<br>1: automatic mode<br>0: manual mode |

## SCAN_STEP_L

SCAN_STEP_L is a frequency scanning speed register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x53 | SCAN_STEP_L | 0x64 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | scan_step_l | | | | | | | |
| Reset | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | scan_step_l | Lower eight bits of the 12-bit frequency scanning speed manually configured. |

## SCAN_STEP_FB

SCAN_STEP_FB is a frequency scanning control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x54 | SCAN_STEP_FB | 0x30 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | fb_speed | | | scan_step_h | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:4] | RW | fb_speed | Carrier frequency slow feedback speed. |
| [3:0] | RW | scan_step_h | Upper four bits of the 12-bit frequency scanning speed manually configured. |

## SCAN_ADJUST

SCAN_ADJUST is an automatic frequency scanning speed register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x55 | SCAN_ADJUST | 0x18 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | scan_adjust | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:0] | RW | scan_adjust | Automatic adjustment of the frequency scanning speed. |

## CR_ZUNI_WAIT

CR_ZUNI_WAIT is a carrier control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x56 | CR_ZUNI_WAIT | 0x8B |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_zuni | | | cr_lock_wait | | | | |
| Reset | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | cr_zuni | Stable damping of the CR PLL. |
| [4:0] | RW | cr_lock_wait | Carrier lock wait time. |

## CR_BW_ADJUST

CR_BW_ADJUST is a carrier bandwidth control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x57 | CR_BW_ADJUST | 0x20 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | bw_adjust | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:0] | RW | bw_adjust | CR bandwidth adjustment. |

## CR_BW_MAX

CR_BW_MAX is a carrier maximum bandwidth control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x58 | CR_BW_MAX | 0xFF |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_bw_max | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | cr_bw_max | Maximum CR bandwidth.<br>Note: The field value multiplied by 32 is the actual maximum bandwidth. |

## CR_BW_SET

CR_BW_SET is a carrier bandwidth control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x59 | CR_BW_SET | 0x1F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_bw_exp | | | cr_bw_coef | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | cr_bw_exp | Exponential part of the bandwidth. |

| | | | |
|---|---|---|---|
| [4:0] | RW | cr_bw_coef | Decimal part of the bandwidth.<br>The actual bandwidth is calculated as follows:<br>Actual bandwidth = cr_bw_coef x 2^cr_bw_exp |

## CR_CN

CR_CN is a CN ratio register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5A | CR_CN | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_cn | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cr_cn | CN ratio. The maximum value is 255. The LSB indicates 0.1875 dB. |

## CR_STATE

CR_STATE is a carrier status register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5B | CR_STATE | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | cr_ok | scan_ok | sync_ok |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |
| [2] | RO | cr_ok | CR completion. |
| [1] | RO | scan_ok | Carrier frequency scanning completion. |
| [0] | RO | sync_ok | Frame synchronization completion. |

## PLS_CODE

PLS_CODE is a PLS_CODE register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5C | PLS_CODE | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | pls_code | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:0] | RO | pls_code | PLS_CODE in DVB-S2 mode. The upper five bits indicate the MODCOD and the lower two bits indicate the type. |

## FREQ_INV

FREQ_INV is a spectrum reversion register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5D | FREQ_INV | 0x02 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | | freq_inverse |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:1] | - | reserved | Reserved. |
| [0] | RO | freq_inverse | Spectrum invert. This field is valid only in DVB-S2 mode. |

## CR_ZUNI_BW_L

CR_ZUNI_BW_L is a carrier bandwidth low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5E | CR_ZUNI_BW_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_zuni_bw_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cr_zuni_bw_l | Lower eight bits of the 13-bit product of the damping value and the bandwidth. |

## CR_ZUNI_BW_H

CR_ZUNI_BW_H is a carrier bandwidth high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5F | CR_ZUNI_BW_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | cr_zuni_bw_h | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:0] | RO | cr_zuni_bw_h | Upper five bits of the 13-bit product of the damping value and the bandwidth. |

## SYNC_FREQ_L

SYNC_FREQ_L is a frame synchronization frequency low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x60 | SYNC_FREQ_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | sync_freq_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | sync_freq_l | Lower eight bits of the 12-bit estimated frame synchronization frequency. The LSB is (2^−12 x fs). |

## SYNC_FREQ_H

SYNC_FREQ_H is a frame synchronization frequency high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x61 | SYNC_FREQ_H | 0x80 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | sync_freq_h | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:0] | RO | sync_freq_h | Upper four bits of the 12-bit estimated frame synchronization frequency. The LSB is (2^−4 x fs). |

## SCAN_FREQ_L

SCAN_FREQ_L is a scanning frequency low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x62 | SCAN_FREQ_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | scan_freq_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | scan_freq_l | Lower eight bits of the 16-bit scanning frequency. The LSB is (2^−16 x fs). |

## SCAN_FREQ_H

SCAN_FREQ_H is a scanning frequency high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x63 | SCAN_FREQ_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | scan_freq_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | scan_freq_h | Upper eight bits of the 16-bit scanning frequency. The LSB is (2^−8 x fs). |

## FREQ_ACC_L

FREQ_ACC_L is a carrier frequency offset slow feedback low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x64 | FREQ_ACC_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | freq_acc_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | freq_acc_l | Lower eight bits of the 16-bit carrier frequency offset slow feedback. The LSB is (2^−16 x fs). |

## FREQ_ACC_H

FREQ_ACC_H is a carrier frequency offset slow feedback high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x65 | FREQ_ACC_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | freq_acc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | freq_acc_h | Upper eight bits of the 16-bit carrier frequency offset slow feedback. The LSB is (2^−8 x fs). |

## TR_FREQ_FB_L

TR_FREQ_FB_L is a carrier frequency offset TR feedback low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x66 | TR_FREQ_FB_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tr_freq_fb_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | tr_freq_fb_l | Lower eight bits of the 16-bit carrier frequency offset TR feedback. The LSB is (2^−16 x fs). |

## TR_FREQ_FB_H

TR_FREQ_FB_H is a carrier frequency offset TR feedback high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x67 | TR_FREQ_FB_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tr_freq_fb_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | tr_freq_fb_h | Upper eight bits of the 16-bit carrier frequency offset TR feedback. The LSB is (2^−8 x fs). |

## CR_LOOP_DC_L

CR_LOOP_DC_L is a carrier PLL control word low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x68 | CR_LOOP_DC_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_loop_dc_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cr_loop_dc_l | Lower eight bits of the 16-bit carrier PLL control word. The LSB is (2^−20 x fs). |

## CR_LOOP_DC_H

CR_LOOP_DC_H is a carrier PLL control word high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x69 | CR_LOOP_DC_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cr_loop_dc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cr_loop_dc_h | Upper eight bits of the 16-bit carrier PLL control word. The LSB is (2^−12 x fs). |

## CHIP_ID_0

CHIP_ID_0 is chip ID register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6C | CHIP_ID_0 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | chip_id_0 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | chip_id_0 | Lowest eight bits of the 32-bit chip ID. |

## CHIP_ID_1

CHIP_ID_1 is chip ID register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6D | CHIP_ID_1 | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | chip_id_1 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | chip_id_1 | Lower eight bits of the 32-bit chip ID. |

## CHIP_ID_2

CHIP_ID_2 is chip ID register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6E | CHIP_ID_2 | 0x36 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | chip_id_2 | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | chip_id_2 | Upper eight bits of the 32-bit chip ID. |

## CHIP_ID_3

CHIP_ID_3 is chip ID register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6F | CHIP_ID_3 | 0x31 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | chip_id_3 | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | chip_id_3 | Uppermost eight bits of the 32-bit chip ID. |

## EQU_CTRL

EQU_CTRL is an equalization control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x70 | EQU_CTRL | 0x06 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | equ_hold | equ_bypass | reserved | | | blind_step | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | equ_hold | Current equalizer factor hold.<br>1: hold<br>0: not hold |
| [6] | RW | equ_bypass | Equalizer operation bypass.<br>1: bypass<br>0: not bypass |

| | | | |
|---|---|---|---|
| [5:3] | - | reserved | Reserved. |
| [2:0] | RW | blind_step | Blind equalization step. Each time the value is added by 1, the step is multiplied by 2. |

## LMS_STEP

LMS_STEP is an equalization step control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x71 | LMS_STEP | 0x02 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | lms_step_4_8 | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |
| [2:0] | RW | lms_step_4_8 | LMS equalization step in QPSK or 8PSK mode. Each time the value is added by 1, the step is multiplied by 2. |

## CN_CTRL

CN_CTRL is a noise power statistics control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x75 | CN_CTRL | 0x48 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | bypass_cnr_est | noise_sta | | reserved | | |
| Reset | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5] | RW | bypass_cnr_est | CNR estimation module bypass.<br>1: bypass<br>0: not bypass |
| [4:3] | RW | noise_sta | Average times for noise power statistics.<br>00: 64<br>01: 128<br>10: 256<br>11: 512 |

| | | | |
|---|---|---|---|
| [2:0] | - | reserved | Reserved. |

## EQU_TAP_REAL

EQU_TAP_REAL is an equalization tap real part register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x76 | EQU_TAP_REAL | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | equ_tap_real | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | equ_tap_real | Real part to be written to tap *N* or to be read from tap *N*. The read or write operation depends on the RD_WR_TAP register. |

## EQU_TAP_IMAG

EQU_TAP_IMAG is an equalization tap imaginary part register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x77 | EQU_TAP_IMAG | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | equ_tap_imag | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | equ_tap_imag | Imaginary part to be written to tap *N* or to be read from tap *N*. The read or write operation depends on the RD_WR_TAP register. |

## EQU_TAP_SEL

EQU_TAP_SEL is a tap select register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x78 | EQU_TAP_SEL | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | equ_tap_sel | | | | | | reserved | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | RW | equ_tap_sel | Selected tap *N* to be read or written. The value is an unsigned number. If the value is greater than the actual tap number, the last tap is selected. |
| [1:0] | - | reserved | Reserved. |

## XREG_INIT_LOW

XREG_INIT_LOW is an equalization control low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7A | XREG_INIT_LOW | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | xreg_init_low | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | xreg_init_low | Lower eight bits of xreg_init. |

## XREG_INIT_MID

XREG_INIT_MID is an equalization control middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7B | XREG_INIT_MID | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | xreg_init_mid | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | xreg_init_mid | Middle eight bits of xreg_init. |

## XREG_INIT_HI

XREG_INIT_HI is an equalization control high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7C | XREG_INIT_HI | 0x60 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | ffe_step | | | xreg_init_hi | |
| Reset | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:2] | RW | ffe_step | Step of the feed forward equalizer (FFE) tap. The value 0 indicates that the FFE tap step is the same as the feedback equalizer (FBE) tap step. Each time the field value is added by 1, the FFE tap is half of the FBE tap step. |
| [1:0] | RW | xreg_init_hi | Upper two bits of xreg_init. |

## RD_WR_TAP

RD_WR_TAP is a tap control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7D | RD_WR_TAP | 0x82 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | rd_wr_tap | reserved | lms_step_16_32 | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4] | RW | rd_wr_tap | Equalizer tap read/write control.<br>0: Tap *N* is read and the read value is stored in the registers whose offset addresses are 0x76 and 0x77. The value *N* is specified by the EQU_TAP_SEL register.<br>1: The values of the registers whose offset addresses are 0x76 and 0x77 are written to tap *N*. The value *N* is specified by the EQU_TAP_SEL register. |
| [3] | - | reserved | Reserved. |
| [2:0] | RW | lms_step_16_32 | LMS equalization step in 16APSK or 32APSK mode. Each time the value is added by 1, the step is multiplied by 2. |

## NOISE_POW_L

NOISE_POW_L is a noise power low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7E | NOISE_POW_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | noise_pow_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | noise_pow_l | Lower eight bits of the output value for noise power statistics. |

## NOISE_POW_H

NOISE_POW_H is a noise power high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7F | NOISE_POW_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cnr_est_ok | noise_pow_h | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | cnr_est_ok | CNR estimation completion. |
| [6:0] | RO | noise_pow_h | Upper seven bits of the output value for noise power statistics. |

## LDPC_ITER

LDPC_ITER is an LDPC iteration control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x82 | LDPC_ITER | 0x50 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fix_iter | iter_num_man | iter_num | | | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | fix_iter | Fixed or selected maximum iteration times.<br>1: fixed maximum iteration times<br>0: automatically selected maximum iteration times |
| [6] | RW | iter_num_man | Manually or automatically configured maximum iteration times.<br>1: manually<br>0: automatically |
| [5:0] | RW | iter_num | Manually configured maximum iteration times. |

## BER_CTRL

BER_CTRL is a BER control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x83 | BER_CTRL | 0xB5 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | stop_sel | frame_num | | | rst_frm_num | | rst_err_num | |
| Reset | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | stop_sel | Iteration check stop.<br>1: Automatic iteration check stops.<br>0: Iteration stops when the maximum iteration times is reached. |
| [6:4] | RW | frame_num | BER statistics period. |
| [3:2] | RW | rst_frm_num | Total frame count for auto reset statistics. |
| [1:0] | RW | rst_err_num | Percentage of correct frames during auto reset. A greater percentage indicates a higher ratio of correct frames to total frames. |

## FEC_BER_L

FEC_BER_L is a BER low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x84 | FEC_BER_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fec_ber_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | fec_ber_l | Lower eight bits of BER statistics. |

## FEC_BER_H

FEC_BER_H is a BER high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x85 | FEC_BER_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fec_ber_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | fec_ber_h | Upper eight bits of BER statistics. |

## FEC_FER_L

FEC_FER_L is an FER low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x86 | FEC_FER_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fec_fer_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | fec_fer_l | Lower eight bits of the error frame count. |

## FEC_FER_H

FEC_FER_H is an FER high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x87 | FEC_FER_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fec_fer_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | fec_fer_h | Upper eight bits of the error frame count. |

## S2_SUCCESS

S2_SUCCESS is an S2 decoding success register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x88 | S2_SUCCESS | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | iter_num | | | | | | bch_cancorr | ldpc_badly |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | RO | iter_num | Half of the actual LDPC decoding iteration times. |
| [1] | RO | bch_cancorr | BCH decoding success.<br>1: success<br>0: failure |
| [0] | RO | ldpc_badly | LDPC decoding badly.<br>1: failure<br>0: success |

## VTB_CTRL1

VTB_CTRL1 is a VTB control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x89 | VTB_CTRL1 | 0x08 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | iq_swap_mod | iq_swap_man | vtb_search_mod | vtb_search_per | | vtb_rate_man | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | iq_swap_mod | I/Q inversion search mode.<br>1: manual mode<br>0: automatic mode |
| [6] | RW | iq_swap_man | I/O manual inversion indicator.<br>1: inverted<br>0: not inverted |
| [5] | RW | vtb_search_mod | VTB code rate search mode.<br>1: manual mode<br>0: automatic mode |
| [4:3] | RW | vtb_search_per | VTB search period. |
| [2:0] | RW | vtb_rate_man | VTB cod rate manually searched.<br>000: 1/2<br>001: 2/3<br>010: 3/4<br>011: 5/6<br>100: 7/8<br>101: 6/7<br>Other values: reserved |

## VTB_THRES

VTB_THRES is a VTB search control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x8A | VTB_THRES | 0x22 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | vtb_lock_th | | | | vtb_loss_th | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | vtb_lock_th | VTB search lock threshold. |

| | | | |
|---|---|---|---|
| [3:0] | RW | vtb_loss_th | VTB search lock loss threshold. |

## VTB_CTRL2

VTB_CTRL2 is a VTB control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x8B | VTB_CTRL2 | 0x38 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | vtb_tout_th | | | | vtb_lock_mod | vtb_adjust_man | vtb_adjust | |
| Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | vtb_tout_th | VTB search timeout threshold. |
| [3] | RW | vtb_lock_mod | VTB search lock mode.<br>1: Lock loss is not checked after the VTB code rate is locked.<br>0: Lock loss is checked after the VTB code rate is locked. |
| [2] | RW | vtb_adjust_man | Strength adjustment mode of VTB inputs.<br>1: The input signal strength is manually adjusted.<br>0: The strength is automatically adjusted based on the code rate. |
| [1:0] | RW | vtb_adjust | Manual adjustment strength for VTB inputs. The vtb_adjust field is valid when vtb_adjust_man is 1. The greater the value of the vtb_adjust field is, the greater the adjusted signal strength is. |

## FS_CTRL1

FS_CTRL1 is S frame synchronization control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x8C | FS_CTRL1 | 0xA9 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_corr_en | fs_lock_th | | fs_loss_th | | fs_search_mod | fs_direc_man | rs_corr_en |
| Reset | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | fs_corr_en | FS frame header correction enable.<br>1: enabled<br>0: disabled |

| | | | |
|---|---|---|---|
| [6:5] | RW | fs_lock_th | FS lock threshold. |
| [4:3] | RW | fs_loss_th | FS lock loss threshold. |
| [2] | RW | fs_search_mod | FS search mode.<br>1: manual mode<br>0: automatic mode |
| [1] | RW | fs_direc_man | Mode search indicator.<br>1: Searching the DirecTV mode is manually configured.<br>0: Searching the DVB-S mode is manually configured. |
| [0] | RW | rs_corr_en | RS correction enable.<br>1: enabled<br>0: disabled |

## FS_CTRL2

FS_CTRL2 is S frame synchronization control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x8D | FS_CTRL2 | 0x5A |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_sear_th | | fs_modtrans_th | | fs_tout_th | | ber_en | ber_clear |
| Reset | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | RW | fs_sear_th | Times threshold for FS search by mode. |
| [5:4] | RW | fs_modtrans_th | Frame count threshold for FS search for a mode. |
| [3:2] | RW | fs_tout_th | FS search timeout threshold. |
| [1] | RW | ber_en | BER statistics enable.<br>1: enabled<br>0: disabled |
| [0] | RW | ber_clear | BER statistics clear.<br>1: cleared<br>0: not cleared |

## SEAR_RESULT

SEAR_RESULT is an S search result register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x8E | SEAR_RESULT | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | vtb_rate | | | ir_directv |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:1] | RO | vtb_rate | Searched VTB code rate.<br>000: 1/2<br>001: 2/3<br>010: 3/4<br>011: 5/6<br>100: 7/8<br>101: 6/7<br>Other values: reserved |
| [0] | RO | ir_directv | DirecTV mode indicator.<br>1: DirecTV mode<br>0: DVB-S mode |

## DEC_RESULT

DEC_RESULT is an S decoding result register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x8F | DEC_RESULT | 0x41 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rst_vcm_err_num | | vtb_tout | fs_tout | vtb_lock | iq_swap | fs_lock | rs_cancorr |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | RW | rst_vcm_err_num | Percentage of correct frames during auto reset in VCM mode. A larger percentage indicates a higher correct rate. |
| [5] | RO | vtb_tout | VTB search timeout indicator.<br>1: Time is out.<br>0: Time is not out. |
| [4] | RO | fs_tout | FS search timeout indicator.<br>1: Time is out.<br>0: Time is not out. |

| | | | |
|---|---|---|---|
| [3] | RO | vtb_lock | VTB search lock.<br>1: locked<br>0: unlocked |
| [2] | RO | iq_swap | I/Q inversion indicator.<br>1: inverted<br>0: not inverted |
| [1] | RO | fs_lock | FS search lock.<br>1: locked<br>0: unlocked |
| [0] | RO | rs_cancorr | RS decoding error indicator.<br>1: error<br>0: success |

## TS_PARALL_CTRL

TS_PARALL_CTRL is a TS output select register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x90 | TS_PARALL_CTRL | 0x6A |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | c_isi_research | reserved | ts_parall | ts_serial2 | ts_a_sel | | | |
| Reset | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | c_isi_research | Stream ID search again enable.<br>1: enabled (automatically cleared)<br>0: disabled |
| [6] | - | reserved | Reserved. |
| [5] | RW | ts_parall | TS parallel output mode select.<br>1: parallel mode<br>0: serial mode |
| [4] | RW | ts_serial2 | 2-bit TS output.<br>1: 2-bit TS output (ts_parall must be set to 1)<br>0: parallel mode or serial mode, which depends on the value of the ts_parall field |
| [3:0] | RW | ts_a_sel | TS_ERR pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |

## TS_10_SEL

TS_10_SEL is a TS output control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x91 | TS_10_SEL | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_1_sel | | | | ts_0_sel | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | ts_1_sel | TS_OUT1 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |
| [3:0] | RW | ts_0_sel | TS_OUT0 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |

## TS_32_SEL

TS_32_SEL is a TS output control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x92 | TS_32_SEL | 0x32 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_3_sel | | | | ts_2_sel | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | ts_3_sel | TS_OUT3 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |
| [3:0] | RW | ts_2_sel | TS_OUT2 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |

## TS_54_SEL

TS_54_SEL is a TS output control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x93 | TS_54_SEL | 0x54 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_5_sel | | | | ts_4_sel | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | ts_5_sel | TS_OUT5 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |
| [3:0] | RW | ts_4_sel | TS_OUT4 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |

## TS_76_SEL

TS_76_SEL is a TS output control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x94 | TS_76_SEL | 0x76 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_7_sel | | | | ts_6_sel | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | ts_7_sel | TS_OUT7 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |
| [3:0] | RW | ts_6_sel | TS_OUT6 pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |

## TS_98_SEL

TS_98_SEL is a TS output control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x95 | TS_98_SEL | 0x98 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_9_sel | | | | ts_8_sel | | | |
| Reset | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | ts_9_sel | TS_VLD pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |
| [3:0] | RW | ts_8_sel | TS_SYNC pin output control. The bits in {ts_err, ts_vld, ts_sync, ts_out[7:0]} are selected for signal output. |

## TS_CTRL0

TS_CTRL0 is TS control register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x96 | TS_CTRL0 | 0x92 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pcr_change | pcr_local_chg | ts_lsb_first | serial_sync8 | mask_ts_clk | ts_on_bf_ok | ts_clk_on | ts_clk_inv |
| Reset | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | pcr_change | PCR modification enable.<br>1: enabled<br>0: disabled |
| [6] | RW | pcr_local_chg | Whether to use the local counter to update the PCR.<br>1: The value of the local counter is used as the updated PCR value.<br>0: The result calculated by using ISCR is used as the updated PCR value. |
| [5] | RW | ts_lsb_first | TS serial output sequence.<br>1: from 0 to 7<br>0: from 7 to 0 |
| [4] | RW | serial_sync8 | Number of output TS serial frame headers during synchronization.<br>1: 8<br>0: 1 |
| [3] | RW | mask_ts_clk | TS parallel clock mask.<br>1: The parallel clock is output only when ts_vld is valid.<br>0: The parallel clock is always output. |

| | | | |
|---|---|---|---|
| [2] | RW | ts_on_bf_ok | TS output control.<br>1: TSs are output before the system is ready.<br>0: TSs are output only after the system is ready. |
| [1] | RW | ts_clk_on | TS output enable.<br>1: enabled<br>0: disabled |
| [0] | RW | ts_clk_inv | TS clock control.<br>1: The TS parallel clock is output after being inverted.<br>0: The TS parallel output is directly output. |

## TS_CTRL3

TS_CTRL3 is TS control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x97 | TS_CTRL3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | is_ccm | matype_addr | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | is_ccm | Current mode.<br>1: CCM mode<br>0: VCM or ACM mode |
| [6:0] | RW | matype_addr | Register address for storing ISI stream information. Read MATTYPE[matype_out] to obtain the configured address and stream information.<br>matype_addr[4:0] is used to select streams.<br>When matype_addr[6:5]==2'b00, the output of MATTYPE[matype_out] is the stream ID.<br>When matype_addr[6:5]==2'b01, the output of MATTYPE[matype_out] is matype1 corresponding to the stream ID.<br>When matype_addr[6:5]==2'b1x, the output of MATTYPE[matype_out] is tmodcod corresponding to the stream ID. |

## TS_CTRL4

TS_CTRL4 is TS control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x98 | TS_CTRL4 | 0xCA |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | isi_sel_vld | clk_auto | ts_clk_div | | | | | |
| Reset | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | isi_sel_vld | TS output selected by specifying the stream ID.<br>1: The output stream is the one specified by isi_sel.<br>0: The output stream is the first stream found. |
| [6] | RW | clk_auto | Automatic generating of the TS clock.<br>1: If there is only one stream in CCM mode, an even TS clock is generated based on the stream rate.<br>0: A fixed clock frequency is generated by using ts_clk_div. |
| [5:0] | RW | ts_clk_div | TS parallel clock that is obtained by dividing the system clock.<br>The frequency divider is calculated as follows: Frequency divider = {ts_clk_div[5:0], ts_clk_div_f[15:0]}/2^16<br>The value of the ts_clk_div field ranges from 8 to 31. |

## TS_CLK_DIV_F_L

TS_CLK_DIV_F_L is a TS clock low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x99 | TS_CLK_DIV_F_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_clk_div_f_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ts_clk_div_f_l | ts_clk_f[7:0]. Lower bits of the decimal part of the TS parallel clock obtained by dividing the system clock. |

## TS_CLK_DIV_F_H

TS_CLK_DIV_F_H is a TS clock high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9A | TS_CLK_DIV_F_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ts_clk_div_f_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ts_clk_div_f_h | ts_clk_f[7:0]. Upper bits of the decimal part of the TS parallel clock obtained by dividing the system clock. |

## ISI_SEL

ISI_SEL is an ISI select register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9B | ISI_SEL | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | isi_sel | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | isi_sel | TS output select when TS_CTRL4[isi_sel_vld] is 1. |

## MATTYPE

MATTYPE is a stream ID register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9C | MATTYPE | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | matype_out | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | matype_out | ISI stream ID output. |

## ROLL_OFF

ROLL_OFF is a roll-off register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9D | ROLL_OFF | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | roll_off | | isi_num | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | RO | roll_off | Roll-off factor.<br>00: 0.35<br>01: 0.25<br>10: 0.20<br>11: reserved |
| [5:0] | RO | isi_num | Number of searched ISI streams. |

## CRC_ERR

CRC_ERR is a CRC check register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9E | CRC_ERR | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | crc_err | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | crc_err | The actual PER is calculated as follows:<br>Actual PER = crc_err/1024 x 100%<br>This field is valid only for S2 signals. When the value of crc_err is less than 1 but is not 0, the field value is 1. When the value of crc_err is greater than 255, the field value is 255. |

## RST_WAIT

RST_WAIT is a reset wait register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9F | RST_WAIT | 0x15 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | crc_pkt_cnt | | | | rst_wait | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | crc_pkt_cnt | Packet count for PER statistics. The actual packet count is crc_pkt_cnt x 1024. When crc_pkt_cnt is 0, the actual packet count is 1024. |
| [3:0] | RW | rst_wait | Reset wait.<br>When CLK_CNT[28:25] == rst_wait, a TS reset signal is generated. CLK_CNT is a counter that uses the FEC clock. CLK_CNT counts when the interface is abnormal. |

## FC_MAX_RELIABLE

FC_MAX_RELIABLE is a blind scanning carrier control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA0 | FC_MAX_RELIABLE | 0xB4 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fc_dlt_sel | | reserved | | | cbs_reliable | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | RW | fc_dlt_sel | Maximum error for blind scanning. When the field value is 0, the error is 3.072 MHz. When the field value is added by 1, the error increases by 1.024 MHz. |
| [5:3] | - | reserved | Reserved. |
| [2:0] | RW | cbs_reliable | A larger value indicates more reliable blind scanning and longer scanning time. |

## FS_SPAN

FS_SPAN is a blind scanning symbol rate range register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA1 | FS_SPAN | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | fs_span | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |
| [2:0] | RW | fs_span | Symbol rate search range when the fs is specified. The value 0 indicates 2^–9 x fs. When the field value is added by 1, the range is doubled. |

## AMP_MIN_FS

AMP_MIN_FS is a blind scanning minimum symbol rate register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA7 | AMP_MIN_FS | 0x67 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | min_fs | | | | |
| Reset | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:0] | RW | min_fs | Minimum symbol rate for blind scanning. The LSB indicates 128 kHz. |

## CBS_CTRL_RDADDR

CBS_CTRL_RDADDR is a blind scanning control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA8 | CBS_CTRL_RDADDR | 0x80 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | use_cbs | know_fs_fc | reserved | cbs_rd_addr | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | use_cbs | Blind scanning enable.<br>1: enabled<br>0: disabled |
| [6] | RW | know_fs_fc | Blind scanning mode.<br>1: known fs (symbol rate) and fc (baseband carrier frequency)<br>0: unknown fs and fc |
| [5] | - | reserved | Reserved. |
| [4:0] | RW | cbs_rd_addr | Address for reading blind scanning results.<br>Multiple results are obtained for each blind scanning and stored in the RAM. Each result has the fs, fc, and reliability information (corresponding to some registers whose offset addresses range from 0xA9 to 0xAF). |

## CBS_FS_L

CBS_FS_L is a blind scanning symbol rate low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA9 | CBS_FS_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cbs_fs_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cbs_fs_l | Lower eight bits of the symbol rate obtained after blind scanning. The LSB indicates 1 kHz. |

## CBS_FS_H

CBS_FS_H is a blind scanning symbol rate high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAA | CBS_FS_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cbs_fs_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cbs_fs_h | Upper eight bits of the symbol rate obtained after blind scanning. The symbol rate is an unsigned number. |

## CBS_FC_L

CBS_FC_L is a blind scanning frequency offset low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAB | CBS_FC_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cbs_fc_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cbs_fc_l | Lower eight bits of the carrier frequency offset obtained after blind scanning. The LSB indicates 1 kHz. |

## CBS_FC_H

CBS_FC_H is a blind scanning frequency offset high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAC | CBS_FC_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cbs_fc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cbs_fc_h | Upper eight bits of the carrier frequency offset obtained after blind scanning. The frequency offset is a signed number. |

## CBS_FINISH

CBS_FINISH is a blind scanning completion register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAD | CBS_FINISH | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | | cbs_finish |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:1] | - | reserved | Reserved. |
| [0] | RO | cbs_finish | Blind scanning completion.<br>1: complete<br>0: not complete |

## CBS_RELIABILITY1

CBS_RELIABILITY1 is a blind scanning reliability register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAE | CBS_RELIABILITY1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | cbs_reliability1 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | cbs_reliability1 | Blind scanning result reliability 1. A larger value indicates more reliable. |

## CBS_R2_NUM

CBS_R2_NUM is a blind scanning signal count register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAF | CBS_R2_NUM | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reliability2 | | | sig_num | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RO | reliability2 | Blind scanning result reliability 2. A larger value indicates more reliable. |
| [4:0] | RO | sig_num | Number of valid signals for current blind scanning. |

## DSEC_ADDR

DSEC_ADDR is a DSEC address register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB0 | DSEC_ADDR | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dsec_addr | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | dsec_addr | When dsec_addr[7] is 1, the current operation is a read operation. When dsec_addr[3] is 0, dsec_addr[2:0] specifies the address for storing the data to be transmitted.<br>When dsec_addr[3] is 1, dsec_addr[2:0] specifies the address for storing the data to be received.<br>When dsec_addr[7] is 0, the current operation is a write operation. When dsec_addr[3] is 0, dsec_addr[2:0] specifies the address for storing the data to be transmitted.<br>When dsec_addr[3] is 1, the address specified by dsec_addr[2:0] is invalid. |

## DSEC_DATA

DSEC_DATA is a DSEC data register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB1 | DSEC_DATA | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dsec_data | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | dsec_data | Transmit data or read the received data.<br>For details, see section 2.18 "TX."<br>If bit[1] in the first byte of the message to be transmitted is 1, the state machine in the DiSEqc automatically enters the RX state after transmission is complete.<br>For details, see section 2.18 "RX." |

## DSEC_RATIO_L

DSEC_RATIO_L is a DSEC frequency low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB2 | DSEC_RATIO_L | 0x88 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dsec_ratio_l | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | dsec_ratio_l | Lower bits of the system clock frequency divider for generating a 22 kHz square wave. diseqc_ratio = fsys/22. The unit of fsys is kHz. |

## DSEC_RATIO_H

DSEC_RATIO_H is a DSEC frequency high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB3 | DSEC_RATIO_H | 0x13 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dsec_ratio_h | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | dsec_ratio_h | Upper bits of the system clock frequency divider for generating a 22 kHz square wave. |

## TX_CTRL1

TX_CTRL1 is a DSEC TX control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB4 | TX_CTRL1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | num_byte | | | dsec_mode | | | hv_sel |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:4] | RW | num_byte | Number of bytes of the message to be transmitted. The actual value is the configured value plus 1. |
| [3:1] | RW | dsec_mode | DiSEqC working mode.<br>000: The DiSEqC is idle.<br>001: Consecutive 22 kHz square waves are transmitted.<br>010: A 0 tone burst is transmitted.<br>011: A 1 data burst is transmitted.<br>100: A complete DiSEqC message is transmitted.<br>Other values: reserved |
| [0] | RW | hv_sel | Horizontal/Vertical polarization direction.<br>1: output high level<br>0: output low level |

## RX_CTRL1

RX_CTRL1 is a DSEC RX control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB5 | RX_CTRL1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | tone_cofig | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | - | reserved | Reserved. |
| [1:0] | RW | tone_cofig | Period deviation for the 22 kHz square waves (44 μs) in the diseqc_in signal.<br>00: 33−60 μs<br>01: 30−60 μs<br>10: 33−66 μs<br>11: 30−66 μs |

## DSEC_EN

DSEC_EN is a DSEC enable register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB7 | DSEC_EN | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | dsec_en | reserved | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | dsec_en | LNB enable.<br>1: enabled<br>0: disabled |
| [6:0] | - | reserved | Reserved. |

## RX_STATE

RX_STATE is a DSEC RX status register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB8 | RX_STATE | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rx_silent_time | | | | rx_recv_bytes | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RO | rx_silent_time | The low level hold time for the DiSEqC input is (rx_silent_time x 16) ms. |
| [3:0] | RO | rx_recv_bytes | Number of bytes to be received. The actual value is the configured value plus 1. |

## INT_STATE

INT_STATE is a DSEC status register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB9 | INT_STATE | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | rx_err_else | rx_err_silent | rx_err_overflow | rx_err_par | rx_message | rx_byte | reserved |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6] | RO | rx_err_else | Bit error or byte error (the received message length in bit is not an integral multiple of 8). |
| [5] | RO | rx_err_silent | Indicator showing that the low level hold time for the DiSEqC input is longer than 192 ms. |
| [4] | RO | rx_err_overflow | Indicator showing that the received data length is greater than 8 bytes. |
| [3] | RO | rx_err_par | Parity error indicator. |
| [2] | RO | rx_message | Message RX completion indicator |
| [1] | RO | rx_byte | Byte RX completion indicator |
| [0] | - | reserved | Reserved. |

## DF_FC_L

DF_FC_L is an FSK frequency offset low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC0 | DF_FC_L | 0x0C |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | df_fc_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | df_fc_l | Lower bits of the FSK modulation frequency offset normalized to the system clock. The actual normalized offset is df_fc/2^21. |

## DF_FC_H

DF_FC_H is an FSK frequency offset high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC1 | DF_FC_H | 0x03 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | df_fc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | df_fc_h | Upper bits of the FSK modulation frequency offset normalized to the system clock. |

## FS_FC_L

FS_FC_L is an FSK symbol rate low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC2 | FS_FC_L | 0x45 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_fc_l | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fs_fc_l | Lower bits of the FSK symbol rate normalized to the system clock. The actual normalized symbol rate is df_fc/2^27. |

## FS_FC_M

FS_FC_M is an FSK symbol rate middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC3 | FS_FC_M | 0x23 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fs_fc_m | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fs_fc_m | Middle bits of the FSK symbol rate normalized to the system clock. |

## FS_FC_H

FS_FC_H is an FSK symbol rate high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC4 | FS_FC_H | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | fs_fc_h | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:0] | RW | fs_fc_h | Upper bits of the FSK symbol rate normalized to the system clock. |

## HEAD_L

HEAD_L is a frame header low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC5 | HEAD_L | 0x0D |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | head_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | head_l | Lower bits of the configured frame header content. |

## HEAD_M

HEAD_M is a frame header middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC6 | HEAD_M | 0x55 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | head_m | | | | | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | head_m | Middle bits of the configured frame header content. |

## HEAD_H

HEAD_H is a frame header high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC7 | HEAD_H | 0x55 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | head_h | | | | | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | head_h | Upper bits of the configured frame header content. |

## NBIT_HEAD

NBIT_HEAD is an FSK control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC8 | NBIT_HEAD | 0x18 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | nbit_head | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [4:0] | RW | nbit_head | Valid bits of the specified header. head[nbit_head − 1:0] is transmitted. |

## CRC_POLY_L

CRC_POLY_L is a CRC low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xC9 | CRC_POLY_L | 0x11 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | crc_poly_l | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | crc_poly_l | Low bits of a specified polynomial for obtaining the CRC result. The LCB corresponds to X^1. |

## CRC_POLY_M

CRC_POLY_M is a CRC middle register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xCA | CRC_POLY_M | 0x89 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | crc_poly_m | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | crc_poly_m | Middle bits of a specified polynomial for obtaining the CRC result. |

## CRC_POLY_H

CRC_POLY_H is a CRC high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xCB | CRC_POLY_H | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | crc_poly_h | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | crc_poly_h | Upper bits of a specified polynomial for obtaining the CRC result. |

## NBIT_CRC

NBIT_CRC is a CRC control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xCC | NBIT_CRC | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | nbit_crc | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:0] | RW | nbit_crc | Valid bits of a specified polynomial for obtaining the CRC result. crc_poly[nbit_crc − 1:0] is used to generate CRC check bits. |

## TCF_FC_L

TCF_FC_L is a TX frequency low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xCD | TCF_FC_L | 0xB8 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tcf_fc_l | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | tcf_fc_l | Lower bits of the TX center frequency normalized to the system clock. The actual normalized frequency is tcf_fc/2^17. |

## TCF_FC_H

TCF_FC_H is a TX frequency high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xCE | TCF_FC_H | 0x1E |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tcf_fc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | tcf_fc_h | Upper bits of the TX center frequency normalized to the system clock. |

## RCF_FC_L

RCF_FC_L is an RX frequency low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xCF | RCF_FC_L | 0xB8 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rcf_fc_l | | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | rcf_fc_l | Lower bits of the RX center frequency normalized to the system clock. The actual normalized frequency is tcf_fc/2^17. |

## RCF_FC_H

RCF_FC_H is an RX frequency high register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD0 | RCF_FC_H | 0x1E |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rcf_fc_h | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | rcf_fc_h | Upper bits of the RX center frequency normalized to the system clock. |

## TX_NBIT_L

TX_NBIT_L is TX control low register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD1 | TX_NBIT_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tx_nbit | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | tx_nbit | Lower bits of the TX bit count provided by users.<br>The bit count ranges from 1 to 256. |

## TX_CTRL2

TX_CTRL2 is a TX control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD2 | TX_CTRL2 | 0x21 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | freq_swap | tx_start | tx_pad | tx_busy | tx_done | reserved | | tx_nbit_h |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | freq_swap | FSK high/low frequency corresponding to the TX/RX bit.<br>1: When the TX/RX bit is 1, the frequency is cf minus df. When the TX/RX bit is 0, the frequency is cf plus df.<br>0: When the TX/RX bit is 1, the frequency is cf plus df. When the TX/RX bit is 0, the frequency is cf minus df. |
| [6] | RW | tx_start | TX start enable.<br>This field is automatically cleared. |
| [5] | RW | tx_pad | Whether to add the frame header and CRC.<br>1: Header is added to the frame header and CRC is added to the frame tail based on the bit sequence provided by users.<br>0: Only the bit sequence provided by users is transmitted. |
| [4] | RO | tx_busy | TX busy indicator. |
| [3] | RO | tx_done | TX completion indicator. |
| [2:1] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [0] | RW | tx_nbit_h | Upper bits of the TX bit count provided by users (excluding the header and CRC). |

## RX_NBIT_L

RX_NBIT_L is an RX control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD3 | RX_NBIT_L | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rx_nbit_l | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | rx_nbit_l | Lower bits of the length of the received FSK frames (excluding the header and CRC). The length unit is bit. |

## RX_CTRL2

RX_CTRL2 is an RX control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD4 | RX_CTRL2 | 0x90 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rx_ena | rx_thresh | | | | rx_done | reserved | rx_nbit_h |
| Reset | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | rx_ena | FSK RX enable.<br>1: enabled<br>0: enabled<br>When this field is 1 and an FSK frame is successfully received, this field is automatically cleared. Set this field to 1 after reading the received data. |
| [6:3] | RW | rx_thresh | Energy threshold for signal detection.<br>The smaller the threshold is, the easier signals are detected. |
| [2] | RO | rx_done | Indicator showing that an FSK packet is successfully received. |
| [1] | - | reserved | Reserved. |
| [0] | RO | rx_nbit_h | Upper bits of the length of the received FSK frames. The length unit is bit. |

## FSK_ADDR

FSK_ADDR is an FSK address register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD5 | FSK_ADDR | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fsk_addr | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fsk_addr | When FSK_ADDR bit[7] is 0, FSK_ADDR bit[4:0] specify the address for storing the data to be transmitted.<br>When FSK_ADDR bit[7] is 1, FSK_ADDR[4:0] specify the address for storing the data to be received. |

## FSK_DATA

FSK_DATA is an FSK data register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD6 | FSK_DATA | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fsk_data | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fsk_data | Transmit data or read the received data.<br>The TX procedure is as follows:<br>Step 1 Write data to FSK_DATA.<br>Step 2 Write a storage address to FSK_ADDR bit[4:0] and set FSK_ADDR bit[7] to 0.<br>Step 3 Repeat step 1 and step 2 until all user data is stored.<br>Step 4 Set head, crc_poly, nbit_head, nbit_crc, freq_swap, tcf_fc, df_fc, fs_fc, tx_pad, and tx_nbit.<br>Step 5 Set TX_CTRL2[tx_start] to 1.<br>Step 6 Wait until TX_CTRL2[tx_done] indicates that transmission is complete.<br>Step 7 Go to step 1 to start the next transmission.<br>----End<br>The RX procedure is as follows:<br>Step 1 Set head, crc_poly, nbit_head, nbit_crc, freq_swap, rcf_fc, df_fc, fs_fc, data1_flen, and flen.<br>Step 2 Set RX_CTRL2[rx_ena] to 1.<br>Step 3 Wait until RX_CTRL2[tx_done] indicates that reception is complete.<br>Step 4 Read rx_nbit to obtain the number of bytes of the received information (excluding the header and CRC). Currently, the value of rx_nbit must be a multiple of 8.<br>Step 5 Write a read address to FSK_ADDR bit[4:0] and set FSK_ADDR bit[7] to 1.<br>Step 6 Read FSK_DATA.<br>Step 7 Repeat step 5 and step 6 until all data is read.<br>----End |

## FSK_RX_LEN

FSK_RX_LEN is an FSK control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xD7 | FSK_RX_LEN | 0x20 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | data1_flen | reserved | flen | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | data1_flen | Whether the received frame includes the frame length field.<br>1: include. The RX end uses the extracted frame length.<br>0: not include. The RX end uses the specified frame length flen. |
| [6] | - | reserved | Reserved. |
| [5:0] | RW | flen | Number of specified RX bytes (excluding the header and CRC1 to CRC32). |

# Contents

# Figures

# Tables

# 3 Hardware

## 3.1 Package and Pins

### 3.1.1 Package and Pinout

#### Package

Hi3136 V100 uses the mapped quad flat non-leaded (MQFN) package. It has 48 pins, its body size is 6 mm x 6 mm (0.24 in. x 0.24 in.), and its ball pitch is 0.4 mm (0.02 in.). Figure 3-1 shows package views. Figure 3-2 shows package dimensions.

**Figure 3-1** Package views

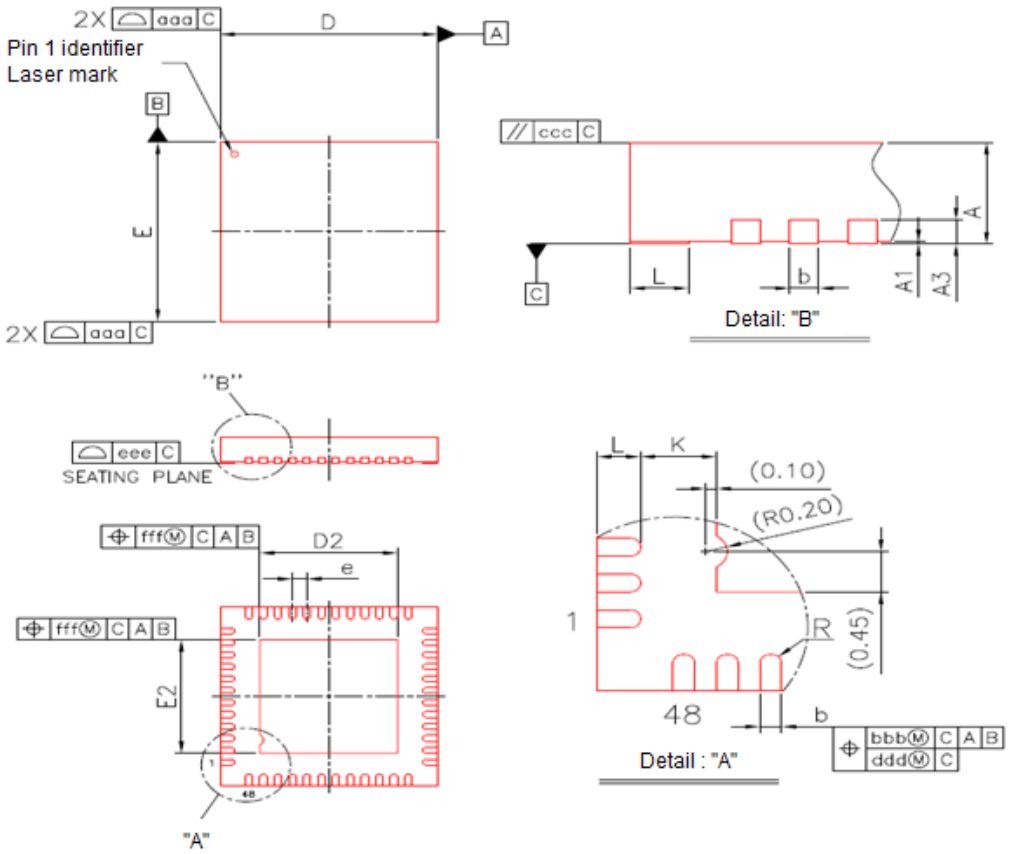


**Figure 3-2** Package dimensions

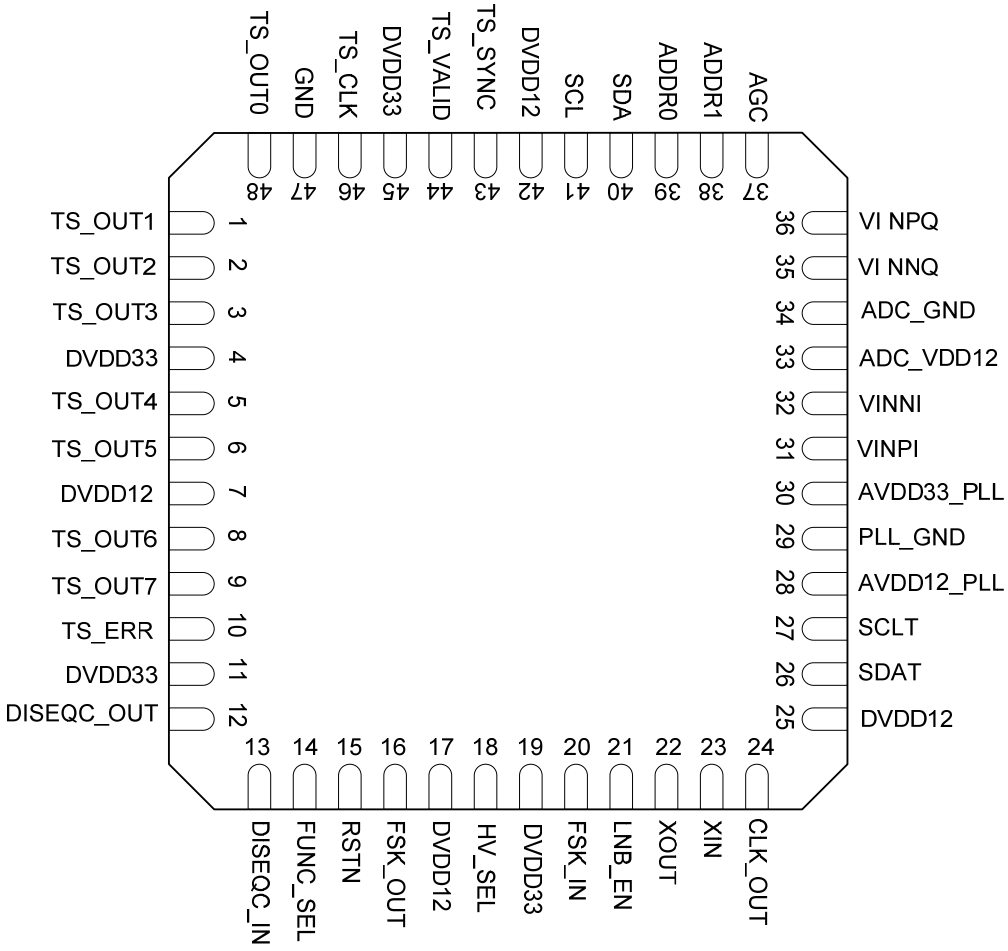
| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| D2/E2 | 3.65 | 3.80 | 3.95 | 0.144 | 0.150 | 0.156 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| K | 0.20 | --- | --- | 0.008 | --- | --- |
| R | 0.075 | --- | --- | 0.003 | --- | --- |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.07 | | | 0.003 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.05 | | | 0.002 | | |
| eee | 0.08 | | | 0.003 | | |
| fff | 0.10 | | | 0.004 | | |

For details, see the JEDEC MO-220 standard.

## Pin Map

Figure 3-3 shows the pin map.

**Figure 3-3** Pin map




## 3.1.2 Pin Descriptions

### Pin Arrangement

Table 3-1 lists the pins of Hi3136 V100 in order.

**Table 3-1** Pin arrangement

| Position | Pin Name | Position | Pin Name |
|---|---|---|---|
| 1 | TS_OUT1 | 25 | DVDD12 |
| 2 | TS_OUT2 | 26 | SDAT |
| 3 | TS_OUT3 | 27 | SCLT |
| 4 | DVDD33 | 28 | AVDD12_PLL |
| 5 | TS_OUT4 | 29 | PLL_GND |

| Position | Pin Name | Position | Pin Name |
|---|---|---|---|
| 6 | TS_OUT5 | 30 | AVDD33_PLL |
| 7 | DVDD12 | 31 | VINPI |
| 8 | TS_OUT6 | 32 | VINNI |
| 9 | TS_OUT7 | 33 | ADC_VDD12 |
| 10 | TS_ERR | 34 | ADC_GND |
| 11 | DVDD33 | 35 | VINNQ |
| 12 | DISEQC_OUT | 36 | VINPQ |
| 13 | DISEQC_IN | 37 | AGC |
| 14 | FUNC_SEL | 38 | ADDR1 |
| 15 | RSTN | 39 | ADDR0 |
| 16 | FSK_OUT | 40 | SDA |
| 17 | DVDD12 | 41 | SCL |
| 18 | HV_SEL | 42 | DVDD12 |
| 19 | DVDD33 | 43 | TS_SYNC |
| 20 | FSK_IN | 44 | TS_VALID |
| 21 | LNB_EN | 45 | DVDD33 |
| 22 | XOUT | 46 | TS_CLK |
| 23 | XIN | 47 | GND |
| 24 | CLK_OUT | 48 | TS_OUT0 |

## Pin Types

Table 3-2 describes the I/O pin types.

**Table 3-2** I/O pin types

| I/O | Description |
|---|---|
| I | Input signal |
| $I_{PD}$ | Input signal, internal pull-down |
| $I_{PU}$ | Input signal, internal pull-up |
| $I_S$ | Input signal with a Schmitt trigger |
| $I_{SPD}$ | Input signal with a Schmitt trigger, internal pull-down |
| $I_{SPU}$ | Input signal with a Schmitt trigger, internal pull-up |

| I/O | Description |
|---|---|
| O | Output signal |
| $O_{OD}$ | Output open drain (OD) |
| I/O | Bidirectional (input/output) signal |
| $I_{PD}$/O | Bidirectional signal, input pull-down |
| $I_{PU}$/O | Bidirectional signal, input pull-up |
| $I_{SPU}$/O | Bidirectional signal with a Schmitt trigger, input pull-up |
| $I_{PD}$/$O_{OD}$ | Bidirectional signal, input pull-down and output OD |
| $I_{PU}$/$O_{OD}$ | Bidirectional signal, input pull-up and output OD |
| $I_S$/O | Bidirectional signal, input with a Schmitt trigger |
| $I_S$/$O_{OD}$ | Bidirectional signal, input with a Schmitt trigger and output OD |
| XIN | Crystal oscillator input |
| XOUT | Crystal oscillator output |
| P | Power supply |
| G | Ground (GND) |

## ADC Pins

Table 3-3 describes ADC pins.

**Table 3-3** ADC pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 34 | ADC_GND | G | None | None | ADC GND. |
| 33 | ADC_VDD12 | P | None | 1.2 | 1.2 V ADC power. |
| 32 | VINNI | I | None | 1.2 | Differential input for channel I. The peak voltage is 1 Vpp in both differential input and single-ended input modes.<br>In single-ended input mode, the pin connects to a 100 nF capacitor and then to GND. |
| 35 | VINNQ | I | None | 1.2 | Differential input for |

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| | | | | | channel Q. The peak voltage is 1 Vpp in both differential input and single-ended input modes.<br>In single-ended input mode, the pin connects to a 100 nF capacitor and then to GND. |
| 31 | VINPI | I | None | 1.2 | Differential input for channel I. The peak voltage is 1 Vpp in both differential input and single-ended input modes. |
| 36 | VINPQ | I | None | 1.2 | Differential input for channel Q. The peak voltage is 1 Vpp in both differential input and single-ended input modes. |

## I²C Pins

Table 3-4 describes $I^2C$ pins.

**Table 3-4** $I^2C$ pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 39 | ADDR0 | I | 4 | 3.3 | Hi3136 device address selection 0. |
| 38 | ADDR1 | I | 4 | 3.3 | Hi3136 device address selection 1. |
| 27 | SCLT | $O_{OD}$ | 4 | 3.3/5 | $I^2C$ bus clock output, OD. This pin is used to control the tuner communication interface. This pin must connect to an external pull-up resistor and then to the 3.3 V or 5 V power. The power voltage depends on the $I^2C$ level of the tuner. |

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 26 | SDAT | $I_S/O_{OD}$ | 4 | 3.3/5 | $I^2C$ bus data output, OD. This pin is used to control the tuner communication interface. This pin must connect to an external pull-up resistor and then to the 3.3 V or 5 V power. The power voltage depends on the $I^2C$ level of the tuner. |
| 41 | SCL | $I_S$ | 4 | 3.3 | Clock input line of the $I^2C$ bus. This pin must connect to an external pull-up resistor and then to the 3.3 V power. |
| 40 | SDA | $I_S/O_{OD}$ | 4 | 3.3 | Data line of the $I^2C$ bus, OD output. This pin must connect to an external pull-up resistor and then to the 3.3 V power. |

## TS Pins

Table 3-5 describes TS pins.

**Table 3-5** TS pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 37 | AGC | $O_{OD}$ | 8 | 3.3/5 | AGC output, OD. This pin is used to control the tuner gain and can connect to a pull-up resistor and then to the 3.3 V or 5 V power. |
| 46 | TS_CLK | O | 8 | 3.3 | TS clock of the Demod output. |
| 48 | TS_OUT0 | O | 8 | 3.3 | Demod data output. |
| 1 | TS_OUT1 | O | 8 | 3.3 | Demod data output. |

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 2 | TS_OUT2 | O | 8 | 3.3 | Demod data output. |
| 3 | TS_OUT3 | O | 8 | 3.3 | Demod data output. |
| 5 | TS_OUT4 | O | 8 | 3.3 | Demod data output. |
| 6 | TS_OUT5 | O | 8 | 3.3 | Demod data output. |
| 8 | TS_OUT6 | O | 8 | 3.3 | Demod data output. |
| 9 | TS_OUT7 | O | 8 | 3.3 | Demod data output. |
| 10 | TS_ERR | O | 8 | 3.3 | TS error indicator. |
| 43 | TS_SYNC | O | 8 | 3.3 | Demod sync signal output. |
| 44 | TS_VALID | O | 8 | 3.3 | Demod output data validity indicator, active high. |

## PLL Pins

Table 3-6 describes PLL pins.

**Table 3-6** PLL pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 28 | AVDD12_PLL | P | None | 1.2 | 1.2 V PLL analog power. |
| 30 | AVDD33_PLL | P | None | 3.3 | 3.3 V PLL analog power. |
| 29 | PLL_GND | G | None | None | PLL analog GND. |

## OSC Pins

Table 3-7 describes oscillator (OSC) pins.

**Table 3-7** OSC pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 24 | CLK_OUT | O | 8 | 3.3 | Slow pass output of the crystal oscillator clock. |
| 23 | XIN | I | None | 3.3 | Crystal oscillator input. |
| 22 | XOUT | O | None | 3.3 | Crystal oscillator output. |

## DiSEqC Pins

Table 3-8 describes DiSEqC pins.

**Table 3-8** DiSEqC pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 13 | DISEQC_IN | $I_S$ | 8 | 3.3 | DiSEqC input. |
| 12 | DISEQC_OUT | O | 8 | 3.3 | DiSEqC output. |
| 21 | LNB_EN | O | 8 | 3.3 | LNB power control enable. |
| 18 | HV_SEL | O | 8 | 3.3 | Antenna horizontal/vertical selection. |

## PG Pins

Table 3-9 describes power/ground (PG) pins.

**Table 3-9** PG pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 4, 11, 19, 45 | DVDD33 | P | None | 3.3 | 3.3 V I/O power. |
| 7, 17, 25, 42 | DVDD12 | P | None | 1.2 | 1.2 V core power. |
| 47 | GND | G | None | None | Digital GND. |

## SYS Pins

Table 3-10 describes system (SYS) pins.

**Table 3-10** SYS pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 14 | FUNC_SEL | $I_{SPD}$ | 4 | 3.3 | Mode selection.<br>0: functional mode<br>1: design for test (DFT) mode |
| 15 | RSTN | $I_{SPU}$ | 4 | 3.3 | System reset signal input, active low. |

## FSK Pins

Table 3-11 describes FSK pins.

**Table 3-11** FSK pins

| Pin Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 20 | FSK_IN | $I_S$ | 4 | 3.3 | FSK input. |
| 16 | FSK_OUT | O | 6 | 3.3 | FSK output. |

# 3.1.3 Multiplexing Control Register

Hi3136 V100 provides the multiplexing control register LOCK_FSKO whose base address is 0x00 and offset address is 0x0C.

## LOCK_FSKO

LOCK_FSKO is the multiplexing control register for the FSKO pin.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0C | LOCK_FSKO | 0x02 |

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | c_lock_fsko | reserved |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [1] | RW | lock_fsko_sel | Pin multiplexing control.<br>0: LOCK<br>1: FSKO |

### 3.1.4 Software Multiplexed Pin

Table 3-12 describes the software multiplexed pin FSK_OUT.

**Table 3-12** Software multiplexed pin FSK_OUT

| Pin Position | Pad Signal | Multiplexing Control Register | Multiplexing Signal 0 | Multiplexing Signal 1 |
|---|---|---|---|---|
| 16 | FSK_OUT | LOCK_FSKO | LOCK | FSK_OUT |

Table 3-13 describes the outputs of the multiplexed pin FSK_OUT.

**Table 3-13** Outputs of the multiplexed pin FSK_OUT

| Signal | Direction | Description |
|---|---|---|
| LOCK | O | Channel lock indicator. |
| FSK_OUT | O | FSK output. |

## 3.2 Electrical Specifications

### 3.2.1 Power Consumption Specifications

Table 3-14 describes the power consumption specifications.

**Table 3-14** Power consumption specifications

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DVDD33 | 3.3 V I/O power | None | 8 | 12 | mA |
| AVDD33_PLL | 3.3 V PLL analog power | None | 1 | 1 | mA |
| DVDD12 | 1.2 V core power | None | 100 | 352 | mA |
| ADC_VDD12 | 1.2 V ADC power | None | 56 | 65 | mA |

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| AVDD12_PLL | 1.2 V PLL analog power | None | 1 | 1 | mA |

## 3.2.2 Rated Working Conditions

**WARNING**

Hi3136 V100 may be unstable or damaged when working beyond the rated working conditions listed in Table 3-15.

Table 3-15 describes the rated working conditions.

**Table 3-15** Rated working conditions

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{OPT}$ | Operating temperature | −40 | +125 | ºC |
| $T_{STG}$ | Storage temperature | −65 | +150 | ºC |
| VI | Input voltage | −0.5 | +4.6 | V |
| VO | Output voltage | −0.5 | +4.6 | V |
| DVDD12 | Internal core voltage | −0.5 | +1.8 | V |
| DVDD33 | I/O power | −0.5 | +4.6 | V |

## 3.2.3 Recommended Working Conditions

Table 3-16 describes the recommended working conditions.

**Table 3-16** Recommended working conditions

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{OPT}$ | Operating temperature | 0 | 25 | 70 | ºC |
| DVDD12 | Internal core voltage | 1.14 | 1.2 | 1.26 | V |
| DVDD33 | I/O power | 2.97 | 3.3 | 3.63 | V |
| AVDD33_PLL | PLL power | 2.97 | 3.3 | 3.63 | V |
| AVDD12_PLL | PLL power | 1.14 | 1.2 | 1.26 | V |
| ADC_VDD12 | ADC power | 1.14 | 1.2 | 1.26 | V |

### 3.2.4 Power-On and Power-Off Sequences

The 3.3 V power is turned on before the 1.2 V power, and they are turned off in reverse order.

### 3.2.5 DC Electrical Specifications

Table 3-17 describes the DC electrical specifications.

**Table 3-17** DC electrical specifications

| Symbol | Description | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | None | DVDD33 + 0.3 | V | The 5 V tolerance voltage is not supported. |
| $V_{IL}$ | Input low voltage | –0.3 | None | 0.8 | V | None |
| $I_L$ | Input leakage current | None | None | ±10 | μA | None |
| $I_{OZ}$ | Tri-state output leakage current | None | None | ±10 | μA | None |
| $V_{OH}$ | Output high voltage | 2.4 | None | None | V | None |
| $V_{OL}$ | Output low voltage | None | None | 0.4 | V | None |
| $R_{PU}$ | Internal pull-up resistor | 30 | 55 | 80 | kΩ | None |
| $R_{PD}$ | Internal pull-down resistor | 30 | 45 | 80 | kΩ | None |

## 3.3 Design Recommendations for Schematic Diagrams

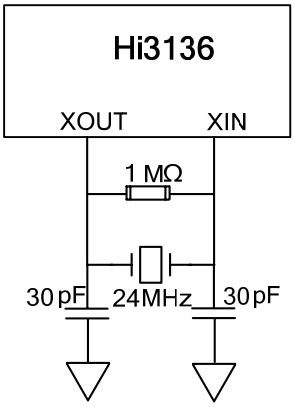
### 3.3.1 Design Recommendations for the Small System

#### 3.3.1.1 Clocking Circuit

The system clock can be generated by combining the internal feedback circuit of Hi3136 V100 with an external 24 MHz crystal oscillator circuit (recommended).

Figure 3-4 shows the recommended connection mode of the crystal oscillator.

**Figure 3-4** Recommended connection mode of the crystal oscillator




The following formula is used to calculate the capacitance of the load capacitor in the crystal oscillator:

$C_L = C1 \times C2/(C1 + C2) + C$

where

- C is the capacitance of the IC's internal capacitor, in the range of 5−7 pF.
- C1 and C2 each are 30 pF in Figure 3-4.
- $C_L$ is the capacitance of the load capacitor in the crystal oscillator, in the range of 20−22 pF. The specific value provided by vendors prevails.

## 3.3.1.2 Reset Circuit

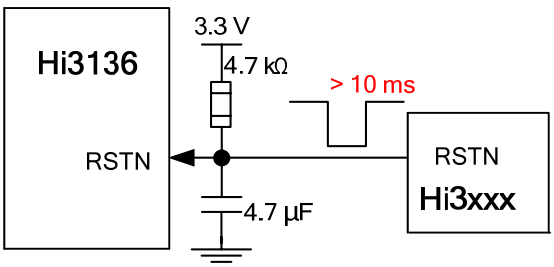
The RSTN pin of Hi3136 V100 is a reset signal input pin. The valid reset signal must have low-level pulses and the pulse width must be greater than 12 cycles of the input crystal oscillator clock from the XIN pin. Typically, the pulse width of the reset signal is 10–100 ms.

During the board design, the RC power-on reset circuit is recommended for the RSTN pin. The RSTN pin connects to a pull-up resistor and then to the 3.3 V power, and connects to a 4.7 µF capacitor and then to GND. This connection mode implements power-on reset. The RSTN pin can also connect to an STB decoder master chip. The master chip may generate a reset signal complying with protocols when the master chip and the decoder are working properly.

If an exception occurs, a specific GPIO pin of the master chip generates a low-level pulse to trigger a reset.

Figure 3-5 shows the typical reset circuit.

**Figure 3-5** Typical reset circuit



### 3.3.1.3 System Configuration Circuit for Hardware Initialization

The system configuration circuit for hardware initialization initializes internal registers over the $I^2C$ bus. The $I^2C$ addresses for Hi3136 V100 are set by configuring the external ADDR0 and ADDR1 pins.

Table 3-18 and Table 3-19 describe address configurations.

**Table 3-18** Address configurations 1

| ADDR1 | ADDR0 | 7-Bit Address | | | | | | | R/W Bit | Write Address (in Hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MSB | | | | | | LSB | | |
| Low | Low | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0xB0 |
| Low | High | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0xB2 |
| High | Low | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0xB4 |
| High | High | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0xB6 |

**Table 3-19** Address configurations 2

| ADDR1 | ADDR0 | 7-Bit Address | | | | | | | R/W Bit | Write Address (in Hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MSB | | | | | | LSB | | |
| Low | Low | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0xB1 |
| Low | High | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0xB3 |
| High | Low | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0xB5 |
| High | High | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0xB7 |

### 3.3.1.4 Circuits for Digital/Analog Signal Interfaces

## Introduction

The level standard of digital interfaces is LVCMOS33. Hi3136 V100 provides the following digital signal interfaces:

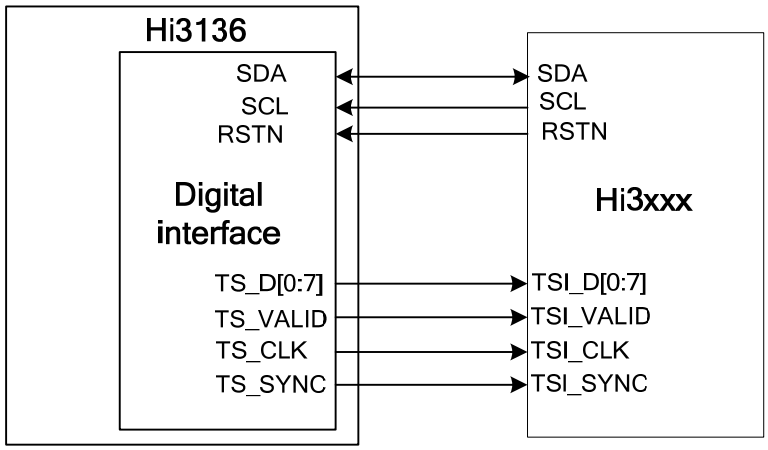
- One TS serial/parallel interface. The working mode can be set to parallel or serial. The working clock frequency is 187.5 MHz in 1-bit serial mode or 94 MHz in 2-bit serial mode. In parallel mode, the working clock frequency is a maximum of 23.5 MHz. The bit width is 8 bits in parallel mode, 1 bit in 1-bit serial mode, or 2 bits in 2-bit serial mode.
- One $I^2C$ interface. The internal registers of Hi3136 V100 and tuner are accessed over the $I^2C$ interface. Hi3136 V100 controls the tuner by using the commands forwarded by the $I^2C$. The maximum $I^2C$ working clock frequency is 400 kHz.

- Two DiSEqC interfaces and two FSK interfaces. The DISEQC_OUT and FSK_OUT interfaces are used to switch antennas. The DiSEqc_IN and FSK_IN interfaces are used to implement the backhaul of control signals provided by antennas.
- One AGC output interface. This interface is used to control the gain of the front-end tuner in pulse density modulation (PDM) mode by using an RC low-pass filtering circuit.
- One RSTN interface. A reset can be performed by using a hardware RC circuit or an STB decoder chip. The RSTN signal is active low.

## TS Topologies

Figure 3-6 shows the typical topology in which Hi3136 V100 connects to an STB decoder chip in parallel.

**Figure 3-6** Topology in which Hi3136 V100 connects to an STB decoder chip in parallel

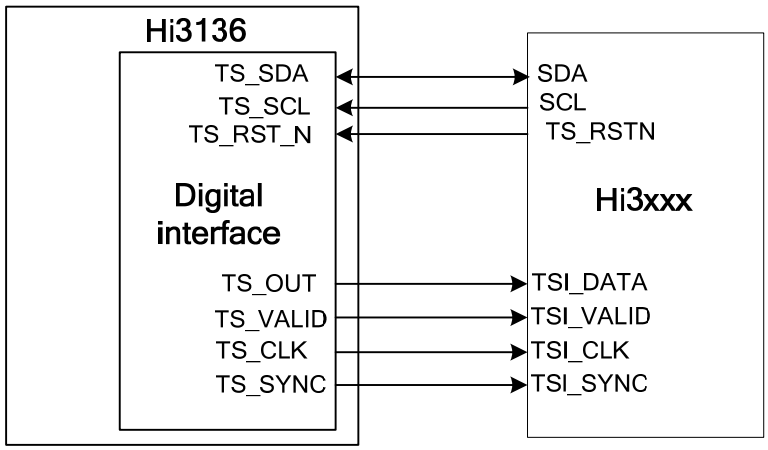



**NOTE**

All TS output pins except TS_CLK in the TS parallel interface can be configured based on the actual layout.

Figure 3-7 shows the typical topology in which Hi3136 V100 connects to an STB decoder chip in series.

**Figure 3-7** Topology in which Hi3136 V100 connects to an STB decoder chip in series



**NOTE**

All TS output pins except TS_CLK in the TS serial interface can be configured based on the actual layout.

## DiSEqC Topology

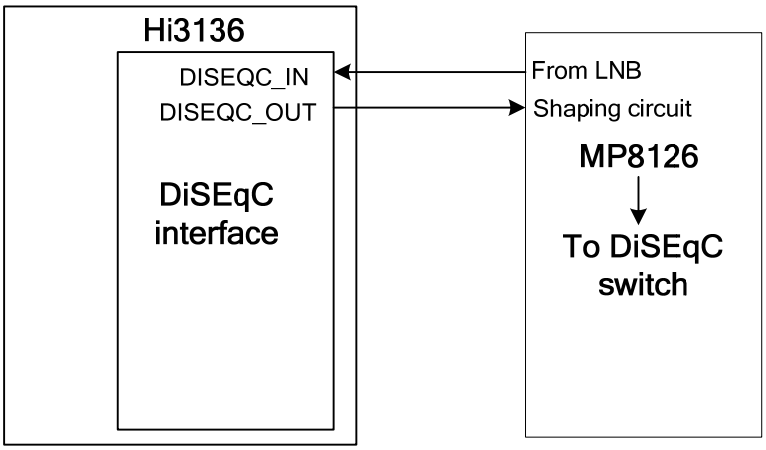
The embedded DiSEqC module in Hi3136 V100 switches LNBs to control multiple satellite signals. In this way, an STB can control multiple antennas. The DiSEqC module provides discontinuous digital signals that are modulated at 22 kHz carriers and LNB power supplies. An external shaping circuit is required for ensuring amplitude and signal quality. Otherwise, the DiSEqC device cannot identify commands.

The following are required configurations:

- 22 kHz frequency range: 22±4.4 kHz
- Peak voltage: 650 mV (±250 mV)
- External bus load capacitance: less than or equal to 250 nF

Figure 3-8 shows the topology in which the DiSEqC interface connects to an external circuit.

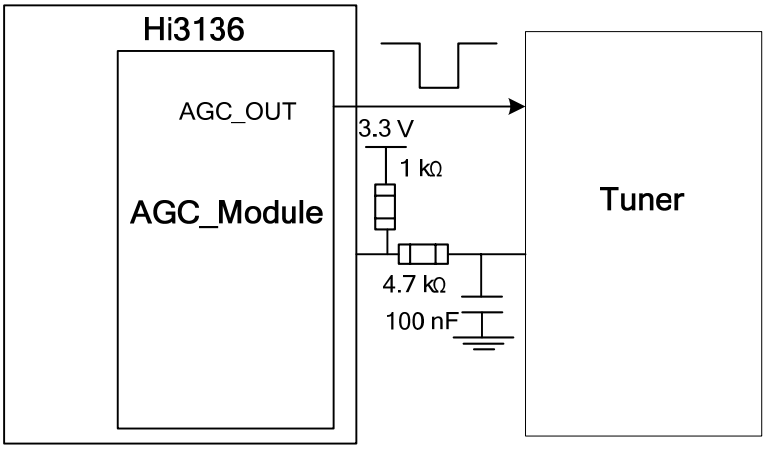
**Figure 3-8** Topology in which the DiSEqC interface connects to the LM317 or MP8126




## AGC Topology

The AGC module converts digital signals into analog signals in PDM output mode by using an external RC low-pass filter and automatically controls the gain of the front-end tuner when the external environment changes. This ensures good output signal quality. During the PCB layout design, the RC filtering circuit needs to be placed close to the AGC output pin of Hi3136 V100, preventing interference to analog radio frequency (RF) signals. Figure 3-9 shows the topology in which the AGC interface connects to a tuner.

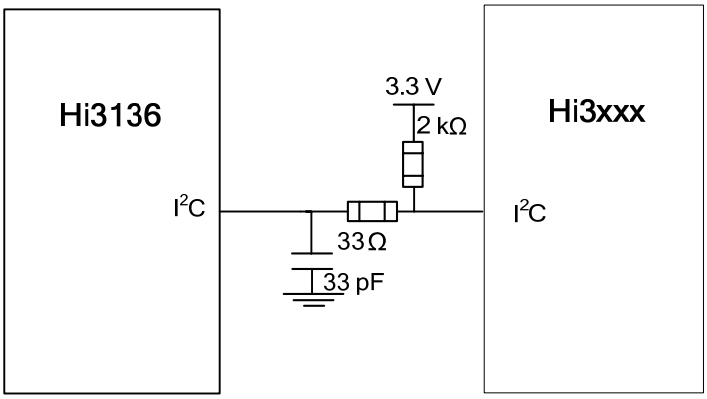
**Figure 3-9** Topology in which the AGC interface connects to a tuner




## I²C Bus

The I²C bus between Hi3136 V100 and an STB decoder chip must connect to a pull-up resistor and then to the 3.3 V power. In Figure 3-10, a 2 kΩ pull-up resistor is used. You can select the resistor based on the I2C bus rate. In addition, a 100 pF or less bypass filtering capacitor must be connected on each I²C trace close to the Hi3136 I²C pin. See Figure 3-10.

**Figure 3-10** Topology in which the I²C interface of Hi3136 V100 connects to an STB decoder chip




## TS Matching Design

The TS matching design is provided based on the number of PCB layers:

- When more than two PCB layers are designed, the trace characteristic impedance is 50 Ω.
  - TS_OUT[0:7] connect to a 33 Ω resistor in series. For details about the topology, see Figure 3-11.
  - TS_CLK, TS_SYNC, and TS_VALID connect to a 33 Ω resistor in series. For details about the topology, see Figure 3-12.
- When two PCB layers are designed, the trace characteristic impedance is 140 Ω.

- TS_OUT[0:7] connect to a 75 Ω resistor in series. For details about the topology, see Figure 3-13.
- TS_CLK, TS_VALID, and TS_SYNC connect to a 75 Ω resistor in series. For details about the topology, see Figure 3-14.

**NOTE**

The maximum trace length is 5000 mils.

**Figure 3-11** Interconnection topology for TS_OUT[0:7] and an STB decoder chip when more than two PCB layers are designed

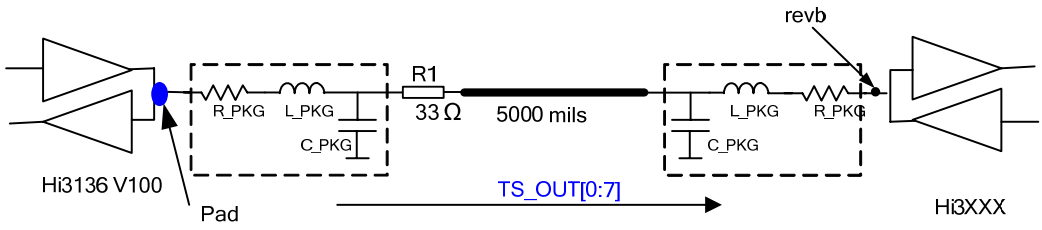



**Figure 3-12** Interconnection topology for TS_CLK/TS_SYNC/TS_VALID and an STB decoder chip when more than two PCB layers are designed

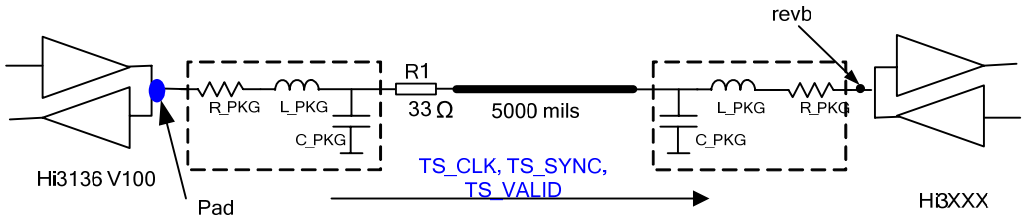



**Figure 3-13** Interconnection topology for TS_OUT[0:7] and an STB decoder chip when two PCB layers are designed

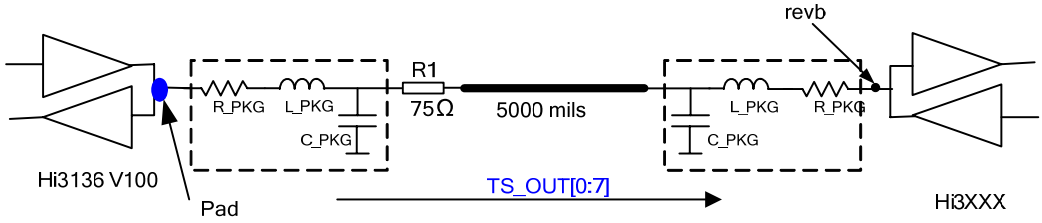
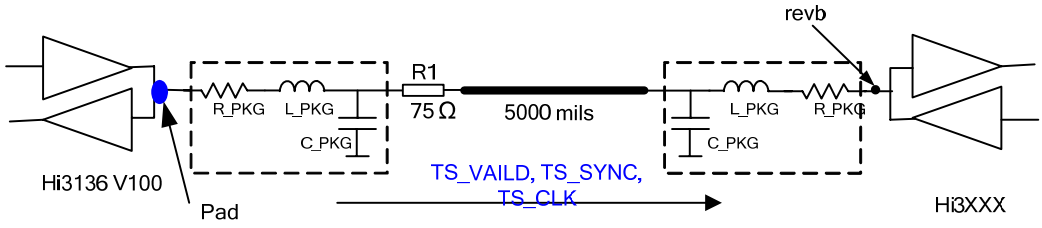



**Figure 3-14** Interconnection topology for TS_VAILD/TS_SYNC/TS_CLK and an STB decoder chip when two PCB layers are designed



### AGC Circuit

After the low-pass filter processes PDM signals, the AC analog signals are significantly reduced. On the RC filtering network, a larger RC value indicates less AC analog signals but slower response. Therefore, an appropriate RC value is required to balance the quantity of AC analog signals and response speed in actual application scenarios. A 4.7 kΩ resistor and a 100 nF capacitor are recommended on the AGC circuit.

## 3.3.2 Power Supplies

**NOTE**

For details about system power supply design, see the schematic diagram of the Hi3136 V100 board.

### 3.3.2.1 Core Power

The core power pins (DVDD12) connect to the 1.2 V digital power. Note the following:

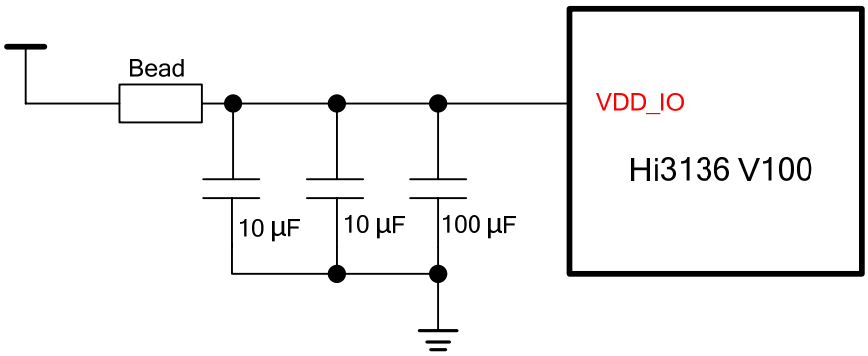
- If there is no 1.2 V power on the board, the low dropout regulator (LDO) is preferred for the power chip and the current of the power chip must be greater than or equal to 500 mA.
- The typical current of the core power is 100 mA and the maximum current is 405 mA.
- Each core power pin connects to a 10 µF filtering bypass capacitor and then to GND. In addition, each core power pin connects to a group of 10 nF and 100 nF decoupling capacitors, which are placed close to the core power pin.

### 3.3.2.2 I/O Power

The I/O power pins (DVDD33) connect to the 3.3 V digital power. Note the following:

- The maximum current of VDD_IO is 12 mA. The LDO is preferred.
- Each I/O power pin connects to a group of 10 nF and 100 nF decoupling capacitors, which are placed close to the I/O power pin.
- The inputs of I/O power pins are isolated by using electromagnetic interference (EMI) beads. See Figure 3-15.

**Figure 3-15** VDD33_IO topology

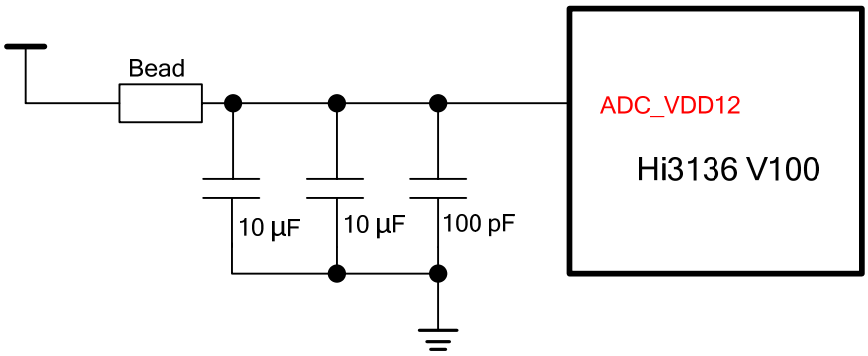



### 3.3.2.3 ADC Power

ADC power pins (ADC_VDD12) connect to the 1.2 V analog power. Note the following:

- The maximum current of the ADC power is 65 mA. The ADC power and core power share a 1.2 V power.
- The ADC power is isolated from the 1.2 V power by using an EMI bead and connects to a 10 µF filtering bypass capacitor and then to GND.
- Each ADC power pin connects to a group of 10 nF and 100 nF decoupling capacitors, which are placed close to the ADC power pin.
- The deviation of the 1.2 V power is within ±5%. See Figure 3-16.

**Figure 3-16** ADC_VDD12 topology




#### 3.3.2.4 Others

Note the following:

- The LDO is preferred for the power chip. The digital and analog power supplies are isolated by using EMI beads and groups of 10 nF and 100 pF decoupling capacitors are connected.
- Ensure that the output voltage of power supplies meets requirements even when ripples and noises occur. For details about the requirements on the power supply of each module, see section 3.2 "Electrical Specifications."

### 3.3.3 Unused Pins

If some pins are not used, do not connect them. You can disable some circuits by configuring registers.

## 3.4 PCB Design Recommendations

### 3.4.1 Stack and Layout

#### 3.4.1.1 Stack

The package of Hi3136 V100 is mapped quad flat non-leaded 48 (MQFN48). The ball pitch is 0.4 mm (0.02 in.). You are advised to design a 4-layer PCB with the following stack:

- Top layer: signal traces
- Internal layer 1: GND plane
- Internal layer 2: power plane

- Bottom layer: signal traces

To reduce the cost, you can also design a 2-layer PCB with the following stack:

- Top layer: signal traces and part of power traces
- Bottom layer: GND plane and part of power traces

Take the following precautions during PCB design:

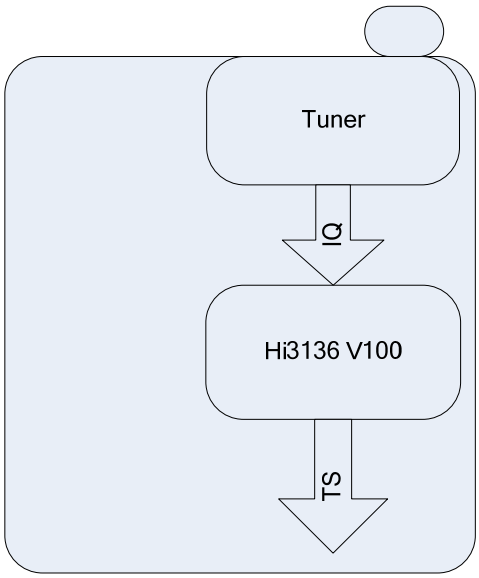
- Components are placed at the top layer. Routing signal traces at the top layer is preferred.
- Power pins are connected by using wide traces.
- Ensure that the bottom layer is a complete GND plane.
- The vias with 8-mil diameter is recommended for master chip fanout.
- The impedance of special signal traces must meet requirements.

The PCB material is FR-4, the PCB thickness is 1.6 mm, and the thickness of the copper foil on the surface is 1 oz.

### 3.4.1.2 Board Layout

Figure 3-17 shows the board layout of the Hi3136 V100 reference design.

**Figure 3-17** Board layout




The following items are considered in the Hi3136 V100 reference design: the layout of RF, analog, and digital signals and electrostatic discharge (ESD) protective components such as the female connector of the RF interface, crystal resonator, and RF loop filter.

The 3.3 V and 1.2 V power pins should be isolated from digital parts by using EMI beads. The components with a small-sized package are recommended.

# 3.4.2 PCB Design Recommendations for the Small System

## 3.4.2.1 Power Supplies of the Small System

### Digital Power

The digital power supplies of Hi3136 V100 include DVDD33 (3.3 V) and DVDD12 (1.2 V). It is recommended that the DVDD33 and DVDD12 be isolated from the 3.3 V and 1.2 V digital power supplies of the board by using EMI beads. All power traces use the exposed pad of Hi3136 V100 as the reference GND. The traces should be as wide as possible when the through-flow capacity is ensured. The minimum trace width is 15 mils for DVDD33 or 25 mils for DVDD12. Ensure that digital power and analog power do not overlap and decoupling capacitors are placed close to Hi3136 V100.

### RF/Analog Power

The RF and analog power supplies must be isolated from other power supplies by using EMI beads. Hi3136 V100 uses the exposed pad as the reference GND. The following are design recommendations:

- Never route digital signal traces, especially high-speed digital signal traces, in the analog power area.
- Connect a decoupling capacitor to each power pin and ensure that traces are as wide as possible and decoupling capacitors are placed close to Hi3136 V100.

## 3.4.2.2 Clock and Reset Circuits

### Clock

The power supplies of the Hi3136 V100 PLL unit are AVDD12_PLL (1.2 V) and AVDD33_PLL. The reference GND of the Hi3136 V100 PLL unit is PLL_GND. Design the PCB according to the following guidelines:

- Ensure that the width of the AVDD12_PLL trace or the AVDD33_PLL trace is 12 mils when the through-flow capacity is ensured.
- It is recommended that GND traces be connected under the exposed pad and the GND planes of Hi3136 V100 and the board are connected.
- The traces of the crystal oscillator circuit for the system clock must be as short as possible and be surrounded by GND traces. The crystal GND part must be isolated from the large-sized GND area to prevent coupling.
- The matched capacitors for the crystal oscillator must be placed close to the crystal oscillator and the crystal oscillator must be placed close to Hi3136 V100. Ensure that the spacing between the crystal oscillator and the board edge is at least 1000 mils. Never route critical traces such as high-speed clock traces under the crystal oscillator and ensure the integrity of the signal traces under the crystal oscillator.

### Reset

Pin 15 is a reset pin. The reset signal trace is a critical trace and is susceptible to interference. The following are design recommendations:

- If more than two PCB layers are designed, route the reset signal trace at an inner layer close to the GND plane and ensure that the trace width is greater than 8 mils. If two PCB layers are designed, ensure that the reset signal trace is surrounded by GND traces.
- Route the reset signal trace at least 30 mils far away from interfaces and power inputs.

# 3.4.3 PCB Design Recommendations for Digital and Analog Interfaces

## 3.4.3.1 Digital Interfaces

### TS Signals

The following are requirements on TS signal traces:

- The maximum signal trace length is 5000 mils.
- The length of all TS signal traces is determined based on the TS_CLK traces. The length deviation is ±250 mils.
- The serial matched resistors are connected close to Hi3136 V100.
- If two PCB layers are designed, the characteristic impedance of TS signal traces should be 140 Ω. It is recommended that a 75 Ω resistor connect to TS_OUT[0:7] in series and a 75 Ω resistor connect to TS_CLK, TS_SYNC, and TS_VALID in series.
- If more than two PCB layers are designed, the characteristic impedance of the TS signal traces should be 50 Ω. A 33 Ω matched resistor is recommended.

### AGC Signals

The following are requirements on AGC signal traces:

- The maximum trace length is 5000 mils and the minimum one is 12 mils. Route GND traces around AGC signal traces. This prevents interference to external signal traces from AGC signals and interference to AGC signal traces from external noise.
- The RC low-pass integrating filter to which AGC outputs are transmitted is placed close to the AGC output pin of Hi3136 V100. This prevents AGC noise from being transmitted to the board, which prevents channel performance from deteriorating.

The following are requirements on the $I^2C$ bus length:

- The maximum length of serial clock (SCL) signal traces is 5000 mils.
- The serial data (SDA) traces are routed based on SCL traces. The length deviation is ±250 mils.

### PCB Routing Recommendations

Route traces on a PCB according to the following guidelines:

**CAUTION**

Never cross the reference GND plane of TS signal traces when routing other signal traces, and ensure that GND traces are routed around signal traces. Serial resistors need to be placed close to Hi3136 V100. For details, see the PCB design documents of the Hi3136EVA board.

- All the TS signal traces must be routed on the planes close to the GND plane. Never route the signal traces across the power and GND plane splits. Ensure that signal traces have a complete reference GND plane.
- To ensure a good signal return path, punch vias around signal traces and changed layers and connect the punched vias to GND.
- Ensure that signal traces are as short as possible. Minimize the use of vias to ensure the impedance continuity of traces. If more than two PCB layers are designed, the characteristic impedance of the single-ended PCB signal trace is 50 Ω ±10%. If two PCB layers are designed, the characteristic impedance of the single-ended PCB signal trace is 140 Ω ±10%. The serial matched resistors are connected close to Hi3136 V100.
- If resistor networks are used, ensure that the TS_CLK trace and TS traces are not routed on the same resistor network.
- Ensure that the spacing between adjacent signal traces is 2–3 times of the trace width according to the 3W rule. The 3W rule indicates that the trace spacing is three times of the trace width.
- Route signal traces far away from data and address buses and route GND traces around the TS_CLK trace.

#### 3.4.3.2 Others

#### Integrity Simulation Design Recommendations for PCB Signals

By using board-level simulation tools, PCB designers can simulate and analyze signal integrity based on the input/output buffer information specification (IBIS) models of the Hi3136 V100 interfaces and interconnected components, transmission line models, and board topologies. Based on the simulation results, the PCB designers can adjust the typologies to meet the signal quality requirements in overshoot, undershoot, ringing, monotonicity, and others.

#### Note

If a clock signal trace connects to multiple loads, ensure good signal quality especially signal edge monotonicity regardless of the frequency.

## 3.5 Heat Design Recommendations

### 3.5.1 Package Thermal Resistance

**CAUTION**

The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.

Table 3-20 describes the thermal resistance of the package.

**Table 3-20** Thermal resistance of the package

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction-to-ambient thermal resistance | $\theta_{JA}$ | 32 | ºC/W |
| Junction-to-case thermal resistance | $\theta_{JC}$ | 6.5 | ºC/W |
| Junction-to-top center of case thermal resistance | $\Psi_{JT}$ | None | ºC/W |
| Junction-to-board thermal resistance | $\theta_{JB}$ | 8.5 | ºC/W |

## 3.5.2 Recommended Thermally Conductive Materials

Table 3-21 describes recommended thermally conductive materials.

**Table 3-21** Recommended thermally conductive materials

| Mode of Fixing Heat Sinks | Model | Thermal Conductivity Coefficient (W/m·k) | Ambient Temperature (°C) | Colloid Type | Insulation Strength (V/Mil) | Flame Retar dance | Bearing Capacity (g) |
|---|---|---|---|---|---|---|---|
| Mechanical fixing | GF2000 | 2 | −60 to +200 | Silicone rubber | 500 | UL9V 0 | None |
| Non-mechanical fixing | Locotite 315 | 0.808 | None | Acrylic resin | 6000 | UL9V 2 | None |

## 3.5.3 Schematic Diagram Design

### 3.5.3.1 Power Supply

Ensure that the efficiency of the board power tree is the highest as long as the power supply is stable. To this end, design the board power supply optimally and use fewer LDO components with large voltage difference to reduce the heat produced during power conversion. An exposed pad is designed at the bottom of the chip and a solder mask opening is designed for the GND plane of the PCB to facilitate heat conduction.

## 3.5.4 PCB Design

### 3.5.4.1 Component Layout

Lay out components based on the product architecture and heat dissipation design:

- Do not lay out the components that consume a large amount of power and produce much heat on the same ventilation path.
- Evenly place the components that consume a large amount of power and produce much heat and increase the size of copper planes under and around the components, ensuring that the heat produced by the PCB is effectively dissipated.

### 3.5.4.2 PCB Heat Dissipation

The recommendations are as follows:

- For the connect style of the vias under Hi3136 V100, select the full connect style but not the thermal connect style, In addition, an opening copper plane is used at the PCB bottom layer on which the exposed pad of Hi3136 V100 is soldered, improving the dissipation efficiency of the board.
- The 1.2 V power traces, 3.3 V power traces, and GND traces should be as wide as possible when the over-current capability is ensured.
- Never place the components that produce much heat around Hi3136 V100.

# 3.6 Soldering Process Recommendations

## 3.6.1 Overview

Determine appropriate reflow soldering temperatures based on the reflow profiles supported by all the components, ICs, and PCB and the reflow profile recommended by the solder paste vendor. This chapter describes only the reflow soldering temperature range supported by Hi3136 V100.

### 3.6.1.1 Coating Material

The elelectrotinning coating is used on the MQFN package.

### 3.6.1.2 Component Package and Storage

The following describes the component package and storage:

- Package of surface-mount components: tray or tape & reel
- Allowed storage duration (at most 60% RH): 12 months at 40ºC (104ºF)
- Packaging material: ESD material

### 3.6.1.3 Soldering Process

Reflow soldering can be used.

Figure 3-18 shows the reflow profiles supported by Hi3136 V100 but not the reflow profiles recommended during soldering. Determine the soldering temperatures based on the reflow profiles of the solder paste, PCB, and all ICs and components. For details, see the JEDEC020D standard.

**Figure 3-18** Soldering temperatures

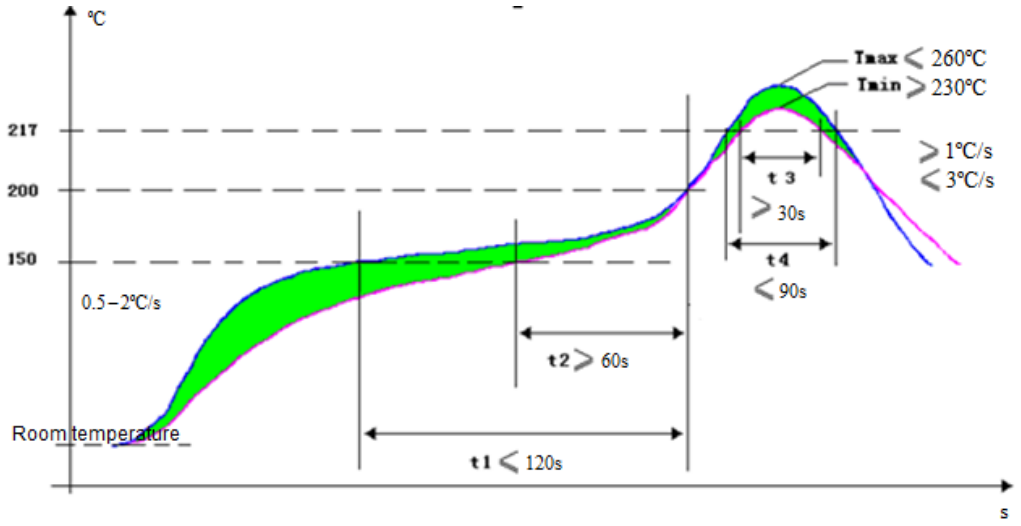



Table 3-22 describes the reflow soldering specifications.

**Table 3-22** Reflow soldering specifications

| Zone | Duration | Heating Up Slope | Peak Temperature | Cooling Down Slope |
|---|---|---|---|---|
| Preheat zone (40–150°C or 104–302°F) | 60−150s | ≤ 2.0ºC/s (≤ 35.6ºF/s) | None | None |
| Soak zone (150–200°C or 302–392°F) | 60−120s | < 1.0ºC/s (≤ 33.8ºF/s) | None | None |
| Reflow zone (> 217°C or 423°F) | 30−90s | None | 230−260ºC (446−500ºF) | None |
| Cooling zone (Tmax to 180°C or 356°F) | None | None | None | 1.0ºC/s ≤ Slope ≤ 4.0ºC/s (33.8ºF/s ≤ Slope ≤ 39.2ºF/s) |

## 3.6.2 Process Preparations

Confirm that all products are dry and materials have not expired.

Test the first sample such as checking the solder paste thickness before mass production. Start mass production only when the first sample passes all tests.

# 3.7 Moisture-Sensitive Specifications

## 3.7.1 Storage and Usage

[Application Scope]

The specifications apply to the storage and usage of all moisture-sensitive ICs of HiSilicon.

[Storage Environment]

You are advised to store products in vacuum packages at 30°C (86°F) or lower and at most 60% relative humidity (RH).

[Shelf Life]

At 30°C (86°F) or lower and at most 60% RH, the shelf life is greater than or equal to 12 months for the vacuum package.

[Floor Life]

Table 3-23 describes the floor life at 30°C (86°F) or lower and at most 60% RH.

**Table 3-23** Floor life

| Level | Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated |
|---|---|
| 1 | Unlimited at 30°C (86°F) or lower and at most 85% RH |
| 2 | 1 year |
| 2a | 4 weeks |
| 3 | 168 hours |
| 4 | 72 hours |
| 5 | 48 hours |
| 5a | 24 hours |
| 6 | Mandatory bake before use. The product must be reflowed within the time limit specified on the label. |

[Usage of Moisture-Sensitive Products]

- If a chip has been exposed to air for 2 hours at 30°C (86°F) or lower and at most 60% RH, rebake it and pack it into a vacuum bag.
- If a chip has been exposed to air for less than 2 hours at 30°C (86°F) or lower and at most 60% RH, replace the desiccant and pack the chip into a vacuum bag.

For details about other storage modes and usage rules, see the JEDEC J-STD-033A standard.

## 3.7.2 Rebaking

[Applicable Products]

All moisture-sensitive ICs of HiSilicon

[Application Scope]

All ICs that need to be rebaked

[Rebaking Reference]

**Table 3-24** Rebaking reference

| Body Thickness | Level | Baking at 125°C (257°F) | Baking at 90°C (194°F) ≤ 5% RH | Baking at 40°C (104°F) ≤ 5% RH |
|---|---|---|---|---|
| ≤ 1.4 mm (0.06 in.) | 2a | 3 hours | 11 hours | 5 days |
| | 3 | 7hours | 23 hours | 9 days |
| | 4 | 7 hours | 23 hours | 9 days |
| | 5 | 7 hours | 24 hours | 10 days |
| | 5a | 10 hours | 24 hours | 10 days |
| ≤ 2.0 mm (0.08 in.) | 2a | 16 hours | 2 days | 22 days |
| | 3 | 17 hours | 2 days | 23 days |
| | 4 | 20 hours | 3 days | 28 days |
| | 5 | 25 hours | 4 days | 35 days |
| | 5a | 40 hours | 6 days | 56 days |
| ≤ 4.5 mm (0.18 in.) | 2a | 48 hours | 7 days | 67 days |
| | 3 | 48 hours | 8 days | 67 days |
| | 4 | 48 hours | 10 days | 67 days |
| | 5 | 48 hours | 10 days | 67 days |
| | 5a | 48 hours | 10 days | 67 days |

Note:

- Table 3-24 lists the minimum rebaking time for moist chips.
- Low-temperature rebaking is recommended.
- For details, see the JEDEC standard.

# 3.8 Interface Timings

## 3.8.1 Output Interface Timings

Hi3136 V100 supports three TS output modes: parallel mode, 1-bit serial mode, and 2-bit serial mode.

The signals from the TS output interface include the data signal TS_OUT[7:0], clock signal TS_CLK, data validity signal TS_VLD, sync header signal TS_SYNC, and packet error signal TS_ERR.

- TS_OUT: TS frame data. This signal is 8 bits in parallel mode, 1 bit in 1-bit serial mode, and 2 bits in 2-bit serial mode.
- TS_CLK: data clock. The clock edge is configurable. The clock output varies according to the output mode.
- TS_VLD: TS packet data validity indicator. It is byte valid in parallel mode or bit valid in 1-bit serial mode.
- TS_SYNC: TS packet sync header indicator. It is byte valid in parallel mode or bit valid in 1-bit serial mode.
- TS_ERR: TS packet error indicator. It is set to 1 if an error occurs in the current TS packet.

**Figure 3-19** Timing in TS parallel output mode

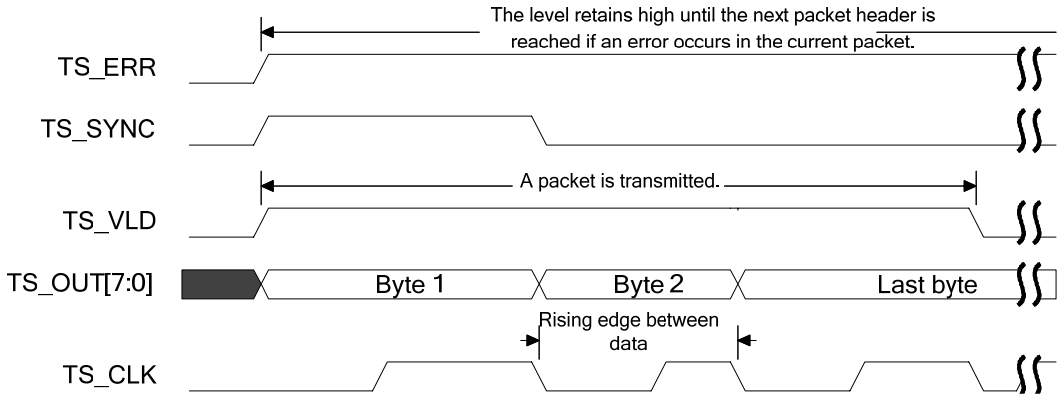



**Figure 3-20** Timing in 1-bit TS serial output mode

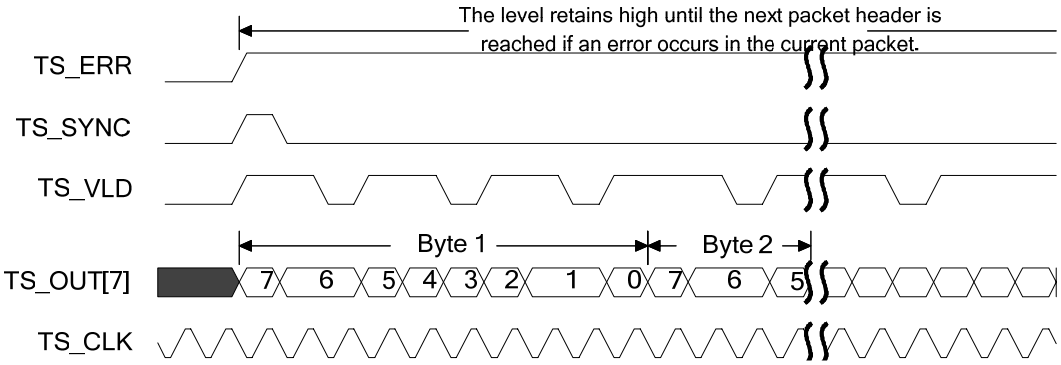
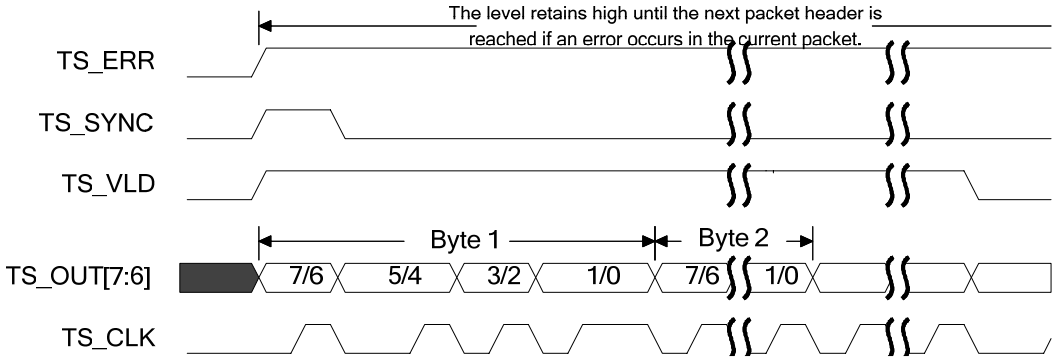


**Figure 3-21** Timing in 2-bit TS serial output mode




## 3.8.2 Output Timing Parameters

Figure 3-22 and Figure 3-23 show the TS output timings.

**Figure 3-22** TS_CLK timing and reverse timing

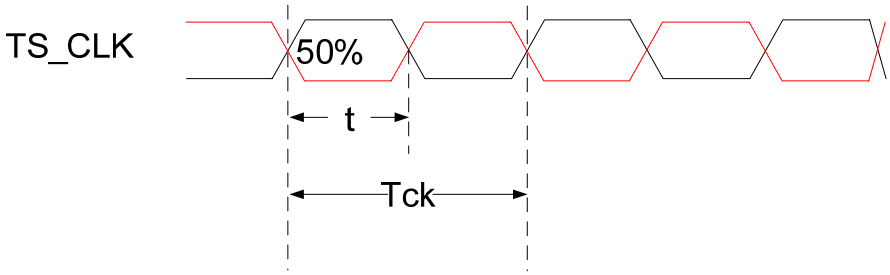
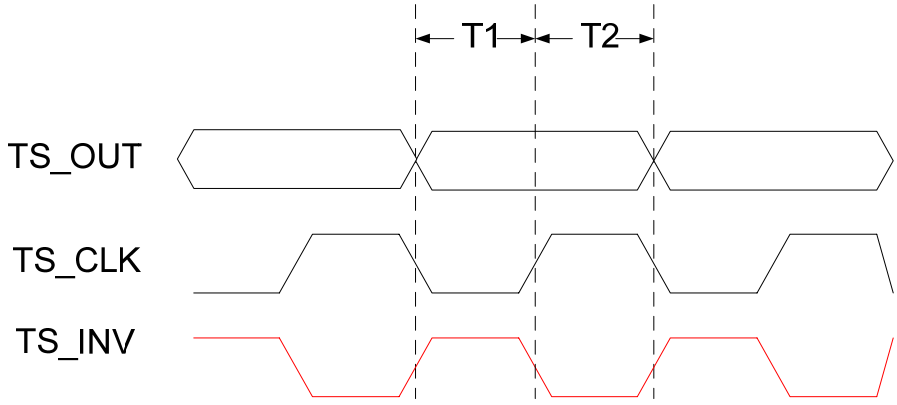



**Figure 3-23** TS timings in parallel and 2-bit serial modes




The minimum values of T1 and T2 are both 5.3 ns.

**Table 3-25** TS output timing parameters

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TS_CLK | Tck | 5.3 | None | 5.3 | ns |
| Output data signal delay | t | 0 | None | 0.48 | ns |

**Table 3-26** TS output timing parameters (reverse)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TS_CLK | Tck | 5.3 | None | 5.3 | ns |
| Output data signal delay | t | 1.0 | None | 2.63 | ns |

# A Acronyms and Abbreviations

**A**

| | |
|---|---|
| **AAC** | advanced audio coding |
| **AAF** | anti-aliasing filter |
| **ABR** | average bit rate |
| **AC** | alternating current |
| **ACA** | accessory charge adapter |
| **ACC** | automatic contrast control |
| **ACD** | auto command done |
| **ACM** | adaptive coding and modulation |
| **ADP** | attach detection protocol |
| **ADC** | analog-to-digital converter |
| **AE** | automatic exposure |
| **AEC** | audio echo cancellation |
| **AES** | advanced encryption standard |
| **AF** | adaption field |
| **AGC** | automatic gain control |
| **AHB** | advanced high-performance bus |
| **AI** | audio input |
| **AIU** | audio input unit |
| **ALU** | arithmetic logic unit |
| **AMBA** | advanced microcontroller bus architecture |
| **AMP** | asymmetric multi-processing |
| **ANI** | automatic number identification |
| **ANR** | automatic noise reduction |

| | |
|---|---|
| **AO** | audio output |
| **AOU** | audio output unit |
| **AP** | access point |
| **APB** | advanced peripheral bus |
| **API** | application programming interface |
| **APLL** | analog phase-locked loop |
| **APSK** | amplitude phase shift keying |
| **AQTD** | alternate queue transfer descriptor |
| **ARM** | advanced RISC machines |
| **ARGB** | alpha, red, green, blue |
| **ASF** | advanced specification format |
| **ATA** | advanced technology attachment |
| **ATAH** | ATA host controller |
| **ATAPI** | advanced technology attachment packet interface |
| **ATR** | answer to reset |
| **ATTR** | attribute |
| **AUD** | audio |
| **AV** | audio & video |
| **AVI** | auxiliary video information |
| **AVS** | audio video coding standard |
| **AWB** | automatic white balance |
| **AXI** | advanced eXtensible interface |

**B**

| | |
|---|---|
| **BB** | baseband |
| **BCH** | Bose-Chaudhuri-Hocquenghem |
| **BCM** | byte counter modified |
| **BEP** | boot entrance point |
| **BER** | bit error rate |
| **BGA** | ball grid array |
| **BIST** | built-in self test |
| **BIU** | bus interface unit |
| **BMC** | bi-phase mark coding |

| | |
|---|---|
| **BND** | bayonet nut connector |
| **BOM** | bill of material |
| **BPD** | bit plan decoder |
| **BPSK** | binary phase shift keying |
| **BRG** | bridge |
| **BSP** | board support package |
| **BVACT** | bottom vertical active area |
| **BVBB** | bottom vertical back blank |
| **BVFB** | bottom vertical front blank |

**C**

| | |
|---|---|
| **CA** | conditional access |
| **CABAC** | context-based adaptive binary arithmetic coding |
| **CAR** | committed access rate |
| **CAS** | column address signal. |
| **CAVLC** | context adaptive variable length coding |
| **CBC** | cipher block chaining |
| **CBR** | constant bit rate |
| **CCB** | change control board |
| **CCC** | command completion coalescing |
| **CCD** | charge-coupled device |
| **CCM** | constant coding and modulation |
| **CD** | command done or collision detection |
| **CDR** | clock data recovery |
| **CEC** | consumer electronics control |
| **CF** | compact flash |
| **CFB** | cipher feedback |
| **CFR** | crest factor reduction |
| **CGI** | common gate interface |
| **CGMS** | copy generation management system |
| **CI** | common interface |
| **CIC** | cascaded integrator comb |
| **CIU** | card interface unit |

| | |
|---|---|
| **CL** | CAS latency |
| **CLK** | clock |
| **CML** | current mode logic |
| **CMOS** | complementary metal-oxide semiconductor |
| **CN** | carrier noise |
| **CNG** | comfort noise generator |
| **CODEC** | coder/decoder |
| **CP** | charge pump |
| **CPL** | completion |
| **CPLD** | complex programmable logic device |
| **CPU** | central processing unit |
| **CR** | carrier recovery |
| **CRC** | cyclic redundancy check |
| **CRG** | clock and reset generator |
| **CRS** | completion retry request |
| **CS** | chip select |
| **CSA** | common scramble algorithm |
| **CSI** | camera serial interface |
| **CSIX** | common switch interface |
| **CSMD** | carrier sense multiple access |
| **CTI** | chroma transient improvement |
| **CTR** | counter |
| **CTS** | clear to send |
| **CVBS** | composite video broadcast signal |
| **CW** | cipher word |

**D**

| | |
|---|---|
| **DAC** | digital-to-analog converter |
| **DAG** | digital automatic gain |
| **DAGC** | digital automatic gain control |
| **DAV** | DMA of audio and video |
| **DC** | direct current |
| **DCD** | data connect detection |

| | |
|---|---|
| **DCRC** | data CRC error |
| **DDC** | display data channel |
| **DDR** | double data-rate |
| **DDRC** | double data rate controller |
| **DHCP** | dynamic host configuration protocol |
| **DEM** | dynamic-element matching |
| **DES** | data encryption standard |
| **DFT** | design for test |
| **DIP** | dual in-line package |
| **DIS** | digital image stabilization |
| **DiSEqC** | digital satellite equipment control |
| **DLL** | delay locked loop |
| **DM** | data mask |
| **DMA** | direct memory access |
| **DMAC** | direct memory access controller |
| **DNR** | digital noise reduction |
| **DP** | data path |
| **DPLL** | digital phase-locked loop |
| **DQ** | data input/output |
| **DQS** | data strobe |
| **DR** | design requirement |
| **DRAM** | dynamic random access memory |
| **DRC** | dynamic range compression |
| **DRM** | digital rights management |
| **DRTO** | data read timeout |
| **DSI** | display serial interface |
| **DSU** | dedicated scaling unit |
| **DTMF** | dual tone multi frequency |
| **DTO** | data transfer over |
| **DVB** | digital video broadcasting |
| **DVB-S** | digital video broadcasting-satellite |
| **DVD** | digital versatile disc |
| **DVI** | digital visual interface |

| | |
|---|---|
| **DVR** | digital video recorder |
| **DWA** | data weighted averaging |
| | |
| **E** | |
| **E2PROM** | electrically erasable programmable read-only memory |
| **EAV** | end of active video |
| **EB** | eviction buffer |
| **EBE** | end-bit error |
| **EBI** | external bus interface |
| **ECB** | electronic codebook |
| **ECC** | error correcting code |
| **ECM** | entitlement control message |
| **ECS** | embedded CPU subsystem |
| **ED** | exposed die |
| **EDID** | extended display identification data |
| **EEE** | energy efficient Ethernet |
| **EHCI** | enhanced host controller interface |
| **EMI** | electromagnetic interference |
| **EMM** | entitlement management message |
| **eMMC** | embedded multimedia card |
| **EOP** | end of PES |
| **EoS** | Ethernet over SONET/SDH |
| **EP** | end point |
| **EPG** | electronic program guide |
| **EQU** | equalizer |
| **ERR** | error |
| **ES** | element stream |
| **eSATA** | external serial advanced technology attachment |
| **ESD** | electrostatic discharge |
| **ESR** | equivalent series resistance |
| **ETH** | Ethernet |
| **ETU** | elementary time unit |

**F**

| | |
|---|---|
| **FAS** | frame aligning signal |
| **FBE** | feedback equalizer |
| **FC** | switch fabric |
| **FCBGA** | flip-chip ball grid array |
| **FCCSP** | flip-chip chip scale package |
| **FEC** | forward error correction |
| **FER** | frame error rate |
| **FFC** | flexible flat cable |
| **FFE** | feed forward equalizer |
| **FIFO** | first in first out |
| **FIQ** | fast interrupt request |
| **FIR** | finite impulse response |
| **FIS** | frame information structure |
| **FOD** | field order detect |
| **FPC** | flexible printed connector |
| **FPU** | floating-point unit |
| **FRUN** | FIFO underrun/overrun error |
| **FSK** | frequency shift keying |
| **FTP** | File Transfer Protocol |

**G**

| | |
|---|---|
| **GFP-F** | frame-mapped generic framing procedure |
| **GFP-T** | transparent generic framing procedure |
| **GHB** | global history buffer |
| **GIC** | generic interrupt controller |
| **GOP** | group of picture |
| **GS** | generic stream |
| **GMAC** | gigabit media access control |
| **GND** | ground |
| **GPIO** | general purpose input/output |
| **GPL** | GNU general public license |
| **GPU** | graphics processing unit |

**H**

| | |
|---|---|
| **HBA** | host bus adapter |
| **HBP** | horizontal back porch |
| **HD** | high definition |
| **HDCP** | high-bandwidth digital content protection |
| **HDI** | high density interconnector |
| **HDMI** | high definition multimedia interface |
| **HFP** | horizontal front porch |
| **HIAO** | high-performance audio output interface |
| **HPW** | horizontal pulse width |
| **HSTL** | high speed transceiver logic |
| **HTML** | hypertext markup language |
| **HACT** | horizontal active area |
| **HFB** | horizontal front blank |
| **HL** | high level |
| **HLDC** | horizontal lens distortion correction |
| **HLE** | hardware locked error |
| **HNP** | host negotiation protocol |
| **HTO** | data starvation-by-host timeout |
| **HP** | high profile |
| **HSIC** | high-speed inter-chip |
| **HSS** | high-speed serializer/deserializer |
| **HTTP** | Hypertext Transfer Protocol |
| **HTTPS** | Hypertext Transfer Protocol Secure |
| **HVBB** | horizontal back blank |

**I**

| | |
|---|---|
| **I** | in-phase |
| **IBIS** | input/output buffer information specification |
| **IC** | integrated circuit |
| **$I^2C$** | inter-integrated circuit |
| **$I^2S$** | inter-IC sound |

| | |
|---|---|
| **I/O** | input/output |
| **IOC** | I/O configuration |
| **IP** | Internet Protocol |
| **ISI** | input stream identifier |
| **ISP** | image signal processor |
| **IDE** | integrated device electronic |
| **LDPC** | low density parity check code |
| **IDR** | intermediate data rate |
| **IF** | intermediate frequency |
| **IGMP** | Internet Group Management Protocol |
| **LMS** | linear mean square |
| **IPF** | IP filter |
| **IPv4** | Internet Protocol Version 4 |
| **IR** | infrared |
| **IRQ** | interrupt request |
| **ISI** | input stream identifier |
| **ISP** | image signal processor |
| **ISR** | interrupt service routine |
| **ITCM** | instruction tightly coupled memory |
| **ITLA** | integrated tunable laser assembly |
| **ITU** | International Telecommunication Union |
| **IV** | initialization vector |

**J**

| | |
|---|---|
| **JPEG** | Joint Photographic Experts Group |
| **JPGE** | JPEG encoder |
| **JTAG** | Joint Test Action Group |

**K**

| | |
|---|---|
| **KL** | key ladder |

**L**

| | |
|---|---|
| **LCD** | liquid crystal display |

| | |
|---|---|
| **LDO** | low dropout regulator |
| **LDPC** | low-density parity check code |
| **LED** | light emitting diode |
| **LFB** | line fill buffer |
| **LFSR** | linear feedback shifting register |
| **LMR** | load mode register |
| **LMS** | least mean square |
| **LNB** | low noise block |
| **LOS** | loss of signal |
| **LPI** | low-power idle |
| **LRB** | line read buffer |
| **LSB** | least significant bit |
| **LSP** | label switched path |
| **LSN** | logic sector number |
| **LTI** | luma transient improvement |
| **LVDS** | low-voltage differential signaling |
| **LVPECL** | low-voltage positive emitter coupled logic |
| **LVTTL** | low-voltage transistor-transistor logic |
| **LVPECL** | low-voltage positive emitter-coupled logic |

**M**

| | |
|---|---|
| **MAC** | media access control |
| **MBAFF** | macroblock adaptive frame field |
| **MCE** | media control engine |
| **MCU** | microprogrammed control unit |
| **MD** | motion detection |
| **MDDRC** | multiport DDRC |
| **MDIO** | management data input/output |
| **MDU** | motion detect unit |
| **MF** | matched filter |
| **MQFN** | mapped quad flat non-leaded |
| **MHL** | mobile high-definition link |
| **MII** | media independent interface |

| | |
|---|---|
| **MIPI** | mobile industry processor interface |
| **MIPS** | microprocessor without interlocked pipeline stages |
| **MLC** | multi-level cell |
| **MLF** | malformed |
| **MMB** | media memory block |
| **MMC** | multimedia card |
| **MMU** | memory management unit |
| **MMZ** | media memory zone |
| **MP** | main profile |
| **MPI** | MPP programming interface |
| **MPE** | media processing engine |
| **MPLL** | multiplying phase-locked loop |
| **MPP** | media processing platform |
| **MRL** | manually-operated retention latch |
| **MSB** | most significant bit |
| **MSE** | mean square error |
| **MSG** | message |
| **MV** | motion vector |

**N**

| | |
|---|---|
| **NAL** | network abstraction layer |
| **NANDC** | NAND flash controller |
| **NC** | not connect |
| **NCQ** | native command queuing |
| **NLP** | non-linear processor |
| **NR** | noise reduction |
| **NRZ** | non-return-to-zero |
| **NTSC** | National Television Systems Committee |
| **NVR** | network video recorder |

**O**

| | |
|---|---|
| **OCT** | on-chip termination |
| **OD** | open drain |

| | |
|---|---|
| **ODT** | on-die termination |
| **OEN** | output enable |
| **OFB** | output feedback |
| **OHCI** | open host controller interface |
| **OOB** | out of band |
| **OP** | operational amplifier |
| **OR** | original requirement |
| **OSC** | oscillator |
| **OSD** | on screen display |
| **OTG** | on-the-go |
| **OTP** | one time programmable |
| **OTU** | optical transponder unit |

**P**

| | |
|---|---|
| **PAD** | packet assembler/disassembler |
| **PAFF** | picture adaptive frame field |
| **PAL** | phase alternating line |
| **PCB** | printed circuit board |
| **PCI** | peripheral component interconnect |
| **PCIe** | peripheral component interconnect express |
| **PCIV** | PCI view |
| **PCR** | program clock reference |
| **PCM** | pulse code modulation |
| **PDM** | pulse density modulation |
| **PECL** | positive emitter coupled logic |
| **PER** | packet error rate |
| **PES** | packetized elementary stream |
| **PG** | power/ground |
| **PHY** | physical |
| **PID** | packet ID |
| **PIM-DM** | protocol independent multicast dense mode |
| **PIM-SM** | protocol independent multicast sparse mode |
| **PIO** | programmable input/output |

| | |
|---|---|
| **SSA** | secure software authentication |
| **PLL** | phase-locked loop |
| **PLS** | physical layer signaling |
| **PM** | port multiplexer |
| **PMoC** | power management of chip |
| **PMP** | personal media player |
| **POR** | power-on reset |
| **PPP** | Point-to-Point Protocol |
| **PPS** | picture parameter set |
| **PRBS** | pseudo random binary sequence |
| **PRDT** | physical region descriptor table |
| **PSI** | program specific information |
| **PSK** | phase shift keying |
| **PSRAM** | pseudo static random access memory |
| **RTCP** | Real-time Transport Control Protocol |
| **RTP** | Real-time Transport Protocol |
| **PT** | packet type |
| **PTS** | presentation time stamp |
| **PUB** | PHY utility block |
| **PUSI** | payload unit start indicator |
| **PWM** | pulse width modulation |

**Q**

| | |
|---|---|
| **Q** | quadrant |
| **QAM** | quadrature amplitude modulation |
| **QDR** | quad data rate |
| **QoS** | quality of service |
| **QP** | quantizer parameter |
| **QPSK** | quaternary phase shift keying |

**R**

| | |
|---|---|
| **RAM** | random access memory |
| **RAS** | row address signal |

| | |
|---|---|
| **RC** | resistor-capacitor |
| **RCA** | Radio Corporation of America |
| **RCRC** | response CRC error |
| **RE** | response error |
| **RF** | radio frequency |
| **RGB** | red-green-blue |
| **RGMII** | reduced gigabit media independent interface |
| **RH** | relative humidity |
| **RoHS** | restriction of the use of certain hazardous substances |
| **ROI** | region of interest |
| **ROM** | read-only memory |
| **ROP** | raster operation |
| **RPR** | resilient packet ring |
| **RLDRAM** | reduced latency dynamic random access memory |
| **RMII** | reduced media-independent interface |
| **RS** | Reed-Solomon |
| **RTC** | real-time clock |
| **RTO** | response timeout |
| **RTS** | request to send |
| **RVDS** | RealView development suite |
| **RX** | receive |
| **RXDR** | receive FIFO data request |

**S**

| | |
|---|---|
| **SAP** | service access point |
| **SAD** | sum of absolute difference |
| **SAR** | successive approximation |
| **SATA** | serial advanced technology attachment |
| **SAV** | start of active video |
| **SBE** | start-bit error |
| **SBP** | secure boot procedure |
| **SCD** | start code detect |
| **SCI** | smart card interface |

| | |
|---|---|
| **SCL** | serial clock |
| **SCR** | system clock reference |
| **SCS** | secure chipset start-up |
| **SCU** | snoop control unit |
| **SD** | secure digital |
| **SDA** | serial data |
| **SDB** | set device bits |
| **SDH** | synchronous digital hierarchy |
| **SDHC** | secure digital high capacity |
| **SDI** | serial digital interface |
| **SDIO** | secure digital input/output |
| **SDK** | software development kit |
| **SDRAM** | synchronous dynamic random access memory |
| **SDV** | system design verification |
| **SI** | specific information |
| **SIO** | sonic input/output |
| **SLC** | single-level cell |
| **SMI** | static memory interface |
| **SNAP** | subnetwork access point |
| **SNR** | signal-to-noise ratio |
| **SNTF** | serial ATA notification |
| **SOA** | semiconductor optical amplifier |
| **SoC** | system-on-chip |
| **SONET** | synchronous optical network |
| **SOP** | start of PES |
| **SP** | simple profile |
| **SPDIF** | Sony/Philips digital interface |
| **SPI** | serial peripheral interface |
| **SPS** | sequence parameter set |
| **SRAM** | static random access memory |
| **SRP** | Session Request Protocol |
| **SSA** | secure software authentication |
| **SSD** | secure software download |

| | |
|---|---|
| **SSMC** | synchronous static memory controller |
| **SSP** | synchronous serial port |
| **SSRAM** | synchronous static random access memory |
| **SSTL-18** | stub series terminated logic for 1.8 V |
| **STA** | station |
| **STB** | set-top box |
| **STM-1** | synchronous transport module level 1 |
| **SVB** | selective voltage bing |
| **SYNC** | synchronization |
| **SYS** | system |

**T**

| | |
|---|---|
| **TBD** | to be determined |
| **TBGA** | tape ball grid array |
| **TC** | traffic class |
| **TCP** | Transmission Control Protocol |
| **TD** | TLP digest |
| **TDES** | triple data encryption standard |
| **TDE** | two-dimensional engine |
| **TE** | tearing effect |
| **TEI** | transport error indicator |
| **TFD** | task file data |
| **TFPBGA** | tape fine-pitch ball grid array |
| **TFT** | thin-film technology |
| **TI** | Texas Instruments |
| **TLV** | type-length-value |
| **TOE** | TCP/IP offload engine |
| **TP** | transponder |
| **TPIT** | TS packet index table |
| **TR** | timing recovery |
| **TS** | transport stream |
| **TSI** | transport stream interface |
| **TT** | teletext |

| | |
|---|---|
| **TV** | television |
| **TVACT** | top vertical active area |
| **TVBB** | top vertical back blank |
| **TVFB** | top vertical front blank |
| **TVS** | transient voltage suppressor |
| **TX** | transmit |
| **TXDR** | transmit FIFO data request |

**U**

| | |
|---|---|
| **UART** | universal asynchronous receiver transmitter |
| **U-boot** | universal boot loader |
| **UC** | unexpected completion |
| **UDP** | User Datagram Protocol |
| **ULPI** | UTMI low pin interface |
| **UPnP** | universal plug and play |
| **UR** | unsupported request |
| **USB** | universal serial bus |
| **USIM** | universal subscriber identity module |
| **UTMI** | USB 2.0 transceiver macrocell interface |

**V**

| | |
|---|---|
| **VACT** | vertical active area |
| **VAD** | voice activity detector |
| **VAPU** | video analysis&process unit |
| **VBB** | vertical back blank |
| **VBI** | vertical blanking interval |
| **VBR** | variable bit rate |
| **VCC** | common connector voltage |
| **VCO** | voltage controller oscillator |
| **VCM** | variable coding and modulation |
| **VCMP** | video compress |
| **VCXO** | voltage control crystal oscillator |
| **VDA** | video detection analysis |

| | |
|---|---|
| **VDH** | video decoder for high-definition |
| **VDM** | video decoding module |
| **VDEC** | video decoding |
| **VDP** | video display |
| **VEDU** | video encoding/decoding unit |
| **VENC** | video encoding |
| **VFB** | vertical front blank |
| **VFMW** | video firmware |
| **VFP** | vertical front porch |
| **VGA** | video graphics array |
| **VI** | video input |
| **VIC** | vector interrupt controller |
| **VICAP** | video capture |
| **VIU** | video input unit |
| **VLD** | valid |
| **VLL** | virtual leased line |
| **VO** | video output |
| **VOIE** | voice encoder |
| **VOU** | video output unit |
| **VPP** | video pre-processing |
| **VPS** | video programming system |
| **VPSS** | video process subsystem |
| **VPW** | vertical pulse width |
| **VSA** | vertical sync start |
| **VQE** | voice quality enhancement |
| **VQM** | voice quality monitor |

**W**

| | |
|---|---|
| **WDG** | watchdog |
| **WE** | write enable |
| **WFE** | wait for event |
| **WFI** | wait for interrupt |
| **WRED** | weighted random early discard |

| | |
|---|---|
| **WSS** | wide screen signaling |

**X**

| | |
|---|---|
| **XAUI** | 10 gigabit attachment unit interface |

**Y**

| | |
|---|---|
| **YUV** | luminance-bandwidth-chrominance |

**Z**

| | |
|---|---|
| **ZME** | zoom engine |