Hi3130 V200 Demodulation and Decoding Processor

# Data Sheet

**Issue** **00B20**

**Date** **2013-07-11**

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# Contents

# About This Document

## Purpose

Hi3130 V200 is a cable digital TV channel receiver chipset. This document describes the features, logic architecture, QAM, operating mode, and hardware design of Hi3130 V200 for guiding user design.

## Related Version

The following table lists the product versions related to this document.

| Product Name | Version |
|---|---|
| Hi3130 | V200 |

## Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronics

## Symbol Conventions

The symbols that may be found in this document are defined as follows.

| Symbol | Description |
|---|---|
|  DANGER | Alerts you to a high risk hazard that could, if not avoided, result in serious injury or death. |
|  WARNING | Alerts you to a medium or low risk hazard that could, if not avoided, result in moderate or minor injury. |

| Symbol | Description |
|---|---|
| CAUTION | Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results. |
| TIP | Provides a tip that may help you solve a problem or save time. |
| NOTE | Provides additional information to emphasize or supplement important points in the main text. |

# Register Attributes

The register attributions that may be found in this document are defined as follows.

| Symbol | Description | Symbol | Description |
|---|---|---|---|
| RO | The register is read-only. | RW | The register is read/write. |
| RC | The register is cleared on a read. | WC | The register can be read.<br>The register is cleared when 1 is written.<br>The register keeps unchanged when 0 is written. |

# Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

# Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

| Type | Symbol | Value |
|---|---|---|
| Data capacity (such as the RAM capacity) | K | 1024 |
| | M | 1,048,576 |
| | G | 1,073,741,824 |
| Frequency, data rate | k | 1000 |

| Type | Symbol | Value |
|---|---|---|
| | M | 1,000,000 |
| | G | 1,000,000,000 |

The expressions of addresses and data are described as follows.

| Symbol | Example | Description |
|---|---|---|
| 0x | 0xFE04, 0x18 | Address or data in hexadecimal |
| 0b | 0b000, 0b00 00000000 | Data or sequence in binary (register description is excluded.) |
| X | 00X, 1XX | In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111. |

# Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

## Issue 00B20 (2013-07-11)

This issue is the first official release.

## Issue 00B10 (2012-12-30)

This issue is the reviewed draft release.

## Issue 00B01 (2012-07-17)

This issue is the first draft release.

# Contents

# Figures

# 1 Product Description

## 1.1 Introduction to Hi3130 V200

Hi3130 V200 is a cable digital TV channel demodulation and decoding chipset. It supports high-performance 16-/32-/64-/128-/256-QAM demodulation and forward error correction (FEC), which implement complete digital cable signal processing from sampling at the intermediate frequency (IF) to outputting MPEG-TSs. Hi3130 V200 complies with the DVB-C (ETS 300 429), ITU J83-A/C, and ITU J83-B standards.

Hi3130 V200 integrates a 12-bit and 40 Msps high-performance analog-to-digital converter (ADC), which ensures precise sampling of up to 256-QAM signals from the IF. After sampling, all the signals are processed in the digital domain. Based on the complex channel conditions, Hi3130 V200 supports demodulation, micro-reflection cancellation, and Reed-Solomon (RS) forward correction, and monitors signal quality to work with the decoder. It also provides two automatic gain control (AGC) outputs and two-wire buses to control the tuner, which simplifies the board design.

The MPEG-TSs output by Hi3130 V200 comply with standard DVB interfaces and can seamlessly connect to the MPEG decoder.

## 1.2 Key Specifications

Hi3130 V200 has the following features:

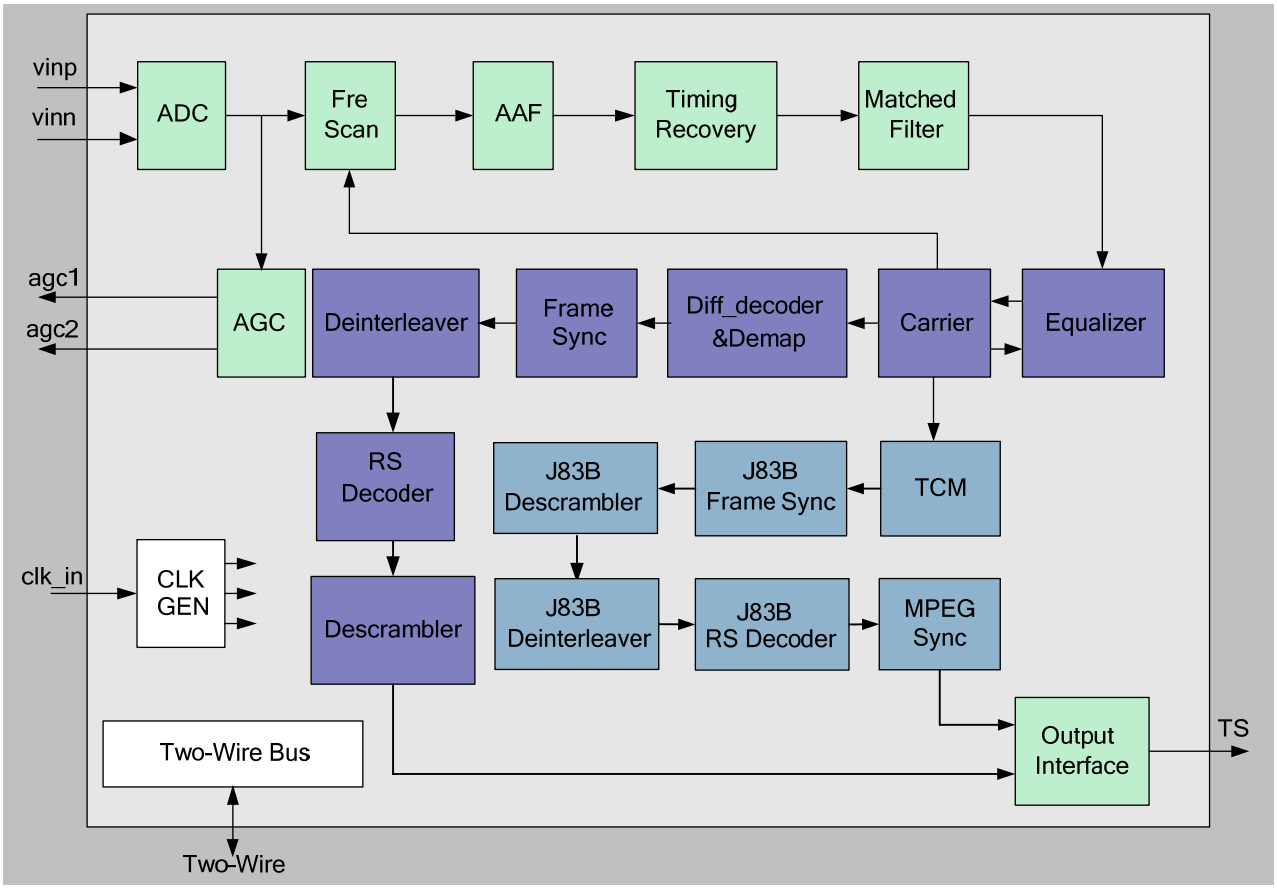
- Supports the DVB-C, ITU J83-A/C, and ITU J83-B standards.
- Supports 16-/32-/64-/128-/256-QAM demodulation.
- Integrates a 12-bit ADC to provide IF solutions and low-IF solutions.
- Supports adaptive digital down sampling, anti-aliasing filtering, and variable symbol rate ranging from 0.87 Msps to 7.19 Msps.
- Supports adaptive digital carrier recovery and a maximum of ±800 kHz frequency offset.
- Supports adaptive digital timing recovery and a maximum of 1% symbol rate deviation.
- Automatically selects the matched filter based on the bandwidth and supports the raised cosine roll-off factor ranging from 0.12 to 0.18.
- Supports adaptive blind equalization and decree feedback equalization to effectively correct micro-reflection and typical distortion in the cable channel.
- Integrates the FEC decoding functionality that complies with the ITU J83-A/C and ITU J83-B standards.

- Controls and monitors internal registers over two-wire buses.
- Monitors signal quality in real time.
- Outputs TSs in serial or parallel mode.
- Supports automatic spectrum inversion recognition and correction.
- Supports channel blind scanning.
- Integrates PLLs and requires only an external low-frequency passive crystal.
- Integrates a crystal oscillator circuit and internally generates the system clock by using the external passive crystal.
- Requires typical power consumption of 200 mW when the symbol rate is 6.9 Msps.
- Supports software-controlled power-saving mode.
- Uses the QFN40 package.
- Supports working voltage of 1.2 V or 3.3 V.

# 1.3 Logical Architecture

Figure 1-1 shows the logic architecture of Hi3130 V200.

**Figure 1-1** Logical architecture



# 1.4 Application Fields

Hi3130 V200 applies to:

- Cable tuner
- Cable STB and integrated digital TV
- Cable modem and digital TV card

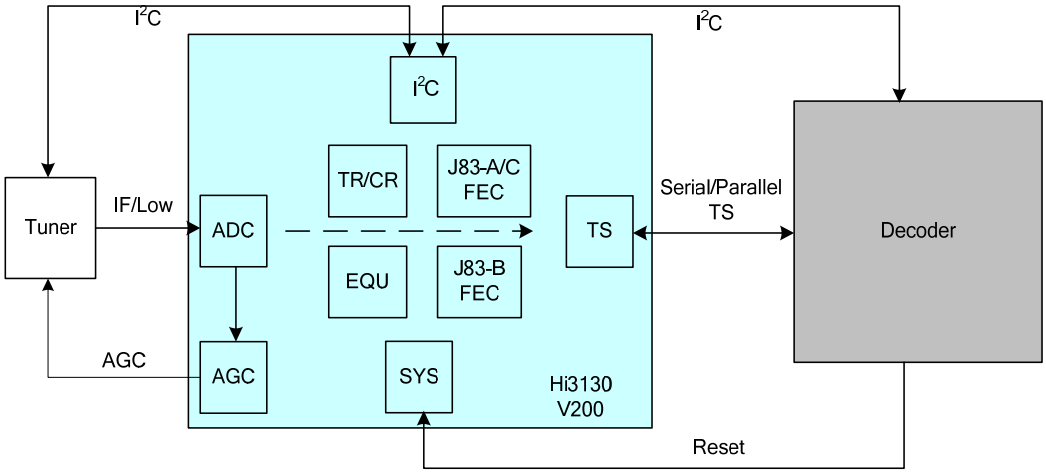
# 1.5 Typical Application

Figure 1-2 shows the typical application of Hi3130 V200. The radio frequency (RF) signals are converted into IF signals by the tuner and transmitted to Hi3130 V200. Hi3130 V200 performs timing recovery, carrier recovery, equalization, and FEC, and outputs standard TS packets to the decoder over the TS interface in parallel or serial mode.

Hi3130 V200 configures and controls the tuner and reads the tuner status over the $I^2C$ interface. The integrated ADC converts the IF or low- IF signals input by the tuner into digital signals, and outputs one or two AGC signals for controlling the IF and RF gains of the tuner.

The decoder configures drivers and reads Hi3130 V200 status over the $I^2C$ interface, and resets Hi3130 V200 over the reset interface after Hi3130 V200 is powered on.

**Figure 1-2** Typical application



# Contents

# Figures

# Tables

# 2 Function Description

## 2.1 ADC

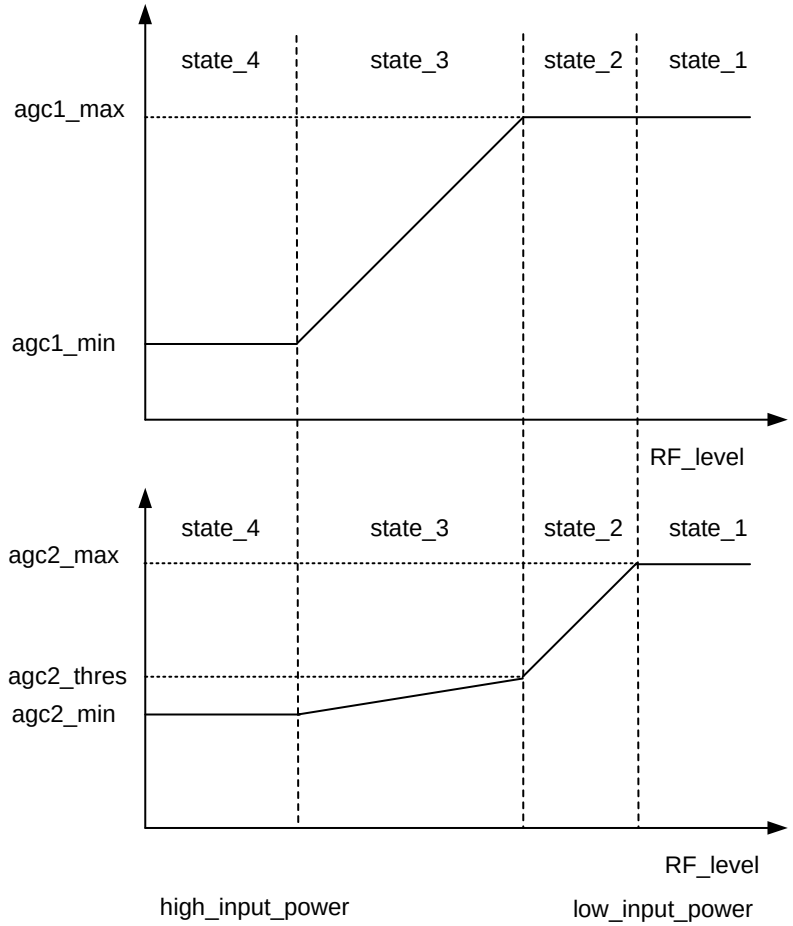
Hi3130 V200 integrates a high-precision 12-bit ADC that supports a maximum of 40 MHz sampling frequency. The ADC can directly sample intermediate frequency (IF) signals output by the front-end tuner. The ADC works in differential input mode. The signal input voltage is 1.0 $V_{p-p}$ and the common-mode voltage is internally generated.

## 2.2 AGC

The QAM module provides two automatic gain control (AGC) output signals: AGC1 and AGC2. AGC1 controls the radio frequency (RF) gain of the tuner and AGC2 controls the IF gain. The AGC compares the average power consumption during ADC sampling with the reference power consumption to obtain two gain control signals. After being transmitted to the Sigma-Delta DAC, the gain control signals are converted into two PWM signals. The analog gain control level is generated after the PWM signals are transmitted to the off-chip resistor-capacitor (RC) filter.

Figure 2-1 demonstrates the AGC working principle.

**Figure 2-1** AGC working principle




The AGC supports two operating modes: dual-AGC mode and separate IF AGC mode. In dual-AGC mode, AGC1 and AGC2 work from initial values. That is, AGC1 and AGC2 work from state_2 and retain in state_2 or switch to state_3. The AGC switch register controls the switch between state_2 to state_3. In state_2 and state_3, the rate variances of AGC1 and AGC2 depend on the configured gain adjustment step. For details about other configurations, see the descriptions of AGC and BAGC registers.

# 2.3 Down Conversion and Frequency Scanning

The signal $f_{Tuner}$ centered on the tuner IF is subsampled and then down-converted by the ADC (the sampling clock is $f_{ckext}$). The down-converted signal is centered on the sampled IF $f_1$.

$$f1 = f_{Tuner} - f_{ckext} \quad (1\text{-}1)$$

where

- $f_1$ = 7.2 MHz
- $f_{Tuner}$ = 36 MHz
- $f_{ckext}$ = 28.8 MHz

The frequency offset transfer module works closely with the frequency scanning module to automatically scan channels. The demodulation frequency is incremented from the specified value based on a specified step. You can set the interval between steps, determines whether to automatically stop scanning channels when the chip detects the locked status, or completely controls frequency scanning.

## 2.4 AAF

The anti-aliasing filter (AAF) is used to remove aliasing generated during ADC sampling and perform down sampling at a symbol rate.

## 2.5 Timing Recovery Module

The timing recovery module is used to estimate and correct the clock errors at the RX end, obtaining the optimum sampling time at the RX end.

The timing recovery module consists of a clock error detector, a loop filter, and an interpolator. The interpolator performs interpolation operations on the baseband signals at the optimum time to obtain a correct sampling value. The loop filter parameters can be set by configuring tr_ctrl_2 to tr_ctrl_6.

## 2.6 Matched Filter

The matched filter is a raised cosine filter and its roll-off factor ranges from 0.12 to 0.18. This filter is used to perform matched filtering on baseband signals.

## 2.7 Equalizer and Carrier Recovery Module

The equalizer eliminates the influences caused by echoes and linear channel distortion based on the blind equalization algorithm and decree feedback equalization algorithm.

The carrier recovery module traces and compensates the frequency offset and phase offset of the carrier. Different loop parameters are used in the acquisition status and trace status, which brings high acquisition bandwidth but small trace errors.

## 2.8 Demap and Differential Decoder

According to the DVB-C and ITU J83-A/C standards, the demap and differential decoder implements differential decoding and demapping and converts symbol streams into byte streams. The subsequent modules process streams by byte. 16-QAM, 32-QAM, 64-QAM, 128-QAM, and 256-QAM correspond to 4-bit, 5-bit, 6-bit, 7-bit, and 8-bit symbols respectively.

# 2.9 Frame Sync Module

The frame sync module detects the sync bytes (0x47 and 0xB8) in TSs to provide frame start signals for subsequent modules.

# 2.10 Deinterleaver

At the TX end, data is interleaved after Reed-Solomon (RS) encoding to avoid continuous bit errors due to burst interference and avoid information inaccuracy due to inadequate RS correction range. After interleaving, the sequence of transferring signals is changed and the continuous bit errors are separated. In this way, the protection against burst bit errors is improved. At the RX end, data must be restored by the deinterleaver before RS decoding.

According to the DVB-C and ITU J83-A/C standards, the interleave depth of the channel demodulation and decoding chip is 12. The interleaver can be bypassed by configuring internal registers.

# 2.11 RS Decoder

According to the DVB-C and ITU J83-A/C standards, the RS decoder implements channel correction. The length of each input data packet is 204 bytes (including 16-byte check words). A maximum of 8-byte errors can be corrected.

The correction function of the RS decoder can be bypassed by configuring ts_ctrl_1[bend_bypass] to facilitate the evaluation of the bit error rate (BER) before RS.

# 2.12 Descrambler

According to the DVB-C and ITU J83-A/C standards, the descrambling polynomial for the RX end is $1 + x^{14} + x^{15}$ and the initialization sequence of the descrambler is 100101010000000.

The descrambler starts after the reversible synchronization header (0xB8) of a TS packet is detected. Then the descrambler performs the following operations on every eight TS packets: configures ts_ctrl_1[sync_byte_inv] to revert or retain the reversible synchronization word of the first TS packet (0xB8 is reverted to 0x47), retains the packet headers (0x47) of other TS packets, and descrambles all other bytes in frames.

# 2.13 Channel Blind Scanning

Hi3130 V200 supports automatic spectrum inversion recognition and correction and channel blind scanning.

Automatic spectrum inversion can be disabled by configuring registers. You can configure the current spectrum status based on the channel conditions.

Channel blind scanning applies to the following cases:

- Queries the signal symbol rate when the modulation mode is known.

- Queries the modulation mode when the signal symbol rate is known.
- Queries both the modulation mode and signal symbol rate with the aid of software.

The symbol rate query range is 3.6 Mbuad to 6.9 Mbaud. If channel blind scanning is disabled by configuring registers, the current modulation mode and signal symbol rate must be manually configured.

# 2.14 J83B TCM Module

The trellis coding modulation (TCM) module uses the Viterbi algorithm. It searches for the path with the minimum metric based on the forward-processed data and hard-decision data, decodes the data processed by using the Viterbi algorithm to generate the data corresponding to constellation points, and outputs serial data in the sequence defined in the J83B standard. For 64 QAM, 28-bit data is output each time for every five input symbols; for 256 QAM, 38-bit data is output each time for every five input symbols.

# 2.15 J83B Frame Sync Module

The J83B frame sync module detects the sync bytes in TSs. In normal mode, it synchronizes data (including identifying sync feature sequences) and outputs symbols in parallel, 4-bit control bit words in the trailer, and locked or unlocked signals.

# 2.16 J83B Descrambler

According to the ITU J83-B standard, the descrambling polynomial at the RX end is x^3 + x + α^3. The descrambler processes all input valid payloads at random. It outputs the trailer directly without processing.

# 2.17 J83B Deinterleaver

At the TX end, data is interleaved after RS encoding to avoid continuous bit errors due to burst interference and avoid information inaccuracy due to inadequate RS correction range. After interleaving, the sequence of transferring signals is changed and the continuous bit errors are separated. In this way, the protection against burst bit errors is improved. At the RX end, data must be restored by the deinterleaver before RS decoding.

According to the ITU J83B standard, the interleaver of the forward error correction (FEC) encoder is a convolutional interleaver. It supports the interleaving modes of 128x1, 128x2, 128x3, 128x4, 64x2, 32x4, 16x8, and 8x16.

# 2.18 J83B RS Decoder

The J83B RS decoder supports decoding of the data processed by the FEC encoder. It decodes the input 128-symbol frames and corrects or detects errors. The J83B RS decoder can correct a maximum of three-symbol errors each time and output the data after error correction. If the

number of errors is greater than three, the decoder identifies the excessive errors but does not correct them.

# 2.19 J83B MPEG Frame Sync Module

The J83B MPEG frame sync module detects the synchronization bytes in TSs. In normal mode, it synchronizes data and outputs bytes in parallel.

# 2.20 Monitoring the Signal Quality

## BER Statistics

The internal BER status registers ber_2, ber_3, and ber_4 of Hi3130 V200 provide statistics on error bits or bytes before RS correction. You can select auto-stop statistical mode or auto-repeat statistical mode.

- Auto-stop statistical mode

**NOTE**

In this mode, ber_1[err_mode] must be set to 0.

To conduct a BER test in auto-stop statistical mode, perform the following steps:

**Step 1** Set ber_1[bert_en] to 0 to disable the BER test.

**Step 2** Configure ber_1[nbyte] to set a statistics interval. The statistics interval indicates that bit errors are counted within a certain number of output data segments.

**Step 3** Set ber_1[err_mode] to 0 to select the auto-stop statistical mode.

**Step 4** Configure ber_1[err_source] to set the statistical unit to bit or byte.

**Step 5** Set ber_1[bert_en] to 1 to start the BER test. The counter starts after being cleared.

**Step 6** After a statistics interval, the counter stops counting and ber_1[bert_en] is automatically cleared. The statistical results are stored in ber_2–ber_4[error_cnt].

**----End**

The BER is calculated as follows:

$$\text{Byte error rate} = \frac{error\_cnt}{2^{2 \times nbyte+12}}$$

$$\text{Bit error rate} = \frac{error\_cnt}{8 \times 2^{2 \times nbyte+12}}$$

When the BER is high, an overflow may occur in the counter. During the statistical interval, if overflows occur in the counters ber_2[error_cnt] to ber_4[error_cnt], the maximum value is retained.

The statistical error data is stored in ber_2[error_cnt] to ber_4[error_cnt]. You can read the data for the BER test.

- Auto-repeat statistical mode

**NOTE**

In this mode, ber_1[err_mode] must be set to 1.

To conduct a BER test in auto-repeat statistical mode, perform the following steps:

**Step 1** Set ber_1[bert_en] to 0 to disable the BER test.

**Step 2** Configure ber_1[nbyte] to set a statistics interval. The statistics interval indicates that bit errors are counted within a certain number of output data segments.

**Step 3** Set ber_1[err_mode] to 1 to select the auto-repeat statistical mode.

**Step 4** Configure ber_1[err_source] to set the statistical unit to bit or byte.

**Step 5** Set ber_1[bert_en] to 1 to start the BER test. The counter starts after being cleared.

**Step 6** Set ber_1[bert_en] to 0 to stop the counter.

**----End**

If an overflow occurs in the counter during the test, the maximum value is retained.

When a statistical interval is reached, the counter restarts to count after being cleared and stores statistical results in registers. In auto-repeat statistical mode, software can read data from BER registers any time. The counter stops counting only after ber_1[bert_en] is set to 0.

**NOTE**

Before reading the BER status registers, you must write a value to cr_ctrl_21.

## PER Statistics

The packet error rate (PER) statistics use the same statistical interval register (ber_1[nbyte]) and statistical enable register (ber_1[bert_en]) as the BER statistics.

When the counter reaches the statistical threshold, the total packet count, uncorrectable packet count, and correctable packet count are stored in the retain register. You can read the rs_ctrl register and calculate the PER.

To calculate the PER, perform the following steps:

**Step 1** Write a value to cr_ctrl_21.

**Step 2** Read rs_ctrl_1 and rs_ctrl_2 to obtain the total packet count. The number of total packets is calculated as follows:

pkt_total = rs_ctrl_1 << 8 + rs_ctrl_2

**Step 3** Read rs_ctrl_5 and rs_ctrl_6 to obtain the total error packet count. The number of total error packets is calculated as follows:

pkt_err = rs_ctrl_5 << 8 + rs_ctrl_6

**Step 4** Calculate the PER in the statistical interval as follows:

PER = pkt_err/pkt_total

**----End**

### SNR Estimation

Hi3130 V200 provides two signal-to-noise ratio (SNR) estimation registers equ_stat_2 and equ_stat_3. Their values reflect the average distance between the calculated constellation point and the mapped constellation point. In addition, a lookup table is used to calculate the equivalent noise level (equivalent C/N estimation) to estimate the signal quality.

## 2.21 TS Output Interface

Hi3130 V200 provides two MPEG2-TS output modes: parallel mode, serial mode.

The signals from the TS output interface include the data signal ts_dat[7:0], clock signal ts_clk, data validity signal ts_val, sync header signal ts_sync, and frame error signal ts_err.

- ts_dat: TS frame data signal (In the serial mode, ts_dat[0] is TS output.)
- ts_clk: data clock signal. The polarity is programmable. The signal can be output continuously or discontinuously in different modes.
- ts_val: TS frame data validity signal (Bytes are valid in parallel mode, and bits are valid in serial mode.)
- ts_sync: TS frame sync validity flag signal, which identifies the data frame header (Bytes are valid in parallel mode, and bits are valid in serial mode.)
- ts_err: TS frame error signal. It is set to 1 when TS frames with errors that cannot be corrected by RS decoding are output.

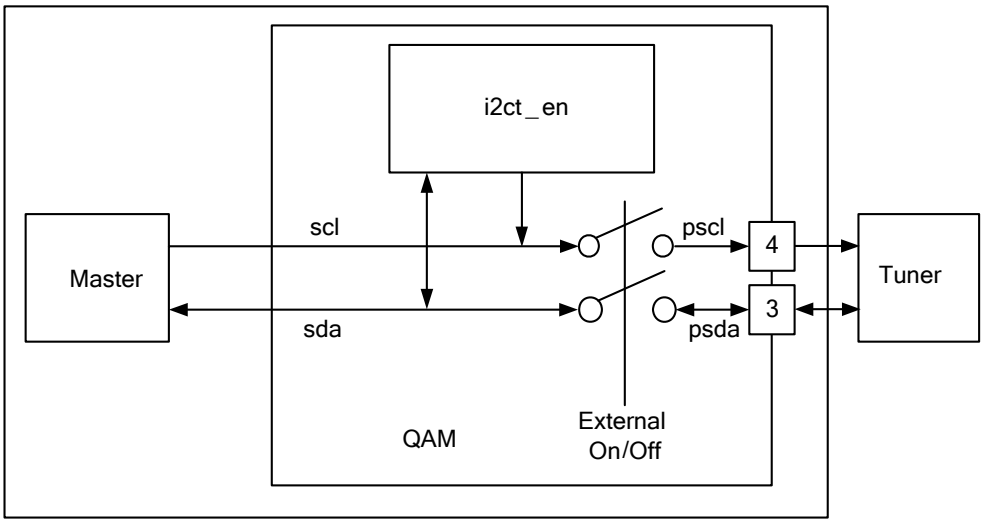
The TS output interface is configured by configuring ts_ctrl_1 and ts_ctrl_2.

## 2.22 Two-Wire Bus Interface

The QAM module accesses internal registers and external tuner registers by using a two-wire bus. Before the QAM accesses tuner registers, mctrl_7[i2ct_en] must be set to 1. After the access, the QAM module automatically clears mctrl_7[i2ct_en]. That is, the QAM returns to the mode of accessing internal registers of the QAM module.

Figure 2-2 shows the connection between Hi3130 V200 and an external tuner over a two-wire bus.

**Figure 2-2** Connection between Hi3130 V200 and an external tuner over a two-wire bus




# 2.23 Register Configuration

Bit 1 and bit 0 of four_reg_sel (0xE0) are the control signals of register select. Therefore, you have to confirm whether four_reg_sel bit[1:0] are mapped to the register to be configured before configuring a register.

The definitions of four_reg_sel bit[1:0] are as follows:

- 2'b00: QAM register configuration
- 2'b10: system control register configuration
- Other values: reserved

For example, to configure the system control register (0x03), perform the following steps:

**Step 1** Set the lower two bits of 0xE0 to 2'b10.

**Step 2** Set 0x03 to the specified value.

**----End**

# 2.24 QAM Register Summary

Table 2-1 describes QAM registers.

**Table 2-1** QAM register summary (base address = 0x0000_0000)

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x02 | equ_ctrl_3 | Equalization control register 3 | 2-13 |
| 0x0A | equ_stat_2 | Equalization status register 2 | 2-13 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x0B | equ_stat_3 | Equalization status register 3 | 2-14 |
| 0x10 | tr_ctrl_2 | TIMING RECOVERY control register 2 | 2-14 |
| 0x11 | tr_ctrl_4 | Timing recovery control register 4 | 2-15 |
| 0x12 | tr_ctrl_5 | Timing recovery control register 5 | 2-15 |
| 0x13 | tr_ctrl_6 | Timing recovery control register 6 | 2-16 |
| 0x14 | tr_ctrl_8 | Timing recovery control register 8 | 2-16 |
| 0x15 | tr_ctrl_9 | Timing recovery control register 9 | 2-17 |
| 0x16 | tr_ctrl_10 | Timing recovery control register 10 | 2-17 |
| 0x1A | tr_stat_1 | Timing recovery status register 1 | 2-18 |
| 0x1B | tr_stat_2 | Timing recovery status register 2 | 2-18 |
| 0x25 | cr_ctrl_21 | Carrier recovery control register 21 | 2-18 |
| 0x26 | cr_ctrl_22 | Carrier recovery control register 22 | 2-19 |
| 0x27 | cr_ctrl_23 | Carrier recovery control register 23 | 2-19 |
| 0x28 | cr_ctrl_24 | Carrier recovery control register 24 | 2-19 |
| 0x29 | cr_ctrl_25 | Carrier recovery control register 25 | 2-20 |
| 0x32 | cr_stat_4 | Carrier recovery status register 4 | 2-20 |
| 0x33 | cr_stat_5 | Carrier recovery status register 5 | 2-21 |
| 0x34 | cr_stat_6 | Carrier recovery status register 6 | 2-21 |
| 0x35 | cr_stat_7 | Carrier recovery status register 7 | 2-21 |
| 0x36 | j83b_tcm_1 | J83B TCM control register 1 | 2-22 |
| 0x37 | j83b_tcm_2 | J83B TCM control register 2 | 2-22 |
| 0x38 | j83b_tcm_3 | J83B TCM control register 3 | 2-23 |
| 0x39 | j83b_tcm_4 | J83B TCM control register 4 | 2-23 |
| 0x3A | j83b_tcm_5 | J83B TCM control register 5 | 2-23 |
| 0x3B | j83b_tcm_6 | J83B TCM status register 6 | 2-24 |
| 0x3C | j83b_di_1 | J83B deinterleaving control register 1 | 2-24 |
| 0x3D | j83b_di_2 | J83B deinterleaving control register 2 | 2-25 |
| 0x3E | j83b_mfsync_1 | J83B MPEG frame sync control register 1 | 2-25 |
| 0x3F | j83b_mfsync_2 | J83B MPEG frame sync status register 2 | 2-26 |
| 0x40 | mctrl_1 | Main control register 1 | 2-27 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x44 | mctrl_5 | Main control register 5 | 2-28 |
| 0x45 | mctrl_6 | Main control register 6 | 2-29 |
| 0x46 | mctrl_7 | Main control register 7 | 2-30 |
| 0x48 | mctrl_9 | Main control register 9 | 2-31 |
| 0x4A | mctrl_11 | Main control register 11 | 2-31 |
| 0x59 | agc_ctrl_15 | AGC control register 15 | 2-32 |
| 0x5C | agc_ctrl_19 | AGC control register 19 | 2-33 |
| 0x5D | agc_ctrl_20 | AGC control register 20 | 2-34 |
| 0x5F | agc_ctrl_22 | AGC control register 22 | 2-34 |
| 0x60 | bagc_ctrl_1 | BAGC control register 1 | 2-34 |
| 0x61 | bagc_ctrl_2 | BAGC control register 2 | 2-35 |
| 0x62 | bagc_ctrl_3 | BAGC control register 3 | 2-35 |
| 0x65 | bagc_ctrl_6 | BAGC control register 6 | 2-36 |
| 0x68 | bagc_ctrl_9 | BAGC control register 9 | 2-36 |
| 0x69 | bagc_ctrl_10 | BAGC control register 10 | 2-36 |
| 0x6B | bagc_ctrl_12 | BAGC control register 12 | 2-37 |
| 0x6E | bagc_ctrl_13 | BAGC control register 13 | 2-37 |
| 0x6F | bagc_ctrl_14 | BAGC control register 14 | 2-37 |
| 0x70 | bagc_stat_1 | BAGC status register 1 | 2-38 |
| 0x71 | bagc_stat_2 | BAGC status register 2 | 2-38 |
| 0x72 | bagc_stat_3 | BAGC status register 3 | 2-39 |
| 0x73 | bagc_stat_4 | BAGC status register 4 | 2-39 |
| 0x79 | bagc_stat_7 | BAGC status register 7 | 2-39 |
| 0x7C | j83b_tcm_ber0 | J83B TCM status register 0 | 2-40 |
| 0x7D | j83b_tcm_ber1 | J83B TCM status register 1 | 2-40 |
| 0x7E | j83b_tcm_ber2 | J83B TCM status register 2 | 2-40 |
| 0x7F | j83b_tcm_ber3 | J83B TCM status register 3 | 2-41 |
| 0x87 | sfreq_agc1_init | AGC control register | 2-41 |
| 0x90 | sync_ctrl_1 | Frame sync control register 1 | 2-42 |
| 0x93 | ber_1 | BER control register 1 | 2-42 |
| 0x94 | ber_2 | BER status register 2 | 2-43 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x95 | ber_3 | BER status register 3 | 2-44 |
| 0x96 | ber_4 | BER status register 4 | 2-44 |
| 0x98 | ts_ctrl_1 | Output control register 1 | 2-44 |
| 0x99 | ts_ctrl_2 | Output control register 2 | 2-45 |
| 0x9B | rs_ctrl_1 | RS decoding control register 1 | 2-46 |
| 0x9C | rs_ctrl_2 | RS decoding control register 2 | 2-47 |
| 0x9D | rs_ctrl_3 | RS decoding control register 3 | 2-47 |
| 0x9E | rs_ctrl_4 | RS decoding control register 4 | 2-47 |
| 0x9F | rs_ctrl_5 | RS decoding control register 5 | 2-48 |
| 0xA0 | rs_ctrl_6 | RS decoding control register 6 | 2-48 |
| 0xA1 | rs_ctrl_8 | RS decoding control register 8 | 2-49 |
| 0xA6 | bs_ctrl_1 | Blind scanning control register 1 | 2-50 |
| 0xA7 | bs_ctrl_2 | Blind scanning control register 2 | 2-51 |
| 0xAC | bs_stat_1 | Blind scanning status register 1 | 2-52 |
| 0xAD | bs_stat_2 | Blind scanning status register 2 | 2-53 |
| 0xAE | bs_stat_3 | Blind scanning status register 3 | 2-53 |
| 0xAF | bs_stat_4 | Blind scanning status register 4 | 2-54 |
| 0xB0 | bs_stat_5 | Blind scanning status register 5 | 2-54 |
| 0xB1 | fs_ctrl_1 | Scanning control register 1 | 2-55 |
| 0xB2 | fs_ctrl_2 | Scanning control register 2 | 2-55 |
| 0xB4 | fs_ctrl_4 | Scanning control register 4 | 2-56 |
| 0xB5 | fs_ctrl_5 | Scanning control register 5 | 2-56 |
| 0xB6 | fs_ctrl_6 | Scanning control register 6 | 2-57 |
| 0xB7 | fs_ctrl_7 | Scanning control register 7 | 2-57 |
| 0xB8 | fs_stat_1 | Scanning status register 1 | 2-58 |
| 0xB9 | fs_stat_2 | Scanning status register 2 | 2-58 |
| 0xBA | j83b_ffsync_1 | J83B FFSYNC control register 1 | 2-58 |
| 0xBB | j83b_ffsync_2 | J83B FFSYNC control register 2 | 2-59 |
| 0xBC | j83b_ffsync_3 | J83B FFSYNC control register 3 | 2-59 |
| 0xBD | j83b_dr_1 | J83B descrambling control register 1 | 2-60 |
| 0xBE | j83b_dr_2 | J83B descrambling control register 2 | 2-60 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0xBF | j83b_dr_3 | J83B descrambling control register 3 | 2-60 |
| 0xE0 | four_reg_sel | Register block select register | 2-61 |

# 2.25 QAM Register Description

## equ_ctrl_3

equ_ctrl_3 is equalization control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x02 | equ_ctrl_3 | 0x20 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | step_lms | | | | step_blind | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | step_lms | Equalizer step in least mean square (LMS) mode. It is set to 0x0–0x7 in normal cases. |
| [3:0] | RW | step_blind | Equalizer step in blind mode. It is set to 0x0–0x7 in normal cases. |

## equ_stat_2

equ_stat_2 is equalization status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0A | equ_stat_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | noise_cal | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | noise_cal | Upper eight bits of the internal noise estimation accumulator.<br>The accumulator value is related to the dispersion degree of the constellation diagram. The value reflects the average distance between the calculated constellation point and the mapped constellation point. A lookup table is used to calculate equivalent noise level (equivalent C/N estimation).<br>For details, see the description of cr_ctrl_21. |

## equ_stat_3

equ_stat_3 is equalization status register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x0B | equ_stat_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | noise_cal | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | noise_cal | Lower eight bits of the internal noise estimation accumulator.<br>The accumulator value is related to the dispersion degree of the constellation diagram. The value reflects the average distance between the calculated constellation point and the mapped constellation point. A lookup table is used to calculate equivalent noise level (equivalent C/N estimation).<br>For details, see the description of cr_ctrl_21. |

## tr_ctrl_2

tr_ctrl_2 is timing recovery control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x10 | tr_ctrl_2 | 0xA0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | t_gain_int | | | | | | | |
| Reset | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | t_gain_int | Lower eight bits of the integration tributary gain for the timing recovery module in acquisition mode.<br>A larger value indicates higher loop bandwidth and a smaller damping coefficient. |

## tr_ctrl_4

tr_ctrl_4 is timing recovery control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x11 | tr_ctrl_4 | 0x7C |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | t_gain_dir | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | t_gain_dir | Lower eight bits of the direct tributary gain for the timing recovery module in acquisition mode.<br>A larger value indicates a larger loop damping coefficient. |

## tr_ctrl_5

tr_ctrl_5 is timing recovery control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x12 | tr_ctrl_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | t_gain_int | reserved | | | t_gain_dir |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [4] | RW | t_gain_int | Upper bits of the integration tributary gain for the timing recovery module in acquisition mode. |
| [3:1] | - | reserved | Reserved. |
| [0] | RW | t_gain_dir | Upper bits of the direct tributary gain for the timing recovery module in acquisition mode. |

## tr_ctrl_6

tr_ctrl_6 is timing recovery control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x13 | tr_ctrl_6 | 0x76 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | t_gain_int2 | | | reserved | t_gain_dir2 | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:4] | RW | t_gain_int2 | Attenuation coefficient of the integration tributary gain for the timing recovery module in trace mode. |
| [3] | - | reserved | Reserved. |
| [2:0] | RW | t_gain_dir2 | Attenuation coefficient of the direct tributary gain for the timing recovery module in trace mode. |

## tr_ctrl_8

tr_ctrl_8 is timing recovery control register 8.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x14 | tr_ctrl_8 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | itpl_ratio | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [2:0] | RW | itpl_ratio | Upper three bits of the ratio of the AD sampling frequency $F_{sample}$ to the symbol rate $F_{symbol}$. The ratio is calculated as follows:<br>$Ratio = \frac{F_{sample}}{2 \times F_{symbol}} \times 2^{14}$ |

## tr_ctrl_9

tr_ctrl_9 is timing recovery control register 9.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x15 | tr_ctrl_9 | 0x86 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | itpl_ratio | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | itpl_ratio | Middle eight bits of the ratio of the AD sampling frequency $F_{sample}$ to the symbol rate $F_{symbol}$. The ratio is calculated as follows:<br>$Ratio = \frac{F_{sample}}{2 \times F_{symbol}} \times 2^{14}$ |

## tr_ctrl_10

tr_ctrl_10 is timing recovery control register 10.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x16 | tr_ctrl_10 | 0x0D |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | itpl_ratio | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | itpl_ratio | Lower eight bits of the ratio of the AD sampling frequency $F_{sample}$ to the symbol rate $F_{symbol}$. The ratio is calculated as follows:<br>The ratio is calculated as follows:<br>$Ratio = \frac{F_{sample}}{2 \times F_{symbol}} \times 2^{14}$ |

## tr_stat_1

tr_stat_1 is timing recovery status register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1A | tr_stat_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | t_offset_est | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | t_offset_est | Upper eight bits of the frequency offset of the symbol clock. For details, see the description of cr_ctrl_21. |

## tr_stat_2

tr_stat_2 is timing recovery status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1B | tr_stat_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | t_offset_est | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | t_offset_est | Lower eight bits of the frequency offset of the symbol clock. For details, see the description of cr_ctrl_21. |

## cr_ctrl_21

cr_ctrl_21 is carrier recovery control register 21.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x25 | cr_ctrl_21 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | crl_snapshot | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | crl_snapshot | Before reading an RO register with more than eight bits (such as t_offset_est), you need to write a value to cr_ctrl_21. Otherwise, the value read from the register is uncertain. |

## cr_ctrl_22

cr_ctrl_22 is carrier recovery control register 22.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x26 | cr_ctrl_22 | 0x17 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | f_gain_dir | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:0] | RW | f_gain_dir | Upper five bits of the direct tributary gain of the carrier recovery module in reduced acquisition mode. |

## cr_ctrl_23

cr_ctrl_23 is carrier recovery control register 23.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x27 | cr_ctrl_23 | 0x7D |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | f_gain_dir | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | f_gain_dir | Lower eight bits of the direct tributary gain of the carrier recovery module in reduced acquisition mode. |

## cr_ctrl_24

cr_ctrl_24 is carrier recovery control register 24.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x28 | cr_ctrl_24 | 0x0F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | f_gain_int | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4:0] | RW | f_gain_int | Upper five bits of the integration tributary gain of the carrier recovery module in reduced acquisition mode. |

## cr_ctrl_25

cr_ctrl_25 is carrier recovery control register 25.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x29 | cr_ctrl_25 | 0x65 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | f_gain_int | | | | | | | |
| Reset | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | f_gain_int | Lower eight bits of the integration tributary gain of the carrier recovery module in reduced acquisition mode. |

## cr_stat_4

cr_stat_4 is carrier recovery status register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x32 | cr_stat_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | f_offset_est | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:0] | RO | f_offset_est | Uppermost four bits of the demodulation frequency offset.<br>For details, see the description of cr_ctrl_21. |

## cr_stat_5

cr_stat_5 is carrier recovery status register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x33 | cr_stat_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | f_offset_est | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | f_offset_est | Upper eight bits of the demodulation frequency offset.<br>For details, see the description of cr_ctrl_21. |

## cr_stat_6

cr_stat_6 is carrier recovery status register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x34 | cr_stat_6 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | f_offset_est | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | f_offset_est | Middle eight bits of the demodulation frequency offset.<br>For details, see the description of cr_ctrl_21. |

## cr_stat_7

cr_stat_7 is carrier recovery status register 7.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x35 | cr_stat_7 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | f_offset_est | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | f_offset_est | Lowest eight bits of the demodulation frequency offset.<br>For details, see the description of cr_ctrl_21. |

## j83b_tcm_1

j83b_tcm_1 is J83B TCM control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x36 | j83b_tcm_1 | 0x08 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | reg2j83b_auto | reg2j83b_phase | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3] | RW | reg2j83b_auto | Whether TCM automatically searches for the phase to initialize the configuration in J83B mode.<br>1: automatic search<br>1: manual configuration |
| [2:0] | RW | reg2j83b_phase | TCM phase that is manually configured in J83B mode. |

## j83b_tcm_2

j83b_tcm_2 is J83B TCM control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x37 | j83b_tcm_2 | 0x7F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2j83b_thres | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | reg2j83b_thres | TCM lock threshold in J83B mode. |

## j83b_tcm_3

j83b_tcm_3 is J83B TCM control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x38 | j83b_tcm_3 | 0x91 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2j83b_lost_num | | | reg2j83b_syncnum | | | reg2j83b_stanum | |
| Reset | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | reg2j83b_lost_num | TCM unlock count in J83B mode. When this count is reached, the TCM unlock status is reported. The value 0 indicates that the unlock status is reported when the TCM is unlocked once, the value 1 indicates that the unlock status is reported when the TCM is unlocked twice, and so on. |
| [4:2] | RW | reg2j83b_syncnum | TCM sync count in J83B mode. When the count is reached, the TCM is locked. The value 0 indicates that the TCM is locked after the TCM is synchronized once, the value 1 indicates that the TCM is locked after the TCM is synchronized twice, and so on. |
| [1:0] | RW | reg2j83b_stanum | Number of TCM sync symbols in J83B mode. It is calculated as follows: 256 << mc2tcm _stacnt x 15. |

## j83b_tcm_4

j83b_tcm_4 is J83B TCM control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x39 | j83b_tcm_4 | 0x32 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2j83b_hold_thres | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | reg2j83b_hold_thres | TCM unlock threshold in J83B mode. |

## j83b_tcm_5

j83b_tcm_5 is J83B TCM control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3A | j83b_tcm_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | tcm2reg_ber_thres | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |
| [2:0] | RW | tcm2reg_ber_thres | TCM BER statistical threshold in J83B mode. The threshold is calculated as follows: 2^(thres + 18). The threshold is a multiple of 30 (15 pairs) symbols. |

## j83b_tcm_6

j83b_tcm_6 is J83B TCM status register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3B | j83b_tcm_6 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | j83b2reg_ctrl_bits | | | | reserved | tcm2reg_syn_fail_num | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RO | j83b2reg_ctrl_bits | Interleaving mode of the deinterleaver in J83B mode. |
| [3] | - | reserved | Reserved. |
| [2:0] | RO | tcm2reg_syn_fail_num | Phase searched by the TCM in J83B mode. |

## j83b_di_1

j83b_di_1 is J83B deinterleaving control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3C | j83b_di_1 | 0x24 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2j83b_lost_per | | | | reserved | reg2j83b_di_level | reg2j83b_di_err_allow | reg2j83b_di_ctrl_word_en |

| Reset | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | reg2j83b_lost_per | MPEG frame sync statistical period threshold in J83B mode. MPEG frame sync is unlocked when the number of invalid frames in the statistical period is greater than the reg2j83b_mpeg_lostlen threshold. |
| [3] | - | reserved | Reserved. |
| [2] | RW | reg2j83b_di_level | Interleaving level of the deinterleaver in J83B mode.<br>0: level 1<br>1: level 2 |
| [1] | RW | reg2j83b_di_err_allow | Whether bit errors are allowed in the interleaving information about the deinterleaver streams in J83B mode.<br>0: no<br>1: yes |
| [0] | RW | reg2j83b_di_ctrl_word_en | Manual configuration enable for the interleaving mode of the deinterleaver in J83B mode.<br>0: automatic<br>1: manual |

## j83b_di_2

j83b_di_2 is J83B deinterleaving control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3D | j83b_di_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2j83b_di_err_max | | | | reg2j83b_di_ctrl_word_in | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | reg2j83b_di_err_max | Maximum number of bit errors allowed in the interleaving information about the deinterleaver streams in J83B mode. |
| [3:0] | RW | reg2j83b_di_ctrl_word_in | Interleaving mode of the deinterleaver that is manually configured in J83B mode. |

## j83b_mfsync_1

j83b_mfsync_1 is J83B MPEG frame sync control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3E | j83b_mfsync_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2j83b_mpeg_lost_en | reg2j83b_mpeg_locklen | | | reg2j83b_mpeg_lostlen | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | reg2j83b_mpeg_lost_en | Whether MPEG frame sync unlock is allowed in J83B mode. |
| [6:4] | RW | reg2j83b_mpeg_locklen | MPEG frame sync lock threshold in J83B mode. |
| [3:0] | RW | reg2j83b_mpeg_lostlen | Threshold for allowing MPEG frame sync unlock in J83B mode. |

## j83b_mfsync_2

j83b_mfsync_2 is J83B MPEG frame sync status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x3F | j83b_mfsync_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tcm2reg_dummy_data | j83b2reg_fec_sync_state | | | reserved | j83b2reg_mpeg_sync_state | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | tcm2reg_dummy_data | Not used. |
| [6:4] | RO | j83b2reg_fec_sync_state | FEC frame sync state machine in J83B mode. |
| [3] | - | reserved | Reserved. |
| [2:0] | RO | j83b2reg_mpeg_sync_state | MPEG frame sync state machine in J83B mode. |

## mctrl_1

mctrl_1 is main control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x40 | mctrl_1 | 0xA0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | version | | | soft_reset | rst_equalizer | rst_rs_tmp | rst_di_tmp | rst_qam |
| Reset | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RO | version | QAM version 101. |
| [4] | RW | soft_reset | Soft reset.<br>0: The QAM module works properly.<br>1: The AGC and ADC are reset.<br>This bit cannot be automatically cleared. During reset, software needs to write 1 and then 0 to the bit. |
| [3] | RW | rst_equalizer | Equalizer reset.<br>0: The QAM module works properly.<br>1: The equalizer is reset.<br>This bit cannot be automatically cleared. During reset, software needs to write 1 and then 0 to the bit. |
| [2] | RW | rst_rs_tmp | RS module reset.<br>0: The QAM module works properly.<br>1: The RS module is reset.<br>This bit cannot be automatically cleared. During reset, software needs to write 1 and then 0 to the bit. |
| [1] | RW | rst_di_tmp | Channel decoding part reset.<br>0: The QAM module works properly.<br>1: The deinterleaver, frame sync module, and descrambler are reset.<br>This bit cannot be automatically cleared. During reset, software needs to write 1 and then 0 to the bit. |
| [0] | RW | rst_qam | Channel demodulation part reset.<br>0: The QAM module works properly.<br>1: The channel demodulation part is reset.<br>This bit cannot be automatically cleared. During reset, software needs to write 1 and then 0 to the bit. |

## mctrl_5

mctrl_5 is main control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x44 | mctrl_5 | 0xA8 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_output_sel | reg2j83b_itu_sel | mf_roll_sel | swap | data_formate | itu_sel | qam_input_ctrl | |
| Reset | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | agc_output_sel | AGC output.<br>0: The AGC1 and AGC2 pins are CMOS outputs.<br>1: The AGC1 and AGC2 pins are open drain (OD) outputs. |
| [6] | RW | reg2j83b_itu_sel | ITU standard select.<br>1: J83-B<br>0: J83-A/C |
| [5] | RW | mf_roll_sel | Coefficients of the matched filter.<br>0: roll-off coefficients for tests<br>1: default roll-off coefficients |
| [4] | RW | swap | AD data format conversion.<br>0: normal format<br>1: exchange between upper and lower bits |
| [3] | RW | data_formate | AD data format conversion.<br>0: normal format<br>1: The MSB is inverted. |
| [2] | RW | itu_sel | ITU-J83 mode.<br>1: ITU-J83C mode<br>0: DVB-C and ITU-J83A modes |
| [1:0] | RW | qam_input_ctrl | Input control.<br>00: The QAM starts to work only after the AGC is locked.<br>01 and 10: The QAM starts to work even when the AGC is not locked.<br>11: The QAM starts to work only after the AGC is locked once and the subsequent unlock is ignored. |

## mctrl_6

mctrl_6 is main control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x45 | mctrl_6 | 0xE0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | lock_pol_sel | auto_srst_en | para_sel | rs_uncorr_reg | de_syn_msk | de_syn_event_reg | de_syn_event_type | lms_blind |
| Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | lock_pol_sel | Int signal polarity.<br>1: active high<br>0: active low |
| [6] | RW | auto_srst_en | Auto reset enable.<br>0: disabled<br>1: enabled |
| [5] | RW | para_sel | Timing recovery, equalizer, and carrier recovery parameter select.<br>1: user-configured parameters<br>0: internal parameters<br>If this bit is set to 0, the equalizer compensation coefficient and scheduled synchronization parameter are set internally. |
| [4] | RW | rs_uncorr_reg | RS error correction failure.<br>1: failed<br>This interrupt is generated if the number of errors in the data frame exceeds the threshold of RS error correction.<br>0: normal |
| [3] | RW | de_syn_msk | Frame sync detector interrupt mask.<br>1: Enable the interrupt.<br>0: Mask the interrupt. |
| [2] | RW | de_syn_event_reg | Frame sync detector interrupt mask.<br>1: Enable the interrupt.<br>0: Mask the interrupt. |
| [1] | RO | de_syn_event_type | Frame sync lock.<br>0: unlocked<br>0: locked |

| | | | |
|---|---|---|---|
| [0] | RO | lms_blind | Equalizer working mode.<br>0: LMS mode<br>1: blind mode |

## mctrl_7

mctrl_7 is main control register 7.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x46 | mctrl_7 | 0x60 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | i2ct_en | scl_output_sel | extad_clken | itlock_sel | itpwm_sel | lock_sel | | fir_en |
| Reset | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | WC | i2ct_en | External two-wire operation enable.<br>When this bit is set to 1, an external two-wire operation is allowed. When the operation is complete, this bit is automatically cleared. |
| [6] | RW | scl_output_sel | scl output<br>0: The pscl pin is CMOS output.<br>1: The psc1 pin is OD output and is pulled up to the 5.5 V power. |
| [5] | RW | extad_clken | Not used. |
| [4] | RW | itlock_sel | Interrupt source select.<br>1: interrupt signal<br>0: locking signal |
| [3] | RW | itpwm_sel | int_pwm pin multiplexing select.<br>1: interrupt<br>0: PWM signal |
| [2:1] | RW | lock_sel | Interrupt source select.<br>00: sync lock<br>01: reserved<br>10: equalization lock<br>11: AGC lock |

| | | | |
|---|---|---|---|
| [0] | RW | fir_en | Notch filter enable.<br>0: disabled. Data is directly transmitted to the next level.<br>1: enabled |

## mctrl_9

mctrl_9 is main control register 9.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x48 | mctrl_9 | 0x08 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | state_sel | | agc1_inv | agc2_inv | gpwm_en | reserved | agc12_sel | agc12b_sel |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | RW | state_sel | Working mode of the timing recovery module.<br>00 and 10: threshold mode<br>01 and 11: count mode |
| [5] | RW | agc1_inv | AGC1 invert enable.<br>1: enabled<br>0: disabled |
| [4] | RW | agc2_inv | AGC2 invert enable.<br>1: enabled<br>0: disabled |
| [3] | RW | gpwm_en | General PWM enable.<br>1: enabled<br>0: disabled |
| [2] | - | reserved | Reserved. |
| [1] | RW | agc12_sel | Not used. |
| [0] | RW | agc12b_sel | Not used. |

## mctrl_11

mctrl_11 is main control register 11.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x4A | mctrl_11 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_lock | st_lock | ca_lock | equ_lock | sync_lock | tcm2reg_sync_lock | j83b2reg_fec_sync_event | j83b2reg_mpeg_sync_event |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | agc_lock | AGC lock.<br>0: unlocked<br>1: locked |
| [6] | RO | st_lock | Timing recovery lock.<br>0: unlocked<br>1: locked |
| [5] | RO | ca_lock | Carrier recovery lock.<br>0: unlocked<br>1: locked |
| [4] | RO | equ_lock | Equalization lock.<br>0: unlocked<br>1: balance lock |
| [3] | RO | sync_lock | Frame sync lock.<br>0: unlocked.<br>1: locked |
| [2] | RO | tcm2reg_sync_lock | TCM lock in J83B mode.<br>0: unlocked<br>0: locked |
| [1] | RO | j83b2reg_fec_sync_event | FEC frame sync lock in J83B mode.<br>0: unlocked<br>1: locked |
| [0] | RO | j83b2reg_mpeg_sync_event | MPEG frame sync lock in J83B mode.<br>0: unlocked<br>1: locked |

## agc_ctrl_15

agc_ctrl_15 is AGC control register 15.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x59 | agc_ctrl_15 | 0x80 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | del_agc_on | frz2_ctrl | | frz1_ctrl | | agc_off | adsat_judge_en | certain_en |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | del_agc_on | AGC1 enable.<br>0: AGC2 works properly and the AGC1 gain is fixed at agc1_max.<br>1: AGC1 and AGC2 work at the same time and the tuner gain is controlled optimally. |
| [6:5] | RW | frz2_ctrl | Test register. It defines the reset value in normal mode. |
| [4:3] | RW | frz1_ctrl | Test register. It defines the reset value in normal mode. |
| [2] | RW | agc_off | AGC1 and AGC2 output enable.<br>0: enabled<br>1: disabled |
| [1] | RW | adsat_judge_en | Test register. It defines the reset value in normal mode. |
| [0] | RW | certain_en | AGC fixed gain enable.<br>0: The gains of AGC1 and AGC2 are adjusted properly.<br>1: The gains of AGC1 and AGC2 are fixed. |

## agc_ctrl_19

agc_ctrl_19 is AGC control register 19.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5C | agc_ctrl_19 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc1_certain | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agc1_certain | Upper eight bits of the fixed AGC1 gain.<br>If the fixed AGC gain is enabled (agc_ctrl_15[certain_en] = 1), the upper eight bits of AGC1 gain are fixed at the field value. |

## agc_ctrl_20

agc_ctrl_20 is AGC control register 20.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5D | agc_ctrl_20 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc2_certain | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agc2_certain | Upper eight bits of the fixed AGC2 gain.<br>If the fixed AGC gain is enabled (agc_ctrl_15[certain_en] = 1), the upper eight bits of AGC2 gain are fixed at the field value. |

## agc_ctrl_22

agc_ctrl_22 is AGC control register 22.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x5F | agc_ctrl_22 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc2_certain | | | | agc1_certain | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RW | agc2_certain | Lower four bits of the fixed AGC2 gain.<br>If the fixed AGC gain is enabled (agc_ctrl_15[certain_en] = 1), the lower four bits of AGC2 gain are fixed at the field value. |
| [3:0] | RW | agc1_certain | Lower four bits of the fixed AGC1 gain.<br>If the fixed AGC gain is enabled (agc_ctrl_15[certain_en] = 1), the lower four bits of AGC1 gain are fixed at the field value. |

## bagc_ctrl_1

bagc_ctrl_1 is BAGC control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x60 | bagc_ctrl_1 | 0x14 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_i_ref | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agc_i_ref | Reference average power consumption of the AGC. |

## bagc_ctrl_2

bagc_ctrl_2 is BAGC control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x61 | bagc_ctrl_2 | 0x02 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | agc2_sd | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | - | reserved | Reserved. |
| [1:0] | RW | agc2_sd | Upper two bits of the initial AGC2 gain.<br>After the AGC is reset by software, AGC2 is adjusted from this value. |

## bagc_ctrl_3

bagc_ctrl_3 is BAGC control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x62 | bagc_ctrl_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc2_sd | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agc2_sd | Lower eight bits of the initial AGC2 gain.<br>After the AGC is reset by software, AGC2 is adjusted from this value. |

## bagc_ctrl_6

bagc_ctrl_6 is BAGC control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x65 | bagc_ctrl_6 | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | i_thres2 | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | i_thres2 | Bandwidth consumed at average power consumption for checking whether the AGC is unlocked when the AGC is locked. |

## bagc_ctrl_9

bagc_ctrl_9 is BAGC control register 9.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x68 | bagc_ctrl_9 | 0x04 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rate_update | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | rate_update | Upper eight bits of the AGC gain adjustment period. |

## bagc_ctrl_10

bagc_ctrl_10 is BAGC control register 10.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x69 | bagc_ctrl_10 | 0xB0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rate_update | | | | | | | |

| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | rate_update | Lower eight bits of the AGC gain adjustment period. |

## bagc_ctrl_12

bagc_ctrl_12 is BAGC control register 12.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6B | bagc_ctrl_12 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pulse_width | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | pulse_width | Refresh cycle of the output PWM wave of the AGC. |

## bagc_ctrl_13

bagc_ctrl_13 is BAGC control register 13.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6E | bagc_ctrl_13 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | if_pwm | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | if_pwm | Upper eight bits of the general-purpose PWM control register.<br>This register is used to generate PWM signals, which are output from int_pwm. |

## bagc_ctrl_14

bagc_ctrl_14 is BAGC control register 14.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x6F | bagc_ctrl_14 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | if_pwm | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | if_pwm | Lower eight bits of the general-purpose PWM control register.<br>This register is used to generate PWM signals, which are output from int_pwm. |

## bagc_stat_1

bagc_stat_1 is BAGC status register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x70 | bagc_stat_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc1_gain | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | agc1_gain | Upper eight bits of the AGC1 gain.<br>For details, see the description of cr_ctrl_21. |

## bagc_stat_2

bagc_stat_2 is BAGC status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x71 | bagc_stat_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc1_gain | | | | reserved | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RO | agc1_gain | Lower four bits of the AGC1 gain.<br>For details, see the description of cr_ctrl_21. |
| [3:0] | RO | reserved | Reserved. |

## bagc_stat_3

bagc_stat_3 is BAGC status register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x72 | bagc_stat_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc2_gain1 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | agc2_gain1 | Upper eight bits of AGC2 gain 1.<br>For details, see the description of cr_ctrl_21. |

## bagc_stat_4

bagc_stat_4 is BAGC status register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x73 | bagc_stat_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc2_gain1 | | | | reserved | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | RO | agc2_gain 1 | Lower four bits of AGC2 gain 1.<br>For details, see the description of cr_ctrl_21. |
| [3:0] | RO | reserved | Reserved. |

## bagc_stat_7

bagc_stat_7 is BAGC status register 7.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x79 | bagc_stat_7 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc_average_power | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | agc_average_power | Average AGC power consumption. |

## j83b_tcm_ber0

j83b_tcm_ber0 is J83B TCM status register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7C | j83b_tcm_ber0 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | tcm2reg_ber_errnum_lat | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:0] | RO | tcm2reg_ber_errnum_lat | Uppermost six bits of the number of TCM BER errors.<br>For details, see the description of cr_ctrl_21. |

## j83b_tcm_ber1

j83b_tcm_ber1 is J83B TCM status register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7D | j83b_tcm_ber1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tcm2reg_ber_errnum_lat | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | tcm2reg_ber_errnum_lat | Upper eight bits of the number of TCM BER errors.<br>For details, see the description of cr_ctrl_21. |

## j83b_tcm_ber2

j83b_tcm_ber2 is J83B TCM status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7E | j83b_tcm_ber2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tcm2reg_ber_errnum_lat | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | tcm2reg_ber_errnum_lat | Lower eight bits of the number of TCM BER errors.<br>For details, see the description of cr_ctrl_21. |

## j83b_tcm_ber3

j83b_tcm_ber3 is J83B TCM status register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x7F | j83b_tcm_ber3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | tcm2reg_ber_errnum_lat | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | tcm2reg_ber_errnum_lat | Lowest eight bits of the number of TCM BER errors.<br>For details, see the description of cr_ctrl_21. |

## sfreq_agc1_init

sfreq_agc1_init is an AGC control register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x87 | sfreq_agc1_init | 0x80 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | agc1_init | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | agc1_init | Initial AGC1 value. |

## sync_ctrl_1

sync_ctrl_1 is frame sync control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x90 | sync_ctrl_1 | 0x0A |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | sync_correct_enb | mismatch | | acg_mode | | trk_mode | |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6] | RW | sync_correct_enb | Correction enable for the sync header and reverse sync header, active high. |
| [5:4] | RW | mismatch | Number of mismatched bits allowed in the next sync byte in trace mode. If the number of mismatched bits is greater than the field value, mismatch is considered. |
| [3:2] | RW | acg_mode | Frame lock after an inverted sync header and consecutive *n* valid frames are detected in sequence. The value of *n* is calculated as follows:<br>n = acq_mode + 3 |
| [1:0] | RW | trk_mode | Frame lock after lock if consecutive (*m* x 204) bytes are detected as invalid frames (no frame header is detected). Then the inverted sync byte is detected again. The values of *m* is calculated as follows:<br>m = trk_mode*2 + 1 |

## ber_1

ber_1 is BER control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x93 | ber_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | bert_en | err_source | err_mode | nbyte | | | reserved | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | WC | bert_en | BER statistics enable.<br>0: invalid<br>1: valid<br>When err_mode is 0 and an overflow occurs in the internal byte counter (the BER statistic threshold is exceeded), ber_en is automatically cleared. |
| [6] | RW | err_source | BER statistics error source.<br>0: Error bits are counted.<br>1: Error bytes are counted. |
| [5] | RW | err_mode | BER statistical mode.<br>0: auto-stop statistical mode. When the internal counter reaches the threshold or an overflow occurs in the BER counter, counting automatically stops and ber_en is automatically cleared.<br>1: auto-repeat statistical mode. When the internal counter reaches the statistics threshold, it is automatically reset and then restarts to count until ber_en is 0. |
| [4:2] | RW | nbyte | BER statistics threshold.<br>The overflow threshold for the internal byte counter is 2^(2 x nbyte+12). This threshold is valid only when err_mode is 0. The value of the internal byte counter ranges from 4,096 to $2^{26}$. |
| [1:0] | - | reserved | Reserved. |

## ber_2

ber_2 is BER status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x94 | ber_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | error_cnt | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | error_cnt | Upper eight bits of the internal error bit/byte counter.<br>This value is the count of raw bit/byte errors, including all errors in the RS check bytes.<br>For details, see the description of cr_ctrl_21. |

## ber_3

ber_3 is BER status register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x95 | ber_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | error_cnt | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | error_cnt | Middle eight bits of the internal error bit/byte counter.<br>This value is the count of raw bit/byte errors, including all errors in the RS check bytes.<br>For details, see the description of cr_ctrl_21. |

## ber_4

ber_4 is BER status register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x96 | ber_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | error_cnt | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | error_cnt | Lower eight bits of the internal error bit/byte counter.<br>This value is the count of raw bit/byte errors, including all errors in the RS check bytes.<br>For details, see the description of cr_ctrl_21. |

## ts_ctrl_1

ts_ctrl_1 is output control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x98 | ts_ctrl_1 | 0x8E |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Name | sync_byte_inv | bend_bypass | m_ckout_ctrl | parity_en | sp_sel | tei_enable | ds_enable | reserved |
|---|---|---|---|---|---|---|---|---|
| Reset | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | sync_byte_inv | Output data invert indicator of the descrambler.<br>1: inverted<br>0: normal |
| [6] | RW | bend_bypass | Decoding module bypass.<br>0: The decoding-related modules are not bypassed.<br>1: All decoding related modules including the deinterleaver, RS decoding module, and descrambler after the demapping module are bypassed. |
| [5] | RW | m_ckout_ctrl | Not used. |
| [4] | RW | parity_en | Output enable for the RS check bit.<br>0: disabled<br>1: enabled |
| [3] | RW | sp_sel | Mode select.<br>1: serial mode<br>0: parallel mode 2. This mode is only for tests and is not used in normal working.<br>This bit is valid only when out_ctrl_2[comm_if_en] is 0. |
| [2] | RW | tei_enable | Transport error indicator (TEI) bit enable.<br>1: The MPEG-2 TEI bit is enabled when an uncorrectable frame error is found.<br>0: The MPEG-2 TEI bit is not enabled even when an uncorrectable frame error is found. |
| [1] | RW | ds_enable | Descrambling enable.<br>1: enabled<br>0: disabled |
| [0] | - | reserved | Reserved. |

## ts_ctrl_2

ts_ctrl_2 is output control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x99 | ts_ctrl_2 | 0x20 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | sync_drop | comm_if_en | comm_if_clk_ctrl | comm_if_clk_base | reserved | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | sync_drop | Sync byte discard.<br>0: The sync bytes in the MPEG-TS frame header are output.<br>1: The sync bytes in the MPEG-TS frame header are not output (the corresponding ts_val is invalid). |
| [6] | RW | comm_if_en | Mode select.<br>1: parallel port mode 1<br>0: parallel port mode 2 or serial port mode. The mode is controlled by out_ctrl_1[sp_sel]. |
| [5] | RW | comm_if_clk_ctrl | ts_clk output polarity. This signal is used only in the field-programmable gate array (FPGA) version.<br>0: direct output<br>1: reverse output |
| [4] | RW | comm_if_clk_base | Not used. |
| [3:0] | - | reserved | Reserved. |

## rs_ctrl_1

rs_ctrl_1 is RS decoding control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9B | rs_ctrl_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pkt_cnt | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | pkt_cnt | Upper eight bits of the TS frame counter.<br>For details about the count of output TS frames, see the description of rs_ctrl_8 bit[5:4].<br>For details about the usage, see the description of cr_ctrl_21. |

## rs_ctrl_2

rs_ctrl_2 is RS decoding control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9C | rs_ctrl_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pkt_cnt | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | pkt_cnt | Lower eight bits of the TS frame counter.<br>For details about the count of output TS frames, see the description of rs_ctrl_8 bit[5:4].<br>For details about the usage, see the description of cr_ctrl_21. |

## rs_ctrl_3

rs_ctrl_3 is RS decoding control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9D | rs_ctrl_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pkt_corr | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | pkt_corr | Upper eight bits of the corrected TS frame counter.<br>After being enabled, this register is used to count the TS frames corrected by the RS module. For details, see the description of rs_ctrl_8 bit[5:4].<br>For details about the usage, see the description of cr_ctrl_21. |

## rs_ctrl_4

rs_ctrl_4 is RS decoding control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9E | rs_ctrl_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pkt_corr | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | pkt_corr | Lower eight bits of the corrected TS frame counter.<br>After being enabled, this register is used to count the TS frames corrected by the RS module. For details, see the description of rs_ctrl_8 bit[5:4].<br>For details about the usage, see the description of cr_ctrl_21. |

## rs_ctrl_5

rs_ctrl_5 is RS decoding control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x9F | rs_ctrl_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pkt_uncorr | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | pkt_uncorr | Upper eight bits of the uncorrected TS frame counter.<br>After being enabled, this register is used to count the TS frames that cannot be corrected by the RS module. For details, see the description of rs_ctrl_8 bit[5:4].<br>For details about the usage, see the description of cr_ctrl_21. |

## rs_ctrl_6

rs_ctrl_6 is RS decoding status register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA0 | rs_ctrl_6 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | pkt_uncorr | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | pkt_uncorr | Lower eight bits of the uncorrected TS frame counter.<br>After being enabled, this register is used to count the TS frames that cannot be corrected by the RS module. For details, see the description of rs_ctrl_8 bit[5:4].<br>For details about the usage, see the description of cr_ctrl_21. |

## rs_ctrl_8

rs_ctrl_8 is RS decoding control register 8.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA1 | rs_ctrl_8 | 0x40 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reg2rs_rs_sel | rs_corr_en | static_hold | static_clear | rs_mode127 | rs2_rs_corr_en | rs2_mode127 | reserved |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | reg2rs_rs_sel | RS mode select. This bit is valid only when reg2j83b_itu_sel is set to 1, that is, in J83B mode.<br>0: RS 1<br>1: RS 2 |
| [6] | RW | rs_corr_en | RS correction mask.<br>0: The RS module works properly (default).<br>1: The correction function of the RS module is masked, but other functions are not affected. |
| [5] | RW | static_hold | Counter hold.<br>0: Counters work normally.<br>1: The TS frame counter (pkt_cnt), corrected TS frame counter (pkt_corr), and uncorrected TS frame counter (pkt_uncorr) retain corresponding count values. |
| [4] | RW | static_clear | Counter clear.<br>0: Counters work normally.<br>1: The TS frame counter (pkt_cnt), corrected TS frame counter (pkt_corr), and uncorrected TS frame counter (pkt_uncorr) are cleared. |

| | | | |
|---|---|---|---|
| [3] | RW | rs_mode127 | Whether to erase the 128th code in RS 1 mode. This bit is valid only when reg2j83b_itu_sel is set to 1, that is, in J83B and RS 1 modes.<br>0: not erase<br>1: erase |
| [2] | RW | rs2_rs_corr_en | RS 2 correction mask. This bit is valid only when reg2j83b_itu_sel is set to 1, that is, in J83B mode.<br>0: The RS module works properly (default).<br>1: The correction function of the RS module is masked, but other functions are not affected. |
| [1] | RW | rs2_mode127 | Whether to erase the 128th code in RS 2 mode. This bit is valid only when reg2j83b_itu_sel is set to 1, that is, in J83B and RS 2 modes.<br>0: not erase<br>1: erase |
| [0] | - | reserved | Reserved. |

## bs_ctrl_1

bs_ctrl_1 is blind scanning control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA6 | bs_ctrl_1 | 0x04 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | spec_inv_en | spec_search_en | rate_search_en | qam_search_en |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3] | RW | spec_inv_en | Spectrum invert.<br>0: The demodulator is not allowed to process any spectrum inversion caused by the transfer channel.<br>1: The demodulator is allowed to process any spectrum inversion caused by the transfer channel. |

| | | | |
|---|---|---|---|
| [2] | RW | spec_search_en | Spectrum auto-inversion enable.<br>0: disabled<br>1: enabled<br>For details about the actual spectrum mode, see the description of bs_stat_1. |
| [1] | RW | rate_search_en | Symbol rate blind scanning enable.<br>0: disabled<br>1: enabled<br>For details about the found modulation mode, see the description of bs_stat_1. |
| [0] | RW | qam_search_en | Modulation mode blind scanning enable.<br>0: disabled<br>1: enabled<br>For details about the found modulation mode, see the description of bs_stat_1. |

## bs_ctrl_2

bs_ctrl_2 is blind scanning control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xA7 | bs_ctrl_2 | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rate_search | | | qam_search | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | RW | rate_search | Range of the symbol rate to be searched when symbol rate blind scanning is enabled. When symbol rate blind scanning is disabled, this field is meaningless.<br>000: invalid<br>001: 1.8–0.9 MBaud<br>010: 1.8–3.6 MBaud<br>011: 1.8–3.6 Mbaud or 0.9–1.8 MBaud<br>100: 3.6–7.2 MBaud<br>101: 3.6–7.2 Mbaud or 0.9–1.8 MBaud<br>110: 3.6–7.2 Mbaud or 1.8–3.6 MBaud<br>111: 3.6–7.2 Mbaud, 1.8–3.6 Mbaud, or 0.9–1.8 MBaud |

| | | | |
|---|---|---|---|
| [4:0] | RW | qam_search | Modulation mode configured by the user when qam_search_en is 0. The details are as follows:<br>0x01: QAM16<br>0x02: QAM32<br>0x04: QAM128<br>0x08: QAM256<br>0x10: QAM64<br>Other values: reserved<br>When qam_search_en is 1, multiple bits are valid, that is, multiple modulation modes can be searched for. For example:<br>0x18: QAM64 and QAM256 |

## bs_stat_1

bs_stat_1 is blind scanning status register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAC | bs_stat_1 | 0x80 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | qam_mode | | | | | rate_range | | spec_inv |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | RO | qam_mode | QAM mode.<br>0x01: QAM16<br>0x02: QAM32<br>0x04: QAM128<br>0x08: QAM256<br>0x10: QAM64<br>Other values: reserved |
| [2:1] | RO | rate_range | Range of the symbol rate obtained after blind scanning.<br>00: 7.2–3.6 MBaud<br>01: 3.6–1.8 MBaud<br>10: 1.8–0.9 MBaud<br>11: reserved |
| [0] | RO | spec_inv | Spectrum invert.<br>0: not inverted<br>1: inverted |

## bs_stat_2

bs_stat_2 is blind scanning status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAD | bs_stat_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | qam_search_status | | rate_search_status | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:2] | RO | qam_search_status | Result of modulation mode blind scanning. This field is valid only when modulation mode blink scanning is enabled.<br>00: Blind scanning is not complete.<br>01: meaningless<br>10: Blind scanning is complete but fails.<br>11: Blind scanning is complete and successful. |
| [1:0] | RO | rate_search_status | Result of symbol rate blind scanning.<br>00: Blind scanning is not complete.<br>01: meaningless<br>10: Blind scanning is complete but fails.<br>11: Blind scanning is complete and successful. |

## bs_stat_3

bs_stat_3 is blind scanning status register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAE | bs_stat_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | | rate_ratio |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:1] | - | reserved | Reserved. |

| | | | |
|---|---|---|---|
| [0] | RO | rate_ratio | After symbol rate blind scanning is complete and successful, the symbol rate is calculated as follows:<br>Fs = Fad/[2^(rate_range + 1) x (rate_ratio)/(2^14)]<br>When rate_range is 0, Fad is 28.8 MHz.<br>When rate_range is 1, Fad is 14.4 MHz.<br>When rate_range is 2, Fad is 7.2 MHz.<br>This bit is the MSB of rate_ratio. |

## bs_stat_4

bs_stat_4 is blind scanning status register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xAF | bs_stat_4 | 0x86 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rate_ratio | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | rate_ratio | After symbol rate blind scanning is complete and successful, the symbol rate is calculated as follows:<br>Fs=Fad/[2^(rate_range + 1) x (rate_ratio)/(2^14)]<br>When rate_range is 0, Fad is 28.8 MHz.<br>When rate_range is 1, Fad is 14.4 MHz.<br>When rate_range is 2, Fad is 7.2 MHz.<br>These bits are the upper eight bits of rate_ratio. |

## bs_stat_5

bs_stat_5 is blind scanning status register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB0 | bs_stat_5 | 0x0D |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | rate_ratio | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | rate_ratio | After symbol rate blind scanning is complete and successful, the symbol rate is calculated as follows:<br>Fs=Fad/[2^(rate_range + 1) x (rate_ratio)/(2^14)]<br>When rate_range is 0, Fad is 28.8 MHz.<br>When rate_range is 1, Fad is 14.4 MHz.<br>When rate_range is 2, Fad is 7.2 MHz.<br>These bits are the lower eight bits of rate_ratio. |

## fs_ctrl_1

fs_ctrl_1 is scanning control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB1 | fs_ctrl_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | test | | fre_init | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | RW | test | Test register. It defines the reset value in normal mode. |
| [5:0] | RW | fre_init | Upper six bits of the initial demodulation frequency.<br>Demodulation frequency = fre_init x $f_{clk}$/[(2^11) x 2 x pi]<br>The frequency scanning circuit works under the sampling clock.<br>$f_{clk}$/[(2^11) x 2 x pi] is the resolution precision. For example, in DVB-C or ITU J83-A/C mode, when $f_{clk}$ is 28.8 MHz, the resolution precision is 2238 Hz; in ITU J83-B mode, when $f_{clk}$ is 25 MHz, the resolution precision is 1943 Hz. |

## fs_ctrl_2

fs_ctrl_2 is scanning control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB2 | fs_ctrl_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fre_init | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fre_init | Lower eight bits of the initial demodulation frequency.<br>Demodulation frequency = fre_init x $f_{clk}$/[(2^11) x 2 x pi]<br>The frequency scanning circuit works under the sampling clock.<br>$f_{clk}$/[(2^11) x 2 x pi] is the resolution precision. For example, in DVB-C or ITU J83-A/C mode, when $f_{clk}$ is 28.8 MHz, the resolution precision is 2238 Hz; in ITU J83-B mode, when $f_{clk}$ is 25 MHz, the resolution precision is 1943 Hz. |

## fs_ctrl_4

fs_ctrl_4 is scanning control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB4 | fs_ctrl_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | scan_step | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | scan_step | Upper eight bits of the scanning interval step.<br>The step between two consecutive frequencies to be demodulated is calculated as follows: scan_step x $f_{clk}$/[(2^11) x 2 x pi] |

## fs_ctrl_5

fs_ctrl_5 is scanning control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB5 | fs_ctrl_5 | 0x70 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | scan_step | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | scan_step | Lower eight bits of the scanning interval step.<br>The step between two consecutive frequencies to be demodulated is calculated as follows:<br>scan_step x $f_{clk}$/[(2^11) x 2 x pi] |

## fs_ctrl_6

fs_ctrl_6 is scanning control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB6 | fs_ctrl_6 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | scan_start | reserved | | scan_end_flag | scan_lock_flag |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:5] | - | reserved | Reserved. |
| [4] | RW | scan_start | Frequency scanning enable.<br>0: disabled<br>1: enabled. |
| [3:2] | - | reserved | Reserved. |
| [1] | RO | scan_end_flag | Frequency scanning end signal.<br>0: not ended<br>1: ended |
| [0] | RO | scan_lock_flag | Whether the frequency scanning is successful.<br>0: failure<br>1: success |

## fs_ctrl_7

fs_ctrl_7 is scanning control register 7.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB7 | fs_ctrl_7 | 0x0A |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | fre_step_num | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:0] | RW | fre_step_num | Maximum frequency scanning step. |

## fs_stat_1

fs_stat_1 is scanning status register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB8 | fs_stat_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | freq_shift | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:0] | RO | freq_shift | Upper six bits of the final frequency offset obtained after frequency scanning. |

## fs_stat_2

fs_stat_2 is scanning status register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xB9 | fs_stat_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | freq_shift | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RO | freq_shift | Lower eight bits of the final frequency offset obtained after frequency scanning. |

## j83b_ffsync_1

j83b_ffsync_1 is J83B FFSYNC control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xBA | j83b_ffsync_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | reg2j83b_fra_locklen | | | reg2j83b_fra_lostlen | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:3] | RW | reg2j83b_fra_locklen | Frame sync lock after a sync timing and consecutive *n* valid frames are detected in sequence. The value of *n* is calculated as follows:<br>n = reg2j83b_fra_locklen + 1 |
| [2:0] | RW | reg2j83b_fra_lostlen | Frame sync unlock after errors are detected in consecutive *m* sync timing positions. Then sync timings are detected again. The value of *m* is calculated as follows:<br>m = reg2j83b_fra_lostlen + 1 |

## j83b_ffsync_2

j83b_ffsync_2 is J83B FFSYNC control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xBB | j83b_ffsync_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | reg2j83b_unlock_toler | | | reg2j83b_lock_mismatch | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:3] | RW | reg2j83b_unlock_toler | When the frame sync module is not locked, the phase change pulse is sent to the TCM if the sync timings are not detected in consecutive *p* frames. The value of *p* is calculated as follows:<br>p = reg2j83bunlock_toler + 2 |
| [2:0] | RW | reg2j83b_lock_mismatch | Number of allowed error bits in the sync timing positions before the frame sync module is locked. If the value is 0, bit errors are not allowed. |

## j83b_ffsync_3

j83b_ffsync_3 is J83B FFSYNC control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xBC | j83b_ffsync_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | reg2j83b_lost_mismatch | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:3] | - | reserved | Reserved. |
| [2:0] | RW | reg2j83b_lost_mismatch | Number of allowed error bits in the sync timing positions after the frame sync module is locked. If the value is 0, bit errors are not allowed. |

## j83b_dr_1

j83b_di_1 is J83B descrambling control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xBD | j83b_dr_1 | 0x7F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | reg2j83b_dr_ini0 | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:0] | RW | reg2j83b_dr_ini0 | Initial value of the internal register a3. |

## j83b_dr_2

j83b_di_2 is J83B descrambling control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xBE | j83b_dr_2 | 0x7F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | reg2j83b_dr_ini1 | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:0] | RW | reg2j83b_dr_ini1 | Initial value of the internal register ff1. |

## j83b_dr_3

j83b_di_3 is J83B descrambling control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xBF | j83b_dr_3 | 0x7F |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | reg2j83b_dr_ini2 | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | - | reserved | Reserved. |
| [6:0] | RW | reg2j83b_dr_ini2 | Initial value of the internal register ff2. |

### four_reg_sel

four_reg_sel is a register block select register.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0xE0 | four_reg_sel | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | | | reg2mem_sel | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:2] | - | reserved | Reserved. |
| [1:0] | RW | reg2mem_sel | Memory select control signal.<br>00: The QAM registers are configured.<br>10: The CRG and hardware IP registers are configured.<br>Other values: reserved |

# 2.26 System Control Register Summary

Table 2-2 describes the system control registers.

**Table 2-2** System control register summary (base address = 0x0000)

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x00 | crg_ctrl_0 | CRG control register 0 | 2-63 |
| 0x01 | crg_ctrl_1 | CRG control register 1 | 2-64 |
| 0x02 | crg_ctrl_2 | CRG control register 2 | 2-64 |

| Offset Address | Register | Description | Page |
|---|---|---|---|
| 0x03 | crg_ctrl_3 | CRG control register 3 | 2-65 |
| 0x04 | crg_ctrl_4 | CRG control register 4 | 2-66 |
| 0x05 | crg_ctrl_5 | CRG control register 5 | 2-66 |
| 0x10 | hard_ctrl_0 | AD control register 0 | 2-67 |
| 0x11 | hard_ctrl_1 | AD control register 1 | 2-67 |
| 0x12 | hard_ctrl_2 | AD control register 2 | 2-67 |
| 0x13 | hard_ctrl_3 | AD control register 3 | 2-68 |
| 0x14 | hard_ctrl_4 | AD control register 4 | 2-68 |
| 0x15 | hard_ctrl_5 | AD control register 5 | 2-68 |
| 0x16 | hard_ctrl_6 | AD control register 6 | 2-69 |
| 0x17 | hard_ctrl_7 | PLL control register 0 | 2-69 |
| 0x18 | hard_ctrl_8 | PLL control register 1 | 2-69 |
| 0x19 | hard_ctrl_9 | PLL control register 2 | 2-70 |
| 0x1A | hard_ctrl_10 | PLL control register 3 | 2-70 |
| 0x1B | hard_ctrl_11 | PLL control register 4 | 2-70 |
| 0x1C | hard_ctrl_12 | PLL control register 5 | 2-71 |
| 0x1D | hard_ctrl_13 | PLL control register 6 | 2-71 |
| 0x1E | hard_ctrl_14 | PLL control register 6 | 2-72 |
| 0x20 | ioshare_ctrl_0 | IOSHARE control register 0 | 2-72 |
| 0x21 | ioshare_ctrl_1 | IOSHARE control register 1 | 2-73 |
| 0x22 | ioshare_ctrl_2 | IOSHARE control register 2 | 2-74 |
| 0x23 | ioshare_ctrl_3 | IOSHARE control register 3 | 2-74 |
| 0x24 | ioshare_ctrl_4 | IOSHARE control register 4 | 2-75 |
| 0x25 | ioshare_ctrl_5 | IOSHARE control register 5 | 2-76 |
| 0x26 | ioshare_ctrl_6 | IOSHARE control register 6 | 2-77 |
| 0x27 | ioshare_ctrl_7 | IOSHARE control register 7 | 2-78 |
| 0x28 | ioshare_ctrl_8 | IOSHARE control register 8 | 2-79 |
| 0x29 | ioshare_ctrl_9 | IOSHARE control register 9 | 2-80 |

# 2.27 System Control Register Description

## crg_ctrl_0

crg_ctrl_0 is CRG control register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x00 | crg_ctrl_0 | 0x2B |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ad_out_clk_sel | qam_clk_out_sel | ext_ad_in_clk_sel | i2c_clk_sel | ads_clk_sel | adc_clk_sel | ts_clk_sel | ts_clk_out_sel |
| Reset | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | ad_out_clk_sel | ADC output associated clock signal.<br>0: The phase is the same as the adc_clk phase.<br>1: The phase is the inverse of the adc_clk phase. |
| [6] | RW | qam_clk_out_sel | qam_clk output clock signal.<br>0: The phase is the same as the qam_clk phase.<br>1: 1: The phase is the inverse of the qam_clk phase. |
| [5] | RW | ext_ad_in_clk_sel | External AD input clock signal.<br>0: exd_ad_in_clk, external AD associated clock<br>1: adc_clk, internal AD clock |
| [4] | RW | i2c_clk_sel | $I^2C$ clock signal.<br>0: xtal_clk<br>1: ref_div2_clk |
| [3] | RW | ads_clk_sel | AD associated clock signal (the QAM uses this clock to sample AD data).<br>0: The phase is the same as the AD clock phase.<br>1: The phase is the inverse of the AD clock phase. |
| [2] | RW | adc_clk_sel | ADC clock signal.<br>0: xtal_clk<br>1: foutdiv_clk |
| [1] | RW | ts_clk_sel | TS clock signal.<br>0: ts_clk_odd<br>1: ts_clk_even |

| | | | |
|---|---|---|---|
| [0] | RW | ts_clk_out_sel | TS output associated clock signal.<br>0: The phase is the same as the ts_clk phase.<br>1: 1: The phase is the inverse of the ts_clk phase. |

## crg_ctrl_1

crg_ctrl_1 is CRG control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x01 | crg_ctrl_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | qam_j83ac_srst_req | qam_j83b_srst_req | chip_srst_req | qam_srst_req | i2c_srst_req | ts_srst_req |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5] | RW | qam_j83ac_srst_req | J83-A/C soft reset request, active high. |
| [4] | RW | qam_j83b_srst_req | J83-B soft reset request, active high. |
| [3] | RW | chip_srst_req | Chip reset request, active high. |
| [2] | RW | qam_srst_req | QAM reset request, active high. |
| [1] | RW | i2c_srst_req | $I^2C$ reset request, active high. |
| [0] | RW | ts_srst_req | TS reset request, active high. |

## crg_ctrl_2

crg_ctrl_2 is CRG control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x02 | crg_ctrl_2 | 0xFF |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ad_out_clk_en | qam_j83ac_clk_en | qam_j83b_clk_en | ts_clk_en | ads_clk_en | qam2x_clk_en | qam_clk_en | i2c_clk_en |

| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RW | ad_out_clk_en | Gating signal of ADC output associated clock ad_out_clk.<br>0: disabled<br>1: enabled (normal output) |
| [6] | RW | qam_j83ac_clk_en | qam_j83ac_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |
| [5] | RW | qam_j83b_clk_en | qam_j83b_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |
| [4] | RW | ts_clk_en | ts_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |
| [3] | RW | ads_clk_en | ads_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |
| [2] | RW | qam2x_clk_en | qam2x_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |
| [1] | RW | qam_clk_en | qam_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |
| [0] | RW | i2c_clk_en | i2c_clk gating signal.<br>0: disabled<br>1: enabled (normal output) |

## crg_ctrl_3

crg_ctrl_3 is CRG control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x03 | crg_ctrl_3 | 0x06 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | ts_clk_div_odd | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:0] | RW | ts_clk_div_odd | TS frequency divider signal (frequency divider ratio).<br>For example, if ts_clk_div_odd is set to 4'h6, the frequency of the reference clock is divided by 6. |

## crg_ctrl_4

crg_ctrl_4 is CRG control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x04 | crg_ctrl_4 | 0x05 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | ts_clk_div_even | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:0] | RW | ts_clk_div_even | TS even frequency divider control signal.<br>ts_clk = 2 x (ts_clk_div_even + 1)<br>For example, if ts_clk_div_even is set to 4'h1, the frequency of the reference clock is divided by 4. |

## crg_ctrl_5

crg_ctrl_5 is CRG control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x05 | crg_ctrl_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | dly_cell_ctrl | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:0] | RW | dly_cell_ctrl | Increased delay between the reference clock and the QAM clock. |

## hard_ctrl_0

hard_ctrl_0 is AD control register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x10 | hard_ctrl_0 | 0x23 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl0 | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl0 | AD control register 0. |

## hard_ctrl_1

hard_ctrl_1 is AD control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x11 | hard_ctrl_1 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl1 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl1 | AD control register 1. |

## hard_ctrl_2

hard_ctrl_2 is AD control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x12 | hard_ctrl_2 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl2 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl2 | AD control register 2. |

## hard_ctrl_3

hard_ctrl_3 is AD control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x13 | hard_ctrl_3 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl3 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl3 | AD control register 3. |

## hard_ctrl_4

hard_ctrl_4 is AD control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x14 | hard_ctrl_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl4 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl4 | AD control register 4. |

## hard_ctrl_5

hard_ctrl_5 is AD control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x15 | hard_ctrl_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl5 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl5 | AD control register 5. |

## hard_ctrl_6

hard_ctrl_6 is AD control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x16 | hard_ctrl_6 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ctrl6 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | ctrl6 | AD control register 6. |

## hard_ctrl_7

hard_ctrl_7 is PLL control register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x17 | hard_ctrl_7 | 0x08 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | ref_div | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:0] | RW | ref_div | Frequency divider parameter of the reference clock, ranging from 1 to 63. |

## hard_ctrl_8

hard_ctrl_8 is PLL control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x18 | hard_ctrl_8 | 0x20 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | fb_div | | | | | | | |

| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | fb_div | Lower eight bits of the feedback frequency divider signal. |

## hard_ctrl_9

hard_ctrl_9 is PLL control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x19 | hard_ctrl_9 | 0x01 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | | | fb_div | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:4] | - | reserved | Reserved. |
| [3:0] | RW | fb_div | Upper four bits of the feedback frequency divider signal. |

## hard_ctrl_10

hard_ctrl_10 is PLL control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1A | hard_ctrl_10 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | frac | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | frac | Lowest eight bits of the decimal frequency divider value. |

## hard_ctrl_11

hard_ctrl_11 is PLL control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1B | hard_ctrl_11 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | frac | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | frac | Middle bits of the decimal frequency divider value. |

## hard_ctrl_12

hard_ctrl_12 is PLL control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1C | hard_ctrl_12 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | frac | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | frac | Uppermost eight bits of the decimal frequency divider value. |

## hard_ctrl_13

hard_ctrl_13 is PLL control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1D | hard_ctrl_13 | 0x11 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | | post_div1 | | | post_div2 | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:6] | - | reserved | Reserved. |
| [5:3] | RW | post_div1 | Level-1 post frequency divider value, ranging from 1 to 7. |
| [2:0] | RW | post_div2 | Level-2 post frequency divider value, ranging from 1 to 7.<br>Output frequency = FVCO/post_div1/post_div2 |

## hard_ctrl_14

hard_ctrl_14 is PLL control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x1E | hard_ctrl_14 | 0x26 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | lock | pd | dac_pd | dsm_pd | foutpost_div_pd | fout4_phase_pd | fout_vco_pd | bypass |
| Reset | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7] | RO | lock | PLL lock indicator signal. |
| [6] | RW | pd | Global clock stop, active high. |
| [5] | RW | dac_pd | DAGC clock stop, active high. |
| [4] | RW | dsm_pd | Delta sigma modulator clock stop, active high. |
| [3] | RW | foutpost_div_pd | All output (excluding VCO clock) stop, active high. |
| [2] | RW | fout4_phase_pd | Phase-4 clock, 2x clock, 3x clock, and 4x clock stop, active high. |
| [1] | RW | fout_vco_pd | VCO clock stop, active high. |
| [0] | RW | bypass | PLL bypass.<br>0: invalid<br>1: bypassed |

## ioshare_ctrl_0

ioshare_ctrl_0 is IOSHARE control register 0.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x20 | ioshare_ctrl_0 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_sel | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Access | Name | Description |
|---|---|---|---|

| | | | |
|---|---|---|---|
| [7:0] | RW | mode_sel | I/O output mode select.<br>mode_sel[0]: Reversing the upper and lower bits of TS output.<br>0: not reversed<br>1: reversed<br>mode_sel[1]: I/O output AD data.<br>0: disabled<br>1: enabled<br>mode_sel[2]: I/O input external AD data.<br>0: disabled<br>1: enabled<br>mode_sel[3]: The I/O output the data output by the I/O data collection logic.<br>0: disabled<br>1: enabled<br>mode_sel[4]: AGC1 output when mode_sel[2:1] is set to 0.<br>0: AGC1<br>1: PWM<br>mode_sel[5]: TS_ERR output when mode_sel[3:1] is set to 0.<br>0: reserved<br>1: int_lock<br>mode_sel[7]: oen control signal when the I/O interface outputs TSs.<br>0: enabled<br>1: disabled |

## ioshare_ctrl_1

ioshare_ctrl_1 is IOSHARE control register 1.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x21 | ioshare_ctrl_1 | 0xFF |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl0 | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl0 | TS_DAT interface oen control signal.<br>0: ts_dat_oen<br>1: 1 |

## ioshare_ctrl_2

ioshare_ctrl_2 is IOSHARE control register 2.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x22 | ioshare_ctrl_2 | 0xFF |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl1 | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl1 | Oen control signal.<br>mode_ctrl1[0]: io_ts_clk_oe control signal.<br>0: reversed phase of tio_ts_clk_oen<br>1: 0<br>mode_ctrl1[1]: io_ts_err_oen control signal.<br>0: tio_ts_err_oen<br>1: 1<br>mode_ctrl1[2]: io_ts_vld_oen control signal.<br>0: tio_ts_vld_oen<br>1: 1<br>mode_ctrl1[3]: io_ts_synv_oen control signal.<br>0: tio_ts_synv_oen<br>1: 1<br>mode_ctrl1[4]: io_ts_agc1_oen control signal.<br>0: tio_agc1_oen<br>1: 1<br>mode_ctrl1[5]: io_clk_out_oen control signal.<br>0: 0<br>1: 1 |

## ioshare_ctrl_3

ioshare_ctrl_3 is IOSHARE control register 3.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x23 | ioshare_ctrl_3 | 0x10 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl2 | | | | | | | |

| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl2 | TS_CLK control signal on the I/O interface for controlling the tristate PAD with the Schmitt trigger and pull-up and pull-down.<br>mode_ctrl[0]: PAD REU interface control<br>0: The value 0 indicates that this bit does not take effect.<br>1: The value 1 indicates PAD pull-up when OE is 0.<br>mode_ctrl[1]: PAD REU interface control<br>0: The value 0 indicates that this bit does not take effect.<br>1: The value 1 indicates PAD pull-down when OE is 0.<br>mode_ctrl[2]: PAD ST interface control<br>0: normal mode<br>1: Schmitt trigger<br>mode_ctrl[3]: PAD DS0 interface control<br>mode_ctrl[4]: PAD DS1 interface control<br>mode_ctrl[5]: PAD DS2 interface control<br>{DS2,DS1,DS0} supports eight drive capabilities. The following list the values under the typical conditions:<br>000: 3.35mA;<br>001: 6.7mA;<br>010: 10.19mA;<br>011: 13.56mA;<br>100: 17.04mA;<br>101: 20.42mA;<br>110: 23.88mA;<br>111: 27.24mA.<br>mode_ctrl[6]: PAD SL interface control.<br>0: high conversion rate<br>1: low conversion rate |

## ioshare_ctrl_4

ioshare_ctrl_4 is IOSHARE control register 4.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x24 | ioshare_ctrl_4 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl3 | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl3 | mode_ctrl3[3:0] are TS_DAT[0] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[0]<br>0001: ts_dat_tmp[1]<br>0010: ts_dat_tmp[2]<br>0011: ts_dat_tmp[3]<br>0100: ts_dat_tmp[4]<br>0101: ts_dat_tmp[5]<br>0110: ts_dat_tmp[6]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err<br>mode_ctrl3[7:4] are TS_DAT[1] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[1]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[2]<br>0011: ts_dat_tmp[3]<br>0100: ts_dat_tmp[4]<br>0101: ts_dat_tmp[5]<br>0110: ts_dat_tmp[6]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err |

## ioshare_ctrl_5

ioshare_ctrl_5 is IOSHARE control register 5.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x25 | ioshare_ctrl_5 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl4 | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl4 | mode_ctrl4[3:0] are TS_DAT[2] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[2]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[3]<br>0100: ts_dat_tmp[4]<br>0101: ts_dat_tmp[5]<br>0110: ts_dat_tmp[6]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err<br>mode_ctrl4[7:4] are TS_DAT[3] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[3]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[4]<br>0101: ts_dat_tmp[5]<br>0110: ts_dat_tmp[6]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err |

## ioshare_ctrl_6

ioshare_ctrl_6 is IOSHARE control register 6.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x26 | ioshare_ctrl_6 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl5 | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl5 | mode_ctrl5[3:0] are TS_DAT[4] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[4]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[5]<br>0110: ts_dat_tmp[6]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err<br>mode_ctrl5[7:4] are TS_DAT[5] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[5]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[4]<br>0110: ts_dat_tmp[6]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err |

## ioshare_ctrl_7

ioshare_ctrl_7 is IOSHARE control register 7.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x27 | ioshare_ctrl_7 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl6 | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl6 | mode_ctrl6[3:0] are TS_DAT[6] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[6]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[4]<br>0110: ts_dat_tmp[5]<br>0111: ts_dat_tmp[7]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err<br>mode_ctrl6[7:4] are TS_DAT[7] output select signals.<br>ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_dat_tmp[7]<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[4]<br>0110: ts_dat_tmp[5]<br>0111: ts_dat_tmp[6]<br>1000: ts_val<br>1001: ts_sync<br>default: ts_err |

## ioshare_ctrl_8

ioshare_ctrl_8 is IOSHARE control register 8.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x28 | ioshare_ctrl_8 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl7 | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl7 | mode_ctrl7[3:0] are TS_VAL output select signals. ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_val<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[4]<br>0110: ts_dat_tmp[5]<br>0111: ts_dat_tmp[6]<br>1000: ts_dat_tmp[7]<br>1001: ts_sync<br>default: ts_err<br>mode_ctrl7[7:4] are TS_SYNC output select signals. ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_sync<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[4]<br>0110: ts_dat_tmp[5]<br>0111: ts_dat_tmp[6]<br>1000: ts_dat_tmp[7]<br>1001: ts_val<br>default: ts_err |

## ioshare_ctrl_9

ioshare_ctrl_9 is IOSHARE control register 9.

| Offset Address | Register Name | Total Reset Value |
|---|---|---|
| 0x29 | ioshare_ctrl_9 | 0x00 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | mode_ctrl8 | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bits | Access | Name | Description |
|---|---|---|---|
| [7:0] | RW | mode_ctrl8 | mode_ctrl8[3:0] are TS_ERR output select signals. ts_dat_tmp is ts_dat controlled by mode_sel[0].<br>0000: ts_err<br>0001: ts_dat_tmp[0]<br>0010: ts_dat_tmp[1]<br>0011: ts_dat_tmp[2]<br>0100: ts_dat_tmp[3]<br>0101: ts_dat_tmp[4]<br>0110: ts_dat_tmp[5]<br>0111: ts_dat_tmp[6]<br>1000: ts_dat_tmp[7]<br>1001: ts_sync<br>default: ts_val<br>mode_ctrl8[7:4] are reserved. |

# Contents

# Figures

# Tables

# 3 Hardware

## 3.1 Package and Pins

### 3.1.1 Package and Pinout

#### 3.1.1.1 Package

Hi3130 V200 uses the quad flat non-leaded (QFN) package. It has 40 pins, its body size is 5 mm x 5 mm (0.020 in. x 0.020 in.), and its pin pitch is 0.4 mm (0.016 in.). Figure 3-1 shows the package views, and Figure 3-2 shows the package dimensions.

**Figure 3-1** Package views

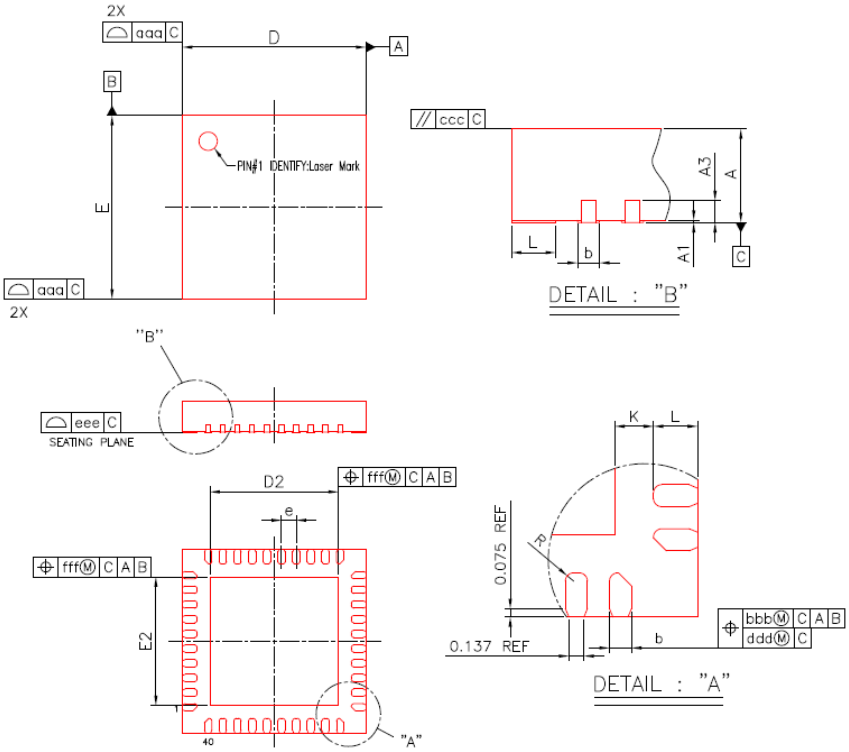


**Figure 3-2** Package dimensions

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| K | 0.20 | --- | --- | 0.008 | --- | --- |
| R | 0.075 | --- | --- | 0.003 | --- | --- |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.07 | | | 0.003 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.05 | | | 0.002 | | |
| eee | 0.08 | | | 0.003 | | |
| fff | 0.10 | | | 0.004 | | |

| Exposed Pad Size | | | | | | |
|---|---|---|---|---|---|---|
| L/F | Dimension in mm | | | Dimension in inch | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| D2/E2 | 3.55 | 3.70 | 3.85 | 0.140 | 0.146 | 0.152 |

### 3.1.1.2 Pinout

## Pin Quantity

The Hi3130 V200 QFN has 40 pins. Table 3-1 lists the number of each type of pins on Hi3130 V200.

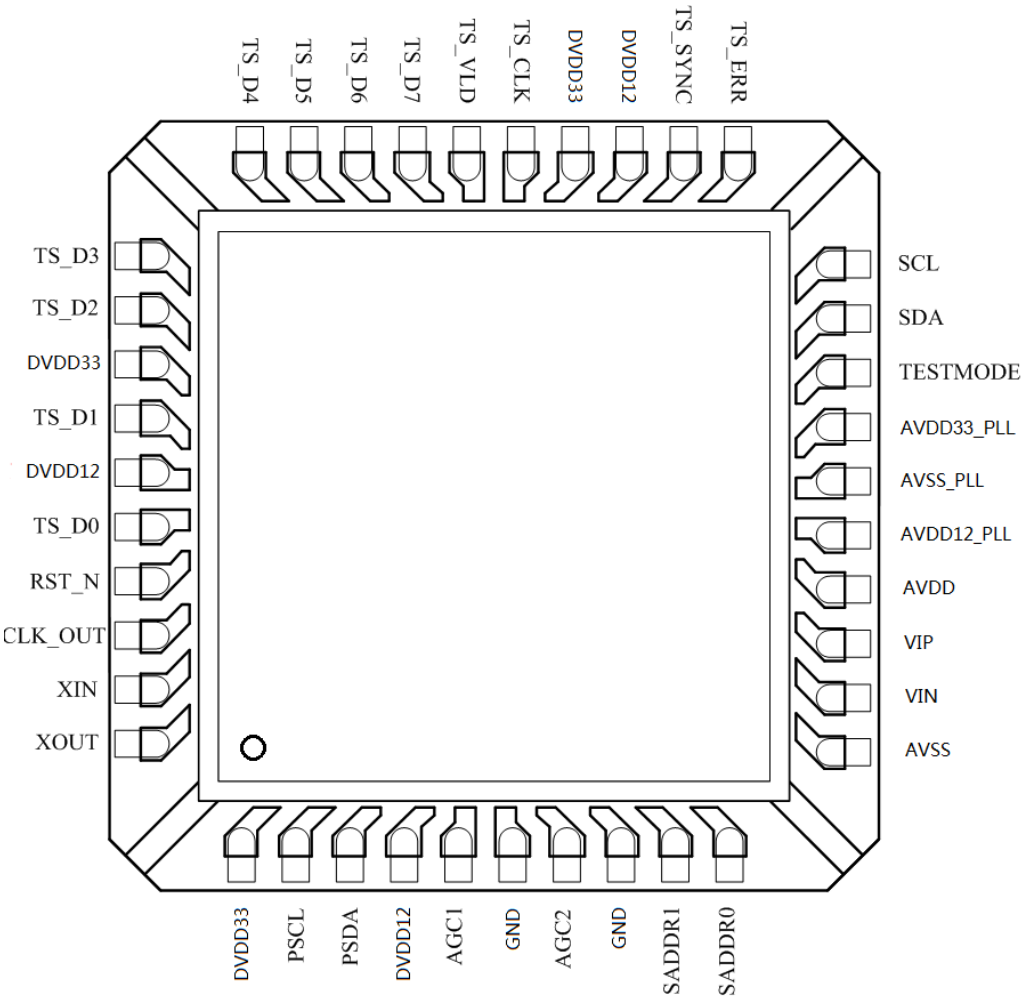
**Table 3-1** Pin quantity by pin type

| Pin Type | Quantity |
|---|---|
| I/O (signal) | 27 |
| Digital power | 6 |
| Digital ground (GND) | 2 |
| Others/Analog power | 3 |
| Others/Analog GND | 2 |
| Total | 40 |

## Pin Map

Figure 3-3 shows the pin map of the Hi3130 V200 QFN.

**Figure 3-3** Pin map of the Hi3130 V200 QFN




# 3.1.2 Pin Description

## Pin Types

Table 3-2 describes the I/O pin types.

**Table 3-2** I/O pin types

| I/O | Description |
|---|---|
| I | Input signal |
| $I_{PD}$ | Input signal, internal pull-down |
| $I_{PU}$ | Input signal, internal pull-up |

| I/O | Description |
|---|---|
| $I_S$ | Input signal with a Schmitt trigger |
| $I_{SPD}$ | Input signal with a Schmitt trigger, internal pull-down |
| $I_{SPU}$ | Input signal with a Schmitt trigger, internal pull-up |
| O | Output signal |
| $O_{OD}$ | Output open drain (OD) |
| I/O | Bidirectional (input/output) signal |
| $I_{PD}$/O | Bidirectional signal, input pull-down |
| $I_{PU}$/O | Bidirectional signal, input pull-up |
| $I_{SPU}$/O | Bidirectional signal with a Schmitt trigger, input pull-up |
| $I_{PD}$/$O_{OD}$ | Bidirectional signal, input pull-down and output OD |
| $I_{PU}$/$O_{OD}$ | Bidirectional signal, input pull-up and output OD |
| $I_S$/O | Bidirectional signal, input with a Schmitt trigger |
| $I_S$/$O_{OD}$ | Bidirectional signal, input with a Schmitt trigger and output OD |
| CIN | Crystal oscillator input |
| COUT | Crystal oscillator output |
| P | Power supply |
| G | GND |

## Pin Arrangement

Table 3-3 lists the pins of Hi3130 V200 in order.

**Table 3-3** Pin arrangement

| Position | Pin Name | Position | Pin Name |
|---|---|---|---|
| 1 | DVDD33 | 21 | TS_ERR |
| 2 | PSCL | 22 | TS_SYNC |
| 3 | PSDA | 23 | DVDD12 |
| 4 | DVDD12 | 24 | DVDD33 |
| 5 | AGC1 | 25 | TS_CLK |
| 6 | GND | 26 | TS_VLD |
| 7 | AGC2 | 27 | TS_D7 |
| 8 | GND | 28 | TS_D6 |

| Position | Pin Name | Position | Pin Name |
|---|---|---|---|
| 9 | SADDR1 | 29 | TS_D5 |
| 10 | SADDR0 | 30 | TS_D4 |
| 11 | AVSS | 31 | TS_D3 |
| 12 | VIN | 32 | TS_D2 |
| 13 | VIP | 33 | DVDD33 |
| 14 | AVDD | 34 | TS_D1 |
| 15 | AVDD12_PLL | 35 | DVDD12 |
| 16 | AVSS_PLL | 36 | TS_D0 |
| 17 | AVDD33_PLL | 37 | RST_N |
| 18 | TESTMODE | 38 | CLK_OUT |
| 19 | SDA | 39 | XIN |
| 20 | SCL | 40 | XOUT |

## Clock Pins

Table 3-4 describes clock pins.

**Table 3-4** Clock pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 39 | XIN | CIN | None | None | Crystal oscillator input (from crystal) or external clock input. The frequency is 28.8 MHz. |
| 40 | XOUT | COUT | None | None | Crystal oscillator output (to crystal). |
| 38 | CLK_OUT | O | 4 | 3.3 | Auxiliary clock output. The frequency is the same as the crystal frequency. It can be disabled. |

## Multiplexed Pin

Table 3-5 describes the multiplexed pin.

**Table 3-5** Multiplexed pin

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 37 | RST_N | $I_{SPU}$ | None | 3.3 | Asynchronous reset, active low. |

## ADC Pins

Table 3-6 describes ADC pins.

**Table 3-6** ADC pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 13 | VIP | I | None | None | Differential analog input signal, positive. The typical value is 0.5 Vpp in single-ended input mode (1 Vpp in differential input mode). |
| 12 | VIN | I | None | None | Differential analog input signal, negative. |
| 14 | AVDD | P | None | 1.2 | 1.2 V ADC analog power. |
| 11 | AVSS | G | None | None | ADC analog power GND. |

## PLL Pins

Table 3-7 describes PLL pins.

**Table 3-7** PLL pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 15 | AVDD12_PLL | P | None | 1.2 | 1.2 V PLL analog power. |
| 17 | AVDD33_PLL | P | None | 3.3 | 3.3 V PLL analog power. |
| 16 | AVSS_PLL | G | None | None | PLL analog power GND. |

## I²C Bus Pins

Table 3-8 describes $I^2C$ bus pins.

**Table 3-8** $I^2C$ bus pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 20 | SCL | $I_S$ | None | 3.3 | $I^2C$ bus clock.<br>The maximum frequency is 400 kHz. |
| 19 | SDA | $I_S/O_{OD}$ | None | 3.3 | $I^2C$ bus data. |
| 2 | PSCL | $O_{OD}$ | None | 3.3/5 | $I^2C$ bus clock output.<br>The maximum frequency is 400 kHz. |
| 3 | PSDA | $I_S/O_{OD}$ | None | 3.3/5 | $I^2C$ bus data output. |
| 9/10 | SADDR 1/0 | I | None | 3.3 | $I^2C$ bus address specified by SADDR[1:0].<br>The address is {10100,SADDR[1:0]}. |

## AGC Pins

Table 3-9 describes automatic gain control (AGC) pins.

**Table 3-9** AGC pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 5 | AGC1 | O/ $O_{OD}$ | 8 | 3.3/5 | Radio frequency (RF) AGC output. This function is invalid in the single AGC application. |
| 7 | AGC2 | O/ $O_{OD}$ | 8 | 3.3/5 | Intermediate frequency (IF) AGC output. |

## TS Pins

Table 3-10 describes TS pins.

**Table 3-10** TS pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 36/34/32–27 | TS_D0–TS_D7 | O | 8 | 3.3 | Parallel or serial MPEG-TS output. (The TS_D0 pin is used in serial mode by default.) |
| 25 | TS_CLK | O | 8 | 3.3 | Parallel or serial MPEG-TS clock output.<br>The maximum frequency is 86.6 MHz. |
| 26 | TS_VLD | O | 8 | 3.3 | MPEG-TS output flag. |
| 22 | TS_SYNC | O | 8 | 3.3 | MPEG-TS frame sync pulse. |
| 21 | TS_ERR | O | 8 | 3.3 | Reed-Solomon (RS) decoding error indicator. |

## Test Pin

Table 3-11 describes the test pin.

**Table 3-11** Test pin

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 18 | TESTMODE | I | None | None | Test pin. It connects to GND in normal mode. |

## Digital Power Pins

Table 3-12 describes digital power pins.

**Table 3-12** Digital power pins

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 1/24/33 | DVDD33 | P | None | 3.3 | 3.3 V digital I/O power. |

| Position | Pin Name | Type | Drive Current (mA) | Voltage (V) | Description |
|---|---|---|---|---|---|
| 4/23/35 | DVDD12 | P | None | 1.2 | 1.2 V digital core power. |
| 6/8 | GND | G | None | None | Digital power GND. |

# 3.2 Electrical Specifications

## 3.2.1 Power Consumption Specifications

Table 3-13 describes the power consumption specifications of Hi3130 V200.

**Table 3-13** Power consumption specifications

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DVDD33 | Digital I/O power | TBD | TBD | TBD | mA |
| DVDD12 | Digital core power | TBD | TBD | TBD | mA |
| AVDD | ADC analog power | TBD | TBD | TBD | mA |
| AVDD33_PLL | PLL analog power | TBD | TBD | TBD | mA |
| AVDD12_PLL | PLL analog power | TBD | TBD | TBD | mA |

## 3.2.2 Rated Working Conditions

**CAUTION**

Hi3130 V200 may be unstable or damaged when working beyond the rated working conditions listed in Table 3-14.

**Table 3-14** Rated working conditions

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| DVDD33 | Digital I/O power | –0.5 | 4.6 | V |
| DVDD12 | Digital core power | –0.5 | 1.8 | V |
| AVDD | ADC analog power | –0.5 | 1.8 | V |

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| AVDD33_PLL | PLL analog power | –0.5 | 4.6 | V |
| AVDD12_PLL | PLL analog power | –0.5 | 1.8 | V |

## 3.2.3 Recommended Working Conditions

Table 3-15 describes the recommended working conditions.

**Table 3-15** Recommended working conditions

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{OPT}$ | Operating environment temperature | 0 | None | 70 | °C |
| DVDD12 | Digital core power | 1.08 | 1.2 | 1.32 | V |
| DVDD33 | Digital I/O power | 2.97 | 3.3 | 3.63 | V |
| AVDD12_PLL | PLL analog power | 1.08 | 1.2 | 1.32 | V |
| AVDD33_PLL | PLL analog power | 2.97 | 3.3 | 3.63 | V |
| AVDD | ADC analog power | 1.08 | 1.2 | 1.32 | V |

## 3.2.4 DC Electrical Specifications

Table 3-16 describes the direct current (DC) electrical specifications.

**Table 3-16** DC electrical specifications

| Symbol | Description | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| DVDD33 | Digital I/O voltage | 2.97 | 3.3 | 3.63 | V | None |
| $V_{IH}$ | Input high voltage | 2.0 | None | DVDD33 + 0.3 | V | 5 V input voltage is not supported. |
| $V_{IL}$ | Input low voltage | –0.3 | None | 0.8 | V | None |
| $I_L$ | Input leakage current | –1 | None | +1 | μA | None |
| $I_{OZ}$ | Tristate output leakage current | –1 | None | +1 | μA | None |
| $V_{OH}$ | Output high voltage | 2.4 | None | None | V | None |
| $V_{OL}$ | Output low voltage | None | None | 0.4 | V | None |

### 3.2.5 Power-On Sequence

The I/O power is turned on before the core power.

## 3.3 Design Recommendations for Schematic Diagrams

### 3.3.1 Power Supply

**NOTE**

For details about system power supply design, see the schematic diagram of the Hi3130 V200 demo board.

Hi3130 V200 has five types of power supplies: 3.3 V digital I/O power DVDD33, 1.2 V core power DVDD12, 3.3 V PLL analog power AVDD33, 1.2 V PLL analog power AVDD12, and 1.2 V ADC power AVDD.

The I/O power DVDD33 is digital power. It is supplied by the on-board 3.3 V digital power shared with the I/O power of the master chip, or supplied by any other power such as the 5 V power that is regulated to 3.3 V with a low dropout regulator (LDO) or by DC-DC conversion. Each DVDD33 pin connects to a 100 nF decoupling capacitor, which is placed close to the power supply pin.

The core power DVDD12 is digital power. It is supplied by the on-board 1.2 V power shared with the core power of the master chip (if the core power of the master chip is 1.2 V), or supplied by any other power such as the 5 V or 3.3 V power that is regulated to 1.2 V with an LDO or by DC-DC conversion. Each DVDD12 pin connects to a 100 nF decoupling capacitor, which is placed close to the power supply pin.

The PLL power AVDD33 is analog power. It is supplied by DVDD33 that connects to 10 μF and 100 nF filtering capacitors and then to GND after being isolated by using an electromagnetic interference (EMI) bead. The filtering capacitors are placed close to the power supply pin.

The PLL power AVDD12 is analog power. It is supplied by DVDD12 that connects to 10 μF and 100 nF filtering capacitors and then to GND after being isolated by using an EMI bead. The filtering capacitors are placed close to the power supply pin.

The ADC power AVDD is analog power. It is supplied by DVDD12 that connects to 10 μF and 100 nF filtering capacitors and then to GND after being isolated by using an EMI bead. The filtering capacitors are placed close to the power supply pin.

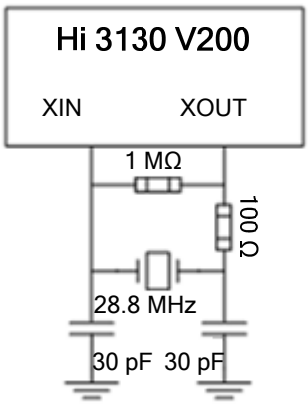
**CAUTION**

- Isolate the analog power from the digital power by using EMI beads to prevent interference to the analog power from digital noises.
- Do not generate the 1.2 V power by converting the 1.5 V power for the DDR3.

## 3.3.2 Clock Circuit

The system clock can be generated by combining the internal feedback circuit of Hi3130 V200 with an external 28.8 MHz crystal oscillator circuit. Figure 3-4 shows the recommended connection mode of the crystal oscillator.

**Figure 3-4** Recommended connection mode of the crystal oscillator

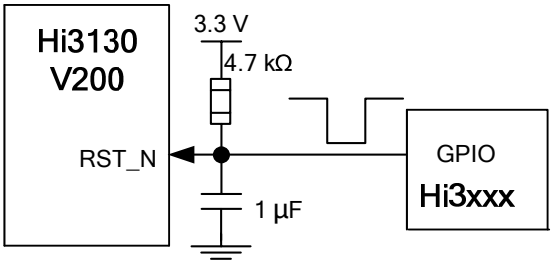



The system clock can also be generated by using the external clock circuit and input over the XIN pin. The CLK_OUT pin can output the 28.8 MHz clock (3.3 V CMOS) for other components. This pin is floated when it is not in use.

## 3.3.3 Reset Circuit

The RST_N pin of Hi3130 V200 is a reset signal input pin. The valid reset signal must have low-level pulses. The RST_N pin can connect to a typical resistor–capacitor (RC) power-on reset circuit, or directly connect to a specific GPIO pin of the master chip to generate a reset signal. The latter mode is more flexible. Figure 3-5 shows the recommended connection mode of the reset circuit.

**Figure 3-5** Recommended connection mode of the reset circuit




If the RC power-on reset is used, ensure that the reset signal is valid after the power is on, and the valid duration of low-level pulses is at least 2 us. This is especially important in low-power standby mode design, in which the reset signal uses the power for the standby mode.

# 3.3.4 Tuner Interfaces

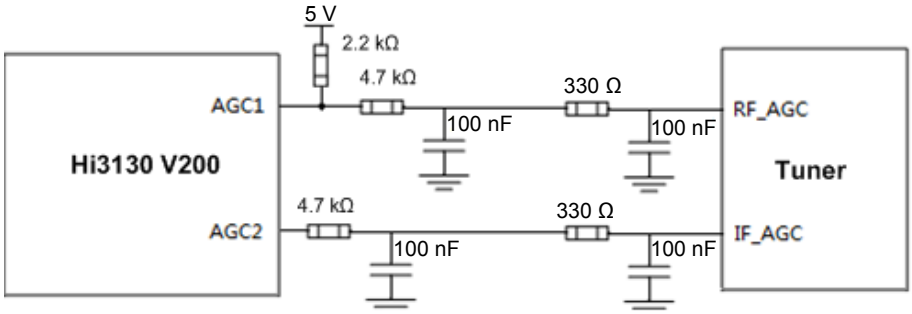
## AGC Circuit

The AGC circuit dynamically adjusts the amplifier gain for the receiver to maintain an approximately constant signal strength based on the average power consumption of the input signals. The PWM signals output by the AGC pins of Hi3130 V200 generate analog voltage to control the internal amplifier of the tuner by using filters, meeting the input power requirement. The AGC circuit uses two-order RC filters. You are advised to connect the first-order RC filter close to Hi3130 V200, and the second-order RC filter close to the tuner.

Early tuners require two AGC signals: RF_AGC and IF_AGC. The control voltage required by the RF amplifier is greater than 3.3 V, which is implemented by connecting the AGC OD output to an external pull-up resistor and then to the 5 V power or adjusting the pull-up or pull-down resistor. The amplifier features vary according to the tuners. Therefore, you must evaluate the amplifier features and adjust AGC parameters (including the maximum value, minimum value, and threshold) when replacing the tuner to meet requirements of the minimum level, maximum level, and anti adjacent-channel interference (ACI) feature.

Currently most tuners use the RF_AGC internal loop mode, and only the IF amplifier needs to be controlled externally. That is, only IF_AGC is output in CMOS output mode, and no external pull-up resistor is required. The AGC parameter values that are within specified ranges apply to various tuners. Figure 3-6 shows the recommended connection mode of the AGC circuit.

**Figure 3-6** Recommended connection mode of the AGC circuit



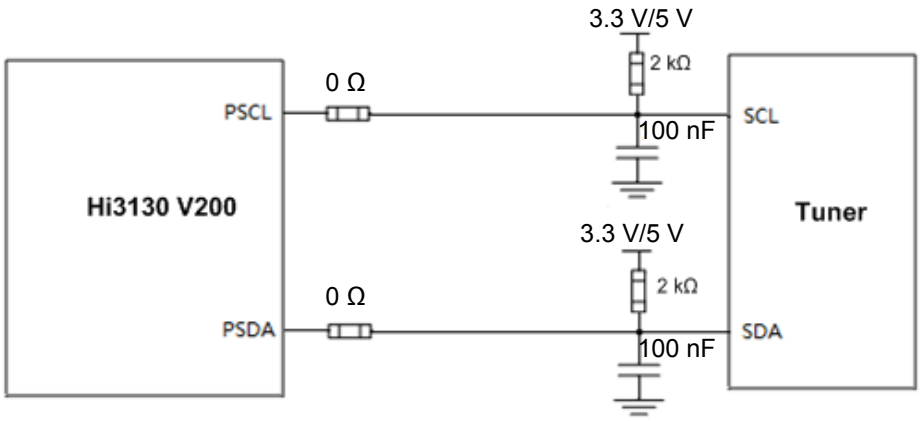

**NOTE**

The AGC1 pin and its circuit are required only when Hi3130 V200 connects to the tuner whose RF_AGC needs to be controlled externally. Otherwise, this pin is floated.

## I²C Circuit

Hi3130 V200 accesses and configures tuner registers over the $I^2C$ bus, which works at a maximum of 400 kHz. As required by the tuner, the $I^2C$ bus must connect to the 3.3 V or 5 V power through pull-up resistors and connect to resistors in series. The $I^2C$ bus must also connect to pF-level bypass filtering capacitors that are close to the tuner pins to filter out interference signals for the tuner. Figure 3-7 shows the recommended connection mode of the $I^2C$ circuit.

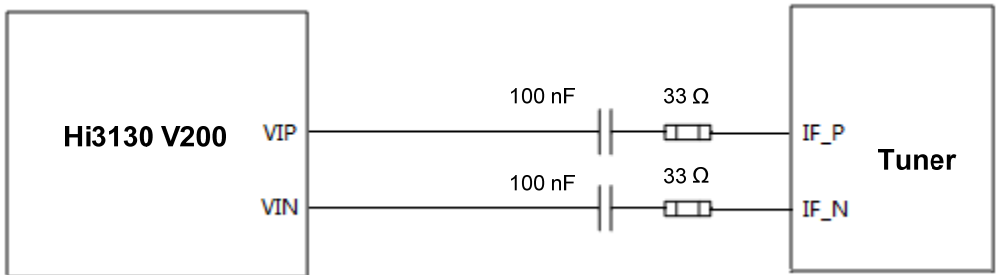
**Figure 3-7** Recommended connection mode of the I²C circuit




## IF Circuit

The IF interface is the traffic channel between Hi3130 V200 and the tuner. This interface uses differential signals to improve the anti-interference capability. The positive and negative differential signals are reversible. The differential traces will not be crossed in the printed circuit board (PCB) design. The IF circuit requirements vary according to the tuners. Figure 3-8 shows the common connection mode of the IF circuit. The IF traces connect to a capacitor and a resistor in series. The capacitor implements alternating current (AC) coupling of signals, and the resistor adjusts the signal range.

**Figure 3-8** Common connection mode of the IF circuit




# 3.3.5 Decoder Interfaces

## Introduction

Hi3130 V200 connects to the decoder over digital interfaces at the 3.3 V, LVCMOS level. The following digital interfaces are involved:

- One TS serial/parallel interface. The working mode can be set to parallel or serial. The working clock frequency is 60 MHz in serial mode or 7.5 MHz in parallel mode. The bit width is 1 bit in serial mode or 8 bits in parallel mode. All the TS pins, except the clock pin, can be flexibly configured to implement the functions of required TS signals, facilitating PCB routing.

- One $I^2C$ interface. The decoder accesses the internal registers of Hi3130 V200 and tuner over the $I^2C$ interface. The maximum $I^2C$ working clock frequency is 400 kHz.

## Connection Mode

Figure 3-9 shows the typical topology in which Hi3130 V200 connects to a decoder over the TS serial interface. Figure 3-10 shows the typical topology in which Hi3130 V200 connects to a decoder over the TS parallel interface.

**Figure 3-9** Topology in which Hi3130 V200 connects to a decoder over the TS serial interface

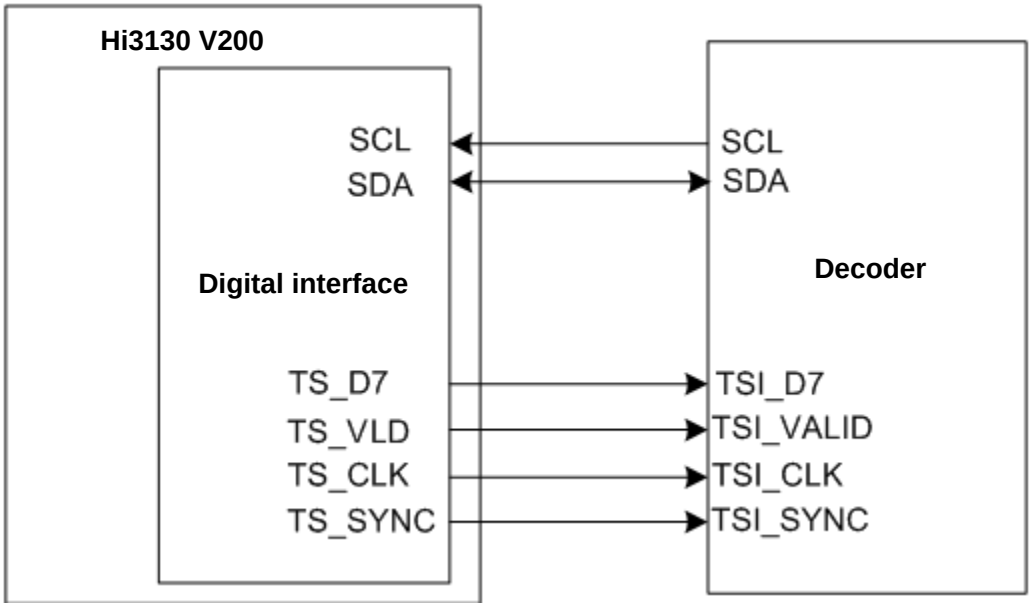
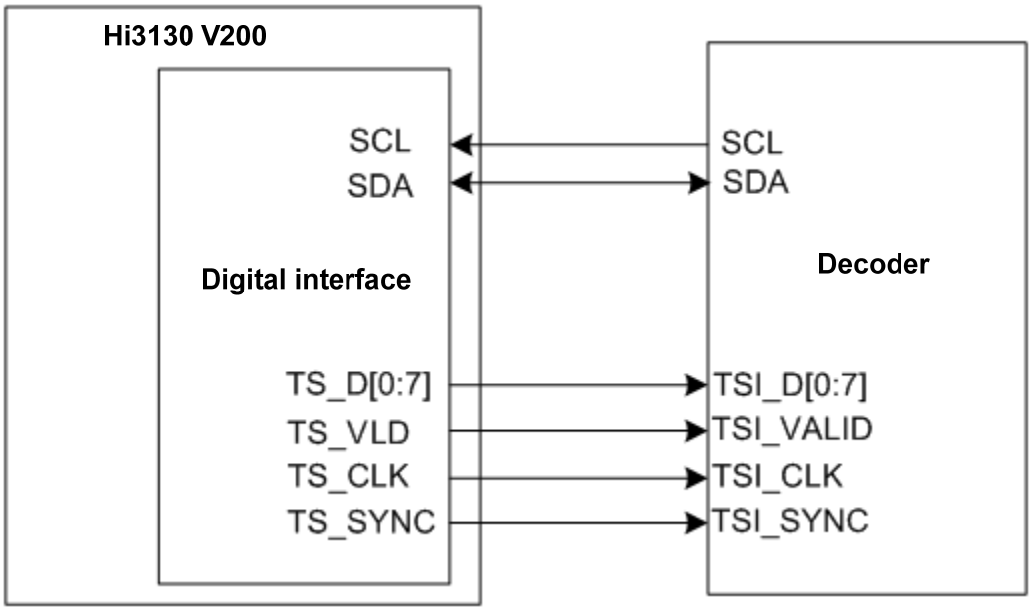



**Figure 3-10** Topology in which Hi3130 V200 connects to a decoder over the TS parallel interface



**NOTE**

If the decoder does not have the TS_ERR pin, the TS_ERR pin of Hi3130 V200 is floated.

## I²C Design Recommendations

The I²C bus between Hi3130 V200 and a decoder connects to a 2 kΩ pull-up resistor and then to the 3.3 V power, depending on the I²C bus rate. A 100 pF or less bypass filtering capacitor is connected on the I²C bus close to the Hi3130 V200 I²C pin.

**NOTE**

The I²C address of Hi3130 V200 is {10100, SADDR[1:0]}, the lower two bits of which are determined by pulling the SADDR1 or SADDR0 pin up or down. Therefore, a maximum of four Hi3130 V200s can be connected on a I²C bus.

In a solution in which Hi3130 V200 works with a Hi3*XXXX* decoder chip, the master chip can read and write to Hi3130 V200 registers over the I²C interface by using the following commands:

- **echo** *A B C D* **>/proc/msp/i2c** (for HD chips)
- **echo** *A B C D* >**/proc/i2c** (for SD chips)

In the preceding commands:

- *A* is the I²C channel of the master chip, which depends on the hardware connection.
- *B* is the hexadecimal I²C address of Hi3130 V200 (the first seven bits and the last bit are stuffed with 0s). When the SADDR1 and SADDR0 pins both connect to GND, *B* is a0 (you cannot write **0x4a** in the command).
- *C* is the hexadecimal address of an Hi3130 V200 register to be read or written, for example, 4a (you cannot write **0x4a** in the command).
- *D* is the hexadecimal value to be written to an Hi3130 V200 register, for example, 7f (you cannot write **0x7f** in the command). If there are only read operations, *D* is not involved.

## TS Matching Design Recommendations

The TS matching design is provided based on the number of PCB layers:

- If more than two PCB layers are designed, the trace characteristic impedance is 50 Ω.
  - A 33 Ω resistor is connected in series close to each pin of TS_D[0:7]. For details about the topology, see Figure 3-11.
  - A 33 Ω resistor is connected in series close to each of TS_CLK, TS_SYNC, and TS_VLD. For details about the topology, see Figure 3-12.
- If two PCB layers are designed, the trace characteristic impedance is 140 Ω.
  - A 75 Ω resistor is connected in series close to each pin of TS_D[0:7]. For details about the topology, see Figure 3-13.
  - A 75 Ω resistor is connected in series close to each of TS_CLK, TS_SYNC, and TS_VLD. For details about the topology, see Figure 3-14.

**NOTE**

- The TS pins that are not in use are floated.
- The length 5000 mils shown in the topologies is the maximum trace length.

**Figure 3-11** Interconnection topology for TS_D[0:7] and a decoder chip when more than two PCB layers are designed

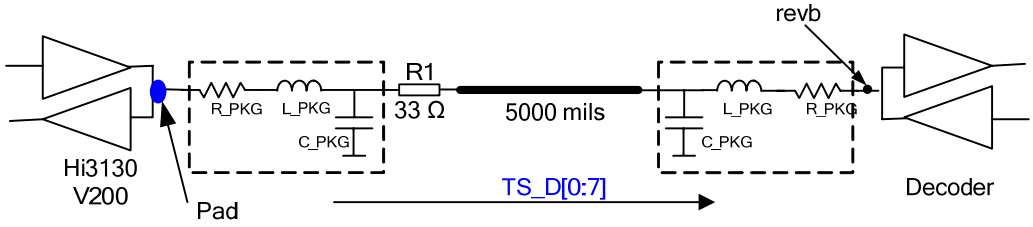



**Figure 3-12** Interconnection topology for TS_CLK/TS_SYNC/TS_VLD and a decoder chip when more than two PCB layers are designed

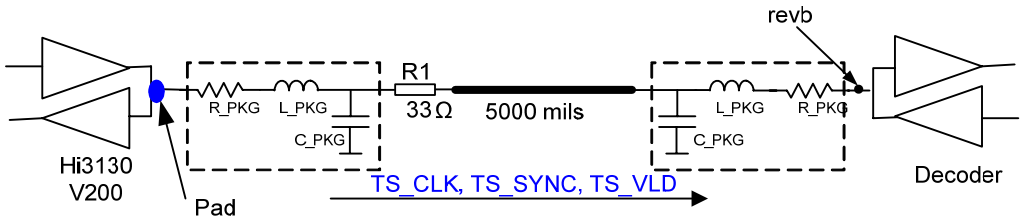



**Figure 3-13** Interconnection topology for TS_D[0:7] and a decoder chip when two PCB layers are designed

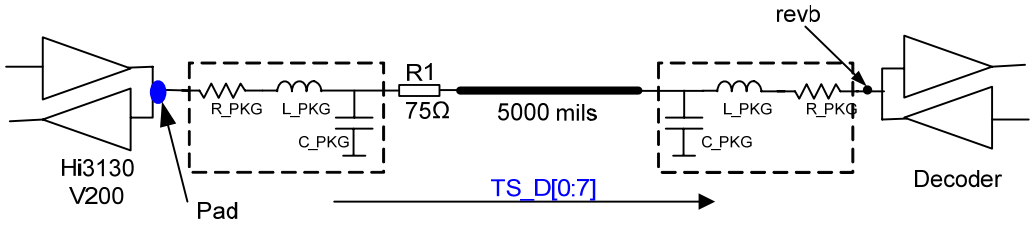
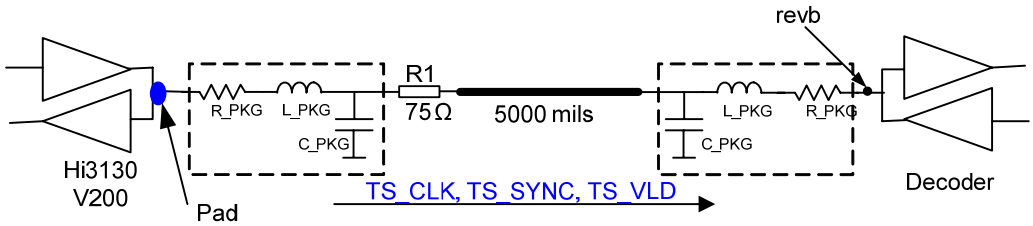



**Figure 3-14** Interconnection topology for TS_CLK/TS_SYNC/TS_VLD and a decoder chip when two PCB layers are designed



# 3.4 PCB Design Recommendations

## 3.4.1 Stack and Layout

### Stack

Hi3130 V200 uses the QFN package. It has 40 pins, and its pin pitch is 0.4 mm (0.016 in.).

You are advised to design a 4-layer PCB with the following stack:

- Top layer: signal traces
- Internal layer 1: GND plane
- Internal layer 2: power plane
- Bottom layer: signal traces

To reduce the cost, you can also design a 2-layer PCB with the following stack:

- Top layer: signal traces and part of power traces
- Bottom layer: GND plane and part of power traces

The PCB design precautions are as follows:

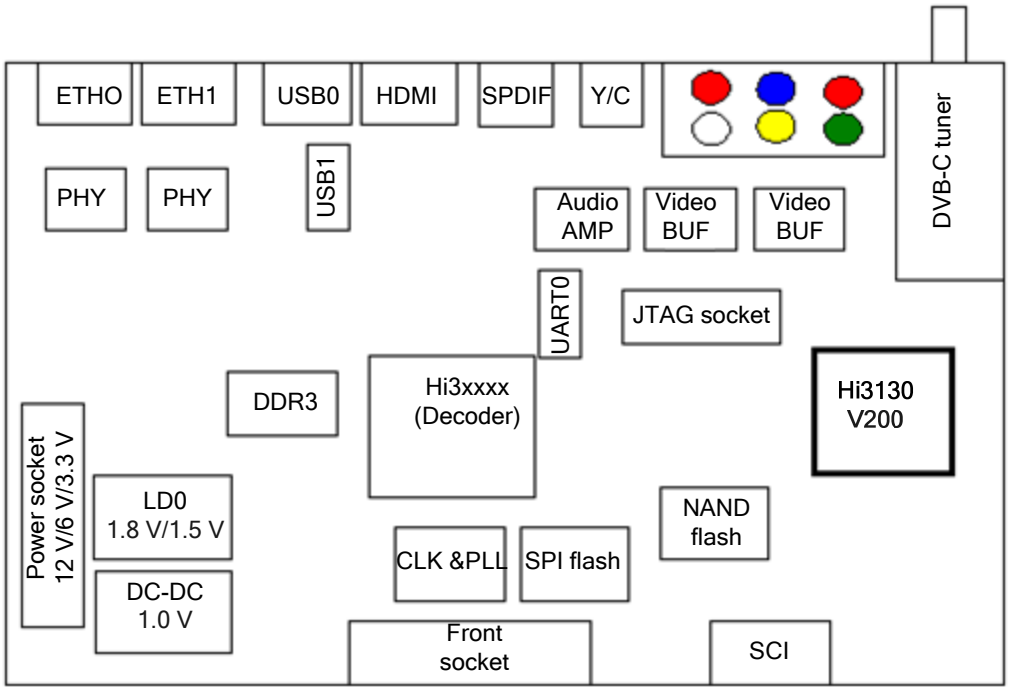
- Components and signal traces are routed at the top layer, and filtering capacitors with small capacitance are placed at the bottom layer.
- Power pins are connected by using wide traces.
- Ensure that the bottom layer is a complete GND plane.
- The recommended via diameter is 8 mils and the trace width is 5 mils.

The PCB material is FR-4, the PCB thickness is 1.6 mm (0.06 in.), and the copper foil thickness is 1 oz.

### Board Layout

Figure 3-15 shows the board layout for the Hi3130 V200 reference design.

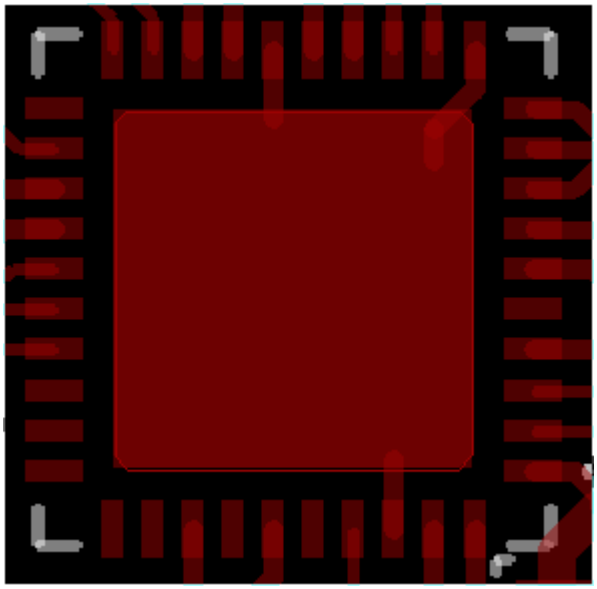
**Figure 3-15** Board layout




## Fanout Package

Figure 3-16 shows the PCB fanout design.

**Figure 3-16** PCB fanout design



# 3.4.2 PCB Design Recommendations for the Small System

## 3.4.2.1 Power Circuits

### Digital Power

The digital power supplies of Hi3130 V200 are the 3.3 V I/O power DVDD33 and 1.2 V core power DVDD12. Hi3130 V200 shares the 3.3 V and 1.2 V digital power with the decoder chip on the board. The exposed pad of Hi3130 V200 is used as the reference GND. The traces should be as wide as possible when the through-flow capacity is ensured. Ensure that digital power and analog power planes do not overlap and decoupling capacitors are placed close to Hi3130 V200.

### Analog Power

The analog power supplies must be isolated from other power supplies by using EMI beads or generated by other power supplies using the LDO. The analog power supplies use the exposed pad of Hi3130 V200 as the reference GND. The design recommendations are as follows:

- Never route digital signal traces especially high-speed digital signal traces in the analog power area.
- Connect a decoupling capacitor to each power pin. Ensure that traces are as wide as possible and decoupling capacitors are placed close to Hi3130 V200.

### GND

The signals of the tuner and QAM ADC module are analog signals. On a board that has mixed signals, analog circuits are susceptible to interference, which may affect indicators such as the signal to noise ratio (SNR). The following are the recommendations:

- Use a complete GND plane, and do not route traces across GND plane splits.
- Route power and signal traces in analog and digital zones respectively.

## 3.4.2.2 Clock and Reset Circuits

### Clock Circuit

The clock circuit of Hi3130 V200 consists of the external crystal circuit and the power and GND circuits of the PLL units (AVDD12_PLL, AVDD33_PLL, and AVSS_PLL). Design the PCB according to the following guidelines:

- AVDD12_PLL is the 1.2 V PLL power. You are advised to isolate it from the board's 1.2 V digital power by using EMI beads. The level deviation of the 1.2 V power must be within ±5%.
- AVDD33_PLL is the 3.3 V PLL power. You are advised to isolate it from the 3.3 V digital power by using EMI beads. The level deviation of the 3.3 V power must be within ±5%.
- AVSS_PLL is the reference GND of the PLL circuit. The AVDD12_PLL, AVDD33_PLL, and the decoupling capacitors of AVDD33_PLL must be connected by referencing AVSS_PLL as the GND plane. AVSS_PLL must connect to the board's digital GND through a single point.
- Place the crystal close to Hi3130 V200 and at least 1000 mils away from the board edge. Never route traces under the crystal. The traces of the circuit must be at most 1/20 of the

wavelength corresponding to the crystal oscillator frequency in length, and surrounded by GND traces.

### Reset Circuit

Pin 37 is a reset pin. The reset signal trace is a critical trace and is susceptible to interference. The following are design recommendations:

- If more than two PCB layers are designed, route the reset signal trace at an inner layer close to the GND plane. If two PCB layers are designed, ensure that the reset signal trace is surrounded by GND traces.
- Route the reset signal trace at least 1000 mils away from interfaces and power inputs.

## 3.4.3 PCB Design Recommendations for Digital and Analog Interfaces

### 3.4.3.1 Digital Interfaces

### TS Signals

The following are TS signal requirements:

- The maximum signal trace length is 5000 mils.
- The length of all TS signal traces is determined based on the TS_CLK traces. The length deviation is ±100 mils.
- The serial matched resistors are connected close to Hi3130 V200.
- If two PCB layers are designed, the characteristic impedance of the TS signal trace should be 140 Ω. A 75 Ω matched resistor is recommended.
- If more than two PCB layers are designed, the characteristic impedance of the TS signal trace should be 50 Ω. A 33 Ω matched resistor is recommended.

### I²C Bus

The following are recommendations for the $I^2C$ traces:

- The maximum serial clock (SCL) trace length is 5000 mils.
- The serial data (SDA) traces are routed based on SCL traces. The allowed length deviation is ±100 mils.

### PCB Routing Recommendations

Route traces on a PCB according to the following guidelines:

**CAUTION**

The digital signal traces at all PCB layers must be routed in the digital part of the PCB.

Never cross the reference GND plane of TS signal traces when routing other signal traces, and ensure that GND traces are routed around signal traces. Place serial resistors close to Hi3130 V200. For details, see the PCB design document of the demo board.

- Route all the TS signal traces on the planes adjacent to the GND plane. Never route the signal traces across the power and GND plane splits. Ensure that signal traces have a complete reference GND plane.
- To ensure a good signal return path, punch vias around signal traces and changed layers and connect the punched vias to GND.
- Ensure that signal traces are as short as possible. Minimize the use of vias to ensure the impedance continuity of traces. If more than two PCB layers are designed, the characteristic impedance of the single-ended PCB signal trace is 50 Ω±10%. If two PCB layers are designed, the characteristic impedance of the single-ended PCB signal trace is 140 Ω±10%. The serial matched resistors are placed close to Hi3130 V200.
- If resistor networks are used, ensure that the TS_CLK trace and TS traces are not routed on the same resistor network.
- Ensure that the spacing between adjacent signal traces is 2–3 times of the trace width according to the 3W rule. The 3W rule indicates that the trace spacing is three times of the trace width.
- Route clock signal traces far away from the data and address buses.

### 3.4.3.2 Analog Interface Design

Route traces on a PCB according to the following guidelines:

**CAUTION**

The analog signal traces at all PCB layers must be routed in the analog part of the PCB.

The intermediate-frequency (ADC input) signals VIP/VIN are routed in differential mode. The trace impedance is not restricted. The trace length must be within 3 inches. It is recommended that the intermediate-frequency signals are surrounded with GND traces.

Table 3-17 describes the recommended match design for signals of the analog interface.

**Table 3-17** Recommended match design for signals of the analog interface

| Signal | Two-Layer PCB | Four-Layer PCB |
|---|---|---|
| VIP/VIN | AC coupled. A 33 Ω resistor and a 0.1 µF capacitor are connected in series close to the tuner. | AC coupled. A 33 Ω resistor and a 0.1 µF capacitor are connected in series close to the tuner. |

| Signal | Two-Layer PCB | Four-Layer PCB |
|---|---|---|
| PSDA/PSCL | A 33 Ω resistor is connected in series close to Hi3130 V200, and a 2 kΩ pull-up resistor is connected close to the tuner. | A 33 Ω resistor is connected in series close to Hi3130 V200, and a 2 kΩ pull-up resistor is connected close to the tuner. |
| AGC1/AGC2 | The first-order RC filter is connected close to Hi3130 V200, and the second-order RC filter is connected close to the tuner. | The first-order RC filter is connected close to Hi3130 V200, and the second-order RC filter is connected close to the tuner. |

#### 3.4.3.3 Others

**Integrity Simulation Design Recommendations for PCB Signals**

By using board-level simulation tools, PCB designers can simulate and analyze signal integrity based on the input/output buffer information specification (IBIS) models of the Hi3130 V200 interfaces and interconnected components, transmission line models, and board topologies. Based on the simulation results, the PCB designers can adjust the typologies to meet the signal quality requirements in overshoot, undershoot, ringing, monotonicity, and others.

**Note**

If a clock signal trace connects to multiple loads, ensure good signal quality especially signal edge monotonicity regardless of the frequency.

## 3.5 Thermal Design Recommendations

### 3.5.1 Rated Operating Environment

Table 3-18 describes rated operating environment parameters.

**NOTE**

The rated operating environment parameters are provided only for evaluation.

**CAUTION**

Hi3130 V200 may be damaged when working beyond the rated operating environment conditions listed in Table 3-18

**Table 3-18** Rated operating environment parameters

| Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Ambient temperature | $T_A$ | –20 | 70 | °C |
| Junction temperature | $T_{JMAX}$ | None | 125 | °C |
| Pin voltage | Vin | –0.5 | 4.6 | V |

## 3.5.2 Recommended Operating Environment

Table 3-19 describes recommended operating environment parameters. The derating standards during thermal design are subject to the data provided in Table 3-19.

**Table 3-19** Recommended operating environment parameters

| Description | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient temperature | $T_A$ | 0 | 25 | 55 | °C |
| Long-term junction temperature | $T_{JMAX}$ | None | None | 125 | °C |

## 3.5.3 Junction Temperature Requirements

## 3.5.4 Package Thermal Resistance

Table 3-20 describes the package thermal resistance of Hi3130 V200.

**CAUTION**

The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.

**Table 3-20** Package thermal resistance

| Description | Symbol | Value | Unit |
|---|---|---|---|
| Junction-to-ambient thermal resistance | $\theta_{JA}$ | 40 | °C/W |
| Junction-to-case thermal resistance | $\theta_{JC}$ | 12 | °C/W |
| Junction-to-top center of case thermal resistance | $\Psi_{JT}$ | None | °C/W |
| Junction-to-board thermal resistance | $\theta_{JB}$ | 15 | °C/W |

## 3.5.5 Recommended Thermally Conductive Materials

Table 3-21 describes recommended thermally conductive materials.

**Table 3-21** Recommended thermally conductive materials

| Mode of Fixing Heat Sinks | Model | Thermal Conductivity Coefficient (w/m x k) | Ambient Temperature (°C) | Colloid Type | Insulation (V/mil) | Flame Retar dance | Bearing Capacity (g) |
|---|---|---|---|---|---|---|---|
| Mechanical fixing | GF2000 | 2 | –60 to +200 | Silicone rubber | 500 | UL9V 0 | None |
| Non-mechanical fixing | Locotite 315 | 0.808 | None | Acrylic resin | 6000 | UL9V 2 | None |

## 3.5.6 Schematic Diagram Design

### Power Supply

Ensure that the efficiency of the board power tree is the highest as long as the power supply is stable. To this end, design the board power supply optimally and use fewer LDO components with large voltage difference to reduce the heat produced during power conversion.

For example, the 1.2 V power of Hi3130 V200 can be supplied by the power on the board. If there is no 1.2 V power on the board, connect the 3.3 V power to diodes in series and regulate the power to 1.2 V by using an LDO. This reduces power consumption and ensures high efficiency.

### Low-Power Configurations for Idle Modules

The loopback clock CLK_OUT may not be used in Hi3130 V200. In this case, you can set this module to the power-down mode or default mode.

**CAUTION**

Enable clock gating for the master chip to reduce power consumption.

### PCB Design

### Component Layout

Lay out components based on the product architecture and heat dissipation design:

- Evenly place the components that consume a large amount of power and produce much heat to avoid overheating of some parts, which may affect the reliability and efficiency

of components. Place Hi3130 V200 and the decoder chip away from power supplies. Increase the size of copper planes under and around the components, ensuring that the heat produced by the PCB is effectively dissipated.

- Design the product architecture properly to ensure that the heat produced internally can be efficiently dissipated.

### PCB Heat Dissipation

The recommendations are as follows:

- For the connect style of the vias under Hi3130 V200, select the full connect style but not the thermal connect style, In addition, use an opening copper plane at the PCB bottom layer on which the exposed pad of Hi3130 V200 is soldered to improve the dissipation efficiency of the board.
- The 1.2 V power traces, 3.3 V power traces, and GND traces should be as wide as possible when the over-current capability is ensured.
- Never place components that produce much heat around Hi3130 V200.
- Increase the size of copper planes under and around the components that produce much heat to ensure that PCB heat can be effectively dissipated. Place inductors and power chips in a distributed manner and increase the size of copper planes around them.

# Soldering Process Recommendations

## 3.6.1 Overview

The appropriate reflow soldering temperatures must be determined based on the reflow profiles supported by all the components, ICs, and PCB, and the reflow profile recommended by the solder paste vendor. This chapter describes only the reflow soldering temperature range supported by Hi3130 V200.

### Solder Ball Material

Pure stannum is used on the QFN package of Hi3130 V200.

### Component Package and Storage

The following describes the component package and storage:

- Package of surface-mount components: tray or tape&reel
- Allowed storage duration (at most 60% RH): 12 months at 40ºC (104ºF)
- Packaging material: electrostatic discharge (ESD) material

### Soldering Process

Reflow soldering can be used.

Figure 3-17 shows the reflow profiles supported by Hi3130 V200 but not the reflow profiles recommended during soldering. The actual soldering temperatures must be determined based on the reflow profiles of the solder paste, PCB, and all ICs and components. For details, see the JEDEC020D standard.

**Figure 3-17** Soldering temperatures

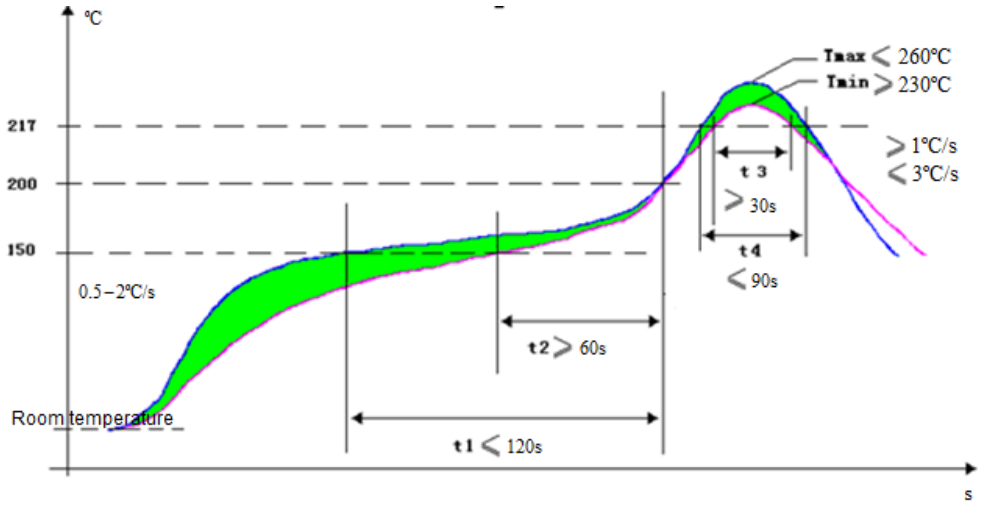



Table 3-22 describes the reflow soldering specifications.

**Table 3-22** Reflow soldering specifications

| Zone | Duration | Heating Up Slope | Peak Temperature | Cooling Down Slope |
|---|---|---|---|---|
| Preheat zone (40–150°C or 104–302°F) | 60−150s | ≤ 2.0ºC/s (≤ 35.6ºF/s) | None | None |
| Soak zone (150–200°C or 302–392°F) | 60−120s | < 1.0ºC/s (< 33.8ºF/s) | None | None |
| Reflow zone (> 217°C or 423°F) | 30−90s | None | 230−260ºC (446−500ºF) | None |
| Cooling zone (Tmax to 180°C or 356°F) | None | None | None | 1.0ºC/s ≤ Slope ≤ 4.0ºC/s (33.8ºF/s ≤ Slope ≤ 39.2ºF/s) |

## 3.6.2 Process Preparations

Confirm that all products are dry and materials have not expired.

Test the first sample such as checking the solder paste thickness before mass production. Start mass production only when the first sample passes all tests.

# 3.7 Moisture-Sensitive Specifications

## 3.7.1 Overview

### Objective

Defines the usage rules for moisture-sensitive integrated circuits (ICs), ensuring that ICs are properly used.

### Application Scope

All HiSilicon products for external customers

### Terminology

- Floor life: time during which a HiSilicon chip can be stored in the workshop at 30°C (86°F) and 60% RH, that is, the time ranging from MBB unpacking to reflow soldering
- Desiccant: a material for absorbing moisture to keep things dry
- Humidity indicator card (HIC): a card that indicates the humidity status
- Moisture sensitivity level (MSL): a level for measuring the moisture degree
- Moisture barrier bag (MBB): a vacuum bag for protecting products against moisture
- Solder reflow: reflow soldering
- Shelf life: storage period

## 3.7.2 HiSilicon Moisture-proof Packaging

### Basic Information

The vacuum packaging materials consist of the following:

- An HIC
- An MBB
- Desiccant

**Figure 3-18** Vacuum packaging materials


### Incoming Inspection

When the vacuum bag is unpacked before SMT in the factories of customers or their partners:

If the largest indicator dot of the HIC is not blue or khaki, rebake the chip by referring to Table 3-24

- If the 10% RH dot of the HIC is blue or khaki, the chip is dry. In this case, replace the desiccant and pack the chip into a vacuum bag.

If the 10% RH dot is not blue or khaki and the 5% RH dot is red or light green, the chip is moist. In this case, rebake the chip by referring to Table 3-24

## 3.7.3 Storage and Usage

### Storage Environment

You are advised to store products at 30°C (86°F) or lower and at most 60% RH.

### Shelf Life

At 30°C (86°F) or lower and at most 60% RH, the shelf life is greater than or equal to 12 months for vacuum packaging.

### Floor Life

Table 3-23 describes the floor life at 30°C (86°F) or lower and at most 60% RH.

**Table 3-23** Floor life

| MSL | Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated |
|---|---|
| 1 | Unlimited at 30°C (86°F) or lower and at most 85% RH |
| 2 | 1 year |
| 2a | 4 weeks |
| 3 | 168 hours |
| 4 | 72 hours |
| 5 | 48 hours |
| 5a | 24 hours |
| 6 | Mandatory bake before use. After bake, the product must be reflowed within the time limit specified on the label. |

### Usage

If a chip has been exposed to air for 2 hours at 30°C (86°F) or lower and at most 60% RH, rebake it and pack it into a vacuum bag.

If a chip has been exposed to air for less than 2 hours at 30°C (86°F) or lower and at most 60% RH, replace the desiccant and pack the chip into a vacuum bag.

For details about other storage modes and usage rules, see the JEDEC J-STD-033A standard.

## 3.7.4 Rebaking

### Application Products

All moisture-sensitive ICs of HiSilicon

### Application Scope

All ICs that need to be rebaked

### Rebaking Reference

**Table 3-24** Rebaking reference

| Body Thickness | Level | Baking at 125°C (257°F) | Baking at 90°C (194°F) ≤ 5% RH | Baking at 40°C (104°F) ≤ 5% RH |
|---|---|---|---|---|
| ≤ 1.4 mm (0.06 in.) | 2a | 3 hours | 11 hours | 5 days |
| | 3 | 7 hours | 23 hours | 9 days |
| | 4 | 7 hours | 23 hours | 9 days |

| Body Thickness | Level | Baking at 125°C (257°F) | Baking at 90°C (194°F) ≤ 5% RH | Baking at 40°C (104°F) ≤ 5% RH |
|---|---|---|---|---|
| | 5 | 7 hours | 24 hours | 10 days |
| | 5a | 10 hours | 24 hours | 10 days |
| ≤ 2.0 mm (0.08 in.) | 2a | 16 hours | 2 days | 22 days |
| | 3 | 17 hours | 2 days | 23 days |
| | 4 | 20 hours | 3 days | 28 days |
| | 5 | 25 hours | 4 days | 35 days |
| | 5a | 40 hours | 6 days | 56 days |
| ≤ 4.5 mm (0.18 in.) | 2a | 48 hours | 7 days | 67 days |
| | 3 | 48 hours | 8 days | 67 days |
| | 4 | 48 hours | 10 days | 67 days |
| | 5 | 48 hours | 10 days | 67 days |
| | 5a | 48 hours | 10 days | 67 days |

**NOTE**

- Table 3-24 lists the minimum rebaking time for moist chips.
- Low-temperature rebaking is recommended.
- For details, see the JEDEC standard.

# 3.8 Interface Timings

## 3.8.1 TS Interface Timing

Figure 3-19 shows the TS interface timing.

**Figure 3-19** TS interface timing

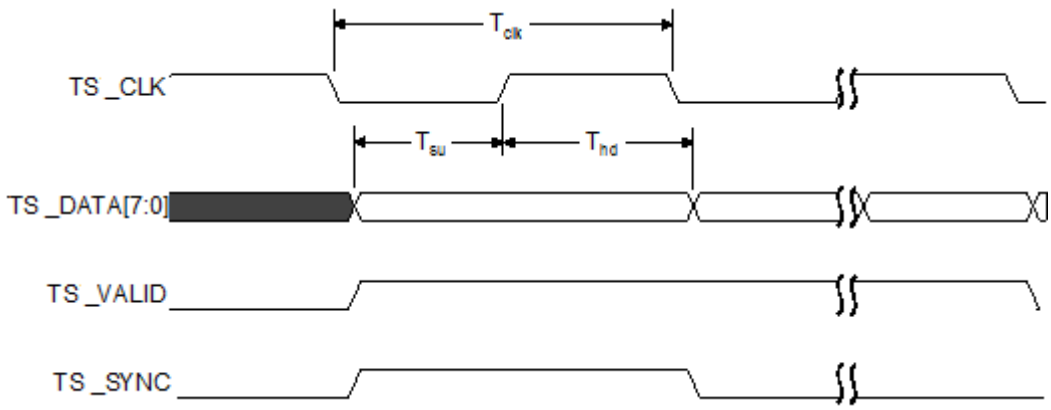


Table 3-25 describes the TS interface timing parameters.

**Table 3-25** TS interface timing parameters

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| TS_CLK clock cycle | $T_{clk}$ | 76.8 | None | None | ns | Parallel |
| | | 11.52 | None | None | ns | Serial |
| Input signal setup time | $T_{su}$ | 67 | None | None | ns | Parallel |
| | | 5.52 | None | None | ns | Serial |
| Input signal hold time | $T_{hd}$ | 2.5 | None | None | ns | Parallel |
| | | 1.1 | None | None | ns | Serial |

## 3.8.2 I²C Interface Timing

Figure 3-20 shows the I²C interface timing.

**Figure 3-20** I²C interface timing

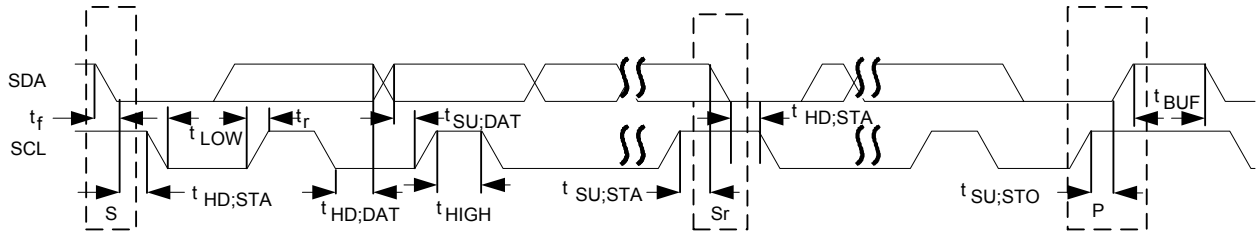



Table 3-26 describes the I²C interface timing parameters.

**Table 3-26** I²C interface timing parameters

| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| SCL frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Start hold time | $t_{HD;STA}$ | 4.0 | None | 0.6 | None | µs |
| SCL low-level cycle | $t_{LOW}$ | 4.7 | None | 1.3 | None | µs |
| SCL high-level cycle | $t_{HIGH}$ | 4.0 | None | 0.6 | None | µs |
| Start setup time | $t_{SU;STA}$ | 4.7 | None | 0.6 | None | µs |
| Data hold time | $t_{HD;DAT}$ | 0 | 3.45 | 0 | 0.9 | µs |

| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Data setup time | $t_{SU;DAT}$ | 250 | None | 100 | None | ns |
| SDA and SCL rising time | $t_r$ | None | 1000 | 20 + $0.1C_b$ | 300 | ns |
| SDA and SCL falling time | $t_f$ | None | 300 | 20 + $0.1C_b$ | 300 | ns |
| End setup time | $t_{SU;STO}$ | 4.0 | None | 0.6 | None | μs |
| Bus release time from start to end | $t_{BUF}$ | 4.7 | None | 1.3 | None | μs |
| Bus load | $C_b$ | None | 400 | None | 400 | pF |
| Low-level noise tolerance | $V_{nL}$ | $0.1V_{DD}$ | None | $0.1V_{DD}$ | None | V |
| High-level noise tolerance | $V_{nH}$ | $0.2V_{DD}$ | None | $0.2V_{DD}$ | None | V |

# Contents

# A Acronyms and Abbreviations

| | |
|---|---|
| **A** | |
| **AAC** | advanced audio coding |
| **AAF** | anti-aliasing filter |
| **ABR** | average bit rate |
| **AC** | alternating current |
| **ACA** | accessory charge adapter |
| **ACC** | automatic contrast control |
| **ACD** | auto command done |
| **ACM** | adaptive coding and modulation |
| **ADP** | attach detection protocol |
| **ADC** | analog-to-digital converter |
| **AE** | automatic exposure |
| **AEC** | audio echo cancellation |
| **AES** | advanced encryption standard |
| **AF** | adaption field |
| **AGC** | automatic gain control |
| **AHB** | advanced high-performance bus |
| **AI** | audio input |
| **AIU** | audio input unit |
| **ALU** | arithmetic logic unit |
| **AMBA** | advanced microcontroller bus architecture |
| **AMP** | asymmetric multi-processing |
| **ANI** | automatic number identification |
| **ANR** | automatic noise reduction |

| | |
|---|---|
| **AO** | audio output |
| **AOU** | audio output unit |
| **AP** | access point |
| **APB** | advanced peripheral bus |
| **API** | application programming interface |
| **APLL** | analog phase-locked loop |
| **APSK** | amplitude phase shift keying |
| **AQTD** | alternate queue transfer descriptor |
| **ARM** | advanced RISC machines |
| **ARGB** | alpha, red, green, blue |
| **ASF** | advanced specification format |
| **ATA** | advanced technology attachment |
| **ATAH** | ATA host controller |
| **ATAPI** | advanced technology attachment packet interface |
| **ATR** | answer to reset |
| **ATTR** | attribute |
| **AUD** | audio |
| **AV** | audio & video |
| **AVI** | auxiliary video information |
| **AVS** | audio video coding standard |
| **AWB** | automatic white balance |
| **AXI** | advanced eXtensible interface |

**B**

| | |
|---|---|
| **BB** | baseband |
| **BCH** | Bose-Chaudhuri-Hocquenghem |
| **BCM** | byte counter modified |
| **BEP** | boot entrance point |
| **BER** | bit error rate |
| **BGA** | ball grid array |
| **BIST** | built-in self test |
| **BIU** | bus interface unit |
| **BMC** | bi-phase mark coding |

| | |
|---|---|
| **BND** | bayonet nut connector |
| **BOM** | bill of material |
| **BPD** | bit plan decoder |
| **BPSK** | binary phase shift keying |
| **BRG** | bridge |
| **BSP** | board support package |
| **BVACT** | bottom vertical active area |
| **BVBB** | bottom vertical back blank |
| **BVFB** | bottom vertical front blank |

**C**

| | |
|---|---|
| **CA** | conditional access |
| **CABAC** | context-based adaptive binary arithmetic coding |
| **CAR** | committed access rate |
| **CAS** | column address signal. |
| **CAVLC** | context adaptive variable length coding |
| **CBC** | cipher block chaining |
| **CBR** | constant bit rate |
| **CCB** | change control board |
| **CCC** | command completion coalescing |
| **CCD** | charge-coupled device |
| **CCM** | constant coding and modulation |
| **CD** | command done or collision detection |
| **CDR** | clock data recovery |
| **CEC** | consumer electronics control |
| **CF** | compact flash |
| **CFB** | cipher feedback |
| **CFR** | crest factor reduction |
| **CGI** | common gate interface |
| **CGMS** | copy generation management system |
| **CI** | common interface |
| **CIC** | cascaded integrator comb |
| **CIU** | card interface unit |

| | |
|---|---|
| **CL** | CAS latency |
| **CLK** | clock |
| **CML** | current mode logic |
| **CMOS** | complementary metal-oxide semiconductor |
| **CN** | carrier noise |
| **CNG** | comfort noise generator |
| **CODEC** | coder/decoder |
| **CP** | charge pump |
| **CPL** | completion |
| **CPLD** | complex programmable logic device |
| **CPU** | central processing unit |
| **CR** | carrier recovery |
| **CRAMFS** | compressed ROM file system |
| **CRC** | cyclic redundancy check |
| **CRG** | clock and reset generator |
| **CRS** | completion retry request |
| **CS** | chip select |
| **CSA** | common scramble algorithm |
| **CSI** | camera serial interface |
| **CSIX** | common switch interface |
| **CSMD** | carrier sense multiple access |
| **CTI** | chroma transient improvement |
| **CTR** | counter |
| **CTS** | clear to send |
| **CVBS** | composite video broadcast signal |
| **CW** | cipher word |

**D**

| | |
|---|---|
| **DAC** | digital-to-analog converter |
| **DAG** | digital automatic gain |
| **DAGC** | digital automatic gain control |
| **DAV** | DMA of audio and video |
| **DC** | direct current |

| | |
|---|---|
| **DCD** | data connect detection |
| **DCRC** | data CRC error |
| **DDC** | display data channel |
| **DDR** | double data-rate |
| **DDRC** | double data rate controller |
| **DHCP** | dynamic host configuration protocol |
| **DEM** | dynamic-element matching |
| **DES** | data encryption standard |
| **DFT** | design for test |
| **DIP** | dual in-line package |
| **DIS** | digital image stabilization |
| **DiSEqC** | digital satellite equipment control |
| **DLL** | delay locked loop |
| **DM** | data mask |
| **DMA** | direct memory access |
| **DMAC** | direct memory access controller |
| **DNR** | digital noise reduction |
| **DP** | data path |
| **DPLL** | digital phase-locked loop |
| **DQ** | data input/output |
| **DQS** | data strobe |
| **DR** | design requirement |
| **DRAM** | dynamic random access memory |
| **DRC** | dynamic range compression |
| **DRM** | digital rights management |
| **DRTO** | data read timeout |
| **DSI** | display serial interface |
| **DSU** | dedicated scaling unit |
| **DTMF** | dual tone multi frequency |
| **DTO** | data transfer over |
| **DVB** | digital video broadcasting |
| **DVB-S** | digital video broadcasting-satellite |
| **DVD** | digital versatile disc |

| | |
|---|---|
| **DVI** | digital visual interface |
| **DVR** | digital video recorder |
| **DWA** | data weighted averaging |

**E**

| | |
|---|---|
| **E2PROM** | electrically erasable programmable read-only memory |
| **EAV** | end of active video |
| **EB** | eviction buffer |
| **EBE** | end-bit error |
| **EBI** | external bus interface |
| **ECB** | electronic codebook |
| **ECC** | error correcting code |
| **ECM** | entitlement control message |
| **ECS** | embedded CPU subsystem |
| **ED** | exposed die |
| **EDID** | extended display identification data |
| **EEE** | energy efficient Ethernet |
| **EHCI** | enhanced host controller interface |
| **EMI** | electromagnetic interference |
| **EMM** | entitlement management message |
| **eMMC** | embedded multimedia card |
| **EOP** | end of PES |
| **EoS** | Ethernet over SONET/SDH |
| **EP** | end point |
| **EPG** | electronic program guide |
| **EQU** | equalizer |
| **ERR** | error |
| **ES** | element stream |
| **eSATA** | external serial advanced technology attachment |
| **ESD** | electrostatic discharge |
| **ESR** | equivalent series resistance |
| **ETH** | Ethernet |
| **ETU** | elementary time unit |

**F**

| | |
|---|---|
| **FAS** | frame aligning signal |
| **FBE** | feedback equalizer |
| **FC** | switch fabric |
| **FCBGA** | flip-chip ball grid array |
| **FCCSP** | flip-chip chip scale package |
| **FEC** | forward error correction |
| **FER** | frame error rate |
| **FFC** | flexible flat cable |
| **FFE** | feed forward equalizer |
| **FIFO** | first in first out |
| **FIQ** | fast interrupt request |
| **FIR** | finite impulse response |
| **FIS** | frame information structure |
| **FOD** | field order detect |
| **FPC** | flexible printed connector |
| **FPU** | floating-point unit |
| **FRUN** | FIFO underrun/overrun error |
| **FSK** | frequency shift keying |
| **FTP** | File Transfer Protocol |

**G**

| | |
|---|---|
| **GFP-F** | frame-mapped generic framing procedure |
| **GFP-T** | transparent generic framing procedure |
| **GHB** | global history buffer |
| **GIC** | generic interrupt controller |
| **GOP** | group of picture |
| **GS** | generic stream |
| **GMAC** | gigabit media access control |
| **GND** | ground |
| **GPIO** | general purpose input/output |
| **GPL** | GNU general public license |

| | |
|---|---|
| **GPU** | graphics processing unit |
| **H** | |
| **HBA** | host bus adapter |
| **HBP** | horizontal back porch |
| **HD** | high definition |
| **HDCP** | high-bandwidth digital content protection |
| **HDI** | high density interconnector |
| **HDMI** | high definition multimedia interface |
| **HFP** | horizontal front porch |
| **HIAO** | high-performance audio output interface |
| **HPW** | horizontal pulse width |
| **HSTL** | high speed transceiver logic |
| **HTML** | hypertext markup language |
| **HACT** | horizontal active area |
| **HFB** | horizontal front blank |
| **HL** | high level |
| **HLDC** | horizontal lens distortion correction |
| **HLE** | hardware locked error |
| **HNP** | host negotiation protocol |
| **HTO** | data starvation-by-host timeout |
| **HP** | high profile |
| **HSIC** | high-speed inter-chip |
| **HSS** | high-speed serializer/deserializer |
| **HTTP** | Hypertext Transfer Protocol |
| **HTTPS** | Hypertext Transfer Protocol Secure |
| **HVBB** | horizontal back blank |
| **I** | |
| **I** | in-phase |
| **IBIS** | input/output buffer information specification |
| **IC** | integrated circuit |
| **$I^2C$** | inter-integrated circuit |

| | |
|---|---|
| **$I^2S$** | inter-IC sound |
| **I/O** | input/output |
| **IOC** | I/O configuration |
| **IP** | Internet Protocol |
| **ISI** | input stream identifier |
| **ISP** | image signal processor |
| **IDE** | integrated device electronic |
| **LDPC** | low density parity check code |
| **IDR** | intermediate data rate |
| **IF** | intermediate frequency |
| **IGMP** | Internet Group Management Protocol |
| **LMS** | linear mean square |
| **IPF** | IP filter |
| **IPv4** | Internet Protocol Version 4 |
| **IR** | infrared |
| **IRQ** | interrupt request |
| **ISI** | input stream identifier |
| **ISP** | image signal processor |
| **ISR** | interrupt service routine |
| **ITCM** | instruction tightly coupled memory |
| **ITLA** | integrated tunable laser assembly |
| **ITU** | International Telecommunication Union |
| **IV** | initialization vector |

**J**

| | |
|---|---|
| **JFFS2** | journaling flash file system version 2 |
| **JPEG** | Joint Photographic Experts Group |
| **JPGE** | JPEG encoder |
| **JTAG** | Joint Test Action Group |

**K**

| | |
|---|---|
| **KL** | key ladder |

**L**

| | |
|---|---|
| **LCD** | liquid crystal display |
| **LDO** | low dropout regulator |
| **LDPC** | low-density parity check code |
| **LED** | light emitting diode |
| **LFB** | line fill buffer |
| **LFSR** | linear feedback shifting register |
| **LMR** | load mode register |
| **LMS** | least mean square |
| **LNB** | low noise block |
| **LOS** | loss of signal |
| **LPI** | low-power idle |
| **LRB** | line read buffer |
| **LSB** | least significant bit |
| **LSP** | label switched path |
| **LSN** | logic sector number |
| **LTI** | luma transient improvement |
| **LVDS** | low-voltage differential signaling |
| **LVPECL** | low-voltage positive emitter coupled logic |
| **LVTTL** | low-voltage transistor-transistor logic |
| **LVPECL** | low-voltage positive emitter-coupled logic |

**M**

| | |
|---|---|
| **MAC** | media access control |
| **MBAFF** | macroblock adaptive frame field |
| **MCE** | media control engine |
| **MCU** | microprogrammed control unit |
| **MD** | motion detection |
| **MDDRC** | multiport DDRC |
| **MDIO** | management data input/output |
| **MDU** | motion detect unit |
| **MF** | matched filter |
| **MQFN** | mapped quad flat non-leaded |

| | |
|---|---|
| **MHL** | mobile high-definition link |
| **MII** | media independent interface |
| **MIPI** | mobile industry processor interface |
| **MIPS** | microprocessor without interlocked pipeline stages |
| **MLC** | multi-level cell |
| **MLF** | malformed |
| **MMB** | media memory block |
| **MMC** | multimedia card |
| **MMU** | memory management unit |
| **MMZ** | media memory zone |
| **MP** | main profile |
| **MPI** | MPP programming interface |
| **MPE** | media processing engine |
| **MPLL** | multiplying phase-locked loop |
| **MPP** | media processing platform |
| **MRL** | manually-operated retention latch |
| **MSB** | most significant bit |
| **MSE** | mean square error |
| **MSG** | message |
| **MV** | motion vector |

**N**

| | |
|---|---|
| **NAL** | network abstraction layer |
| **NANDC** | NAND flash controller |
| **NC** | not connect |
| **NCQ** | native command queuing |
| **NLP** | non-linear processor |
| **NR** | noise reduction |
| **NRZ** | non-return-to-zero |
| **NTSC** | National Television Systems Committee |
| **NVR** | network video recorder |

**O**

| | |
|---|---|
| **OCT** | on-chip termination |
| **OD** | open drain |
| **ODT** | on-die termination |
| **OEN** | output enable |
| **OFB** | output feedback |
| **OHCI** | open host controller interface |
| **OOB** | out of band |
| **OP** | operational amplifier |
| **OR** | original requirement |
| **OSC** | oscillator |
| **OSD** | on screen display |
| **OTG** | on-the-go |
| **OTP** | one time programmable |
| **OTU** | optical transponder unit |

**P**

| | |
|---|---|
| **PAD** | packet assembler/disassembler |
| **PAFF** | picture adaptive frame field |
| **PAL** | phase alternating line |
| **PCB** | printed circuit board |
| **PCI** | peripheral component interconnect |
| **PCIe** | peripheral component interconnect express |
| **PCIV** | PCI view |
| **PCR** | program clock reference |
| **PCM** | pulse code modulation |
| **PDM** | pulse density modulation |
| **PECL** | positive emitter coupled logic |
| **PER** | packet error rate |
| **PES** | packetized elementary stream |
| **PG** | power/ground |
| **PHY** | physical |
| **PID** | packet ID |
| **PIM-DM** | protocol independent multicast dense mode |

| | |
|---|---|
| **PIM-SM** | protocol independent multicast sparse mode |
| **PIO** | programmable input/output |
| **SSA** | secure software authentication |
| **PLL** | phase-locked loop |
| **PLS** | physical layer signaling |
| **PM** | port multiplexer |
| **PMoC** | power management of chip |
| **PMP** | personal media player |
| **POR** | power-on reset |
| **PPP** | Point-to-Point Protocol |
| **PPS** | picture parameter set |
| **PRBS** | pseudo random binary sequence |
| **PRDT** | physical region descriptor table |
| **PSI** | program specific information |
| **PSK** | phase shift keying |
| **PSRAM** | pseudo static random access memory |
| **RTCP** | Real-time Transport Control Protocol |
| **RTP** | Real-time Transport Protocol |
| **PT** | packet type |
| **PTS** | presentation time stamp |
| **PUB** | PHY utility block |
| **PUSI** | payload unit start indicator |
| **PWM** | pulse width modulation |

**Q**

| | |
|---|---|
| **Q** | quadrant |
| **QAM** | quadrature amplitude modulation |
| **QDR** | quad data rate |
| **QoS** | quality of service |
| **QP** | quantizer parameter |
| **QPSK** | quaternary phase shift keying |

**R**

| | |
|---|---|
| **RAM** | random access memory |
| **RAS** | row address signal |
| **RC** | resistor-capacitor |
| **RCA** | Radio Corporation of America |
| **RCRC** | response CRC error |
| **RE** | response error |
| **RF** | radio frequency |
| **RGB** | red-green-blue |
| **RGMII** | reduced gigabit media independent interface |
| **RH** | relative humidity |
| **RoHS** | restriction of the use of certain hazardous substances |
| **ROI** | region of interest |
| **ROM** | read-only memory |
| **ROP** | raster operation |
| **RPR** | resilient packet ring |
| **RLDRAM** | reduced latency dynamic random access memory |
| **RMII** | reduced media-independent interface |
| **RS** | Reed-Solomon |
| **RTC** | real-time clock |
| **RTO** | response timeout |
| **RTS** | request to send |
| **RVDS** | RealView development suite |
| **RX** | receive |
| **RXDR** | receive FIFO data request |

**S**

| | |
|---|---|
| **SAP** | service access point |
| **SAD** | sum of absolute difference |
| **SAR** | successive approximation |
| **SATA** | serial advanced technology attachment |
| **SAV** | start of active video |
| **SBE** | start-bit error |
| **SBP** | secure boot procedure |

| | |
|---|---|
| **SCD** | start code detect |
| **SCI** | smart card interface |
| **SCL** | serial clock |
| **SCR** | system clock reference |
| **SCS** | secure chipset start-up |
| **SCU** | snoop control unit |
| **SD** | secure digital |
| **SDA** | serial data |
| **SDB** | set device bits |
| **SDH** | synchronous digital hierarchy |
| **SDHC** | secure digital high capacity |
| **SDI** | serial digital interface |
| **SDIO** | secure digital input/output |
| **SDK** | software development kit |
| **SDRAM** | synchronous dynamic random access memory |
| **SDV** | system design verification |
| **SI** | specific information |
| **SIO** | sonic input/output |
| **SLC** | single-level cell |
| **SMI** | static memory interface |
| **SNAP** | subnetwork access point |
| **SNR** | signal-to-noise ratio |
| **SNTF** | serial ATA notification |
| **SOA** | semiconductor optical amplifier |
| **SoC** | system-on-chip |
| **SONET** | synchronous optical network |
| **SOP** | start of PES |
| **SP** | simple profile |
| **SPDIF** | Sony/Philips digital interface |
| **SPI** | serial peripheral interface |
| **SPS** | sequence parameter set |
| **SRAM** | static random access memory |
| **SRP** | Session Request Protocol |

| | |
|---|---|
| **SSA** | secure software authentication |
| **SSD** | secure software download |
| **SSMC** | synchronous static memory controller |
| **SSP** | synchronous serial port |
| **SSRAM** | synchronous static random access memory |
| **SSTL-18** | stub series terminated logic for 1.8 V |
| **STA** | station |
| **STB** | set-top box |
| **STM-1** | synchronous transport module level 1 |
| **SVB** | selective voltage bing |
| **SYNC** | synchronization |
| **SYS** | system |

**T**

| | |
|---|---|
| **TBD** | to be determined |
| **TBGA** | tape ball grid array |
| **TC** | traffic class |
| **TCP** | Transmission Control Protocol |
| **TD** | TLP digest |
| **TDES** | triple data encryption standard |
| **TDE** | two-dimensional engine |
| **TE** | tearing effect |
| **TEI** | transport error indicator |
| **TFD** | task file data |
| **TFPBGA** | tape fine-pitch ball grid array |
| **TFT** | thin-film technology |
| **TI** | Texas Instruments |
| **TLV** | type-length-value |
| **TOE** | TCP/IP offload engine |
| **TP** | transponder |
| **TPIT** | TS packet index table |
| **TR** | timing recovery |
| **TS** | transport stream |

| | |
|---|---|
| **TSI** | transport stream interface |
| **TT** | teletext |
| **TV** | television |
| **TVACT** | top vertical active area |
| **TVBB** | top vertical back blank |
| **TVFB** | top vertical front blank |
| **TVS** | transient voltage suppressor |
| **TX** | transmit |
| **TXDR** | transmit FIFO data request |

**U**

| | |
|---|---|
| **UART** | universal asynchronous receiver transmitter |
| **U-boot** | universal boot loader |
| **UC** | unexpected completion |
| **UDP** | User Datagram Protocol |
| **ULPI** | UTMI low pin interface |
| **UPnP** | universal plug and play |
| **UR** | unsupported request |
| **USB** | universal serial bus |
| **USIM** | universal subscriber identity module |
| **UTMI** | USB 2.0 transceiver macrocell interface |

**V**

| | |
|---|---|
| **VACT** | vertical active area |
| **VAD** | voice activity detector |
| **VAPU** | video analysis&process unit |
| **VBB** | vertical back blank |
| **VBI** | vertical blanking interval |
| **VBR** | variable bit rate |
| **VCC** | common connector voltage |
| **VCO** | voltage controller oscillator |
| **VCM** | variable coding and modulation |
| **VCMP** | video compress |

| | |
|---|---|
| **VCXO** | voltage control crystal oscillator |
| **VDA** | video detection analysis |
| **VDH** | video decoder for high-definition |
| **VDM** | video decoding module |
| **VDEC** | video decoding |
| **VDP** | video display |
| **VEDU** | video encoding/decoding unit |
| **VENC** | video encoding |
| **VFB** | vertical front blank |
| **VFMW** | video firmware |
| **VFP** | vertical front porch |
| **VGA** | video graphics array |
| **VI** | video input |
| **VIC** | vector interrupt controller |
| **VICAP** | video capture |
| **VIU** | video input unit |
| **VLD** | valid |
| **VLL** | virtual leased line |
| **VO** | video output |
| **VOIE** | voice encoder |
| **VOU** | video output unit |
| **VPP** | video pre-processing |
| **VPS** | video programming system |
| **VPSS** | video process subsystem |
| **VPW** | vertical pulse width |
| **VSA** | vertical sync start |
| **VQE** | voice quality enhancement |
| **VQM** | voice quality monitor |

**W**

| | |
|---|---|
| **WDG** | watchdog |
| **WE** | write enable |
| **WFE** | wait for event |

| | |
|---|---|
| **WFI** | wait for interrupt |
| **WRED** | weighted random early discard |
| **WSS** | wide screen signaling |

**X**

| | |
|---|---|
| **XAUI** | 10 gigabit attachment unit interface |

**Y**

| | |
|---|---|
| **YAFFS** | yet another flash file system |
| **YUV** | luminance-bandwidth-chrominance |

**Z**

| | |
|---|---|
| **ZME** | zoom engine |