Hi3798M V100 Hardware Design

User Guide

Issue 05

Date 2015-11-02

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About This Document

Purpose

This document describes the implementation, methods, and instances for board impedance control during hardware design as well as the DC-DC peripheral impedance selection for the CPU and core power.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3798M	V1XX

Intended Audience

This document is intended for:

- Technical support engineers
- Hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 05 (2015-11-02)

This issue is the fifth official release, which incorporates the following change:

Chapter 6 FAQs

Section 6.8 is added.

Issue 04 (2015-07-29)

This issue is the fourth official release, which incorporates the following change:

Chapter 6 FAQs

Section 6.7 is added.

Issue 03 (2015-06-09)

This issue is the third official release, which incorporates the following change:

Chapter 6 FAQs

Section 6.6 is added.

Issue 02 (2015-04-30)

This issue is the second official release, which incorporates the following change:

Chapter 6 FAQs

Sections 6.4 and 6.5 are added.

Issue 01 (2014-11-20)

This issue is the first official release, which incorporates the following changes:

Chapters 3 and 6 are added, and chapter 1 is modified.

Issue 00B02 (2014-08-30)

This issue is the second draft release, which incorporates the following change:

Chapters 3, 4, and 5 are added.

Issue 00B01 (2014-08-19)

This issue is the first draft release.

Contents

Figures

Tables

1 Board Impedance Control

Impedance control for signals on the board significantly affects the interface specifications and performance, especially that for DDR signals. This directly affects system stability. You are advised to control the impedance for important signals (DDR signals and some signals of the master chip) of the 2-layer or 4-layer PCB by strictly following the HiSilicon demo board.

Figure 1-1 Reference design for DDR signals and some signals of the master chip for the HiSilicon 2-layer PCB

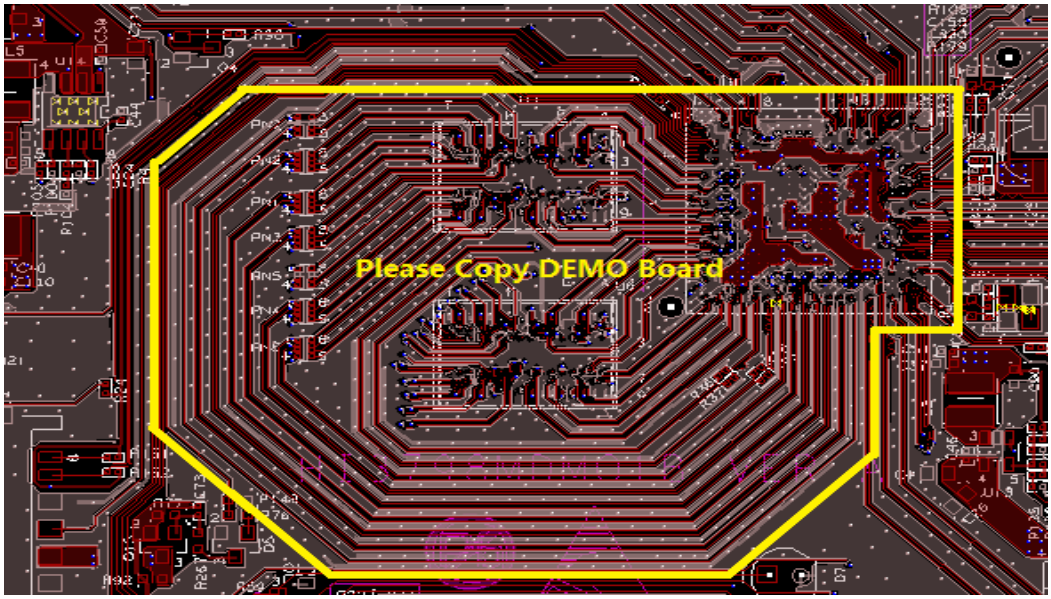
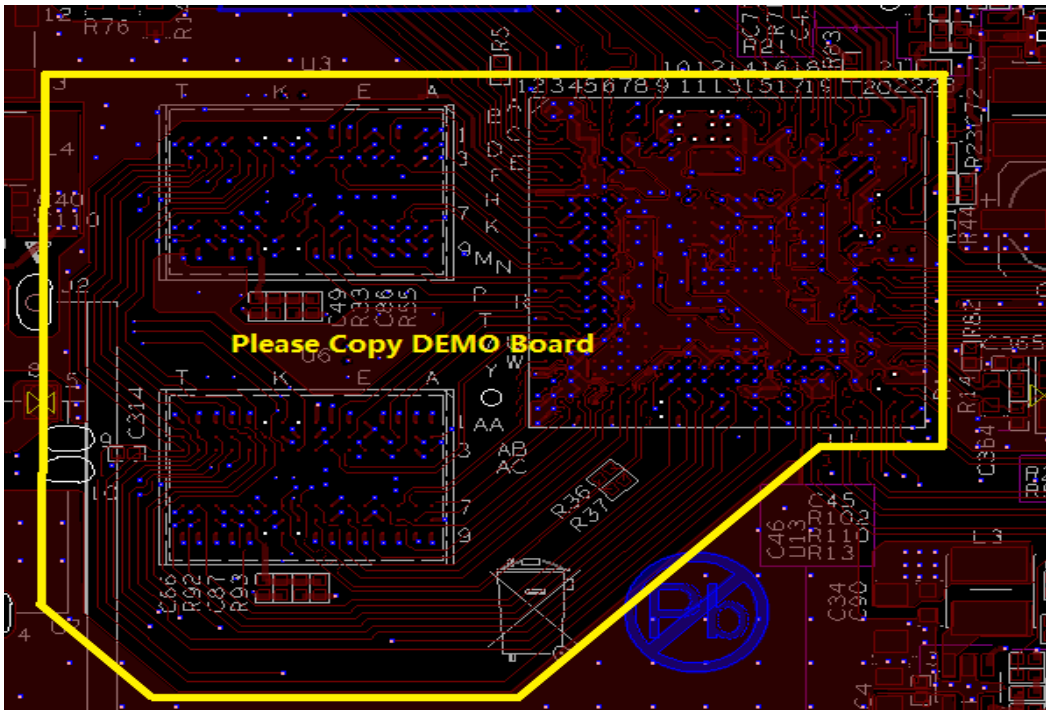


Figure 1-2 Reference design for DDR signals and some signals of the master chip for the HiSilicon 4-layer PCB



1.1 Impedance Control Method

During board design, you can adjust the trace width and distance between traces to control the impedance.

1.1.1 Impedance Calculator

To calculate the impedance by using an impedance calculator, perform the following steps (the calculation method may vary slightly according to the impedance calculator):

Step 1 Select single-ended impedance control or differential impedance control.

Step 2 Select the impedance control model based on the 2-layer or 4-layer PCB.

Step 3 Specify the parameters such as the board material and signal routing.

Step 4 Calculate the impedance.

Step 5 Check whether the calculation result is consistent with the target impedance. If yes, route the traces according to the parameters (trace width and distance between traces); if not, go to step 3.

----End

The following parameters are the primary factors that affect the impedance: H1, Er1, W1, W2, S1, G1, G2, D1, T1, C1, C2, C3, and CEr.

For details about the calculator model and parameters for the single-ended impedance, see Figure 1-3.

Figure 1-3 Calculation model for the single-ended impedance of the 2-layer PCB

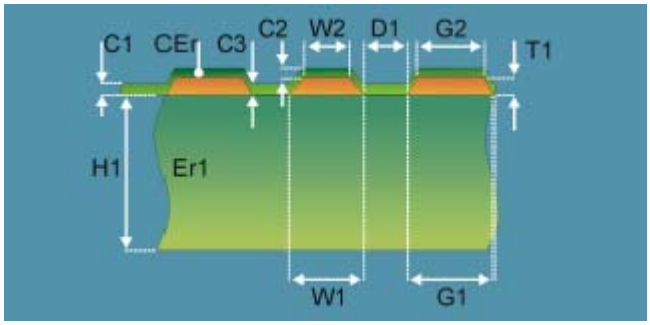


Figure 1-4 Calculation model for the single-ended impedance of the 4-layer PCB

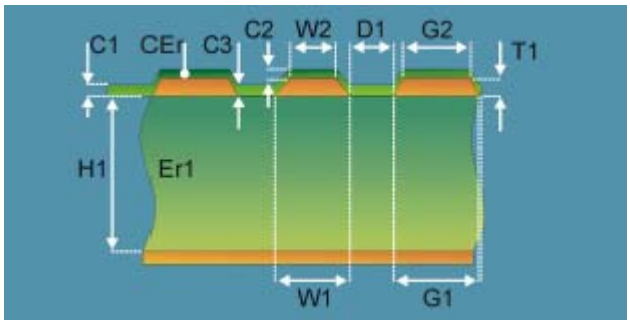


Table 1-1 Single-ended impedance control parameters

Parameter	Definition	Value Description
H1	Substrate 1 Height	Board thickness for the 2-layer PCB, or the spacing between the layer and the reference plane for the 4-layer PCB
Er1	Substrate 1 Dielectric	Related to the board material type. The FR-4 value 4.2 is recommended.
W1	Lower Trace Width	Variable, depending on the impedance
W2	Upper Trace Width	W1 minus 1 mil
G1	Lower Ground Strip Width	Variable, 20 mils at least
G2	Upper Ground Strip Width	G1 minus 1 mil
D1	Ground Strip Separation	5 mils (recommended) for the 2-layer PCB, or greater than 1.5 times trace width for the 4-layer PCB
T1	Trace Thickness	1.5 mils (recommended)
C1	Coating Above Substrate	1 mil by default. It hardly affects the impedance.

C2	Coating Above Trace	1 mil by default. It hardly affects the impedance.
C3	Coating Between Traces	1 mil by default. It hardly affects the impedance.
CEr	Coating Dielectric	4.2 (recommended)

For details about the calculator model and parameters for the differential impedance, see Figure 1-5, Figure 1-6, and Table 1-2.

Figure 1-5 Calculation model for the differential impedance of the 2-layer PCB

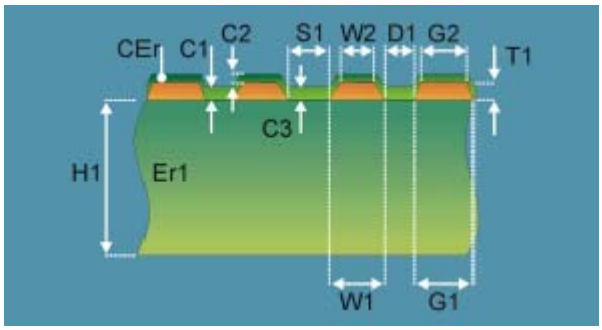


Figure 1-6 Calculation model for the differential impedance of the 4-layer PCB

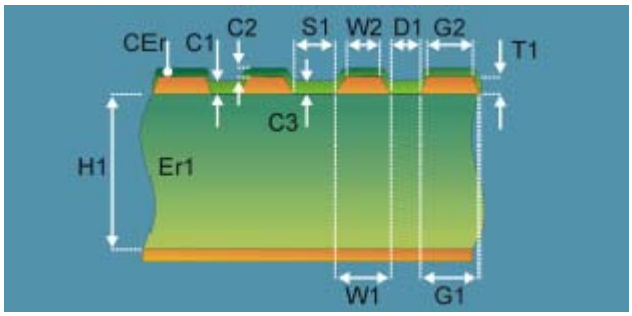


Table 1-2 Differential impedance control parameters

Parameter	Definition	Value Description
H1	Substrate 1 Height	Board thickness for the 2-layer PCB, or the spacing between the layer and the reference plane for the 4-layer PCB
Er1	Substrate 1 Dielectric	Related to the board material type. The FR-4 value 4.2 is recommended.
W1	Lower Trace Width	Variable, depending on the impedance
S1	Trace Separation	Variable, depending on the impedance
W2	Upper Trace Width	W1 minus 1 mil

G1	Lower Ground Strip Width	Variable, 20 mils at least
G2	Upper Ground Strip Width	G1 minus 1 mil
D1	Ground Strip Separation	5 mils for the 2-layer PCB, or greater than 1.5 times trace width for the 4-layer PCB
T1	Trace Thickness	1.5 mils (recommended)
C1	Coating Above Substrate	1 mil by default. It hardly affects the impedance.
C2	Coating Above Trace	1 mil by default. It hardly affects the impedance.
C3	Coating Between Traces	1 mil by default. It hardly affects the impedance.
CEr	Coating Dielectric	4.2 (recommended)

1.1.2 Impedance Control for Hi3798M V100

For the Hi3798M V100 board, you need to control the 100 Ω, 90 Ω, and 50 Ω impedance, as described in Table 1-3.

Table 1-3 Impedance control requirements

Signal Traces	4-Layer PCB	2-Layer PCB	Deviation
Four pairs of HDMI differential traces	100 Ω	100 Ω	±10%
Four pairs of DQS differential traces for the DDR	100 Ω	100 Ω	±10%
Two pairs of CLK differential traces for the DDR	100 Ω	100 Ω	±10%
Two pairs of differential traces for the Ethernet port	100 Ω	100 Ω	±10%
USB differential traces	90 Ω	90 Ω	±10%
DDR single-ended traces	50 Ω	Control the trace width and spacing in priority. The impedance is typically 60 Ω to 70 Ω.	±10%

1.2 Impedance Control Instances

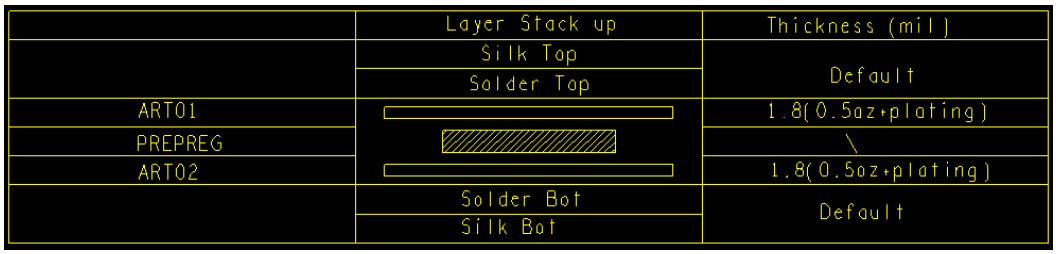
1.2.1 Impedance Control for the 2-Layer PCB

Stack Information

The board thickness is 1.6 mm (about 63 mils).

The thickness of the copper plane at the top and bottom layers is 1.8 mils.

Figure 1-7 Stack information of the 2-layer PCB



100 Ω Impedance Control

The 100 Ω impedance needs to be controlled for the following traces:

- Four pairs of HDMI differential traces
- DDR_DQS differential traces
- DDR_CLK differential traces
- Two pairs of differential traces for the Ethernet port

Calculate the target impedance by using an impedance calculator. See Figure 1-8 and Table 1-4.

Figure 1-8 Calculating the 100 Ω differential impedance for the 2-layer PCB

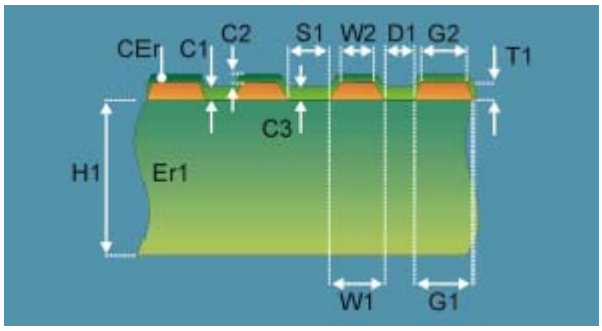


Table 1-4 100 Ω differential impedance control parameters

Parameter	Description	Value (mil)
H1	Substrate 1 Height	63
Er1	Substrate 1 Dielectric	4.2
W1	Lower Trace Width	5.5
W2	Upper Trace Width	4.5
S1	Trace Separation	6
G1	Lower Ground Strip Width	20

G2	Upper Ground Strip Width	19
D1	Ground Strip Separation	5
T1	Trace Thickness	1.8
C1	Coating Above Substrate	1
C2	Coating Above Trace	1
C3	Coating Between Traces	1
CEr	Coating Dielectric	4.2

The calculated impedance is 104.78 Ω based on the preceding parameters.

Therefore, when the board thickness is 1.6 mm and the substrate dielectric is 4.2, **W1** must be 5.5 mils, **S1** must be 6 mils, **D1** must be 5 mils, and **T1** must be 1.8 mils.

90 Ω Impedance Control

The 90 Ω impedance needs to be controlled for the USB 2.0 and USB 3.0 differential traces.

Calculate the target impedance by using an impedance calculator. See Figure 1-9 and Table 1-5.

Figure 1-9 Calculating the 90 Ω differential impedance for the 2-layer PCB

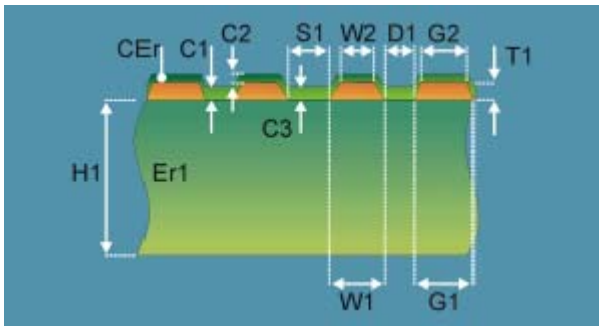


Table 1-5 90 Ω differential impedance control parameters

Parameter	Description	Value (mil)
H1	Substrate 1 Height	63
Er1	Substrate 1 Dielectric	4.2
W1	Lower Trace Width	6
W2	Upper Trace Width	5
S1	Trace Separation	5
G1	Lower Ground Strip Width	20

G2	Upper Ground Strip Width	19
D1	Ground Strip Separation	5
T1	Trace Thickness	1.8
C1	Coating Above Substrate	1
C2	Coating Above Trace	1
C3	Coating Between Traces	1
CEr	Coating Dielectric	4.2

The calculated impedance is 96.85 Ω based on the preceding parameters.

Therefore, when the board thickness is 1.6 mm and the substrate dielectric is 4.2, **W1** must be 6 mils, **S1** must be 5 mils, **D1** must be 5 mils, and **T1** must be 1.8 mils.

DDR Single-Ended Impedance Control

For the DDR single-ended trace of the 2-layer PCB, the following factors must be considered first during routing: signal width, spacing between signal traces, and spacing between signal traces and GND traces. You are advised to design the trace width, spacing, GND, and GND vias by strictly following the HiSilicon demo board.

As shown on the demo board, when the board thickness is 1.6 mm and the substrate dielectric is 4.2, **W1** must be 5 mils, **S1** must be 10 mils, **D1** must be 5 mils, and **T1** must be 1.8 mils.

1.2.2 Impedance Control for the 4-Layer PCB

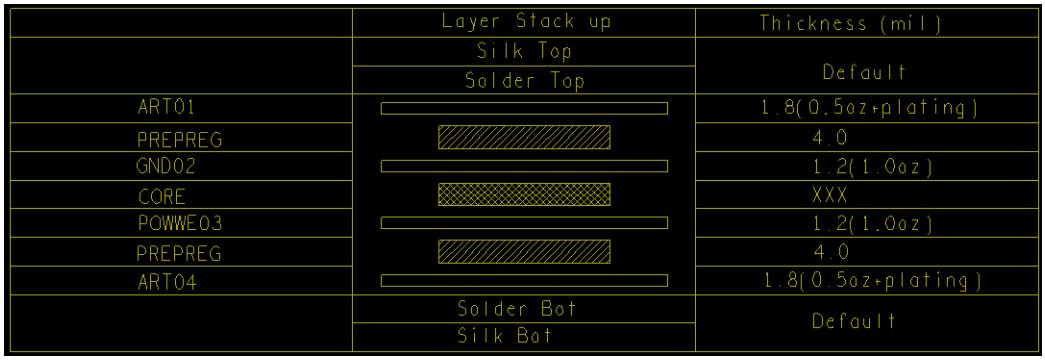
Stack Information

The board thickness is 1.6 mm (about 63 mils).

The thickness of the copper plane at the top and bottom layers is 1.8 mils.

The spacing between the top/bottom layer and its reference layer is 4 mils.

Figure 1-10 Stack information of the 4-layer PCB



100 Ω Impedance Control

The 100 Ω impedance needs to be controlled for the following traces:

- Four pairs of HDMI differential traces
- DDR_DQS differential traces
- DDR_CLK differential traces
- Two pairs of differential traces for the Ethernet port

Calculate the target impedance by using an impedance calculator. See Figure 1-11 and Table 1-6.

Figure 1-11 Calculating the 100 Ω differential impedance for the 4-layer PCB

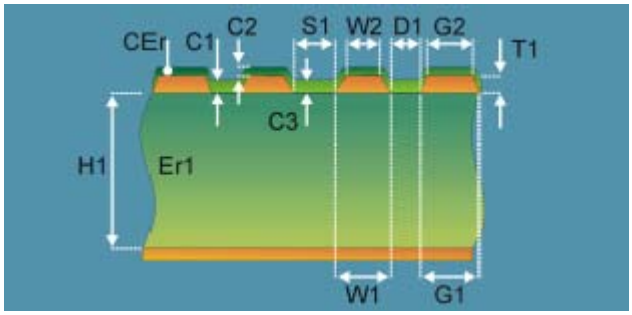


Table 1-6 100 Ω differential impedance control parameters

Parameter	Description	Value (mil)
H1	Substrate 1 Height	4
Er1	Substrate 1 Dielectric	4.2
W1	Lower Trace Width	4.5
W2	Upper Trace Width	3.5
S1	Trace Separation	6
G1	Lower Ground Strip Width	20
G2	Upper Ground Strip Width	19
D1	Ground Strip Separation	6.75
T1	Trace Thickness	1.8
C1	Coating Above Substrate	1
C2	Coating Above Trace	1
C3	Coating Between Traces	1
CEr	Coating Dielectric	4.2

The calculated impedance is 95.32 Ω based on the preceding parameters.

Therefore, when the board thickness is 1.6 mm and the substrate dielectric is 4.2, **W1** must be 4.5 mils, **S1** must be 6 mils, **D1** must be greater than 6.75 mils (GND traces are not necessarily required), and **T1** must be 1.8 mils.

90 Ω Impedance Control

The 90 Ω impedance needs to be controlled for the USB 2.0 and USB 3.0 differential traces.

Calculate the target impedance by using an impedance calculator. See Figure 1-12 and Table 1-7.

Figure 1-12 Calculating the 90 Ω differential impedance for the 4-layer PCB

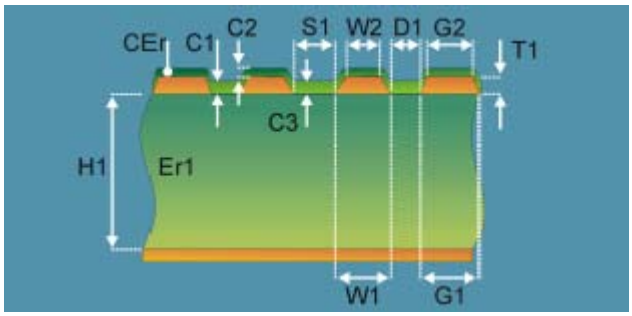


Table 1-7 90 Ω differential impedance control parameters

Parameter	Description	Value (mil)
H1	Substrate 1 Height	4
Er1	Substrate 1 Dielectric	4.2
W1	Lower Trace Width	6
W2	Upper Trace Width	5
S1	Trace Separation	7
G1	Lower Ground Strip Width	20
G2	Upper Ground Strip Width	19
D1	Ground Strip Separation	6.75
T1	Trace Thickness	1.8
C1	Coating Above Substrate	1
C2	Coating Above Trace	1
C3	Coating Between Traces	1
CEr	Coating Dielectric	4.2

The calculated impedance is 87.35 Ω based on the preceding parameters.

Therefore, when the board thickness is 1.6 mm and the substrate dielectric is 4.2, **W1** must be 6 mils, **S1** must be 7 mils, **D1** must be greater than 6.75 mils (GND traces are not necessarily required), and **T1** must be 1.8 mils.

50 Ω Impedance Control

The 50 Ω impedance needs to be controlled for the DDR single-ended traces.

Calculate the target impedance by using an impedance calculator. See Figure 1-13 and Table 1-8.

Figure 1-13 Calculating the 50 Ω single-ended impedance for the 4-layer PCB

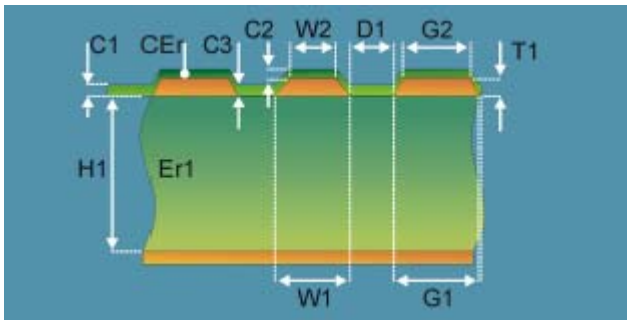


Table 1-8 50 Ω single-ended impedance control parameters

Parameter	Description	Value (mil)
H1	Substrate 1 Height	4
Er1	Substrate 1 Dielectric	4.2
W1	Lower Trace Width	5
W2	Upper Trace Width	4
G1	Lower Ground Strip Width	20
G2	Upper Ground Strip Width	19
D1	Ground Strip Separation	7.5
T1	Trace Thickness	1.8
C1	Coating Above Substrate	1
C2	Coating Above Trace	1
C3	Coating Between Traces	1
CEr	Coating Dielectric	4.2

The calculated impedance is 52.82 Ω based on the preceding parameters.

Therefore, when the board thickness is 1.6 mm and the substrate dielectric is 4.2, **W1** must be 5 mils, **D1** must be greater than 6.75 mils (GND traces are not necessarily required), and **T1** must be 1.8 mils.

1.3 Confirmation of Board Production Parameters

After layout by using the preceding parameters, the board design is delivered to the board manufacturer for manufacturing. The board manufacturer fine-tunes the parameters such as the trace width, spacing, and substrate based on impedance control and sends the result to the PCB layout engineer for confirmation. It is recommended that the PCB layout engineer check whether the impedance is correct by using the impedance calculator and parameters from the board manufacturer.

2 DC-DC Peripheral Impedance for the CPU and Core Power

Table 2-1 describes the DC-DC peripheral impedance for the CPU and core power.

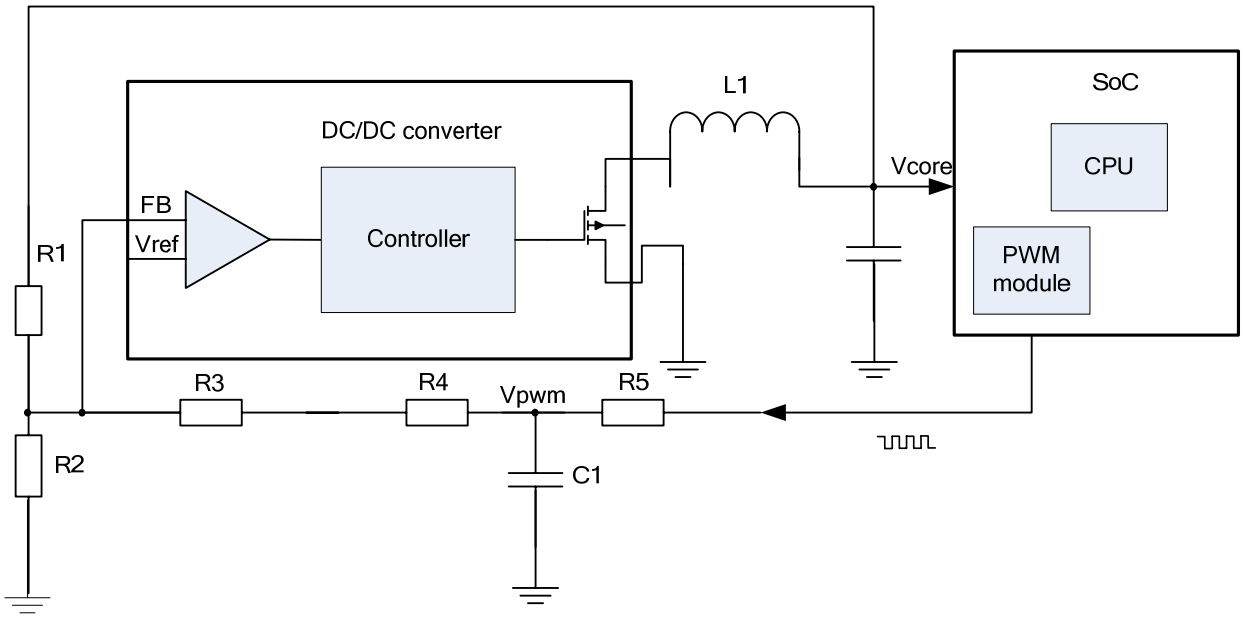
Table 2-1 DC-DC peripheral impedance for the CPU and core power

Recommended Peripheral Impedance for the Hi3798M V100 CPU Power (Vmax = 1.5, Vmin = 0.92)								
Vref (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	R5 (kΩ)	C (μF)	Vmax (V)	Umin (V)
0.6	15	11.3	33	51	1	2.2	1.50	0.92
0.765	20	24.9	10	100	1	2.2	1.52	0.92
0.803	34.8	49.9	47	150	1	2.2	1.50	0.92
0.807	34.8	51	47	150	1	2.2	1.50	0.92
Recommended Peripheral Impedance for the Hi3798M V100 Core Power (Vmax = 1.32, Vmin = 0.9)								
Vref (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	R5 (kΩ)	C (μF)	Vmax (V)	Umin (V)
0.6	14.7	13.7	14.7	100	1	2.2	1.32	0.90
0.8	26.1	49.9	4.99	200	1	2.2	1.32	0.90
0.807	20	39.2	5.49	150	1	2.2	1.32	0.90
0.765	27	45.3	12	200	1	2.2	1.32	0.90
0.92	12	39	11	82	1	2.2	1.32	0.90
0.923	18.7	61.9	33	113	1	2.2	1.32	0.90
0.925	20	66.5	34.8	121	1	2.2	1.32	0.90

CAUTION

- The DC-DC with less than or equal to 2% Vref precision is recommended.
- The DC-DC working frequency must be greater than or equal to 640 kHz.

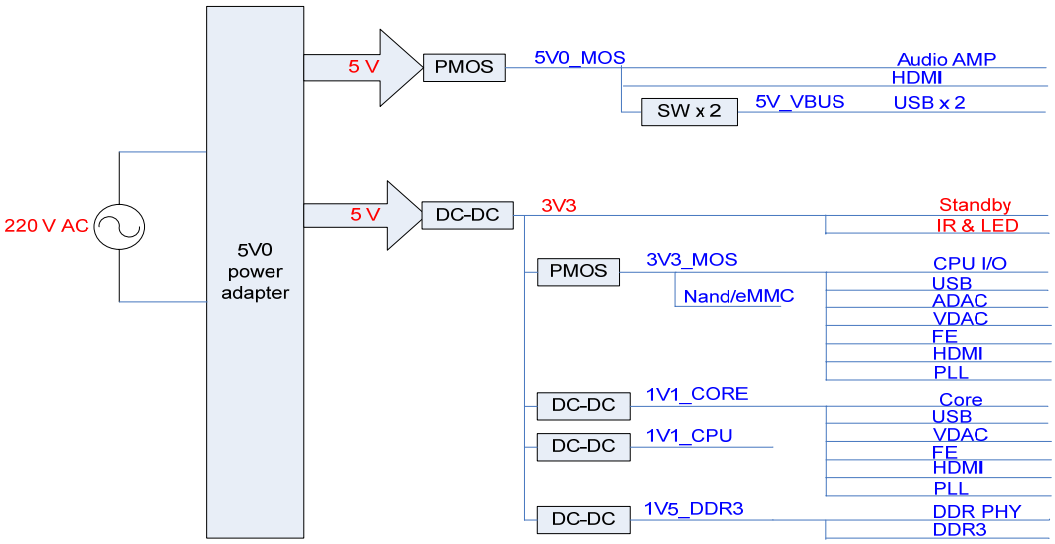
Figure 2-1 Implementation of PWM voltage adjustment



3 Board Standby Design

Hi3798M V100 supports passive standby. The standby power consumption is significantly affected due to the efficiency difference between the DC-DC power and AC-DC power adapter on the board. Figure 3-1 shows the reference power design with less than 0.5 W standby power consumption.

Figure 3-1 Power tree of the HiSilicon demo board



The HiSilicon reference design uses the 5 V power adapter. The power supplies in blue in the preceding figure need to be turned off during standby, and the power supplies in red cannot be turned off during standby.

Table 3-1 describes the standby power consumption of the HiSilicon demo board when it works properly.

Table 3-1 Standby power consumption of the Hi3798M V100 demo board

Power Consumption (W)	Current of the 5 V Adapter (mA)	Voltage of the 5 V Adapter (V)
0.44	32	5.35

The standby power consumption of the board is calculated as follows: 5.35 V x 32 mA = 171.2 mW

The standby power consumption of the STB is 440 mW.

Therefore, the actual efficiency η of the power adapter during standby is calculated as follows:

η = 171.2 mW/440 mW x 100% = 38.9%

If the standby power consumption needs to be less than 0.5 W, the minimum efficiency of the power adapter should be as follows:

η_{min} = 171.2 mW/500 mW x 100% = 34.2%

The low-power design is related to the power consumption of the mother board as well as the conversion rate of the power adapter. The calculated value 38.9% is the conversion rate of the HiSilicon power adapter in standby mode.

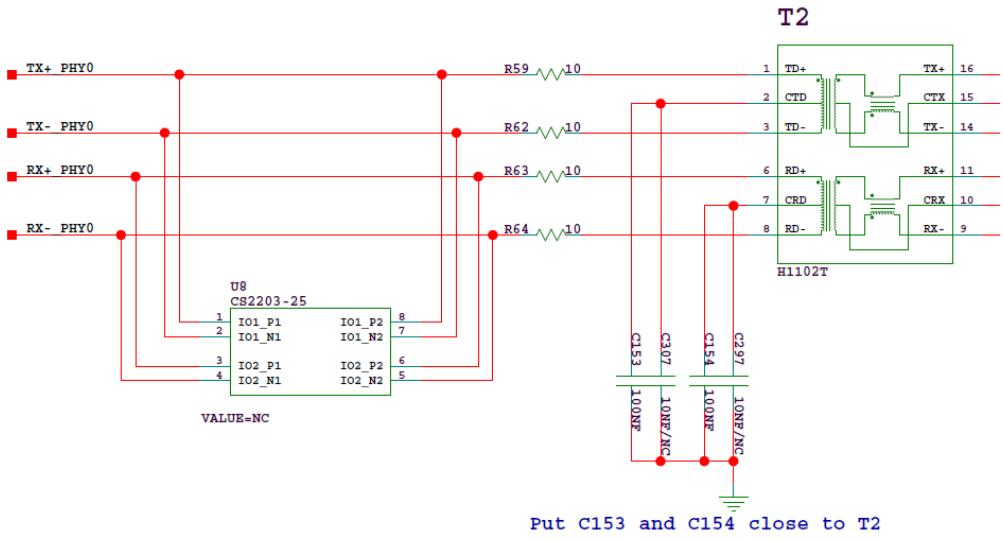
The standby power consumption is closely related to the design of the power adapter. The most important specification is the conversion rate of the power adapter with light load. According to tests, if the standby power consumption must be less than 0.5 W, the conversion rate of the power adapter cannot be lower than 34.2%.

In addition to the efficiency of the power adapter, the efficiency of the board DC-DC is also an important factor that affects the standby power consumption. The DC-DC efficiency is very low in light load state. You should pay special attention to it during design.

4 500 V Surge Withstand Capability in Differential Mode

Connect a transient voltage suppressor (TVS) CS2033 or four 10 Ω resistors in serial to the TX and RX interfaces between the master chip and the transformer of the network port close to the transformer. The four 10 Ω resistors in serial provide at most 500 V surge withstand capability in differential mode. If you require the 1000 V or 1500 V capability, the TVS is recommended.

Figure 4-1 Functional diagram of the 500 V surge withstand capability in differential mode



5 6 kV Board ESD Design

To ensure the 6 kV electrostatic discharge (ESD) contact discharge of the board, a shield cover must be reserved at the bottom side of the board for protecting the master chip and the DDR.

Figure 5-1 Shield cover at the bottom side of the Hi3798M DMO1A board

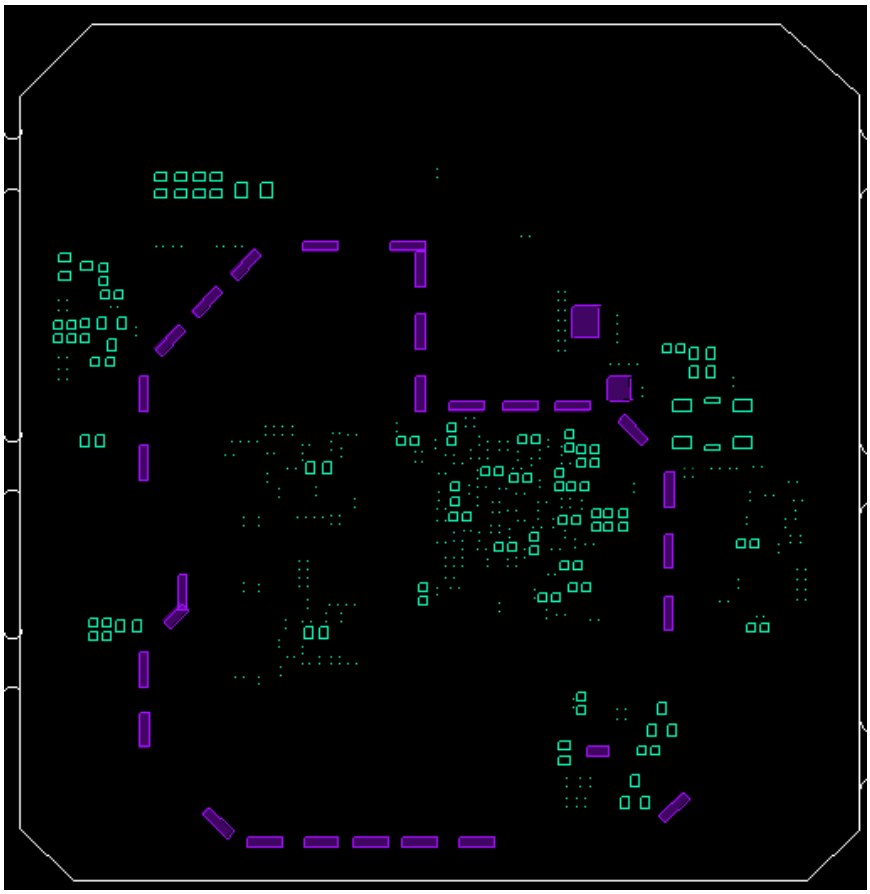


Figure 5-2 Shield cover at the bottom side of the Hi3798M DMO1B board

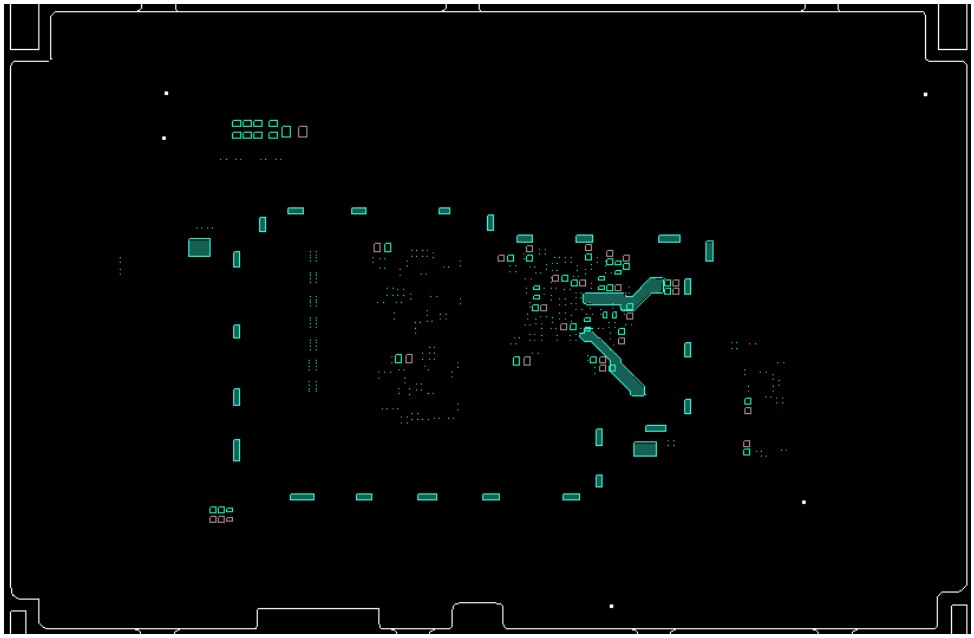


Figure 5-3 Shield cover at the bottom side of the Hi3798M DMO1C board

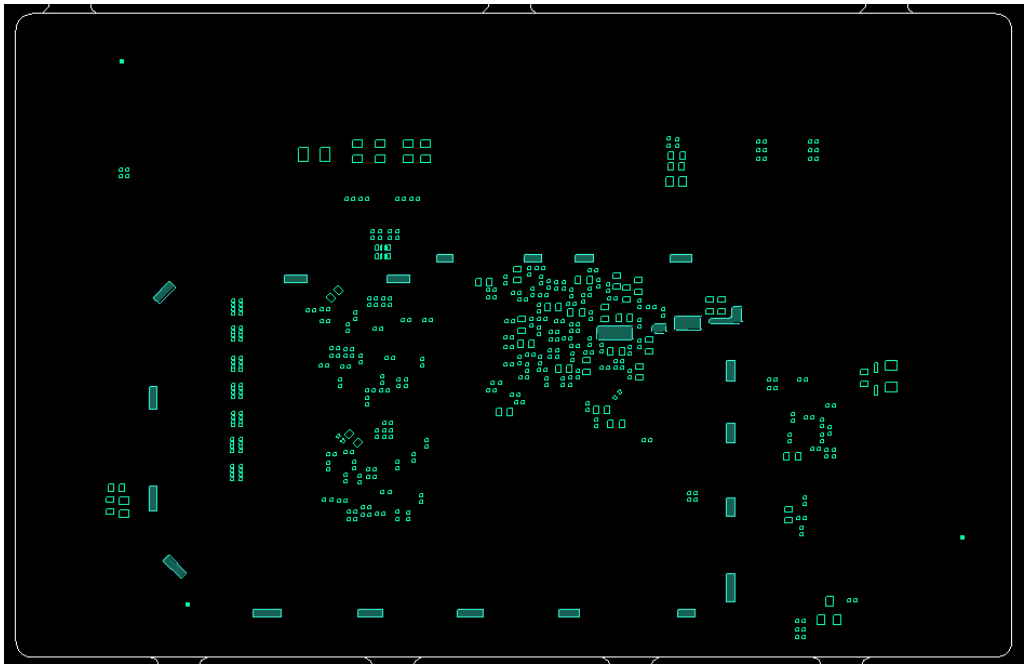
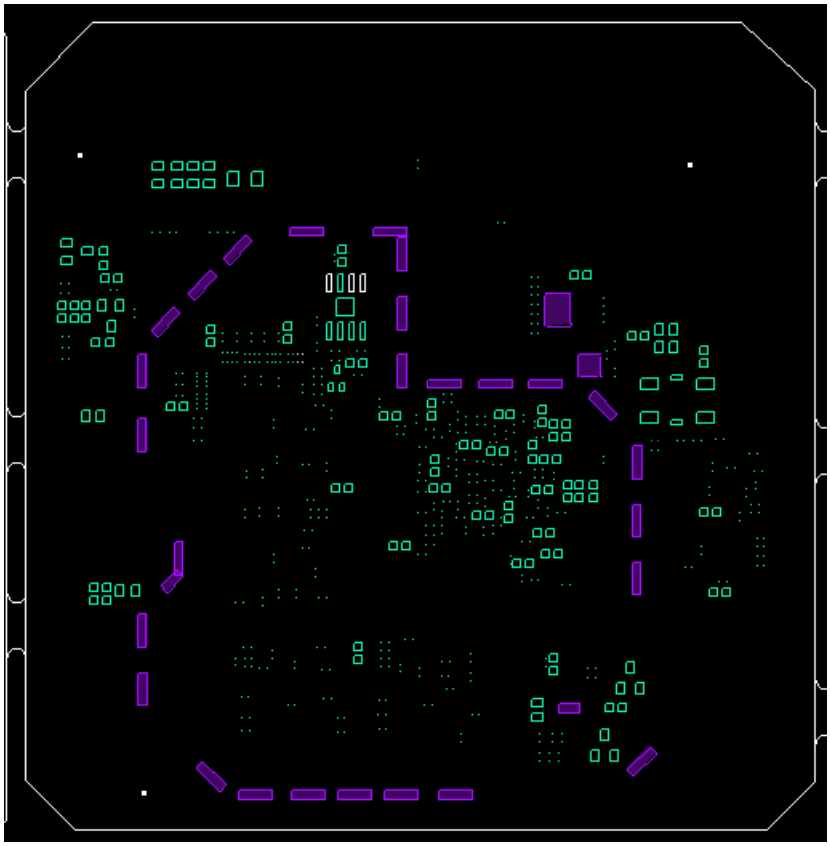


Figure 5-4 Shield cover at the bottom side of the Hi3798M DMO1D board



6 FAQs

6.1 GPIO Power Domain

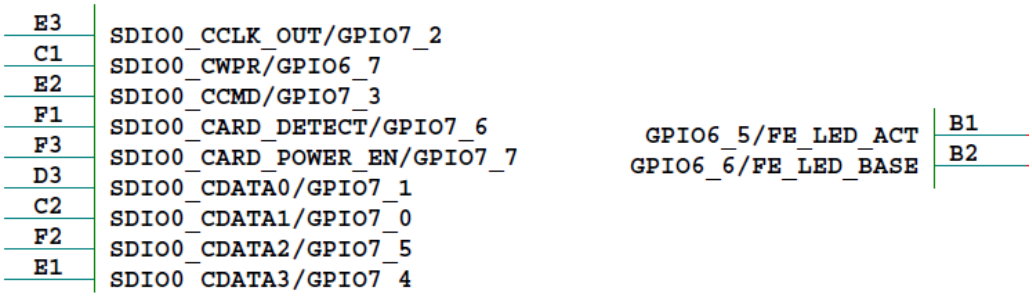
Problem Description

When the 1.8 V SD card is inserted into the SDIO 3.0 interface, the voltage of the GPIO7_0, GPIO7_1, GPIO7_2, GPIO7_4, GPIO7_5, GPIO7_6, GPIO7_7, GPIO6_5, GPIO6_6, and GPIO6_7 pins is changed to 1.8 V.

Solution

During board design, do not connect the pins shown in Figure 6-1 to pins in the 3.3 V power domain.

Figure 6-1 1.8 V GPIO pins



6.2 eMMC Power-On Timing

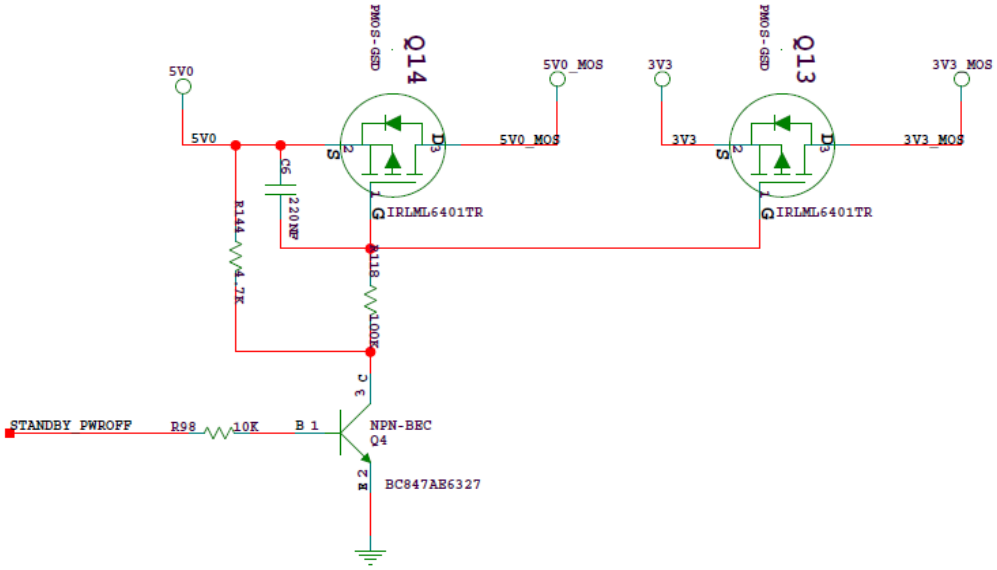
Problem Description

The eMMC is burnt successfully but cannot be started sometimes, and the eMMC read error is displayed.

Solution

Change the power-on timing of the I/O power of the master chip and the 3.3 V eMMC power. Add a soft-start circuit, as shown in Figure 6-2. Use 3V3_MOS for the master chip I/O power and eMMC power, and ensure that the 3V3_MOS power is turned on 10 ms after the 1V1_CORE power is turned on.

Figure 6-2 3V3_MOS soft-start circuit



6.3 fSD/eMMC CLK I/O Driving Capability

Problem Description

For the Hi3798M V100 2-layer PCB, the fSD/eMMC CLK I/O driving capability can be 1 mA or 2 mA.

Solution

- When the fSD/eMMC CLK I/O driving capability is set to 1 mA, the chip rise time is beyond specifications, which may result in data sampling errors. Therefore, the 1 mA driving capability needs to be changed to 2 mA. For details, see the value of the 0xf8a21030 register in the **pin_mux_drv_emmc** sheet of the fastboot configuration table. 2 mA corresponds to the value **0xd01** (default value).
- When the fSD/eMMC CLK I/O driving capability is set to 2 mA, the signal timings and sampling level are normal, and data read and write are not affected. However, overshoot occurs for CLK signals, which may result in electromagnetic compatibility (EMC) issues. If you have high requirements on the EMC, you are advised to connect a 75 Ω matched resistor in series to the CLK signals; otherwise, you do not need to modify the hardware.

6.4 ESD Performance for the QFP Package

Problem Description

The STB ESD performance is poor when the Hi3798M V100 QFP package is used.

Solution

- Reserve a shield cover at the top layer and bottom layer respectively to protect the master chip, crystal, and DDR.
- Reserve a 600 Ω@100 MHz EMI bead with the 0402 package (LB3) and two 100 nF grounded capacitors with the 0402 package (C118 and C119) in the STANDBY_PWROFF circuit, and place them near the master chip during PCB layout. Figure 6-3 shows the reference design of the DMO board. When ESD issues occur, adjust the EMI bead and the capacitance as required.
- Reserve a 600 Ω@100 MHz EMI bead with the 0402 package (LB5) and two 100 nF grounded capacitors with the 0402 package (C108 and C122) in the 3V3_STANDBY circuit, and place them near the master chip during PCB layout. Figure 6-4 shows the reference design of the DMO board. When ESD issues occur, adjust the EMI bead and the capacitance as required.
- Reserve two 600 Ω@100 MHz EMI bead (LB21 and LB22) in the PLL circuit, and place them near the master chip during PCB layout. Figure 6-5 shows the reference design of the DMO board. When ESD issues occur, adjust the EMI bead and the capacitance as required.

Figure 6-3 STANDBY_PWROFF circuit

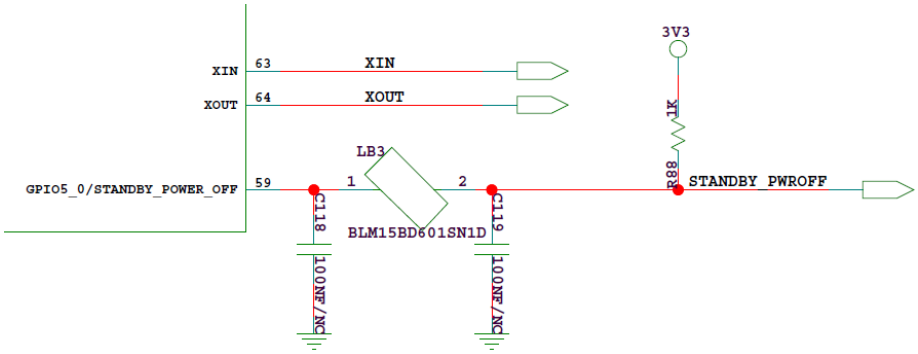


Figure 6-4 3V3_STANDBY circuit

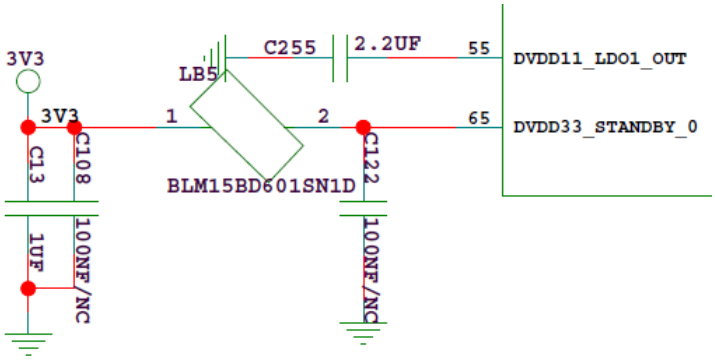
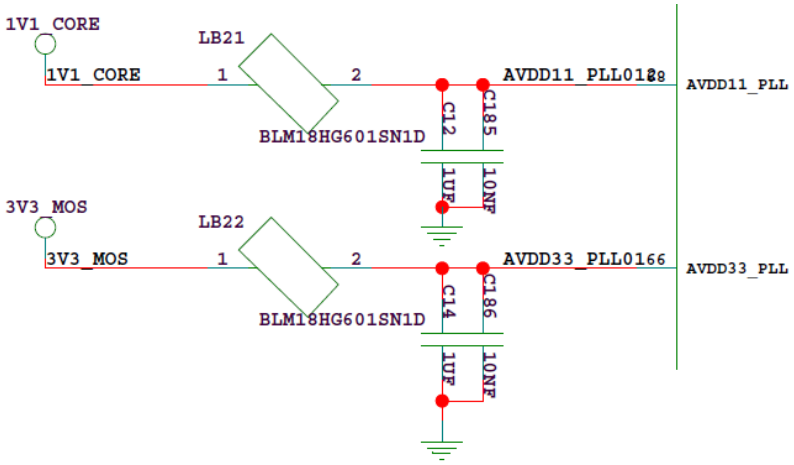


Figure 6-5 PLL circuit



6.5 Heat Dissipation Performance for the QFP Package

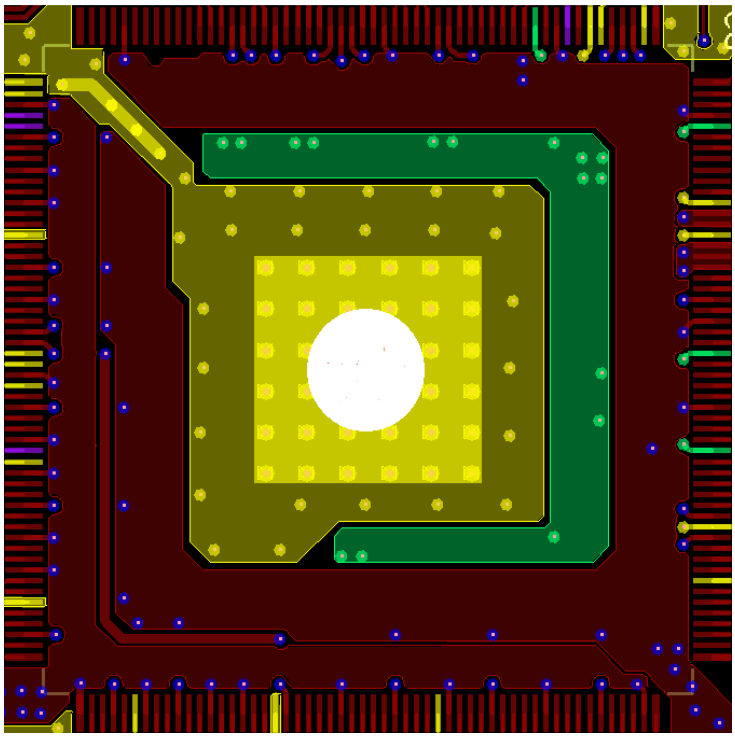
Problem Description

The heat dissipation performance needs to be optimized for the Hi3798M V100 QFP board to reduce the chip junction temperature.

Solution

Punch thermal vias on the PCB thermal pad under the exposed pad of the master chip and pour solder paste, as shown in Figure 6-6. Note that this thermal pad is a grounded pad and needs to be soldered properly to the exposed pad of the master chip. You are advised to adjust the size of the thermal vias based on the soldering process.

Figure 6-6 Thermal vias on the PCB



6.6 Abnormal Boot Mode

Problem Description

When Hi3798M V100 is configured to boot from the eMMC flash by default, it sometimes incorrectly identifies the boot mode as booting from the NAND flash.

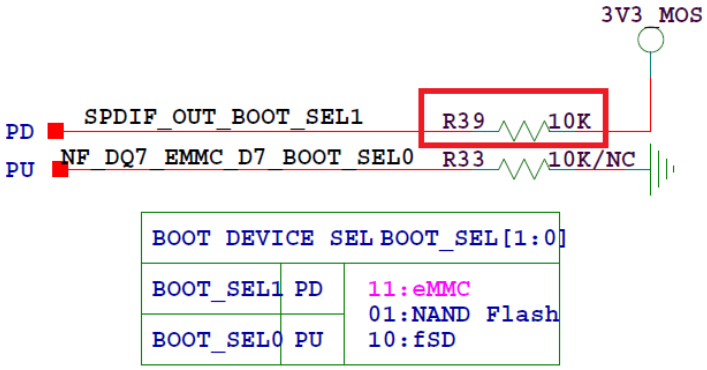
Analysis

For Hi3798M V100, the boot configuration pin BOOT_SEL1 is multiplexed with the S/PDIF pin. If an external S/PDIF component with internal pull-down resistors is connected, and the pull-up resistor R39 is 10 kΩ (as shown in Figure 6-7), the voltage on BOOT_SEL1 is determined as low level after voltage division. In this case, the system incorrectly identifies the boot mode as booting from the NAND flash.

Solution

If an external S/PDIF component is connected, change the pull-up resistor R39 of BOOT_SEL1 from 10 kΩ to 1 kΩ. If there is no external S/PDIF component connected, retain the 10 kΩ R39, as shown in Figure 6-7.

Figure 6-7 Circuit of pull-up/down resistors of boot configuration pins



6.7 768 MB DDR Capacity Configuration

Problem Description

Special attention must be paid during the hardware design when the DDR capacity of the Hi3798M V100 board is 768 MB.

Solution

- BOM: For the 768 MB memory version, the lower 16 bits of the DQ signals connect to the 512 MB DDR (corresponding to U3 in the schematic diagram design), and the upper 16 bits of the DQ signals connect to the 256 MB DDR (corresponding to U6 in the schematic diagram design).
- The fastboot table with the name containing **768mbyte** is required.
- In the Hi3798M hardware reference design, the 1A, 1B, 1C, 1F, and 1G versions but not the 1D version support the 768 MB DDR.

6.8 System Stability Improvement Measure for the Hi3798M V100 1F/1G Version

Problem Description

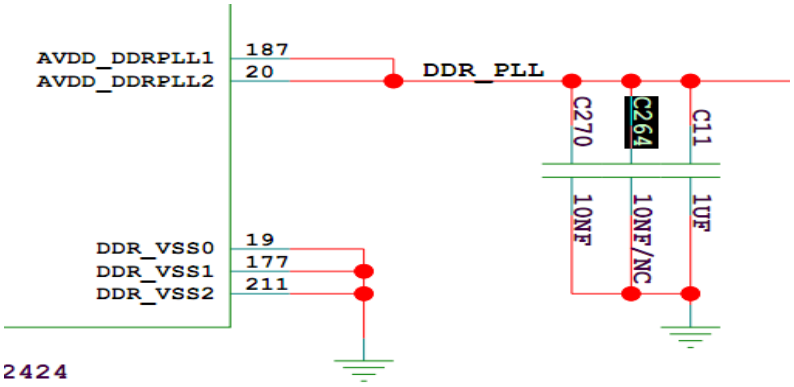
For the 1F and 1G Hi3798M V100 QFP versions, when system instability occurs or the stability of the board testing needs to be strengthened, what modifications can be made on the hardware and design?

Solution

- SCH:

  The 10 nF capacitor for C264 corresponding to the schematic diagram in the HiSilicon release package must be not connected.

Figure 6-8 C264 of schematic diagram



  - The LB7 beads corresponding to the DDR PLL in the HiSilicon release package must be changed to 600 Ω@100 MHz beads. The 10 nF capacitor for non-connected C264 must be pasted.

- Table: The boot table needs to be updated to the table released by HiSilicon after November, 2015. The DDR part in the table is modified to rectify this issue. The key modification points on the DDR in the table are as follows:
  - On the sysctrl_CA and sysctrl_noCA pages of the table, modify the red word in the yellow row respectively. Both the Hi3798M V100 1F and 1G versions need to make such modification. See Figure 6-9.

Figure 6-9 Screenshot of the row to be modified on the sysctrl_CA and sysctrl_noCA pages

DDR_TRAINING_CFG	0xd0	0x100	0	write	31	0	0x000000FF

  - Add a new row in yellow (three rows in total) on the ddrphy, ddr_poweron, and ddr_wakeup pages respectively. Both the Hi3798M V100 1F and 1G versions need to make such modification. See screenshots in Figure 6-10 and Figure 6-11.

Figure 6-10 Screenshot of adding a new yellow row on the ddrphy page

ODTCTRL	0x44	0x1	0	write	31	0	0x000000FF
TRAINCTRL0	0x48	0xd04410c0	0	write	31	0	0x000000FF
TRAINCTRL	0xd0	0xb036f026	0	write	31	0	0x000000FF

Figure 6-11 Screenshot of adding a new yellow row on the ddr_poweron page

MISC	0xa38070	0x1	0	write	0	16	0x000000FD

  - Modify two yellow rows on the ddrphy page. Only the Hi3798M V100 1F version needs to make such modification. See the screenshot in Figure 6-12.

Figure 6-12 Screenshot of the rows to be modified on the ddrphy page

ACCMDBDL2	0x128	0x4	0	write	31	0	0x0000000FF
ACCMDBDL3	0x1a8	0x4	0	write	31	0	0x0000000FF

- The default value for the DQ read/write on the ddrphy page also needs to be changed for both the Hi3798M V100 1F and 1G versions. It is not convenient to provide the screenshot. Please refer to the table directly.