Hi3796M V100 Intelligent Network Terminal Media Processor

Hardware User Guide

Issue 01

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About This Document

Purpose

This document describes the hardware package, pins, pin multiplexing registers, electrical specifications, schematic diagram design, printed circuit board (PCB) design, thermal design, soldering technology, moisture-sensitive specifications, and interface timings for Hi3796M V100. It also describes precautions for using Hi3796M V100.

This document provides hardware design reference for hardware development engineers.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3796M	V1XX

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Alerts you to a high risk hazard that could, if not avoided, result in serious injury or death.

Symbol	Description
WARNING	Alerts you to a medium or low risk hazard that could, if not avoided, result in moderate or minor injury.
CAUTION	Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results.
TIP	Provides a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points in the main text.

Register Attributes

The register attributions that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576

Type	Symbol	Value
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 01 (2015-08-20)

This issue is the first official release, which incorporates the following changes.

The information aboat TS interface is modified.

Issue 00B02 (2014-12-26)

This issue is the second draft release, which incorporates the following changes.

The pull-up/pull-down enable information about some pin multiplexing registers is updated.

Issue 00B01 (2014-11-20)

This issue is the first draft release.

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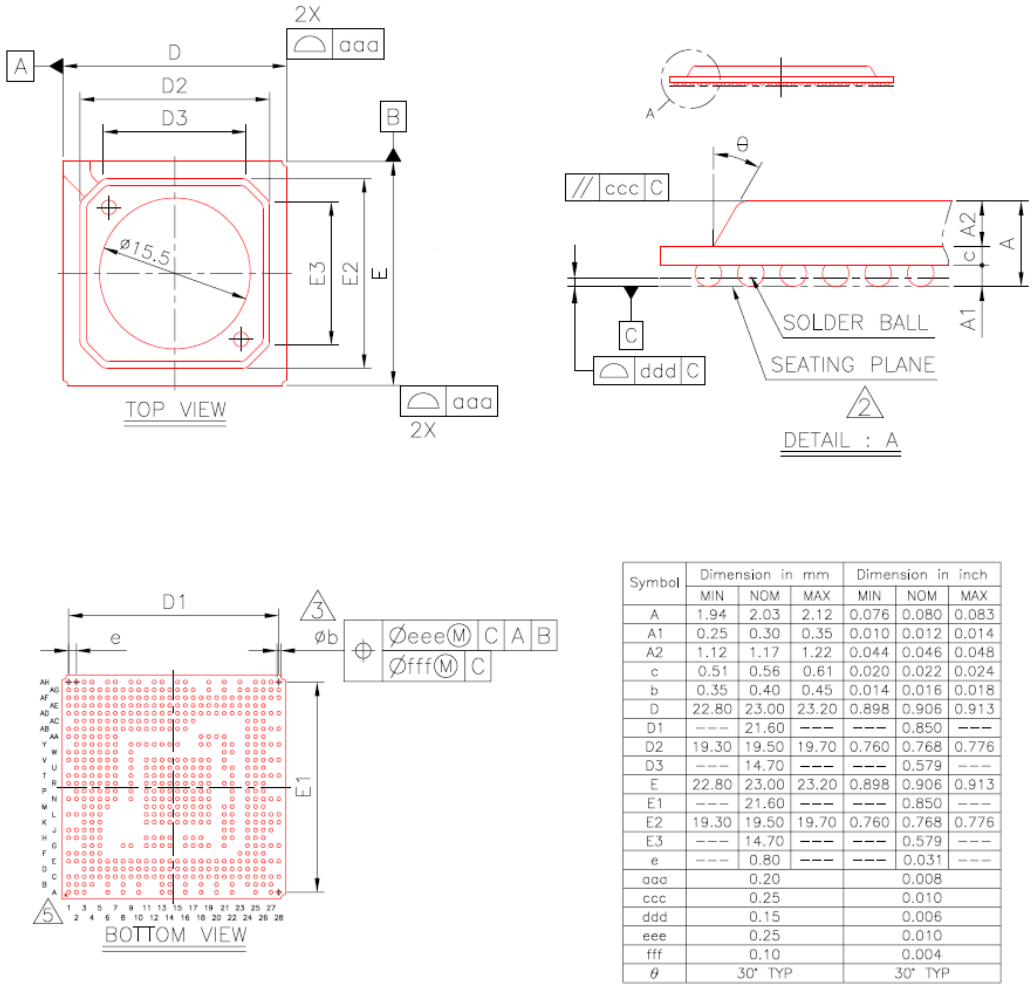
1 Package and Pins

1.1 Package and Pinout

1.1.1 Package

Hi3796M V100 uses the plastic ball grid array (PBGA) package with 573 pins. Its body size is 23 mm x 23 mm (0.91 in. x 0.91 in.), and its ball pitch is 0.8 mm (0.03 in.). Figure 1-1 shows the package views.

Figure 1-1 Hi3796M V100 package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.94	2.03	2.12	0.076	0.080	0.083
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	1.12	1.17	1.22	0.044	0.046	0.048
c	0.51	0.56	0.61	0.020	0.022	0.024
b	0.35	0.40	0.45	0.014	0.016	0.018
D	22.80	23.00	23.20	0.898	0.906	0.913
D1	---	21.60	---	---	0.850	---
D2	19.30	19.50	19.70	0.760	0.768	0.776
D3	---	14.70	---	---	0.579	---
E	22.80	23.00	23.20	0.898	0.906	0.913
E1	---	21.60	---	---	0.850	---
E2	19.30	19.50	19.70	0.760	0.768	0.776
E3	---	14.70	---	---	0.579	---
e	---	0.80	---	---	0.031	---
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
θ	30° TYP			30° TYP		

1.1.2 Pin Map

Figure 1-2 to Figure 1-5 show the pin maps of Hi3796M V100.

Figure 1-2 Pin map part 1 (A1−P14)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	VSS	VSS			FE_RXN		USB0_DM		I2S0_DOUT0			SPI_SCLK	SPI_CSN1
B	FE_LED_ACT	VSS	VSS	AVSS_FE		FE_RXP		USB0_DP		I2S0_WS			SPI_CSN0	VSS
C	SDIO0_CWPR	FE_LED_BASE	VSS	AVSS_FE	FE_TXN	AVSS_FE	AVSS_FE	AVSS_USB	USB1_DM	AVSS_USB	I2S0_MCLK	SLIC_RST	SPI_SDO	VSS
D			SDIO0_CDATA1	AVSS_FE	FE_TXP	AVSS_FE	AVSS_FE	AVSS_USB	USB1_DP	AVSS_USB	I2S0_DIN0	I2S0_BCLK	SPI_SDI	VSS
E	SDIO0_CCLK_OUT	VSS	SDIO0_CDATA0	VSS	AVSS_FE	AVDD33_FE	AVDD33_FE	AVSS_USB	AVSS_USB	AVDD33_USB01	VSS	VSS	DVDD33	DVDD33
F	VSS	SDIO0_CCMD	VSS	VSS	VSS									
G			SDIO0_CDATA3	VSS	DVDD33			AVSS_FE	FE_REXT		USBRBIAS	AVSS_USB	VSS	VSS
H	VSS	VSS	SDIO0_CDATA2	VSS	VSS						AVCC11_USB	AVSS_USB	VSS	VSS
J	SDIO0_CARD_POW	SDIO0_CARD_DET	VSS	VSS	VSS									
K			VSS	DVDD3318_LDO2	DVDD3318_LDO2						AVSS_FE	AVDD11_FE	VSS	VDD
L	VSS	VSS	VSS	VSS	VSS						VSS	VSS	VSS	VDD
M			VSS	VSS	VSS	VSS					VSS	VSS	VSS	VDD
N	DDR3_DQ2	DDR3_DQ6	VSS	DDR3_DQ0	DDR3_DQ4	VSS	VDDIO_DDR		VDDIO_DDR		VSS	VSS	VSS	VDD
P		VSS	DDR3_DQ11	DDR3_DQ13	DDR3_DQ15	VSS	VDDIO_DDR		VDDIO_DDR		VSS	VSS	VSS	VDD

Figure 1-3 Pin map part2 (R1−AH14)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R	VSS	DDR3_DQ9	VSS	DDR3_DM0	VSS	VDDIO_DDR	VDDIO_DDR		VSS		VDD	VSS	VSS	VDD
T	DDR3_DQS0_N	DDR3_DQS0_P	VSS	VSS	DDR3_DM1	VSS	VDDIO_DDR		AVDD_DDRPLL1		VDD	VSS	VSS	VDD
U		DDR3_DQS1_P	DDR3_DQS1_N	DDR3_DQ8	DDR3_DQ10	VSS	VDDIO_DDR		VSS		VDD	VDD	VDD	VDD
V	DDR3_DQ1	VSS	VSS	DDR3_DQ12	VSS	VSS	VDDIO_DDR		VSS		VDD	VDD	VDD	VDD
W	VSS	DDR3_DQ7	DDR3_DQ3	DDR3_DQ14	VSS	VSS	VDDIO_DDR		VDDIO_DDR					
Y		VSS	DDR3_DQ5	VSS	DDR3_DQ20	VSS	VDDIO_DDR		VDDIO_DDR	VSS	VDDIO_CK_DDR	VDDIO_CK_DDR	VSS	AVDD_DDRPLL2
AA	VSS	DDR3_DQ18	DDR3_DQ22	DDR3_DQ29	DDR3_DQ16	VSS	VDDIO_DDR							
AB	DDR3_DQ25	VSS	DDR3_DQ27	DDR3_DQ31	VSS	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR
AC		DDR3_DQS2_N	DDR3_DQS2_P	VSS	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VSS	VSS	VSS	VDDIO_DDR	VSS	VSS
AD	DDR3_DQS3_P	DDR3_DQS3_N	VSS	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VSS	VSS	DDR3_CKE	DDR3_ADDR4	VSS	DDR3_ADDR15	VSS
AE	VSS	DDR3_DM3	VSS	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VSS	VSS	DDR3_ADDR10	VSS	DDR3_ADDR1	DDR3_ADDR11	DDR3_BA2	DDR3_WE_N
AF	DDR3_DM2	VSS	VSS	VSS	DDR3_DQ24	DDR3_DQ17	DDR3_DQ23	DDR3_CLK1_P	VSS	DDR3_BA1	DDR3_ADDR6	DDR3_ADDR14	DDR3_ADDR9	VSS
AG	VSS	VSS	DDR3_DQ30	DDR3_DQ26	VSS	DDR3_DQ19	VSS	DDR3_CLK1_N	DDR3_CLK0_N	DDR3_ADDR12	VSS	DDR3_ADDR8	VSS	DDR3_RESET_N
AH	VSS	VSS	DDR3_DQ28	VSS		VSS	DDR3_DQ21		DDR3_CLK0_P	VSS		VSS	DDR3_CS_N_0	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Figure 1-4 Pin map part3 (R15−AH28)

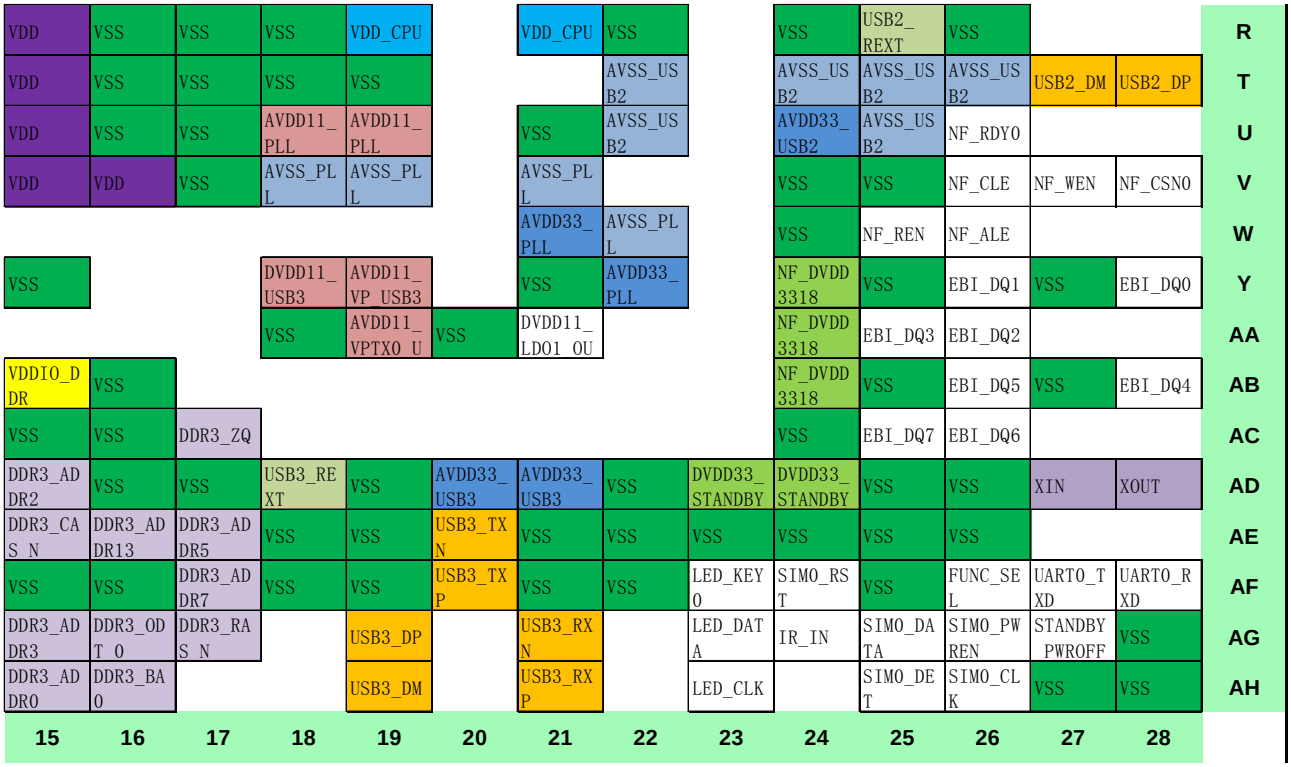
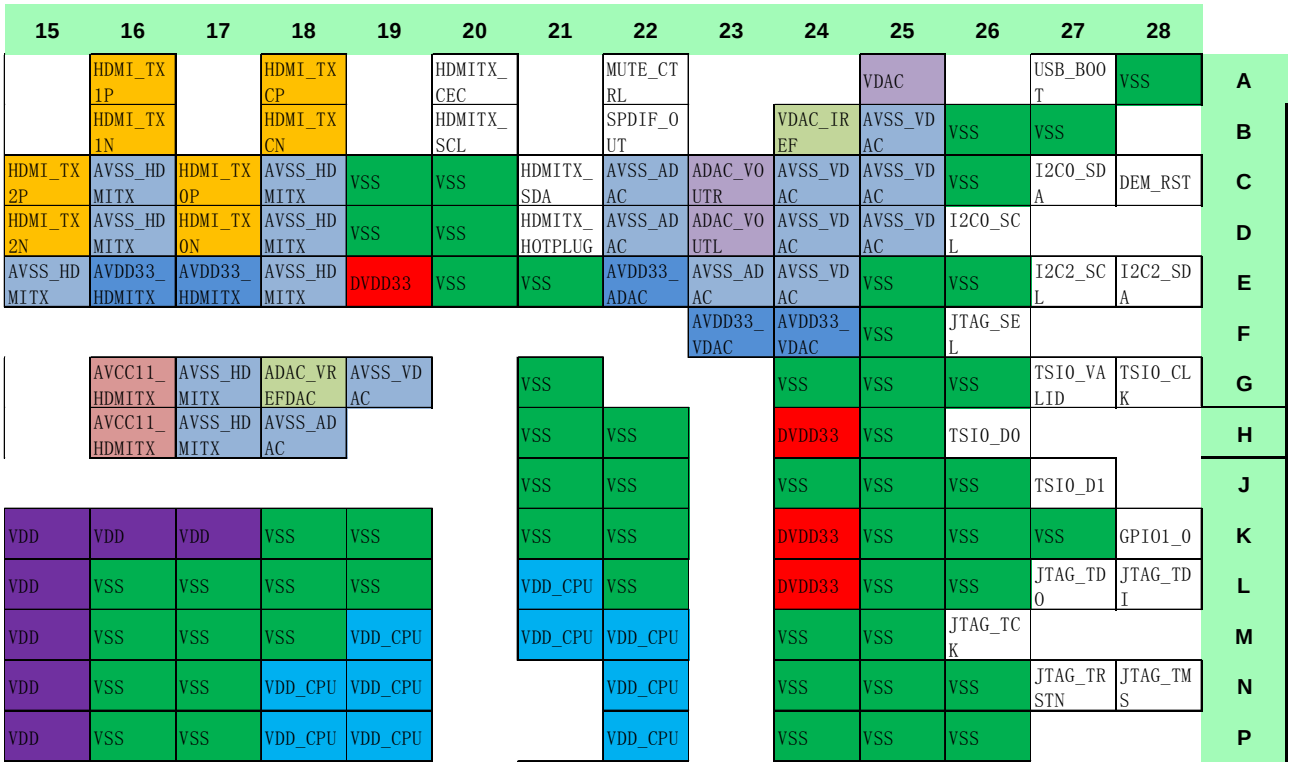


Figure 1-5 Pin map part4 (A15−P28)



1.1.3 Pin Arrangement

Table 1-1 lists the pins of Hi3796M V100 by position.

Table 1-1 Pin arrangement

Position	Pin Name	Position	Pin Name
A1	VSS	E24	AVSS_VDAC
A2	VSS	E25	VSS
A3	VSS	E26	VSS
A6	FE_RXN	E27	I2C2_SCL
A8	USB0_DM	E28	I2C2_SDA
A10	I2S0_DOUT0	F1	VSS
A13	SPI_SCLK	F2	SDIO0_CCMD
A14	SPI_CSN1	F3	VSS
A16	HDMI_TX1P	F4	VSS
A18	HDMI_TXCP	F5	VSS
A20	HDMITX_CEC	F23	AVDD33_VDAC
A22	MUTE_CTRL	F24	AVDD33_VDAC
A25	VDAC	F25	VSS
A27	USB_BOOT	F26	JTAG_SEL
A28	VSS	G3	SDIO0_CDATA3
AA1	VSS	G4	VSS
AA2	DDR3_DQ18	G5	DVDD33
AA3	DDR3_DQ22	G8	AVSS_FE
AA4	DDR3_DQ29	G9	FE_REXT
AA5	DDR3_DQ16	G11	USBRBIAS
AA6	VSS	G12	AVSS_USB
AA7	VDDIO_DDR	G13	VSS
AA18	VSS	G14	VSS
AA19	AVDD11_VPTX0_USB3	G16	AVCC11_HDMITX
AA20	VSS	G17	AVSS_HDMITX
AA21	DVDD11_LDO1_OUT	G18	ADAC_VREFDAC
AA24	NF_ DVDD3318	G19	AVSS_VDAC

Position	Pin Name	Position	Pin Name
AA25	EBI_DQ3	G21	VSS
AA26	EBI_DQ2	G24	VSS
AB1	DDR3_DQ25	G25	VSS
AB2	VSS	G26	VSS
AB3	DDR3_DQ27	G27	TSI0_VALID
AB4	DDR3_DQ31	G28	TSI0_CLK
AB5	VSS	H1	VSS
AB6	VDDIO_DDR	H2	VSS
AB7	VDDIO_DDR	H3	SDIO0_CDATA2
AB8	VDDIO_DDR	H4	VSS
AB9	VDDIO_DDR	H5	VSS
AB10	VDDIO_DDR	H11	AVCC11_USB01
AB11	VDDIO_DDR	H12	AVSS_USB
AB12	VDDIO_DDR	H13	VSS
AB13	VDDIO_DDR	H14	VSS
AB14	VDDIO_DDR	H16	AVCC11_HDMITX
AB15	VDDIO_DDR	H17	AVSS_HDMITX
AB16	VSS	H18	AVSS_ADAC
AB24	NF_ DVDD3318	H21	VSS
AB25	VSS	H22	VSS
AB26	EBI_DQ5	H24	DVDD33
AB27	VSS	H25	VSS
AB28	EBI_DQ4	H26	TSI0_D0
AC2	DDR3_DQS2_N	J1	SDIO0_CARD_POWER_EN
AC3	DDR3_DQS2_P	J2	SDIO0_CARD_DETECT
AC4	VSS	J3	VSS
AC5	VDDIO_DDR	J4	VSS
AC6	VDDIO_DDR	J5	VSS
AC7	VDDIO_DDR	J21	VSS
AC8	VDDIO_DDR	J22	VSS
AC9	VSS	J24	VSS

Position	Pin Name	Position	Pin Name
AC10	VSS	J25	VSS
AC11	VSS	J26	VSS
AC12	VDDIO_DDR	J27	TSI0_D1
AC13	VSS	K3	VSS
AC14	VSS	K4	DVDD3318_LDO2_OUT
AC15	VSS	K5	DVDD3318_LDO2_OUT
AC16	VSS	K11	AVSS_FE
AC17	DDR3_ZQ	K12	AVDD11_FE
AC24	VSS	K13	VSS
AC25	EBI_DQ7	K14	VDD
AC26	EBI_DQ6	K15	VDD
AD1	DDR3_DQS3_P	K16	VDD
AD2	DDR3_DQS3_N	K17	VDD
AD3	VSS	K18	VSS
AD4	VDDIO_DDR	K19	VSS
AD5	VDDIO_DDR	K21	VSS
AD6	VDDIO_DDR	K22	VSS
AD7	VDDIO_DDR	K24	DVDD33
AD8	VSS	K25	VSS
AD9	VSS	K26	VSS
AD10	DDR3_CKE	K27	VSS
AD11	DDR3_ADDR4	K28	GPIO1_0
AD12	VSS	L1	VSS
AD13	DDR3_ADDR15	L2	VSS
AD14	VSS	L3	VSS
AD15	DDR3_ADDR2	L4	VSS
AD16	VSS	L5	VSS
AD17	VSS	L11	VSS
AD18	USB3_REXT	L12	VSS
AD19	VSS	L13	VSS
AD20	AVDD33_USB3	L14	VDD

Position	Pin Name	Position	Pin Name
AD21	AVDD33_USB3	L15	VDD
AD22	VSS	L16	VSS
AD23	DVDD33_STANDBY	L17	VSS
AD24	DVDD33_STANDBY	L18	VSS
AD25	VSS	L19	VSS
AD26	VSS	L21	VDD_CPU
AD27	XIN	L22	VSS
AD28	XOUT	L24	DVDD33
AE1	VSS	L25	VSS
AE2	DDR3_DM3	L26	VSS
AE3	VSS	L27	JTAG_TDO
AE4	VDDIO_DDR	L28	JTAG_TDI
AE5	VDDIO_DDR	M3	VSS
AE6	VDDIO_DDR	M4	VSS
AE7	VSS	M5	VSS
AE8	VSS	M6	VSS
AE9	DDR3_ADDR10	M11	VSS
AE10	VSS	M12	VSS
AE11	DDR3_ADDR1	M13	VSS
AE12	DDR3_ADDR11	M14	VDD
AE13	DDR3_BA2	M15	VDD
AE14	DDR3_WE_N	M16	VSS
AE15	DDR3_CAS_N	M17	VSS
AE16	DDR3_ADDR13	M18	VSS
AE17	DDR3_ADDR5	M19	VDD_CPU
AE18	VSS	M21	VDD_CPU
AE19	VSS	M22	VDD_CPU
AE20	USB3_TXN	M24	VSS
AE21	VSS	M25	VSS
AE22	VSS	M26	JTAG_TCK
AE23	VSS	N1	DDR3_DQ2

Position	Pin Name	Position	Pin Name
AE24	VSS	N2	DDR3_DQ6
AE25	VSS	N3	VSS
AE26	VSS	N4	DDR3_DQ0
AF1	DDR3_DM2	N5	DDR3_DQ4
AF2	VSS	N6	VSS
AF3	VSS	N7	VDDIO_DDR
AF4	VSS	N9	VDDIO_DDR
AF5	DDR3_DQ24	N11	VSS
AF6	DDR3_DQ17	N12	VSS
AF7	DDR3_DQ23	N13	VSS
AF8	DDR3_CLK1_P	N14	VDD
AF9	VSS	N15	VDD
AF10	DDR3_BA1	N16	VSS
AF11	DDR3_ADDR6	N17	VSS
AF12	DDR3_ADDR14	N18	VDD_CPU
AF13	DDR3_ADDR9	N19	VDD_CPU
AF14	VSS	N22	VDD_CPU
AF15	VSS	N24	VSS
AF16	VSS	N25	VSS
AF17	DDR3_ADDR7	N26	VSS
AF18	VSS	N27	JTAG_TRSTN
AF19	VSS	N28	JTAG_TMS
AF20	USB3_TXP	P2	VSS
AF21	VSS	P3	DDR3_DQ11
AF22	VSS	P4	DDR3_DQ13
AF23	LED_KEY0	P5	DDR3_DQ15
AF24	SIM0_RST	P6	VSS
AF25	VSS	P7	VDDIO_DDR
AF26	FUNC_SEL	P9	VDDIO_DDR
AF27	UART0_TXD	P11	VSS
AF28	UART0_RXD	P12	VSS

Position	Pin Name	Position	Pin Name
AG1	VSS	P13	VSS
AG2	VSS	P14	VDD
AG3	DDR3_DQ30	P15	VDD
AG4	DDR3_DQ26	P16	VSS
AG5	VSS	P17	VSS
AG6	DDR3_DQ19	P18	VDD_CPU
AG7	VSS	P19	VDD_CPU
AG8	DDR3_CLK1_N	P22	VDD_CPU
AG9	DDR3_CLK0_N	P24	VSS
AG10	DDR3_ADDR12	P25	VSS
AG11	VSS	P26	VSS
AG12	DDR3_ADDR8	R1	VSS
AG13	VSS	R2	DDR3_DQ9
AG14	DDR3_RESET_N	R3	VSS
AG15	DDR3_ADDR3	R4	DDR3_DM0
AG16	DDR3_ODT_0	R5	VSS
AG17	DDR3_RAS_N	R6	VDDIO_DDR
AG19	USB3_DP	R7	VDDIO_DDR
AG21	USB3_RXN	R9	VSS
AG23	LED_DATA	R11	VDD
AG24	IR_IN	R12	VSS
AG25	SIM0_DATA	R13	VSS
AG26	SIM0_PWREN	R14	VDD
AG27	STANDBY_PWROFF	R15	VDD
AG28	VSS	R16	VSS
AH1	VSS	R17	VSS
AH2	VSS	R18	VSS
AH3	DDR3_DQ28	R19	VDD_CPU
AH4	VSS	R21	VDD_CPU
AH6	VSS	R22	VSS
AH7	DDR3_DQ21	R24	VSS

Position	Pin Name	Position	Pin Name
AH9	DDR3_CLK0_P	R25	USB2_ REXT
AH10	VSS	R26	VSS
AH12	VSS	T1	DDR3_DQS0_N
AH13	DDR3_CS_N_0	T2	DDR3_DQS0_P
AH15	DDR3_ADDR0	T3	VSS
AH16	DDR3_BA0	T4	VSS
AH19	USB3_DM	T5	DDR3_DM1
AH21	USB3_RXP	T6	VSS
AH23	LED_CLK	T7	VDDIO_DDR
AH25	SIM0_DET	T9	AVDD_DDRPLL1
AH26	SIM0_CLK	T11	VDD
AH27	VSS	T12	VSS
AH28	VSS	T13	VSS
B1	FE_LED_ACT	T14	VDD
B2	VSS	T15	VDD
B3	VSS	T16	VSS
B4	AVSS_FE	T17	VSS
B6	FE_RXP	T18	VSS
B8	USB0_DP	T19	VSS
B10	I2S0_WS	T22	AVSS_USB2
B13	SPI_CSN0	T24	AVSS_USB2
B14	VSS	T25	AVSS_USB2
B16	HDMI_TX1N	T26	AVSS_USB2
B18	HDMI_TXCN	T27	USB2_DM
B20	HDMITX_SCL	T28	USB2_DP
B22	SPDIF_OUT	U2	DDR3_DQS1_P
B24	VDAC_IREF	U3	DDR3_DQS1_N
B25	AVSS_VDAC	U4	DDR3_DQ8
B26	VSS	U5	DDR3_DQ10
B27	VSS	U6	VSS
C1	SDIO0_CWPR	U7	VDDIO_DDR

Position	Pin Name	Position	Pin Name
C2	FE_LED_BASE	U9	VSS
C3	VSS	U11	VDD
C4	AVSS_FE	U12	VDD
C5	FE_TXN	U13	VDD
C6	AVSS_FE	U14	VDD
C7	AVSS_FE	U15	VDD
C8	AVSS_USB	U16	VSS
C9	USB1_DM	U17	VSS
C10	AVSS_USB	U18	AVDD11_PLL
C11	I2S0_MCLK	U19	AVDD11_PLL
C12	SLIC_RST	U21	VSS
C13	SPI_SDO	U22	AVSS_USB2
C14	VSS	U24	AVDD33_USB2
C15	HDMI_TX2P	U25	AVSS_USB2
C16	AVSS_HDMITX	U26	NF_RDY0
C17	HDMI_TX0P	V1	DDR3_DQ1
C18	AVSS_HDMITX	V2	VSS
C19	VSS	V3	VSS
C20	VSS	V4	DDR3_DQ12
C21	HDMITX_SDA	V5	VSS
C22	AVSS_ADAC	V6	VSS
C23	ADAC_VOUTR	V7	VDDIO_DDR
C24	AVSS_VDAC	V9	VSS
C25	AVSS_VDAC	V11	VDD
C26	VSS	V12	VDD
C27	I2C0_SDA	V13	VDD
C28	DEM_RST	V14	VDD
D3	SDIO0_CDATA1	V15	VDD
D4	AVSS_FE	V16	VDD
D5	FE_TXP	V17	VSS
D6	AVSS_FE	V18	AVSS_PLL

Position	Pin Name	Position	Pin Name
D7	AVSS_FE	V19	AVSS_PLL
D8	AVSS_USB	V21	AVSS_PLL
D9	USB1_DP	V24	VSS
D10	AVSS_USB	V25	VSS
D11	I2S0_DIN0	V26	NF_CLE
D12	I2S0_BCLK	V27	NF_WEN
D13	SPI_SDI	V28	NF_CSN0
D14	VSS	W1	VSS
D15	HDMI_TX2N	W2	DDR3_DQ7
D16	AVSS_HDMITX	W3	DDR3_DQ3
D17	HDMI_TX0N	W4	DDR3_DQ14
D18	AVSS_HDMITX	W5	VSS
D19	VSS	W6	VSS
D20	VSS	W7	VDDIO_DDR
D21	HDMITX_HOTPLUG	W9	VDDIO_DDR
D22	AVSS_ADAC	W21	AVDD33_PLL
D23	ADAC_VOUTL	W22	AVSS_PLL
D24	AVSS_VDAC	W24	VSS
D25	AVSS_VDAC	W25	NF_REN
D26	I2C0_SCL	W26	NF_ALE
E1	SDIO0_CCLK_OUT	Y2	VSS
E2	VSS	Y3	DDR3_DQ5
E3	SDIO0_CDATA0	Y4	VSS
E4	VSS	Y5	DDR3_DQ20
E5	AVSS_FE	Y6	VSS
E6	AVDD33_FE	Y7	VDDIO_DDR
E7	AVDD33_FE	Y9	VDDIO_DDR
E8	AVSS_USB	Y10	VSS
E9	AVSS_USB	Y11	VDDIO_CK_DDR
E10	AVDD33_USB01	Y12	VDDIO_CK_DDR
E11	VSS	Y13	VSS

Position	Pin Name	Position	Pin Name
E12	VSS	Y14	AVDD_DDRPLL2
E13	DVDD33	Y15	VSS
E14	DVDD33	Y18	DVDD11_USB3
E15	AVSS_HDMITX	Y19	AVDD11_VP_USB3
E16	AVDD33_HDMITX	Y21	VSS
E17	AVDD33_HDMITX	Y22	AVDD33_PLL
E18	AVSS_HDMITX	Y24	NF_DVDD3318
E19	DVDD33	Y25	VSS
E20	VSS	Y26	EBI_DQ1
E21	VSS	Y27	VSS
E22	AVDD33_ADAC	Y28	EBI_DQ0
E23	AVSS_ADAC	-	-

1.2 Pin Description

1.2.1 Pin Types

Table 1-2 describes the I/O pin types.

Table 1-2 I/O types

I/O	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with a Schmitt trigger
I_{SPD}	Input signal with a Schmitt trigger, internal pull-down
ISPU	Input signal with a Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down

I/O	Description
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with a Schmitt trigger, input pull-up
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with a Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with a Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

1.2.2 ADAC Pins

Table 1-3 describes audio digital-to-analog converter (ADAC) pins.

Table 1-3 ADAC pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
D23	ADAC_VOUTL	O	-	3.3	Audio-left channel output
C23	ADAC_VOUTR	O	-	3.3	Audio-right channel output
G18	ADAC_VREFDAC	I/O	-	3.3	Reference source. This pin connects to a 10 µF external capacitor and a 100 nF ceramic capacitor with low equivalent series resistance (ESR) in parallel. The 100 nF capacitor should be placed as close as possible to this pin.
E22	AVDD33_ADAC	P	-	-	3.3 V ADAC analog power
C22, D22, E23, H18	AVSS_ADAC	G	-	-	ADAC analog GND

1.2.3 HDMI Pins

Table 1-4 describes high-definition multimedia interface (HDMI) pins.

Table 1-4 HDMI pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
G16, H16	AVCC11_HDMITX	P	-	1.1	1.1 V HDMI transmit (TX) analog power
E16, E17	AVDD33_HDMITX	P	-	3.3	3.3 V HDMI TX analog power
C16, C18, D16, D18, E15, E18, G17, H17	AVSS_HDMITX	G	-	-	HDMI TX analog GND
D17	HDMI_TX0N	O	-	3.3	Serial differential signal of channel 0
C17	HDMI_TX0P				
B16	HDMI_TX1N	O	-	3.3	Serial differential signal of channel 1
A16	HDMI_TX1P				
D15	HDMI_TX2N	O	-	3.3	Serial differential signal of channel 2
C15	HDMI_TX2P				
B18	HDMI_TXCN	O	-	3.3	Differential pixel clock
A18	HDMI_TXCP				
A20	HDMITX_CEC	I_S/O_{OD}	4	3.3	Function 0: reserved Function 1: HDMITX_CEC Channel control signal of the HDMI TX interface Function 2: GPIO4_7 General-purpose input/output (GPIO) Function 3: reserved
D21	HDMITX_HOTPLUG	I_S/O	4	3.3/5	Function 0: reserved Function 1: HDMITX_HOTPLUG Hot plug signal of the HDMI TX interface Function 2: GPIO4_6 GPIO Function 3: reserved
B20	HDMITX_SCL	I_S/O_{OD}	4	3.3/5	Function 0: reserved Function 1: HDMITX_SCL

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					I^2C bus clock signal of the HDMI TX interface Function 2: GPIO4_5 GPIO Functions 3 and 4: reserved
C21	HDMITX_SDA	I_S/O_{OD}	4	3.3/5	Function 0: reserved Function 1: HDMITX_SDA I^2C bus data signal of the HDMI TX interface Function 2: GPIO4_4 GPIO Functions 3 and 4: reserved

1.2.4 USB Pins

Table 1-5 describes USB pins.

Table 1-5 USB pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
H11	AVCC11_USB01	P	-	1.1	1.1 V USB analog power
Y19	AVDD11_VP_USB3	P	-	1.1	1.1 V USB 3.0 analog power
AA19	AVDD11_VPTX0_USB3	P	-	1.1	1.1 V USB 3.0 analog power
E10	AVDD33_USB01	P	-	3.3	3.3 V USB 2.0 analog power
U24	AVDD33_USB2	P	-	3.3	3.3 V USB 2.0 analog power
AD20, AD21	AVDD33_USB3	P	-	3.3	3.3 V USB 3.0 analog power
C8, C10, D8, D10, E8, E9, G12, H12	AVSS_USB	G	-	-	USB 2.0 analog GND
T22, T24, T25, T26, U22, U25	AVSS_USB2	G	-	-	USB 2.0 analog GND

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
Y18	DVDD11_USB3	P	-	1.1	1.1 V USB digital power
A27	USB_BOOT	I_{SPU}/O	4	3.3	Function 0: USB_BOOT USB bootstrap enable during booting 0: enabled 1: disabled Function 1: GPIO2_5 GPIO
A8	USB0_DM	I/O	-	0.4/3.3	USB 2.0 differential bus. In high-speed mode, the working voltage of this port is 0 V to 400 mV; in full-speed or low-speed mode, the voltage of this port is 0 V to 3.3 V.
B8	USB0_DP				
C9	USB1_DM	I/O	-	0.4/3.3	USB 2.0 differential bus. In high-speed mode, the working voltage of this port is 0 to 400 mV; in full-speed or low-speed mode, the voltage of this port is 0 to 3.3 V.
D9	USB1_DP				
T27	USB2_DM	I/O	-	0.4/3.3	USB 2.0 differential bus. In high-speed mode, the working voltage of this port is 0 to 400 mV; in full-speed or low-speed mode, the voltage of this port is 0 to 3.3 V.
T28	USB2_DP				
R25	USB2_ REXT	I/O	-	3.3	USB 2.0, connects to an external 135±1% Ω resistor
AH19	USB3_DM	I/O	-	3.3	USB 3.0 differential bus in USB 2.0 mode
AG19	USB3_DP				
AD18	USB3_REXT	I/O	-	3.3	USB 3.0, connects to an external 135 Ω±10% resistor
AG21	USB3_RXN	I/O	-	0.4/3.3	USB 3.0 differential bus in USB 2.0 mode. In high-speed mode, the working voltage of this port is 0 to 400 mV; in full-speed or low-speed mode, the voltage of this port is 0 to 3.3 V.
AH21	USB3_RXP				
AE20	USB3_TXN	I/O	-	1.1.	USB 3.0 TX data differential bus
AF20	USB3_TXP				

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
G11	USBRBIAS	I/O	-	3.3	USB 2.0, connecting to an external 135 Ω±10% resistor

1.2.5 DDR Pins

DDR Power Pins

Table 1-6 describes DDR power pins.

Table 1-6 DDR power pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
N7, N9, P7, P9, R6, R7, T7, U7, V7, W7, W9, Y7, Y9, AA7, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AC5, AC6, AC7, AC8, AC12, AD4, AD5, AD6, AD7, AE4, AE5, AE6	VDDIO_DDR	P	-	1.5	DDR3 interface power
Y11, Y12	VDDIO_CK_DDR	P	-	1.5	DDR3 clock interface power

DDR Signal Pins

Table 1-7 describes DDR signal pins.

Table 1-7 DDR signal pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
T9	AVDD_DDRPLL1	P	-	3.3	DDR3 phase-locked loop (PLL) 3.3 V analog power
Y14	AVDD_DDRPLL2	P	-	3.3	DDR3 PLL 3.3 V analog power
AH15	DDR3_ADDR0	O	-	1.5	DDR3 SDRAM address signal 0
AE11	DDR3_ADDR1	O	-	1.5	DDR3 SDRAM address signal 1
AD15	DDR3_ADDR2	O	-	1.5	DDR3 SDRAM address signal 2
AG15	DDR3_ADDR3	O	-	1.5	DDR3 SDRAM address signal 3

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AD11	DDR3_ADDR4	O	-	1.5	DDR3 SDRAM address signal 4
AE17	DDR3_ADDR5	O	-	1.5	DDR3 SDRAM address signal 5
AF11	DDR3_ADDR6	O	-	1.5	DDR3 SDRAM address signal 6
AF17	DDR3_ADDR7	O	-	1.5	DDR3 SDRAM address signal 7
AG12	DDR3_ADDR8	O	-	1.5	DDR3 SDRAM address signal 8
AF13	DDR3_ADDR9	O	-	1.5	DDR3 SDRAM address signal 9
AE9	DDR3_ADDR10	O	-	1.5	DDR3 SDRAM address signal 10
AE12	DDR3_ADDR11	O	-	1.5	DDR3 SDRAM address signal 11
AG10	DDR3_ADDR12	O	-	1.5	DDR3 SDRAM address signal 12
AE16	DDR3_ADDR13	O	-	1.5	DDR3 SDRAM address signal 13
AF12	DDR3_ADDR14	O	-	1.5	DDR3 SDRAM address signal 14
AD13	DDR3_ADDR15	O	-	1.5	DDR3 SDRAM address signal 15
AH16	DDR3_BA0	O	-	1.5	DDR3 SDRAM BANK address signal 0
AF10	DDR3_BA1	O	-	1.5	DDR3 SDRAM BANK address signal 1
AE13	DDR3_BA2	O	-	1.5	DDR3 SDRAM BANK address signal 2
AE15	DDR3_CAS_N	O	-	1.5	DDR3 SDRAM column address select signal
AH9	DDR3_CLK0_P	O	-	1.5	DDR3 SDRAM differential clock
AF8	DDR3_CLK1_P	O	-	1.5	DDR3 SDRAM differential clock
AG9	DDR3_CLK0_N	O	-	1.5	DDR3 SDRAM differential clock
AG8	DDR3_CLK1_N	O	-	1.5	DDR3 SDRAM differential clock
AD10	DDR3_CKE	O	-	1.5	DDR3 SDRAM clock enable signal
AH13	DDR3_CS_N_0	O	-	1.5	DDR3 SDRAM CS0
R4	DDR3_DM0	I/O	-	1.5	DDR3 SDRAM data mask enable 0, active high

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
T5	DDR3_DM1	I/O	-	1.5	DDR3 SDRAM data mask enable 1, active high
AF1	DDR3_DM2	I/O	-	1.5	DDR3 SDRAM data mask enable 2, active high
AE2	DDR3_DM3	I/O	-	1.5	DDR3 SDRAM data mask enable 3, active high
N4	DDR3_DQ0	I/O	-	1.5	DDR3 SDRAM data line 0
V1	DDR3_DQ1	I/O	-	1.5	DDR3 SDRAM data line 1
N1	DDR3_DQ2	I/O	-	1.5	DDR3 SDRAM data line 2
W3	DDR3_DQ3	I/O	-	1.5	DDR3 SDRAM data line 3
N5	DDR3_DQ4	I/O	-	1.5	DDR3 SDRAM data line 4
Y3	DDR3_DQ5	I/O	-	1.5	DDR3 SDRAM data line 5
N2	DDR3_DQ6	I/O	-	1.5	DDR3 SDRAM data line 6
W2	DDR3_DQ7	I/O	-	1.5	DDR3 SDRAM data line 7
U4	DDR3_DQ8	I/O	-	1.5	DDR3 SDRAM data line 8
R2	DDR3_DQ9	I/O	-	1.5	DDR3 SDRAM data line 9
U5	DDR3_DQ10	I/O	-	1.5	DDR3 SDRAM data line 10
P3	DDR3_DQ11	I/O	-	1.5	DDR3 SDRAM data line 11
V4	DDR3_DQ12	I/O	-	1.5	DDR3 SDRAM data line 12
P4	DDR3_DQ13	I/O	-	1.5	DDR3 SDRAM data line 13
W4	DDR3_DQ14	I/O	-	1.5	DDR3 SDRAM data line 14
P5	DDR3_DQ15	I/O	-	1.5	DDR3 SDRAM data line 15
AA5	DDR3_DQ16	I/O	-	1.5	DDR3 SDRAM data line 16
AF6	DDR3_DQ17	I/O	-	1.5	DDR3 SDRAM data line 17
AA2	DDR3_DQ18	I/O	-	1.5	DDR3 SDRAM data line 18
AG6	DDR3_DQ19	I/O	-	1.5	DDR3 SDRAM data line 19
Y5	DDR3_DQ20	I/O	-	1.5	DDR3 SDRAM data line 20

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AH7	DDR3_DQ21	I/O	-	1.5	DDR3 SDRAM data line 21
AA3	DDR3_DQ22	I/O	-	1.5	DDR3 SDRAM data line 22
AF7	DDR3_DQ23	I/O	-	1.5	DDR3 SDRAM data line 23
AF5	DDR3_DQ24	I/O	-	1.5	DDR3 SDRAM data line 24
AB1	DDR3_DQ25	I/O	-	1.5	DDR3 SDRAM data line 25
AG4	DDR3_DQ26	I/O	-	1.5	DDR3 SDRAM data line 26
AB3	DDR3_DQ27	I/O	-	1.5	DDR3 SDRAM data line 27
AH3	DDR3_DQ28	I/O	-	1.5	DDR3 SDRAM data line 28
AA4	DDR3_DQ29	I/O	-	1.5	DDR3 SDRAM data line 29
AG3	DDR3_DQ30	I/O	-	1.5	DDR3 SDRAM data line 30
AB4	DDR3_DQ31	I/O	-	1.5	DDR3 SDRAM data line 31
T2	DDR3_DQS0_P	I/O	-	1.5	DDR3 DQS strobe signal 0, for controlling DQ[7:0]
U2	DDR3_DQS1_P	I/O	-	1.5	DDR3 DQS strobe signal 1, for controlling DQ[15:8]
AC3	DDR3_DQS2_P	I/O	-	1.5	DDR3 DQS strobe signal 2, for controlling DQ[23:16]
AD1	DDR3_DQS3_P	I/O	-	1.5	DDR3 DQS strobe signal 3, for controlling DQ[31:24]
T1	DDR3_DQS0_N	I/O	-	1.5	DDR3 DQS strobe signal 0, for controlling DQ[7:0]
U3	DDR3_DQS1_N	I/O	-	1.5	DDR3 DQS strobe signal 1, for controlling DQ[15:8]
AC2	DDR3_DQS2_N	I/O	-	1.5	DDR3 DQS strobe signal 2, for controlling DQ[23:16]
AD2	DDR3_DQS3_N	I/O	-	1.5	DDR3 DQS strobe signal 3, for controlling DQ[31:24]
AG16	DDR3_ODT_0	O	-	1.5	On-die termination (ODT) match control signal of the DDR3 SDRAM
AG17	DDR3_RAS_N	O	-	1.5	Row address select signal of the DDR SDRAM

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AG14	DDR3_RESET_N	O	-	1.5	Reset signal of the DDR3 SDRAM, active low
AE14	DDR3_WE_N	O	-	1.5	Write enable signal of the DDR SDRAM, active low
AC17	DDR3_ZQ	O	-	1.5	ZQ calibration signal of the DDR SDRAM

1.2.6 FE Pins

Table 1-8 describes FE pins.

Table 1-8 FE pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
K12	AVDD11_FE	P	-	1.1	FE PHY 1.1 V analog power
E6, E7	AVDD33_FE	P	-	3.3	FE PHY 3.3 V analog power
B4, C4, C6, C7, D4, D6, D7, E5, G8, K11	AVSS_FE	G	-	-	FE PHY analog GND
B1	FE_LED_ACT	I/O_{OD}	4	3.3	Function 0: reserved Function 1: FE_LED_ACT Ethernet port link status indicator The LED controlled by this signal blinks quickly when the interval between transmitted data packets is short, and it blinks slowly when the interval is long. Configurable OD or CMOS output, OD output by default Function 2: GPIO2_1 GPIO
C2	FE_LED_BASE	I/O_{OD}	4	3.3	Function 0: GPIO2_2 GPIO Function 1: FE_LED_BASE Ethernet port link status indicator 0: linked

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					1: not linked Configurable OD or CMOS output, OD output by default
G9	FE_REXT	I/O	-	3.3	Internal reference voltage. This pin needs to connect to an external 10 kΩ±1% pull-down resistor.
A6	FE_RXN	I	-	3.3	Differential RX signals, adaptive polarity
B6	FE_RXP				
C5	FE_TXN	O	-	3.3	Differential TX signals, adaptive polarity
D5	FE_TXP				

1.2.7 PLL Pins

Table 1-9 describes PLL pins.

Table 1-9 PLL pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
U18, U19	AVDD11_PLL	P	-	1.1	PLL 1.1 V analog power
W21, Y22	AVDD33_PLL	P	-	3.3	PLL 3.3 V analog power
V18, V19, V21, W22	AVSS_PLL	G	-	-	PLL analog GND

1.2.8 VDAC Pins

Table 1-10 describes video digital-to-analog converter (VDAC) pins.

Table 1-10 VDAC pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
F23, F24	AVDD33_ VDAC	P	-	3.3	3.3 V VDAC analog power
B25, C24, C25, D24, D25, E24, G19	AVSS_VD AC	G	-	-	VDAC analog GND

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
A25	VDAC	O	-	3.3	VDAC analog output
B24	VDAC_IREF	I/O	-	3.3	Reference power

1.2.9 EBI Pins

Table 1-11 describes external bus interface (EBI) pins.

Table 1-11 EBI pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
Y28	EBI_DQ0	I/O	8	1.8/3.3	Function 0: EBI_DQ0 NAND flash data bus Function 1: SDIO1_CDATA0 Card data, high level by default
Y26	EBI_DQ1	I/O	8	1.8/3.3	Function 0: EBI_DQ1 NAND flash data bus Function 1: SDIO1_CDATA1 Card data, high level by default
AA26	EBI_DQ2	I/O	8	1.8/3.3	Function 0: EBI_DQ2 NAND flash data bus Function 1: SDIO1_CDATA2 Card data, high level by default
AA25	EBI_DQ3	I/O	8	1.8/3.3	Function 0: EBI_DQ3 NAND flash data bus Function 1: SDIO1_CDATA3 Card data, high level by default
AB28	EBI_DQ4	I/O	8	1.8/3.3	Function 0: EBI_DQ4 NAND flash data bus Function 1: SDIO1_CDATA4 Card data, high level by default
AB26	EBI_DQ5	I/O	8	1.8/3.3	Function 0: EBI_DQ5 NAND flash data bus Function 1: SDIO1_CDATA5 Card data, high level by default
AC26	EBI_DQ6	I/O	8	1.8/3.3	Function 0: EBI_DQ6

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					NAND flash data bus Function 1: SDIO1_CDATA6 Card data, high level by default
AC25	EBI_DQ7	I_{SPU}/ O	8	1.8/3.3	Function 0: EBI_DQ7 NAND flash data bus Function 1: SDIO1_CDATA7 Card data, high level by default Function 2: BOOT_SEL0 Type of the memory from which the system boots, valid only during power-on {BOOT_SEL1,BOOT_SEL0} 00: reserved 01: NAND flash 10: SD 11: eMMC

1.2.10 SYS Pins

Table 1-12 describes system (SYS) pins.

Table 1-12 SYS pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AF26	FUNC_SEL	I_{SPD}	-	3.3/5	Mode select 0: functional mode 1: test mode
A22	MUTE_CTRL	I/O	4	3.3	Function 0: GPIO4_3 GPIO Function 1: MUTE_CTRL Mute control signal
C28	DEM_RST	I/O	4	3.3	Function 0: GPIO1_5 GPIO Function 1: DEM_RST Demod reset signal
AD27	XIN	C_{IN}	-	3.3	Crystal input
AD28	XOUT	C_{OUT}	-	3.3	Crystal output

1.2.11 I²C Pins

Table 1-13 describes inter-integrated circuit (I^2C) pins.

Table 1-13 I^2C pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
D26	I2C0_SCL	I_S/O_{OD}	4	3.3/5	Function 0: GPIO1_6 GPIO Function 1: I2C0_SCL I^2C0 bus clock, OD output
C27	I2C0_SDA	I_S/O_{OD}	4	3.3/5	Function 0: GPIO1_7 GPIO Function 1: I2C0_SDA I^2C0 bus data, OD output
E27	I2C2_SCL	I_S/O_{OD}	4	3.3/5	Function 0: PMC_PWM0 Pulse-width modulation (PWM) output signal 0. For details, see descriptions of PWM in chapter 11 of the *Hi3796M V100 Intelligent Network Terminal Media Processor Data Sheet*. Functions 1, 2, and 3: reserved Function 4: I2C2_SCL I^2C2 bus clock, OD output Function 5: reserved Function 6: GPIO2_6 GPIO
E28	I2C2_SDA	I_S/O_{OD}	4	3.3/5	Function 0: PMC_PWM1 PWM output signal 1. For details, see descriptions of PWM in chapter 11 of the *Hi3796M V100 Intelligent Network Terminal Media Processor Data Sheet*. Function 1: GPIO2_7 GPIO Functions 2 and 3: reserved Function 4: I2C2_SDA I^2C2 bus data/address, OD output

1.2.12 I²S Pins

Table 1-14 describes inter-IC sound (I^2S) pins.

Table 1-14 I^2S pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
D12	I2S0_BCLK	I/O	4	3.3	Function 0: GPIO6_3 GPIO Function 1: I2S0_BCLK Bit stream clock of the I^2S or pulse code modulation (PCM) interface
D11	I2S0_DIN0	I/O	4	3.3	Function 0: GPIO6_7 GPIO Function 1: I2S0_DIN0 Data input of the I^2S or PCM interface
A10	I2S0_DOUT0	I/O	4	3.3	Function 0: GPIO6_5 GPIO Function 1: I2S0_DOUT0 Data output of the I^2S or PCM interface
C11	I2S0_MCLK	I/O	4	3.3	Function 0: GPIO6_6 GPIO Function 1: I2S0_MCLK Main clock of the I^2S or PCM interface. It can act as the working clock of the audio CODEC (low-end DAC).
B10	I2S0_WS	I/O	4	3.3	Function 0: GPIO6_4 GPIO Function 1: I2S0_WS Audio channel select signal at the I^2S RX end (connected to the ADC interface)

1.2.13 IR Pin

Table 1-15 describes the infrared (IR) pin.

Table 1-15 IR pin

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AG24	IR_IN	I_{SPU}	-	3.3/5	Function 0: IR_IN IR input Function 1: GPIO5_1 GPIO

1.2.14 JTAG Pins

Table 1-16 describes Joint Test Action Group (JTAG) pins.

Table 1-16 JTAG pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
F26	JTAG_SEL	I_{SPD}	4	3.3	Multiplexing control indication of JTAG pins 0: The JTAG pins are multiplexed by configuring the pin multiplexing registers. 1: The JTAG pins are always used as JTAG interfaces.
M26	JTAG_TCK	I_{SPD}/O	4	3.3	Function 0: JTAG_TCK JTAG clock input Function 1: reserved Function 2: TSI0_VALID Validity indicator for TSI0 data input, active high Function 5: GPIO0_6 GPIO Function 6: reserved
L28	JTAG_TDI	I_{SPU}/O	4	3.3	Function 0: JTAG_TDI JTAG data input Function 1: reserved Function 2: TSI0_SYNC TSI0 input data sync indicator Function 5: GPIO0_7 GPIO
L27	JTAG_TDO	I/O	4	3.3	Function 0: JTAG_TDO JTAG data output

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: reserved Function 2: TSI1_D7 TSI1 1-bit serial data input Function 5: GPIO2_0 GPIO
N28	JTAG_TMS	I_{SPU}/O	4	3.3	Function 0: JTAG_TMS JTAG mode select input or data output through software trace, controlled by using the CPU Function 1: TSI0_D7 TSI0 1-bit serial input, or 2-bit serial input Function 5: GPIO0_4 GPIO Function 6: reserved
N27	JTAG_TRSTN	I_{SPD}/O	4	3.3	Function 0: JTAG_TRSTN JTAG reset input Function 1: reserved Function 2: TSI0_CLK Clock input of TSI0, maximum 190 MHz in serial mode Function 5: GPIO0_5 GPIO Function 6: reserved

1.2.15 LED Pins

Table 1-17 describes light emitting diode (LED) pins.

Table 1-17 LED pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AH23	LED_CLK	I/O	4	3.3/5	Function 0: GPIO5_6 GPIO Function 1: LED_CLK LED serial output sync clock
AG23	LED_DATA	I/O	4	3.3/5	Function 0: GPIO5_5 GPIO

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: LED_DATA LED serial output data
AF23	LED_KEY0	I/O	4	3.3/5	Function 0: LED_KEY0 Matrix keyboard input 0 Function 1: GPIO5_2 GPIO Function 2: reserved

1.2.16 NANDC Pins

Table 1-18 describes NAND flash controller (NANDC) pins.

Table 1-18 NANDC pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
Y24, AA24, AB24	NF_DVDD3318	P	-	1.8/3.3	1.8 V/3.3 V NAND flash power
W26	NF_ALE	I/O	4	1.8/3.3	Function 0: NF_ALE Address latch signal of the NAND flash Function 1: SDIO1_CARD_POWER_EN Power supply enable control signal, active high Function 2: GPIO0_1 GPIO
V26	NF_CLE	I/O	4	1.8/3.3	Function 0: NF_CLE Command latch signal of the NAND flash Function 1: SDIO1_CWPR Card write protection detection signal, active high Function 2: GPIO0_2 GPIO
V28	NF_CSN0	I_{PU}/O	8	1.8/3.3	Function 0: NF_CSN0 NAND flash CS signal, active low Function 1: SDIO1_CCMD Card command, high level by

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					default
U26	NF_RDY0	I_{SPU}/O	4	1.8/3.3	Function 0: NF_RDY0 Status indicator signal of the NAND flash 1: ready 0: busy Function 1: SDIO1_RST eMMC reset signal
W25	NF_REN	O	8	1.8/3.3	Function 0: NF_REN Read enable signal of the NAND flash, active low Function 1: SDIO1_CCLK_OUT Output working clock for the card
V27	NF_WEN	I/O	4	1.8/3.3	Function 0: NF_WEN Write enable signal of the NAND flash, active low Function 1: SDIO1_CARD_DETECT Card detection signal, active low Function 2: GPIO0_0 GPIO

1.2.17 SDIO Pins

Table 1-19 describes secure digital input/output (SDIO) pins.

Table 1-19 SDIO pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
J2	SDIO0_CARD_DETECT	I/O	4	3.3	Function 0: GPIO3_6 GPIO Function 1: SDIO0_CARD_DETECT Card detection signal, active low
J1	SDIO0_CARD_POWER_EN	I/O	4	3.3	Function 0: GPIO3_7 GPIO Function 1:

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					SDIO0_CARD_POWER_EN Power supply enable control signal, active high, low level by default
E1	SDIO0_CCLK_OUT	I/O	4	3.3	Function 0: GPIO3_2 GPIO Function 1: SDIO0_CCLK_OUT Output working clock for the card
F2	SDIO0_CCMD	I/O	4	3.3	Function 0: GPIO3_3 GPIO Function 1: SDIO0_CCMD Card command, high level by default
E3	SDIO0_CDATA0	I/O	4	3.3	Function 0: GPIO3_1 GPIO Function 1: SDIO0_CDATA0 Card data, high level by default
D3	SDIO0_CDATA1	I/O	4	3.3	Function 0: GPIO3_0 GPIO Function 1: SDIO0_CDATA1 Card data, high level by default
H3	SDIO0_CDATA2	I_S/O_{OD}	4	3.3/5	Function 0: GPIO3_5 GPIO Function 1: SDIO0_CDATA2 Card data, high level by default
G3	SDIO0_CDATA3	I_S/O_{OD}	4	3.3/5	Function 0: GPIO3_4 GPIO Function 1: SDIO0_CDATA3 Card data, high level by default
C1	SDIO0_CWPR	I/O	4	3.3	Function 0: GPIO2_3 GPIO Function 1: SDIO0_CWPR Card write protection detection signal, active high

1.2.18 SIM Pins

Table 1-20 describes SIM pins.

Table 1-20 SIM pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AH26	SIM0_CLK	I/O_{OD}	4	3.3/5	Bidirectional clock signal of the smart card, OD or CMOS
AG25	SIM0_DATA	I_{SPD}/O_{OD}	4	3.3/5	Smart card bidirectional data signal, OD output
AH25	SIM0_DET	I_{SPD}/O	4	3.3/5	Smart card detection signal, active low or active high (default)
AG26	SIM0_PWREN	I/O_{OD}	4	3.3/5	Smart card enable signal, active low or active high (default), OD or CMOS
AF24	SIM0_RST	I/O	4	3.3/5	Smart card reset signal, active low, OD or CMOS

1.2.19 SLIC Pins

Table 1-21 describes subscriber line interface card (SLIC) pins.

Table 1-21 SLIC pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
C12	SLIC_RST	I/O	4	3.3	Function 0: GPIO6_2 GPIO Function 1: SLIC_RST SLIC chip reset signal
B13	SPI_CSN0	I/O	4	3.3	Function 0: GPIO6_0 GPIO Function 1: SPI_CSN0 SPI CS0 output Function 2: UART2_RTSN Modem state output: request to send (RTS), active low. The reset value is 0. Function 3: I2C1_SDA I^2C1 bus data, OD output
A14	SPI_CSN	I/O	4	3.3	Function 0: GPIO6_1

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
	1				GPIO Function 1: SPI_CSN1 SPI CS1 output
A13	SPI_SCLK	I/O	4	3.3/5	Function 0: GPIO0_3 GPIO Function 1: SPI_SCLK SPI clock signal Function 2: UART2_CTSN Modem state input: clear to send (CTS), active low
D13	SPI_SDI	I/O_{OD}	4	3.3/5	Function 0: GPIO4_1 GPIO Function 1: SPI_SDI SPI data input Function 2: UART2_TXD UART2 data TX Function 3: I2C1_SCL I^2C1 bus clock, OD output
C13	SPI_SDO	I/O	4	3.3/5	Function 0: GPIO4_0 GPIO Function 1: SPI_SDO SPI data output Function 2: UART2_RXD UART2 data RX

1.2.20 SPDIF Pin

Table 1-22 describes the Sony/Philips digital interface format (SPDIF) pin.

Table 1-22 SPDIF pin

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
B22	SPDIF_OUT	I_{SPD}/O	4	3.3	Function 0: reserved Function 1: SPDIF_OUT SPDIF data output Function 2: GPIO4_2 GPIO Function 3: BOOT_SEL1

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					Type of the memory from which the system boots, valid only during power-on {BOOT_SEL1, BOOT_SEL0} 00: reserved 01: NAND flash 10: SD 11: eMMC

1.2.21 STANDBY_PWROFF Pin

Table 1-23 describes the STANDBY_PWROFF pin.

Table 1-23 STANDBY_PWROFF pin

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AG27	STANDBY_PWROFF	I/O	-	3.3/5	Function 0: STANDBY_PWROFF Chip power-off control in standby mode Function 1: GPIO5_0 GPIO

1.2.22 TSI Pins

Table 1-24 describes TSI pins.

Table 1-24 TSI pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
G28	TSI0_CLK	I/O	4	3.3	Function 0: GPIO1_3 GPIO Function 1: TSI0_CLK Clock input of TSI0, maximum 190 MHz in serial mode
H26	TSI0_D0	I/O	4	3.3	Function 0: GPIO1_2 GPIO Function 1: TSI0_D0 TSI0 1-bit serial input, or 2-bit

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
					serial input Function 2: TSI1_SYNC TSI1 input data sync indicator
J27	TSI0_D1	I/O	4	3.3	Function 0: GPIO1_1 GPIO Function 1: TSI0_D1 TSI0 2-bit serial data input Function 2: TSI1_VALID Validity indicator for TSI1 data input, active high
K28	GPIO1_0	I/O	4	3.3	Function 0: GPIO1_0 GPIO Function 1: reserved Function 2: TSI1_CLK TSI1 clock input, maximum 190 MHz in serial mode
G27	TSI0_VALID	I/O	4	3.3	Function 0: GPIO1_4 GPIO Function 1: TSI0_VALID Validity indicator for TSI0 data input, active high

1.2.23 UART Pins

Table 1-25 describes Universal asynchronous receiver/transmitter (UART) pins.

Table 1-25 UART pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AF28	UART0_RXD	I/O_{OD}	4	3.3/5	Function 0: UART0_RXD UART0 data RX Function 1: UART1_RXD UART1 data RX
AF27	UART0_TXD	I/O_{OD}	4	3.3/5	Function 0: UART0_TXD UART0 data TX Function 1: UART1_TXD UART1 data TX

1.2.24 PG Pins

DVDD33 Pins

Table 1-26 describes DVDD33 pins.

Table 1-26 DVDD33 pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
E13, E14, E19, G5, H24, K24, L24	DVDD33	P	-	3.3	3.3 V I/O interface power

DVDD11_LDO1_OUT Pin

Table 1-27 describes the DVDD11_LDO1 pin.

Table 1-27 DVDD11_LDO1 pin

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AA21	DVDD11_LDO1_OUT	P	-	1.1	1.1 V core power output from the internal LDO, connecting to an external filter capacitor

DVDD33_STANDBY Pins

Table 1-28 describes DVDD33_STANDBY pins.

Table 1-28 DVDD33_STANDBY pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
AD23, AD24	DVDD33_STANDBY	P	-	3.3	3.3 V standby power

DVDD3318_LDO2_OUT Pins

Table 1-29 describes DVDD3318_LDO2 pins.

Table 1-29 DVDD3318_LDO2 pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
K4, K5	DVDD3318_LDO2_OUT	P	-	3.3/1.8	3.3 V or 1.8 V power output from the internal SDIO_LDO, connecting to external filter capacitors

VDD_CPU Pins

Table 1-30 describes VDD_CPU pins.

Table 1-30 VDD_CPU pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
L21, M19, M21, M22, N18, N19, N22, P18, P19, P22, R19, R21	VDD_CPU	P	-	1.1	CPU core power

VDD Pins

Table 1-31 describes VDD pins.

Table 1-31 VDD pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
K14, K15, K16, K17, L14, L15, M14, M15, N14, N15, P14, P15, R11, R14, R15, T11, T14, T15, U11, U12, U13, U14, U15, V11, V12, V13, V14, V15, V16	VDD	P	-	1.1	1.1 V core voltage

VSS Pins

Table 1-32 describes VSS pins.

Table 1-32 VSS pins

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
A1, A2, A3, A28, B2, B3, B14, B26, B27, C3, C14, C19, C20, C26, D14, D19, D20, E2, E4, E11, E12, E20, E21, E25, E26, F1, F3, F4, F5, F25, G4, G13, G14, G21, G24, G25, G26, H1,	VSS	G	-	-	Digital GND

Position	Pin	Type	Drive Current (mA)	Voltage (V)	Description
H2, H4, H5, H13, H14, H21, H22, H25, J3, J4, J5, J21, J22, J24, J25, J26, K3, K13, K18, K19, K21, K22, K25, K26, K27, L1, L2, L3, L4, L5, L11, L12, L13, L16, L17, L18, L19, L22, L25, L26, M3, M4, M5, M6, M11, M12, M13, M16, M17, M18, M24, M25, N3, N6, N11, N12, N13, N16, N17, N24, N25, N26, P2, P6, P11, P12, P13, P16, P17, P24, P25, P26, R1, R3, R5, R9, R12, R13, R16, R17, R18, R22, R24, R26, T3, T4, T6, T12, T13, T16, T17, T18, T19, U6, U9, U16, U17, U21, V2, V3, V5, V6, V9, V17, V24, V25, W1, W5, W6, W24, Y2, Y4, Y6, Y10, Y13, Y15, Y21, Y25, Y27, AA1, AA6, AA18, AA20, AB2, AB5, AB16, AB25, AB27, AC4, AC9, AC10, AC11, AC13, AC14, AC15, AC16, AC24, AD3, AD8, AD9, AD12, AD14, AD16, AD17, AD19, AD22, AD25, AD26, AE1, AE3, AE7, AE8, AE10, AE18, AE19, AE21, AE22, AE23, AE24, AE25, AE26, AF2, AF3, AF4, AF9, AF14, AF15, AF16, AF18, AF19, AF21, AF22, AF25, AG1, AG2, AG5, AG7, AG11, AG13, AG28, AH1, AH2, AH4, AH6, AH10, AH12, AH27, AH28					

1.3 Register Summary

Table 1-33 describes the pin multiplexing control registers.

Table 1-33 Summary of pin multiplexing control registers (base address: 0xF8A2_1000)

Offset Address	Register	Description	Page
0x000	ioshare_0	Multiplexing control register for the EBI_DQ7 pin	43
0x004	ioshare_1	Multiplexing control register for the EBI_DQ6 pin	44
0x008	ioshare_2	Multiplexing control register for the EBI_DQ5 pin	45
0x00C	ioshare_3	Multiplexing control register for the EBI_DQ4 pin	46
0x010	ioshare_4	Multiplexing control register for the EBI_DQ3 pin	47
0x014	ioshare_5	Multiplexing control register for the EBI_DQ2 pin	49
0x018	ioshare_6	Multiplexing control register for the EBI_DQ1 pin	50
0x01C	ioshare_7	Multiplexing control register for the EBI_DQ0 pin	51
0x020	ioshare_8	Multiplexing control register for the NF_WEN pin	52
0x024	ioshare_9	Multiplexing control register for the NF_ALE pin	53

Offset Address	Register	Description	Page
0x028	ioshare_10	Multiplexing control register for the NF_CLE pin	54
0x02C	ioshare_11	Multiplexing control register for the NF_CSN0 pin	55
0x030	ioshare_12	Multiplexing control register for the NF_REN pin	56
0x034	ioshare_13	Multiplexing control register for the NF_RDY0 pin	58
0x054	ioshare_21	Multiplexing control register for the JTAG_TMS pin	59
0x058	ioshare_22	Multiplexing control register for the JTAG_TRSTN pin	59
0x05C	ioshare_23	Multiplexing control register for the JTAG_TCK pin	60
0x060	ioshare_24	Multiplexing control register for the JTAG_TDI pin	61
0x064	ioshare_25	Multiplexing control register for the JTAG_TDO pin	62
0x068	ioshare_26	Multiplexing control register for the GPIO1_0 pin	63
0x06C	ioshare_27	Multiplexing control register for the TSI0_D1 pin	64
0x070	ioshare_28	Multiplexing control register for the TSI0_D0 pin	65
0x074	ioshare_29	Multiplexing control register for the TSI0_CLK pin	66
0x078	ioshare_30	Multiplexing control register for the TSI0_VALID pin	67
0x07C	ioshare_31	Multiplexing control register for the I2C2_SCL pin	63
0x080	ioshare_32	Multiplexing control register for the I2C2_SDA pin	69
0x090	ioshare_36	Multiplexing control register for the DEM_RST pin	70
0x094	ioshare_37	Multiplexing control register for the I2C0_SCL pin	71
0x098	ioshare_38	Multiplexing control register for the I2C0_SDA pin	72
0x0AC	ioshare_43	Multiplexing control register for the SPDIF_OUT pin	70
0x0B0	ioshare_44	Multiplexing control register for the MUTE_CTRL pin	74
0x0B4	ioshare_45	Multiplexing control register for the HDMITX_SDA pin	75
0x0B8	ioshare_46	Multiplexing control register for the HDMITX_SCL pin	76
0x0BC	ioshare_47	Multiplexing control register for the HDMITX_HOTPLUG pin	77
0x0C0	ioshare_48	Multiplexing control register for the HDMITX_CEC pin	78
0x0D8	ioshare_54	Multiplexing control register for the FE_LED_ACT pin	79
0x0DC	ioshare_55	Multiplexing control register for the FE_LED_BASE pin	80
0x0E0	ioshare_56	Multiplexing control register for the SDIO0_CWPR pin	81
0x0E4	ioshare_57	Multiplexing control register for the SDIO0_CDATA1 pin	82
0x0E8	ioshare_58	Multiplexing control register for the SDIO0_CDATA0 pin	84

Offset Address	Register	Description	Page
0x0EC	ioshare_59	Multiplexing control register for the SDIO0_CCLK_OUT pin	85
0x0F0	ioshare_60	Multiplexing control register for the SDIO0_CCMD pin	86
0x0F4	ioshare_61	Multiplexing control register for the SDIO0_CDATA3 pin	87
0x0F8	ioshare_62	Multiplexing control register for the SDIO0_CDATA2 pin	88
0x0FC	ioshare_63	Multiplexing control register for the SDIO0_CARD_DETECT pin	89
0x100	ioshare_64	Multiplexing control register for the SDIO0_CARD_POWER_EN pin	90
0x138	ioshare_78	Multiplexing control register for the USB_BOOT pin	91
0x13C	ioshare_79	Multiplexing control register for the SPI_SCLK pin	92
0x140	ioshare_80	Multiplexing control register for the SPI_SDO pin	93
0x144	ioshare_81	Multiplexing control register for the SPI_SDI pin	94
0x148	ioshare_82	Multiplexing control register for the SPI_CSN0 pin	95
0x14C	ioshare_83	Multiplexing control register for the SPI_CSN1 pin	95
0x150	ioshare_84	Multiplexing control register for the SLIC_RST pin	96
0x154	ioshare_85	Multiplexing control register for the I2S0_BCLK pin	97
0x158	ioshare_86	Multiplexing control register for the I2S0_WS pin	98
0x15C	ioshare_87	Multiplexing control register for the I2S0_DOUT0 pin	99
0x160	ioshare_88	Multiplexing control register for the I2S0_MCLK pin	100
0x164	ioshare_89	Multiplexing control register for the I2S0_DIN0 pin	101
0x0044	SC_IO_REUSE_SEL	Multiplexing control register for the MCU subsystem pin	102

Note that the base address for SC_IO_REUSE_SEL is 0xF800_0000, which is different from that for other registers.

1.4 Register Description

ioshare_0

ioshare_0 is a multiplexing control register for the EBI_DQ7 pin.

Offset Address	Register Name	Total Reset Value
0x000	ioshare_0	0x00001F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_0_PU	ioctrl_0_DSx			ioctrl_0_SR	reserved						ioshare_0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_0_PU	Pull-up enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_0_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ7 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA7 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_0_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA7 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:2]	-	reserved	Reserved
[1:0]	RW	ioshare_0	Multiplexing control for the EBI_DQ7 pin 00: EBI_DQ7

			01: SDIO1_CDATA7 10: BOOT_SEL0 Other values: reserved

ioshare_1

ioshare_1 is a multiplexing control register for the EBI_DQ6 pin.

Offset Address	Register Name	Total Reset Value
0x004	ioshare_1	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_1_PD	ioctrl_1_DSx			ioctrl_1_SR	reserved							ioshare_1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_1_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_1_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ6 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA6 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_1_SR	Slew rate control enable 0: disabled

			1: enabled When this pin is multiplexed as the SDIO1_CDATA6 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_1	Multiplexing control for the EBI_DQ6 pin 0: EBI_DQ6 1: SDIO1_CDATA6

ioshare_2

ioshare_2 is a multiplexing control register for the EBI_DQ5 pin.

Offset Address	Register Name	Total Reset Value
0x008	ioshare_2	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_2_PD	ioctrl_2_DSx			ioctrl_2_SR	reserved							ioshare_2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_2_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_2_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ5 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA5 function:

			• The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_2_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA5 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_2	Multiplexing control for the EBI_DQ5 pin 0: EBI_DQ5 1: SDIO1_CDATA5

ioshare_3

ioshare_3 is a multiplexing control register for the EBI_DQ4 pin.

Offset Address	Register Name	Total Reset Value
0x00C	ioshare_3	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_3_PD	ioctrl_3_DSx			ioctrl_3_SR	reserved							ioshare_3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_3_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_3_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA

			101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ4 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA4 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_3_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA4 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_3	Multiplexing control for the EBI_DQ4 pin 0: EBI_DQ4 1: SDIO1_CDATA4

ioshare_4

ioshare_4 is a multiplexing control register for the EBI_DQ3 pin.

Offset Address	Register Name	Total Reset Value
0x010	ioshare_4	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_4_PD				ioctrl_4_DSx				ioctrl_4_SR				reserved								ioshare_4	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_4_PD	Pull-down enable 0: disabled 1: enabled

[11:9]	RW	ioctrl_4_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ3 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA3 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_4_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA3 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_4	Multiplexing control for the EBI_DQ3 pin 0: EBI_DQ3 1: SDIO1_CDATA3

ioshare_5

ioshare_5 is a multiplexing control register for the EBI_DQ2 pin.

Offset Address	Register Name	Total Reset Value
0x014	ioshare_5	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_5_PD	ioctrl_5_DSx			ioctrl_5_SR	reserved							ioshare_5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_5_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_5_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ2 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA2 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_5_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA2 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_5	Multiplexing control of the EBI_DQ2 pin 0: EBI_DQ2

			1: SDIO1_CDATA2

ioshare_6

ioshare_6 is a multiplexing control register for the EBI_DQ1 pin.

Offset Address	Register Name	Total Reset Value
0x018	ioshare_6	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_6_PD	ioctrl_6_DSx			ioctrl_6_SR	reserved							ioshare_6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_6_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_6_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ1 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA1 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_6_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA1 function, the value 1 is recommended in 3.3 V mode, and the value 0 is

			recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_6	Multiplexing control for the EBI_DQ1 pin 0: EBI_DQ1 1: SDIO1_CDATA1

ioshare_7

ioshare_7 is a multiplexing control register for the EBI_DQ0 pin

Offset Address	Register Name	Total Reset Value
0x01C	ioshare_7	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_7_PD	ioctrl_7_DSx			ioctrl_7_SR	reserved							ioshare_7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_7_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_7_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_DQ0 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CDATA0 function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode.

			When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_7_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CDATA0 function, the value 1 is recommended in 3.3 V mode, and the value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_7	Multiplexing control for the EBI_DQ0 pin 0: EBI_DQ0 1: SDIO1_CDATA0

ioshare_8

ioshare_8 is a multiplexing control register for the NF_WEN pin.

Offset Address	Register Name	Total Reset Value
0x020	ioshare_8	0x00000500

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_8_PD	reserved	ioctrl_8_DSx		ioctrl_8_SR	reserved							ioshare_8
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_8_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_8_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the NF_WEN function, the value 10 is recommended.

			When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_8_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_8	Multiplexing control for the NF_WEN pin 00: NF_WEN 01: SDIO1_CARD_DETECT 10: GPIO0_0 Other values: reserved

ioshare_9

ioshare_9 is a multiplexing control register for the NF_ALE pin.

Offset Address	Register Name	Total Reset Value
0x024	ioshare_9	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_9_PD	reserved	ioctrl_9_DSx		ioctrl_9_SR	reserved							ioshare_9
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_9_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_9_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the NF_ALE function, the value 10 is recommended. When this pin is multiplexed as other functions, the value 11 is recommended.

[8]	RW	ioctrl_9_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CARD_POWER_EN function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_9	Multiplexing control for the NF_ALE pin 00: NF_ALE 01: SDIO1_CARD_POWER_EN 10: GPIO0_1 Other values: reserved

ioshare_10

ioshare_10 is a multiplexing control register for the NF_CLE pin.

Offset Address	Register Name	Total Reset Value
0x028	ioshare_10	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_10_PD	reserved	ioctrl_10_DSx		ioctrl_10_SR	reserved						ioshare_10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_10_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_10_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA

			When this pin is multiplexed as the NF_CLE function, the value 10 is recommended. When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_10_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CWPR function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_10	Multiplexing control for the NF_CLE pin 00: NF_CLE 01: SDIO1_CWPR 10: GPIO0_2 Other values: reserved

ioshare_11

ioshare_11 is a multiplexing control register for the NF_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x02C	ioshare_11	0x00001F00

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					ioctrl_11_OPU, ioctrl_11_DSx, ioctrl_11_SR	reserved	ioshare_11
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 1 1 1	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_11_OPU	Pull-up enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_11_DSx	Drive control 000: 12 mA 001: 11 mA

			010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_CSN0 function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CCMD function: • The value 110 is recommended in 3.3 V mode. • The value 101 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_11_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CCMD function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_11	Multiplexing control for the NF_CSN0 pin 0: NF_CSN0 1: SDIO1_CCMD

ioshare_12

ioshare_12 is a multiplexing control register for the NF_REN pin.

Offset Address	Register Name	Total Reset Value
0x030	ioshare_12	0x00000D00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_12_PD	ioctrl_12_DSx			ioctrl_12_SR	reserved							ioshare_12
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_12_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_12_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the NF_REN function, the value 110 is recommended. When this pin is multiplexed as the SDIO1_CCLK_OUT function: • The value 101 is recommended in 3.3 V mode. • The value 010 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_12_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO1_CCLK_OUT function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	-	reserved	Reserved
[0]	RW	ioshare_12	Multiplexing control for the NF_REN pin

			0: NF_REN 1: SDIO1_CCLK_OUT

ioshare_13

ioshare_13 is a multiplexing control register for the NF_RDY0 pin.

Offset Address	Register Name	Total Reset Value
0x034	ioshare_13	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_13_OPU	reserved			ioctrl_13_DSx				ioctrl_13_SR				reserved								ioshare_13
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_13_OPU	Pull-up enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_13_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the NF_RDY0 function, the value 10 is recommended. When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_13_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_13	Multiplexing control for the NF_RDY0 pin 0: NF_RDY0 1: SDIO1_RST

ioshare_21

ioshare_21 is a multiplexing control register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x054	ioshare_21	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_21_PU	reserved		ioctrl_21_DSx		ioctrl_21_SR		reserved				ioshare_21			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_21_PU	Pull-up enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_21_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_21_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_21	Multiplexing control for the JTAG_TMS pin 000: JTAG_TMS 001: TSI0_D7 101: GPIO0_4 Other values: reserved

ioshare_22

ioshare_22 is a multiplexing control register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x058	ioshare_22	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_22_PD	reserved	ioctrl_22_DSx		ioctrl_22_SR	reserved				ioshare_22			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_22_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_22_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_22_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_22	Multiplexing control for the JTAG_TRSTN pin 000: JTAG_TRSTN 010: TSI0_CLK 101: GPIO0_5 Other values: reserved

ioshare_23

ioshare_23 is a multiplexing control register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x05C	ioshare_23	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_23_PD	reserved	ioctrl_23_DSx		ioctrl_23_SR	reserved				ioshare_23			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_23_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_23_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_23_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_23	Multiplexing control for the JTAG_TCK pin 000: JTAG_TCK 010: TSI0_VALID 101: GPIO0_6 Other values: reserved

ioshare_24

ioshare_24 is a multiplexing control register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x060	ioshare_24	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_24_PU	reserved	ioctrl_24_DSx		ioctrl_24_SR	reserved				ioshare_24			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_24_PU	Pull-up enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_24_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_24_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_24	Multiplexing control for the JTAG_TDI pin 000: JTAG_TDI 010: TSI0_SYNC 101: GPIO0_7 Other values: reserved

ioshare_25

ioshare_25 is a multiplexing control register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x064	ioshare_25	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_25_PD	reserved		ioctrl_25_DSx		ioctrl_25_SR		reserved				ioshare_25			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_25_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_25_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_25_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_25	Multiplexing control for the JTAG_TDO pin 000: JTAG_TDO 010: TSI1_D7 101: GPIO2_0 Other values: reserved

ioshare_26

ioshare_26 is a multiplexing control register for the GPIO1_0 pin.

Offset Address	Register Name	Total Reset Value
0x068	ioshare_26	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_26_PD	reserved		ioctrl_26_DSx		ioctrl_26_SR		reserved				ioshare_26			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_26_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_26_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_26_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_26	Multiplexing control for the GPIO1_0 pin 00: GPIO1_0 10: TSI1_CLK Other values: reserved

ioshare_27

ioshare_27 is a multiplexing control register for the TSI0_D1 pin.

Offset Address	Register Name	Total Reset Value
0x06C	ioshare_27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_27_PD	reserved		ioctrl_27_DSx		ioctrl_27_SR		reserved							ioshare_27		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_27_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_27_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_27_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_27	Multiplexing control for the TSI0_D1 pin 00: GPIO1_1 01: TSI0_D1 10: TSI1_VALID Other values: reserved

ioshare_28

ioshare_28 is a multiplexing control register for the TSI0_D0 pin.

Offset Address	Register Name	Total Reset Value
0x070	ioshare_28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_28_PD	reserved		ioctrl_28_DSx		ioctrl_28_SR		reserved							ioshare_28		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_28_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_28_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_28_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_28	Multiplexing control for the TSI0_D0 pin 00: GPIO1_2 01: TSI0_D0 10: TSI1_SYNC Other values: reserved

ioshare_29

ioshare_29 is a multiplexing control register for the TSI0_CLK pin.

Offset Address	Register Name	Total Reset Value
0x074	ioshare_29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_29_PD	reserved		ioctrl_29_DSx		ioctrl_29_SR		reserved								ioshare_29
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_29_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_29_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_29_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_29	Multiplexing control for the TSI0_CLK pin 0: GPIO1_3 1: TSI0_CLK

ioshare_30

ioshare_30 is a multiplexing control register for the TSI0_VALID pin.

Offset Address	Register Name	Total Reset Value
0x078	ioshare_30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_30_PD	reserved		ioctrl_30_DSx		ioctrl_30_SR		reserved							ioshare_30
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_30_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_30_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_30_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_30	Multiplexing control for the TSI0_VALID pin 0: GPIO1_4 1: TSI0_VALID

ioshare_31

ioshare_31 is a multiplexing control register for the I2C2_SCL pin.

Offset Address	Register Name	Total Reset Value
0x07C	ioshare_31	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_31_PD	reserved	ioctrl_31_DSx		ioctrl_31_SR	reserved				ioshare_31			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_31_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_31_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_31_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_31	Multiplexing control for the I2C2_SCL pin 000: PMC_PWM0 100: I2C2_SCL 110: GPIO2_6 Other values: reserved

ioshare_32

ioshare_32 is a multiplexing control register for the I2C2_SDA pin.

Offset Address	Register Name	Total Reset Value
0x080	ioshare_32	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_32_PD	reserved	ioctrl_32_DSx		ioctrl_32_SR	reserved				ioshare_32			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_32_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_32_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_32_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_32	Multiplexing control for the I2C2_SDA pin 000: PMC_PWM1 001: GPIO2_7 100: I2C2_SDA Other values: reserved

ioshare_36

ioshare_36 is a multiplexing control register for the DEM_RST pin.

Offset Address	Register Name	Total Reset Value
0x090	ioshare_36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_36_PD	reserved		ioctrl_36_DSx		ioctrl_36_SR		reserved								ioshare_36
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_36_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_36_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_36_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_36	Multiplexing control for the DEM_RST pin 0: GPIO1_5 1: DEM_RST

ioshare_37

ioshare_37 is a multiplexing control register for the I2C0_SCL pin.

Offset Address	Register Name	Total Reset Value
0x094	ioshare_37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_37_PD	reserved		ioctrl_37_DSx		ioctrl_37_SR		reserved							ioshare_37
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_37_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_37_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_37_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_37	Multiplexing control for the I2C0_SCL pin 0: GPIO1_6 1: I2C0_SCL

ioshare_38

ioshare_38 is a multiplexing control register for the I2C0_SDA pin.

Offset Address	Register Name	Total Reset Value
0x098	ioshare_38	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_38_PD	reserved	ioctrl_38_DSx		ioctrl_38_SR	reserved							ioshare_38
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]		reserved	Reserved
[12]	RW	ioctrl_38_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_38_DSx	Drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_38_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_38	Multiplexing control for the I2C0_SDA pin 0: GPIO1_7 1: I2C0_SDA

ioshare_43

ioshare_43 is a multiplexing control register for the SPDIF_OUT pin.

Offset Address	Register Name	Total Reset Value
0x0AC	ioshare_43	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_43_PD	reserved	ioctrl_43_DSx		ioctrl_43_SR	reserved							ioshare_43		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_43_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_43_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_43_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_43	Multiplexing control for the SPDIF_OUT pin 00: reserved 01: SPDIF_OUT 10: GPIO4_2 11: BOOT_SEL1

ioshare_44

Ioshare_44 is a multiplexing control register for the MUTE_CTRL pin.

Offset Address	Register Name	Total Reset Value
0x0B0	ioshare_44	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_44_PD	reserved		ioctrl_44_DSx		ioctrl_44_SR		reserved							ioshare_44
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_44_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_44_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_44_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_44	Multiplexing control for the MUTE_CTRL pin 0: GPIO4_3 1: MUTE_CTRL

ioshare_45

ioshare_45 is a multiplexing control register for the HDMITX_SDA pin.

Offset Address	Register Name	Total Reset Value
0x0B4	ioshare_45	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_45_PD	reserved	ioctrl_45_DSx		ioctrl_45_SR	reserved				ioshare_45			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_45_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_45_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_45_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_45	Multiplexing control for the HDMITX_SDA pin 000: reserved 001: HDMITX_SDA 010: GPIO4_4 Other values: reserved

ioshare_46

ioshare_46 is a multiplexing control register for the HDMITX_SCL pin.

Offset Address	Register Name	Total Reset Value
0x0B8	ioshare_46	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_46_PD	reserved	ioctrl_46_DSx		ioctrl_46_SR	reserved				ioshare_46			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_46_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_46_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_46_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:3]	RW	reserved	Reserved
[2:0]	RW	ioshare_46	Multiplexing control for the HDMITX_SCL pin 001: HDMITX_SCL 010: GPIO4_5 Other values: reserved

ioshare_47

Ioshare_47 is a multiplexing control register for the HDMITX_HOTPLUG pin.

Offset Address	Register Name	Total Reset Value
0x0BC	ioshare_47	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_47_PD	reserved	ioctrl_47_DSx		ioctrl_47_SR	reserved							ioshare_47		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_47_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_47_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_47_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_47	Multiplexing control for the HDMITX_HOTPLUG pin. 01: HDMITX_HOTPLUG 10: GPIO4_6 Other values: reserved

ioshare_48

ioshare_48 is a multiplexing control register for the HDMITX_CEC pin.

Offset Address	Register Name	Total Reset Value
0x0C0	ioshare_48	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_48_PD	reserved	ioctrl_48_DSx		ioctrl_48_SR	reserved							ioshare_48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_48_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_48_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_48_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_48	Multiplexing control for the HDMITX_CEC pin 01: HDMITX_CEC 10: GPIO4_7 Other values: reserved

ioshare_54

ioshare_54 is a multiplexing control register for the FE_LED_ACT pin.

Offset Address	Register Name	Total Reset Value
0x0D8	ioshare_54	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_54_PD	reserved	ioctrl_54_DSx		ioctrl_54_SR	reserved							ioshare_54
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_54_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_54_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_54_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_54	Multiplexing control for the FE_LED_ACT pin 01: FE_LED_ACT 10: GPIO2_1 Other values: reserved

ioshare_55

ioshare_55 is a multiplexing control register for the FE_LED_BASE pin.

Offset Address	Register Name	Total Reset Value
0x0DC	ioshare_55	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_55_PD	reserved	ioctrl_55_DSx		ioctrl_55_SR	reserved							ioshare_55
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_55_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_55_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_55_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_55	Multiplexing control for the FE_LED_BASE pin 0: GPIO2_2 1: FE_LED_BASE

ioshare_56

ioshare_56 is a multiplexing control register for the SDIO0_CWPR pin.

Offset Address	Register Name	Total Reset Value
0x0E0	ioshare_56	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_56_PD	reserved	ioctrl_56_DSx		ioctrl_56_SR	reserved							ioshare_56
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_56_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_56_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_56_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_56	Multiplexing control for the SDIO0_CWPR pin 0: GPIO2_3 1: SDIO0_CWPR

ioshare_57

ioshare_57 is a multiplexing control register for the SDIO0_CDATA1 pin.

Offset Address	Register Name	Total Reset Value
0x0E4	ioshare_57	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_57_PD	ioctrl_57_DSx			ioctrl_57_SR	reserved							ioshare_57
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_57_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_57_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the SDIO0_CDATA1 function: • The value 111 is recommended in 3.3 V mode. • The value 100 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_57_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO0_CDATA1 function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_57	Multiplexing control for the SDIO0_CDATA1 pin 0: GPIO3_0 1: SDIO0_CDATA1

ioshare_58

ioshare_58 is a multiplexing control register for the SDIO0_CDATA0 pin.

Offset Address	Register Name	Total Reset Value
0x0E8	ioshare_58	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_58_PD	ioctrl_58_DSx			ioctrl_58_SR	reserved							ioshare_58
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_58_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_58_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the SDIO0_CDATA0 function: • The value 111 is recommended in 3.3 V mode. • The value 100 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_58_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO0_CDATA0 function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.

[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_58	Multiplexing control for the SDIO0_CDATA0 pin 0: GPIO3_1 1: SDIO0_CDATA0

ioshare_59

ioshare_59 is a multiplexing control register for the SDIO0_CCLK_OUT pin.

Offset Address	Register Name	Total Reset Value
0x0EC	ioshare_59	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_59_PD	ioctrl_59_DSx			ioctrl_59_SR	reserved							ioshare_59
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_59_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_59_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the SDIO0_CCLK_OUT function: • The value 101 is recommended in 3.3 V mode. • The value 011 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_59_SR	Slew rate control enable 0: disabled 1: enabled

			When this pin is multiplexed as the SDIO0_CCLK_OUT function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_59	Multiplexing control for the SDIO0_CCLK_OUT pin 0: GPIO3_2 1: SDIO0_CCLK_OUT

ioshare_60

ioshare_60 is a multiplexing control register for the SDIO0_CCMD pin.

Offset Address	Register Name	Total Reset Value
0x0F0	ioshare_60	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_60_PD	ioctrl_60_DSx			ioctrl_60_SR	reserved							ioshare_60
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_60_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_60_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the SDIO0_CCMD function: • The value 111 is recommended in 3.3 V mode. • The value 100 is recommended in 1.8 V mode.

			When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_60_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO0_CCMD function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_60	Multiplexing control for the SDIO0_CCMD pin 0: GPIO3_3 1: SDIO0_CCMD

ioshare_61

ioshare_61 is a multiplexing control register for the SDIO0_CDATA3 pin.

Offset Address	Register Name	Total Reset Value
0x0F4	ioshare_61	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_61_PD				ioctrl_61_DSx				ioctrl_61_SR				reserved								ioshare_61	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_61_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_61_DSx	Drive control 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA

			110: 2 mA 111: 1 mA When this pin is multiplexed as the SDIO0_CDATA3 function: • The value 111 is recommended in 3.3 V mode. • The value 100 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_61_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO0_CDATA3 function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_61	Multiplexing control for the SDIO0_CDATA3 pin 0: GPIO3_4 1: SDIO0_CDATA3

ioshare_62

ioshare_62 is a multiplexing control register for the SDIO0_CDATA2 pin.

Offset Address	Register Name	Total Reset Value
0x0F8	ioshare_62	0x00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_62_PD	ioctrl_62_DSx			ioctrl_62_SR	reserved							ioshare_62
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_62_PD	Pull-down enable 0: disabled 1: enabled
[11:9]	RW	ioctrl_62_DSx	Drive control 000: 12 mA

			001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA When this pin is multiplexed as the SDIO0_CDATA2 function: • The value 111 is recommended in 3.3 V mode. • The value 100 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 111 is recommended.
[8]	RW	ioctrl_62_SR	Slew rate control enable 0: disabled 1: enabled When this pin is multiplexed as the SDIO0_CDATA2 function: • The value 1 is recommended in 3.3 V mode. • The value 0 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 1 is recommended.
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_62	Multiplexing control for the SDIO0_CDATA2 pin 0: GPIO3_5 1: SDIO0_CDATA2

ioshare_63

ioshare_63 is a multiplexing control register for the SDIO0_CARD_DETECT pin.

Offset Address	Register Name	Total Reset Value
0x0FC	ioshare_63	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_63_PD	reserved	ioctrl_63_DSx		ioctrl_63_SR	reserved							ioshare_63
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved

[12]	RW	ioctrl_63_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_63_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_63_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_63	Multiplexing control for the SDIO0_CARD_DETECT pin 0: GPIO3_6 1: SDIO0_CARD_DETECT

ioshare_64

ioshare_64 is a multiplexing control register for the SDIO0_CARD_POWER_EN pin.

Offset Address	Register Name	Total Reset Value
0x100	ioshare_64	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_64_PD	reserved	ioctrl_64_DSx		ioctrl_64_SR				reserved										ioshare_64
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_64_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_64_DSx	Drive control 00: 4 mA

			01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the SDIO0_CARD_POWER_EN function: • The value 11 is recommended in 3.3 V mode. • The value 10 is recommended in 1.8 V mode. When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_64_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_64	Multiplexing control for the SDIO0_CARD_POWER_EN pin 0: GPIO3_7 1: SDIO0_CARD_POWER_EN

ioshare_78

ioshare_78 is a multiplexing control register for the USB_BOOT pin.

Offset Address	Register Name	Total Reset Value
0x138	ioshare_78	0x00001700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_78_PU	reserved		ioctrl_78_DSx		ioctrl_78_SR		reserved										ioshare_78
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_78_PU	Pull-up enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_78_DSx	Drive control 00: 4 mA 01: 3 mA

			10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_78_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_78	Multiplexing control for the USB_BOOT pin 0: USB_BOOT 1: GPIO2_5

ioshare_79

ioshare_79 is a multiplexing control register for the SPI_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x13C	ioshare_79	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ioctrl_79_PD	reserved	ioctrl_79_DSx		ioctrl_79_SR				reserved								ioshare_79			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_79_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_79_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the SPI_SCLK function, the value 10 is recommended. When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_79_SR	Slew rate control enable 0: disabled

			1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_79	Multiplexing control for the SPI_SCLK pin 00: GPIO0_3 01: SPI_SCLK 10: UART2_CTSN Other values: reserved

ioshare_80

ioshare_80 is a multiplexing control register for the SPI_SDO pin.

Offset Address	Register Name	Total Reset Value
0x140	ioshare_80	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_80_PD	reserved	ioctrl_80_DSx		ioctrl_80_SR	reserved							ioshare_80
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_80_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_80_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_80_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_80	Multiplexing control for the SPI_SDO pin 00: GPIO4_0

			01: SPI_SDO 10: UART2_RXD Other values: reserved

ioshare_81

ioshare_81 is a multiplexing control register for the SPI_SDI pin.

Offset Address	Register Name	Total Reset Value
0x144	ioshare_81	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_81_PD	reserved	ioctrl_81_DSx		ioctrl_81_SR	reserved							ioshare_81
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_81_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_81_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_81_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_81	Multiplexing control for the SPI_SDI pin 00: GPIO4_1 01: SPI_SDI 10: UART2_TXD 11: I2C1_SCL

ioshare_82

ioshare_82 is a multiplexing control register for the SPI_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x148	ioshare_82	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_82_PD	reserved	ioctrl_82_DSx		ioctrl_82_SR	reserved							ioshare_82
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_82_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_82_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_82_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:2]	RW	reserved	Reserved
[1:0]	RW	ioshare_82	Multiplexing control for the SPI_CSN0 pin 00: GPIO6_0 01: SPI_CSN0 10: UART2_RTSN 11: I2C1_SDA

ioshare_83

ioshare_83 is a multiplexing control register for the SPI_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x14C	ioshare_83	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_83_PD	reserved	ioctrl_83_DSx		ioctrl_83_SR	reserved							ioshare_83
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_83_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_83_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_83_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_83	Multiplexing control for the SPI_CSN1 pin 0: GPIO6_1 1: SPI_CSN1

ioshare_84

ioshare_84 is a multiplexing control register for the SLIC_RST pin.

Offset Address	Register Name	Total Reset Value
0x150	ioshare_84	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_84_PD	reserved		ioctrl_84_DSx		ioctrl_84_SR		reserved							ioshare_84
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_84_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_84_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_84_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_84	Multiplexing control for the SLIC_RST pin 0: GPIO6_2 1: SLIC_RST

ioshare_85

ioshare_85 is a multiplexing control register for the I2S0_BCLK pin.

Offset Address	Register Name	Total Reset Value
0x154	ioshare_85	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_85_PD	reserved	ioctrl_85_DSx		ioctrl_85_SR	reserved							ioshare_85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_85_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_85_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the I2S0_BCLK function, the value 10 is recommended. When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_85_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_85	Multiplexing control for the I2S0_BCLK pin 0: GPIO6_3 1: I2S0_BCLK

ioshare_86

ioshare_86 is a multiplexing control register for the I2S0_WS pin.

Offset Address	Register Name	Total Reset Value
0x158	ioshare_86	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_86_PD	reserved	ioctrl_86_DSx		ioctrl_86_SR	reserved							ioshare_86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_86_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_86_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_86_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_86	Multiplexing control for the I2S0_WS pin 0: GPIO6_4 1: I2S0_WS

ioshare_87

ioshare_87 is a multiplexing control register for the I2S0_DOUT0 pin.

Offset Address	Register Name	Total Reset Value
0x15C	ioshare_87	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_87_PD	reserved	ioctrl_87_DSx		ioctrl_87_SR	reserved							ioshare_87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_87_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_87_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_87_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_87	Multiplexing control for the I2S0_DOUT0 pin 0: GPIO6_5 1: I2S0_DOUT0

ioshare_88

ioshare_88 is a multiplexing control register for the I2S0_MCLK pin.

Offset Address	Register Name	Total Reset Value
0x160	ioshare_88	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_88_PD	reserved	ioctrl_88_DSx		ioctrl_88_SR	reserved							ioshare_88
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_88_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_88_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is multiplexed as the I2S0_MCLK function, the value 01 is recommended. When this pin is multiplexed as other functions, the value 11 is recommended.
[8]	RW	ioctrl_88_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_88	Multiplexing control for the I2S0_MCLK pin 0: GPIO6_6 1: I2S0_MCLK

ioshare_89

ioshare_89 is a multiplexing control register for the I2S0_DIN0 pin.

Offset Address	Register Name	Total Reset Value
0x164	ioshare_89	0x00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			ioctrl_89_PD	reserved	ioctrl_89_DSx		ioctrl_89_SR	reserved							ioshare_89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12]	RW	ioctrl_89_PD	Pull-down enable 0: disabled 1: enabled
[11]	RW	reserved	Reserved
[10:9]	RW	ioctrl_89_DSx	Drive control 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA (recommended)
[8]	RW	ioctrl_89_SR	Slew rate control enable 0: disabled 1: enabled (recommended)
[7:1]	RW	reserved	Reserved
[0]	RW	ioshare_89	Multiplexing control for the I2S0_DIN0 pin 0: GPIO6_7 1: I2S0_DIN0

SC_IO_REUSE_SEL

CAUTION

The base address for SC_IO_REUSE_SEL is 0xF800_0000, which is different from that for other registers.

SC_IO_REUSE_SEL is an MCU subsystem pin multiplexing control register.

Offset Address	Register Name	Total Reset Value
0x0044	SC_IO_REUSE_SEL	0x0038_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							sim0_det_padctrl_PD	sim0_data_padctrl_PD	sim0_clk_padctrl_PD	sim0_clk_padctrl_DS		sim0_clk_padctrl_SR	reserved	led_data_padctrl_PD	led_clk_padctrl_PD	reserved		stb_gpio_sel	reserved	ir_gpio_sel	csn0_gpio_sel			reserved		data_gpio_sel	clk_gpio_sel	reserved		uart_txd_gpio_sel	uart_rxd_gpio_sel
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved
[24]	RW	sim0_det_padctrl_PD	SIM0_DET pull-down control enable 0: disabled 1: enabled
[23]	RW	sim0_data_padctrl_PD	SIM0_DATA pull-down control enable 0: disabled 1: enabled
[22]	RW	sim0_clk_padctrl_PD	SIM0_CLK pull-down control enable 0: disabled 1: enabled
[21:20]	RW	sim0_clk_padctrl_DS	SIM0_CLK drive current 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA When this pin is used as the SIM0_CLK function, the value 01 is recommended in OD output mode, and the value 10 is recommended in CMOS output mode. When this pin is used as other functions, the value 11 is recommended.
[19]	RW	sim0_clk_padctrl_SR	SIM0_CLK SR control enable 0: enabled 1: disabled (recommended)
[18]	RW	reserved	Reserved

[17]	RW	led_data_padctrl_PD	LED_DATA pull-down control enable 0: disabled 1: enabled
[16]	RW	led_clk_padctrl_PD	LED_CLK pull-down control enable 0: disabled 1: enabled
[15:14]	RW	reserved	Reserved
[13]	RW	stb_gpio_sel	Multiplexing control for the STANDBY_PWROFF pin 0: STANDBY_PWROFF 1: GPIO5_0
[12:11]	RW	reserved	Reserved
[10]	RW	ir_gpio_sel	Multiplexing control for the IR_IN pin 0: IR_IN 1: GPIO5_1
[9:8]	RW	csn0_gpio_sel	Multiplexing control for the LED_CSN0 pin 00: LED_KEY0 01: GPIO5_2 10: reserved
[7:6]	RW	reserved	Reserved
[5]	RW	data_gpio_sel	Multiplexing control for the LED_DATA pin 0: GPIO5_5 1: LED DATA
[4]	RW	clk_gpio_sel	Multiplexing control for the LED_CLK pin 0: GPIO5_6 1: LED CLK
[3:2]	RW	reserved	Reserved
[1]	RW	uart_txd_gpio_sel	Multiplexing control for the UART0_TXD pin 0: UART0_TXD 1: UART1_TXD
[0]	RW	uart_rxd_gpio_sel	Multiplexing control for the UART0_RXD pin 0: UART0_RXD 1: UART1_RXD

1.5 Software Multiplexed Pins

1.5.1 MEM

Table 1-34 lists the software multiplexed signals of the MEM.

Table 1-34 Software multiplexed signals of the MEM

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
AC25	EBI_DQ7	ioshare_0	EBI_DQ7	SDIO1_CDATA7	BOOT_SEL0
AC26	EBI_DQ6	ioshare_1	EBI_DQ6	SDIO1_CDATA6	-
AB26	EBI_DQ5	ioshare_2	EBI_DQ5	SDIO1_CDATA5	-
AB28	EBI_DQ4	ioshare_3	EBI_DQ4	SDIO1_CDATA4	-
AA25	EBI_DQ3	ioshare_4	EBI_DQ3	SDIO1_CDATA3	-
AA26	EBI_DQ2	ioshare_5	EBI_DQ2	SDIO1_CDATA2	-
Y26	EBI_DQ1	ioshare_6	EBI_DQ1	SDIO1_CDATA1	-
Y28	EBI_DQ0	ioshare_7	EBI_DQ0	SDIO1_CDATA0	-
V27	NF_WEN	ioshare_8	NF_WEN	SDIO1_CARD_DETECT	GPIO0_0
W26	NF_ALE	ioshare_9	NF_ALE	SDIO1_CARD_POWER_EN	GPIO0_1
V26	NF_CLE	ioshare_10	NF_CLE	SDIO1_CWPR	GPIO0_2
V28	NF_CSN0	ioshare_11	NF_CSN0	SDIO1_CCMD	-
W25	NF_REN	ioshare_12	NF_REN	SDIO1_CCLK_OUT	-
U26	NF_RDY0	ioshare_13	NF_RDY0	SDIO1_RST	-

Table 1-35 describes the software multiplexed signals of the MEM.

Table 1-35 Description of the software multiplexed signals of the MEM

Signal	Direction	Description
BOOT_SEL0	I	Type of the memory from which the system boots, valid only during power-on {BOOT_SEL1, BOOT_SEL0} 00: reserved 01: NAND flash 10: SD 11: eMMC

Signal	Direction	Description
EBI_DQ0	I/O	NAND flash data bus
EBI_DQ1	I/O	NAND flash data bus
EBI_DQ2	I/O	NAND flash data bus
EBI_DQ3	I/O	NAND flash data bus
EBI_DQ4	I/O	NAND flash data bus
EBI_DQ5	I/O	NAND flash data bus
EBI_DQ6	I/O	NAND flash data bus
EBI_DQ7	I/O	NAND flash data bus
GPIO0_0	I/O	GPIO
GPIO0_1	I/O	GPIO
GPIO0_2	I/O	GPIO
NF_ALE	O	Address latch signal of the NAND flash
NF_CLE	O	Command latch signal of the NAND flash
NF_CSN0	O	NAND flash CS signal, active low.
NF_RDY0	I	Status indicator of the NAND flash 1: ready 0: busy
NF_REN	O	Read enable signal of the NAND flash, active low
NF_WEN	O	Write enable signal of the NAND flash, active low
SDIO1_CARD_DETECT	I	Card detection signal, active low
SDIO1_CARD_POWER_EN	O	Power supply enable control signal, active high
SDIO1_CCLK_OUT	O	Output working clock for the card
SDIO1_CCMD	I/O	Card command, high level by default
SDIO1_CDATA0	I/O	Card data, high level by default
SDIO1_CDATA1	I/O	Card data, high level by default
SDIO1_CDATA2	I/O	Card data, high level by default
SDIO1_CDATA3	I/O	Card data, high level by default
SDIO1_CDATA4	I/O	Card data, high level by default
SDIO1_CDATA5	I/O	Card data, high level by default

Signal	Direction	Description
SDIO1_CDATA6	I/O	Card data, high level by default
SDIO1_CDATA7	I/O	Card data, high level by default
SDIO1_CWPR	I	Card write protection detection signal, active high
SDIO1_RST	O	eMMC reset signal

1.5.2 JTAG

Table 1-36 lists the software multiplexed signals of the JTAG interface.

Table 1-36 Software multiplexed signals of the JTAG interface

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3	Multiplexing Signal 4
N28	JTAG_TMS	ioshare_21	JTAG_TMS	TSI0_D7	GPIO0_4	PHY_MHL_CLK	-
N27	JTAG_TRSTN	ioshare_22	JTAG_TRSTN	-	TSI0_CLK	GPIO0_5	PHY_ASCLK
M26	JTAG_TCK	ioshare_23	JTAG_TCK	-	TSI0_VALID	GPIO0_6	PCLK_REF
L28	JTAG_TDI	ioshare_24	JTAG_TDI	-	TSI0_SYNC	GPIO0_7	-
L27	JTAG_TDO	ioshare_25	JTAG_TDO	-	TSI1_D7	GPIO2_0	-

Table 1-37 describes the software multiplexed signals of the JTAG interface.

Table 1-37 Description of software multiplexed signals of the JTAG interface

Signal	Direction	Description
GPIO0_4	I/O	GPIO
GPIO0_5	I/O	GPIO
GPIO0_6	I/O	GPIO
GPIO0_7	I/O	GPIO
GPIO2_0	I/O	GPIO
JTAG_TCK	I	JTAG clock input
JTAG_TDI	I	JTAG data input

Signal	Direction	Description
JTAG_TDO	O	JTAG data output
JTAG_TMS	I/O	JTAG mode select input or data output through software trace, which is controlled by using the CPU
JTAG_TRSTN	I	JTAG reset input
PCLK_REF	O	HDMI TX output test signal
PHY_ASCLK	O	HDMI TX output test signal
PHY_MHL_CLK	O	HDMI TX output test signal
TSI0_D7	I	TSI0 1-bit serial input, or 2-bit serial input
TSI1_D7	I	TSI1 1-bit serial data input

1.5.3 TS

Table 1-38 lists the software multiplexed signals of the TSI.

Table 1-38 Software multiplexed signals of the TSI

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
K28	GPIO1_0	ioshare_26	GPIO1_0	-	TSI1_CLK
J27	TSI0_D1	ioshare_27	GPIO1_1	TSI0_D1	TSI1_VALID
H26	TSI0_D0	ioshare_28	GPIO1_2	TSI0_D0	TSI1_SYNC
G28	TSI0_CLK	ioshare_29	GPIO1_3	TSI0_CLK	-
G27	TSI0_VALID	ioshare_30	GPIO1_4	TSI0_VALID	-

Table 1-39 describes the software multiplexed signals of the TSI.

Table 1-39 Description of software multiplexed signals of the TSI

Signal	Direction	Description
DEM_RST	O	Demod reset signal
GPIO1_0	I/O	GPIO
GPIO1_1	I/O	GPIO
GPIO1_2	I/O	GPIO
GPIO1_3	I/O	GPIO

Signal	Direction	Description
GPIO1_4	I/O	GPIO
TSI0_CLK	I	Clock input of TSI0, maximum 190 MHz in serial mode
TSI0_D0	I	TSI0 1-bit serial input, or 2-bit serial input
TSI0_D1	I	TSI0 2-bit serial data input
TSI0_SYNC	I	TSI0 input data sync indicator
TSI0_VALID	I	Validity indicator for TSI0 data input, active high
TSI1_CLK	I	TSI1 clock input, maximum 190 MHz in serial mode
TSI1_D7	I	TSI1 1-bit serial data input
TSI1_SYNC	I	TSI1 input data sync indicator
TSI1_VALID	I	Validity indicator for TSI1 data input, active high

1.5.4 I²C

Table 1-40 lists the software multiplexed signals of the I²C.

Table 1-40 Software multiplexed signals of the I²C

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
E27	I2C2_SCL	ioshare_31	PMC_PWM0	I2C2_SCL	GPIO2_6
E28	I2C2_SDA	ioshare_32	PMC_PWM1	GPIO2_7	I2C2_SDA
D26	I2C0_SCL	ioshare_37	GPIO1_6	I2C0_SCL	-
C27	I2C0_SDA	ioshare_38	GPIO1_7	I2C0_SDA	-

Table 1-41 describes the software multiplexed signals of the I²C.

Table 1-41 Description of the software multiplexed signals of the I²C

Signal	Direction	Description
GPIO1_6	I/O	GPIO
GPIO1_7	I/O	GPIO
GPIO2_6	I/O	GPIO
GPIO2_7	I/O	GPIO
I2C0_SCL	I/O	I²C0 bus clock, OD output

Signal	Direction	Description
I2C0_SDA	I/O	I^2C0 bus data, OD output
I2C2_SCL	I/O	I^2C2 bus clock, OD output
I2C2_SDA	I/O	I^2C2 bus data, OD output
PMC_PWM0	O	PMC_PWM0 output
PMC_PWM1	O	PMC_PWM1 output

1.5.5 Audio

Table 1-42 lists the software multiplexed signals of the audio interface.

Table 1-42 Software multiplexed signals of the audio interface

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3
B22	SPDIF_OUT	ioshare_43	RSA_END	SPDIF_OUT	GPIO4_2	BOOT_SEL1
A22	MUTE_CTRL	ioshare_44	GPIO4_3	MUTE_CTRL	-	-
D12	I2S0_BCLK	ioshare_85	GPIO6_3	I2S0_BCLK	-	-
B10	I2S0_WS	ioshare_86	GPIO6_4	I2S0_WS	-	-
A10	I2S0_DOUT0	ioshare_87	GPIO6_5	I2S0_DOUT0	-	-
C11	I2S0_MCLK	ioshare_88	GPIO6_6	I2S0_MCLK	-	-
D11	I2S0_DIN0	ioshare_89	GPIO6_7	I2S0_DIN0	-	-

Table 1-43 describes the software multiplexed signals of the audio interface.

Table 1-43 Description of software multiplexed signals of the audio interface

Signal	Direction	Description
BOOT_SEL1	I	Type of the memory from which the system boots, valid only during power-on {BOOT_SEL1, BOOT_SEL0} 00: reserved

Signal	Direction	Description
		01: NAND flash 10: SD 11: eMMC
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO
GPIO6_3	I/O	GPIO
GPIO6_4	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO6_7	I/O	GPIO
I2S0_BCLK	I/O	Bit stream clock of the I^2S or PCM interface
I2S0_DIN0	I	Data input of the I^2S or PCM interface
I2S0_DOUT0	O	Data output of the I^2S or PCM interface
I2S0_MCLK	O	Main clock of the I^2S or PCM interface. It can act as the working clock of the audio CODEC (low-end DAC).
I2S0_WS	I/O	Audio channel select signal at the I^2S RX end (connected to the ADC interface)
MUTE_CTRL	O	Mute control signal
RSA_END	O	Whether the RSA signature authentication of the CA debugging output interface is complete 0: no 1: yes
SPDIF_OUT	O	SPDIF data output

1.5.6 HDMI TX

Table 1-44 lists the software multiplexed signals of the HDMI TX interface.

Table 1-44 Software multiplexed signals of the HDMI TX interface

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
C21	HDMITX_SDA	ioshare_45	-	HDMITX_SDA	GPIO4_4
B20	HDMITX_SCL	ioshare_46	-	HDMITX_SCL	GPIO4_5

D21	HDMITX_HOT PLUG	ioshare_47	-	HDMITX_HOTPLU G	GPIO4_6
A20	HDMITX_CEC	ioshare_48	-	HDMITX_CEC	GPIO4_7

Table 1-45 describes the software multiplexed signals of the HDMI TX interface.

Table 1-45 Description of software multiplexed signals of the HDMI TX interface

Signal	Direction	Description
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO
HDMITX_CEC	I/O	Channel control signal of the HDMI TX interface
HDMITX_HOTPLUG	I	Hot plug signal of the HDMI TX interface
HDMITX_SCL	I/O	I^2C bus clock of the HDMI TX interface
HDMITX_SDA	I/O	I^2C bus data of the HDMI TX interface

1.5.7 NET

Table 1-46 lists the software multiplexed signals of the Ethernet port.

Table 1-46 Software multiplexed signals of the Ethernet port

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2
B1	FE_LED_A CT	ioshare_54	-	FE_LED_ACT	GPIO2_1
C2	FE_LED_B ASE	ioshare_55	GPIO2_2	FE_LED_BASE	-

Table 1-47 describes the software multiplexed signals of the Ethernet port.

Table 1-47 Description of the software multiplexing signals of the Ethernet port

Signal	Direction	Description
FE_LED_ACT	O	Ethernet port link status indicator 1: linked

Signal	Direction	Description
		0: not linked The LED controlled by this signal blinks quickly when the interval between transmitted data packets is short, and it blinks slowly when the interval is long. Configurable OD or CMOS output, OD output by default
FE_LED_BASE	O	Ethernet port link status indicator 1: linked 0: not linked Configurable OD or CMOS output, OD output by default
GPIO2_1	I/O	GPIO
GPIO2_2	I/O	GPIO

1.5.8 SDIO

Table 1-48 lists the software multiplexed signals of the SDIO interface.

Table 1-48 Software multiplexed signals of the SDIO interface

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
C1	SDIO0_CWPR	ioshare_56	GPIO2_3	SDIO0_CWPR
D3	SDIO0_CDATA1	ioshare_57	GPIO3_0	SDIO0_CDATA1
E3	SDIO0_CDATA0	ioshare_58	GPIO3_1	SDIO0_CDATA0
E1	SDIO0_CCLK_OUT	ioshare_59	GPIO3_2	SDIO0_CCLK_OUT
F2	SDIO0_CCMD	ioshare_60	GPIO3_3	SDIO0_CCMD
G3	SDIO0_CDATA3	ioshare_61	GPIO3_4	SDIO0_CDATA3
H3	SDIO0_CDATA2	ioshare_62	GPIO3_5	SDIO0_CDATA2
J2	SDIO0_CARD_DETECT	ioshare_63	GPIO3_6	SDIO0_CARD_DETECT
J1	SDIO0_CARD_POWER_EN	ioshare_64	GPIO3_7	SDIO0_CARD_POWER_EN

Table 1-49 describes the software multiplexed signals of the SDIO interface.

Table 1-49 Description of software multiplexed signals of the SDIO interface

Signal	Direction	Description
GPIO2_3	I/O	GPIO
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO
GPIO3_7	I/O	GPIO
SDIO0_CARD_DETECT	I	Card detection signal, active low
SDIO0_CARD_POWER_EN	O	Power supply enable control signal, active high, low level by default
SDIO0_CCLK_OUT	O	Output working clock for the card
SDIO0_CCMD	I/O	Card command, high level by default
SDIO0_CDATA0	I/O	Card data, high level by default
SDIO0_CDATA1	I/O	Card data, high level by default
SDIO0_CDATA2	I/O	Card data, high level by default
SDIO0_CDATA3	I/O	Card data, high level by default
SDIO0_CWPR	I	Card write protection detection signal, active high

1.5.9 SYS

Table 1-50 lists the software multiplexed signals of SYS.

Table 1-50 Software multiplexed signals of SYS

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1
A27	USB_BOOT	ioshare_78	USB_BOOT	GPIO2_5
C12	SLIC_RST	ioshare_84	GPIO6_2	SLIC_RST
C28	DEM_RST	ioshare_36	GPIO1_5	DEM_RST

Table 1-51 describes the software multiplexed signals of SYS.

Table 1-51 Description of software multiplexed signals of SYS

Signal	Direction	Description
GPIO2_5	I/O	GPIO
GPIO6_2	I/O	GPIO
SLIC_RST	O	SLIC chip reset signal
USB_BOOT	I	USB bootstrap enable during booting 0: enabled 1: disabled

1.5.10 SPI

Table 1-52 lists the software multiplexed signals of the SPI.

Table 1-52 Software multiplexed signals of the SPI

Position	Pad Signal	Multiplexing Control Register	Multiplexing Signal 0	Multiplexing Signal 1	Multiplexing Signal 2	Multiplexing Signal 3
A13	SPI_SCLK	ioshare_79	GPIO0_3	SPI_SCLK	UART2_CTSN	-
C13	SPI_SDO	ioshare_80	GPIO4_0	SPI_SDO	UART2_RXD	-
D13	SPI_SDI	ioshare_81	GPIO4_1	SPI_SDI	UART2_TXD	I2C1_SCL
B13	SPI_CSN0	ioshare_82	GPIO6_0	SPI_CSN0	UART2_RTSN	I2C1_SDA
A14	SPI_CSN1	ioshare_83	GPIO6_1	SPI_CSN1	-	-

Table 1-53 describes the software multiplexed signals of the SPI.

Table 1-53 Description of software multiplexed signals of the SPI

Signal	Direction	Description
GPIO0_3	I/O	GPIO
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO

Signal	Direction	Description
I2C1_SCL	I/O	I^2C1 bus clock, OD output
I2C1_SDA	I/O	I^2C1 bus data, OD output
SPI_CSN0	O	SPI CS0 output
SPI_CSN1	O	SPI CS1 output
SPI_SCLK	O	SPI clock signal
SPI_SDI	I	SPI data input
SPI_SDO	O	SPI data output
UART2_CTSN	I	Modem state input, clear to send (CTS), active low
UART2_RTSN	O	Modem state output, request to send (RTS), active low. The reset value is 0.
UART2_RXD	I	UART2 data RX
UART2_TXD	O	UART2 data TX

2 Electrical Specifications

2.1 Power Consumption

Table 2-1 describes the power consumption parameters.

Table 2-1 Power consumption parameters

Symbol	Description	Min	Typ	Max	Unit
VDD	Core power	TBD	TBD	TBD	mA
VDD_CPU	CPU power	TBD	TBD	TBD	mA
DVDD33	Interface power	TBD	TBD	TBD	mA
VDDIO_DDR	DDR interface power	TBD	TBD	TBD	mA

2.2 Rated Operating Voltages

WARNING

If the maximum rated operating voltages in Table 2-2 are exceeded, the chip may not work stably or be damaged.

Table 2-2 Rated operating conditions

Symbol	Parameter	Min	Max	Unit
VDD	Core power	−0.5	1.8	V
VDD_CPU	CPU power	−0.5	1.8	V

Symbol	Parameter	Min	Max	Unit
DVDD33	Interface power	−0.5	4.6	V
DVDD33_STANDBY	Interface power	−0.5	4.6	V
NF_DVDD3318	Interface power	−0.5	4.6	V
VDDIO_DDR	Interface power	−0.5	4.6	V
VDDIO_CK_DDR	Interface power	−0.5	4.6	V

2.3 Recommended Operating Conditions

Table 2-3 describes the recommended operating conditions.

Table 2-3 Recommended operating conditions

Symbol	Description	Min	Typ	Max	Unit
VDD	Core power	TBD	TBD	TBD	V
VDD_CPU	CPU core power	TBD	TBD	TBD	V
DVDD33	Interface power	3.125	3.3	3.6	V
DVDD33_STANDBY	Interface power of the always-on area	3.125	3.3	3.6	V
NF_DVDD3318	NAND flash interface power	3.125/1.71	3.3/1.8	3.6/1.98	V
VDDIO_DDR	DDR3 interface power	1.425	1.5	1.575	V
VDDIO_CK_DDR	DDR3 clock interface power	1.425	1.5	1.575	V
AVDD_DDRPLL1 AVDD_DDRPLL2	3.3 V DDR3 PLL analog power	3.125	3.3	3.6	V
AVDD11_PLL	1.1 V PLL analog power	1.045	1.1	1.155	V
AVDD33_PLL	3.3 V PLL analog power	3.125	3.3	3.465	V
AVDD33_USB2	3.3 V USB 2.0 analog power	3.125	3.3	3.6	V
AVDD33_VDAC	3.3 V VDAC analog power	3.125	3.3	3.465	V
AVDD33_ADAC	3.3 V ADAC analog power	3.125	3.3	3.465	V
AVCC11_HDMITX	1.1 V HDMI TX analog power	1.045	1.1	1.155	V
AVDD33_USB0	3.3 V USB 2.0 analog	3.125	3.3	3.6	V

Symbol	Description	Min	Typ	Max	Unit
	power				
AVDD33_USB1	3.3 V USB 2.0 analog power	3.125	3.3	3.6	V
AVDD33_FE	3.3 V FE PHY analog power	3.125	3.3	3.465	V
AVDD11_FE	1.1 V FE PHY analog power	1.045	1.1	1.155	V

2.4 DC/AC Electrical Specifications

Table 2-4 describes the direct current (DC) electrical specifications.

Table 2-4 DC electrical specifications (DVDD33 = 3.3 V, some interfaces also support the 5 V input)

Symbol	Parameter	Min	Typ	Max	Unit	Description
DVDD33	Interface voltage	3.125	3.3	3.6	V	-
V_{IH}	High-level input voltage	2.0	-	DVDD33 + 0.3	V	Incompatible with the 5 V input voltage. Some interfaces support the 5 V input voltage, and the maximum input voltage is 5.5 V.
V_{IL}	Low-level input voltage	–0.3	-	0.8	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	2.4	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.4	V	-
R_{PU}	Internal pull-up impedance	27	40	64	kΩ	-
R_{PD}	Internal pull-down impedance	31	46	78	kΩ	-

Symbol	Parameter	Min	Typ	Max	Unit	Description
R_{PU8k}	Pull-up impedance	7.1	8.5	10	kΩ	-
R_{PD8k}	Pull-down impedance	7.1	8.4	10	kΩ	-

Table 2-5 DC electrical specifications (NF_DVDD3318 = 1.8 V)

Symbol	Parameter	Min	Typ	Max	Unit	Description
NF_DVDD3318	Interface voltage	1.71	1.8	1.98	V	1.8 V NAND flash interface
V_{IH}	High-level input voltage	0.65 x NF_DVDD3318	-	NF_DVDD3318 + 0.3	V	
V_{IL}	Low-level input voltage	–0.3	-	0.35 x NF_DVDD3318	V	-
I_L	Input leakage current	-	-	±10	µA	-
I_{OZ}	Tristate output leakage current	-	-	±10	µA	-
V_{OH}	High-level output voltage	NF_DVDD3318 − 0.45 V	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.45	V	-
R_{PU}	Internal pull-up impedance	53	89	163	kΩ	-
R_{PD}	Internal pull-down impedance	54	96	189	kΩ	-
R_{PU8k}	Pull-up impedance	7.4	9	11	kΩ	-
R_{PD8k}	Pull-down impedance	7.1	8.9	11	kΩ	-

Table 2-6 describes the DC electrical specifications in DDR3 mode.

Table 2-6 DC electrical specifications in DDR3 mode (VDDIO_DDR = 1.5 V)

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO_DDR	Interface voltage	1.425	1.5	1.575	V
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	-
VTT	Termination voltage	Vref – 40 mV	Vref	Vref + 40 mV	mV
$V_{IH(DC)}$	High-level input voltage	Vref + 0.1	-	VDDIO_DDR + 0.3	V
$V_{IL(DC)}$	Low-level input voltage	–0.3	-	Vref – 0.1	V
V_{OH}	High-level output voltage	0.8 x VDDIO_DDR	-	(1 + 0.1) x VDDIO_DDR	V
V_{OL}	Low-level output voltage	0	-	0.2 x VDDIO_DDR	V
R_{ON}	Output impedance	34	-	80	Ω

Table 2-7 describes the alternating current (AC) electrical specifications in DDR3 mode.

Table 2-7 AC electrical specifications in DDR3 mode (VDDIO_DDR = 1.5 V)

Symbol	Parameter	Min	Max	Unit
$V_{IH(AC)}$	High-level input voltage	Vref + 0.15	VDDIO_DDR + 0.3	V
$V_{IL(AC)}$	Low-level input voltage	-	Vref – 0.15	V
V_{OH}	High-level output voltage	VTT + 0.1 x VDDIO_DDR	-	V
V_{OL}	Low-level output voltage	-	VTT – 0.1 x VDDIO_DDR	V

2.5 Power-On and Power-Off Sequences

Note the following:

- Turn on the 3V3_Standby, 1.1 V, 3V3_MOS, and 1.5 V power supplies in sequence. The power-on process must be complete within 60 ms.
- Turn off the low voltage power and then the 3.3 V power.

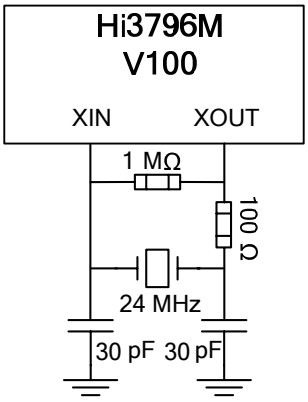
3 Schematic Diagram Design Recommendations

3.1 Small System

3.1.1 Clocking Circuit

The system clock can be generated by combining the internal feedback circuit of Hi3796M V100 with an external 24 MHz crystal oscillator circuit. The frequency deviation of the crystal oscillator must be less than or equal to 30 ppm. Figure 3-1 shows the recommended connection mode of the crystal oscillator.

Figure 3-1 Recommended connection mode of the crystal oscillator



CAUTION

The crystal capacitor must match the external capacitor to GND and the PCB trace capacitor in capacitance.

The system clock can also be generated directly by using the external crystal oscillator clock circuit and input over the XIN pin.

3.1.2 Reset and Watchdog Circuits

Hi3796M V100 integrates a power-on reset (POR) circuit, which internally connects to watchdog signals. No external reset circuit is required.

3.1.3 JTAG Debug Interface

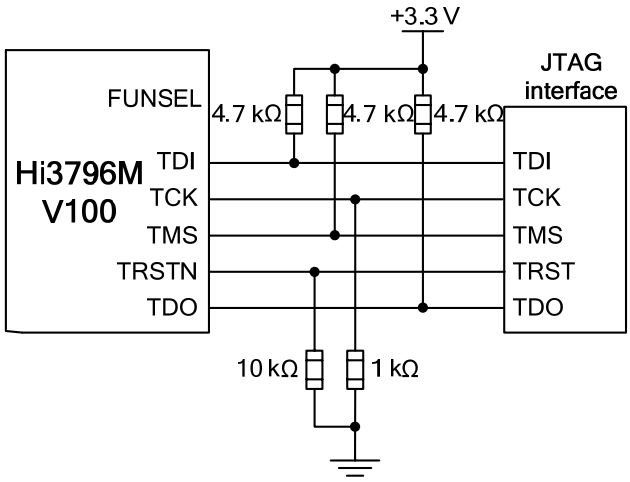
The Hi3796M V100 JTAG interface complies with the IEEE1149.1 standard. PCs can connect to the Realview-ICE simulator over this interface for debugging the chip. Table 3-1 describes the signals of the JTAG debug interface.

Table 3-1 Signals of the JTAG debug interface

Signal	Description
TCK	JTAG clock input, internal pull-down. You are advised to connect this signal to a pull-down resistor on the board.
TDI	JTAG data input, internal pull-up. You are advised to connect this signal to a pull-up resistor on the board.
TMS	JTAG mode select input, internal pull-up. You are advised to connect this signal to a pull-up resistor on the board.
TRSTN	JTAG reset input, internal pull-down. When the chip works properly, you are advised to connect this signal to a pull-down resistor on the board. When the debugging simulators (such as the Realview-ICE) are connected through the JTAG interface, it is recommended that a pull-up resistor be connected on the board.
TDO	JTAG data output. You are advised to connect this signal to a pull-up resistor on the board.

Figure 3-2 shows the JTAG connection mode and standard connector pins.

Figure 3-2 JTAG connection mode and standard connector pins



Hi3796M V100 can work in normal mode or test mode by configuring the FUNC_SEL pin, which is pulled down internally by default. For details, see Table 3-2.

Table 3-2 FUNC_SEL pin configuration

FUNC_SEL	Description
0	Hi3796M V100 works in normal mode. In this case, you can debug the chip over the JTAG interface. This mode is the default mode.
1	Hi3796M V100 works in test mode. In this case, the design for testability (DFT) test or board interconnection test can be performed.

3.1.4 System Configuration Circuit for Hardware Initialization

Hi3796M V100 has an embedded quad-core Cortex A7 CPU and can boot from the NAND flash, SD card, or eMMC. The NAND flash memories with various specifications are supported. The option to boot from the NAND flash, SD card, or eMMC during hardware initialization depends on the signals described in Table 3-3, which are configured by connecting pull-up and pull-down resistors on the board.

Table 3-3 Description of hardware configuration signals

Signal	Direction	Description
JTAG_SEL	I	JTAG pin multiplexing control signal 0: The JTAG pin multiplexing depends on pin multiplexing registers. 1: JTAG pins are multiplexed as the JTAG function, and pin multiplexing registers do not take effect.
BOOTSEL1/BOOTSEL0	I	Type of the memory from which the system boots, valid only during power-on {BOOT_SEL1, BOOT_SEL0} 00: reserved 01: NAND flash 10: SD 11: eMMC

3.1.5 DDR Circuit

3.1.5.1 DDRC Interface

The Hi3796M V100 DDRC supports the DDR3 SDRAM standard interface and the interface level standard is SSTL-15. The DDRC has the following features:

- Provides one DDRC interface, one DDR SDRAM CS, one ODT, and two groups of CKs; supports the 32-bit or 16-bit data bus; supports the 16-bit address bus at the maximum.

- Supports two mainstream 16-bit DDR3 SDRAMs with maximum 1 GB (4 Gbits x 2 = 8 Gbits = 1 GB) capacity, four mainstream 8-bit DDR3 SDRAMs with maximum 2 GB (4 Gbits x 4 = 16 Gbits = 2 GB) capacity, and 800 MHz bus frequency.
- Supports write leveling for the DDR3 SDRAM A/C signal and DDRC CK signal. The A/C signal supports the 2T mode.
- Supports various low-power modes such as the power-down mode and self-refresh mode.
- Supports the DDR3L, that is, supports the 1.35 V voltage for the DDR3L.

3.1.5.2 DDR Topology

Figure 3-3 and Figure 3-4 show the typical topology of connecting Hi3796M V100 to external DDR3 SDRAMs.

Figure 3-3 T-shape topology of connection between Hi3796M V100 and DDR3 SDRAMs

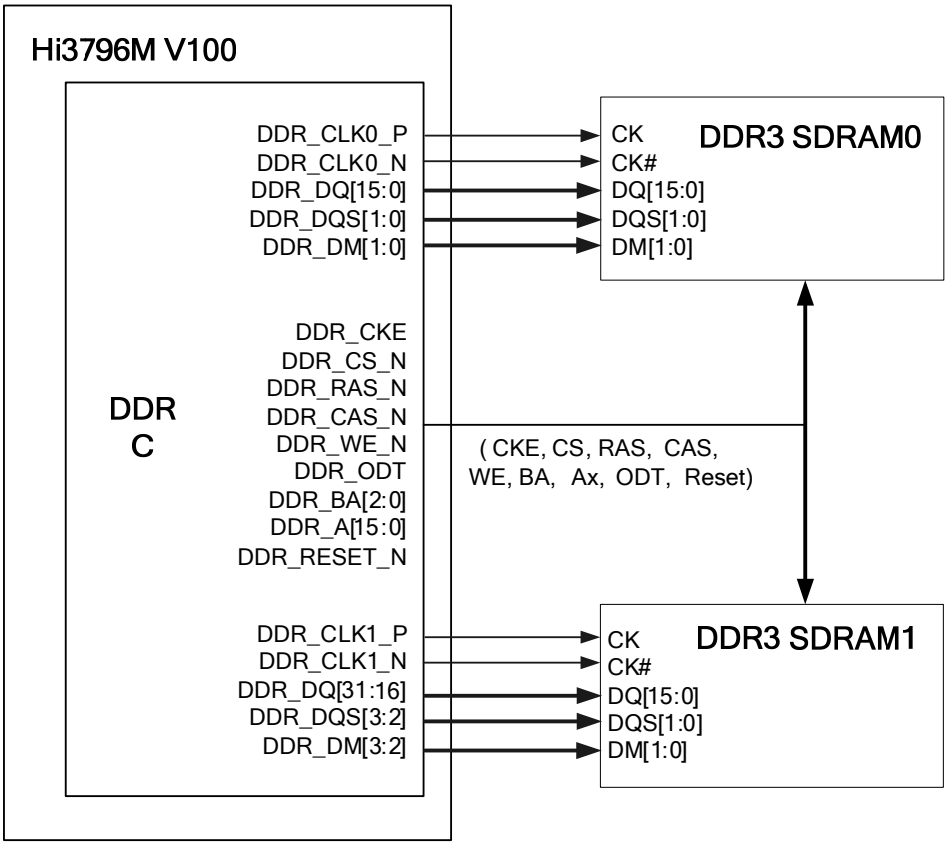
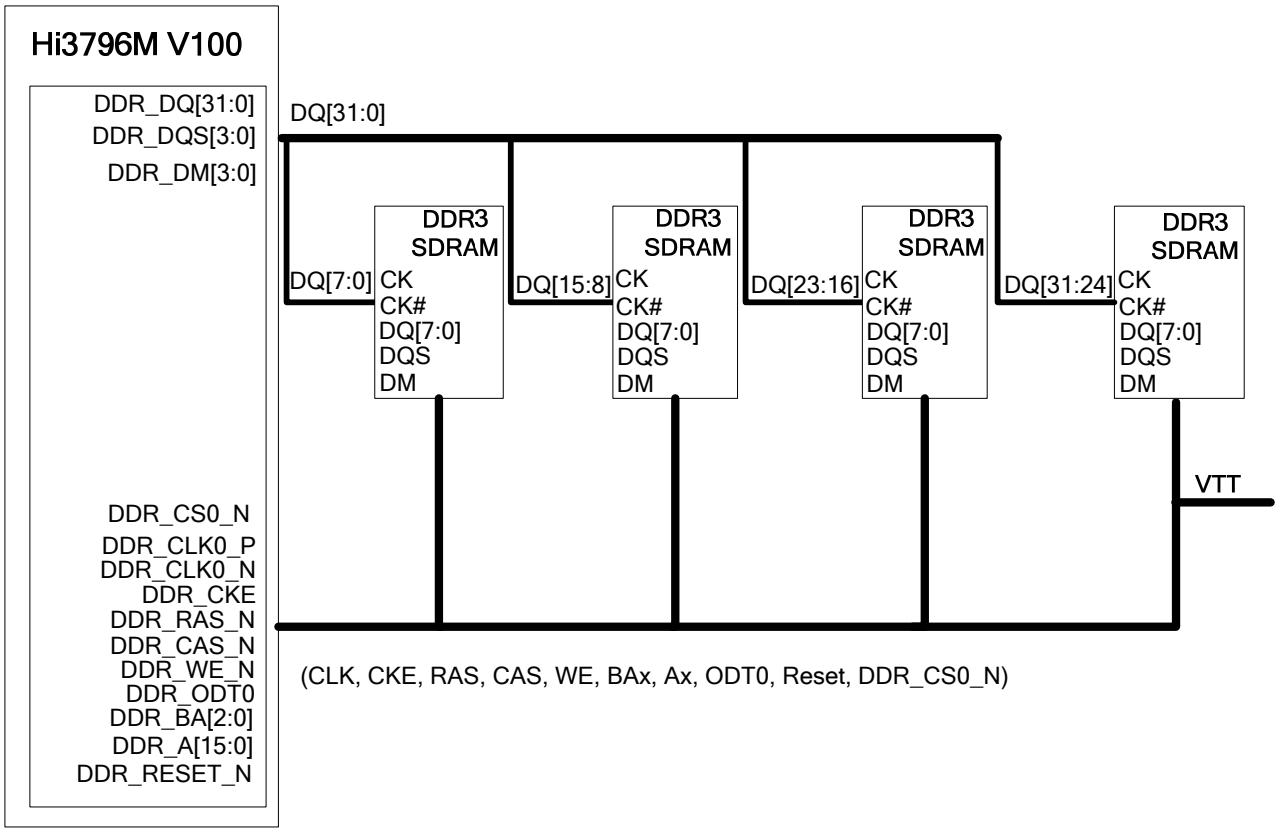


Figure 3-4 Fly-by topology of connection between Hi3796M V100 and DDR3 SDRAMs



3.1.5.3 Design Recommendations for Matched Modes

Bidirectional DQ, DQS, and DM Signals

In the connection between Hi3796M V100 and DDR SDRAMs, the point-to-point topology is used for the DQ, DQS_P/DQS_N, and DM signals. Table 3-4 describes the recommended topology design.

Table 3-4 Recommended topology design for the DQ, DQS_P/DQS_N, and DM signals

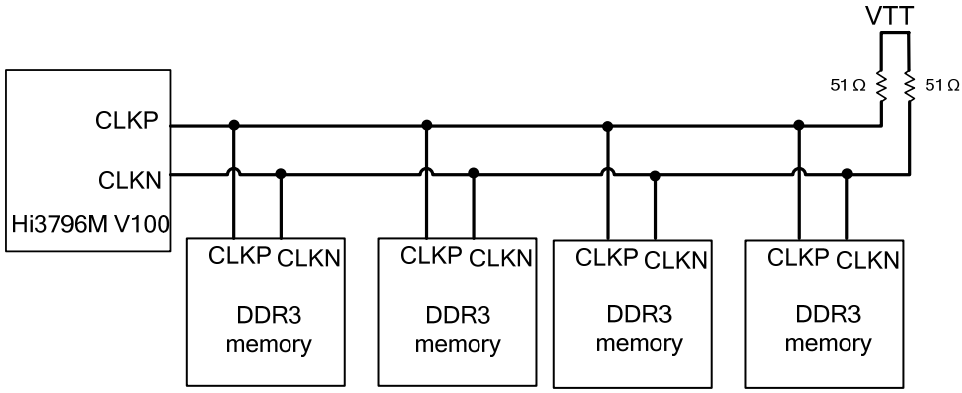
Signal	Connection Mode
DQx	The signal is directly connected.
DQSx_P/N	The signal is directly connected.
DM	The signal is directly connected.

Differential Clocks

In the connection between Hi3796M V100 and DDR SDRAMs, the one-drive-two or one-drive-four topology can be used for the differential signals DDR_CLK_N and DDR_CLK_P.

The 4-layer PCB design uses the one-drive-two or one-drive-four fly-by topology. The VTT power is required for the one-drive-four topology but not the one-drive-two topology. In the one-drive-four topology, one pair of clock signals drives four 8-bit DDRs. Two 51 Ω pull-up resistors are connected at the load end to VTT, as shown in Figure 3-5.

Figure 3-5 One-drive-four fly-by topology for the differential signals DDR_CLK_N and DDR_CLK_P



Address Signals and Control Signals

- In the one-drive-two fly-by topology, the ADDR, ODT, and CSN signals drive two 16-bit DDRs. VTT is not required at the terminal end.
- In the one-drive-four fly-by topology, the ADDR, ODT, and CSN signals drive four 8-bit DDRs. The 51 Ω pull-up resistors are connected at the load end to VTT.

3.1.5.4 Component Selection Recommendations

The maximum working clock frequency for the DDR3 SDRAM of Hi3796M V100 is 800 MHz. The DDR SDRAMs are selected based on the *List of Components Compatible with Hi3796M V100*.

3.1.6 Flash Circuit

3.1.6.1 Interfaces

- The NAND interface connects to an external SLC or MLC NAND flash with maximum 32 GB capacity and supports the 4-bit, 8-bit, 24-bit, 28-bit, 40-bit, or 64-bit ECC mode, randomization, and read retry functions. When the MLC NAND flash is used, a power-off protection circuit for the MLC NAND flash is recommended. For details, see the HiSilicon reference design.
- The SDIO interface connects to an external SD card or eMMC and supports the eMMC 4.41 interface protocol.
- The NAND flash, eMMC, and SD card share a set of pins. Therefore, you can connect the chip to only one type of memory.

3.1.6.2 Signal Processing

NAND Flash Interface

The NAND flash interface supports the 8-bit SLC or MLC NAND flash. Table 3-5 describes the recommended pull-up/-down connection design for the NAND flash interface.

Table 3-5 Recommended pull-up/-down connection design for the NAND flash interface

Signal	Internal Pull-up/Pull-down	Connection Mode
DQ[0:7]	N/A	The signal is directly connected.
NF_RDY/NF_CSN	8 kΩ pull-up	The signal is directly connected.
NF_WEN/NF_REN	N/A	The signal is directly connected.
NF_CLE/NF_ALE	N/A	The signal is directly connected.

eMMC Flash Interface

The eMMC flash interface supports the component that complies with the eMMC 4.41 protocol. Table 3-6 describes the recommended pull-up/-down connection design for the eMMC flash interface.

Table 3-6 Recommended pull-up/-down connection design for the eMMC flash interface

Signal	Internal Pull-up/Pull-down	Connection Mode
SDIO1_CLK	N/A	For the 3.3 V I/O, the signal connects to a 0 Ω resistor in series; for the 1.8 V I/O, the signal connects to a 22 Ω resistor in series.
SDIO1_CMD	N/A	The signal is directly connected. It connects to a 47 kΩ pull-up resistor and then to eMMC_VDD.
SDIO1_DQ[7:0]	N/A	The signal is directly connected. It connects to a 47 kΩ pull-up resistor and then to eMMC_VDD.
SDIO1_CWPR/CCMD_ODPULLUP_EN	N/A	The signal is directly connected.
SDIO1_PWREN_EN/CARD_DETECT	N/A	The signal is directly connected.

SD Card Interface

Table 3-7 describes the recommended pull-up/-down connection design for the SD card interface. The SD card interface supports the SDIO 3.0 1.8 V mode. The LDO is integrated in

the chip. This interface connects to pull-up resistors and then to the LDO for output. For details, see the HiSilicon reference design.

Table 3-7 Recommended pull-up/-down connection design for the SD card interface

Signal	Internal Pull-up/Pull-down	Connection Mode
SDIO1_CLK	N/A	The signal connects to a 22 Ω resistor in series.
SDIO1_CMD	N/A	The signal is directly connected. It connects to a 47 kΩ pull-up resistor and then to SD_VDD.
SDIO1_DQ[3:0]	N/A	The signal is directly connected. It connects to a 47 kΩ pull-up resistor and then to SD_VDD.
SDIO1_CWPR/ CARD_DETECT	N/A	The signal connects to a 47 kΩ pull-up resistor and then to SD_VDD.
SDIO1_PWREN_EN	N/A	The signal is directly connected.

3.2 Power Supply

NOTE

For details about the system power supply design, see the schematic diagram of the Hi3796M V100 demo board.

3.2.1 CPU/Core Power Supply

Hi3796M V100 uses independent CPU and core power supplies (pin name: VDD_CPU and VDD) and supports adaptive voltage scaling (AVS) and dynamic voltage and frequency scaling (DVFS). The CPU and core are supplied by the independent DC-DC/power management unit (PMU). For details about the decoupling circuits of VDD_CPU and VDD, see the schematic diagram of the Hi3796M V100 reference design.

3.2.2 I/O Power Supply

The I/O power pins DVDD33 are connected to the 3.3 V digital power. A 100 nF decoupling capacitor is connected close to the power pin for every two to three DVDD33 pins. For details, see the Hi3796M V100 reference design.

3.2.3 DDR Power Supply

The DDR power supply is designed as follows:

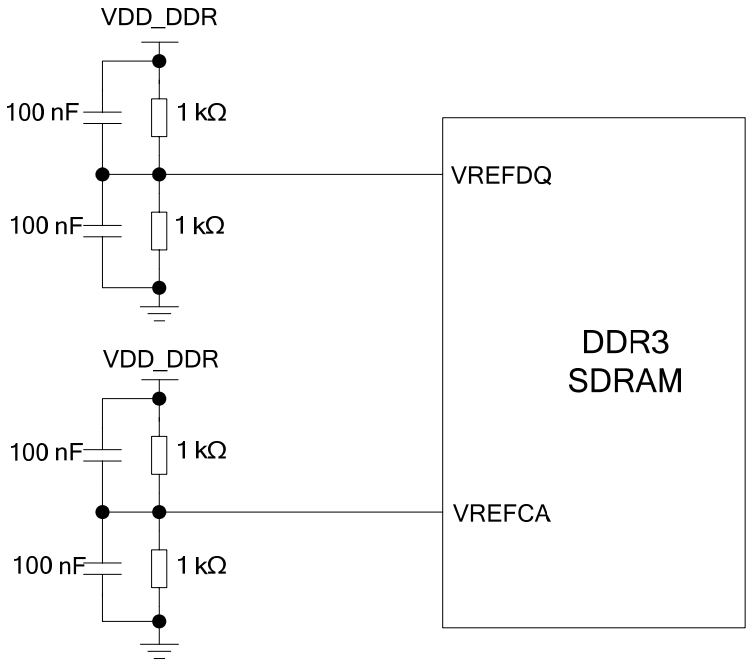
- The Hi3796M V100 DDRC and its interfaces comply with the DDR3 SSTL-15 level standard. The Vref circuit is integrated to generate the reference voltage VDDIO_DDR/2.
- The internal clock of the Hi3796M V100 DDR PHY is generated by an independent PLL. The PLL requires independent power supply (pin name: AVDD_DDRPLL), which is implemented by isolating AVDD_DDRPLL from the 3.3 V digital power using electromagnetic interface (EMI) beads. A 100 nF ceramic filter capacitor is connected

close to each DDR PLL pin, and at least one 1 µF grounded filter capacitor is connected to the DDR PLL power supply. For details, see the Hi3796M V100 reference design.

- The Hi3796M V100 DDR power pins VDDIO_DDR/VDDIO_CK_DDR connect to the DDR digital power. The Hi3796M V100 DDR PHY must use the same power supply design with all connected DDR SDRAMs. A 100 nF ceramic filter capacitor is connected for every one or two power pins close to the power pin, and at least one 10 µF grounded filter capacitor is connected to each DDR power supply. For details, see the Hi3796M V100 reference design.
- You are advised to design an independent DC-DC circuit on the board to supply power to the DDR3 SDRAM and the Hi3796M V100 DDR PHY. The VDDIO_DDR/2 voltage is supplied to the Vref pins of the DDR3 SDRAM by using 1 kΩ±1% voltage divider resistors. A 100 nF decoupling capacitor is connected close to each power pin and reference power pin. Independent Vref circuits are provided for VREFDQ and VREFCA on the DDR SDRAM.

Figure 3-6 shows the reference design of the DDR3 voltage-divider circuit.

Figure 3-6 Reference design of the voltage-divider power supply network



3.2.4 PLL Power Supply

The PLL analog power pins are AVDD33_PLL and AVDD11_PLL, which must be isolated by using EMI beads on the board. Filter capacitors need to be connected close to the pins. For each power supply, a 1 µF capacitor must connect to a 100 nF capacitor in parallel to compose a filtering circuit.

3.2.5 Standby Power Supply

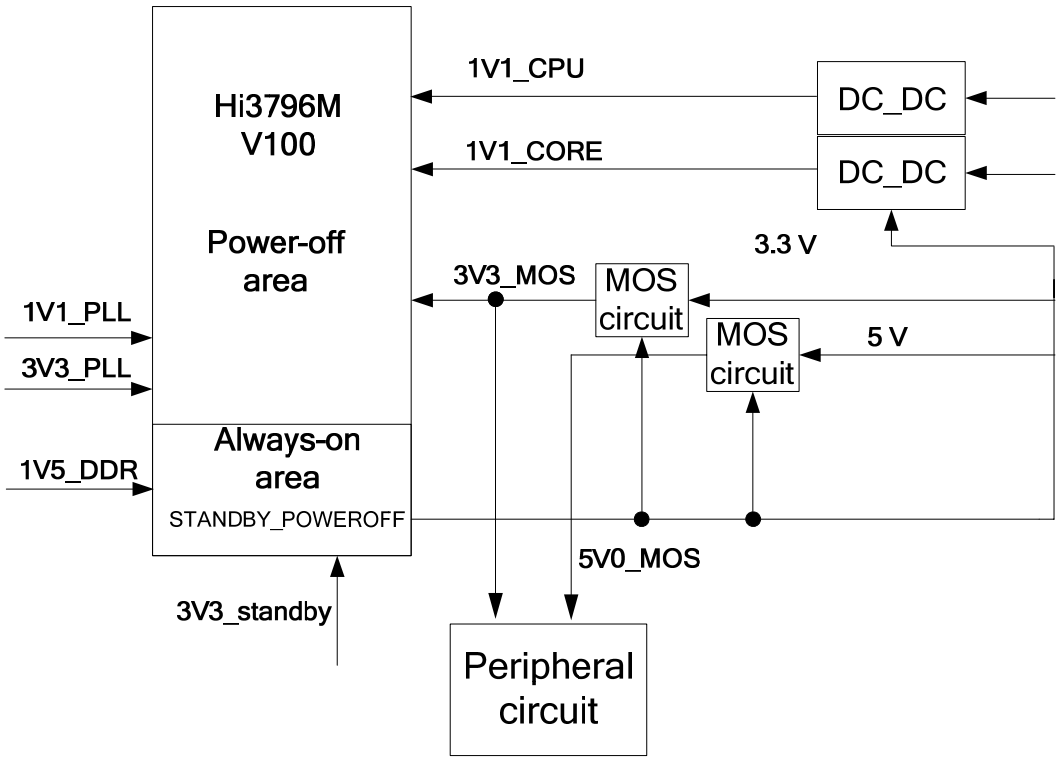
The 3.3 V uninterruptible power is supplied to the DVDD33_STANDBY pin on the board, and the power is not turned off when the system enters the standby mode. Hi3796M V100 integrates a 3.3-to-1.1 V low-dropout (LDO) regulator for supplying the 1.1 V power in

standby mode. You need to connect DVDD11_STANDBY_DECAP to an external 2.2 μF capacitor and then to GND. The filter capacitor must be placed close to the pin.

3.2.6 Standby Circuit

The Hi3796M V100 system uses the passive standby mode. The system is divided into the always-on area and the power-off area. The power supplies of the two areas are independent. As shown in Figure 3-7, the power supply of the always-on area is provided by the power chip, and that of the power-off area is controlled by the STANDBY_PWROFF signal using the MOS. In the passive standby design, the DDR data needs to be saved, and therefore the DDR cannot be powered off. However, the DDR data needs to be cleared and the DDR needs to be powered off during standby in some advanced secure CA design. The HiSilicon reference design, including the design of power consumption data, is based on the passive standby design.

Figure 3-7 Block diagram of the Hi3796M V100 board standby circuit



3.2.7 Precautions

Ensure that the output voltage of each power supply meets the requirements when ripples and noises occur. For details about the power supply requirements of each module, see chapter 2 "Electrical Specifications."

3.3 Peripheral Interfaces

3.3.1 SDIO Interface

Hi3796M V100 provides one SDIO controller that supports the SDIO 3.0 protocol.

- The independent 3.3 V power supply is used, which shares the power supply domain with the 3.3 V I/O.
- The LDO is integrated. The SDIO_DVDD18_DECAP pin connects to an external 2.2 μF filter capacitor and then to GND to provide the 1.8 V I/O level complying with the SDIO 3.0 protocol.

Table 3-8 describes the recommended mode for connecting SDIO signals.

Table 3-8 Recommended mode for connecting SDIO signals

Signal	Connection Mode
SDIO0_CDATA[7:0]	The signal is directly connected. It connects to a 47 kΩ pull-up resistor and then to SDIO DVDD18 DECAP.
SDIO0_CCMD	The signal is directly connected. It connects to a 47 kΩ pull-up resistor and then to SDIO DVDD18 DECAP.
SDIO0_CCLK	For the 3.3 V I/O, the signal is directly connected. For the 1.8 V I/O, the signal connects to a 22 Ω resistor in series at the Hi3796M V100 end.
SDIO0_CARD_POWER_EN	The signal is directly connected.
SDIO0_CARD_DETECT	The signal is directly connected. It connects to a 10 kΩ pull-up resistor and then to 3V3_MOS.
SDIO0_CWPR	The signal is directly connected.

3.3.2 Ethernet Ports

Hi3796M V100 integrates an FE PHY. The design recommendations are as follows:

- The FE_TXN/P and FE_RXN/P signals are routed in differential mode. The differential impedance is 100 Ω±10%. The traces are parallel and have the same length, and the length of the traces on the board is shorter than 5 inches.
- FE_REXT connects to a 10 kΩ±1% pull-down resistor. The trace is as short as possible.
- AVDD33_FE and AVSS_FE are the 3.3 V analog power pin and GND pin. The AVDD33_FE power voltage deviation must fall within ±5%. You are advised to isolate the 3.3 V FE analog power from the 3.3 V board digital power by using EMI beads. In addition, planes are recommended for reducing the parasitic effect, coupling noises, and power supply impedance. Filter capacitors are placed close to AVDD33_FE and AVSS_FE. AVSS_FE can be short-circuited to the common VSS on the board.
- The 1.1 V FE LDO is integrated. AVDD11_FE is the filter pin of the LDO, and it connects to an external 2.2 μF capacitor and then to GND.

It is recommended that a protective circuit for the FE PHY circuit be designed to implement ESD and surge protection. To prevent FE PHY traces from being affected by protective components, you are advised to design the PCB based on the following guidelines:

- Place the protective components between the transformer and PHY close to the transformer.
- Use TVS tubes as protective components. Ensure that the breakdown voltage is 8 kV and the breakdown time is less than 1 ns.

3.3.3 USB Ports

USB Power Supply

Hi3796M V100 integrates three USB 2.0 host ports and one USB 3.0 port. The USB power supply pin is AVDD33_USB01/2, and the GND pin is AVSS_USB, corresponding to the 3.3 V power and GND. The design recommendations are as follows:

- AVDD33_USB and AVSS_USB are respectively the 3.3 V analog power pin and GND pin. The level deviation of AVDD33_USB must be within ±5%. You are advised to isolate the 3.3 V USB analog power and 3.3 V board digital power by using EMI beads. In addition, planes are recommended for reducing the parasitic effect, coupling noise, and power supply impedance. Filter capacitors are placed close to AVDD33_USB and AVSS_USB pins. AVSS_USB can be short-circuited to the common VSS on the board.
- USB2.0_REXT connects to a 135 Ω±1% resistor and then to VSS; USB3.0_REXT connects to a 200 Ω±1% resistor and then to VSS.
- The impedance deviation of each pair of USB differential traces must be 90 Ω±10%, and the spacing between Hi3796M V100 and the connector must be 5 inches or shorter.
- The total capacitance of parallel capacitors that connect to the external VBUS power supply line of a single USB unit must be greater than 100 μF.

USB Protective Circuit

A protective circuit must be designed on the USB circuit to ensure electrostatic discharge (ESD) protection. To prevent USB traces from being affected by protective components, follow the following guidelines:

- Place the protective components close to the USB connector port.
- Use TVS tubes with low parasitic capacitance as protective components. Ensure that the breakdown voltage is 8 kV and the breakdown time is less than 1 ns.
- Ensure that the parasitic capacitors of the protective components are less than 2 pF.

3.3.4 ADAC Interface

- The ADAC power pin AVDD33_ADAC must be isolated from the digital power noises on the board by using EMI beads. A 1 μF filter capacitor is required close to the pin.
- The ADAC_VREFDAC pin must connect to a 2.2 μF capacitor, which is placed close to the pin.

3.3.5 VDAC Interface

VDAC Power Supply

The VDAC analog power supply pins are AVDD11_VDAC and AVDD33_VDAC, and the GND pin is AVSS_VDAC. They must be isolated on the board as follows:

- It is recommended that the analog power AVDD33_VDAC and AVDD11_VDAC be isolated from the board core power and 3.3 V digital power respectively by using EMI beads. The filtering reference plane is the AVSS_VDAC analog video GND. A filter capacitor is placed close to the power pin and AVSS pin.
- The analog video GND plane and the digital GND are combined to use the same GND plane.
- The level deviation of the 1.1 V and 3.3 V analog video power must be within ±5%.

VDAC Interface

Hi3796M V100 provides one VDAC for outputting CVBS signals.

- VDAC_REXT connects to a 12 kΩ±1% resistor and then to AVSS_VDAC.
- The VDAC power pin AVDD33_VDAC must be isolated from noises on the board by using EMI beads, and the level deviation must be within ±5%.

VDAC Protective Circuit

A protective circuit for the VDAC output port is required to implement ESD protection. You are advised to design the PCB based on the following guidelines:

- Place protective components close to the connector of the VDAC output port.
- Use TVS tubes or switch diodes as protective components.

3.3.6 HDMI Interface

Hi3796M V100 provides one HDMI TX interface that supports the HDMI 1.4 protocol.

- The HDMI_TX analog power AVCC11_HDMITX and AVDD33_HDMITX connect to the 1.1 V digital core power and 3.3 V I/O power. EMI beads are required on the board to isolate the HDMI_TX analog power from the digital power noises. Filter capacitors must be placed close to the pins. AVSS connects to digital VSS. Ensure that AVSS is far away from high-frequency noises.
- The four groups of HDMI differential signals must be protected by the ESD components that are placed close to the HDMI. The recommended capacitance is 1 pF or smaller.
- The dedicated I^2C signal for the HDMI supports the 3.3 V or 5 V I/O level.
- Anti-backflow design is required for the HDMI circuit. For details, see the schematic diagram of the Hi3796M V100 demo board.

3.3.7 TSI Interface

Hi3796M V100 supports one parallel TSI or two 1-bit serial TSIs. Table 3-9 describes the recommended pin multiplexing. For details about the design, see the HiSilicon demo board.

Table 3-9 Recommended TSI connection

Pin	One 2-Bit Serial TSI	Two 1-Bit Serial TSI
N28	-	TSI0_D7
N27	-	TSI0_CLK
M26	-	TSI0_VALID
L28	-	GPIO0_7 (DEMOD0_RSTN)
L27	-	TSI1_D7
K28	-	TSI1_CLK
J27	TSI0_D1	TSI1_VALID
H26	TSI0_D0	TSI1_SYNC
G28	TSI0_CLK	GPIO1_3 (DEMOD0_SDA)
G27	TSI0_VALID	GPIO1_4 (DEMOD0_SCL)
C28	DEM_RST	DEM_RST (DEMOD1_RSTN)
D26	I2C0_SCL	I2C0_SCL (DEMOD1_SCL)
C27	I2C0_SDA	I2C0_SDA (DEMOD1_SDA)

3.3.8 SCI Interface

Hi3796M V100 integrates one SCI interface for communicating with the SIM card. This interface supports the 3.3 V and 5 V SIM cards.

- The CLK signal supports the CMOS and OD output modes.
  - In OD output mode, the CLK signal must connect to a 560 Ω pull-up resistor.
  - In CMOS output mode, the CLK signal does not need to connect to a pull-up resistor. However, an external voltage adapter chip such as TDA8024 must be connected when a 5 V SIM card connects to the SCI.
- The DATA signal needs to connect to a 560 Ω pull-up resistor.

4 PCB Design Recommendations

4.1 Stack and Layout

4.1.1 Stack

Hi3796M V100 uses the PBGA-573 package. Its body size is 23 mm x 23 mm (0.91 in. x 0.91 in.), and its ball pitch is 0.8 mm (0.03 in.). You are advised to design a 4-layer PCB with the following stack:

- Top layer: signal traces
- Inner layer 1: GND plane
- Inner layer 2: power plane
- Bottom layer: signal traces

Note the following when designing a 4-layer PCB:

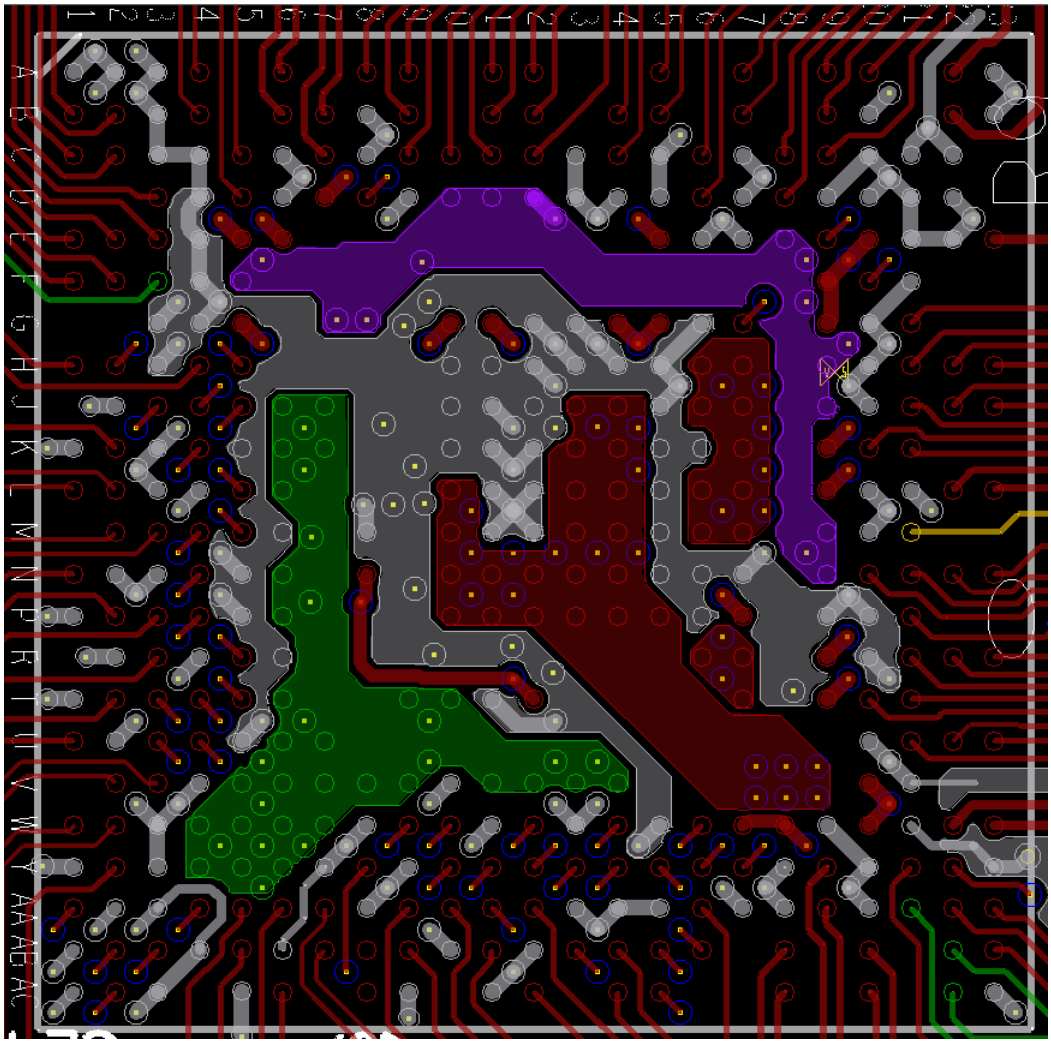
- Place components at the top layer, route signal traces at the top layer and bottom layer, and place filter capacitors with small capacitance at the bottom layer.
- Use wide traces to connect power pins.
- Ensure that inner layer 1 is a complete GND plane.
- The recommended via diameter is 8 mils and the trace width is 5 mils.

The PCB material is FR-4, the PCB thickness is 1.2 mm (0.05 in.), and the copper foil thickness is 1 oz.

4.1.2 Fanout

Figure 4-1 shows the fanout.

Figure 4-1 PBGA-573 fanout



4.2 PCB Design Recommendations for the Small System

4.2.1 Power Supplies for the Small System

Core/CPU Power Supply

You are advised to place the core/CPU power supply near the chip power input area and design power planes on the PCB to shorten the routing traces. Note that the narrowest trace for the core/CPU power must support the flow of 3 A current. It is recommended that a decoupling capacitor connect to every one or two pins and be placed close to the pins, and capacitors with different capacitance be evenly placed. Punch as many vias as possible for power and GND traces to ensure coupling of the top layer, power supply, and GND.

The AVS/DVFS control circuits must be designed according to the Hi3796M V100 reference design. When DC-DC is used, the resistor-capacitor circuit (RC) in the DC-DC adjustment

circuit of VDD_CPU and VDD_CORE needs to be placed near the master chip, and the traces must be surrounded with GND traces.

For details, see the Hi3796M V100 reference design.

DDR Power Supply

The V_{REF} power supplies of the DDR3 SDRAM must be isolated from other power supplies by using 20 mils or wider traces and surrounding the V_{REF} traces with GND traces. In addition, a decoupling capacitor must be connected for every one or two power pins close to the pins. The DDR3 SDRAM power pins VDD and VDDIO must be connected on the same power network as the DDR VDDIO_ DDR power pin of Hi3796M V100. A decoupling capacitor must be connected for every one or two power pins close to the pins, and decoupling capacitors with different capacitance need to be evenly placed.

The design recommendations for the V_{REF} are as follows:

- According to the SSTL-15 standard, the noise of the V_{REF} cannot be greater than ±1% of the V_{REF} level. To reduce the noise, ensure that the V_{REF} traces are as wide as possible. In addition, you are advised to route the V_{REF} traces at the power layer over a copper plane. This copper plane cannot be used as the reference plane for routing signal traces.
- A decoupling capacitor must connect to each V_{REF} pin. The V_{REF} traces must be as wide as possible and 20–25 mils away from other signal traces.

The VTT traces of DDR3 SDRAM must be routed on stripe copper planes close to the DDR3 SDRAM, and capacitors with different capacitance are evenly placed on the copper planes.

For details, see the Hi3796M V100 reference design.

4.2.2 Clock and Reset Circuits

Clock

The Hi3796M V100 PLL power supplies are AVDD11_PLL and AVDD33_PLL, and its GND is AVSS_PLL. You are advised to design the PCB based on the following guidelines:

- AVDD33_PLL is the 3.3 V PLL power supply. You are advised to isolate it from the3.3 V digital power supply on the board by using EMI beads. The level deviation of the 3.3 V power must be within ±5%.
- AVDD11_PLL is the 1.1 V PLL power supply. You are advised to isolate it from the 1.1 V digital power supply by using EMI beads. The level deviation of the 1.1 V power must be within ±5%.
- VSS_PLL is the reference GND of the PLL circuit. The decoupling capacitors of AVDD33_PLL and AVDD11_PLL must use VSS_PLL as the reference GND, and filter capacitors must be placed close to the pins.
- The system clock traces of the crystal oscillator circuit must be 1000 mils or shorter, and be surrounded with GND traces.

Reset

The reset circuit is not required on the board due to embedded POR circuit.

4.2.3 DDR Signals

The Hi3796M V100 DDR supports the maximum frequency of 800 MHz or 1600 MHz. Signal integrity (SI) and power integrity (PI) simulations of the DDR routing are strictly carried out, and DDR routing reference for different application scenarios is provided. You must design the DDR routing by completely following the HiSilicon Hi3796M V100 reference design.

Route DDR traces on a PCB based on the following guidelines:

- All the DDR3 SDRAM signal traces must be routed at the layers close to the GND plane. Do not route the signal traces by crossing the power and GND plane splits. Ensure that the reference planes are complete when routing all the DDR signal traces.
- To ensure a good signal return path and reduce coupling of different reference layers, punch vias around signal traces and changed layers, connect the punched vias to GND, and place capacitors around the vias.
- Ensure that signal traces are as short as possible. Minimize the use of vias to ensure the impedance continuity of traces.
- If resistor networks are used, ensure that the signals from the same resistor network belong to the same DDR signal group. Never route DQS traces and address or control signal traces on the same resistor network.
- Ensure that the spacing between adjacent signal traces is 2–3 times the trace width according to the 3W rule.
- Route clock signal traces far away from the data and address buses.
- Route the address signal traces far away from data signal traces.
- Ensure that DDR3 SDRAM signal traces are surrounded with GND traces and at least 20 mils away from a non-DDR3 signal trace.
- Connect a decoupling capacitor to each V_{REF} pin. Ensure that the trace to each V_{REF} pin is as wide as possible and 20–25 mils away from other signal traces.

4.2.4 Flash Signals

NAND Flash

You are advised to avoid crossing the power and GND plane splits and maintain complete power and GND reference planes when you route signal traces to reduce signal reflection. The impedance of the transmission line must be 50 Ω±10%.

Route the NAND flash signal traces on a PCB based on the following guidelines:

- Route the signal traces at the layers close to the GND plane. Never route signal traces across the power and GND plane splits. Ensure that signal traces have a complete reference GND plane.
- To ensure a smooth signal current return path, punch vias around signal traces and changed layers, and connect the vias to GND.
- Ensure that signal traces are as short as possible, and minimize the use of vias to ensure the impedance continuity of traces.
- Ensure that the spacing between adjacent signal traces is 2–3 times the trace width.
- Ensure that all data signal traces have the same length.

Table 4-1 describes the recommended mode for connecting NAND flash signals.

Table 4-1 Recommended mode for connecting signals of a single NAND flash

Signal	Connection Mode
NF_RDY/NF_CSN/NF_CLE/NF_ALE/DQ[0:7]	The impedance is 50 Ω and the trace must be shorter than 4 inches.
NF_WEN/NF_REN	The impedance is 50 Ω and the trace must be shorter than 2.5 inches.

eMMC Flash/SD

The routing design for eMMC/SD signals is similar to that for NAND flash signals. Table 4-2 describes the recommended mode for connecting eMMC signals.

Table 4-2 Recommended mode for connecting eMMC signals

Signal	Connection Mode
SDIO1_CLK	The impedance is 50 Ω and the trace must be shorter than 4 inches.
SDIO1_CMD	The impedance is 50 Ω and the trace must be shorter than 4 inches.
SDIO1_DQ[7:0]	The impedance is 50 Ω and the trace must be shorter than 4 inches.

4.3 PCB Design Recommendations for Typical Peripheral Interfaces

4.3.1 SDIO Interface

You are advised to avoid crossing the power and GND plane splits and maintain complete power and GND reference planes when you route signal traces to reduce signal reflection. Route SDIO signal traces on a PCB based on the following guidelines:

- Route the signal traces at the layers close to the GND plane. Never route signal traces across the power and GND plane splits. Ensure that signal traces have a complete reference GND plane.
- To ensure a smooth signal current return path, punch vias around signal traces and changed layers, and connect the vias to GND.
- Ensure that signal traces are as short as possible, and minimize the use of vias to ensure the impedance continuity of traces.
- Ensure that the spacing between adjacent signal traces is 2–3 times the trace width.
- Ensure that all data signal traces have the same length.
- Place the 2.2 μF filter capacitor close to the SDIO_DVDD18_DECAP pin.

Table 4-3 describes the recommended mode for connecting SDIO signals.

Table 4-3 Recommended mode for connecting SDIO signals

Signal	Connection Mode
SDIO_CCMD /SDIO_CDATA[0:3]	The impedance is 50 Ω and the trace must be shorter than four inches.
SDIO_CCLK	The impedance is 50 Ω and the trace must be shorter than five inches.

FE PHY

The following requirements must be met to ensure good signal quality:

- The FE PHY data signals FE_TXN/P and FE_RXN/P are routed in differential mode.
- Each pair of differential data traces has the same length and even spacing, and the impedance is 100 Ω±10%.
- The differential traces must be routed far away from clock components such as the clock resonator, clock oscillator, and clock drive.

You are advised to route the FE PHY data signals based on the following guidelines:

- Place the 10 kΩ REXT resistors close to the chip pins.
- Ensure that the differential data traces are short and straight, and each pair of differential traces has the same length.
- Ensure that the width of differential data traces is constant.
- Ensure that the spacing between adjacent differential data traces is constant. Route traces on the routing planes close to the GND plane, and do not change a routing plane.
- Route differential data traces by referencing complete GND planes and do not cross the plane splits. Ensure that differential traces are surrounded with GND traces.
- Minimize the use of vias and corners when routing differential data traces. When corners are required, use arcs or 45° turns rather than a 90° turn, reducing signal reflection and impedance variance.
- Ensure that there is no branch on differential data traces.
- Keep the differential data traces more than 50 mils away from other high-speed periodic signals and strong current signals to reduce crosstalk. Keep the differential data traces at least 20 mils away from low-speed non-periodic signals.

4.3.2 USB Ports

The following requirements must be met to ensure good signal quality:

- The data traces of the USB port are routed in differential mode.
- The differential data traces have the same length and even spacing.
- The impedance deviation of each USB differential trace is 90 Ω ±10%.
- The differential traces are routed far away from clock components such as the clock resonator, clock oscillator, and clock drive.
- Each USB trace must be shorter than or equal to 5 inches.

You are advised to design the PCB routing based on the following guidelines to provide the 480 MHz/s USB 2.0 port and 5 Gbit/s USB 3.0 port:

- Place the REXT resistors close to the chip pins.
- Ensure that the differential data traces are short and straight, and each pair of differential traces has the same length.
- Ensure that the width of differential data traces is constant.
- Ensure that the spacing between adjacent differential data traces is constant. Route traces on the routing planes close to the GND plane, and do not change a routing plane.
- Route differential data traces by referencing complete GND planes and do not cross the plane splits.
- Minimize the use of vias and corners when routing differential data traces. When corners are required, use arcs or 45° turns rather than a 90° turn, reducing signal reflection and impedance variance.
- Ensure that there is no branch on differential data traces.
- Keep the differential data traces more than 50 mils away from other high-speed periodic signals and strong current signals to reduce crosstalk. Keep the differential data traces at least 20 mils away from low-speed non-periodic signals.

4.3.3 ADAC Interface

To ensure the output audio quality of the ADAC, design the PCB routing based on the following guidelines:

- Connect a 2.2 µF filter capacitor to the audio V_{REF} in parallel close to the ADAC_VREFDAC pin.
- Route the ADAC output signals based on the 3W rule.
- Do not use the analog video GND plane as the reference plane for other signal traces.
- When corners are required, use arcs or 45° turns rather than a 90° turn to reduce signal reflection.

4.3.4 VDAC Interface

To ensure the output video quality of the VDAC, design PCB routing based on the following guidelines:

- Connect the VDAC output end to an external 75 Ω resistor in series close to Hi3796M V100 to reduce VDAC drive inductive reactance.
- Place the analog video filtering circuit close to Hi3796M V100.
- Place the external 12 kΩ calibration resistor for the VDAC output close to the VDAC_REXT pin.
- Use a VDAC to drive only a single load. If you need to drive multiple loads to output multi-channel video signals, drives are recommended.
- Route all analog signal traces on the planes close to the analog video GND plane and do not change a routing plane.
- Do not use the analog video GND plane as the reference plane for other signal traces.
- When corners are required, use arcs or 45° turns rather than a 90° turn to reduce signal reflection.

4.3.5 HDMI Interface

Hi3796M V100 has one HDMI output interface.

Table 4-4 describes the recommended mode for connecting HDMI signals.

Table 4-4 Recommended mode for connecting HDMI signals

Signal	Connection Mode
TMDS_CLK	The differential impedance is 100 Ω and the trace must be shorter than 5 inches.
TMDS_DATA[2:0]	The differential impedance is 100 Ω and the trace must be shorter than 5 inches.

Note the following:

- The four pairs of HDMI differential traces must be as short as possible and have the same length. The length deviation of each pair of differential traces should be within 10 mils, and the length deviation between each pair of differential traces should be within 50 mils.
- The impedance of each pair of differential traces must be within 100 Ω.
- Route the four pairs of differential traces at the top layer and do not change the layer or punch vias.
- Do not cross power and GND plane splits when routing the four pairs of differential traces. Ensure that there is a complete current return plane beneath.
- Route the four pairs of differential traces far away from each other and surround each pair with GND traces.
- Never route 90°-turn or T-shaped traces.
- If there are vias besides HDMI traces, connect the vias to GND and fan the HDMI traces out through GND vias. In addition, punch a GND via next to the signal vias to ensure an even and continuous current return path.
- Use TVS tubes with less than 0.8 pF capacitance for the HDMI protective circuit.

4.3.6 TSI Interface

Table 4-5 describes the recommended mode for connecting TSI signals.

Table 4-5 Recommended mode for connecting TSI signals

Signal	Connection Mode
TSI_D[7:0]/TSI_VALID/TSI_SYNC	The impedance is 50 Ω and the trace must be shorter than 6 inches.
TSI_CLK	Serial clock: The impedance is 50 Ω, a 50 Ω resistor is connected in series at the component end, and the trace must be shorter than 6 inches.

4.3.7 SCI Interface

Table 4-6 describes the recommended mode for connecting SCI signals.

Table 4-6 Recommended mode for connecting SCI signals

Signal	Connection Mode
SIM_DATA (OD)	The impedance is 50 Ω and the trace must be shorter than 3.5 inches. This signal connects to a 560 Ω pull-up resistor.
SIM_CLK (OD)	The impedance is 50 Ω and the trace must be shorter than 3.5 inches. This signal connects to a 560 Ω pull-up resistor.
SIM_CLK (CMOS)	The impedance is 50 Ω and the trace must be shorter than 7 inches. A 33 Ω resistor is connected in series at the source end.

4.3.8 Others

PCB Signal Integrity Simulation

By using the board-level simulation tools, the PCB designers can simulate and analyze signal integrity based on the input/output buffer information specification (IBIS) models of the Hi3796M V100 interfaces, IBIS models of interconnected components, transmission line models, and board topologies. Based on the simulation results, PCB designers can adjust the typologies to meet the signal quality requirements in overshoot, undershoot, ringing, monotonicity, and others.

Note

If a clock signal trace connects to multiple loads, ensure good signal quality especially signal edge monotonicity regardless of the frequency.

5 Thermal Design Recommendations

5.1 Rated Operating Environment

Table 5-1 describes package thermal resistance of Hi3796M V100.

CAUTION

The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.

Table 5-1 Package thermal resistance design

Parameter	Symbol	Min	Typ	Max	Unit
Rated ambient temperature	T_A	–20	-	70	°C
Rated temperature	T_{JMAX}	-	None	125	°C
Junction-to-ambient thermal resistance	θ_{JA}	-	23	-	°C/W
Junction-to-board thermal resistance	θ_{JB}	-	9.62	-	°C/W
Junction-to-case thermal resistance	θ_{JC}	-	5.53	-	°C/W
Junction-to-top center of case thermal resistance	Ψ_{JT}	-	-	-	°C/W

The thermal resistance in the table is reference values assuming that no heat sinks are installed on a multi-layer PCB. The actual thermal resistance varies according to the design, size, thickness, material, and other physical factors of the PCB.

Table 5-2 describes recommended operating environment parameters.

Table 5-2 Recommended operating environment parameters

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature	T_A	0	25	55	°C
Temperature after long-term working	T_{JMAX}	-	-	125	°C

5.2 Reference Design for Heat Dissipation

Classification of Common Heat Sinks

Heat sink materials include aluminum alloy, copper alloy, aluminum-copper alloy, and ceramics.

Heat sink technologies include aluminum extrusion, cutting, bonding, casting, and mechanical lamination.

Recommendations for Heat Sink Materials and Technologies

The aluminum alloy heat sink is recommended because of its low cost. The following are the recommendations for heat sink technologies:

- The extruded heat sink outperforms the cast aluminum heat sink. 25–30% of the cast aluminum heat sink is aluminum, and the remaining is carbon and alloy. 70–80% of the extruded heat sink is aluminum, and the remaining is carbon and alloy. Therefore, the cast aluminum heat sink offers lower heat dissipation efficiency than the extruded heat sink.
- The black aluminum heat sink provides 3–8% higher heat dissipation efficiency than the silvery white one in natural environments, because the black outperforms the silver in thermal radiation.
- Common heat sinks are black and are processed by anodic oxidation.

To sum up, the aluminum alloy heat sink with the black surface and processed by anodic oxidation is recommended.

Heat Sink Size

The thermal resistance of the aluminum heat sink is calculated as follows:

$R = 1/(h \times A)$

where:

- **A** indicates the superficial area of the heat sink.
- **h** indicates the heat dissipation coefficient that depends on the temperature difference, wind speed, and material, thickness, and density of the heat sink.

A greater heat sink superficial area means a smaller thermal resistance. The following data is inferred (assume that the heat sink is 2 mm thick):

Superficial Area (cm^2)	Thermal Resistance (°C/W)
500	2.0
250	2.9
100	4.0
50	5.2
25	6.5

The thermal resistance of the heat sink required by Hi3796M V100 is calculated as follows:

Rsa = (Tj – Ta)/Q – (Rjc + Rcs) (formula 1)

- Tj: indicates the highest junction temperature (125°C) supported by Hi3796M V100.
- Ta: indicates the maximum ambient temperature (55°C) for long-term working.
- Q: indicates the power consumption (3.5 W) of Hi3796M V100.
- Rsa: indicates the thermal resistance of the heat sink (taking the wind speed into account).
- Rcs: indicates the thermal resistance (for example, 5°C/W) of heat-conducting media such as the thermal conductive adhesive.
- Rjc: indicates the package thermal resistance of Hi3796M V100 (4.1°C/W).

After the required thermal resistance of the heat sink is calculated by using formula 1, the superficial area of the heat sink can be obtained based on the preceding mapping between the superficial area and the thermal resistance.

For the Hi3796M V100:

- Rjc = 4.1°C/W
- Tj = 125°C

Assume that the ambient environment is 55°C, the STB temperature increases by 15°C (reference value), and Hi3796M V100 uses the thermal conductive adhesive with 5°C/W thermal resistance. The heat sink size can be calculated by using formula 1 as follows:

Rsa = (125 – 55 – 15)/3.5 – (4.1 + 5) = 6.6°C/W (The maximum power consumption indicated by Q is used here.)

Based on the preceding data, the heat sink with the superficial area of 25 cm^2 or greater meets the heat dissipation requirement of Hi3796M V100 with 4-layer PCB design.

NOTE

The preceding specifications are for reference only. You need to select heat sinks based on the board design.

Recommended Thermally Conductive Materials

Table 5-3 describes recommended thermally conductive materials.

Table 5-3 Recommended thermally conductive materials

Mode of Fixing Heat Sinks	Model	Thermal Conductivity Coefficient (w/m x k)	Ambient Temperature (°C)	Colloid Type	Insulation (V/mil)	Flame Retardance	Bearing Capacity (g)
Mechanical fixing	GF2000	2	−60 to +200	Silicone rubber	500	UL9V0	None
Non-mechanical fixing	Locotite 315	0.808	None	Acrylic resin	6000	UL9V2	None

Relationship Between the Fixing Mode and Heat Sink Mass

The fixing mode of the heat sink depends on the heat sink mass. You are advised not to fix a large-mass heat sink by using the thermally conductive adhesive. Table 5-4 describes the relationship between the fixing mode and the heat sink mass. You can select the fixing mode based on the board design.

Table 5-4 Relationship between the fixing mode and heat sink mass

Fixing Mode	Mass		
	m < 85 g	85 g ≤ m < 150 g	m ≥ 150 g
Thermally conductive adhesive	√	-	-
Push-pin buckle	√	-	-
Spring and screw	-	√	√
Dedicated metal buckle (non-preferable)	√	√	√
Plastic holder (non-preferable)	√	-	-

5.3 Reference Thermal Design for Circuits

5.3.1 Schematic Diagram

Power Supplies

Ensure that the efficiency of the board power tree is the highest as long as the power supplies are stable. To this end, design the board power supplies optimally and use fewer LDO components with large voltage difference to reduce the heat produced during power conversion.

The board supplies power to peripherals such as the USB device and SD card. You can retain the power supplies during design and shut down the power supplies when they are not used. The main ICs on the board must support the power-down mode.

Choose high-efficiency DC/DC circuits for power supplies that provide large currents. High-efficiency DC/DC circuits must be chosen for the core/CPU power supply and DDR because their working currents are large.

Low-Power Configurations for Idle Modules

Idle modules of Hi3796M V100 need to be set to the power-down mode or default mode.

SVB Control

Selective voltage binning (SVB) control is recommended for the core and CPU voltages of Hi3796M V100. That is, you can select an appropriate core voltage based on the actual chip technology to reduce power consumption.

CAUTION

Enable clock gating for Hi3796M V100 to reduce power consumption.

5.3.2 PCB

Component Layout

Lay out components based on the product architecture and heat dissipation design:

- Evenly place the components that consume a large amount of power and produce much heat to avoid local overheating, which may affect the reliability and efficiency of components. Place Hi3796M V100 away from power supplies.
- Design the product architecture properly to ensure that the heat produced internally can be efficiently dissipated.

Routing

The routing recommendations are as follows:

- For the connection style of vias under the Hi3796M V100, select the full connection style but not the thermal connection style to improve the board heat dissipation efficiency.
- The GND signals and 1.1 V, 1.5 V, and 3.3 V power signals of Hi3796M V100 are connected over copper sheets. When the signal overcurrent capability is ensured, more vias on copper sheets are recommended.
- Increase the size of copper planes under and around the components that produce much heat to ensure that PCB heat can be effectively dissipated. Place inductors and power chips in a distributed manner and increase the size of copper planes around them.

6 Soldering Process Recommendations

6.1 Overview

Objective

Define the zone temperatures in the surface mounting technology (SMT) phase.

Application Scope

HiSilicon Hi3796M V100

Basic Information

All HiSilicon products for customers comply with the restriction of the use of certain hazardous substances (RoHS) directive. In the part number format Hi*xxxx*RBC V*xxx*, the letter R indicates RoHS. These products are lead-free. The lead-free technology and mixing technology are used in the reflow soldering of HiSilicon chips.

Reflow Chart

Note the following:

- HiSilicon chips: All HiSilicon chips for customers are lead-free RoHS-compliant products.
- Lead-free technology: A technology in which solder paste and all components (including the board, all ICs, capacitors, and resistors) are lead-free.
- Mixing technology: A technology in which lead solder pastes, lead-free BGAs, and lead ICs are used.

6.2 Requirements of Lead-Free Reflow Soldering

Figure 6-1 shows a lead-free reflow soldering curve.

Figure 6-1 Lead-free reflow soldering curve

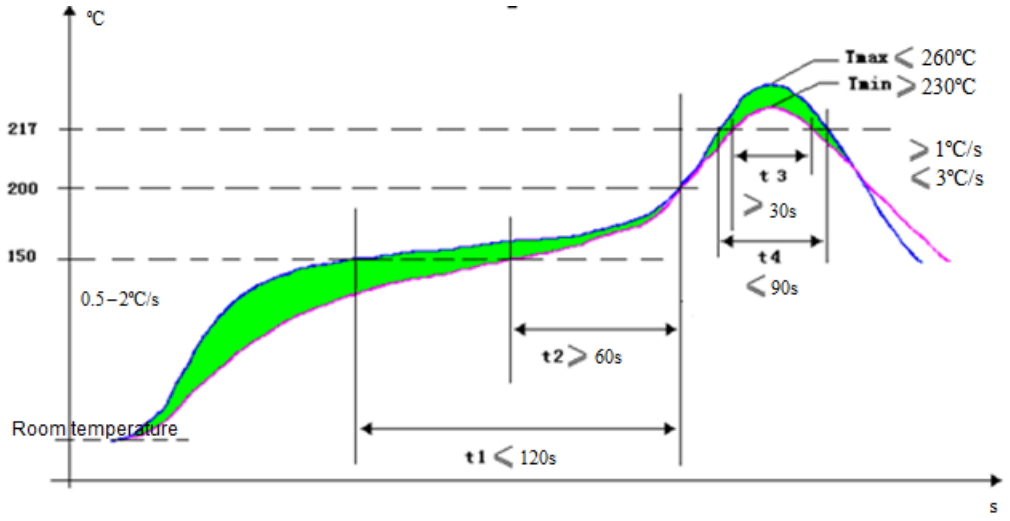


Table 6-1 describes lead-free reflow soldering parameters.

Table 6-1 Lead-free reflow soldering parameters

Zone	Duration	Heating Up Slope	Peak Temperature	Cooling Down Slope
Preheat zone (40–150°C or 104–302°F)	60–150s	≤ 2.0ºC/s (≤ 35.6ºF/s)	None	None
Soak zone (150–200°C or 302–392°F)	60–120s	< 1.0ºC/s (< 33.8ºF/s)	None	None
Reflow zone (> 217°C or 423°F)	60–90s	None	230−260ºC (446−500ºF)	None
Cooling zone (Tmax to 180°C or 356°F)	None	None	None	1.0ºC/s ≤ Slope ≤ 4.0ºC/s (33.8ºF/s ≤ Slope ≤ 39.2ºF/s)

NOTE

- Preheat zone: The temperate range is 40–150°C (104–302°F), the heating up slope must be about 2.0°C/s (36°F/s), and the zone duration must be 50–60s.
- Soak zone: The temperature range is 150–200°C (302–392°F), the heating up slope must be less than 1.0°C/s (34°F/s), and the zone duration must be 60–120s. Slow heating is required; otherwise, soldering is poor.
- Reflow zone: The zone temperature increases from 217°C (423°F) to Tmax, and then decreases from Tmax to 217°C (423°F). The zone duration must be 60–90s.
- Cooling zone: The zone temperature decreases from Tmax to 180°C (356°F). The cooling down slope must be within 4.0°C/s (39°F/s).
- The ambient temperate must increase from 25°C (77°F) to 250°C (482°F) within 6 minutes.

- The reflow soldering curve shown in Figure 6-1 is recommended. However, you can adjust it as required.
- Typically, the duration of the reflow zone is 60–90s. For the boards with great heat capacity, the duration can be extended to 120s. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 6-2 describes the thermal resistance standard for the lead-free package according to the IPC/JEDEC 020D standard.

Table 6-2 Thermal resistance standard for the lead-free package in the IPC/JEDEC 020D standard

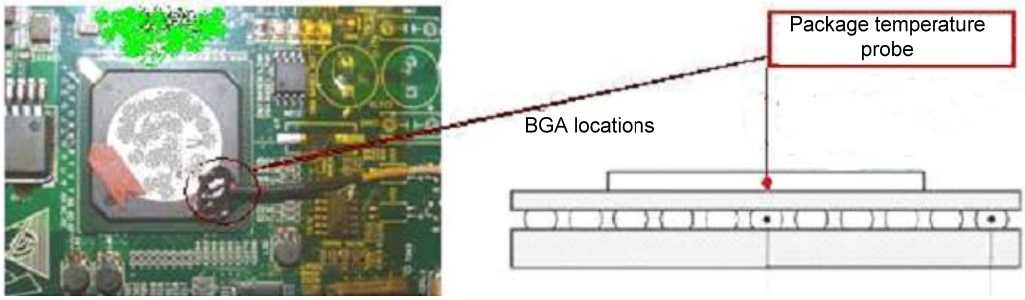
Package Thickness	Temperature 1 (Package Volume < 350 mm^3 or 0.02 $in.^3$)	Temperature 2 (Package Volume = 350–2000 mm^3 or 0.02–0.12 $in.^3$)	Temperature 3 (Package Volume > 2000 mm^3 or 0.12 $in.^3$)
< 1.6 mm (0.06 in.)	260°C (500°F)	260°C (500°F)	260°C (500°F)
1.6–2.5 mm (0.06–0.10 in.)	260°C (500°F)	250°C (482°F)	245°C (473°F)
> 2.5 mm (0.10 in.)	250°C (482°F)	245°C (473°F)	245°C (473°F)

The component soldering terminals (such as the solder ball and pin) and external heat sinks are not taken into account for volume calculation.

The measurement method for the reflow soldering curve is as follows:

According to the JEP140 standard, to measure the package temperature, you are advised to place the temperature probe of the thermocouple close to the chip surface if the package is thin or to drill a hole on the package surface and place the temperature probe of the thermocouple into the hole if the chip package is thick. The second method is recommended based on the thickness of most chip packages. However, this method is not applicable if the chip package is too thin to drill a hole. See Figure 6-2.

Figure 6-2 Measuring the package temperature



NOTE

To measure the QFP package temperature, place the temperature probe close to pins.

6.3 Requirements of Mixing Reflow Soldering

Lead-free components must be properly soldered during mixing reflow soldering. Table 6-3 describes mixing reflow soldering parameters.

Table 6-3 Mixing reflow soldering parameters

Zone	Item	Lead BGA	Lead-free BGA	Other Components
Preheat zone (40–150°C or 104–302°F)	Duration	60–150s		
	Heating up slope	< 2.5°C/s (37°F/s)		
Soak zone (150–183°C or 302–361°F)	Duration	30–90s		
	Heating up slope	< 1.0°C/s (34°F/s)		
Reflow zone (> 183°C or 361°F)	Peak temperature	210–240°C (410–464°F)	220–240°C (428–464°F)	210–245°C (410–473°F)
	Duration	30–120s	60–120s	30–120s
Cooling zone (Tmax to 150°C or 302°F)	Cooling down slope	1.0°C/s ≤ Slope ≤ 4.0°C/s (34°F/s ≤ Slope ≤ 39°F/s)		

NOTE

The preceding parameter values are provided based on the soldering joint temperature. The maximum and minimum soldering joint temperatures for the board must meet the requirements described in Table 6-3.

When the soldering curve is adjusted, the package thermal resistance requirements on the board components must be met. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 6-4 describes the thermal resistance standard for the lead package according to the IPC/JEDEC 020D standard.

Table 6-4 Thermal resistance standard for the lead package

Package Thickness	Temperature 1 (Package Volume < 350 mm^3 or 0.02 $in.^3$)	Temperature 1 (Package Volume ≥ 350 mm^3 or 0.02 $in.^3$)
< 2.5 mm (0.10 in.)	235°C (455°F)	220°C (428°F)
≥ 2.5 mm (0.10 in.)	220°C (428°F)	220°C (428°F)

The component soldering terminals (such as the solder ball and pin) and external heat sinks are not taken into account for volume calculation.

According to the JEP140 standard, the method for measuring the temperature of the package soldered with the mixing technology is the same as that for measuring the temperature of the package soldered with the lead-free technology. For details, see section 6.2 "Requirements of Lead-Free Reflow Soldering."

7 Moisture-Sensitive Specifications

7.1 Overview

Objective

Define the usage rules for moisture-sensitive ICs, ensuring that ICs are properly used.

Application Scope

All HiSilicon products for external customers

Terminology

- Floor life: time during which a HiSilicon chip can be stored in the workshop at 30°C (86°F) and 60% relative humidity (RH), that is, the time from moisture barrier bag (MBB) unpacking to reflow soldering
- Desiccant: a material for absorbing moisture to keep things dry
- Humidity indicator card (HIC): a card that indicates the humidity status
- Moisture sensitivity level (MSL): a level for measuring the moisture degree
- MBB: a vacuum bag for protecting products against moisture
- Solder reflow: reflow soldering
- Shelf life: storage period

7.2 HiSilicon Moisture-proof Packaging

7.2.1 Basic Information

The vacuum packaging materials consist of the following:

- An HIC
- An MBB
- Desiccant

Figure 7-1 Vacuum packaging materials

7.2.2 Incoming Inspection

When the vacuum bag is unpacked before SMT in the factories of customers or their partners:

- If the largest indicator dot of the HIC is not blue or khaki, rebake the chip by referring to Table 7-1.
- If the 10% RH dot of the HIC is blue or khaki, the chip is dry. In this case, replace the desiccant and pack the chip into a vacuum bag.

If the 10% RH dot is not blue or khaki and the 5% RH dot is red or light green, the chip is moist. In this case, rebake the chip by referring to Table 7-1.

7.2.3 Storage and Usage

Storage Environment

You are advised to store products at 30°C (86°F) or lower and at most 60% RH.

Shelf Life

At 30°C (86°F) or lower and at most 60% RH, the shelf life is greater than or equal to 12 months for vacuum packaging.

Floor Life

Table 7-1 describes the floor life at 30°C (86°F) or lower and at most 60% RH.

Table 7-1 Floor life

MSL	Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated
1	Unlimited at 30°C (86°F) or lower and at most 85% RH

MSL	Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, the product must be reflowed within the time limit specified on the label.

Usage

- If a chip has been exposed to air for more than 2 hours at 30°C (86°F) or lower and at most 60% RH, rebake it and pack it into a vacuum bag.
- If a chip has been exposed to air for not more than 2 hours at 30°C (86°F) or lower and at most 60% RH, replace the desiccant and pack the chip into a vacuum bag.

For details about other storage modes and usage rules, see the JEDEC J-STD-033A standard.

7.3 Rebaking

Applicable Products

All moisture-sensitive ICs of HiSilicon

Application Scope

All ICs that need to be rebaked

Rebaking Reference

Table 7-2 Rebaking reference

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
≤ 1.4 mm (0.06 in.)	2a	3 hours	11 hours	5 days
	3	7 hours	23 hours	9 days
	4	7 hours	23 hours	9 days
	5	7 hours	24 hours	10 days
	5a	10 hours	24 hours	10 days

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
≤ 2.0 mm (0.08 in.)	2a	16 hours	2 days	22 days
	3	17 hours	2 days	23 days
	4	20 hours	3 days	28 days
	5	25 hours	4 days	35 days
	5a	40 hours	6 days	56 days
≤ 4.5 mm (0.18 in.)	2a	48 hours	7 days	67 days
	3	48 hours	8 days	67 days
	4	48 hours	10 days	67 days
	5	48 hours	10 days	67 days
	5a	48 hours	10 days	67 days

NOTE

- Table 7-2 lists the minimum rebaking time for moist chips.
- Low-temperature rebaking is recommended.
- For details, see the JEDEC standard.

8 Interface Timings

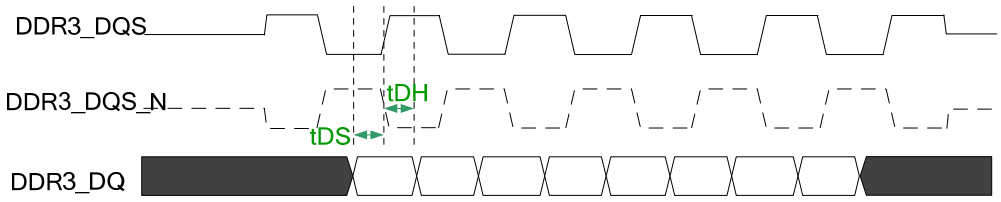
8.1 DDR Interface Timings

8.1.1 Write Timings

Write Timing of DDR3_DQS Relative to DDR3_DQ

The major parameters in the write timing of DDR3_DQS relative to DDR3_DQ are tDS and tDH.

Figure 8-1 Write timing of DDR3_DQS relative to DDR3_DQ



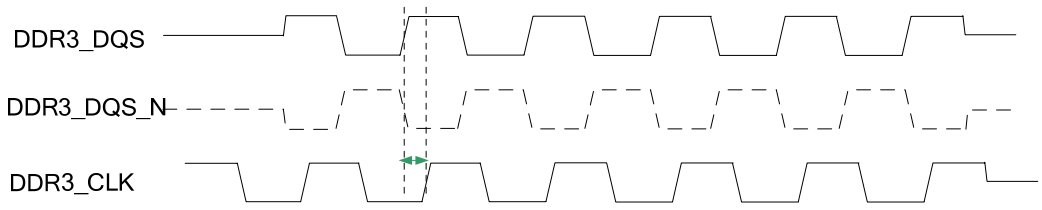
NOTE

The write timing in Figure 8-1 applies to the two 16-bit DQ fields {DDR3_DQS[1:0], DDR3_DQS_N[1:0], DDR3_DQ[15:0]} and {DDR3_DQS[3:2], DDR3_DQS_N[3:2], DDR3_DQ[31:16]}.

Write Timing of DDR3_DQS Relative to DDR3_CLK

Figure 8-2 shows the write timing of DDR3_DQS relative to DDR3_CLK.

Figure 8-2 Write timing of DDR3_DQS relative to DDR3_CLK (CMDADDR PHY)



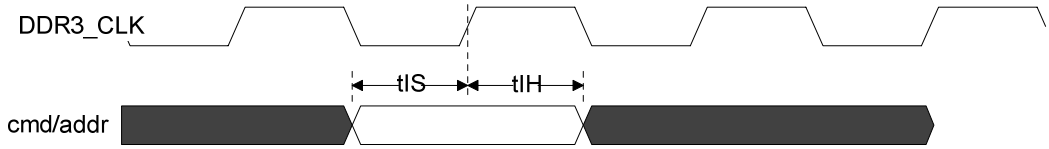
NOTE

The phase deviation of DDR3_DQS[3:0] and DDR3_DQS_N[3:0] relative to DDR3_CLK (CMDADDR PHY) cannot exceed a quarter of T DRAM clock (DDR3_CLK) in the position marked with a green arrow.

Write Timing of CMD/ADDR Relative to DDR3_CLK

The sampling clock of command and address signals is DDR3_CLK. Figure 8-3 shows the write timing of CMD/ADDR relative to DDR3_CLK.

Figure 8-3 Write timing of CMD/ADDR relative to DDR3_CLK



8.1.2 Read Timings

Read Timing of ADDR/CMD Relative to DDR3_CLK

The read timing of CMD/ADDR relative to DDR3_CLK is the same as the write timing of CMD/ADDR relative to DDR3_CLK.

Read Timing of DDR3_DQS Relative to DDR3_DQ

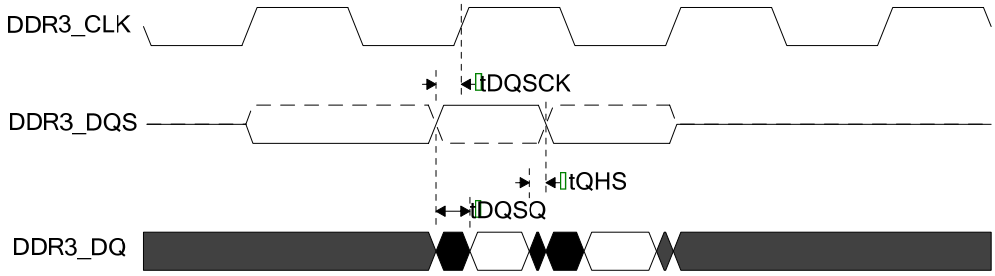
The read timings of DDR3_DQS relative to DDR3_DQ are classified into the DDR*n* SDRAM output timing, DDR3_DQS timing on the DDR PHY side, and DDR3_DQ timing on the DDR PHY side.

For the DDR*n* SDRAM output timing, ideally the phases of the DQS signal from the DDR (DDR3_DQS connected to the chip) and DDR3_CLK output by the DDR PHY are the same. However, due to external interferences, when the DQS is transmitted to the DDR PHY side, it has tDQSCK skew relative to DDR3_CLK, and the skew cannot exceed 0.35 ns.

The DQ signal from the DDR also has phase jitters relative to DQS. tDQSQ and tQHS are the timing parameters for measuring the jitters. As shown in Figure 8-4, tDQSQ indicates the jitter of the latest valid DQ relative to DQS (observed on the DDR PHY side), and it cannot exceed 0.2 ns; tQHS indicates the jitter of the earliest valid DQ relative to DQS (or the jitter of the earliest invalid DQ relative to the next DQS flip-flop), and it is 0.3 ns.

Figure 8-4 shows the output timing of the DDR*n* SDRAM.

Figure 8-4 Output timing of the DDR*n* SDRAM



8.1.3 Timing Parameters

The DDR interface timings comply with the JEDEC standards (JESD79-2E and JESD79-3B). All the timings discussed in this document are output timings on the DDR PHY side.

For HD chips, take the timing parameters of DDR3-1066 as an example.

Table 8-1 and Table 8-2 describe the clock parameters of the DDR3-1066 SDRAM.

Table 8-1 Clock parameters of the DDR3-1066 SDRAM

Parameter	Typ	Unit
DDR clock frequency	533.00	MHz
PLL jitter	0.200	ns
PLL duty cycle	47.000	%
Clock skew	0.100	ns

Table 8-2 Parameters of the DDR3-1066 SDRAM

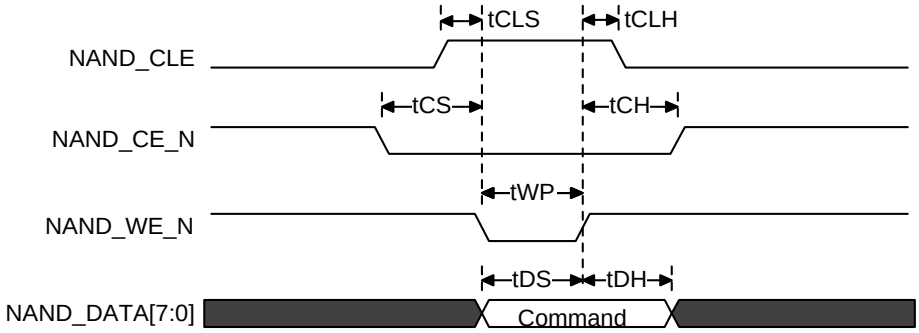
Parameter	Symbol	Typ	Unit
Setup time of the DQS falling edge relative to the DDR clock	tDSS	0.500	ns
Hold time of the DQS falling edge relative to the DDR clock	tDSH	0.500	ns
Setup time of DQ/DM relative to DQS	tDS	0.075	ns
Hold time of DQ/DM relative to DQS	tDH	0.150	ns
Skew of DQS relative to DQ	tDQSQ	0.200	ns
Setup time of ADDR/CMD relative to the DDR clock	tIS	0.200	ns
Hold time of ADDR/CMD relative to the DDR clock	tIH	0.275	ns
Skew of the DQS output relative to the DDR clock	tDQSCK	0.400	ns

8.2 NANDC Interface Timings

8.2.1 Command Cycle Timing

Figure 8-5 shows the NANDC command cycle timing.

Figure 8-5 NANDC command cycle timing



NOTE

The level widths of NAND_WE_N and NAND_RE_N can be set to high or low by configuring the NF_PULSE_WIDTH register of the NANDC. Therefore, some parameters in the NANDC interface timing diagrams vary according to the settings of NF_PULSE_WIDTH. In the following tables, these parameters are marked with "Configurable."

Table 8-3 describes the parameters of the NANDC command cycle timing.

Table 8-3 Parameters of the NANDC command cycle timing

Parameter	Symbol	Min	Max	Unit	Remarks
Setup time of NAND_CLE	tCLS	0	-	ns	-
Hold time of NAND_CLE	tCLH	10	-	ns	Configurable
Setup time of NAND_CE_N	tCS	0	-	ns	-
Hold time of NAND_CE_N	tCH	10	-	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	-	ns	Configurable
Data setup time	tDS	10	-	ns	Configurable
Data hold time	tDH	10	-	ns	Configurable

8.2.2 Address Cycle Timing

Figure 8-6 shows the NANDC address cycle timing.

Figure 8-6 NANDC address cycle timing

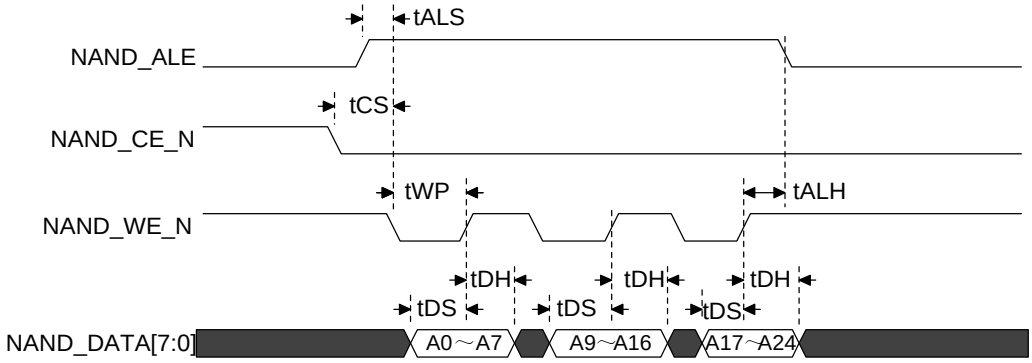


Table 8-4 describes the parameters of the NANDC address cycle timing.

Table 8-4 Parameters of the NANDC address cycle timing

Parameter	Symbol	Min	Max	Unit	Remarks
Setup time of NAND_CE_N	tCS	0	-	ns	-
Pulse width of NAND_WE_N	tWP	15	-	ns	Configurable
Setup time of NAND_ALE	tALS	0	-	ns	-
Hold time of NAND_ALE	tALH	10	-	ns	Configurable
Data setup time	tDS	10	-	ns	Configurable
Data hold time	tDH	10	-	ns	Configurable

8.2.3 Data Write Timing

Figure 8-7 shows the NANDC data write timing.

Figure 8-7 NANDC data write timing

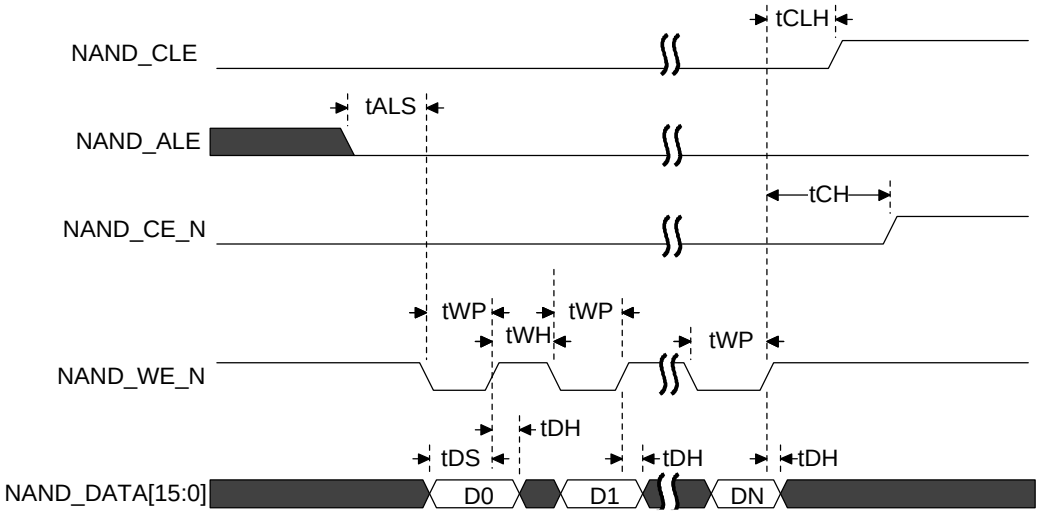


Table 8-5 describes the parameters of the NANDC data write timing.

Table 8-5 Parameters of the NANDC data write timing

Parameter	Symbol	Min	Max	Unit	Remarks
Hold time of NAND_CLE	tCLH	10	-	ns	Configurable
Hold time of NAND_CE_N	tCH	10	-	ns	Configurable
Pulse width of NAND_WE_N	tWP	15	-	ns	Configurable
Setup time of NAND_ALE	tALS	0	-	ns	Configurable
Data setup time	tDS	10	-	ns	Configurable
Data hold time	tDH	10	-	ns	Configurable
High-level hold time of NAND_WE_N	tWH	15	-	ns	Configurable

8.2.4 Data Read Timing

Figure 8-8 shows the NANDC data read timing.

Figure 8-8 NANDC data read timing

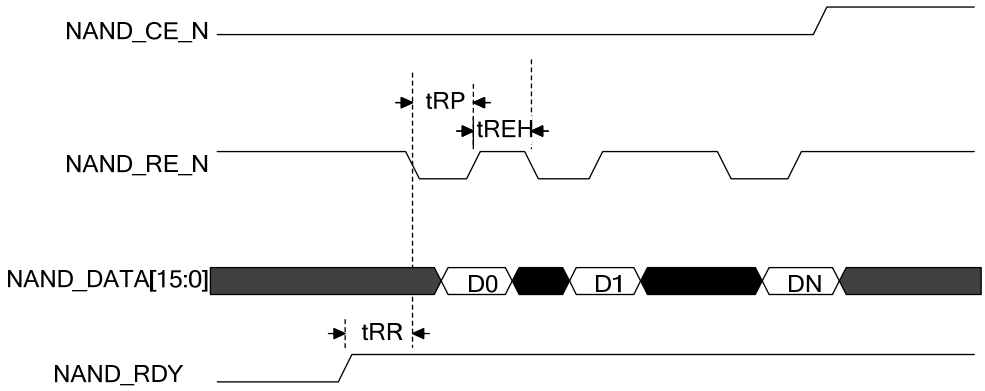


Table 8-6 describes the parameters of the NANDC data read timing.

Table 8-6 Parameters of the NANDC data read timing

Parameter	Symbol	Min	Max	Unit	Remarks
Low-level wait time of NAND_RE_N	tRR	15	-	ns	Configurable
Pulse width of NAND_RE_N	tRP	15	-	ns	Configurable
High-level width of NAND_RE_N	tREH	15	-	ns	Configurable

The tRR delay is configurable.

8.3 TSI Interface Timings

Figure 8-9 shows the TSI interface timings.

Figure 8-9 TSI interface timings

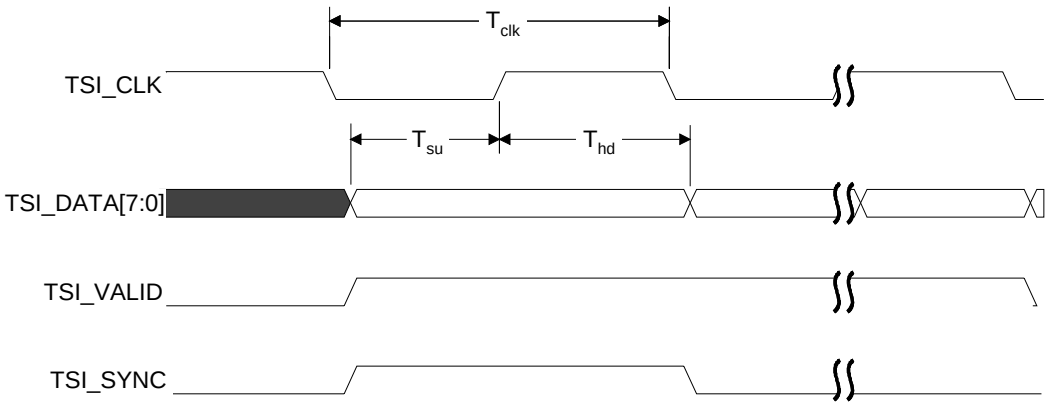


Table 8-7 describes the parameters of the TSI interface timings.

Table 8-7 Parameters of the TSI interface timings

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
TSI_CLK clock cycle	T_{clk}	20	-	-	ns	Parallel
		5.26	-	-	ns	Serial
Input signal setup time	T_{su}	9.3	-	-	ns	Parallel
		2.5	-	-	ns	Serial
Input signal hold time	T_{hd}	2.0	-	-	ns	Parallel
		1.5	-	-	ns	Serial

8.4 Ethernet MAC Interface Timings

8.4.1 MDIO Interface Timings

Figure 8-10 shows the read timing of the MDIO interface.

Figure 8-10 MDIO read timing

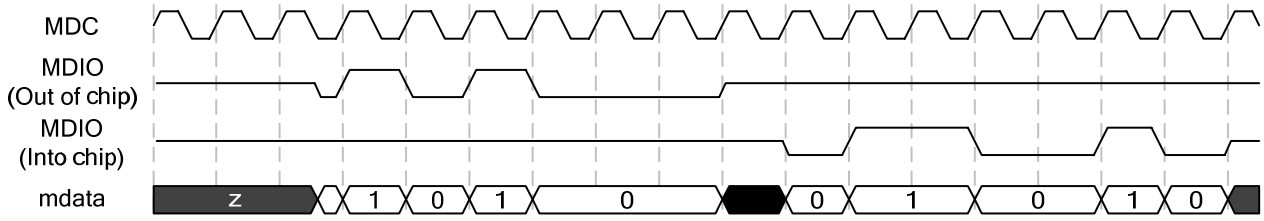


Figure 8-11 shows the write timing of the MDIO interface.

Figure 8-11 MDIO write timing

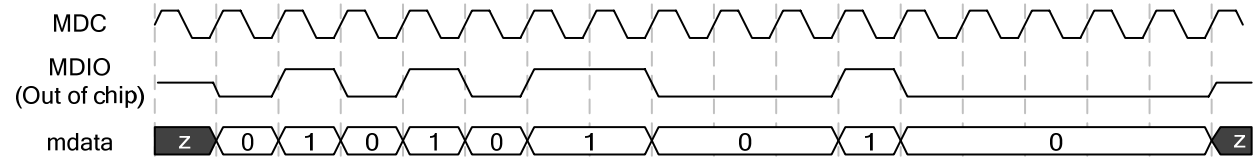


Figure 8-12 illustrates the MDIO interface timing parameters.

Figure 8-12 MDIO interface timing

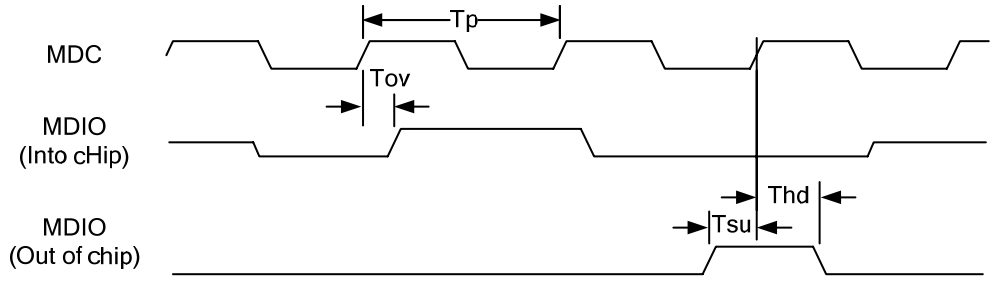


Table 8-8 describes the timing parameters of the MDIO interface.

Table 8-8 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	166	20833	ns
MDIO clock cycle	Tp	MDC	333	41667	ns
MDIO data TX setup time	Tsu	MDIO	10	-	ns
MDIO data TX hold time	Thd	MDIO	10	-	ns

The MDC clock cycle Tp can be changed by adjusting the MDC frequency (MDIO_RWCTRL[frq_dv]). To be specific, you can divide the 150 MHz frequency of the Ethernet working clock by 100, 50, or other values. Tov is related to the clock period Tp of the MDC and it is about Tmdc/2.

8.5 SIO Interface Timings

8.5.1 I²S Mode Interface Timings

Figure 8-13 shows the RX timing of the I^{2}S interface.

Figure 8-13 RX timing of the I^{2}S interface

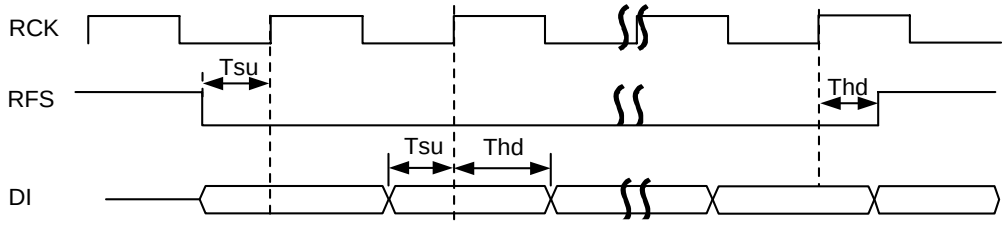


Figure 8-14 shows the TX timing of the I^{2}S interface.

Figure 8-14 TX timing of the I²S interface

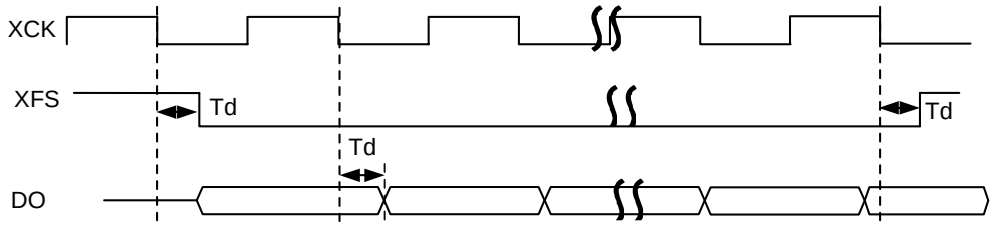


Table 8-9 describes the timing parameters of the I²S interface.

Table 8-9 Timing parameters of the I²S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	-	-	ns
Input signal hold time	T_{hd}	10	-	-	ns
Output signal delay	T_d	0	-	8	ns

8.5.2 PCM Mode Interface Timings

Figure 8-15 shows the RX timing of the PCM interface.

Figure 8-15 RX timing of the PCM interface

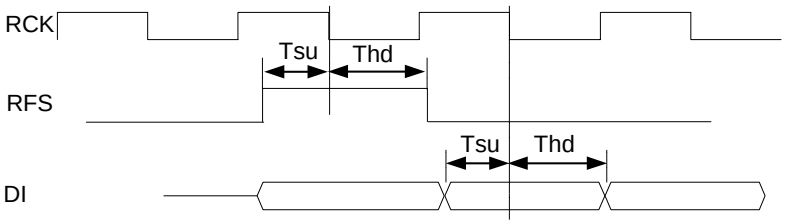


Figure 8-16 shows the TX timing of the PCM interface.

Figure 8-16 TX timing of the PCM interface

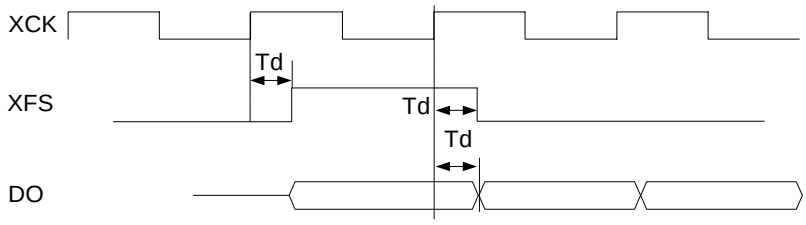


Table 8-10 describes the timing parameters of the PCM interface.

Table 8-10 Timing parameters of the PCM interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	-	-	ns
Input signal hold time	T_{hd}	10	-	-	ns
Output signal delay	T_d	0	-	8	ns

8.6 I²C Interface Timings

Figure 8-17 shows the transfer timing of the I²C interface.

Figure 8-17 Transfer timing of the I²C interface

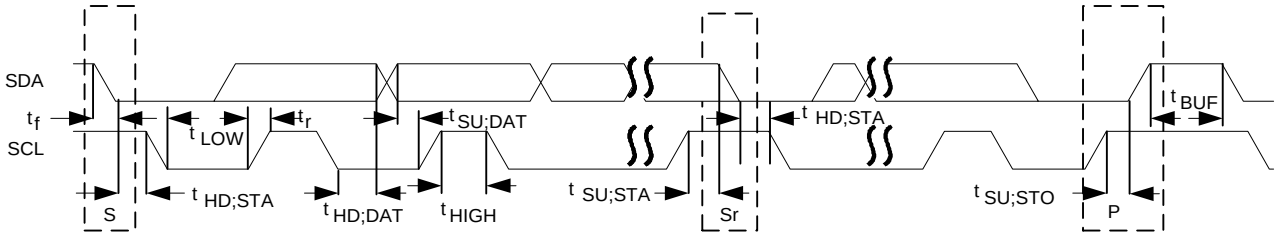


Table 8-11 describes the timing parameters of the I²C interface.

Table 8-11 Timing parameters of the I²C interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Start hold time	$t_{HD;STA}$	4.0	-	0.6	-	µs
SCL low-level cycle	t_{LOW}	4.7	-	1.3	-	µs
SCL high-level cycle	t_{HIGH}	4.0	-	0.6	-	µs
Start setup time	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	-	100	-	ns
SDA and SCL rising time	t_r	-	1000	$20 + 0.1C_b$	300	ns
SDA and SCL falling time	t_f	-	300	$20 + 0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus release time from start	t_{BUF}	4.7	-	1.3	-	µs

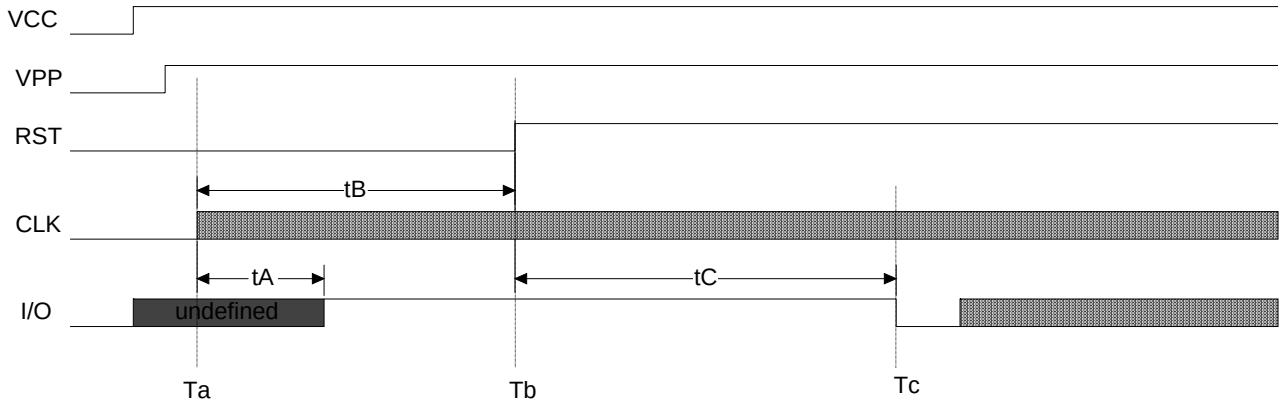
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
to end						
Bus load	C_b	-	400	-	400	pF
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	-	$0.2V_{DD}$	-	V

8.7 SCI Interface Timings

8.7.1 Activation and Cold Reset Timing

The frequency (f) of an A-type card (5 V) ranges from 1 MHz to 5 MHz; the frequency (f) of a B-type card (3 V) ranges from 1 MHz to 4 MHz. Figure 8-18 shows the timing of the activation and cold reset interface. The value ranges of tA, tB, and tC are as follows: tA ≤ 200/f, tB ≥ 400/f, and 400/f ≤ tC ≤ 40000/f.

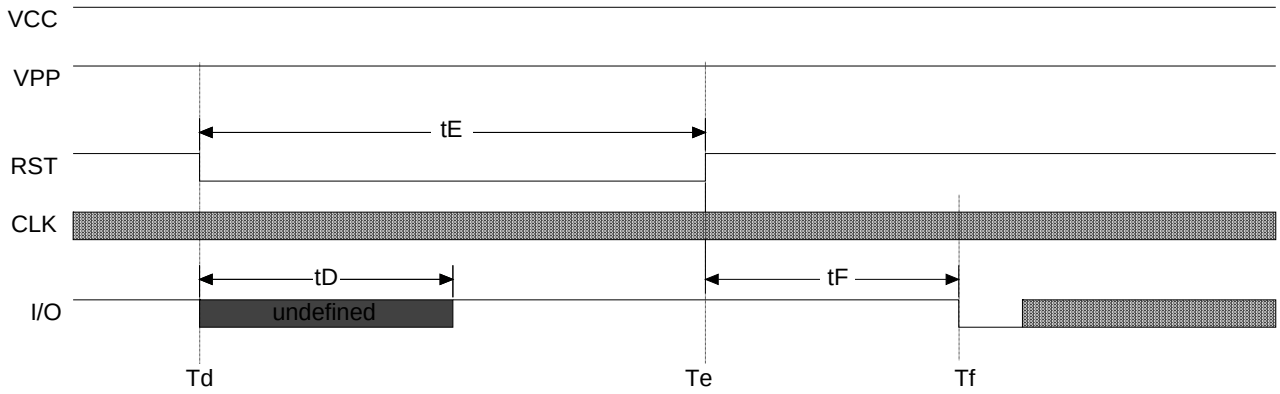
Figure 8-18 Activation and cold reset timing of the SCI interface



8.7.2 Hot Reset Timing

The frequency (f) of an A-type card (5 V) ranges from 1 MHz to 5 MHz; the frequency (f) of a B-type card (3 V) ranges from 1 MHz to 4 MHz. Figure 8-19 shows the hot reset timing. The value ranges of tD, tE, and tF are as follows: tD ≤ 200/f, tE ≥ 400/f, and 400/f ≤ tF ≤ 40000/f.

Figure 8-19 SCI hot reset timing



8.7.3 Release Timing

Figure 8-20 shows the timing of the SCI release interface.

Figure 8-20 SCI release timing

8.8 SPI Interface Timings

NOTE

In Figure 8-21 to Figure 8-23, the conventions are as follows:

- MSB: most significant bit
- LSB: least significant bit
- SPI_CK(0): SPO = 0
- SPI_CK(1): SPO = 1

Figure 8-21 shows the SPICK timing of the SPI interface.

Figure 8-21 SPICK timing

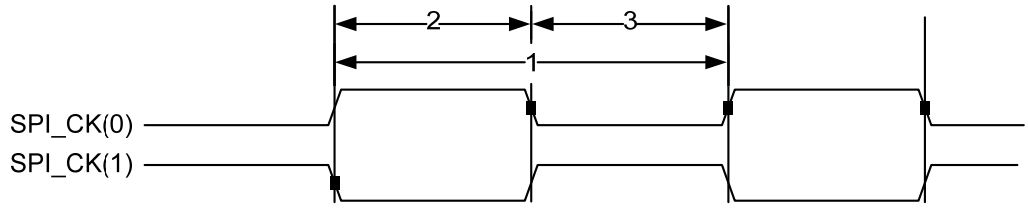


Figure 8-22 and Figure 8-23 show the timings of the SPI interface in master mode.

Figure 8-22 SPI interface timing in master mode (sph = 0)

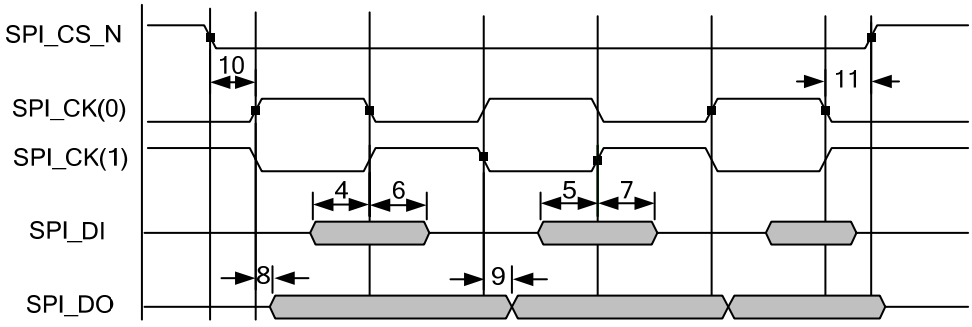


Figure 8-23 SPI interface timing in master mode (sph = 1)

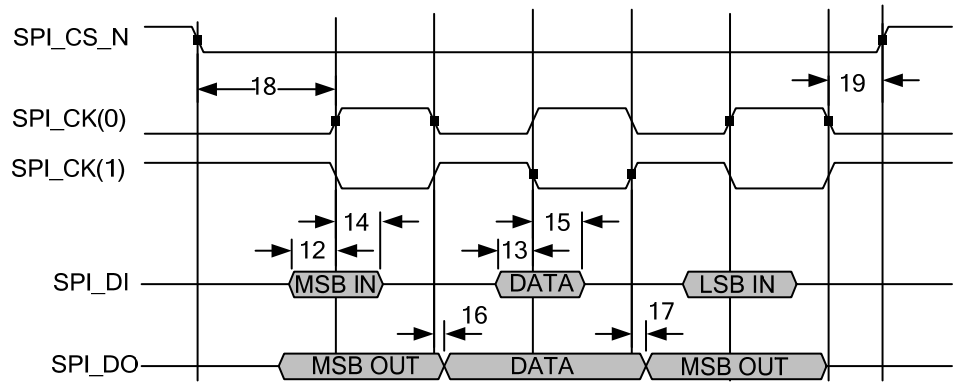


Table 8-12 describes the timing parameters of the SPI interface.

Table 8-12 Timing parameters of the SPI interface

No	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	-	-	-	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	-	-	-	ns
3	Pulse duration, SPI_CK low (all master	tw2	-	-	-	ns

No	Parameter	Symbol	Min	Typ	Max	Unit
	modes)					
4	Setup time, SPI_DI (input) valid before the SPI_CK (output) falling edge	tsu1	-	-	-	ns
5	Setup time, SPI_DI (input) valid before the SPI_CK (output) rising edge	tsu2	-	-	-	ns
6	Hold time, SPI_DI (input) valid after the SPI_CK (output) falling edge	th1	-	-	-	ns
7	Hold time, SPI_DI (input) valid after the SPI_CK (output) rising edge	th2	-	-	-	ns
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	-	-	-	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	-	-	-	ns
10	Delay time, SPI_CS_N (output) falling edge to the first SPI_CK (output) rising or falling edge	td3	-	-	-	ns
11	Delay time, SPI_CK (output) rising or falling edge to the SPI_CS_N (output) rising edge	td4	-	-	-	ns
12	Setup time, SPI_DI (input) valid before the SPI_CK (output) rising edge	tsu3	-	-	-	ns
13	Setup time, SPI_DI (input) valid before the SPI_CK (output) falling edge	tsu4	-	-	-	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	-	-	-	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	-	-	-	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	-	-	-	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	-	-	-	ns
18	Delay time, SPI_CS_N (output) falling edge to the first SPI_CK (output) rising or falling edge	td7	-	-	-	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	-	-	-	ns

8.9 MMC/SD/SDIO Interface Timings

Figure 8-24 shows the output timing.

Figure 8-24 Output timing

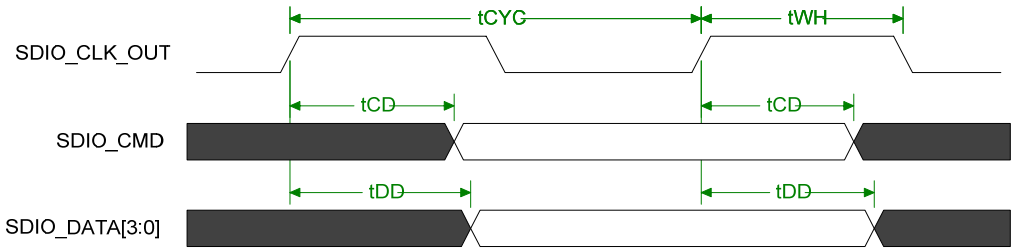


Figure 8-25 shows the input timing.

Figure 8-25 Input timing

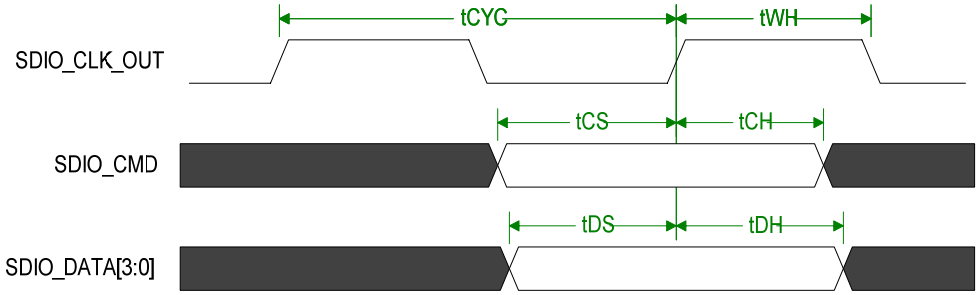


Table 8-13 describes the timing parameters of the MMC interface.

Table 8-13 Timing parameters of the MMC interface

Parameter	Description	Min	Max	Unit
tCYC	Card clock cycle	10	34000[a]	ns
tWH	High level duration of the card clock	4.95	16999.8	ns
tCCLK_IN	Working clock cycle of the MMC module	10−66.67		ns
tCD	SDIO_CMD output delay	1.9[b]	6.7[b]	ns
tDD	SDIO_DATA output delay	1.7[b]	6.4[b]	ns
tCS	SDIO_CMD input setup time	3.1[c]	-	ns
tCH	SDIO_CMD input hold time	0.7[c]	-	ns

Parameter	Description	Min	Max	Unit
tDS	SDIO_DATA input setup time	3.3[c]	-	ns
tDH	SDIO_DATA input hold time	0.7[c]	-	ns

NOTE

- a. The minimum frequency of the SDIO clock source input is 15 MHz. In the SDIO module, the clock source frequency can be divided by 510 at most. That is, the clock cycle can be 34 ms (1000/15 x 510). For details, see the SDIO CLKDIV register.
- b. (1) The phase shift of the output drive clock is set to 90º. Eight phase shifts including 0º, 45º, 90º, 135º, 180º, 225º, 270º, and 315º are supported. For details, see the description of PERI_CRG39 bit[18:16] in the *Hi3796M V100 Intelligent Network Terminal Media Processor Data Sheet*. (2) The parameters in Table 8-13 apply only to the SD 3.0 protocol. According to the eMMC protocol, the minimum data output delay is 2.5 ns in DDR50 mode. When an eMMC is connected, the drive clock phase can be adjusted to meet the hold time requirement.
- c. The phase shift of the input sampling clock is set to 90º. Eight phase shifts including 0º, 45º, 90º, 135º, 180º, 225º, 270º, and 315º are supported. For details, see the description of PERI_CRG39 bit[14:12] in the *Hi3796M V100 Intelligent Network Terminal Media Processor Data Sheet*.