ePad Soldering for HiSilicon QFP Chips

User Guide

Issue **00B01**

Date **2015-06-04**

HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

About This Document

Purpose

This document describes the ePad soldering process for HiSilicon quad flat package (QFP) chips and the precautions to be taken.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3110E	V200/V400/V500
Hi3716M	V300/V310
Hi3798M	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B01 (2015-06-04)

This issue is the first draft release.

Contents

About This Document iii
1 Overview 1
2 Soldering Process 2
2.1 Recommended Thermal Pad Design Scheme 2
2.2 Recommended Stencil Apertures 2

Figures

Figure 1-1 Package side view 1

Figure 2-1 Schematic diagram of the stencil apertures on the QFP thermal pad 3

Figure 2-2 Relationship between the ePad aperture and the pin aperture on the stencil 3

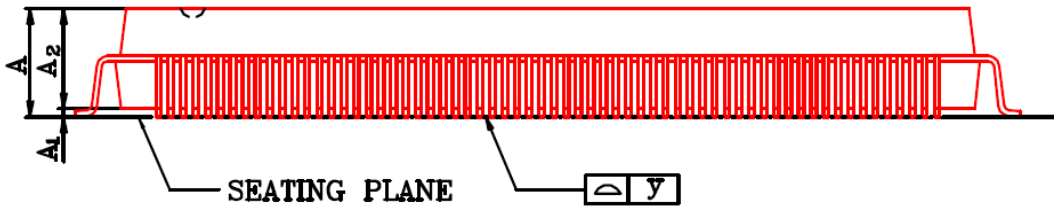
1 Overview

The HiSilicon QFP chips with the exposed pad (ePad) are listed as follows:Hi3110E V200/V400/V500

- Hi3716M V300/V310
- Hi3798M V100

For a HiSilicon QFP chip, the coplanarity between pins and the PCB ground pad is limited to 0.05−0.125 mm (A1 in Figure 1-1, international standard: 0.05−0.15 mm).

Figure 1-1 Package side view



where

- A: height of the QFP chip
- A1: component standoff
- A2: thickness of the chip

2 Soldering Process

2.1 Recommended Thermal Pad Design Scheme

For a HiSilicon QFP chip, you are advised to design the thermal pad as follows:

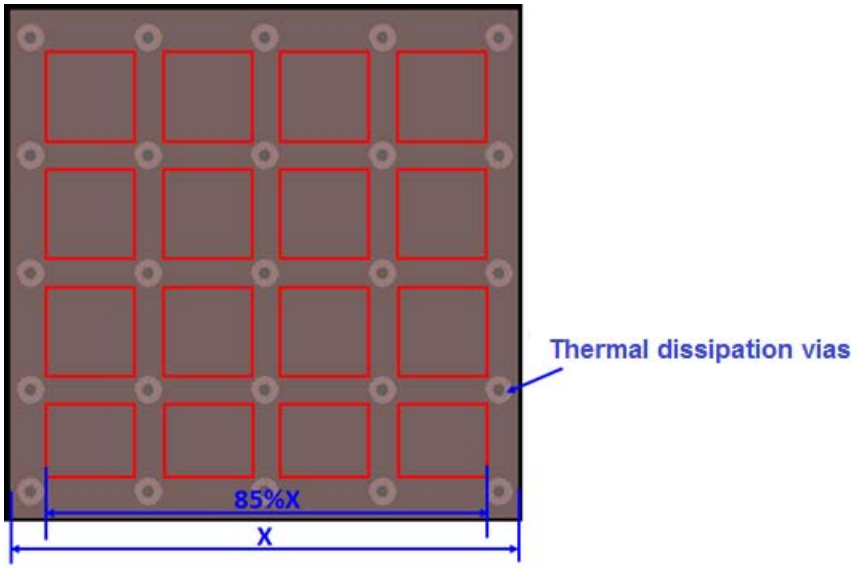
- Adopt the component ePad design scheme for the thermal pad on the PCB side.
- Ensure that the vias on the thermal pad are not too dense, and their center spacing is no less than 50 mils to reserve enough area for soldering.

2.2 Recommended Stencil Apertures

For a HiSilicon QFP chip, you are advised to design the apertures for ePad stencil as follows:

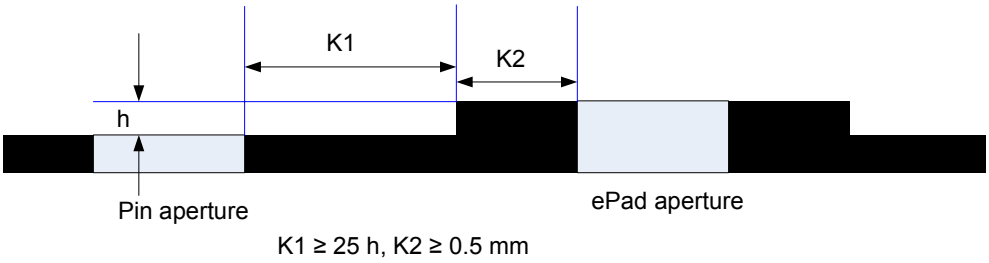
- The stencil aperture size on the PCB thermal pad is 50% to 70% of the size of the master thermal pad.
- The stencil aperture is indented inward by 15%. The spacing between the edge of the stencil aperture on the PCB thermal pad and the inner side of the pin pad must be greater than 0.2 mm. The thermal pad is split using rib network. The center of the rib overlaps with that of the vias as shown in Figure 2-1. (There is no strict requirement on the rib width, but the size requirement of the aperture should be met first if there is any.)

Figure 2-1 Schematic diagram of the stencil apertures on the QFP thermal pad



- The recommended thickness of the stencil is 0.12 mm. Partial step-up thickening can be used if the customer has a high stannum demand. The recommended step-up thickness is 0.15 mm, and the step height (*h*) should be less than 0.05 mm (0.03 mm is recommended). For the stencil design, see Figure 2-2.

Figure 2-2 Relationship between the ePad aperture and the pin aperture on the stencil



where

- h: step height of the step stencil
- K1: distance between the edge of the step-up stencil and the aperture of the adjacent stencil
- K2: distance between the aperture of the step-up stencil and the step-up edge