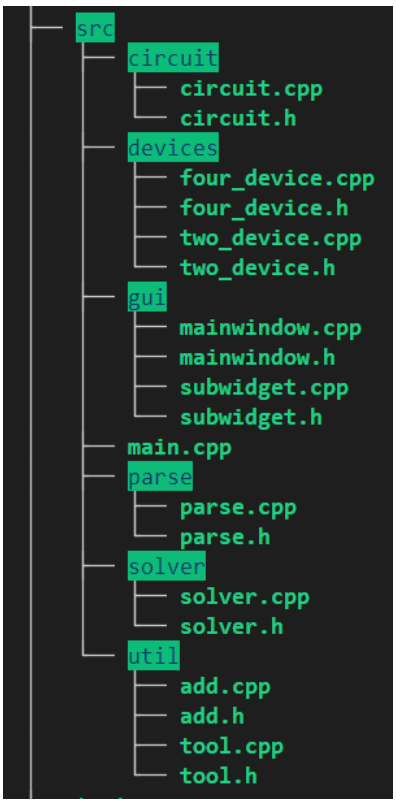
HW4_Report

1.实验概述：

相比于 HW3 的代码，按照老师的提示，代码结构改进如下：



其中 circuit 负责管理功能，它的主要成员如下：

```
file_parse *m_parser;
solver *m_solver;
vector<TwoSideDevice> two_dev_list;  //c和l仅仅是值，build_matrix的时候输入为wj,然后对于c和l乘以它
vector<FourSideDevice> four_dev_list; //c和l仅仅是值，build_matrix的时候输入为wj,然后对于c和l乘以它
//对于node,使用unordermap node2row string int
unordered_map<string, int> node2row;
```

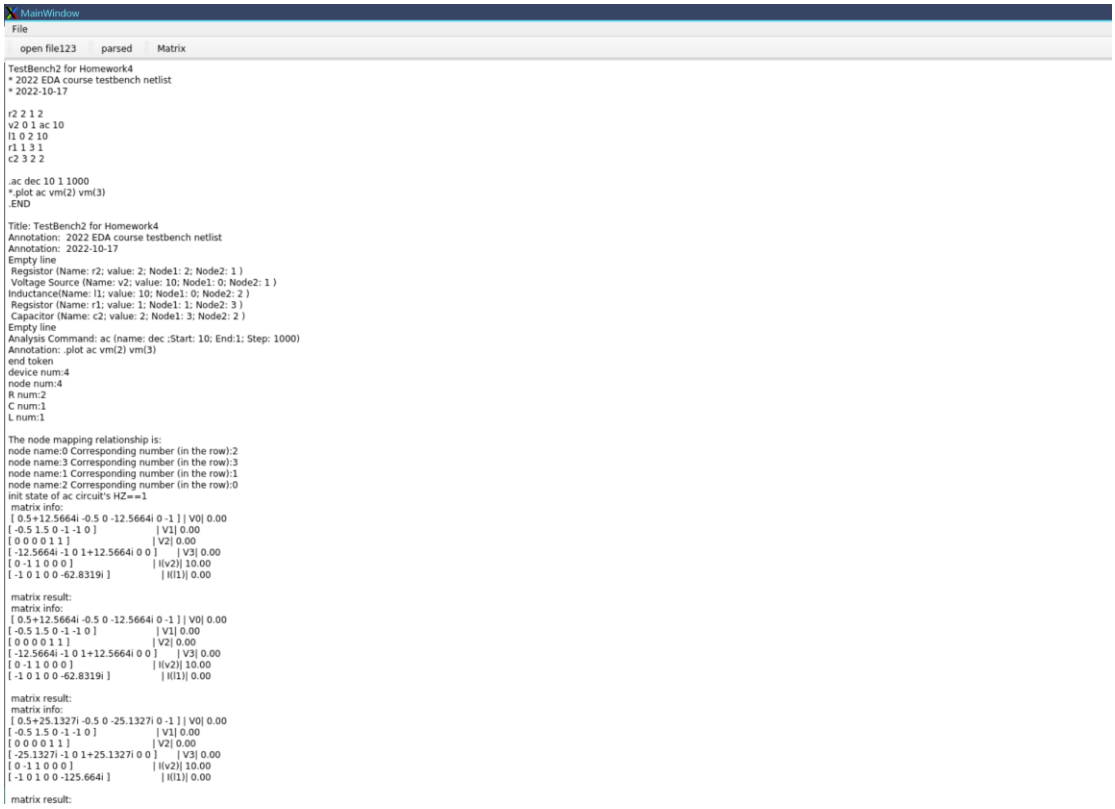
双端和四端器件的 vector，指向 parser 和 solver 的指针，一个哈希表来实现 node name 和编号（在 MNA 矩阵中的哪一行）的映射。

Circuit 会将器件队列和哈希表引用传递给 parser 和 solver 来实现信息的共享。

Parser 负责 HW3 中的网表语句解析工作，在解析的同时填充器件队列和哈希表。

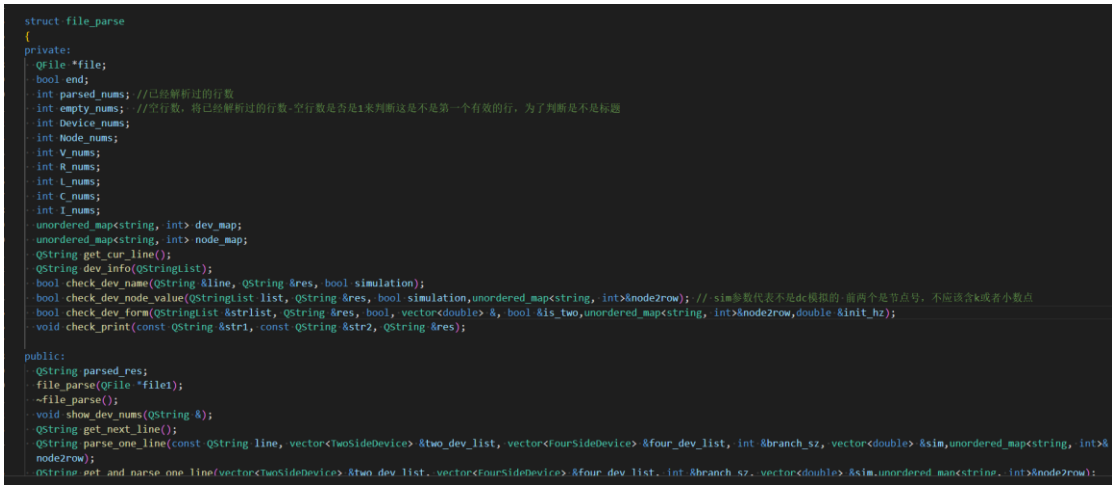
Solver 负责根据上述信息计算，构建 MNA 矩阵，LHS，RHS。

2.GUI 整体截图：

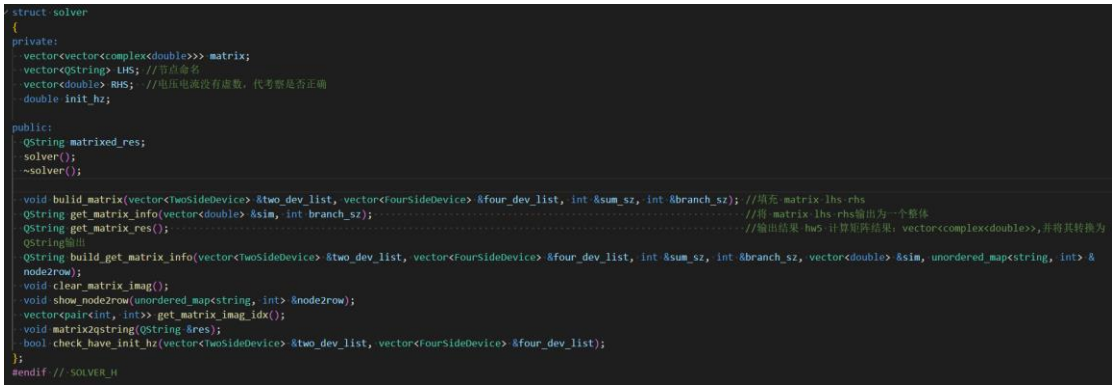


3.关键代码和结果展示:

```
struct circuit
{
private:
    bool has_parsed;
    bool has_matrixed; //这两个bool既可以在circuit中，也可以在parse和solver中，优劣势?
    //bool simulation;   //是否有类似.dc的模拟

    //bool is_dc;
    /*
    分成初始状态和模拟动态状态(针对dc，ac情况并没有初始频率，也就不打印初始matrix)
    一个电路要么是交流，要么是直流??
    dc初始矩阵:需要把虚部清除，遍历即可，不需要记录信息。
    dc模拟时:要先对dc模拟的name在LHS中匹配找到对应的行(parser中实现)，然后修改RHS中的值即可;电压电流源均适用
    ac初始矩阵:需要遍历，记录哪些位置具有虚部信息（vector<pair<int, int>>),貌似并没有初始情况，那么就直接模拟
    ac模拟时，调用写好的函数for循环乘以不同的频率即可。相比dc之所以不需要匹配LHS,是因为电路中只有一个频率，所有虚部都受到影响????
    个人认为这个二维vector不需要在circuit中记录，有点浪费空间，规模较小，遍历时间比较短，每次matrix时候重新算即可。

    以什么样的形式遍历展现到ui中,同时每个值都要计算对应时刻的结果。
    */
    file_parse *m_parser;
    solver *m_solver;
    vector<TwoSideDevice> two_dev_list;   //c和l仅仅是值，build_matrix的时候输入为wj,然后对于c和l乘以它
    vector<FourSideDevice> four_dev_list; //c和l仅仅是值，build_matrix的时候输入为wj,然后对于c和l乘以它
    //对于node,使用unordermap node2row string int
    unordered_map<string, int> node2row;
    vector<double> sim; //记录模拟的相关信息
    int sum_sz;
    int branch_sz; //r c l v i中，l和v需要开branch行 而为什么不顺序遇到 l v直接加到矩阵里，是为了和课件的矩阵形式一致? branch放在最后
```



```
struct file_parse
{
private:
  QFile *file;
  bool end;
  int parsed_nums; //已经解析过的行数
  int empty_nums;  //空行数，将已经解析过的行数-空行数是否是1来判断这是不是第一个有效的行，为了判断是不是标题
  int Device_nums;
  int Node_nums;
  int V_nums;
  int R_nums;
  int L_nums;
  int C_nums;
  int I_nums;
  unordered_map<string, int> dev_map;
  unordered_map<string, int> node_map;
  QString get_cur_line();
  QString dev_info(QStringList);
  bool check_dev_name(QString &line, QString &res, bool simulation);
  bool check_dev_node_value(QStringList list, QString &res, bool simulation,unordered_map<string, int>&node2row);// sim参数代表不是dc模拟的 前两个是节点号，不应该含k或者小数点
  bool check_dev_form(QStringList &strlist, QString &res, bool, vector<double> &, bool &is_two,unordered_map<string, int>&node2row,double &init_hz);
  void check_print(const QString &str1, const QString &str2, QString &res);

public:
  QString parsed_res;
  file_parse(QFile *file1);
  ~file_parse();
  void show_dev_nums(QString &);
  QString get_next_line();
  QString parse_one_line(const QString line, vector<TwoSideDevice> &two_dev_list, vector<FourSideDevice> &four_dev_list, int &branch_sz, vector<double> &sim,unordered_map<string, int>&
  node2row);
  QString get_and_parse_one_line(vector<TwoSideDevice> &two_dev_list, vector<FourSideDevice> &four_dev_list, int &branch_sz, vector<double> &sim,unordered_map<string, int>&node2row);
```



```
struct solver
{
private:
  vector<vector<complex<double>>> matrix;
  vector<QString> LHS; //节点命名
  vector<double> RHS;  //电压电流没有虚数，代考察是否正确
  double init_hz;

public:
  QString matrixed_res;
  solver();
  ~solver();

  void bulid_matrix(vector<TwoSideDevice> &two_dev_list, vector<FourSideDevice> &four_dev_list, int &sum_sz, int &branch_sz); //填充 matrix lhs rhs
  QString get_matrix_info(vector<double> &sim, int branch_sz);                                                                //将 matrix lhs rhs输出为一个整体
  QString get_matrix_res();                                                                                                   //输出结果 hw5 计算矩阵结果：vector<complex<double>>,并将其转换为
  QString输出
  QString build_get_matrix_info(vector<TwoSideDevice> &two_dev_list, vector<FourSideDevice> &four_dev_list, int &sum_sz, int &branch_sz, vector<double> &sim, unordered_map<string, int> &
  node2row);
  void clear_matrix_imag();
  void show_node2row(unordered_map<string, int> &node2row);
  vector<pair<int, int>> get_matrix_imag_idx();
  void matrix2qstring(QString &res);
  bool check_have_init_hz(vector<TwoSideDevice> &two_dev_list, vector<FourSideDevice> &four_dev_list);
};
#endif // SOLVER_H
```

实现了多次点击 parse 和 matrix 的缓冲功能，只计算一次：

```
}
QString circuit::get_parse_res() //不支持修改的话，就做一个缓存，只parse一次
{
    if (has_parsed)
        return m_parser->parsed_res;
    else
    {
        has_parsed = true;
        return m_parser->parse(two_dev_list, four_dev_list, sum_sz, branch_sz, sim, node2row);
    }
}

QString circuit::get_matrix_res()
{
    if (has_parsed)
    {
        if (has_matrixed)
            return m_solver->matrixed_res;
        else
        {
            has_matrixed = true;
            return m_solver->build_get_matrix_info(two_dev_list, four_dev_list, sum_sz, branch_sz, sim, node2row);
        }
    }
```

Testbench1:

```
Title: TestBench1 for Homework4
Annotation:  2022 EDA course testbench netlist
Annotation:  2022-10-17
Empty line
 Voltage Source (Name: Vin; value: 3; Node1: 1; Node2: 0 )
 Regsistor (Name: R1; value: 200; Node1: 1; Node2: 2 )
 Capacitor (Name: C1; value: 20p; Node1: 1; Node2: 2 )
 Regsistor (Name: R2; value: 100; Node1: 2; Node2: 0 )
Inductance(Name: L1; value: 10m; Node1: 2; Node2: 0 )
Empty line
Analysis Command: DC (name: Vin ;Start: 1; End:2; Step: 0.1)
end token
device num:4
node num:3
R num:2
C num:1
L num:1

The node mapping relationship is:
node name:2 Corresponding number (in the row):2
node name:0 Corresponding number (in the row):1
node name:1 Corresponding number (in the row):0
matrix info:
 [ 0.005 0 -0.005 1 0 ]      | V0| 0.00
[ 0 0.01 -0.01 -1 -1 ]      | V1| 0.00
[ -0.005 -0.01 0.015 0 1 ] | V2| 0.00
[ 1 -1 0 0 0 ]              | I(Vin)| 3.00
[ 0 -1 1 0 0 ]              | I(L1)| 0.00

 matrix result:
 matrix info:
 [ 0.005 0 -0.005 1 0 ]      | V0| 0.00
[ 0 0.01 -0.01 -1 -1 ]      | V1| 0.00
[ -0.005 -0.01 0.015 0 1 ] | V2| 0.00
[ 1 -1 0 0 0 ]              | I(Vin)| 1.00
[ 0 -1 1 0 0 ]              | I(L1)| 0.00

 matrix result:
 matrix info:
 [ 0.005 0 -0.005 1 0 ]      | V0| 0.00
[ 0 0.01 -0.01 -1 -1 ]      | V1| 0.00
[ -0.005 -0.01 0.015 0 1 ] | V2| 0.00
[ 1 -1 0 0 0 ]              | I(Vin)| 1.10
[ 0 -1 1 0 0 ]              | I(L1)| 0.00

 matrix result:
 matrix info:
 [ 0.005 0 -0.005 1 0 ]      | V0| 0.00
[ 0 0.01 -0.01 -1 -1 ]      | V1| 0.00
[ -0.005 -0.01 0.015 0 1 ] | V2| 0.00
[ 1 -1 0 0 0 ]              | I(Vin)| 1.20
[ 0 -1 1 0 0 ]              | I(L1)| 0.00
```

Testbench2:

```
Title: TestBench2 for Homework4
Annotation:  2022 EDA course testbench netlist
Annotation:  2022-10-17
Empty line
 Regsistor (Name: r2; value: 2; Node1: 2; Node2: 1 )
 Voltage Source (Name: v2; value: 10; Node1: 0; Node2: 1 )
Inductance(Name: l1; value: 10; Node1: 0; Node2: 2 )
 Regsistor (Name: r1; value: 1; Node1: 1; Node2: 3 )
 Capacitor (Name: c2; value: 2; Node1: 3; Node2: 2 )
Empty line
Analysis Command: ac (name: dec ;Start: 1; End:1000; Step: 10)
Annotation: .plot ac vm(2) vm(3)
end token
device num:4
node num:4
R num:2
C num:1
L num:1

The node mapping relationship is:
node name:0 Corresponding number (in the row):2
node name:3 Corresponding number (in the row):3
node name:1 Corresponding number (in the row):1
node name:2 Corresponding number (in the row):0
init state of ac circuit's HZ==1
 matrix info:
 [ 0.5+12.5664i -0.5 0 -12.5664i 0 -1 ] | V0| 0.00
[ -0.5 1.5 0 -1 -1 0 ]                  | V1| 0.00
[ 0 0 0 0 1 1 ]                        | V2| 0.00
[ -12.5664i -1 0 1+12.5664i 0 0 ]      | V3| 0.00
[ 0 -1 1 0 0 0 ]                       | I(v2)| 10.00
[ -1 0 1 0 0 -62.8319i ]                | I(l1)| 0.00

 matrix result:
 matrix info:
 [ 0.5+12.5664i -0.5 0 -12.5664i 0 -1 ] | V0| 0.00
[ -0.5 1.5 0 -1 -1 0 ]                  | V1| 0.00
[ 0 0 0 0 1 1 ]                        | V2| 0.00
[ -12.5664i -1 0 1+12.5664i 0 0 ]      | V3| 0.00
[ 0 -1 1 0 0 0 ]                       | I(v2)| 10.00
[ -1 0 1 0 0 -62.8319i ]                | I(l1)| 0.00

 matrix result:
 matrix info:
 [ 0.5+25.1327i -0.5 0 -25.1327i 0 -1 ] | V0| 0.00
[ -0.5 1.5 0 -1 -1 0 ]                  | V1| 0.00
[ 0 0 0 0 1 1 ]                        | V2| 0.00
[ -25.1327i -1 0 1+25.1327i 0 0 ]      | V3| 0.00
[ 0 -1 1 0 0 0 ]                       | I(v2)| 10.00
[ -1 0 1 0 0 -125.664i ]                | I(l1)| 0.00
```

每次的增量从一开始的 10，到 100，到 1000：

[-1 0 1 0 0 -5026.55i] | I(I1)| 0.00

matrix result:
matrix info:
[0.5+1130.97i -0.5 0 -1130.97i 0 -1] | V0| 0.00
[-0.5 1.5 0 -1 -1 0] | V1| 0.00
[0 0 0 0 1 1] | V2| 0.00
[-1130.97i -1 0 1+1130.97i 0 0] | V3| 0.00
[0 -1 1 0 0 0] | I(v2)| 10.00
[-1 0 1 0 0 -5654.87i] | I(I1)| 0.00

matrix result:
matrix info:
[0.5+1256.64i -0.5 0 -1256.64i 0 -1] | V0| 0.00
[-0.5 1.5 0 -1 -1 0] | V1| 0.00
[0 0 0 0 1 1] | V2| 0.00
[-1256.64i -1 0 1+1256.64i 0 0] | V3| 0.00
[0 -1 1 0 0 0] | I(v2)| 10.00
[-1 0 1 0 0 -6283.19i] | I(I1)| 0.00

matrix result:
matrix info:
[0.5+2513.27i -0.5 0 -2513.27i 0 -1] | V0| 0.00
[-0.5 1.5 0 -1 -1 0] | V1| 0.00
[0 0 0 0 1 1] | V2| 0.00
[-2513.27i -1 0 1+2513.27i 0 0] | V3| 0.00
[0 -1 1 0 0 0] | I(v2)| 10.00
[-1 0 1 0 0 -12566.4i] | I(I1)| 0.00

matrix result:
matrix info:
[0.5+3769.91i -0.5 0 -3769.91i 0 -1] | V0| 0.00
[-0.5 1.5 0 -1 -1 0] | V1| 0.00
[0 0 0 0 1 1] | V2| 0.00
[-3769.91i -1 0 1+3769.91i 0 0] | V3| 0.00
[0 -1 1 0 0 0] | I(v2)| 10.00
[-1 0 1 0 0 -18849.6i] | I(I1)| 0.00

matrix result:

Testbench3:

```
Title: TestBench3 for Homework4
Annotation:  2022-10-17
Annotation:  Origin: Lecture 6 Circuit III Page-14
Empty line
 Regsistor (Name: R1; value: 5; Node1: 1; Node2: 0 )
FourSideDevice,lazy to parse it
 Regsistor (Name: R3; value: 6; Node1: 1; Node2: 2 )
 Regsistor (Name: R4; value: 8; Node1: 2; Node2: 0 )
I Source (Name: Is; value: 10; Node1: 0; Node2: 2 )
 Voltage Source (Name: Vs; value: 1; Node1: 3; Node2: 2 )
 Regsistor (Name: R8; value: 5; Node1: 3; Node2: 4 )
FourSideDevice,lazy to parse it
Analysis Command: DC (name: VS ;Start: 1; End:2; Step: 0.1)
end token
device num:6
node num:5
R num:4
C num:0
L num:0

The node mapping relationship is:
node name:4 Corresponding number (in the row):4
node name:2 Corresponding number (in the row):2
node name:0 Corresponding number (in the row):1
node name:3 Corresponding number (in the row):3
node name:1 Corresponding number (in the row):0
matrix info:
 [ 2.36667 -0.2 -2.16667 0 0 0 0 ]      | V0| 0.00
[ -2.2 0.325 1.875 0 0 0 -1 ]          | V1| -10.00
[ -0.166667 -0.125 0.291667 0 0 -1 0 ] | V2| 10.00
[ 0 0 0 0.2 -0.2 1 0 ]                 | V3| 0.00
[ 0 0 0 -0.2 0.2 0 1 ]                 | V4| 0.00
[ 0 0 -1 1 0 0 0 ]                     | I(Vs)| 1.00
[ -13 -1 13 0 1 0 0 ]                  | I(E7)| 0.00

 matrix result:
 matrix info:
 [ 2.36667 -0.2 -2.16667 0 0 0 0 ]      | V0| 0.00
[ -2.2 0.325 1.875 0 0 0 -1 ]          | V1| -10.00
[ -0.166667 -0.125 0.291667 0 0 -1 0 ] | V2| 10.00
[ 0 0 0 0.2 -0.2 1 0 ]                 | V3| 0.00
[ 0 0 0 -0.2 0.2 0 1 ]                 | V4| 0.00
[ 0 0 -1 1 0 0 0 ]                     | I(Vs)| 1.00
[ -13 -1 13 0 1 0 0 ]                  | I(E7)| 0.00

 matrix result:
 matrix info:
 [ 2.36667 -0.2 -2.16667 0 0 0 0 ]      | V0| 0.00
[ -2.2 0.325 1.875 0 0 0 -1 ]          | V1| -10.00
[ -0.166667 -0.125 0.291667 0 0 -1 0 ] | V2| 10.00
[ 0 0 0 0.2 -0.2 1 0 ]                 | V3| 0.00
[ 0 0 0 -0.2 0.2 0 1 ]                 | V4| 0.00
[ 0 0 -1 1 0 0 0 ]                     | I(Vs)| 1.10
[ -13 -1 13 0 1 0 0 ]                  | I(E7)| 0.00
```

Testbench4:

```
Title: TestBench4 for Homework4
Annotation:  2022 EDA course testbench netlist
Annotation:  2022-10-17
Annotation:  Origin: From Qixu Xie's Small Signal Model - AC Test
Annotation:  Origin: node□□□□□□□□□□□□
Annotation:  vin meg
 Voltage Source (Name: Vin; value: 0; Node1: in; Node2: gnd )
 Capacitor (Name: Cin; value: 1p; Node1: in; Node2: gnd )
Empty line
Annotation: first stage
FourSideDevice,lazy to parse it
 Regsistor (Name: R1; value: 0.75Meg; Node1: out1; Node2: gnd )
 Capacitor (Name: C1; value: 619f; Node1: out1; Node2: gnd )
Empty line
Annotation: compensation capacitor
 Capacitor (Name: Cc; value: 1p; Node1: out1; Node2: out2 )
Empty line
Annotation: second stage
FourSideDevice,lazy to parse it
 Regsistor (Name: R2; value: 99.47K; Node1: out2; Node2: gnd )
 Capacitor (Name: C2; value: 5p; Node1: out2; Node2: gnd )
Empty line
Analysis Command: AC (name: DEC ;Start: 1; End:1000Meg; Step: 10)
Annotation: .plot ac vdec(out2) vp(out2)
end token
device num:8
node num:4
R num:2
C num:4
L num:0

The initial frequency of the circuit is: 1.00
The node mapping relationship is:
node name:out1 Corresponding number (in the row):2
node name:out2 Corresponding number (in the row):3
node name:gnd Corresponding number (in the row):1
node name:in Corresponding number (in the row):0
init state of ac circuit's HZ==1
 matrix info:
[ 6.28319e-12i -6.28319e-12i 0 0 1 ]                                          | V0| 0.00
[ -160.6-6.28319e-12i 1156.93+3889.29i -996.333-3889.29i -1.00533e-05-3.14159e-11i -1 ] | V1| 0.00
[ 160.6 -161.933-3889.29i 1.33333+3889.29i -6.28319e-12i 0 ]                    | V2| 0.00
[ 0 -995-3.14159e-11i 995-6.28319e-12i 1.00533e-05+3.76991e-11i 0 ]             | V3| 0.00
[ 1 -1 0 0 0 ]                                                        | I(Vin)| 0.00

 matrix result:
 matrix info:
[ 6.28319e-12i -6.28319e-12i 0 0 1 ]                                          | V0| 0.00
[ -160.6-6.28319e-12i 1156.93+3889.29i -996.333-3889.29i -1.00533e-05-3.14159e-11i -1 ] | V1| 0.00
[ 160.6 -161.933-3889.29i 1.33333+3889.29i -6.28319e-12i 0 ]                    | V2| 0.00
[ 0 -995-3.14159e-11i 995-6.28319e-12i 1.00533e-05+3.76991e-11i 0 ]             | V3| 0.00
[ 1 -1 0 0 0 ]                                                        | I(Vin)| 0.00

 matrix result:
 matrix info:
[ 1.25664e-11i -1.25664e-11i 0 0 1 ]                                          | V0| 0.00
[ -160.6-1.25664e-11i 1156.93+7778.58i -996.333-7778.58i -1.00533e-05-6.28319e-11i -1 ] | V1| 0.00
[ 160.6 -161.933-7778.58i 1.33333+7778.58i -1.25664e-11i 0 ]                    | V2| 0.00
[ 0 -995-6.28319e-11i 995-1.25664e-11i 1.00533e-05+7.53982e-11i 0 ]             | V3| 0.00
[ 1 -1 0 0 0 ]                                                        | I(Vin)| 0.00

 matrix result:
 matrix info:
[ 1.88496e-11i -1.88496e-11i 0 0 1 ]                                          | V0| 0.00
```

遇到的一些问题:

按照不同的文件夹进行组织代码，比如说 circuit/circuit.h 中需要 include<device.h>，那么需要../device/device.h，通过在 pro 文件中 INCLUDEPATH +=./src 解决；

cout 有时候有问题，该为 qDebug()（深层原因是 qdebug 自带换行）；

circuit，parser 和 solver 之间的信息共享，最后通过引用传递实现，可能会有更合适的方式。