

# Lab1

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A1 架构:

Matlab 实现:

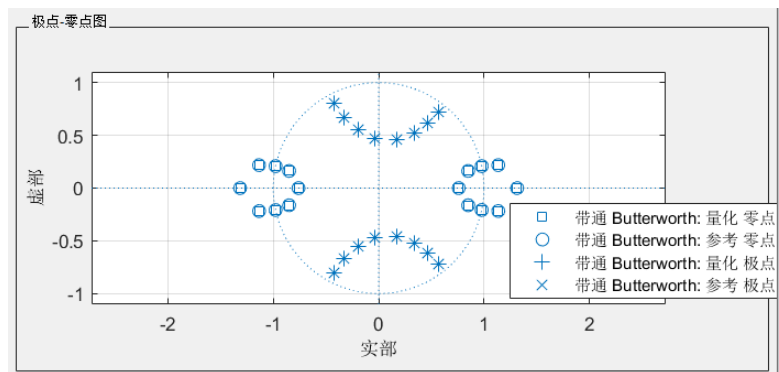


图 1 零极点分布图

滤波器算法: 定点

系数 字长: 16 ☐ 最佳精度小数长度

☒ 分子 小数长度: 8 ☒ 定标值 小数长度: 11

☐ 分子 范围 (+/-): 16 ☐ 定标值 范围 (+/-): 16

☒ 分母 小数长度: 8

☐ 分母 范围 (+/-): 16

应用

图 2 抽头系数

```
节 #1
-----
量化 分子:
0100
0000
fe45
量化 分母:
0100
0015
003a
量化 增益:
0006
节 #2
-----
量化 分子:
0100
0000
ff6c
量化 分母:
0100
```

图 3 部分参数

响应类型 <input type="radio"/> 低通 <input type="radio"/> 高通 <input checked="" type="radio"/> 带通 <input type="radio"/> 带阻 <input type="radio"/> 微分器 设计方法 <input checked="" type="radio"/> IIR Buttenworth <input type="radio"/> FIR 等波纹	滤波器阶数 <input type="radio"/> 指定阶: 10 <input checked="" type="radio"/> 最小阶 选项 完全匹配: 阻带	频率设定 单位: MHz Fs: 10 Fstop1: 0.5 Fpass1: 1.5 Fpass2: 3.2 Fstop2: 4	幅值设定 单位: dB Astop1: 60 Apass: 1 Astop2: 60
---	--	---	--

图 4 滤波器设置

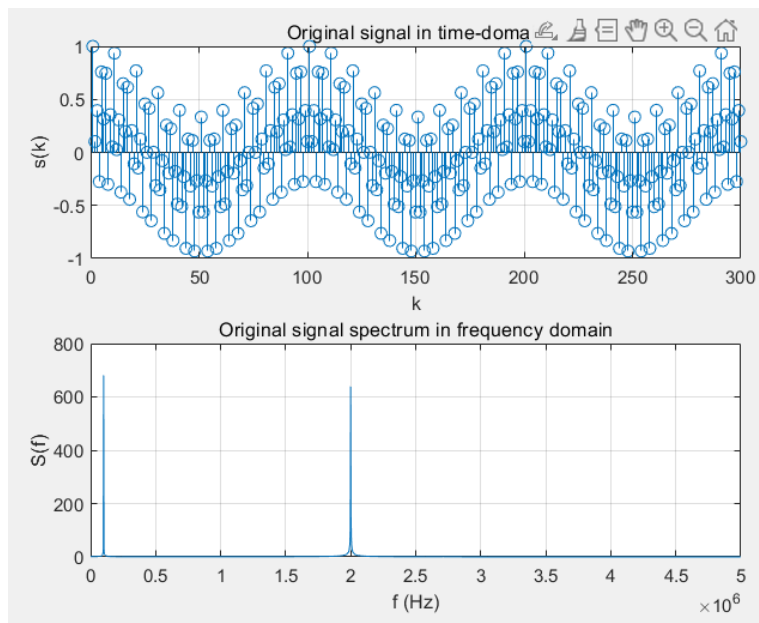


图 5 matlab 仿真结果（滤波前）

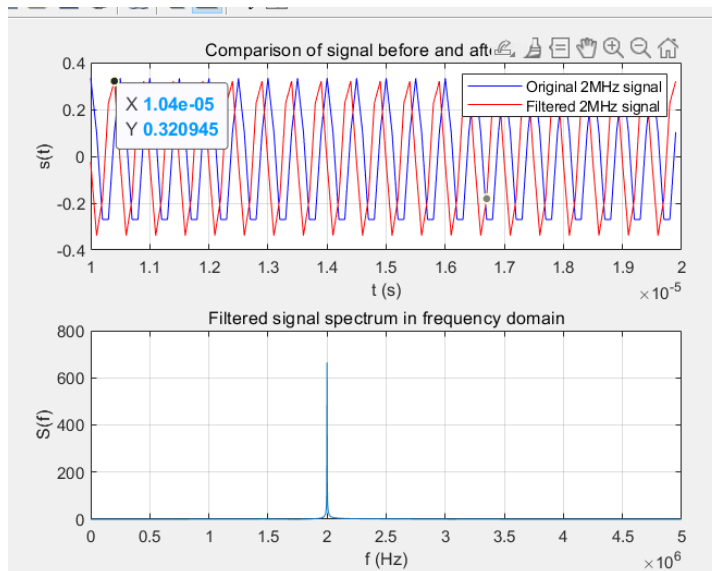
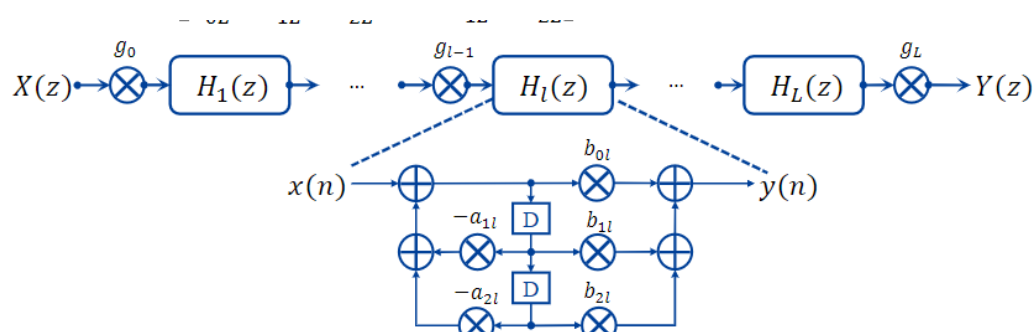


图 6 matlab 仿真（滤波后）

优化前的 IIR 滤波器电路图 A1: (直接 II 型, 八节二阶节)



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(需要注意的是, 为了满足 60Mhz 的频率要求, 在第四和第五节之间插入寄存器 (流水线):

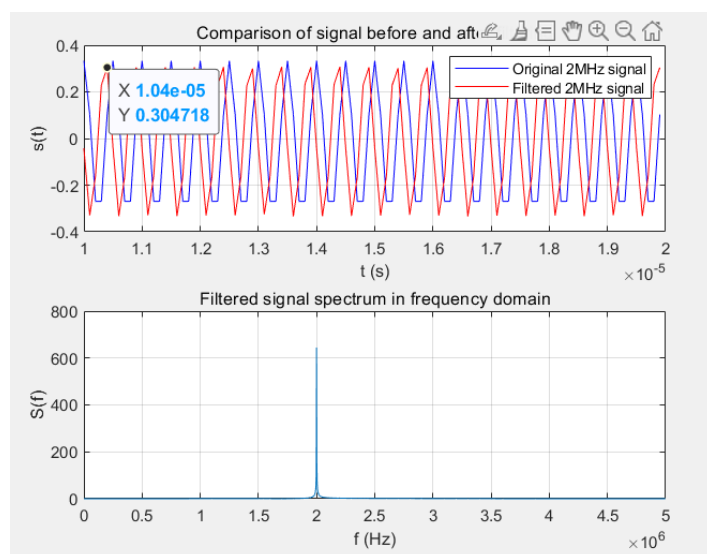
```
pe pe1(.in(pp1_1),.a1(a1_0),.a2(a1_1),.b1(b1_1),.b2(b1_2),.out(out_1),.clk(clk),.rst(rst));
pe pe2(.in(out_1),.a1(a2_0),.a2(a2_1),.b1(b2_1),.b2(b2_2),.out(out_2),.clk(clk),.rst(rst));
pe pe3(.in(out_2),.a1(a3_0),.a2(a3_1),.b1(b3_1),.b2(b3_2),.out(out_3),.clk(clk),.rst(rst));
pe pe4(.in(out_3),.a1(a4_0),.a2(a4_1),.b1(b4_1),.b2(b4_2),.out(out_4),.clk(clk),.rst(rst));
pe pe5(.in(pp1_4),.a1(a5_0),.a2(a5_1),.b1(b5_1),.b2(b5_2),.out(out_5),.clk(clk),.rst(rst));
pe pe6(.in(out_5),.a1(a6_0),.a2(a6_1),.b1(b6_1),.b2(b6_2),.out(out_6),.clk(clk),.rst(rst));
pe pe7(.in(out_6),.a1(a7_0),.a2(a7_1),.b1(b7_1),.b2(b7_2),.out(out_7),.clk(clk),.rst(rst));
pe pe8(.in(out_7),.a1(a8_0),.a2(a8_1),.b1(b8_1),.b2(b8_2),.out(out_8),.clk(clk),.rst(rst));
fixpmul fixpmul_10(.a(pp1_0),.b(gm),.o(out_0));
always@(posedge clk or negedge rst)
```

如图所示 ppl\_4 为寄存器类型, 其他的 out\_\* 为 wire 类型, 直接组合逻辑连接。

Verilog 验证结果:

```
lab1 > src > Verilog > result.txt
1 000000c0
2 000000a4
3 fffff9a6
4 fffffa30
5 000017d8
6 000017e0
7 fffffc90
8 fffffc5b
9 000042c2
10 00005e43
11 fffffd44
12 fffff9c21
13 fffffee30
14 00003be9
15 00004c6f
16 000056a
17 fffffa148
```

将结果作为输入, 用 matlab 显示波形, 结果为:



可以看到和初始用 matlab 模拟的结果一致, 因此 verilog 仿真正确 (之后的仿真结果

只需要和这个 result.txt 对比，如果一致那么也一样可以说明仿真成功，并不需要单独写 testbench)

Vivado 结果：

Synthesize:

频率：最低要求为 60Mhz，周期为 16.67ns，可见 16ns 满足要求。

The screenshot shows the Vivado IDE interface. The 'Timing Constraints' window is open, displaying a table with columns: Position, Clock Name, Period (ns), Rise At (ns), Fall At (ns), Add Clock, Source Objects, Source File, Scoped Cell, and Current Instance. A single constraint is listed: 1, clk, 16.000, 0.000, 8.000, [get\_ports clk], ~unsaved co. Below this, the 'All Constraints' section shows the command: create\_clock -period 16.000 -name clk -waveform [0.000 8.000] [get\_ports clk].

The 'Design Timing Summary' report is also visible, showing various timing metrics:

Setup	Hold	Pulse Width
Worst Negative Slack (NMS): 1.163 ns	Worst Hold Slack (HMS): 0.083 ns	Worst Pulse Width Slack (PPWS): 7.650 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 737	Total Number of Endpoints: 737	Total Number of Endpoints: 647

All user specified timing constraints are met.

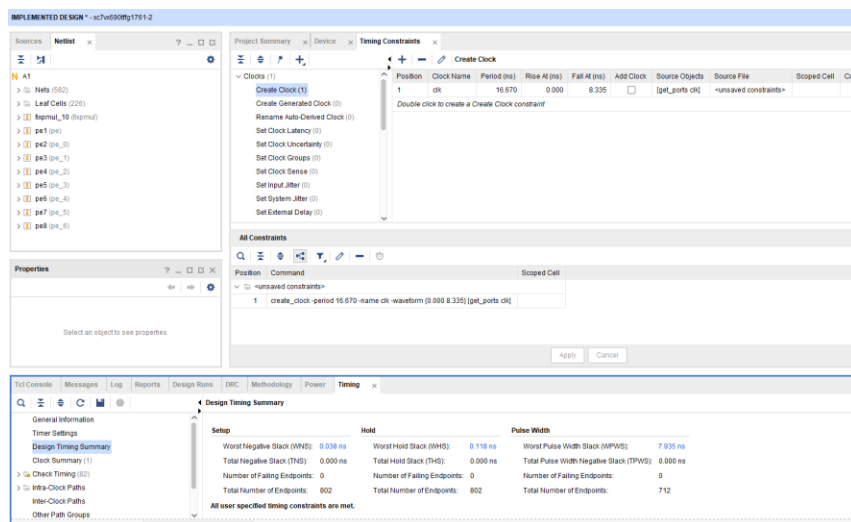
资源情况：

The screenshot shows the 'Utilization' report in the Vivado IDE. The report is organized into a hierarchy of components, with a table showing the resource usage for each component.

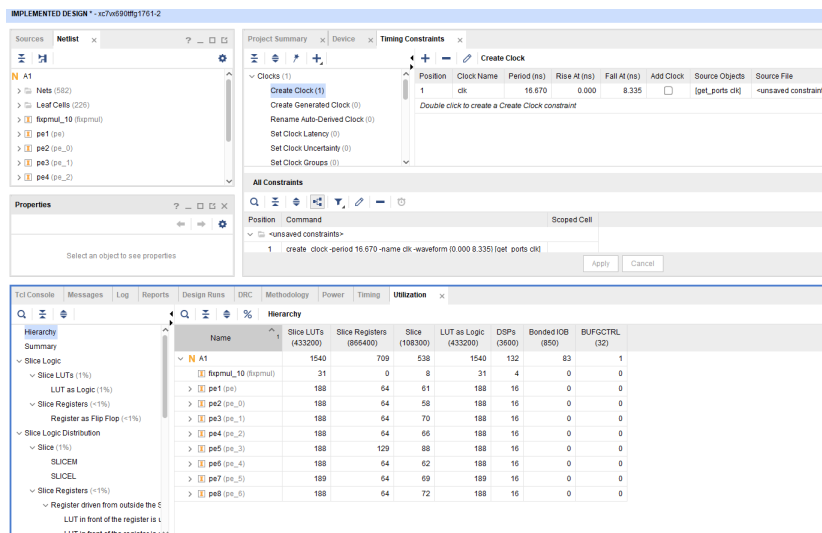
Name	Slice LUTs (43200)	Slice Registers (86640)	DSPs (3600)	Bonded IOB (850)	BUFCTRL (32)
A1	1540	644	132	83	1
flpmul_10 (flpmul)	31	0	4	0	0
pe1 (pe)	188	64	16	0	0
pe2 (pe_0)	188	64	16	0	0
pe3 (pe_1)	188	64	16	0	0
pe4 (pe_2)	188	64	16	0	0
pe5 (pe_3)	188	64	16	0	0
pe6 (pe_4)	188	64	16	0	0
pe7 (pe_5)	189	64	16	0	0
pe8 (pe_6)	188	64	16	0	0

Implemente:

频率：



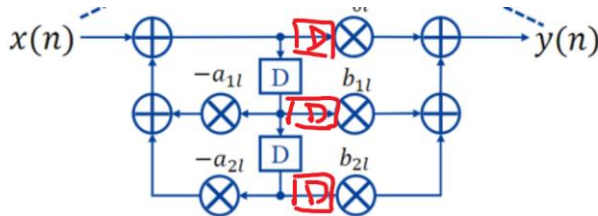
资源：



A2 架构:

优化后的 （频率为 1/2）

在 8 个处理单元间插入 reg，并在每个 pe 中设置一级流水线（A2 架构）  
（也即插入流水线来减小关键路径，提高频率）



对应代码中的 buffer0,buffer1,buffer2:

```

always@(posedge clk or negedge rst)
begin
    if(!rst)
    begin
        reg1<=0;reg2<=0; buffer0<=0;buffer1<=0;buffer2<=0;result<=0;
    end
    else
    begin
        buffer0<=in_in_1;
        buffer1<=reg1;
        buffer2<=reg2;
        reg1<=in_in_1;
        reg2<=reg1;
        result<=out;
    end
end

```

Vivado 结果:

Synthesize:

频率:

可见频率为 7.5ns,符合小于一半的要求。

The top screenshot shows the 'Timing Constraints' window in Vivado. It displays a table with columns: Position, Clock Name, Period (ns), Rise At (ns), Fall At (ns), Add Clock, Source Objects, Source File, Scoped Cell, and Current Instance. A single constraint is listed: '1 clk 7.500 0.000 3.750'. Below this, the 'All Constraints' section shows the command 'create\_clock -period 7.500 -name clk -waveform {0.000 3.750} [get\_ports clk]'. The bottom screenshot shows the 'Design Timing Summary' window. It provides a detailed overview of timing metrics, including Setup, Hold, and Pulse Width constraints, and a summary of the design's performance.

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	clk	7.500	0.000	3.750	<input type="checkbox"/>	[get_ports clk]	unsaved.co		

Position	Command	Scoped Cell
1	create_clock -period 7.500 -name clk -waveform {0.000 3.750} [get_ports clk]	

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.154 ns	Worst Hold Slack (WHS): 0.066 ns	Worst Pulse Width Negative Slack (WPWS): 3.400 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Falling Endpoints: 0	Number of Falling Endpoints: 0	Number of Falling Endpoints: 0
Total Number of Endpoints: 1217	Total Number of Endpoints: 1217	Total Number of Endpoints: 1128

All user specified timing constraints are met.

资源:

The screenshot shows the 'Utilization' window in Vivado, displaying a hierarchy of resources used in the design. The resources are categorized into Slice Logic, Slice Registers, Memory, DSP, IO and GT Specific, Bonded IOB, Clocking, Specific Feature, and Primitives. The utilization is summarized in a table below.

Name	Slice LUTs (433200)	Slice Registers (866400)	DSPs (3600)	Bonded IOB (850)	BUFGCTRL (32)
N A2	1540	1125	132	83	1
fixpmul_10 (fixpmul)	31	0	4	0	0
pe1 (pe)	188	128	16	0	0
pe2 (pe_0)	188	128	16	0	0
pe3 (pe_1)	188	128	16	0	0
pe4 (pe_2)	188	128	16	0	0
pe5 (pe_3)	188	128	16	0	0
pe6 (pe_4)	188	128	16	0	0
pe7 (pe_5)	189	128	16	0	0
pe8 (pe_6)	188	128	16	0	0

Implemente:

频率：可见其频率略比 Synthesize 的高， 猜测可能是物理实现比 Synthesize 多考虑了一些细节，比如连线的长度影响延迟。

The screenshot shows the Xilinx Vivado IDE interface. The top panel displays the 'Timing Constraints' window, which includes a 'Create Clock' section with a table for clock parameters and a list of constraints. The bottom panel shows the 'Design Timing Summary' window, which provides a detailed overview of the timing analysis results.

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped C
1	clk	8.000	0.000	4.000	<input type="checkbox"/>	[pe_ports clk]	<unsaved constraints>	

Double click to create a Create Clock constraint

**All Constraints**

Position	Command	Scoped Cell
1	create_clock -period 8.000 -name clk -waveform (0.000 4.000) [pe_ports clk]	

Apply Cancel

**Design Timing Summary**

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (82)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

Setup

Hold

Pulse Width

Worst Negative Slack (WNS): 0.467 ns

Worst Hold Slack (WHS): 0.145 ns

Worst Pulse Width Slack (WPWS): 3.600 ns

Total Negative Slack (TNS): 0.000 ns

Total Hold Slack (THS): 0.000 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Total Number of Endpoints: 1283

Total Number of Endpoints: 1283

Total Number of Endpoints: 1194

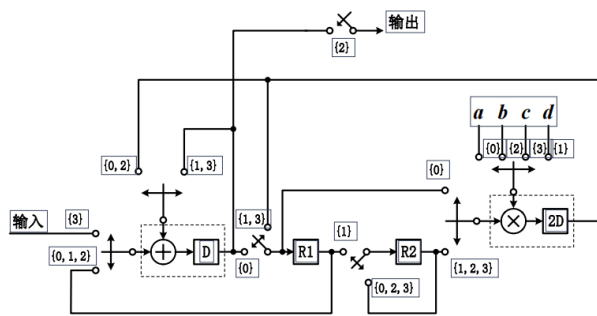
All user specified timing constraints are met.

资源：

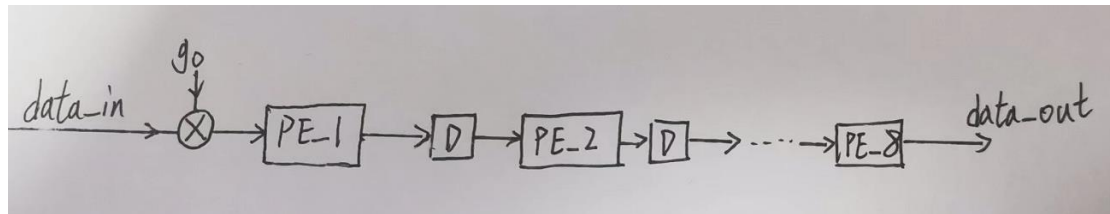
The screenshot shows the Xilinx Vivado IDE interface. The top panel displays the 'Utilization' window, which provides a detailed overview of the resource utilization for the design. The bottom panel shows the 'Hierarchy' window, which displays the design hierarchy and the utilization of resources across different components.

Name	Slice LUTs (433200)	Slice Registers (866400)	Slice (108300)	LUT as Logic (433200)	DSPs (3600)	Bonded IOB (850)	BUFGCTRL (32)
A1	1540	709	538	1540	132	83	1
fxpmul_10 (fxpmul)	31	0	8	31	4	0	0
pe1 (pe)	188	64	61	188	16	0	0
pe2 (pe_0)	188	64	58	188	16	0	0
pe3 (pe_1)	188	64	70	188	16	0	0
pe4 (pe_2)	188	64	66	188	16	0	0
pe5 (pe_3)	188	129	88	188	16	0	0
pe6 (pe_4)	188	64	62	188	16	0	0
pe7 (pe_5)	189	64	69	189	16	0	0
pe8 (pe_6)	188	64	72	188	16	0	0

A3 架构：

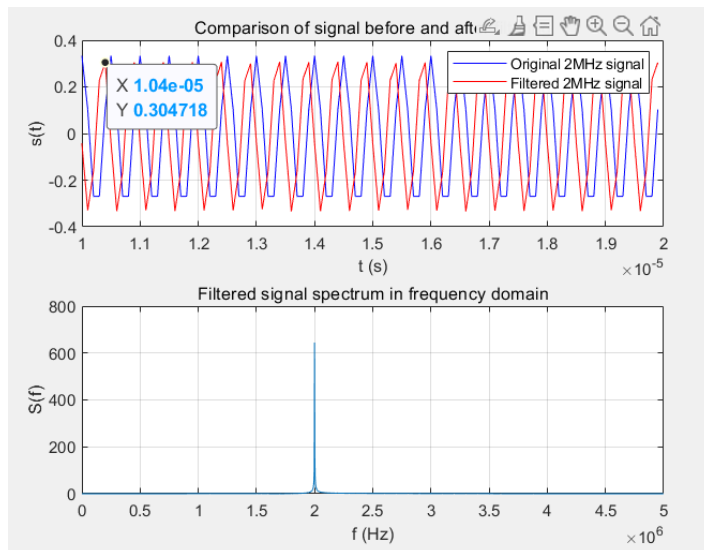


A3\_pe:



A3\_pe 是对 A1\_pe 进行折叠后得到的结果，在相邻 pe 之间存在寄存器，来优化时钟周期，同时使结构满足时序。

将 Rtl 代码得到的结果作为输入，用 matlab 显示波形，结果为：



可以看到和初始用 matlab 模拟的结果一致，因此 verilog 仿真正确

Vivado 结果：

Synthesize:

频率：

可见其甚至比提高频率的 A2 架构更快。



SYNTHESIZED DESIGN \*-xc7v6900fpg1761-2

Sources Netlist x Project Summary x Device x Timing Constraints x

Netlist

- N A3
  - Nets (877)
  - Leaf Cells (423)
    - flpmul\_10 (flpmul)
    - pe1 (A3\_pe\_0)
    - pe2 (A3\_pe\_1)
    - pe3 (A3\_pe\_2)

Properties

Select an object to see properties

Timing Constraints

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	clk	6.000	0.000	3.000	<input type="checkbox"/>	[get_ports clk]	<unsaved co		

All Constraints

Position Command Scoped Cell

1 create\_clock-period 6.000 -name clk-waveform (0.000 3.000) [get\_ports clk]

Apply Cancel

Tcl Console Messages Log Reports Design Runs Timing x Utilization

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (84)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

Setup

Worst Negative Slack (WNS)	0.593 ns	Worst Hold Slack (WHS)	0.071 ns	Worst Pulse Width Slack (WPWS)	2.650 ns
Total Negative Slack (TNS)	0.000 ns	Total Hold Slack (THS)	0.000 ns	Total Pulse Width Negative Slack (TPWS)	0.000 ns
Number of Failing Endpoints	0	Number of Failing Endpoints	0	Number of Failing Endpoints	0
Total Number of Endpoints	3028	Total Number of Endpoints	3028	Total Number of Endpoints	1493

All user specified timing constraints are met.

资源：可以看到其 DSPs 一栏 pe 从原始架构中的 16 减小到了 4,这正好验证了使用折叠架构从 4 个加法器和四个乘法器减小到分别各一个，变为 1/4，满足要求。

Select an object to see properties

Tcl Console Messages Log Reports Design Runs Utilization x

Utilization

Hierarchy

Name	Slice LUTs (433200)	Slice Registers (856400)	DSPs (3600)	Bonded IOB (850)	BUFGCTRL (32)
N A3	1382	1476	36	85	1
pe8 (A3_pe_8)	175	146	4	0	0
pe7 (A3_pe_5)	151	146	4	0	0
pe6 (A3_pe_4)	157	146	4	0	0
pe5 (A3_pe_3)	160	146	4	0	0
pe4 (A3_pe_2)	152	146	4	0	0
pe3 (A3_pe_1)	169	146	4	0	0
pe2 (A3_pe_0)	160	146	4	0	0
pe1 (A3_pe_0)	144	146	4	0	0
flpmul_10 (flpmul)	62	0	4	0	0

Implemente：

频率：

IMPLEMENTED DESIGN \*-xc7v6900fpg1761-2

Sources Netlist x Project Summary x Device x Timing Constraints x

Netlist

- N A3
  - Nets (876)
  - Leaf Cells (434)
    - flpmul\_10 (flpmul)
    - pe1 (A3\_pe\_0)
    - pe2 (A3\_pe\_1)
    - pe3 (A3\_pe\_2)
    - pe4 (A3\_pe\_3)
    - pe5 (A3\_pe\_4)
    - pe6 (A3\_pe\_5)
    - pe7 (A3\_pe\_6)
    - pe8 (A3\_pe\_6)

Properties

Select an object to see properties

Timing Constraints

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	LUTs (200)	Slice Registers (856400)
1	clk	6.000	0.000	3.000	<input type="checkbox"/>	[get_ports clk]	<unsaved constraints>			

All Constraints

Position Command Scoped Cell

1 create\_clock-period 6.000 -name clk-waveform (0.000 3.000) [get\_ports clk]

Apply Cancel

Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing x

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (84)

Intra-Clock Paths

Inter-Clock Paths

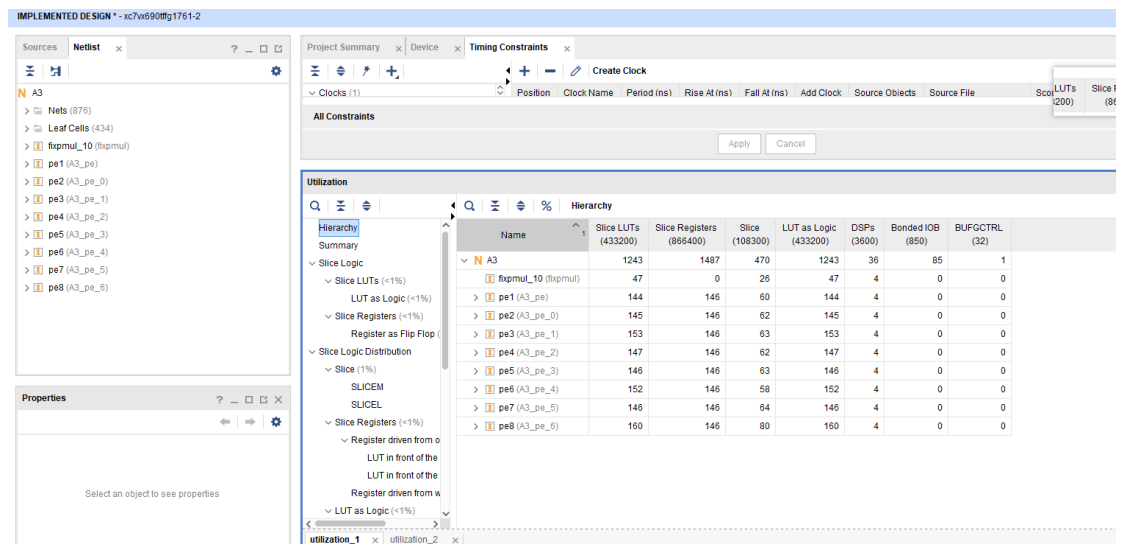
Other Path Groups

Setup

Worst Negative Slack (WNS)	0.184 ns	Worst Hold Slack (WHS)	0.101 ns	Worst Pulse Width Slack (WPWS)	2.600 ns
Total Negative Slack (TNS)	0.000 ns	Total Hold Slack (THS)	0.000 ns	Total Pulse Width Negative Slack (TPWS)	0.000 ns
Number of Failing Endpoints	0	Number of Failing Endpoints	0	Number of Failing Endpoints	0
Total Number of Endpoints	3039	Total Number of Endpoints	3039	Total Number of Endpoints	1504

All user specified timing constraints are met.

资源：



分工：

Matlab 的验证和分析：

贾鑫鹏

数据预处理：吴非

主要为输入数据和输出数据在十进制，二进制，十六进制之间的转换（python）

A1 架构的实现：

贾鑫鹏实现了主体计算逻辑，吴非进行了其中不可综合部分和使能信号控制等小细节的修改。

A2：吴非

A3：贾鑫鹏

Vivado 的验证：吴非

实验报告的 Matlab 和 A3 部分由贾鑫鹏完成，吴非负责剩余部分的撰写。

总结：

本实验通过对 IIR 架构的 matlab 和 verilog 的探索实现，对 IIR 有了更深刻的了解，并对 VLSI 的并行，折叠，流水线等常用的手段进行了实践，验证了理论知识，加深了印象，同时也熟悉了 matlab 和 vivado 等常用软件的操作。

（实验过程中的小结论：Input 是 reg 还是 wire 类型不影响 vivado 时序报告结果。）