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Electrical–thermal modeling of through-silicon via (TSV) arrays in interposer

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SUMMARY

In this paper, electrical–thermal modeling of through-silicon via (TSV) arrays is presented. In order to address the thermal effect on TSVs, TSV array design and modeling need to take into account the effect of realistic system thermal profile to meet design budget. To obtain temperature estimation for a 3D system, cascadic multigrid method is employed using an initial guess obtained by simulation using equivalent thermal conductivity to represent critical regions. By considering the thermal effect on electrical conductivities of TSV conductor and silicon substrate, the electrical–thermal modeling of TSV array in the interposer is carried out using cylindrical modal basis functions. The temperature effect on TSV insertion loss, crosstalk, and *RLCG* parameters are discussed with examples along with correlation with measurements. Copyright © 2012 John Wiley & Sons, Ltd.

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KEY WORDS: cascadic multigrid method (CMG), through-silicon via (TSV), thermal effect, cylindrical modal basis function

1. INTRODUCTION

Through-silicon via (TSV) is becoming the key enabling component for achieving miniaturized systems because of its short interconnection length and reduced parasitic effects. Because of increasing power density in 2D and 3D integrated systems, thermal effect on system performance including voltage drop, leakage power, and reliability has been studied [1–3]. For modeling of TSV array in 3D stacking system using silicon interposer (shown in Figure 1), because of the temperature-dependent electrical resistivity of silicon substrate and TSV filling material, thermal effect on TSV array characteristics and its impact on circuit performance such as crosstalk and insertion loss need to be evaluated. The effect of temperature variation on noise coupling of TSV pair was studied using measurements in [4]. However, high-density TSV array modeling with temperature effect has not been carried out so far. To take the thermal effect into account for large TSV arrays, electrical–thermal modeling method is required, which is the subject of this paper.

In the past, several approaches have been devoted to modeling and characterization of TSV parameters based on measurement [5], closed form formulae [6, 7], and partial element equivalent circuit method [8]. For modeling of TSV arrays, numerical TSV modeling method using cylindrical modal basis functions was proposed in [9]. Using small number of basis functions, one can model large TSV arrays efficiently, and the modeling results have been correlated with full wave solvers and measurements. This modeling method using cylindrical modal basis functions has been used for coupling analysis for large TSV arrays in both frequency and time domain [10]. For thermal effect on TSV, temperature effect on TSV pair capacitance and conductance has been studied in [11]. Temperature-dependent modeling of single TSV capacitance was proposed and verified with measurement in [12]. However, electrical–thermal modeling of TSV arrays has not been addressed so far.

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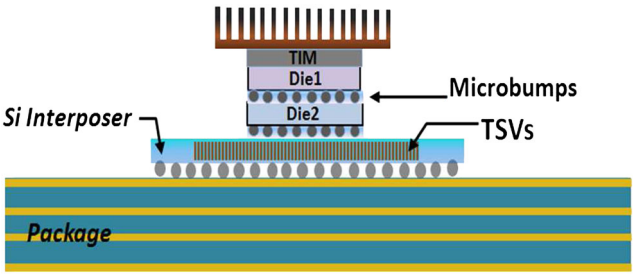

Figure 1. A 3D stacking system using silicon interposer.

In order to address thermal effect on TSV, this paper proposes an electrical–thermal modeling approach, which is extended from the cylindrical modal basis functions-based TSV modeling method [9] and the finite volume thermal modeling method [13]. The extended method captures the effect of temperature variation on TSV *RLCG* parameters, insertion loss, and TSV array crosstalk, which is crucial for signal integrity design. Therefore, the proposed method benefits TSV design parameter tuning and adjustment with realistic system thermal profile. To obtain accurate temperature estimation of 3D system including high-density TSV array, the finite volume method (FVM) based thermal modeling is adopted. With hierarchical mesh refinement, the whole system is solved efficiently using cascadic multigrid (CMG) method. To further speed up the simulation, the initial guess is obtained from simulation using equivalent thermal conductivity to represent critical regions.

The organization of this paper is as follows. In Section 2, the TSV electrical–thermal modeling method is introduced. In Section 3, TSV array modeling with temperature-sensitive material parameters is presented along with correlation with measurements. Section 4 discusses the FVM-based thermal modeling and CMG solving method. In Section 5, a TSV array example is simulated and discussed with thermal effects on TSV characteristics. Finally, the conclusion is summarized in Section 6.

2. ELECTRICAL–THERMAL MODELING OF TSV ARRAY

To capture the thermal effect on TSV arrays with realistic system thermal profile, the electrical–thermal modeling, which consists of thermal modeling of 3D system and electrical modeling of TSV array, is required. To obtain temperature distribution in silicon interposer region that contains the TSV array (Figure 1), FEM-based or FDM-based thermal simulation [14, 15] can be performed with assumed boundary conditions surrounding the interposer region. However, the accuracy is limited because of the non-uniform die power map as well as the thermal coupling between adjacent regions and stacked dies, which can result in localized hotspots. Therefore, full-system thermal modeling including die, interposer, and package is required to obtain interposer temperature estimation [1, 16].

The electrical–thermal modeling flow is shown in Figure 2. The modeling starts with the initial TSV array design parameters. In general, the system thermal profile or temperature distribution may not be available to circuit/TSV designers at the initial design stage because of undetermined system layout. The TSV array electrical–thermal modeling procedure is listed as follows:

(1) Obtaining initial TSV array design parameters including TSV length, diameter, pitch, oxide liner thickness, material properties, and so on.
(2) Electrical TSV array modeling to obtain TSV *RLCG* parameters, crosstalk, and insertion losses at room temperature.
(3) Deciding whether TSV crosstalk and insertion loss are within the design budget. If not, go back to step 1 to adjust the TSV layout parameters. Otherwise, go to the next step.
(4) With updated TSV array layout parameters, 3D system thermal simulation to obtain interposer temperature distribution.
(5) Electrical TSV modeling with updated temperature-dependent material properties. The temperature effect on TSV characteristics including *RLCG* parameters, crosstalk, and insertion loss can be obtained.
(6) Deciding whether the new TSV array characteristics meet the design budget or not. If not, go back to step 1 to adjust the TSV layout parameters and then go to step 4. Otherwise, multiport *S*-parameters and Spice-based macro-model are generated.

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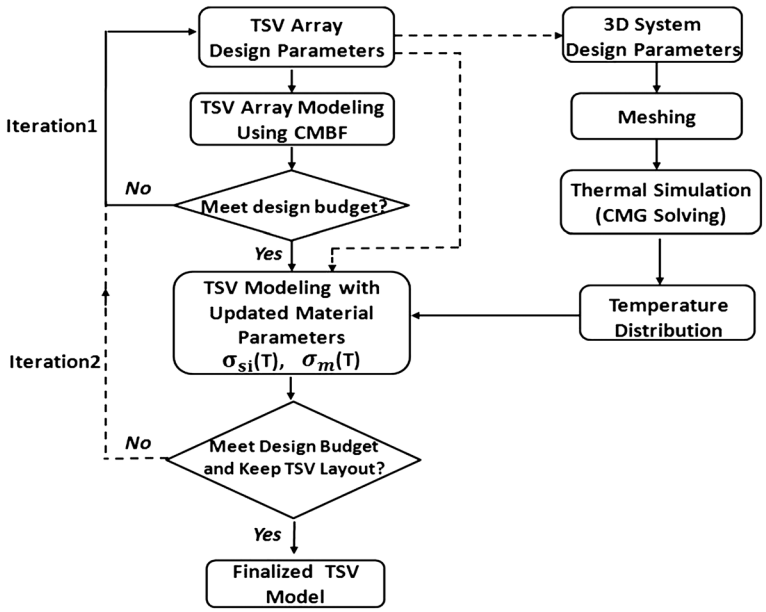

Figure 2. Electrical–thermal modeling flow for TSV array.

It is important to note that the electrical performance of TSV can be affected by TSV diameter, pitch, oxide liner thickness, and material properties including substrate conductivity [2]. In step 3, these parameters need to be considered when adjusting the TSV layout. For conventional TSV array design and modeling, it only consists of steps 1–3 without considering the system thermal profile, which can introduce discrepancy. It is important to note that the interposer thermal profile can also be calculated on the basis of the initial TSV design parameters and thus steps 2 and 3 can be bypassed, as shown in Figure 2. However, it may result in inaccurate temperature estimation. It should be noted that in the second iteration, to reduce the computational cost, the temperature estimation in the first iteration can also be used if limited TSV array geometrical modification is performed. The details of TSV array modeling with temperature effect and system thermal modeling is discussed in the following two sections.

3. ELECTRICAL TSV ARRAY MODELING WITH TEMPERATURE EFFECT

3.1. Temperature effect on material

To model TSV array, temperature-dependent material properties need to be taken into account. The temperature-dependent electrical resistivity of TSV filling materials such as copper and tungsten is described by [1]

$$\rho_{\mathrm{m}}(T) = \rho_0[1 + \alpha(T - T_0)] \tag{1}$$

where ρ_0 is the electrical resistivity at T_0, and α is the temperature coefficient of the electrical resistance. For silicon interposer, its conductivity is affected by the doping density and temperature. The temperature-dependent silicon conductivity can be described by [11]

$$\sigma_{\mathrm{si}}(T) = 1.602 \times 10^{-17} N_{\mathrm{a}} \mu_{\mathrm{p}}(T)(S/m) \tag{2}$$

The parameter N_{a} represents the concentration of substrate dopant impurity, and $\mu_{\mathrm{p}}(T)$ represents the temperature-dependent carrier mobility [17].

3.2. TSV array modeling

For TSV array modeling with temperature effect, the temperature-dependent metal conductivity $\sigma_{\mathrm{m}}(T)$ ($\sigma_{\mathrm{m}} = 1/\rho_{\mathrm{m}}$) and silicon conductivity $\sigma_{\mathrm{si}}(T)$ need to be used. In addition, because of the finite conductivity of silicon, which differs from other substrates such as glass ceramic and FR-4, complex permittivity of silicon needs to be used and described by [18]

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$$\varepsilon_{\mathrm{si}}(T) = \varepsilon_0 \varepsilon_{\mathrm{si},i}\left(1 - j\tan\delta - j\frac{\sigma_{\mathrm{si}}(T)}{\omega\varepsilon_0\varepsilon_{\mathrm{si},i}}\right) \tag{3}$$

where $\varepsilon_{\mathrm{si},i}$ is the real part of dielectric constant of silicon, and $\tan\delta$ is the intrinsic loss tangent due to the dielectric loss of an intrinsic silicon without doping.

To obtain equivalent circuit model for TSV array structure, three parts need to be extracted, as illustrated in Figure 3. The three parts include (i) conductor series resistance and inductance: this represents the resistive loss, self-inductance, and inductive coupling between TSV conductors, which can be extracted by using the electric field integral equation (EFIE) with cylindrical conduction mode basis functions (CMBFs) [19]. (ii) Substrate parallel conductance and capacitance: this represents the resistive loss and capacitive coupling in the substrate, which can be extracted by using the scalar potential integral equation (SPIE) with cylindrical accumulation mode basis functions (AMBFs). (iii) Oxide liner excess capacitance: this represents capacitive coupling between the conductor and substrate, which can be extracted by using EFIE with polarization mode basis functions (PMBFs). The modeling of TSV array has been discussed in detail in previous work [9] without considering temperature effect on material properties. Here, the model extraction is briefly explained with temperature-dependent material properties.

3.2.1. Conductor series resistance and inductance extraction. The EFIE equation used for the inductance and resistance extraction is given by

$$\frac{\vec{J}(\vec{r},w)}{\sigma_{\mathrm{m}}(T)} + \frac{j\omega u}{4\pi}\int_{V'} G(\vec{r}\,,\,\vec{r'})\vec{J}(\vec{r'},\omega)\mathrm{d}V' = -\nabla\Phi(\vec{r},\omega) \tag{4}$$

The current density of a conductor segment j can be approximated using the following equation

$$\vec{J}_j(\vec{r},\omega) \cong \sum_{n,q} I_{jnq}\,\vec{w}_{jnq}(\vec{r},\omega) \tag{5}$$

where $\vec{w}_{jnq}(\vec{r},\omega)$ is the cylindrical CMBF in conductor segment j with order n and orientation q.

After inserting the approximation of Equation (5) into the current density term in Equation (4), the following equivalent voltage equation can be obtained.

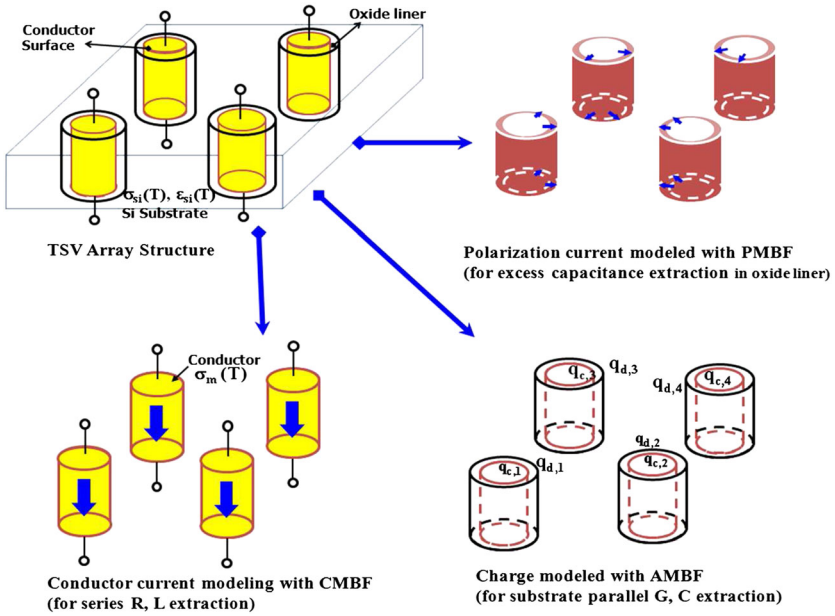

Figure 3. TSV array parameter extraction using cylindrical modal basis functions.

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$$\sum_{n,q} I_{jnq} R_{imd,jnq} + j\omega \sum_{n,q} I_{jnq} L_{imd,jnq} = \Delta V^{j}{}_{imd} \tag{6}$$

$$\text{where, } R_{imd,jnq} = \frac{1}{\sigma_m(T)} \int_{V_i} \overrightarrow{w}^{*}_{imd}(\overrightarrow{r_i}, \omega) \cdot \overrightarrow{w}_{jnq}(\overrightarrow{r_j}, \omega)$$

$$L_{imd,jnq} = \frac{\mu}{4\pi} \int_{V_j} \int_{V_i} \overrightarrow{w}^{*}_{imd}(\overrightarrow{r_i}, \omega) \cdot \overrightarrow{w}_{jnq}(\overrightarrow{r_j}, \omega) \frac{1}{|\overrightarrow{r_i} - \overrightarrow{r_j}|} \mathrm{d}V_j \mathrm{d}V_i$$

$$\Delta V^{j}_{imd} = -\frac{1}{\sigma_m(T)} \int_{S_i} \Phi_j(\overrightarrow{r_i})\, \overrightarrow{w}^{*}_{imd}(\overrightarrow{r_i}, \omega) \cdot \mathrm{d}\overrightarrow{S_i}$$

In the preceding equations, i, m, d represent the index of inductive cell, the order of CMBF, and the orientation of CMBF, respectively [9].

3.2.2. Substrate parallel conductance and capacitance calculation. The SPIE used for substrate parallel conductance and capacitance calculation is expressed as

$$\frac{1}{4\pi\varepsilon_{\mathrm{si}}(T)} \int_{V'} G(\overrightarrow{r}, \overrightarrow{r'}) q(\overrightarrow{r'}, \omega) \mathrm{d}V' = \Phi(\overrightarrow{r}, \omega) \tag{7}$$

By inserting the charge density distribution function $q = \sum_{n=0} Q_{knq} v_{knq}$ and applying the inner product of

$$\langle \overrightarrow{v}_{lmd}(\overrightarrow{r}, \omega), \overrightarrow{x} \rangle = \int_S v_{lmd}(\overrightarrow{r}, \omega) x \mathrm{d}S \tag{8}$$

the following equation can be deduced from the SPIE (7).

$$\sum_{lnq} P^{C,D}_{kmd,lnq} Q_{lnq} = \Phi^{C,D}_{kmd} \tag{9}$$

where $P^{C,D}_{kmd,lnq} = \frac{1}{4\pi\varepsilon_{\mathrm{si}}(T)} \int_{S_l} \int_{S_k} v_{kmd}(\overrightarrow{r_k}) v_{lnq}(\overrightarrow{r_l}) \frac{1}{|\overrightarrow{r_i} - \overrightarrow{r_j}|}$.

Here, k, m, d represent the index of conductor number, modal order, and orientation of cylindrical AMBF v_{knq}, respectively. $P^{C,D}_{kmd,lnq}$ is the partial potential coefficient between the (k, m, d)th and (l, n, q) th order modes. The superscripts C and D represent the conductor surface and insulator surface of the TSV, respectively [9].

3.2.3. Oxide liner excess capacitance extraction. The EFIE used for the extraction of the excess capacitance in oxide liner is given by

$$\frac{\overrightarrow{J^P}(\overrightarrow{r}, \omega)}{j\omega\varepsilon_0(\varepsilon_{\mathrm{ox}} - \varepsilon_{\mathrm{si}}(T))} + j\omega \frac{u}{4\pi} \int_{V'} G(\overrightarrow{r}, \overrightarrow{r'}) \overrightarrow{J^P}(\overrightarrow{r'}, \omega) \mathrm{d}V' = -\nabla\Phi(\overrightarrow{r}, \omega) \tag{10}$$

Using a similar process for inductance and resistance extraction, one can deduce and express the following equation as

$$\sum_{l,n,q} I_{lnq} \frac{1}{j\omega C^{ex}_{kmd,lnq}} + \sum_{l,n,q} j\omega L_{kmd,lnq} I_{lnq} = \int_{V_k} \overrightarrow{u}_{kmd} \cdot (-\nabla\Phi) \mathrm{d}V_k \tag{11}$$

where $C^{\mathrm{ex}}_{kmd,lnq} = \frac{\varepsilon_0(\varepsilon_{ox} - \varepsilon_{si}(T))}{\int \overrightarrow{u}_{kmd} \cdot \overrightarrow{u}_{lnq} \mathrm{d}V_k}$

$$L_{kmd,lnq} = \frac{\mu}{4\pi} \int_{V_k} \int_{V_l} G(\overrightarrow{r_k}, \overrightarrow{r_l}) \overrightarrow{u}_{kmd}(\overrightarrow{r_k}) \cdot \overrightarrow{u}_{lnq}(\overrightarrow{r_l}) \frac{1}{|\overrightarrow{r_i} - \overrightarrow{r_j}|} \mathrm{d}V_l \mathrm{d}V_k$$

Here, k, m, d represent the index of conductor number, modal order, and orientation of cylindrical PMBF $\overrightarrow{u}_{kmd}$, respectively.

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Equations (6) (9) and (11) can be combined into a large matrix equation, which relates the terminal currents and nodal voltages to the modal circuit elements consisting of the conductor *R–L* elements, parallel conductance, and capacitance in silicon substrate, excess capacitance in TSV oxide liner. By ensuring the continuity relationship between the current and charge, eliminating the internal current and charge vectors in the conductor cell as well as on the insulator surface, the reduced matrix equation relating the terminal currents and conductor model voltage can be derived as

$$(Y_c(T) + j\omega C^{eq}(T))\Phi^C = \begin{pmatrix} I_t \\ 0 \end{pmatrix} \tag{12}$$

For TSV array with n-ports, the series resistance, self-inductance, and mutual inductance can be extracted from system matrix $Y_c(T)$, which is temperature dependent. The equivalent $n \times n$ capacitance matrix and conductance matrix can be obtained from system matrix $C^{eq}(T)$. Note that the $n \times n$ capacitance and conductance matrices include the effects of oxide liner layer and silicon substrate. For the TSV pair case, the equivalent circuit model is shown in [9].

The TSV modeling method described earlier is used to obtain the model for large TSV array with temperature-dependent material properties in frequency domain in this paper. This TSV modeling method using cylindrical modal basis functions can take into account the design parameters including TSV diameter, pitch, oxide liner thickness, and material properties. As a result, the effect of parameter adjustment on TSV performance can be captured automatically in step 3 of electrical–thermal modeling of TSV array (Figure 2). For time domain analysis, the TSV array model in frequency domain is converted to a Spice sub-circuit model using Idem [20], which enables the development of a macro-model by preserving passivity and causality. After generating the Spice sub-circuit model, the temperature effect on crosstalk waveform in the TSV array can also be obtained by performing time domain simulation.

3.3. Model validation

The aforementioned TSV modeling method has been validated by correlating with full wave solver in frequency domain [9]. To further validate our modeling approach, an experimental example consisting of four TSVs is simulated in time domain, as shown in Figure 4(a). The TSV cross-sectional dimension is shown in Figure 4(b). Note that the simulation and measurement are carried out at room temperature. A rectangular clock signal with peak-to-peak amplitude of 1 V is excited at TSV-1. The coupled waveform is measured at the top end of TSV-2. The comparison between simulated coupled waveform and measurement results [21] with input clock frequencies of 100 MHz and 1 GHz is shown in Figure 5. The good agreement between the measurement results and results from the proposed model validates the TSV modeling method. Note that the pads and reference GND are also considered in the modeling. It is found that the coupling between TSVs dominates the coupling, especially when the lines are short as in this example.

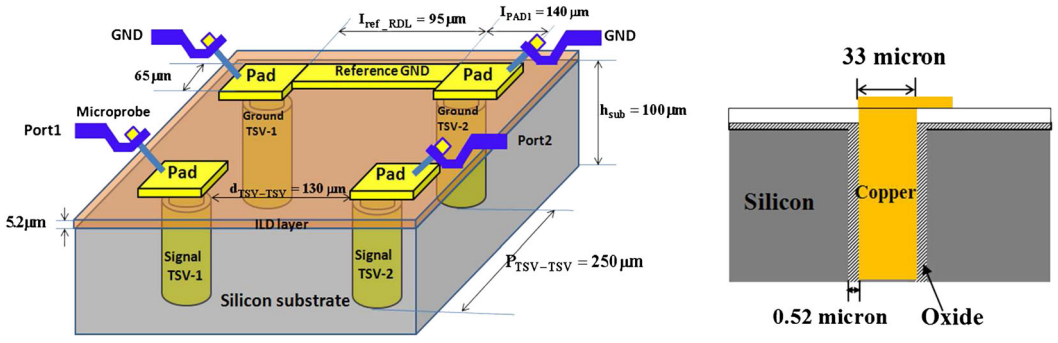

Figure 4. (a) A 2 × 2 TSV array configuration. (b) TSV cross-sectional dimension.

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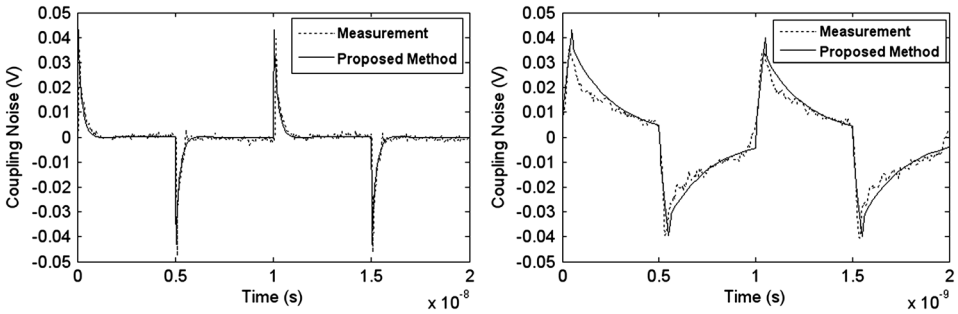

Figure 5. TSV–TSV coupled waveform with input clock frequencies of (a) 100 MHz and (b) 1 GHz.

4. 3D SYSTEM THERMAL MODELING

4.1. Finite volume schemes

Because of the scale difference in 3D system, non-uniform meshing grid is preferred to reduce the number of unknowns and also capture all the object details accurately for thermal simulation. In this paper, 3D non-uniform rectangular grid has been used.

4.1.1. Heat conduction. The 3D non-uniform grid for conduction modeling is shown in Figure 6(a). $T_{i,j,k}$ represents the temperature at grid point (i,j,k), which is surrounded by other six nodes. $\Delta x_1, \Delta x_2$, $\Delta y_1, \Delta y_2$, Δz_1, and Δz_2 are the nodal distances between node (i,j,k) and its adjacent nodes in x, y, and z directions, respectively. The dashed cell intersects with the mid-points of lines from point (i, j, k) to the surrounding six nodes. By using the finite volume formulation procedure as in [1, 13], one can obtain the finite volume scheme at node (i,j,k) as

$$\frac{T_{i,j,k}-T_{i-1,j,k}}{\frac{\Delta x_1}{k_x l_y l_z}}+\frac{T_{i,j,k}-T_{i+1,j,k}}{\frac{\Delta x_2}{k_x l_y l_z}}+\frac{T_{i,j,k}-T_{i,j-1,k}}{\frac{\Delta y_1}{k_y l_x l_z}}+\frac{T_{i,j,k}-T_{i,j+1,k}}{\frac{\Delta y_2}{k_y l_x l_z}}+\frac{T_{i,j,k}-T_{i,j,k-1}}{\frac{\Delta z_1}{k_z l_x l_y}}+\frac{T_{i,j,k}-T_{i,j,k+1}}{\frac{\Delta z_2}{k_z l_x l_y}}=P_{\text{total}} \tag{13}$$

where $l_x=(\Delta x_1+\Delta x_2)/2$, $l_y=(\Delta y_1+\Delta y_2)/2$, and $l_z=(\Delta z_1+\Delta z_2)/2$. $P_{total}=\iint_{dashed\ cell}-P(x,y,z)\mathrm{d}S$ is the total heat source in the dashed cell. k_x, k_y, and k_z represent the thermal conductivity in x, y, and z directions, respectively.

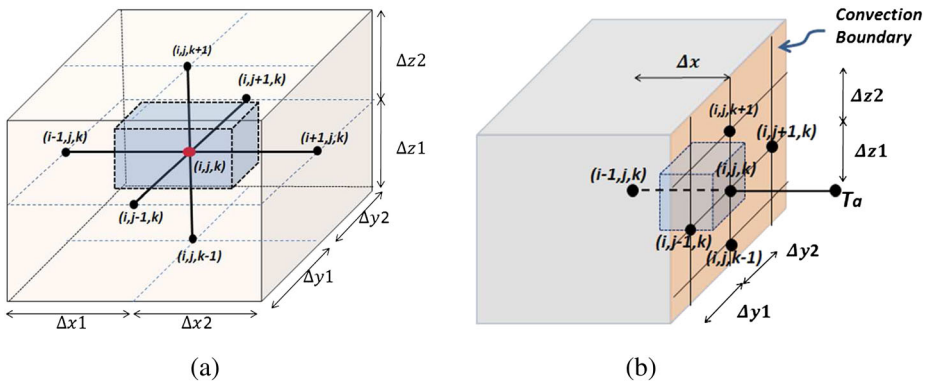

Figure 6. (a) A 3D rectangular grid for heat conduction. (b) Convection boundary with non-uniform mesh.

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4.1.2. Convection modeling. To obtain temperature distribution of realistic systems, the convection boundary condition

$$k\frac{\partial T}{\partial n}|_{convection} = -h_c(T - T_a) \tag{14}$$

needs to be taken into account. In Equation (14), T_a and h_c represent the ambient temperature and convection coefficient, respectively. As shown in Figure 6(b), the finite volume cell (shown in dashed line) is intersecting with the mid-points of lines from node (i, j, k) to other five adjacent nodes except the node in the air medium. The finite volume scheme for heat equation with convection boundary condition at node (i,j,k) can be derived as

$$\frac{T_{i,j,k} - T_{i-1,j,k}}{\frac{\Delta x}{k_x l_y l_z}} + \frac{T_{i,j,k} - T_{i,j-1,k}}{\frac{2\Delta y_1}{k_y l_x l_z}} + \frac{T_{i,j,k} - T_{i,j+1,k}}{\frac{2\Delta y_2}{k_y l_x l_z}} + \frac{T_{i,j,k} - T_{i,j,k-1}}{\frac{2\Delta z_1}{k_z l_x l_y}} + \frac{T_{i,j,k} - T_{i,j,k+1}}{\frac{2\Delta z_2}{k_z l_x l_y}} + \frac{T_{i,j,k} - T_a}{\frac{1}{h_c l_y l_z}} = P_{total} \tag{15}$$

4.2. Cascadic multigrid simulation

Because of the multiple scales in integrated systems containing TSVs, stacked dies, and package, efficient numerical solvers are required. Complex IC package can be simulated using multigrid method with appropriate smoother, restriction and interpolation operators [13]. Usually, multigrid-based solving algorithm needs to be tuned for a given problem on the basis of geometric and material parameters to reach its maximum performance. As a result, it is not as general as other iterative methods such as conjugate gradient (CG) method. Instead of using standard multigrid method, the CMG method [22], which does not require additional tuning for a given problem, can be adopted to solve the system equation $Yx = b$ formulated using FVM. It is important to note that for the CMG method to be applied for simulating 3D system efficiently, special consideration and treatment are required considering high-density structures, which is addressed in this section. The CMG simulation flow chart is shown as in Figure 7.

As shown in Figure 7, the problem with the coarsest meshing grid, which has fewer unknowns, is solved first. Then, the solution is interpolated to next mesh level. For each mesh level except the initial mesh level, the CG method with a diagonal pre-conditioner is used to accelerate the convergence of the solution before it is interpolated to finer grids. As the initial approximation is interpolated from the previous level, the starting residual is small, and thus convergence can be reached efficiently. As the preconditioned CG (PCG) method is used, the stop criteria ε needs to be used to check the convergence [23]. In this paper, the L2 residual norm-based stop criteria is used, which is described by

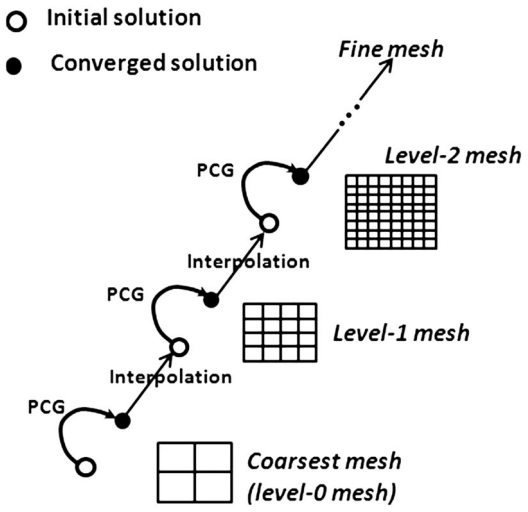

Figure 7. Cascadic multigrid simulation flow chart.

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$$\|r_t\| < \varepsilon \|r_0\| \tag{16}$$

where $\|r_0\|$ and $\|r_t\|$ represent the L2 norm of the residual for initial and t-th PCG iteration, respectively. As the residual is already calculated in each PCG iteration, no extra matrix–vector multiplication is needed.

For a 3D system to be simulated efficiently using CMG, special consideration is required because of high-density TSV array and micro-bumps. As the 3D system contains large amount of TSVs and micro-bumps, the initial coarsest mesh may have thousands of unknowns. Therefore, iterative PCG solving is required, and an approximate good initial guess is needed to accelerate the simulation. The entire thermal simulation flow is shown in Figure 8. To obtain an initial approximate solution for CMG method, equivalent thermal conductivity of critical regions needs to be extracted first. To extract the effective thermal conductivity in x, y, and z directions for die, interposer, and micro-bump regions, the uniform temperature is assigned at one side whereas distributed heat sources are assigned on the other side. By adding very small thermal resistances between heat source nodes, all the heat source ports are lumped together, and thus uniform temperature can be obtained at the heat source ports. As a result, the effective thermal conductivity can be obtained on the basis of the temperature gradient and total heat flow. The smaller 'quasi-problem' of $Y'x' = b'$, which uses the equivalent thermal conductivity k_x, k_y, and k_z to represent the die, micro-bump, and interposer layers, is simulated first by using a direct solver (Figure 8). The solution is then interpolated to the meshing grid of the original problem for the CMG method. As a result, the CMG method can converge quickly with the interpolated initial values. It is important to note that because thermal modeling is based on the FVM using volumetric discretization, the effect of TSV density on the interposer equivalent thermal conductivity [24] as well as the temperature can be taken into account automatically in the process of thermal simulation and for extracting equivalent thermal conductivity of critical regions.

5. RESULTS AND DISCUSSION

A 3D integration example including stacked dies, thermal interface material (TIM), four-layer package, micro-bumps, silicon interposer, and underfill is simulated. The whole system view is shown in Figure 1. The stacked die size is 8 mm × 8 mm. The silicon interposer size is 30 mm × 30 mm, and the package size is 60 mm × 60 mm. The 120 × 120 TSV array is distributed in the center of silicon interposer, as shown in Figure 1. The TSV diameter is 20 μm, and the pitch between TSVs is 66.7 μm. The detailed geometric parameter and material thermal conductivity are listed in Table 1. Two design cases are studied. For design

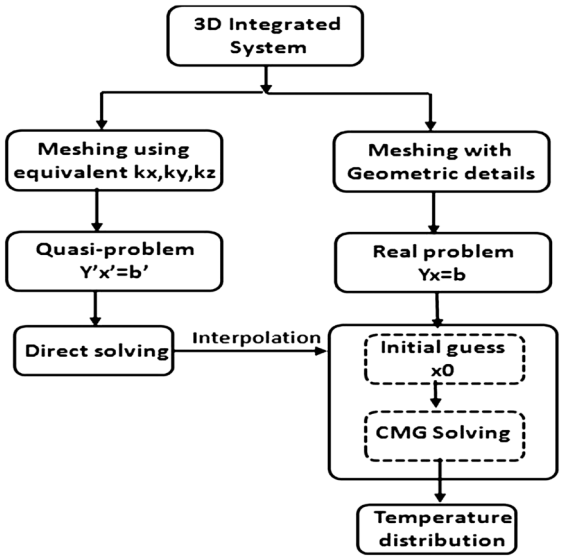

Figure 8. Thermal simulation flow chart.

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Table I. Geometric parameters and thermal conductivity.

	Material thickness (mm)	Thermal conductivity (W/m K)
Glass-ceramic	0.35	5
Copper plane	0.03	400
Die	0.2	110
Underfill	0.2	0.4
Micro-bump	0.2	60
TIM	0.2	2.0
TSV	0.2	400

case 1, the power consumption of die 1 and die 2 are 8 and 2 W, respectively. For design case 2, the power consumption of die 1 and die 2 are 30 and 12.5 W, respectively. Their non-uniform die power maps are shown in Figure 9(a and b), respectively. Among the 120×120 TSV array, a 5×5 TSV array, which is located at the center of the 120×120 TSV array, is shown in Figure 10(a). The TSV cross-sectional view is shown in Figure 10(b). The interposer thickness and oxide thickness are 200 and 0.1 μm, respectively. The TSV filling material is copper. The conductivity of silicon interposer is 10.4 S/m at room temperature. Its doping density is 1.32×10^{15} cm^{-3}. Air convection with convection coefficient of 10 W/m^2 K is applied to the top surface of silicon interposer and to both sides of the package.

5.1. Temperature distribution

To obtain the temperature distribution of the silicon interposer, thermal simulation of the 3D system (Figure 1) is required. In the thermal simulation, the interposer and stacked die regions contain large amount of TSVs and micro-bumps, which require very fine meshing grids. To obtain an initial approximate guess for CMG method, the 'quasi-problem', which uses the equivalent thermal conductivity k_x, k_y, and k_z to represent the interposer, die, and micro-bump layers, is simulated first by using a direct solver. The approximate

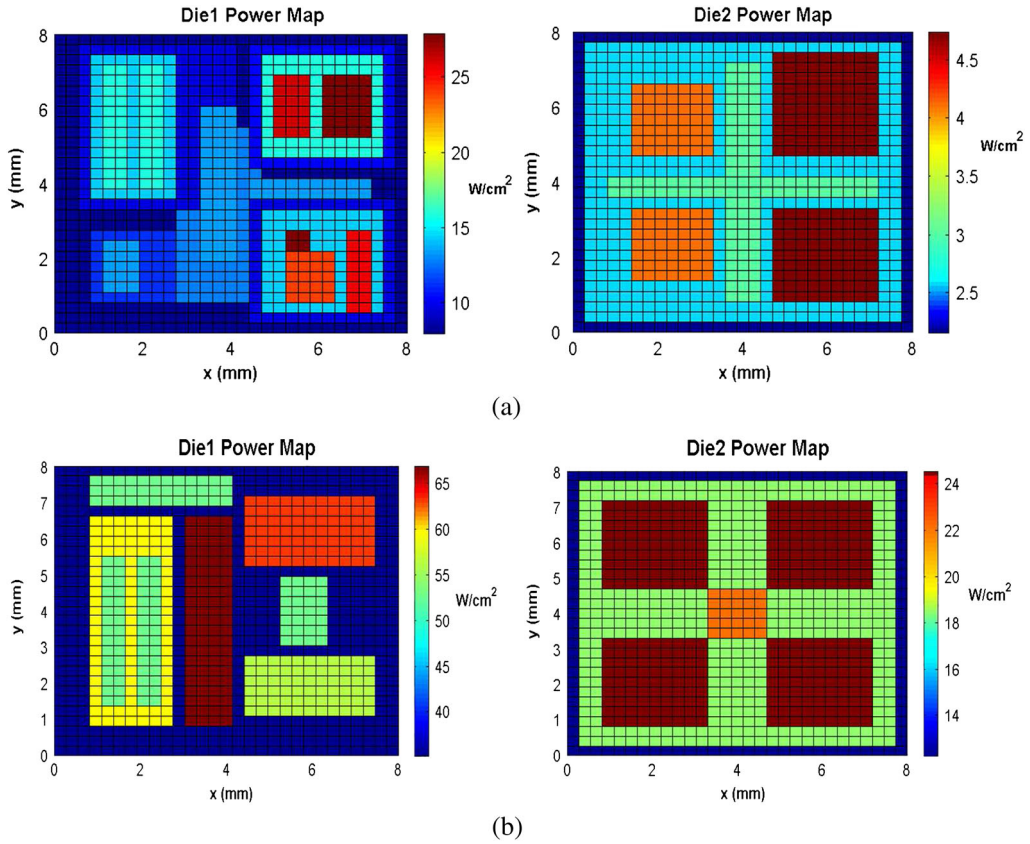

Figure 9. Die power maps for (a) case 1 and (b) case 2.

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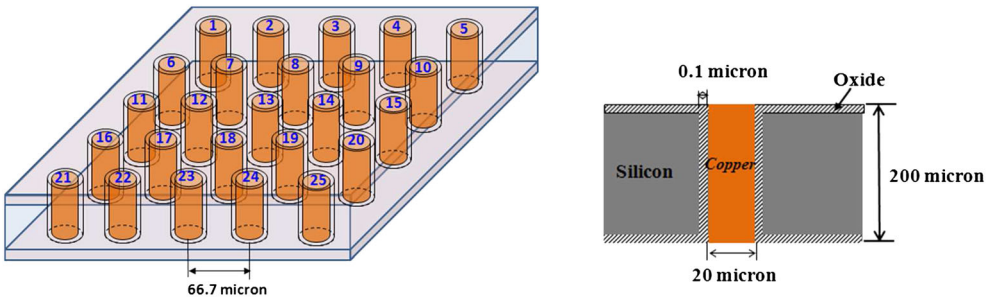

(a) (b)

Figure 10. (a) A 5 × 5 TSV array structure and (b) TSV cross-section.

solution is then interpolated to the meshing grid of the original problem for CMG method. The stop criteria ε is set to be 1e−4 for both level 0 and level 1 mesh.

In this example, the quasi-problem only requires 0.36 million unknowns and 10 s solving time by using a direct sparse solver. The original problem requires 1.3 million unknowns for the coarsest mesh (level 0 mesh) and 5.2 million unknowns for the level 1 mesh. With the interpolated solution obtained from the quasi-problem, CMG converges in 1130 and 2370 iterations for level 0 and level 1, respectively. The total simulation time are 296 and 3345 s for level 0 and level 1, respectively. The residual convergence comparison between PCG and CMG methods is shown in Figure 11. As shown in Figure 11, to reach the same convergence tolerance of 1e−4, CMG method only requires 2370 iterations whereas PCG method requires 5710 iterations. The total simulation time for PCG method is 9309 s, about 2.5 times of the CMG method.

The simulated temperature distributions of the silicon interposer for the two design cases are shown in Figure 12. As seen from Figure 12, the interposer temperature varies from 36.5°C to 40.5°C for case 1 and 76°C to 92°C for case 2 because of the non-uniform die power map (Figure 9). Therefore, electrical TSV array modeling with material property calculated at room temperature can introduce discrepancy due to system temperature increase. In 3D system, the pitch between adjacent TSVs is usually in the range of 50–100 μm, depending on the process used. For 5 × 5 or 10 × 10 TSV array, it covers an area less than 1 mm^2. Because of the high thermal conductivity of silicon interposer, the temperature variation in the 5 × 5 TSV array region is usually very small (<1°C in our simulation). As a result, single temperature (40°C for case 1 and 92°C for case 2 for this example) can be used for the 5 × 5 TSV array region while still maintaining accuracy. Although this method has been applied to a 5 × 5 TSV array, it can be applied to larger TSV arrays as well because of the efficiency of the modeling methodology.

5.2. Temperature effect on TSV characteristics

With the initial TSV design parameters, the electrical modeling of 5 × 5 TSV array (Figure 10(a)) using CMBFs is first carried out at room temperature of 25°C. The simulated TSV insertion loss and

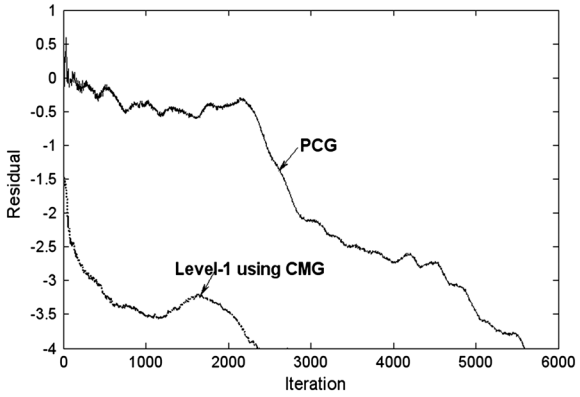

Figure 11. Residual convergence comparison between CMG and PCG.

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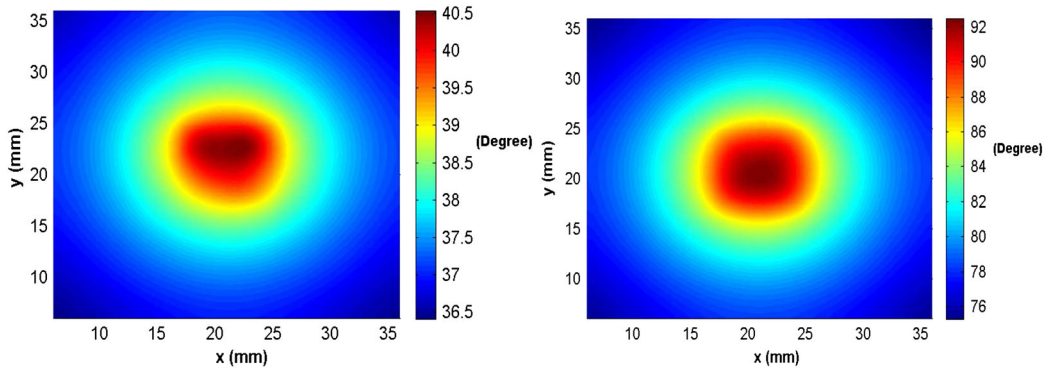

Figure 12. Simulated interposer temperature distribution for (a) case 1 design and (b) case 2 design.

crosstalk are shown in Figures 13 and 14, respectively. As the temperature distribution is already simulated for the two cases, the material properties of silicon interposer and TSV conductor can be updated, and electrical modeling of the TSV array is carried out with temperature effect (step 5 in Figure 2). For comparison purpose, the insertion loss and crosstalk with simulated temperatures (40°C for design case 1 and 92°C for design case 2) for the 5×5 TSV array region are also shown in Figures 13 and 14, respectively.

It is observed that with updated TSV array temperatures of 40°C and 92°C, the insertion losses of TSV-1 and TSV-7 are reduced, and more design budget is gained. As seen from Figure 13, the temperature effect on insertion loss is not obvious up to 0.2 GHz. From 0.2 to 10 GHz, the insertion

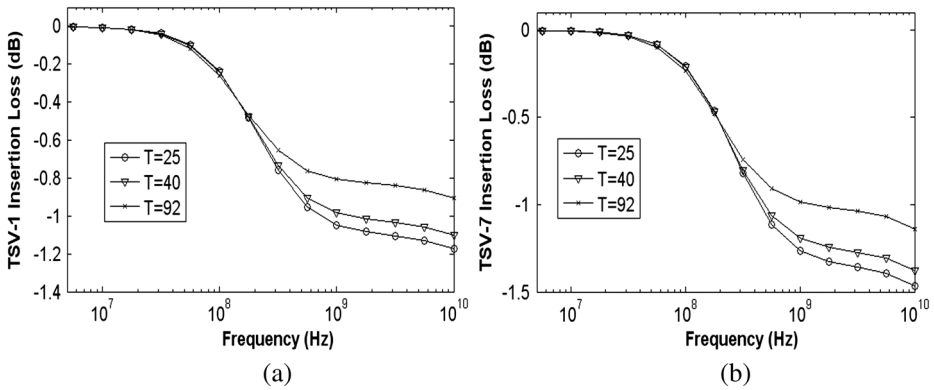

Figure 13. Insertion loss of (a) TSV-1 and (b) TSV-7.

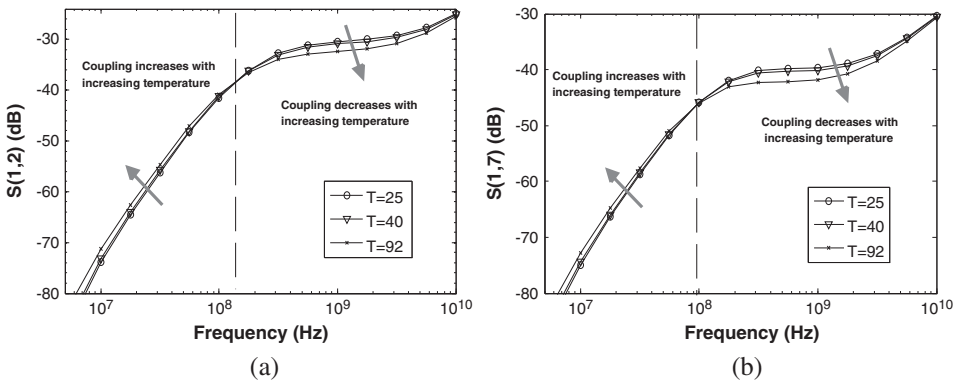

Figure 14. Near end crosstalk between (a) TSV-1 and TSV-2, and (b) TSV-1 and TSV-7 with initial and simulated temperatures.

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loss is reduced with increasing TSV array temperature. This is caused by the reduced silicon interposer conductivity because of temperature increase. As shown in Figure 14(a and b), the temperature effect on TSV coupling shows frequency-dependent behavior regions. In low frequency range, the near end coupling between TSV-1 and TSV-2, and TSV-1 and TSV-7 increases with temperature. However, at higher frequencies (from 100 MHz to several GHz), the trend is reversed, and better isolation is obtained with increasing temperature, which is also because the silicon substrate conductivity is reduced with increasing temperature, as indicated by Equation (2). As frequency further increases to 10 GHz, the coupling converges, and the temperature effect cannot be observed. The same trend was shown by the measurements for TSV pairs in [4]. The variations of TSV insertion loss and crosstalk caused by temperature indicate the importance of temperature effects on TSV array modeling for real designs.

The TSV-1 self-parameters including series resistance, series inductance, shunt capacitance, and conductance with initial and simulated temperatures are shown in Figure 15(a–d), respectively. As shown in Figure 15(a), with updated TSV array temperatures, the series resistance of TSV-1 increases linearly because of the temperature coefficient of the electrical resistance, which is $0.0039\,K^{-1}$ for copper TSV in this example. As seen from Figure 15(b), the updated temperature has no effect on series inductance at low frequencies because of the uniform current distribution inside TSV conductor. At higher frequencies, because of skin effect, which happens around 0.1 GHz, the inside current distribution is affected by the temperature resulting in small variation of TSV inductance.

For TSV self-capacitance, the temperature effect is obvious in the range of 0.05–1 GHz, as shown in Figure 15(c). With increasing temperature, the equivalent capacitance is reduced. This is because silicon permittivity also depends on the temperature, as indicated by Equation (3). As seen from Figure 15(d), in low frequency range, the conductance does not change with temperature. However, in frequency range of 0.2–10 GHz, the conductance decreases with temperature, which is caused by the decreasing silicon substrate conductivity with increasing temperature. For TSVs, as the series resistance is in the scale of milliohms (Figure 15(a)) and inductance in the scale of pH (Figure 15(b)), the insertion loss of TSV at higher frequencies is mainly caused by the shunt capacitance and conductance.

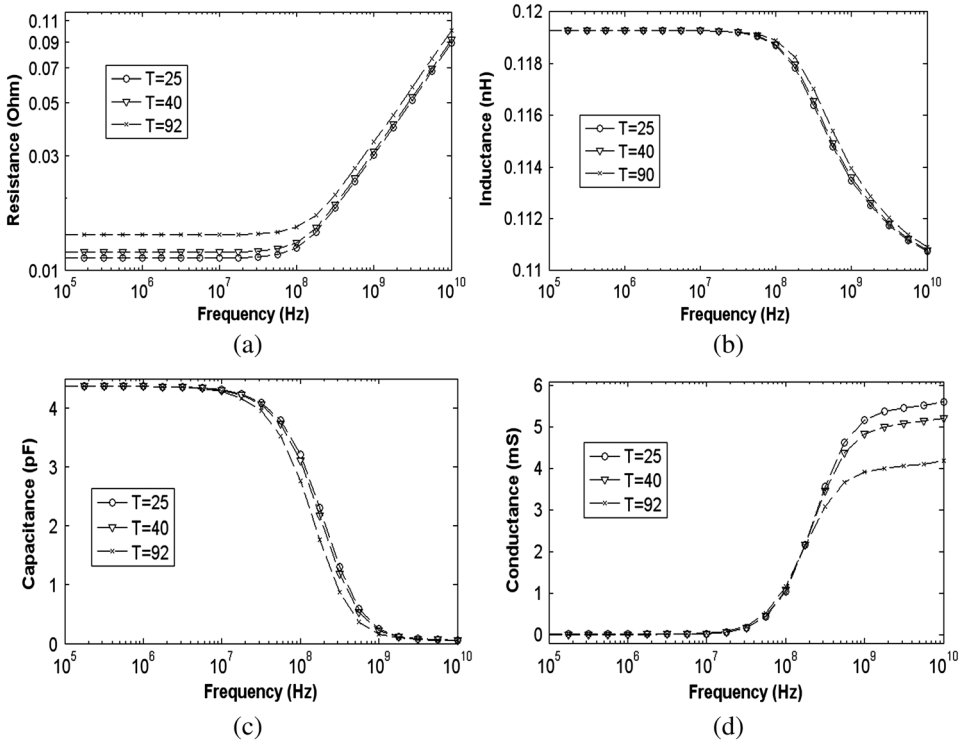

Figure 15. TSV-1 self-*RLCG* parameters (a) resistance, (b) inductance, (c) capacitance, and (d) conductance.

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The time domain TSV coupled noise with temperature effect is also simulated. For the time domain simulation, rectangular clock signal with peak-to-peak amplitude of 2 V is excited at the top end of four signal TSVs including TSV-1, TSV-3, TSV-11, and TSV-13 (Figure 10(a)). The bottom ends of the four TSVs are terminated using 50 Ω resistors. TSV-7 is the victim TSV used to observe the coupled noise. As the number of neighboring ground TSVs in the system can affect the signal crosstalk, the effect of ground/signal (G/S) TSV ratio on coupled noise is first examined. Three cases are studied with G/S TSV ratio of 1:4, 2:4, and 4:4. The ground TSV ID numbers for the three cases are shown in Table 2. Note that the top and bottom ends of all other TSVs in the 5×5 TSV array (Figure 10(a)) are all terminated with 50 Ω resistors connecting to ground.

With different G/S TSV ratio, the coupled noise at the top end of TSV-7 with input clock frequency of 1 GHz is shown in Figure 16(a). The rise and fall times of the clock signal are both set to 50 ps. The peak values of coupled noise and percentage change due to increasing G/S TSV ratio are listed in Table 2. It is observed that by increasing G/S ratio from 1:4 to 2:4 and 4:4, the coupled noise can be reduced by 18% and 39%, respectively, indicating the importance of ground to signal TSV ratio on crosstalk. With G/S TSV ratio of 4:4, the coupled noise with temperature effect is also investigated, and the coupled waveform is shown in Figure 16(b). As seen from Figure 16(b), the coupled noise decreases with increasing temperature. The peak values of the coupled noise and percentage change due to temperature effect are listed in Table 3. As seen from Table 3, by increasing system temperature from 25°C to 92°C, the temperature effect can result in 13% reduction of coupled noise.

Table II. Effect of ground/signal TSV ratio on coupling noise.

	G/S TSV ratio		
	1:4	2:4	4:4
Ground TSV	TSV-2	TSV-2, TSV-12	TSV-2, TSV-6, TSV-8, TSV-12
Peak value (mV)	97.6	79.6	59.6
Percentage change	—	18.4	38.9

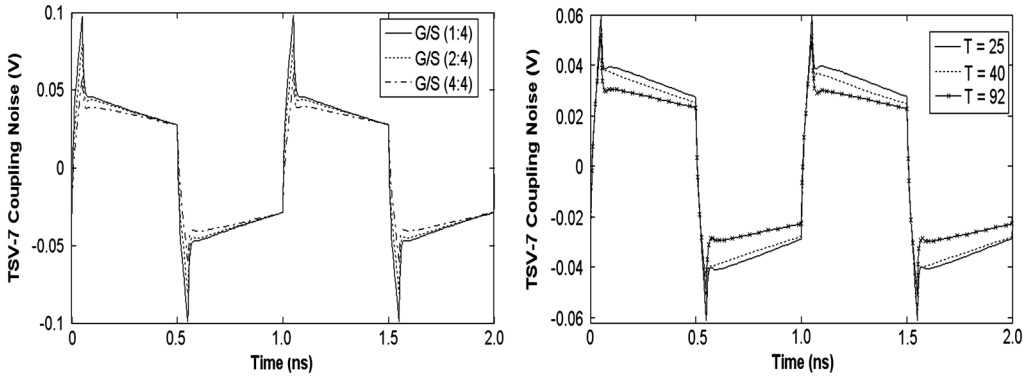

Figure 16. (a) Coupled noise with different G/S TSV ratio and (b) temperature effect on coupled waveform.

Table III. Temperature effect on TSV coupling noise.

	Temperature		
	25°C	40°C	92°C
Peak value (mV)	59.6	58.3	51.8
Percentage change	—	2.2	13.0

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6. CONCLUSION

In this paper, electrical–thermal modeling of TSV array is presented. The effect of system thermal profile on TSV characteristics including TSV *RLCG* parameters, insertion loss, and crosstalk is studied. The modeling results show that the temperature-sensitive material properties especially the silicon conductivity cannot be neglected for TSV array design and modeling. The CMG solving method shows good capability for thermal simulation of 3D systems.

REFERENCES

1. Xie J, Swaminathan M. Electrical–thermal co-simulation of 3D integrated systems with micro-fluidic cooling and joule heating effects. *IEEE Trans Compon, Packag Manuf Technol* 2011; **1**(2):234–246.
2. Liu Y, Dick RP, Shang L, Yang H. Accurate temperature-dependent integrated circuit leakage power estimation is easy. *Design, Automation & Test in Europe Conference & Exhibition (DATE)* 2007: 1–6.
3. Sri-Jayantha SM, McVicker G, Bernstein K, Knickerbocker JU. Thermomechanical modeling of 3D electronic packages. *IBM J Res Dev* 2008; **52**(6):623–634.
4. Lee M, Cho J, Kim J, Pak JS, Kim J, Lee H, Lee J, Park K. Temperature-dependent through-silicon via (TSV) model and noise coupling. *IEEE 20th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)* 2011; 247–250.
5. Ryu C, Lee J, Lee H, Lee K, Oh T, Kim J. High frequency electrical model of through wafer via for 3-D stacked chip packaging. *Proc. Electron. Systemintegrat. Technol. Conf*. 2006; 215–220.
6. Katti G, Stucchi M, Meyer KD, Dehaene W. Electrical modeling and characterization of through silicon via for three-dimensional ICs. *IEEE Trans Electron Devices* 2010; **57**(1):256–262.
7. Liu E-X, Li E-P, Ewe W-B, Lee HM. Multi-physics modeling of through-silicon vias with equivalent-circuit approach. *2010 IEEE 19th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)* 2010; 33–36.
8. Wang XP, Zhao WS, Yin WY. Electrothermal modelling of through silicon via (TSV) interconnects. *IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS)* 2010; 1–4.
9. Han KJ, Swaminathan M. Electromagnetic modeling of through-silicon via (TSV) interconnections using cylindrical modal basis functions. *IEEE Trans. Adv. Packag.* 2010; **33**(4):804–817.
10. Xie B, Swaminathan M, Han KJ, Xie J. Coupling analysis of through-silicon via arrays in silicon interposers for 3D system. *IEEE International Symposium on Electromagnetic Compatibility* 2011; 16–21.
11. Zhao W-S, Wang X-P, Yin W-Y. Electrothermal effects in high density through silicon via (TSV) array. *Prog Electromagnet Res* 2011; **115**:223–242.
12. Katti G, Stucchi M, Velenis D, Soree B, Meyer KD, Dehaene W. Temperature-dependent modeling and characterization of through-silicon via capacitance. *IEEE Electron Device Letters* 2011; **32**(4): 563–565.
13. Xie J, Swaminathan M. Fast electrical–thermal co-simulation using multigrid method for 3D integration. *accepted by 62nd Electronic Components and Technology Conference (ECTC)* 2012.
14. Rzepka S, Banerjee K, Meusel E, Hu C. Characterization of self-heating in advanced VLSI interconnect lines based on thermal finite element simulation. *IEEE Trans Compo, Packag Manuf Technol Part A* 1998; **21**(3):406–411.
15. Tsai C-H, Kang S-M. Cell-level placement for improving substrate thermal distribution. *IEEE Trans. Computer-Aided Design Integr Circ Syst* 2000; **19**(2):253–266.
16. Xie J, Swaminathan M. Simulation of power delivery networks with joule heating effects for 3D integration. *Electronics System Integration Technology Conferences (ESTC)* 2010; 1–6.
17. Yin W-Y, Kang K, Mao J-F. Electromagnetic–thermal characterization of on-chip coupled (a)symmetrical interconnects. *IEEE Trans. Adv. Packag.* 2007; **30**(4):851–863.
18. Yang R-Y, Hung C-Y, Su Y-K, Weng M-H, Wu H-W. Loss characteristics of silicon substrate with different resistivities. *Microwave Opt. Technol. Lett.* 2006; **48**(9): 1773–1776.
19. Han KJ, Swaminathan M. Inductance and resistance calculations in three-dimensional packaging using cylindrical conduction-mode basis functions. *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.* 2009; **28**(6): 846–859.
20. IDEM: Identification of Electrical Macromodels [Online]. Available: http://www.emc.polito.it/software/IdEM/idem_home.asp 2009.
21. Cho J, Song E, *et al*. Modeling and analysis of through-silicon via (TSV) noise coupling and suppression using a guard ring. *IEEE Trans. CPMT* 2011; **1**(2):220–233.
22. Shi Z-C, Xu X-J, Man H-Y. Cascadic multigrid for finite volume method for elliptic problems. *J Comput Math* 2004; **22**(6): 905–920.
23. Xie J, Swaminathan M. DC IR drop solver for large scale 3D power delivery networks. *19th conference on Electrical Performance of Electronic Packaging and Systems* 2010; 217–220.
24. Hoe YYG, Yue TG, Damaruganath P, Chong CT, Lau JH, Zhang X, Vaidyanathan K. Effect of TSV interposer on the thermal performance of FCBGA package, *11th Electronics Packaging Technology Conference (EPTC)* 2009; 778–786.

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