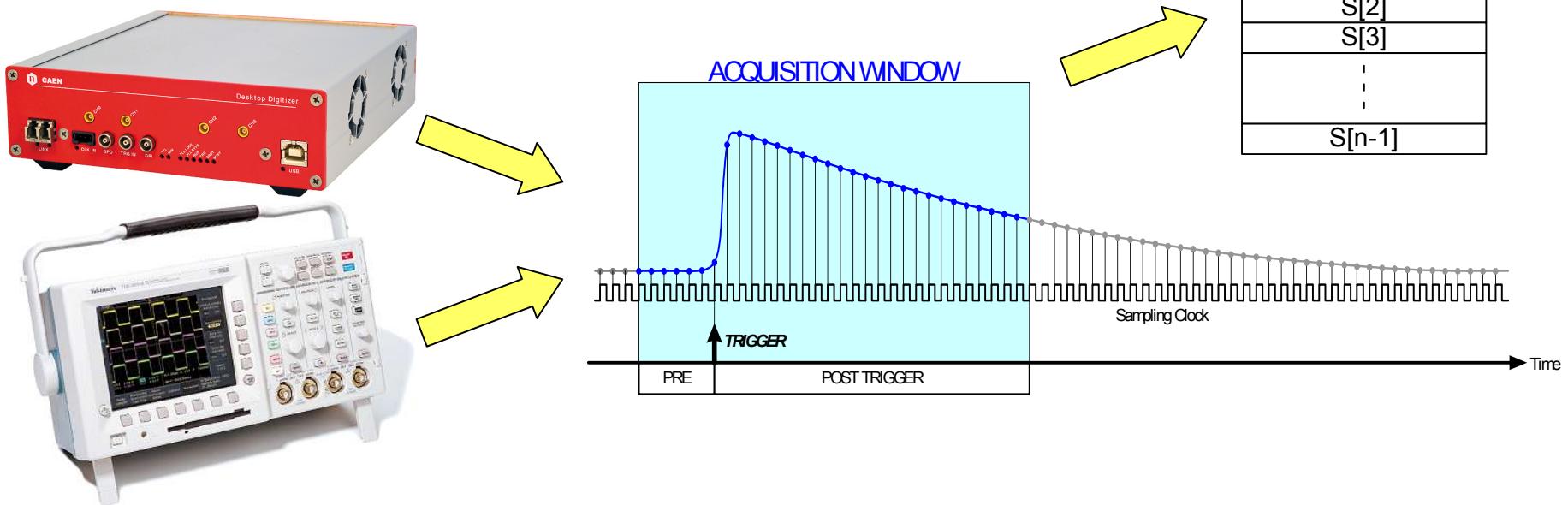


Outline

- Overview on the CAEN Digitizer family
- Description of the hardware of the waveform digitizers
- Use of the digitizers with Digital Pulse Processing for physics applications
- Comparison between the traditional analog acquisition chains and the new fully digital approach
- Multi board systems
- DPP algorithms:
 - Zero suppression
 - Pulse Height Analysis
 - Charge Integration
 - Pulse Shape Discrimination
 - Time measurement

Digitizers vs Oscilloscopes

- The principle of operation of a waveform digitizer is the same as the digital oscilloscope: when the trigger occurs, a certain number of samples is saved into one memory buffer (acquisition window)
- However, there are important differences:
 - no dead-time between triggers (Multi Event Memory)
 - multi-board synchronization for system scalability
 - high bandwidth data readout links
 - on-line data processing (FPGA or DSP)



CAEN Digitizers Highlights



- VME, NIM, Desktop form factors
- VME64X, Optical Link (CONET), USB 2.0
- Memory buffer: up to 10MB/ch (max. 1024 events)
- Multi-board synchronization and trigger distribution
- Programmable PLL for clock synthesis
- Programmable digital I/Os
- Analog output with majority or linear sum
- FPGA firmware for Digital Pulse Processing
- Software for Windows and Linux

- **From 2 to 64 channels**
- **Up to 5 GS/s sampling rate - Up to 14 bit**
- **FPGA firmware for Digital Pulse Processing**

Digitizers Selection Table

Model ⁽¹⁾	Form Factor	N. of ch. ⁽⁴⁾	Max. Sampling Frequency (MS/s)	N. of Bits	Input Dynamic Range (Vpp) ⁽⁴⁾	Single Ended / Differential Input	Bandwidth (MHz)	Memory (MS/ch) ⁽⁴⁾	DPP firmware ⁽⁵⁾
x724	VME	8	100	14	0.5 / 2.25 / 10	SE / D	40	0.5 / 4	PHA
	Desktop/NIM	4 / 2				SE			
x720	VME	8	250	12	2	SE / D	125	1.25 / 10	CI, PSD
	Desktop/NIM	4 / 2				SE			
x721	VME	8	500	8	1	SE / D	250	2	no
x731	VME	8 - 4	500 - 1000	8	1	SE / D	250/500	2/4	no
x730	VME	8	500	12	2	SE / D	250	1.25 / 10	PSD
	Desktop/NIM	4 / 2				SE			
x751	VME	8 - 4	1000 - 2000	10	1	SE / D	500	1.8 / 14.4 - 3.6 / 28.8	PSD
	Desktop/NIM	4 - 2				SE			
x761	VME	2	4000	10	1	SE / D	TBD	7.2 / 57.6	no
	Desktop/NIM	1				SE			
x740	VME	64	62.5	12	2 / 10	SE	30	0.19 / 1.5	no
	Desktop/NIM	32							
x742	VME	32+2	5000 ⁽²⁾	12	1	SE	600	0.128 / 1 ⁽³⁾	no
	Desktop/NIM	16+1							

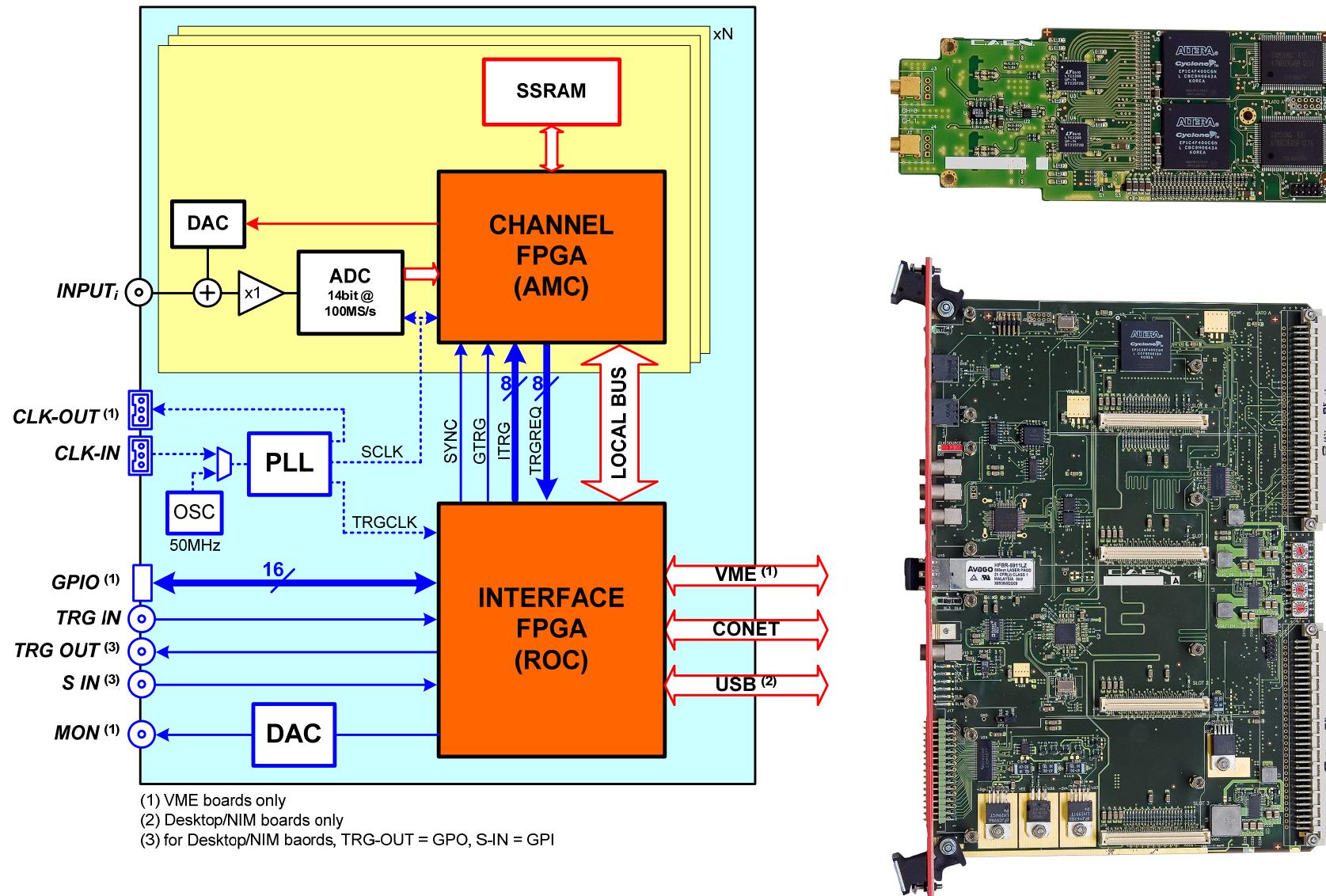
(1) The x in the model name is V1 for VME, VX1 for VME64X, DT5 for Desktop and N6 for NIM

(2) Sampling frequency of the analog memory (switched capacitor array); A/D conversion takes place at lower speed (dead-time)

(3) The memory size for the x742 is 128/1024 events of 1024 samples each

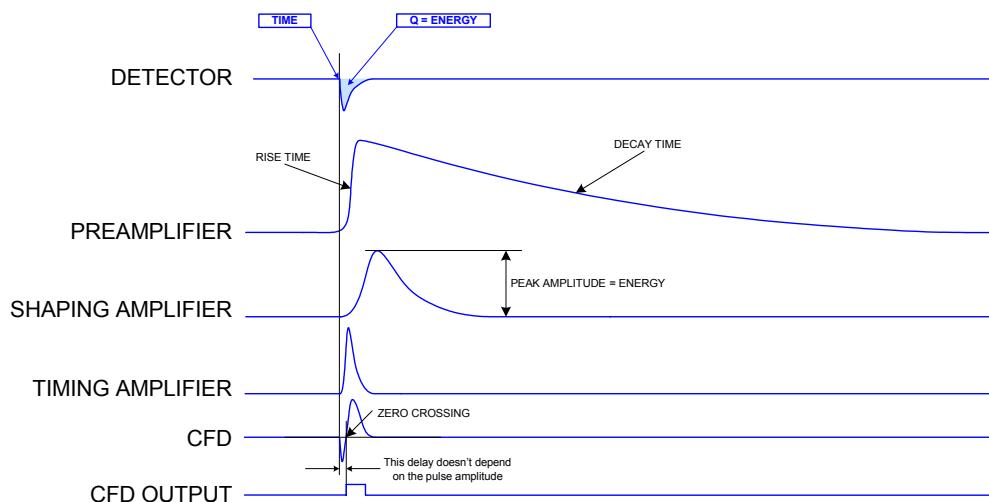
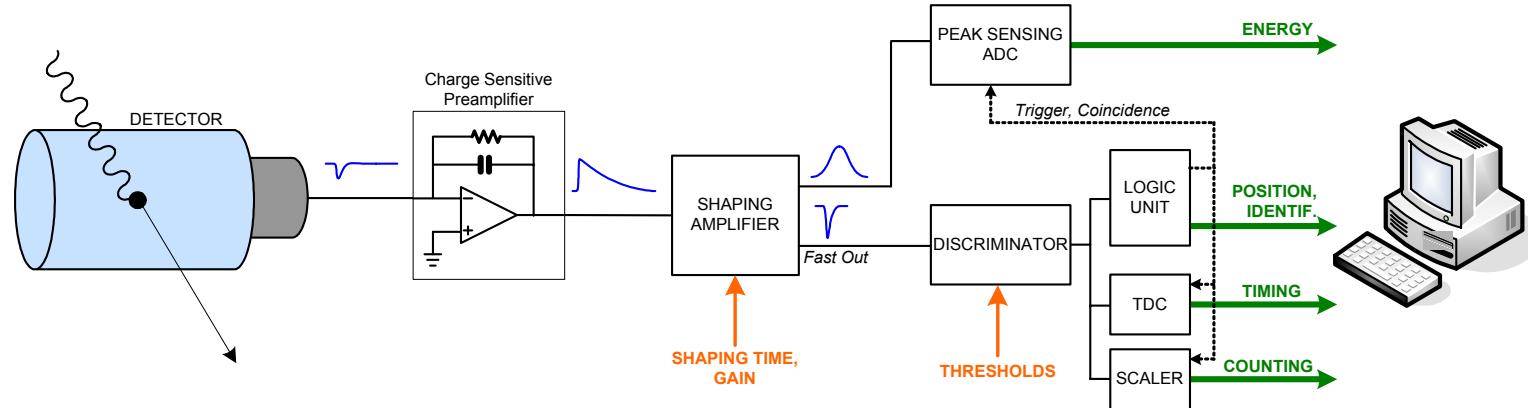
(4) The indication "size 1/size 2" denotes different options

(5) DPP-PHA: Pulse Height Analysis (Trapezoidal Filters), DPP-Cl: Charge Integration (digital QDC), DPP-PSD: Pulse Shape Discrimination



- Traditionally, the acquisition chains for radiation detectors are made out of mainly analog circuits; the A to D conversion is performed at the very end of the chain
- Nowadays, the availability of very fast and high precision flash ADCs permits to design acquisition systems in which the A to D conversion occurs as close as possible to the detector
- **The data throughput is extremely high: it is no possible to transfer raw data to the computers and make the analysis off-line!**
- On-line digital data processing is needed to extract only the information of interest (Zero Suppression & Digital Pulse Processing)
- The aim of the DPP for Physics Applications is to provide FPGA algorithms able to make in digital the same functions of analog modules such as Shaping Amplifiers, Discriminators, Charge ADCs, Peak Sensing ADCs, TDCs, Scalers, Coincidence Units, etc.

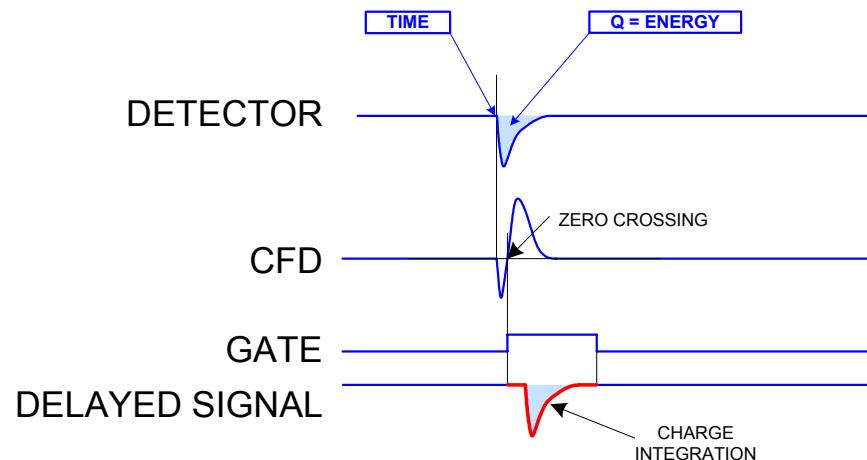
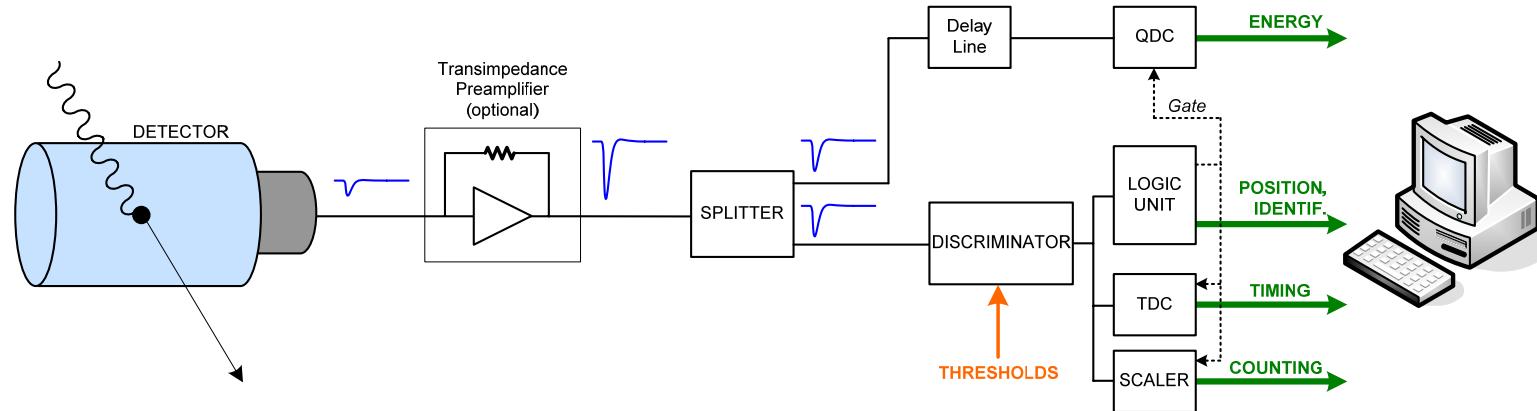
Traditional chain for spectroscopy



- Typically used with semiconductor detectors (Si, Ge)
- The preamp. output signal is rather slow (typ. decay time = 50us)
- Very high energy resolution (good S/N ratio)

Traditional chain: another example

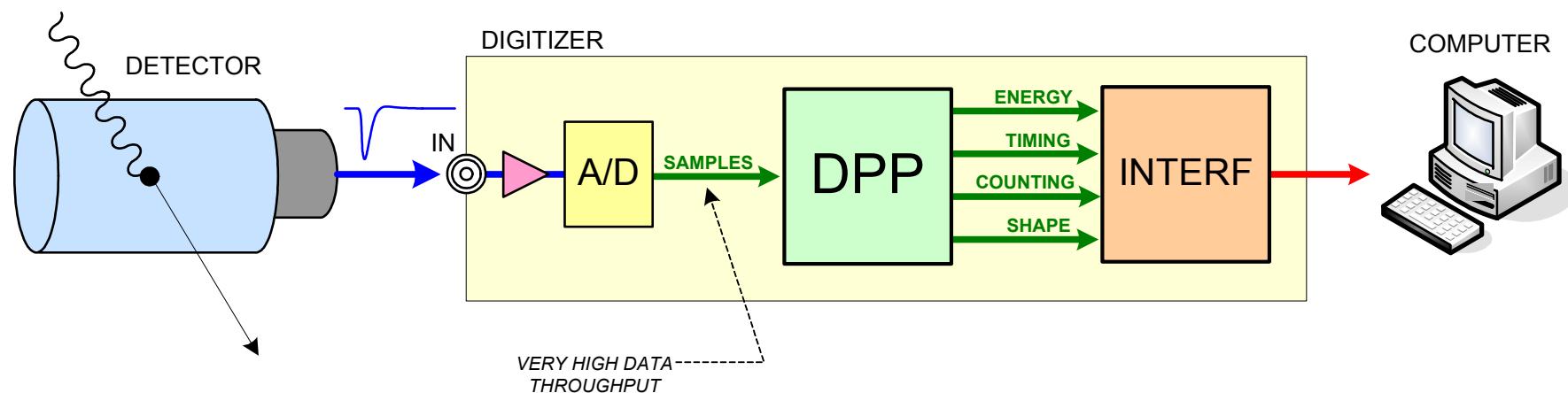
trans-impedance (current sensitive) preamplifier



- Typ. used with scintillators + PMTs or SiPMs
- The preamplifier is optional (the gain is already in the PMT)
- Fast signals (typ. 10-100ns)

Benefits of the digital approach

- One single board can do the job of several analog modules
- Full information preserved: *A/D conversion as early as possible, data reduction as late as possible*
- Reduction in size, cabling, power consumption and cost per channel
- High reliability and reproducibility
- Flexibility (different digital algorithms can be designed and loaded at any time into the same hardware)



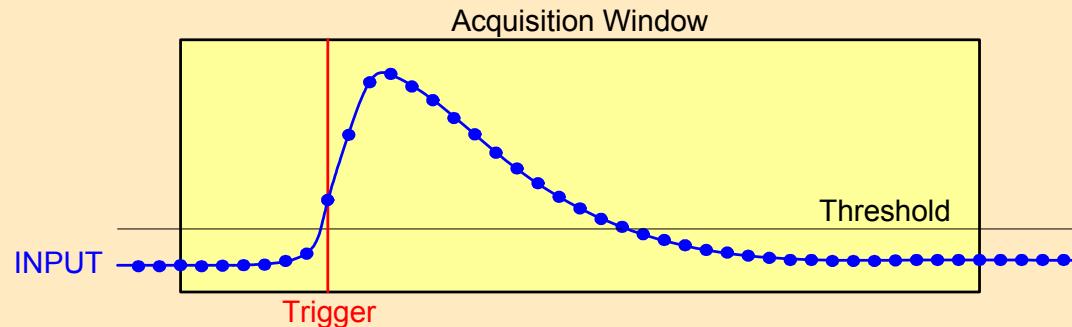
- With the standard firmware, the digitizer operates in oscilloscope mode: with the trigger, the list of samples (raw data) belonging to the acquisition window is saved to the memory of the board
- The trigger can be external or internal (threshold crossing); in both cases, it is common to all the channels

With the DPP Firmware, you can:

- Identify input pulses and generate a local trigger on them
- Calculate the time of arrival of the trigger
- Subtract the baseline
- Calculate the energy (usually pulse height or charge)
- Build an event made of a configurable combination of Trigger Time Stamp, Pulse Height/Charge and raw waveforms (i.e. series of ADC samples belonging to a programmable size acquisition window)
- Save events into a memory buffer and manage the readout through the Optical Link, USB or VME
- Detect pile-up conditions and manage count loss (dead-time)
- Implement coincidences between channels within the board as well as across different boards

Acquisition mode: raw waveform vs DPP

STD FW

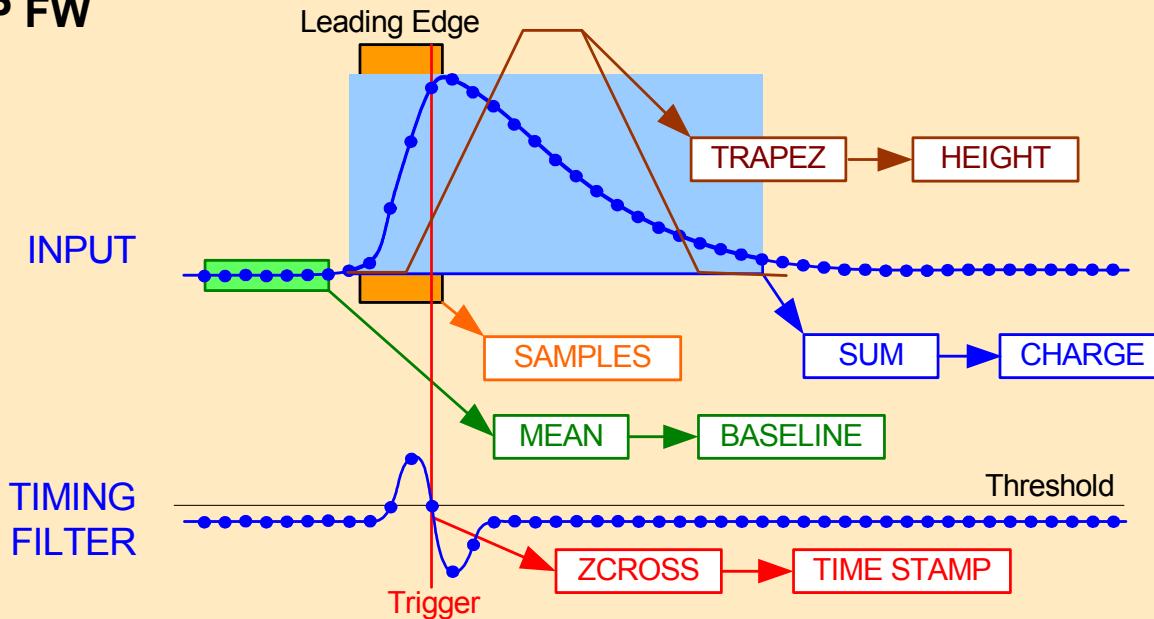


EVENT DATA

S1
S2
S3
S4
S5
S6
S7
Sn

Typ. Nsample > 1K

DPP FW



EVENT DATA

TIME STAMP
CHARGE
BASELINE
HEIGHT
S1
S2
S3
S4

Typ. Nsample < 100

What does *synchronization* mean?

1. same sampling clock propagated to all flash ADCs:
 - ✓ External clock in/out⁽¹⁾; first board can act as a clock master and distributes the clock to many slaves in daisy chain
 - ✓ PLL for clock synthesis; lock to an external clock reference
 - ✓ Programmable Phase Adjust for cable delay compensation
2. same T zero for the time stamps:
 - ✓ Sync Input for a simultaneous start/stop of the acquisition and/or for time stamp reset
 - ✓ Sync Distribution through the boards in daisy-chain (via TrgOut)
 - ✓ Use of the first trigger to start the acquisition
3. trigger propagation and correlation:
 - ✓ External Trigger In/Out (NIM/TLL on LEMO connectors)
 - ✓ Global or individual Trigger propagation through LVDS GPIOs⁽¹⁾
 - ✓ Neighbour triggering options for segmented and clove detectors

(1) for VME modules only

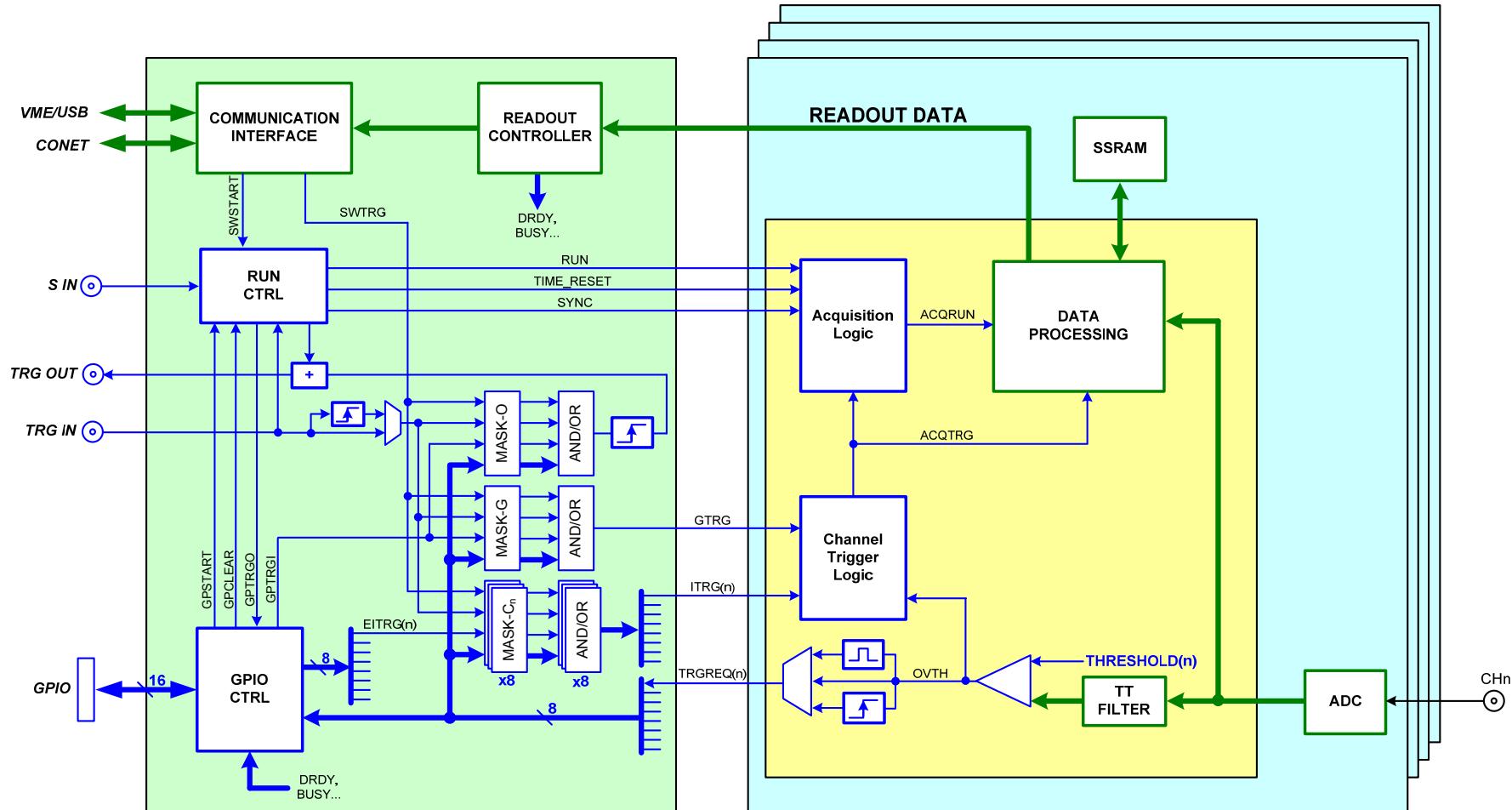
Hardware approach

- Propagate local triggers from each channel to the others within the board
- Trigger from other channels (requests) can be used as trigger validation
- Apply individual trigger masks and simple combinatorial logics on board (AND, OR, Majority)
- Use GPIOs on the front panel to propagate individual trigger inputs/outputs from/to external logic boards (e.g. V1495)

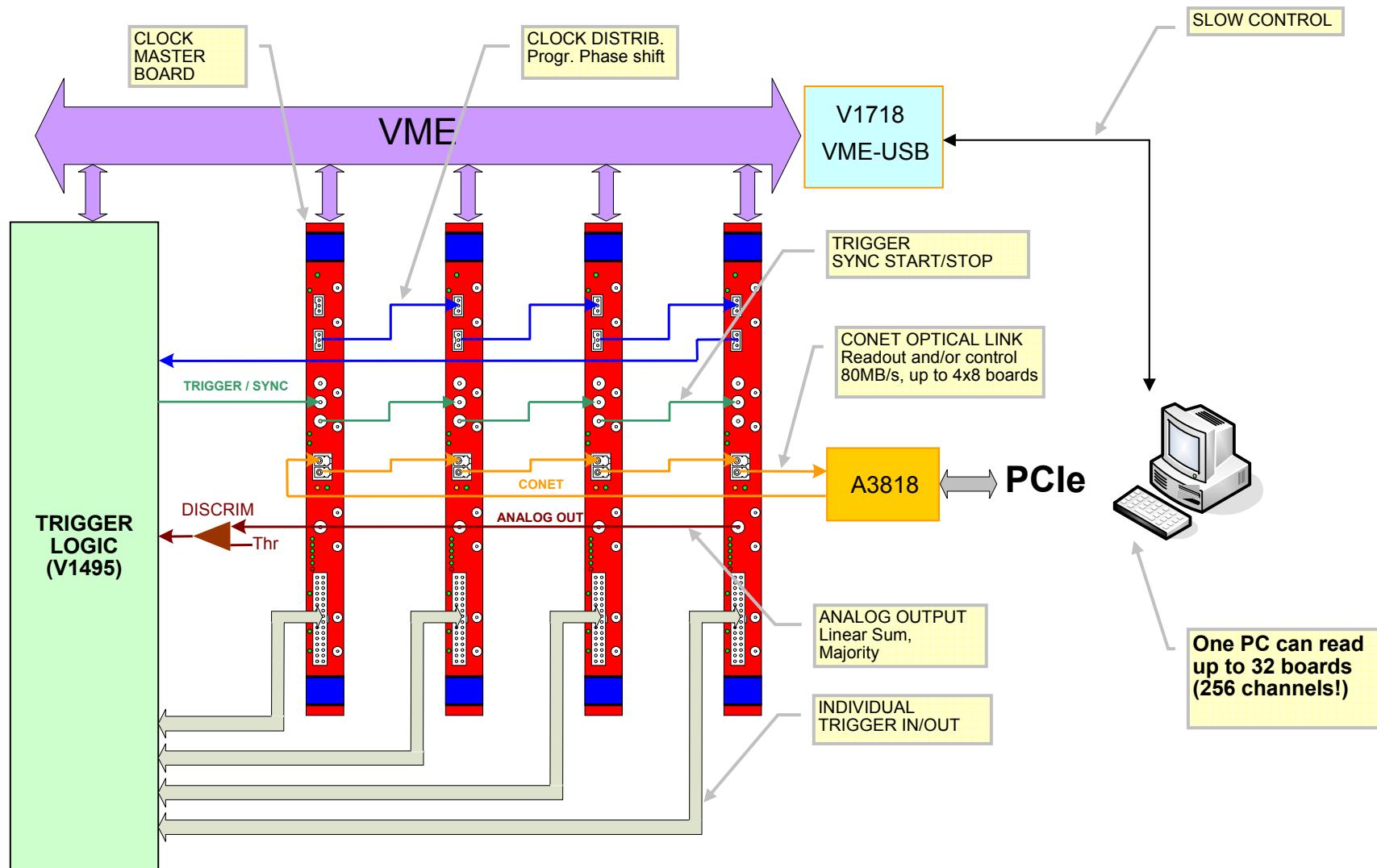
Software approach

- Read all events as long as you have enough bandwidth (i.e. make data suppression as late as you can): preserve the information!
- In list mode, the bandwidth requirement is very low (e.g. 8 bytes per event)
- Coincidence, anticoincidence, validation, etc. can be applied off-line in the software using the time stamps

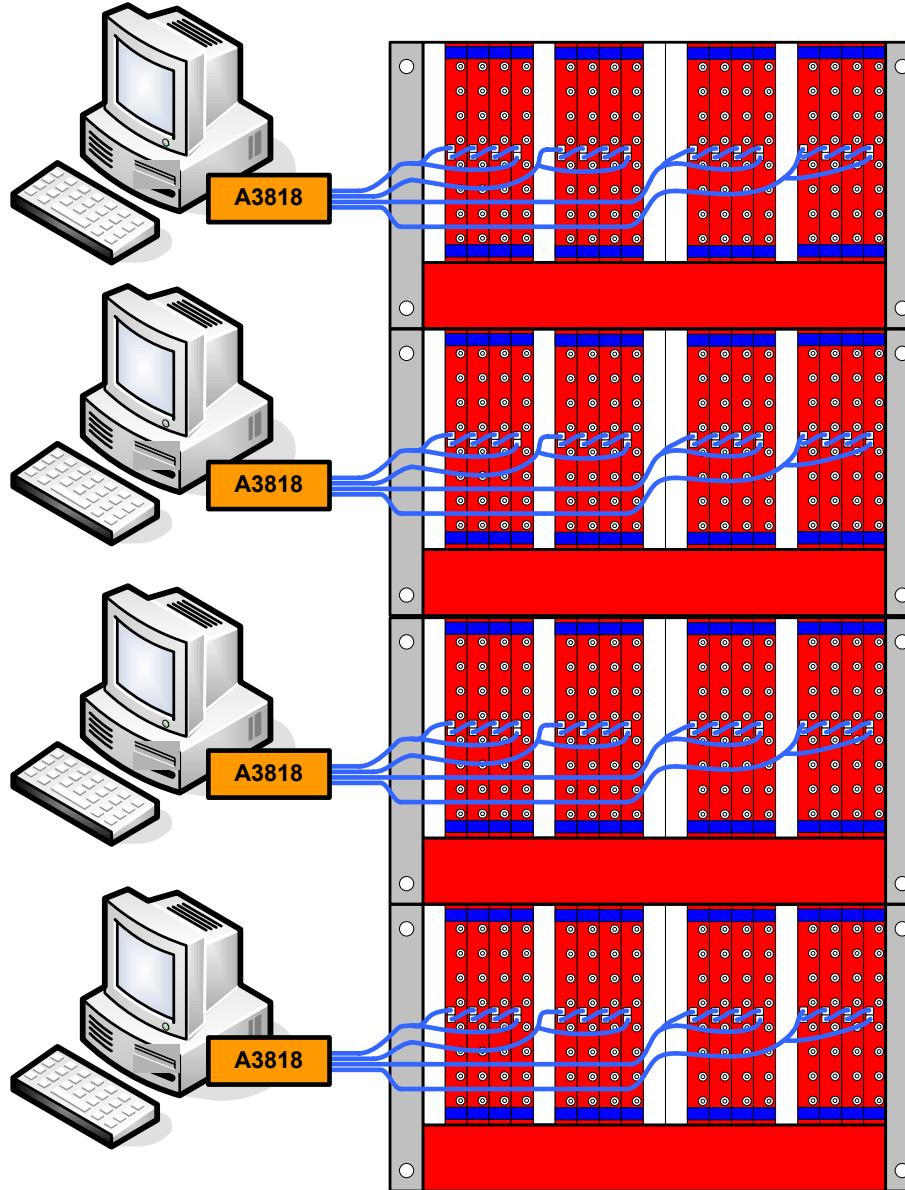
Trigger Logic Block Diagram



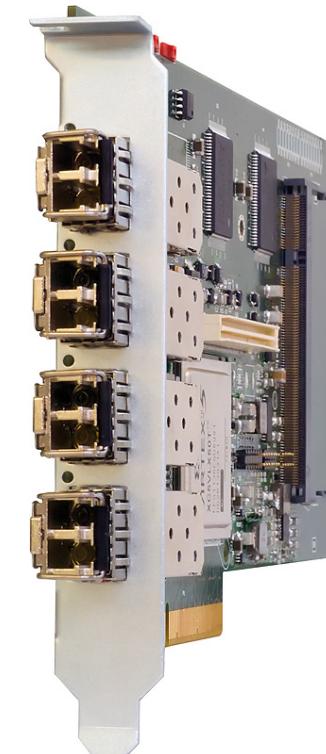
Example of System Integration



Example of a GB/s Readout



- 64 V1751 modules in 4 VME crates
- 512 channels (10 bit @ 1GHz)
- 4 A3818s 4 link PCIe cards
- 16 parallel CONET links
- 4 digitizers daisy chained
- Readout Bandwidth = ~2 MB/s/ch
- Total aggregate throughput = ~ 1GB/s

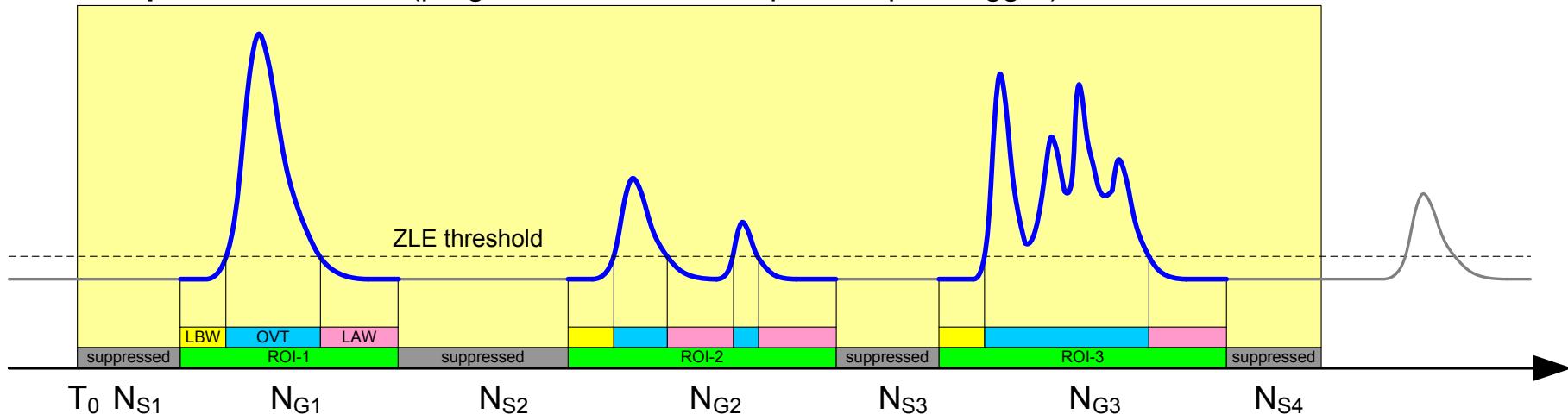


A3818
PCIe 8x
CONEt Controller

ZERO SUPPRESSION

- The zero suppression (**Zero Length Encoding**) in a waveform digitizer consists in removing from the acquisition window the parts of the waveform that don't contain useful information
- DPP only used for the pulse identification (Region Of Interest) and not to extract relevant quantities from the waveforms
- Typically used in beam experiments where the trigger is common to all channels, but only few of them contains events
- Available in the standard firmware of the x724, x720, x721 and x731; current version of the ZLE suffers from a readout bandwidth reduction
- A new ZLE algorithm that guarantees the best readout performances is under development for the x720 and x751

Acquisition Window (programmable size with pre and post trigger)



Look Back Window: programmable size

OverThreshold: lasts as long as the signal is over threshold

Look Ahead Window: programmable size; can be retriggered

T_0 Time Stamp of the first sample of the Acquisition Window

N_S Number of skipped samples belonging to the suppressed region

N_G Number of good samples belonging to the ROI

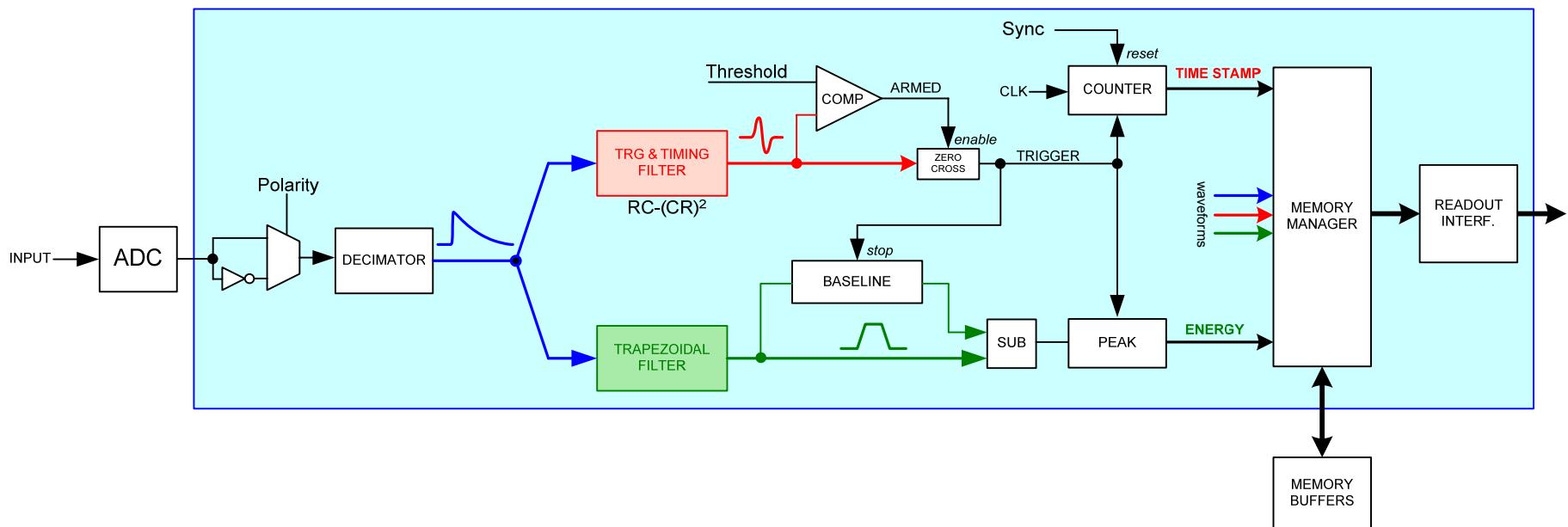
Readout Data

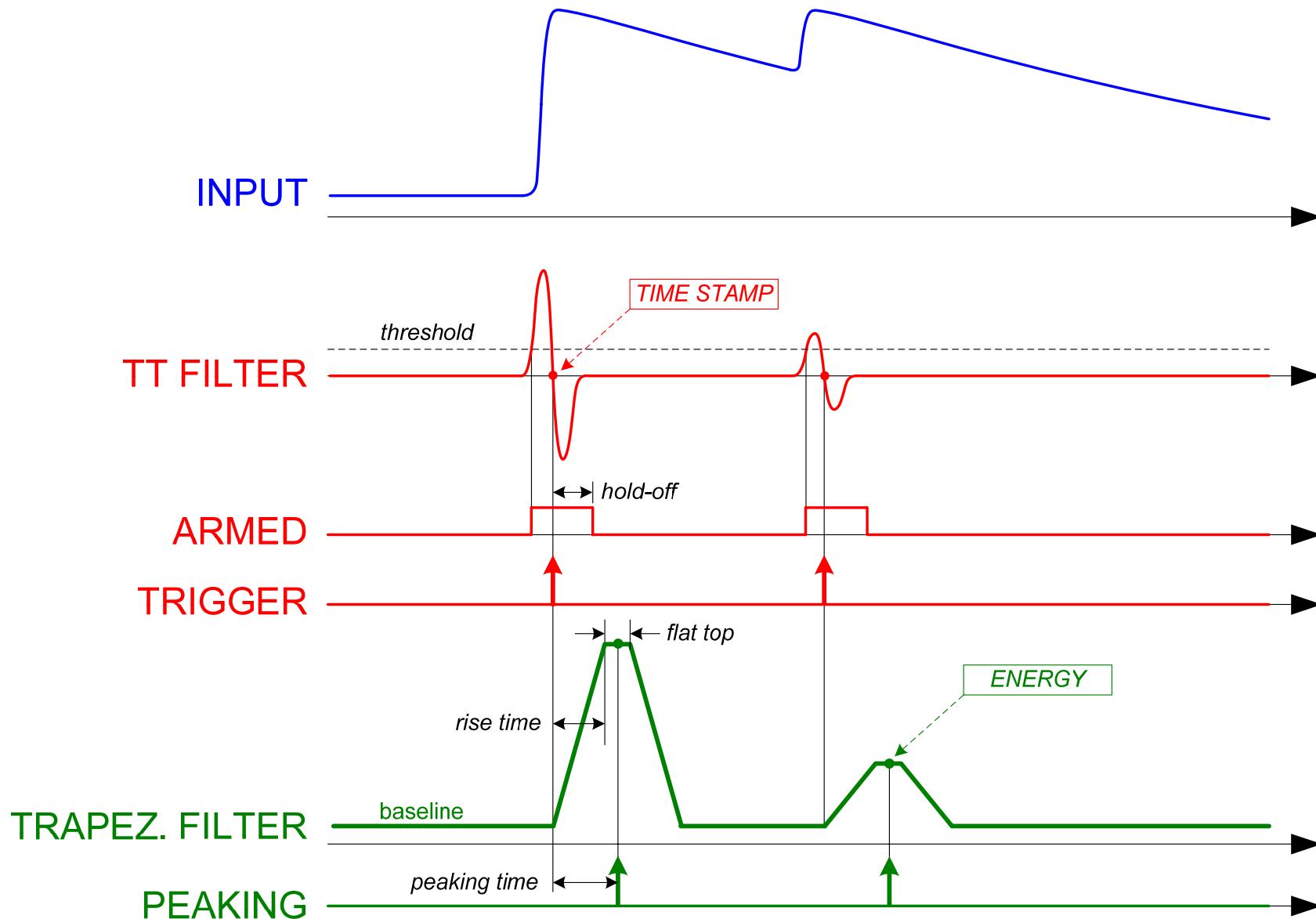
T_0
N_S1
$NG1$
samples of ROI-1
N_S2
$NG2$
samples of ROI-2
N_S3
$NG3$
samples of ROI-3
N_S4

DPP-PHA
PULSE HEIGHT ANALYSIS

- Digital implementation of the shaping amplifier + peak sensing ADC (Multi-Channel Analyzer)
- Charge sensitive preamplifier directly connected to the digitizer
- Implemented in the 14 bit, 100MSps digitizers (mod. 724)
- Provides pulse height, time stamp (10ns) and optionally raw data
- Pile-up rejection, Baseline restoration, ballistic deficit correction
- Low dead time => high counting rate (up to 1Mcps)
- Best suited for high resolution spectroscopy (HPGe and Si detectors)
- Also suitable for homeland security and biomedical applications
- Can work with segmented detectors (synchronizations, coincidences and neighbour triggering)

- **Decimator:** reduces sampling rate and increases resolution
- **Trigger & Timing Filter:** identifies pulses and generates triggers and time stamps
- **Energy Filter:** shapes the input signal (trapezoid), restores the baseline and calculates the pulse height
- **Memory Manager:** builds the events as a combination of time stamp, energy and waveforms (samples)



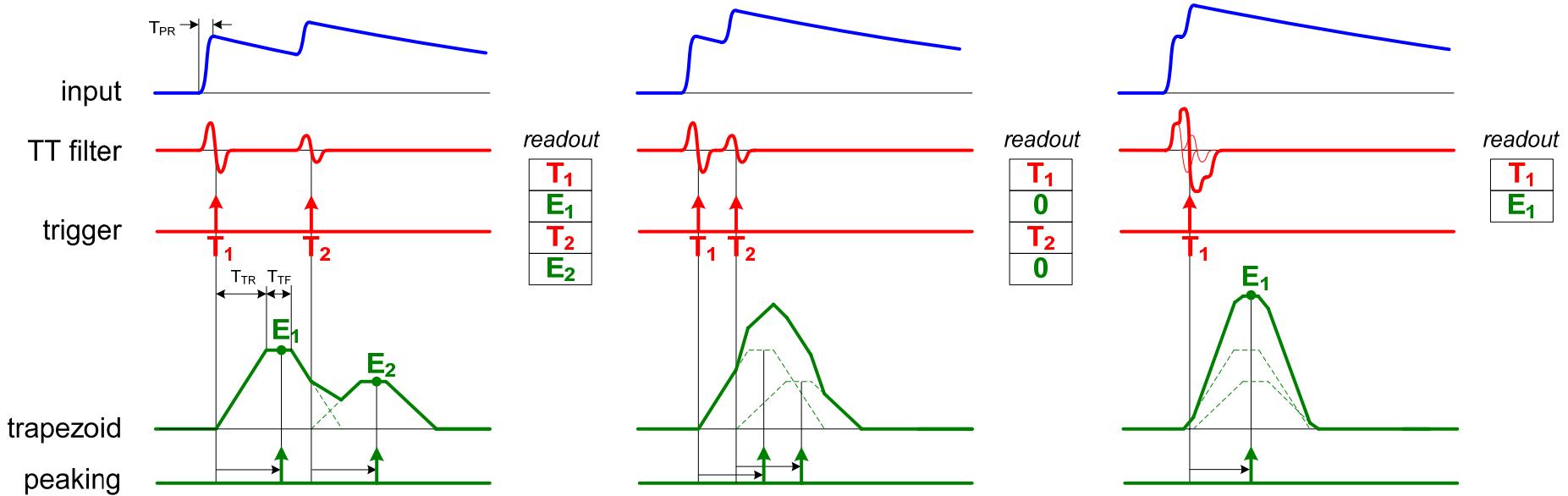


- Pulse triggering is the basis for all DPP and Zero Suppression algorithms
- Fast Shaping filter: digital version of the RC-CR^N filter (N=1, 2)
- Immune to baseline fluctuation and low frequency noise (ground loop)
- Pulse identification also with the presence of pile-up
- High frequency noise rejection (RC smoothing filter)
- Can operate as a digital CFD
- Zero crossing for precise timing information
- Off-line interpolation to overcome the sampling period granularity
- Zero crossing of CFD can also be used for ***Rise Time Discrimination*** (identification of double pulses piling up within their rise time)

- The trapezoidal shaper (**Moving Window Deconvolution**) is the digital version of the gaussian shaper of the analog spectroscopy amplifiers
- The rise/fall time of the trapezoid corresponds to the shaping time: higher rise times result in better resolution but also higher probability of pile-up (dead time)
- Also the trapezoidal shaping requires pole-zero cancellation (controlled by a digital parameter that represents the exponential decay time)
- The baseline is calculated by averaging a programmable number of samples before the start of the trapezoid
- Flat top duration, peaking time (position of the peak in the flat top) and peaking averaging are also programmable for an optimum ballistic deficit correction

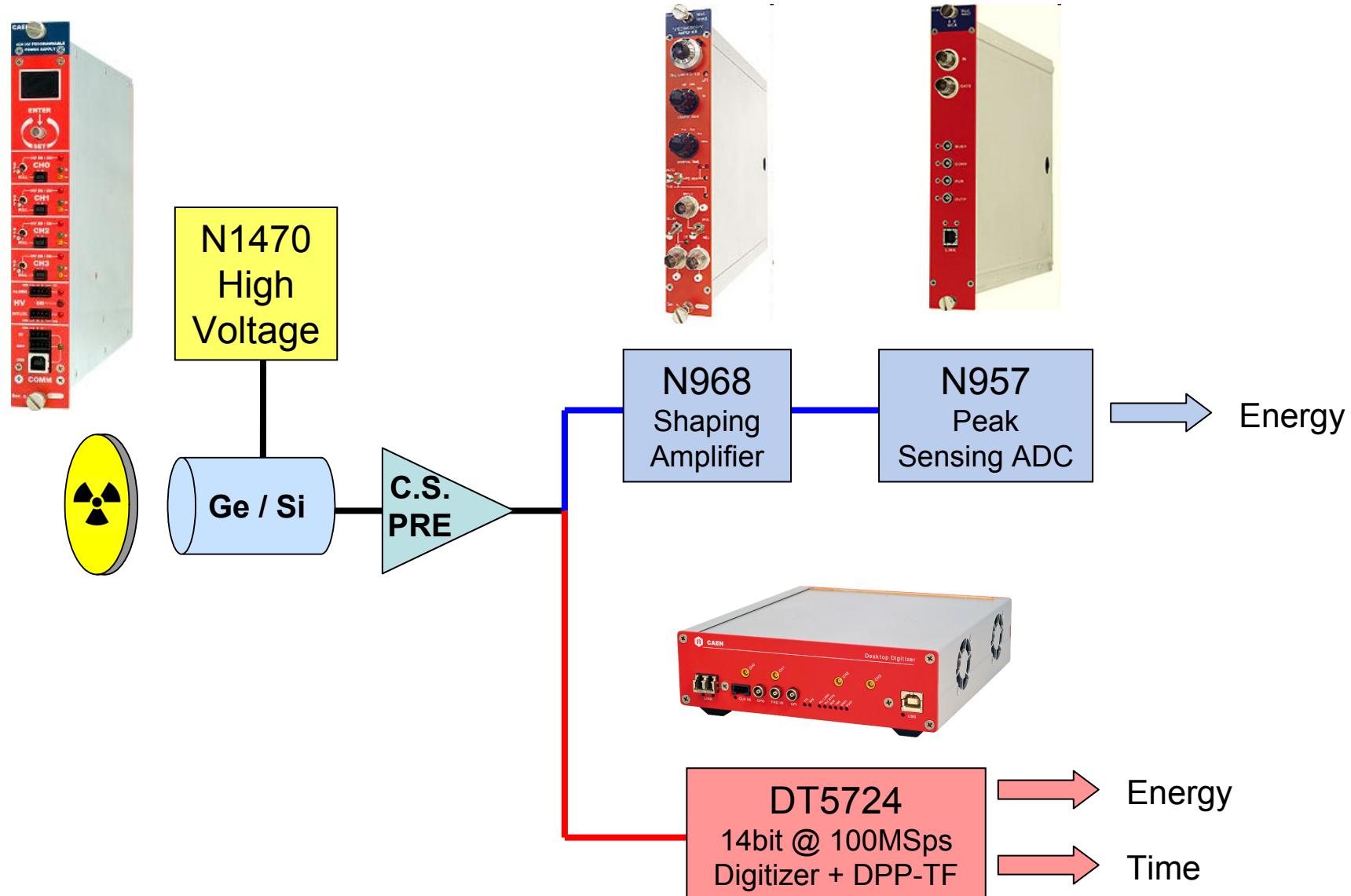
Pile-up in the Trapezoidal Filter

- **Case 1:** $\Delta T > T_{TR} + T_{TF}$ (2nd trapezoid starts on the falling edge of the 1st one). Both energies are good (no pile-up events)
- **Case 2:** $\sim T_{PR} < \Delta T < T_{TR} + T_{TF}$ (2nd trapezoid starts on the rising edge or flat top of the 1st one). Pulse height calculation is not possible, no energy information is available (pile-up events); still two time stamps.
- **Case 3:** $\Delta T < \sim T_{PR}$ (input pulses piling up on their rising edge). The TT filter doesn't distinguish the double pulse condition. Only one event is recorded (energy sum). The Rise Time Discriminator might mitigate this unwanted effect.



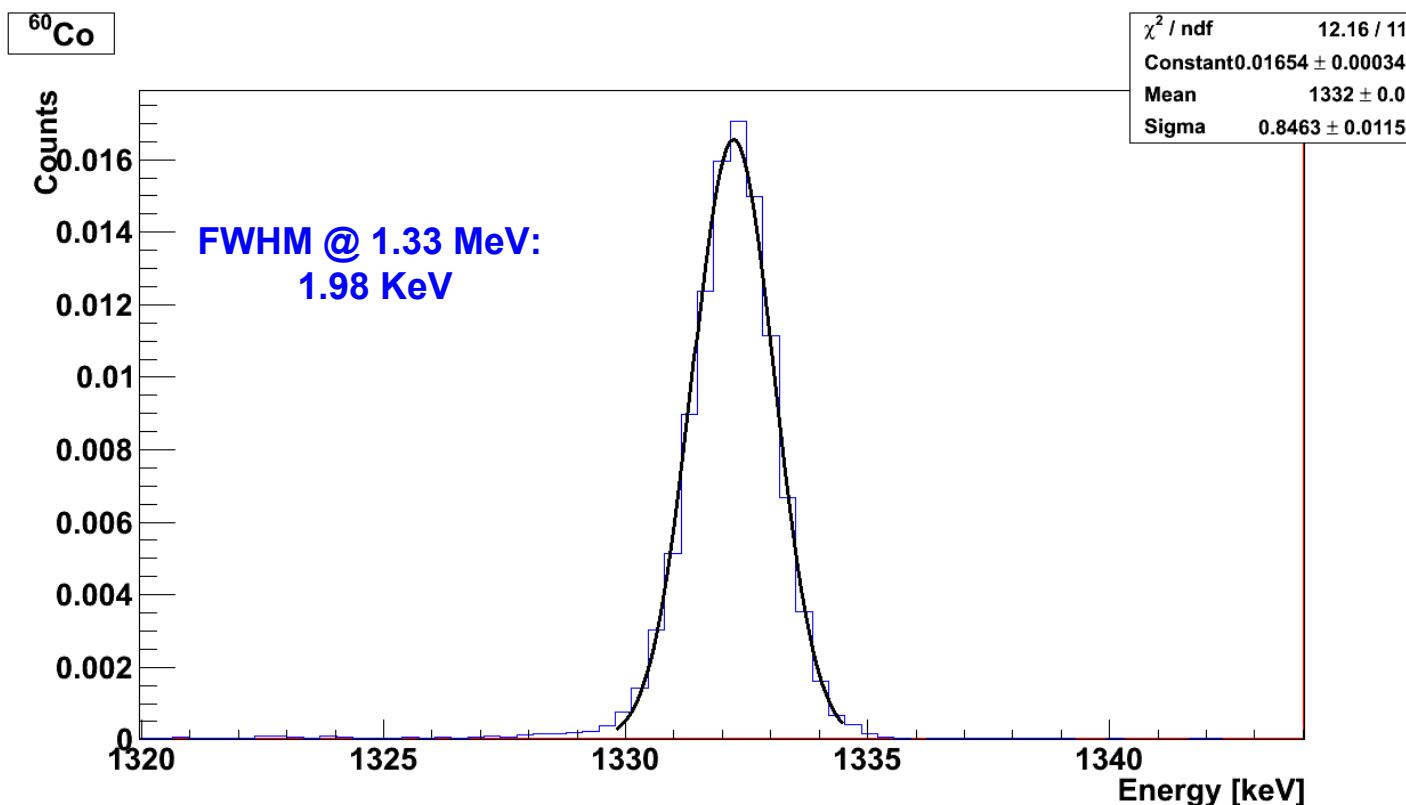
- Unlike the analog chain, in the DPP-PHA there is **no conversion time**
- The A/D conversion and the pulse processing is always alive; dead time in the energy filter is only given by the trapezoid overlap ($T_{rise} + T_{flat}$)
- Although pile-up causes the loss of energy values, the **timestamps is given for almost all pulses**: therefore, the true rate can be calculated
 - $DeadTime = RealTime * (Energy\ Count / Time-Stamp\ Count)$
- Double pulse resolution \approx Rise Time (two pulses separated by at least the pulse rise time can be distinguished)
- The **Rise Time Discriminator** allows double pulses piling up on the rising edge to be detected and counted twice (the relevant energies are discarded)
- Residual multiple pulses that cannot be distinguished (despite the RTD) can be counted on a statistical basis
- The x724+DPP-PHA operates in List Mode and the histogram is calculated off-line: the 'dead-time' correction is done by the readout software that uses the time stamps of the missed energies in order to dynamically redistribute them onto the energy spectrum

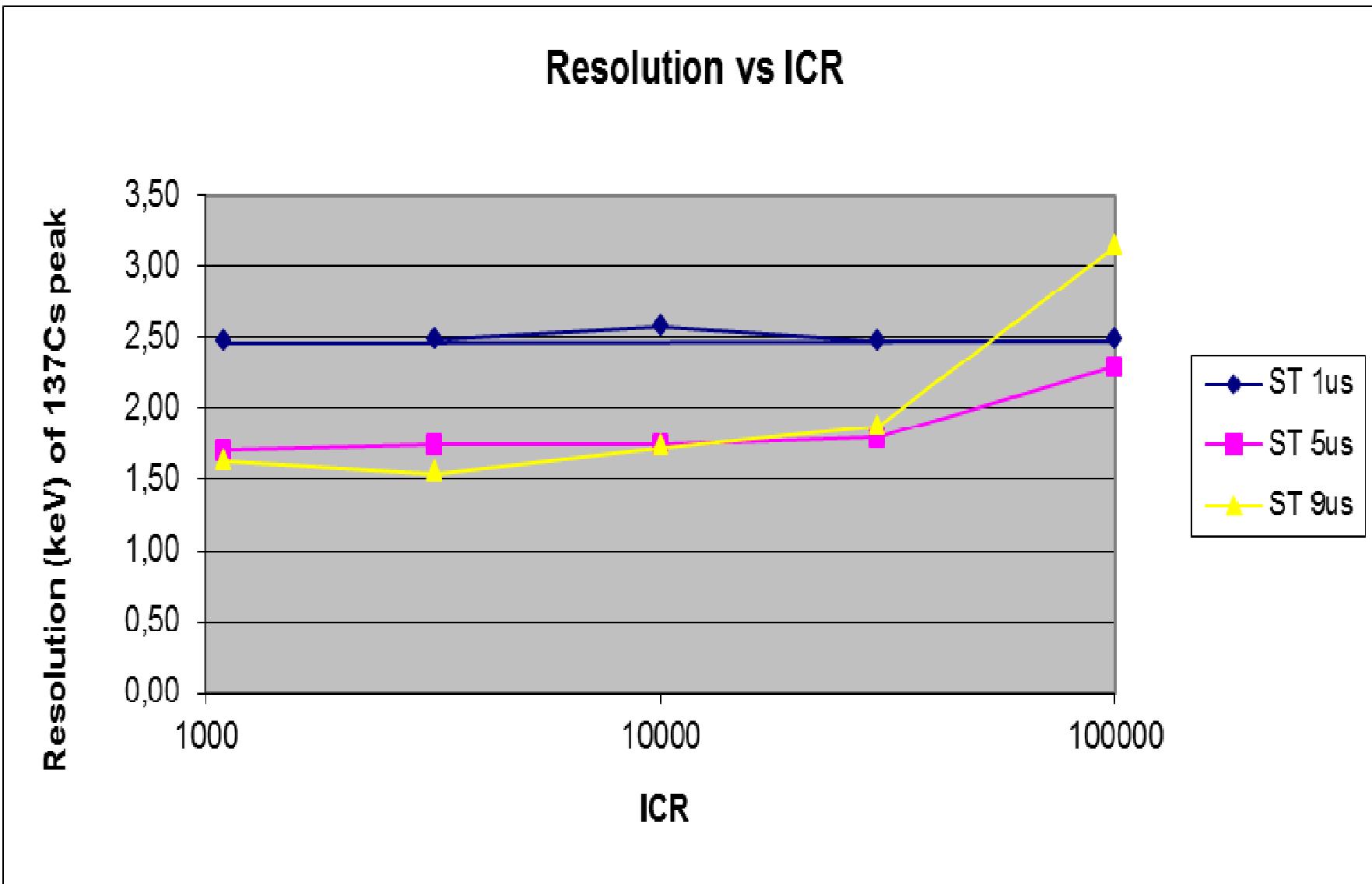
DPP-TF vs Analog Chain set-ups

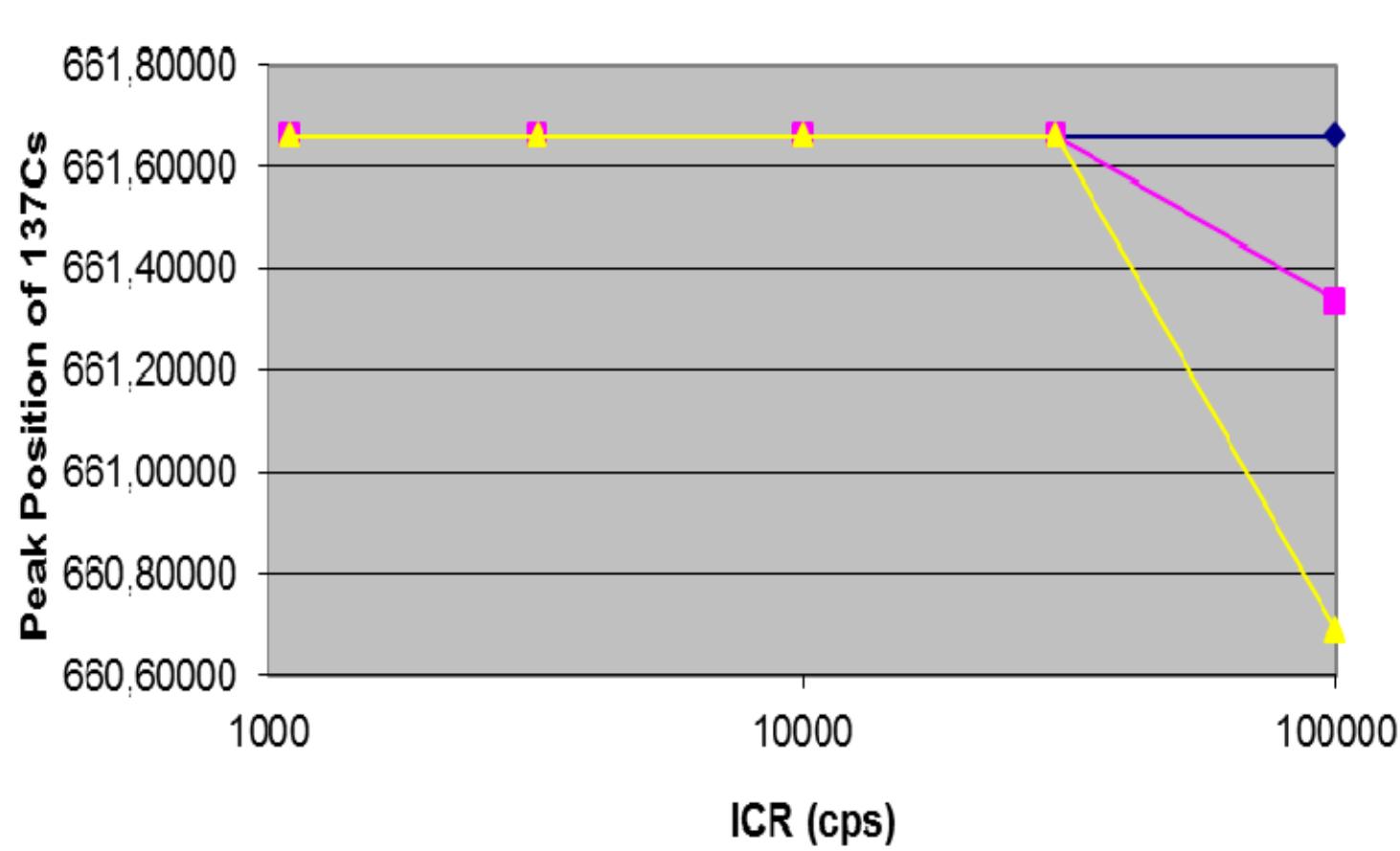


Test Results with HPGe detectors

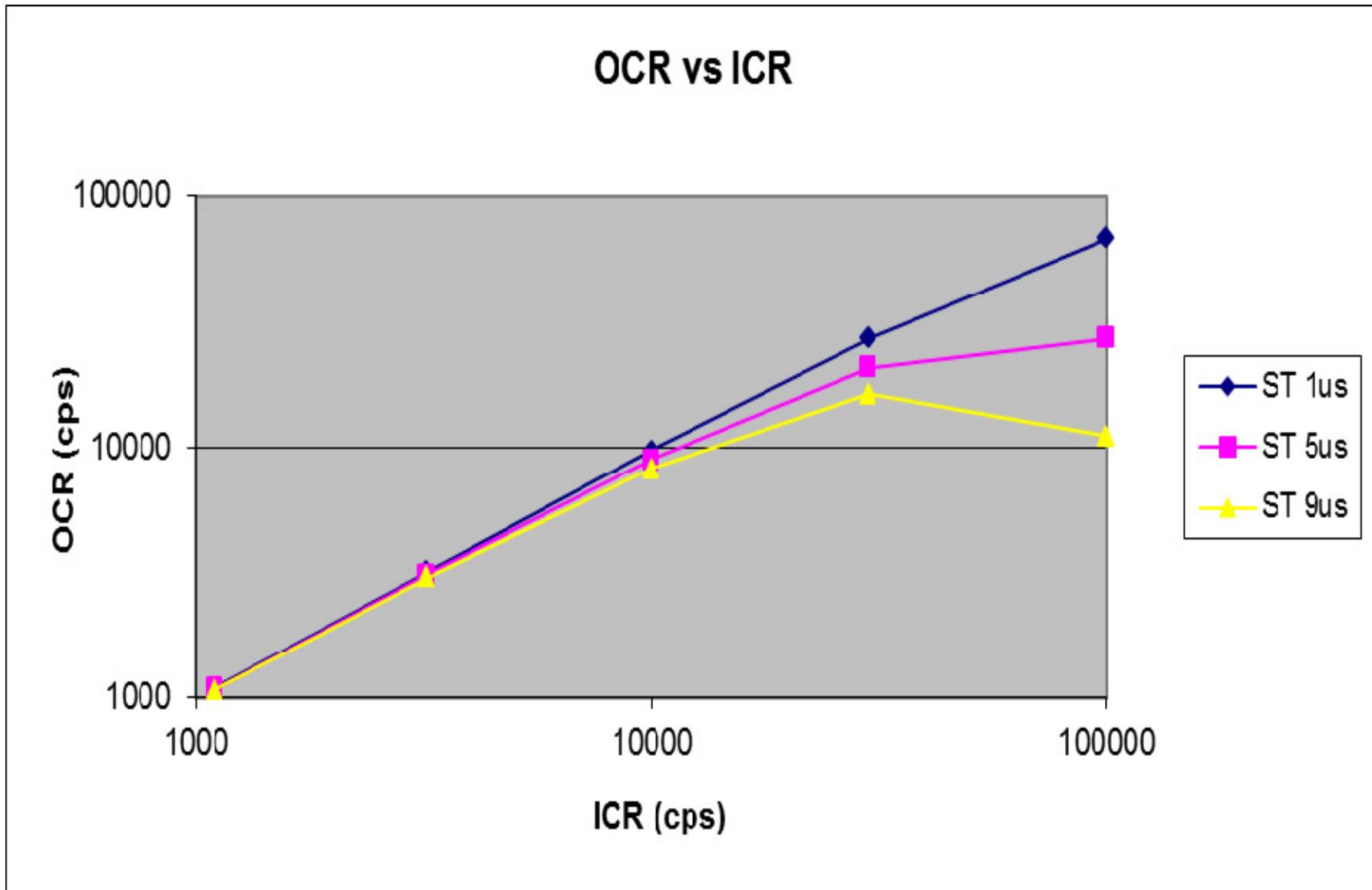
- Preliminary tests performed at LNL (Legnaro - Italy) on Nov-2008 and Feb-2009
- Duke University on Jul-2010
- University of Palermo (Dep. Of Phisycs) on Jan 2011. Detector: Ortec HP-Ge mod. GEM40P4 cooled with an X-cooler (Peltier). Preamp: A257P (time constant = 100 μ s).
- Saclay (France), lab of radiochemistry on March 2011. Different types of detectors and sources.



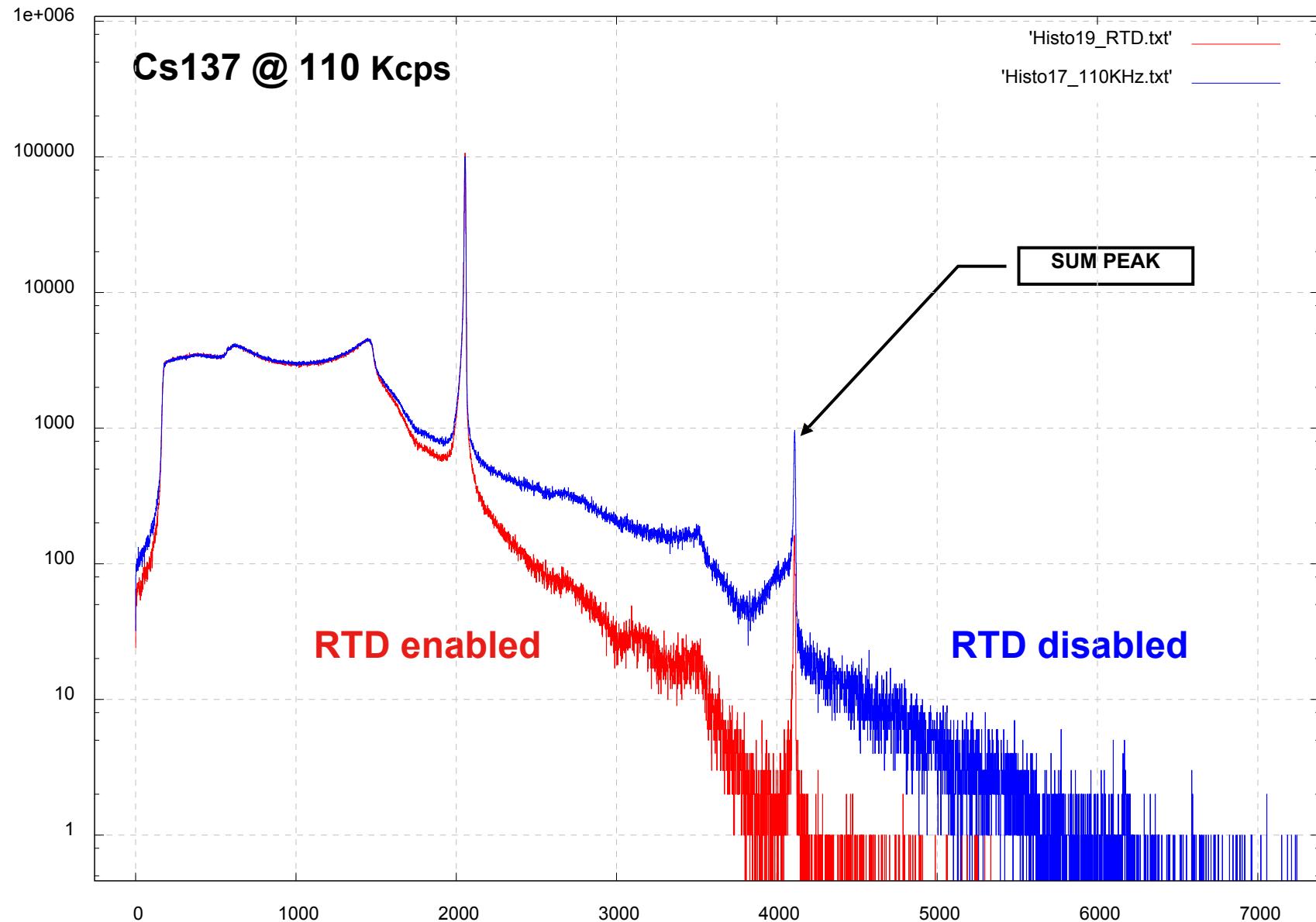




Test Results with HPGe (III)

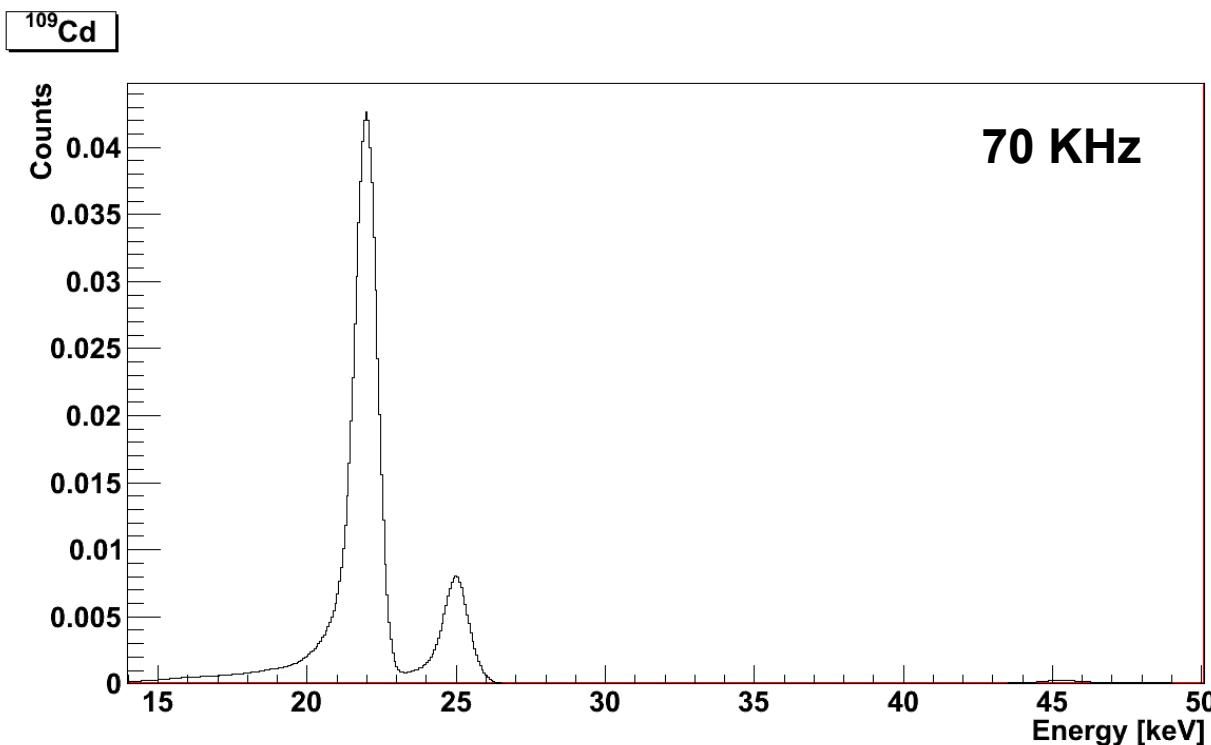


Test Results with HPGe (IV)

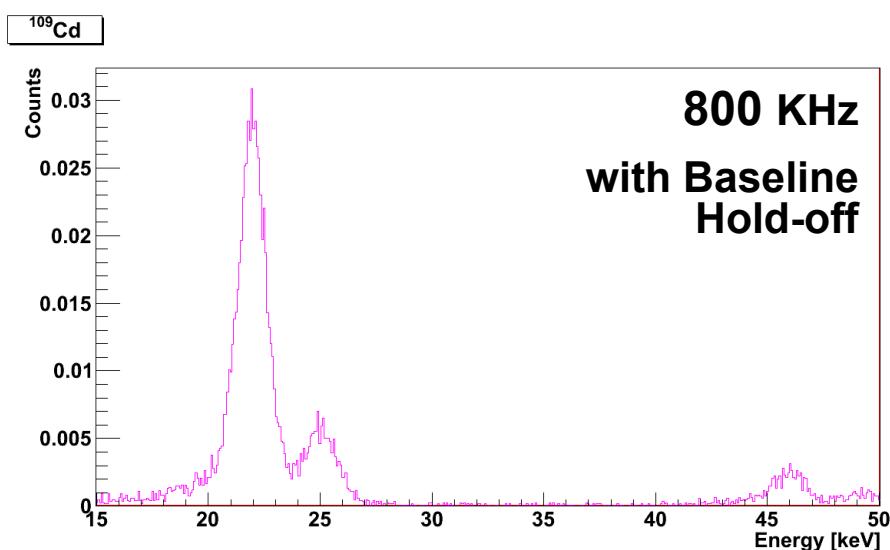
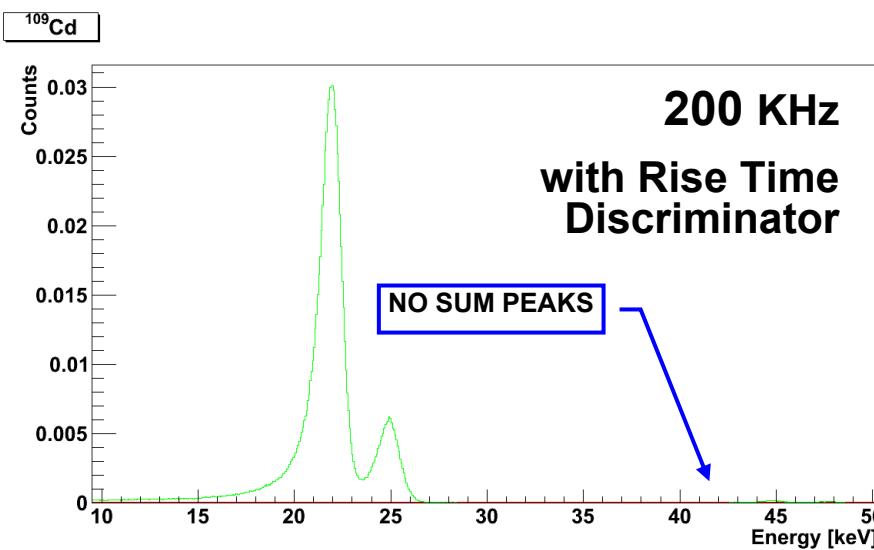
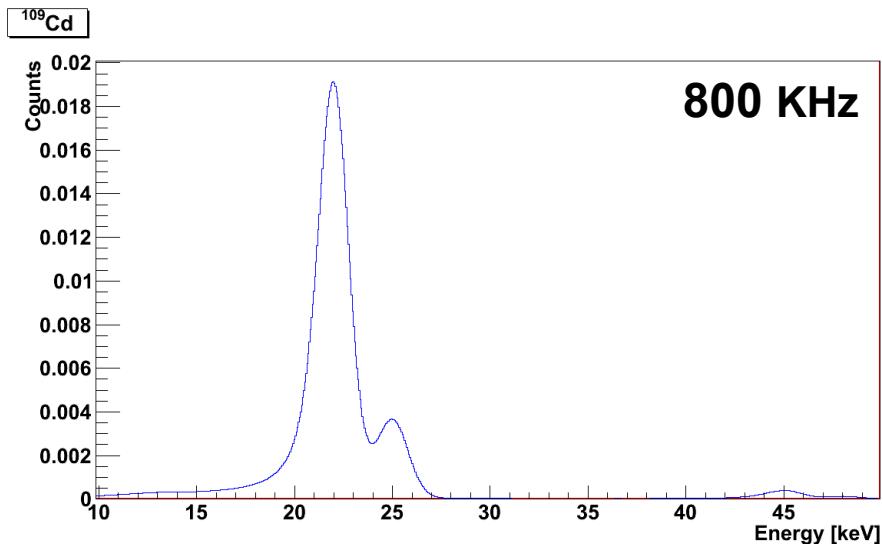
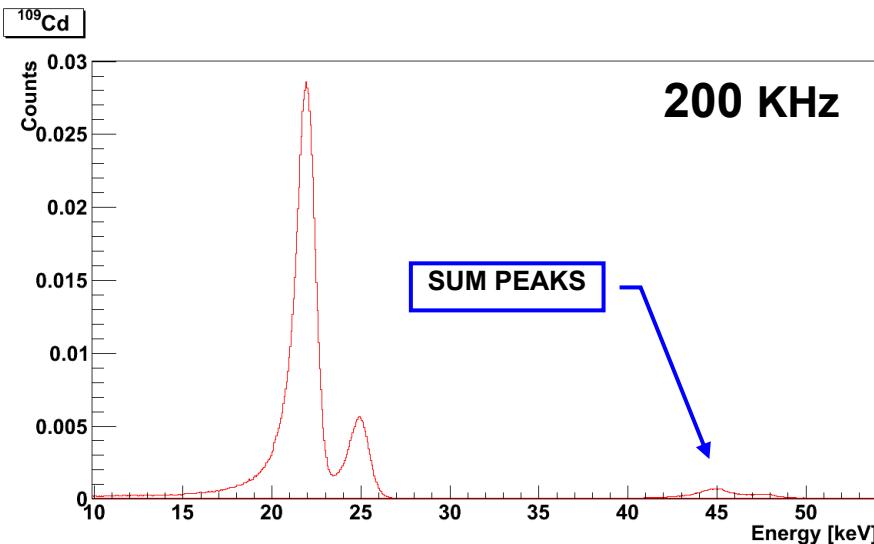


Test Results with CdTe at high rate (I)

- Tests executed at University of Palermo on February 2011
- Detector: CdTe from Amptek with embedded FET integrator
- Rise Time = 140 ns, Decay Time = 100 μ s
- Source = ^{109}Cd , X-ray peaks at 22 and 25 KeV
- Tested at 70, 200 and 800 KHz with different DPP parameters



Test Results with CdTe at high rate (II)



- CAEN is designing a full featured 2 channel, 16K Digital Pulse Height Analyzer (**DPHA**) in the form factor of the Desktop Digitizers
- Two BNC inputs with four SW selectable dynamic ranges
- Two SHV high voltage supplies for the detector bias ($\pm 6\text{kV}$, 1mA)
- Two DB9 with low voltage supplies for the pre-amplifiers ($\pm 12\text{V}$, $\pm 24\text{V}$), temp. sensor and HV inhibit; the latter also on BNC (back panel)
- Readout from USB (30MB/s) and Optical Link (80MB/s)
- Drivers, Libraries and Readout Software for Windows, Linux and LabView

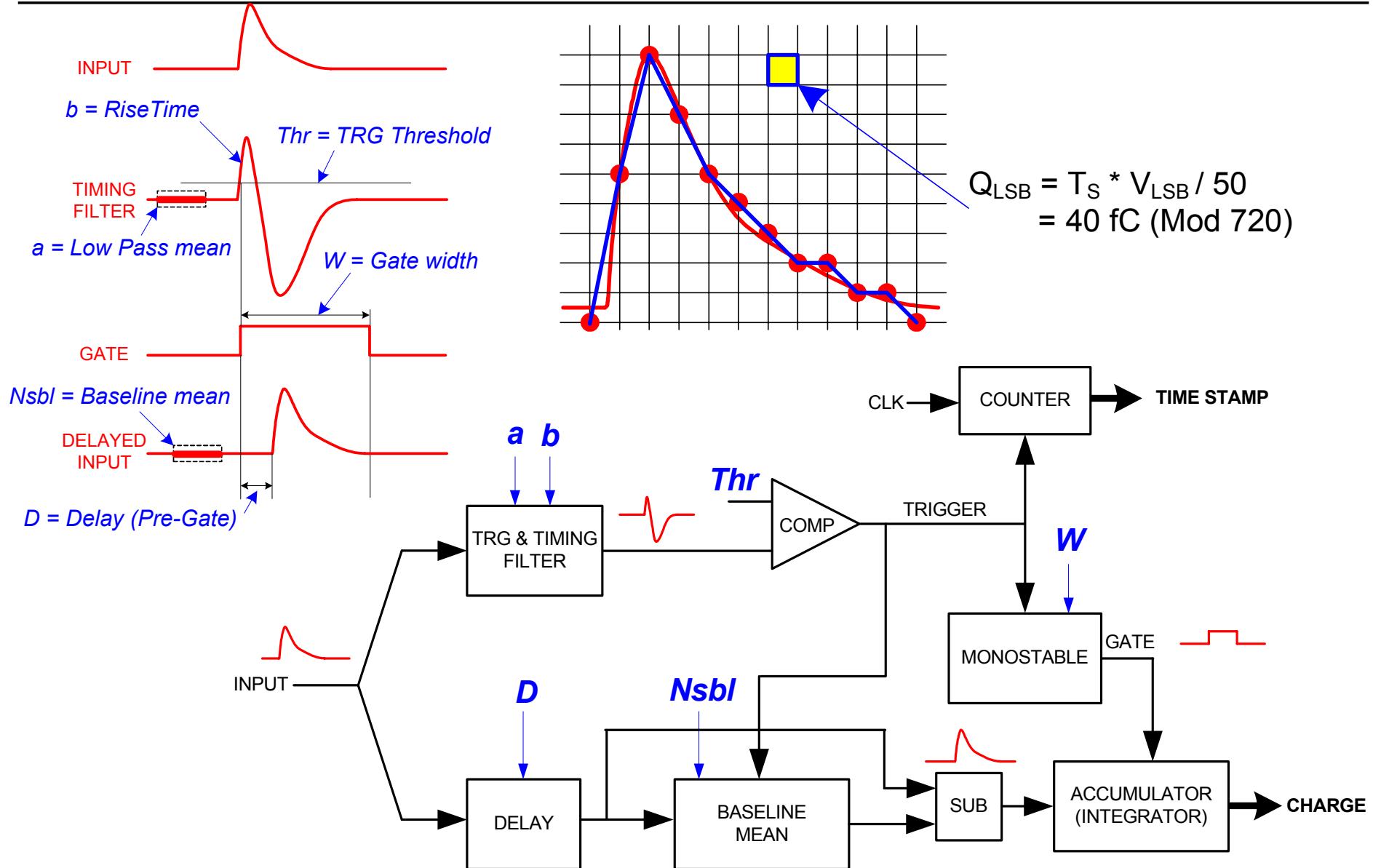


DPP-CI

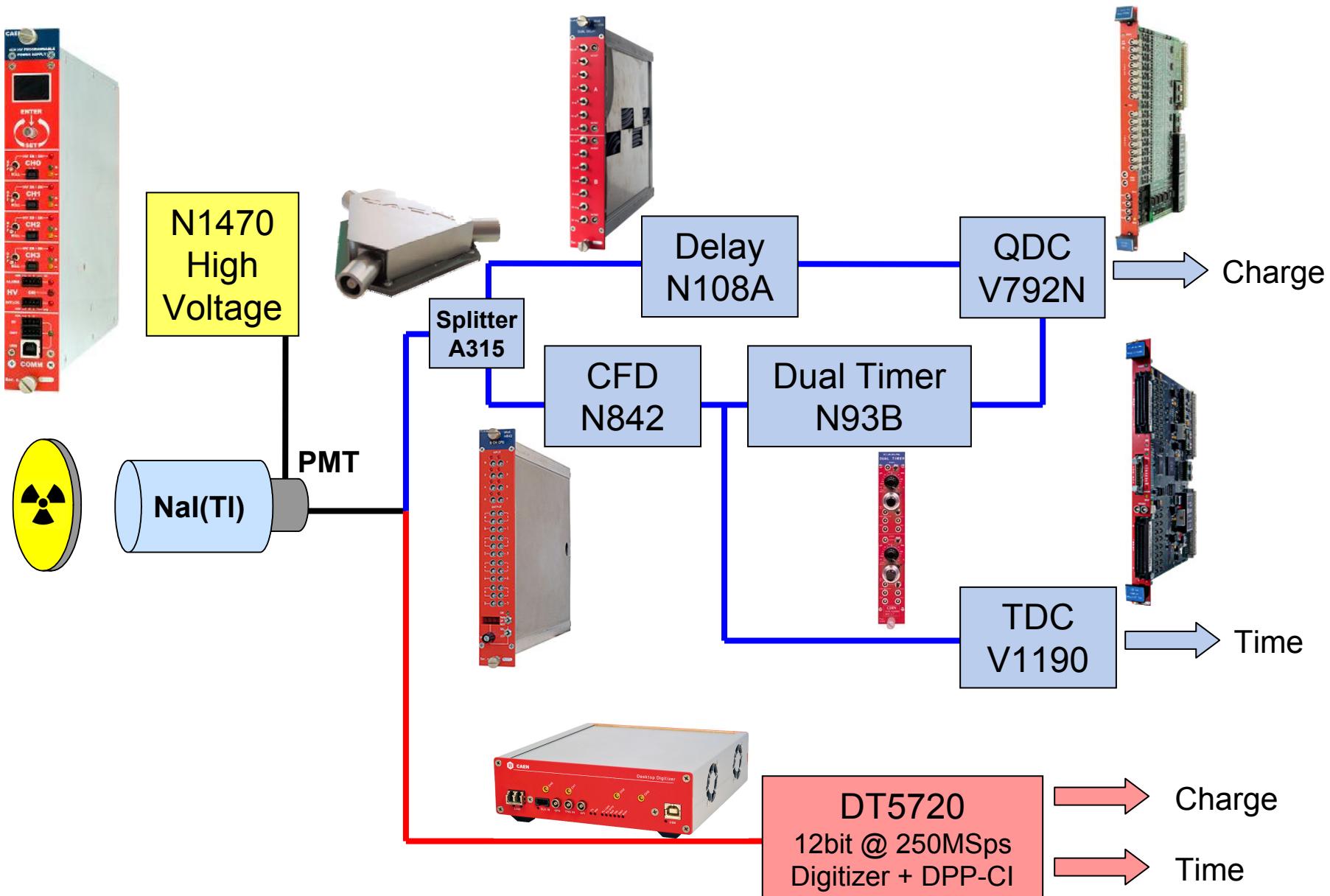
DIGITAL CHARGE INTEGRATION

- Digital implementation of the QDC + discriminator and gate generator
- Implemented in the Mod. x720 - 12 bit, 250MS/s
- Self-gating integration; no delay line to fit the pulse within the gate
- Baseline restoration (pedestal cancellation)
- Extremely high dynamic range
- Dead-timeless acquisition (no conversion time)
- Energy and timing information can be combined
- Typically used for PMT or SiPM/MPPC readout

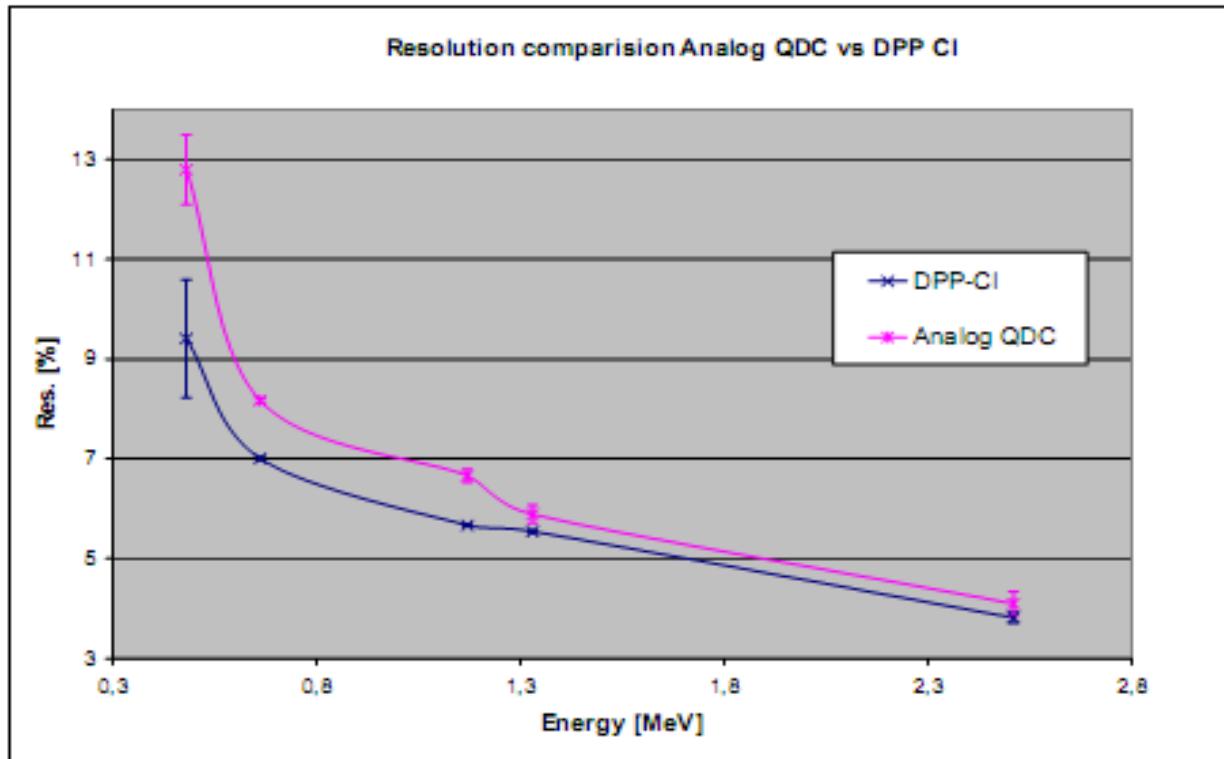
DPP-CI Block Diagram



DPP-CI vs Analog Chain set-up



DPP-CI: Test Results with NaI+PMT

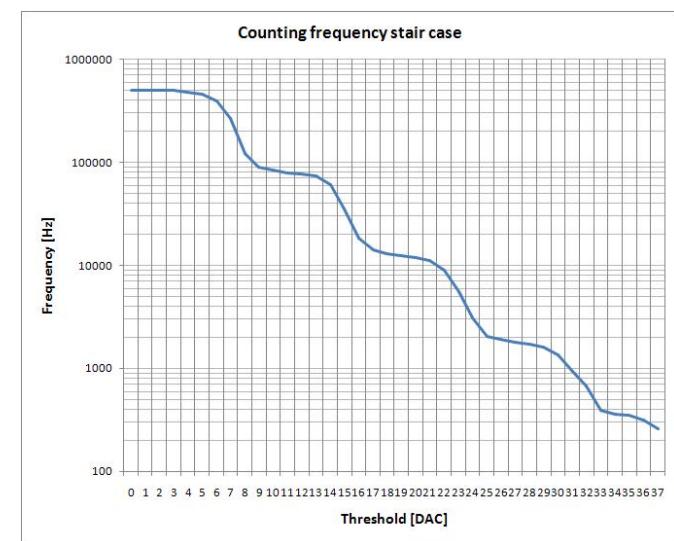
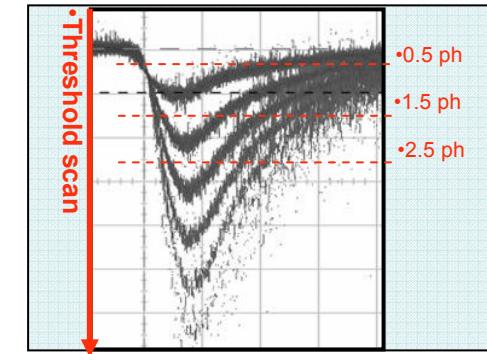
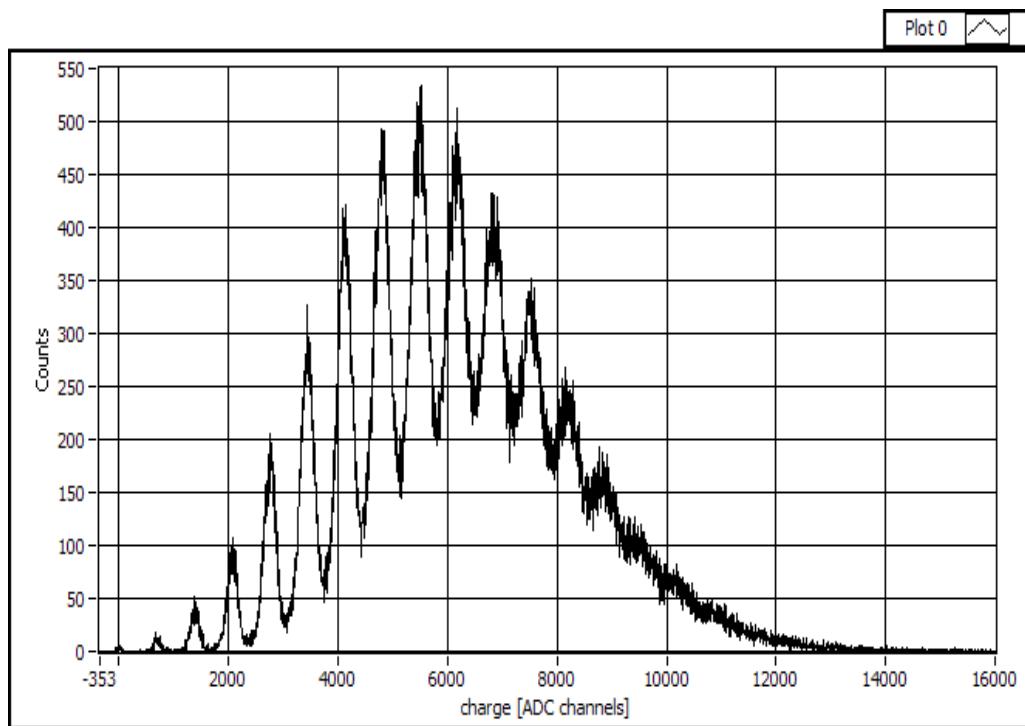


NaI detector and PMT directly connected to the QDC or digitizer

*Resolution = FWHM * 100 / Mean*

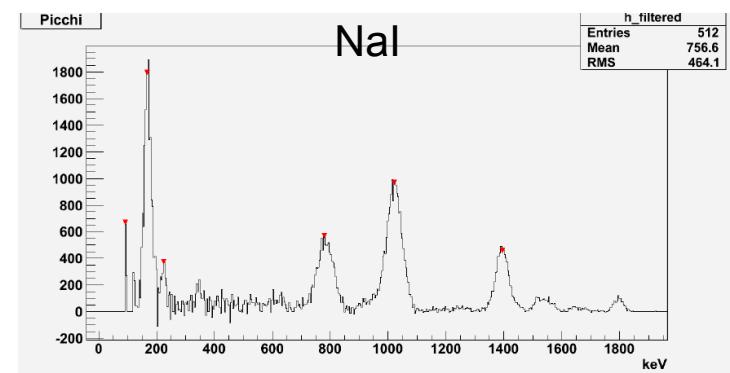
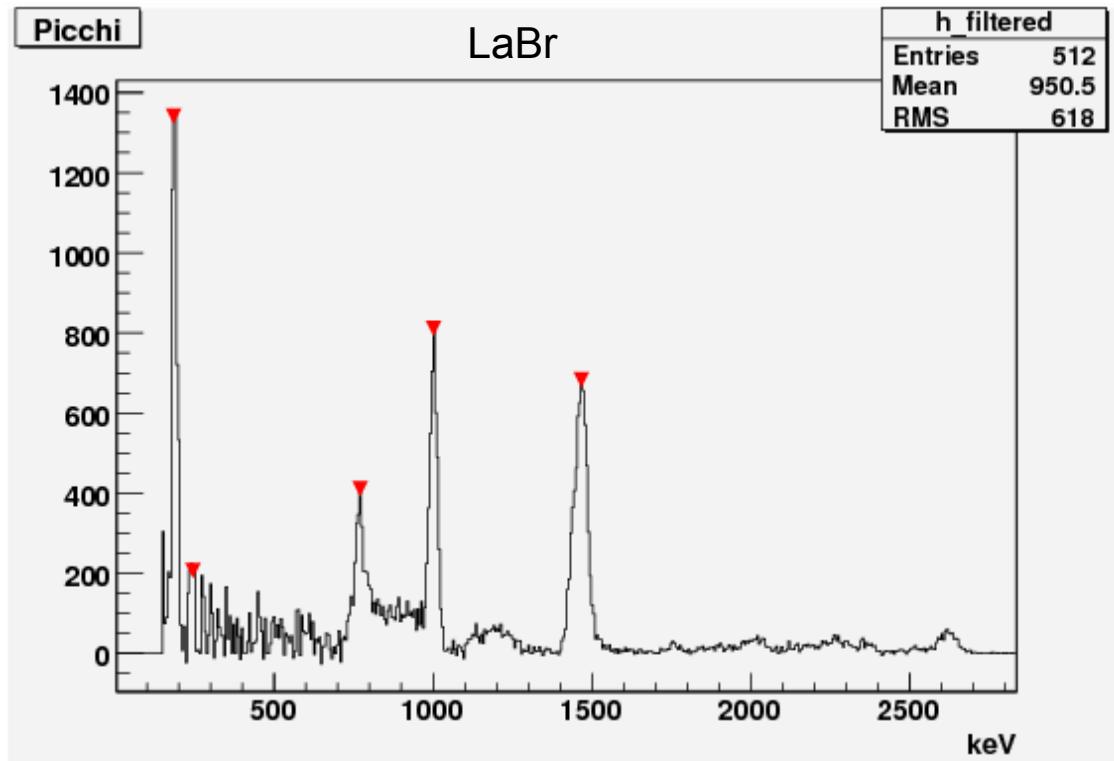
	DPP-CI	Analog QDC
Energy (MeV)	Res (%)	Res (%)
0.481 (¹³⁷ Cs Compton edge)	9.41 ± 1.18	12.80 ± 0.70
0.662 (¹³⁷ Cs Photopeak)	7.01 ± 0.04	8.17 ± 0.04
1.17 (⁶⁰ Co Photopeak)	5.46 ± 0.02	5.89 ± 0.13
1.33 (⁶⁰ Co Photopeak)	5.67 ± 0.03	6.66 ± 0.18
2.51 (⁶⁰ Co Sum peak)	3.82 ± 0.11	4.10 ± 0.24

DPP-CI: Test Results with SiPM kit SP5600



DPP-CI: Test Results with LaBr

- Project: SLIM.CHECK (detection of illicit radioactive material)
- Test performed at JRC Ispra by INFN PD (acknowledges: G. Visti)
- 4 detectors: **LaBr**, **NaI(Tl)**, **NE213**, **^3He** , all read by a V1720 with DPP-CI
- Source ^{238}U (348 Kg)

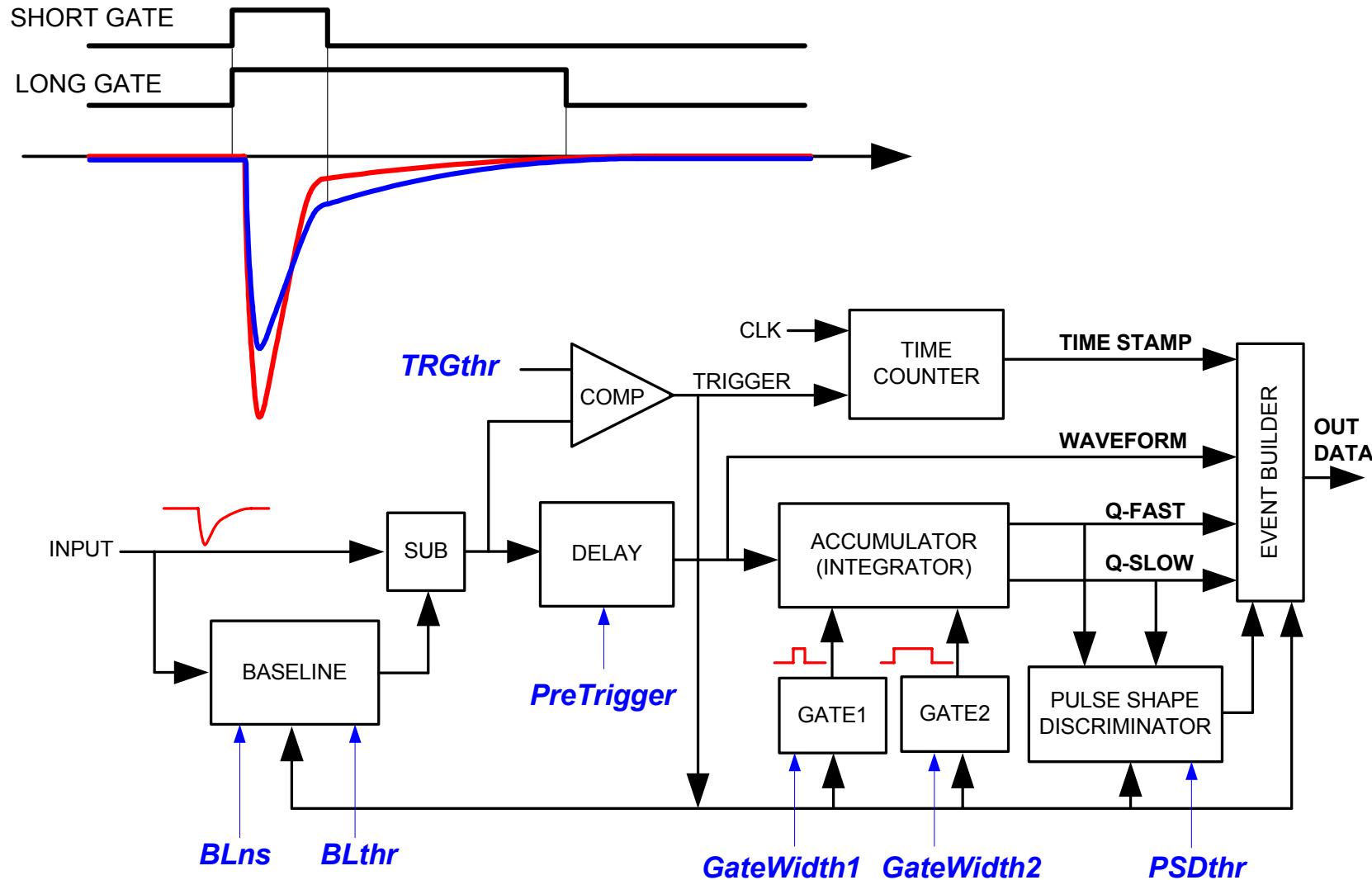


DPP-PSD

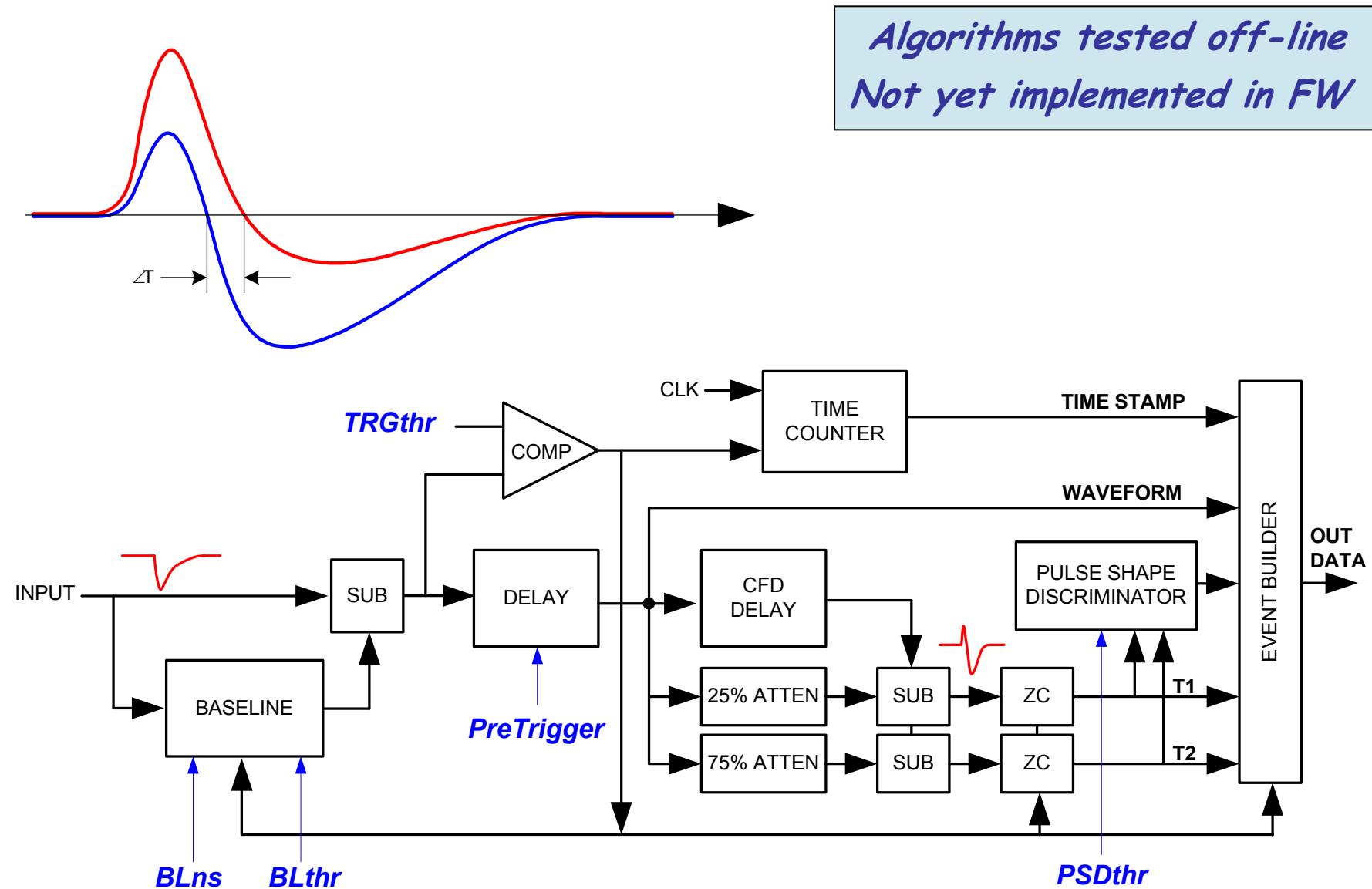
PULSE SHAPE DISCRIMINATION

- Digital implementation of the $\Delta E/E$ analysis (double gate charge integration)
- Implemented in the Mod. x720 - 12 bit, 250MS/s and Mod x751 - 10 bit, 1GS/s or 2GS/s
- $PSD = (Q_{LONG} - Q_{SHORT}) / Q_{LONG}$
- Typically used with organic liquid scintillators (e.g. BC501)
- Dead-timeless acquisition (no conversion time)
- Alternative analysis (not implemented yet) based on the Rise Time Discrimination technique: ΔT in the Zero Crossing of two CFDs at 25% and 75%; applied to integrated output (either from C.S. preamp or digital integrator)

DPP_PSD Block Diagram (I)



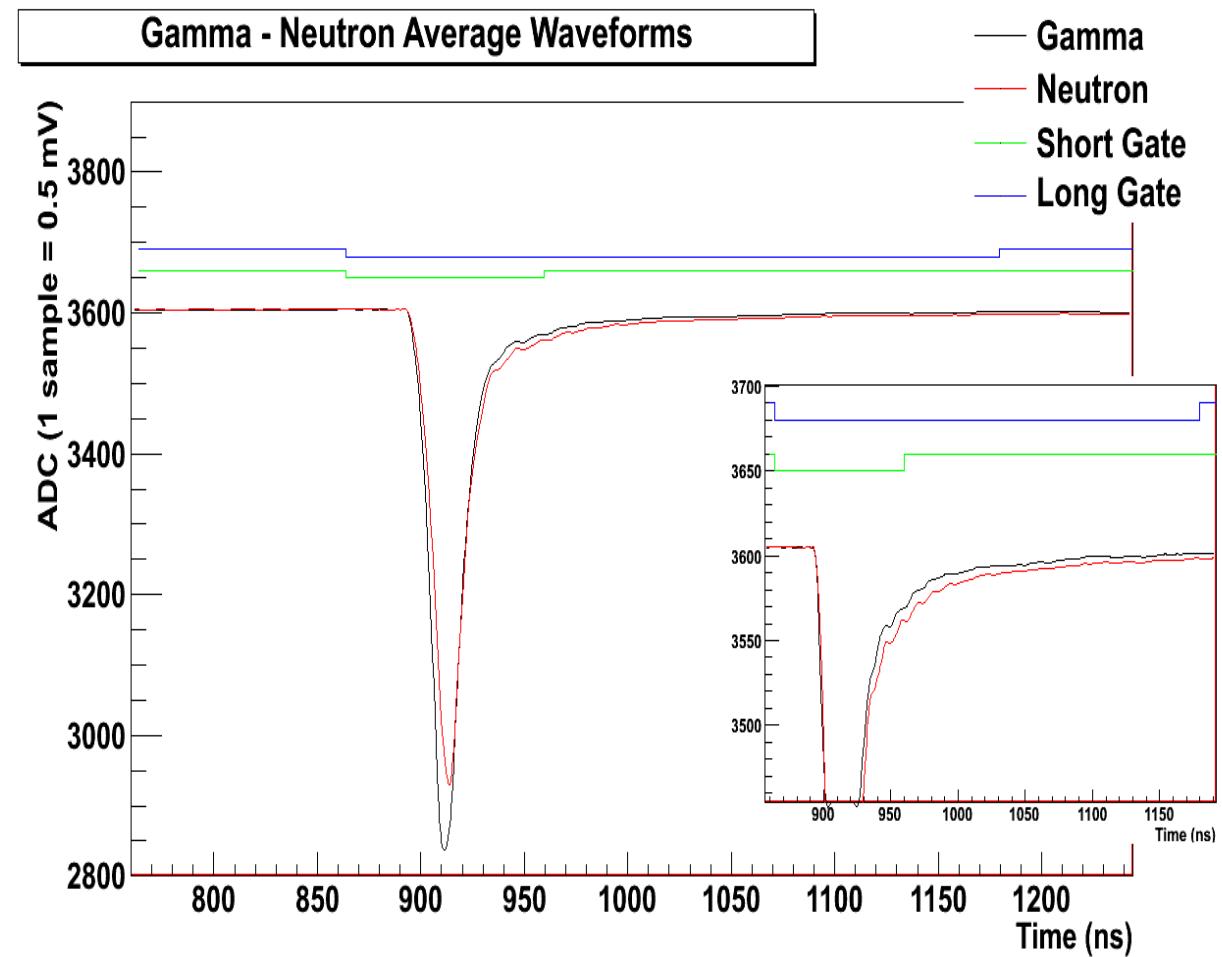
DPP_PSD Block Diagram (II)



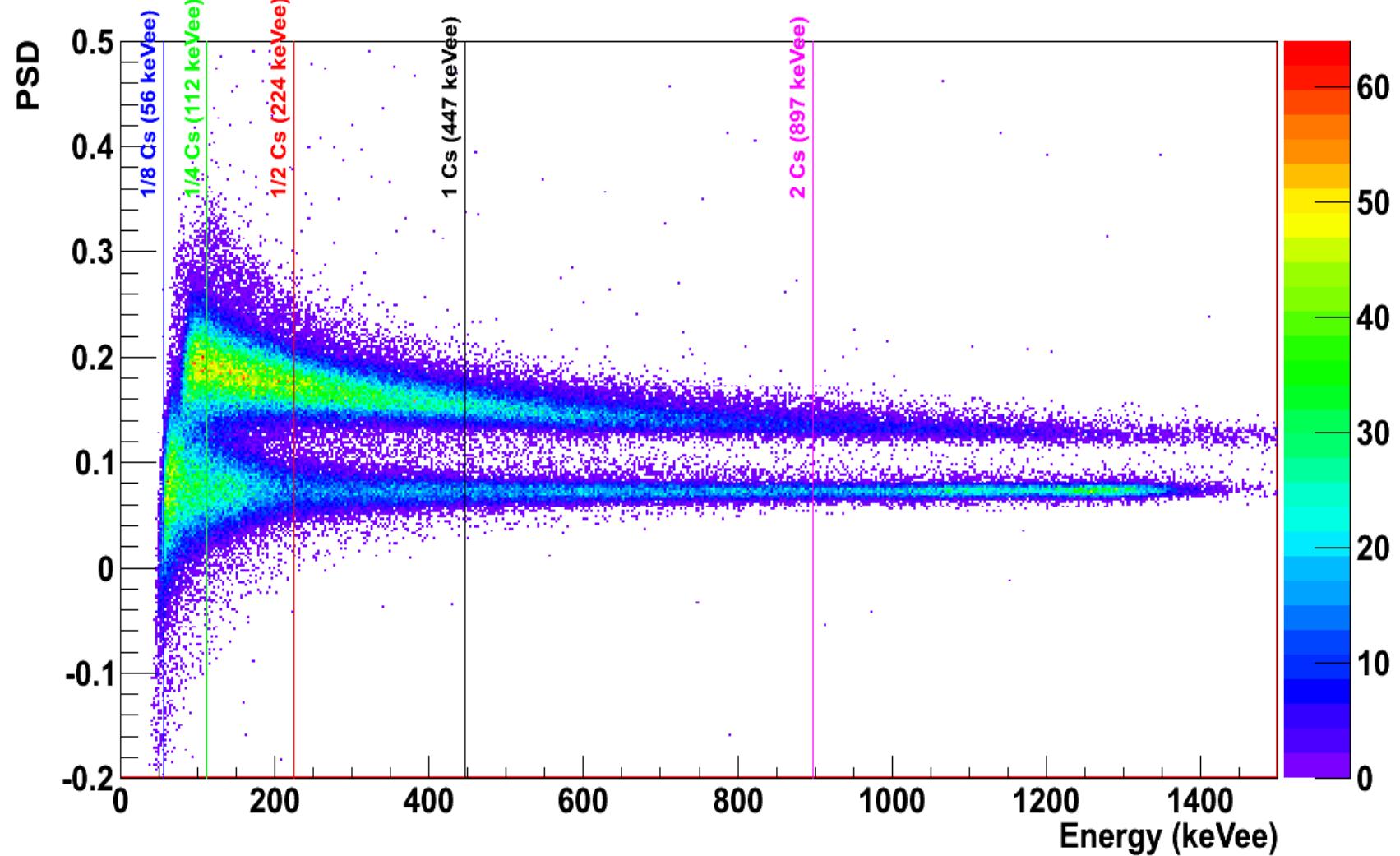
γ -n Discrimination: test results (I)

Detector: BC501A 5x2 inches,

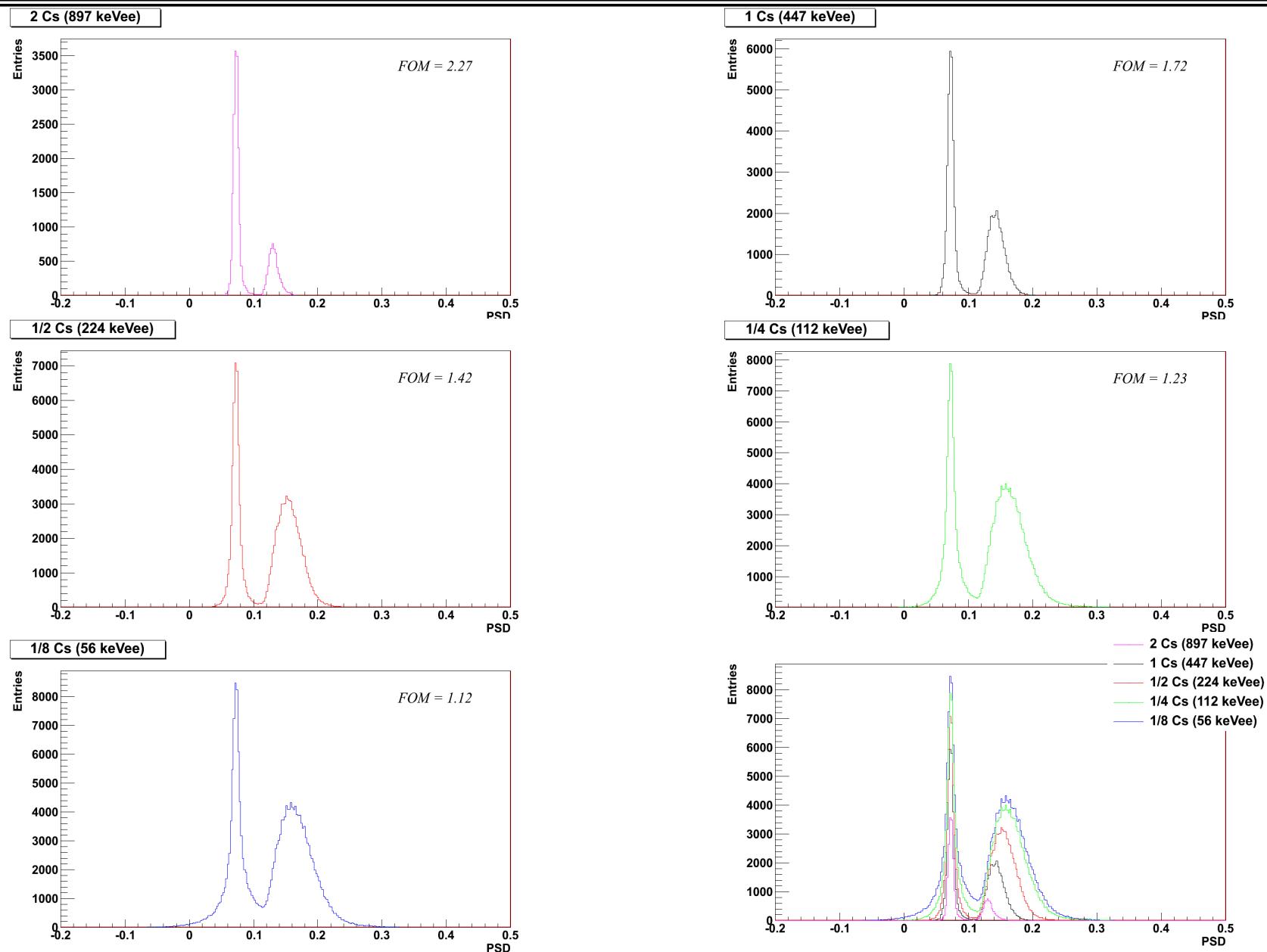
PMT: Hamamatsu R1250



γ -n Discrimination: test results (II)

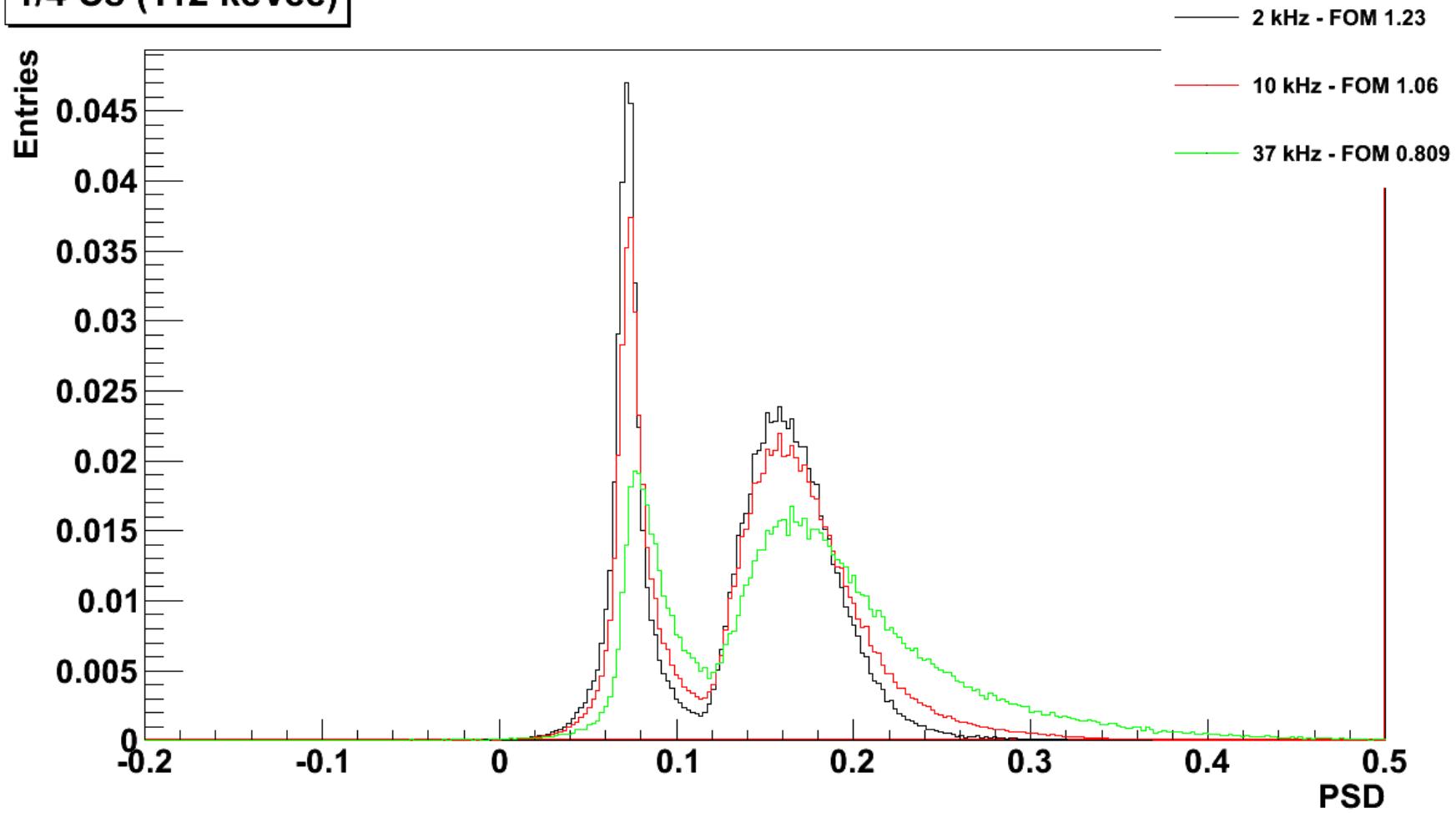


γ -n Discrimination: test results (III)

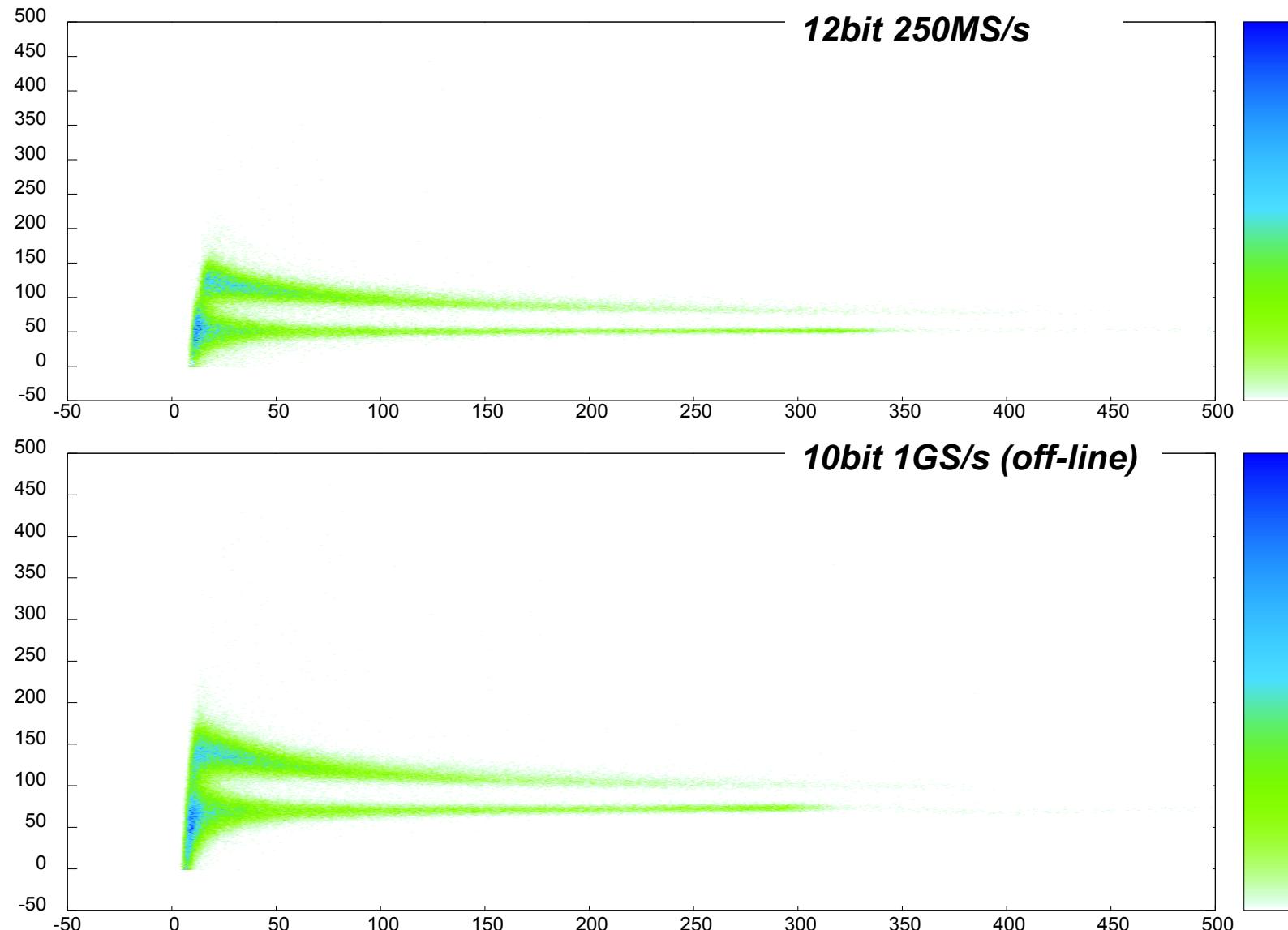


γ -n Discrimination: test results (IV)

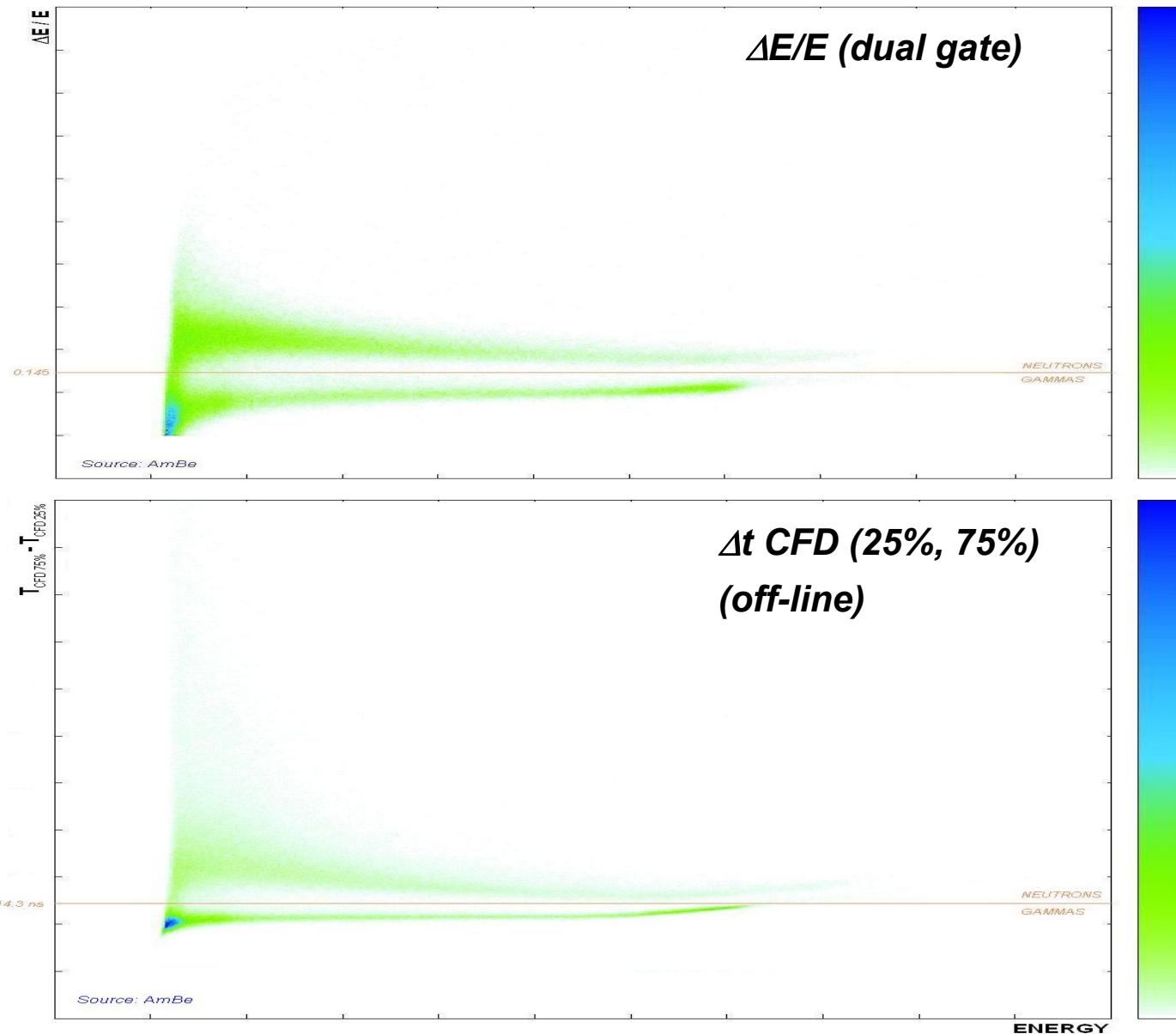
1/4 Cs (112 keVee)



γ -n Discrimination: test results (V)

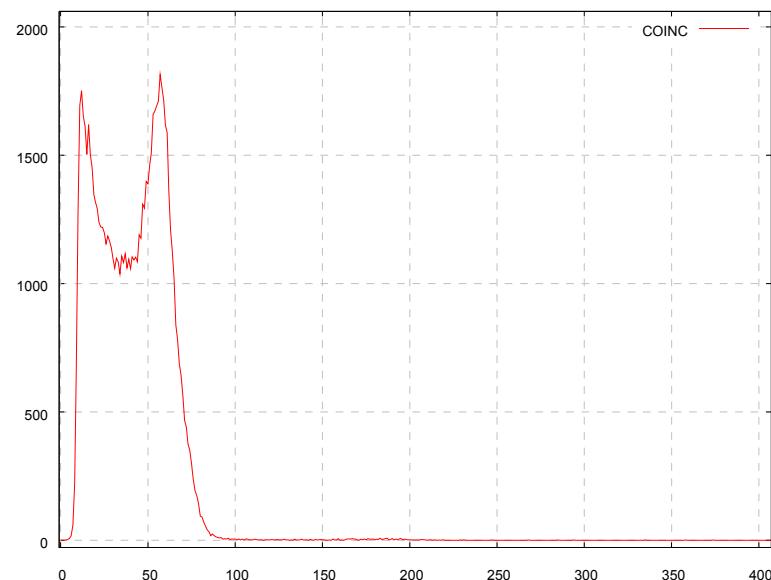
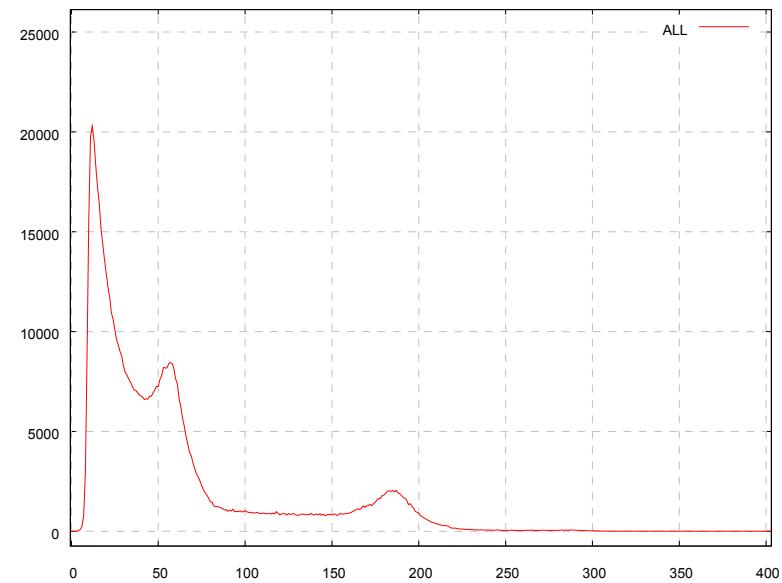
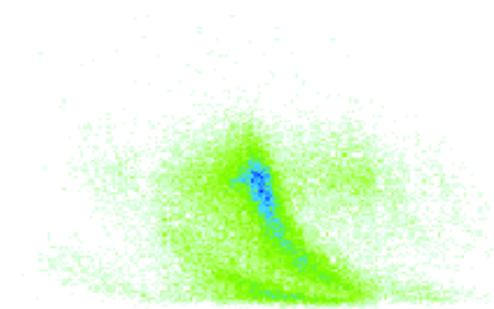


γ -n Discrimination: test results (VI)



Practical example of off-line coincidence

- Detectors: 2 BC501A
- Source: Na22
- 740.000 events acquired in list mode (energy+time stamp) from both detectors
- Off-line analysis: search for time-stamp coincidence within 50 ns
- Energy spectrum of all events (up) and after coincidence (down)
- Energy vs Time of Flight 2-D plot (below)



DPP for timing

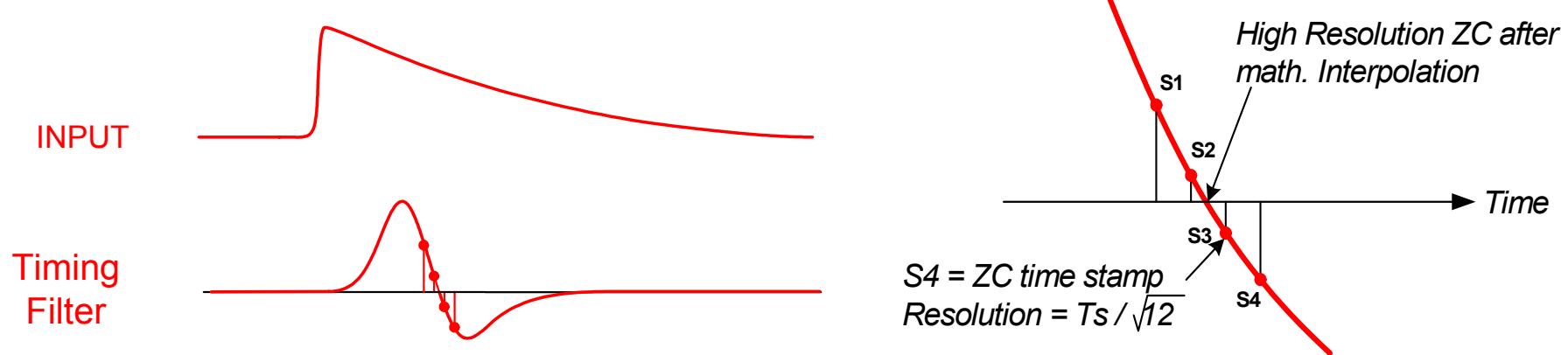
TIMING ANALYSIS WITH DIGITIZERS

Conventional TDCs vs Digitizers

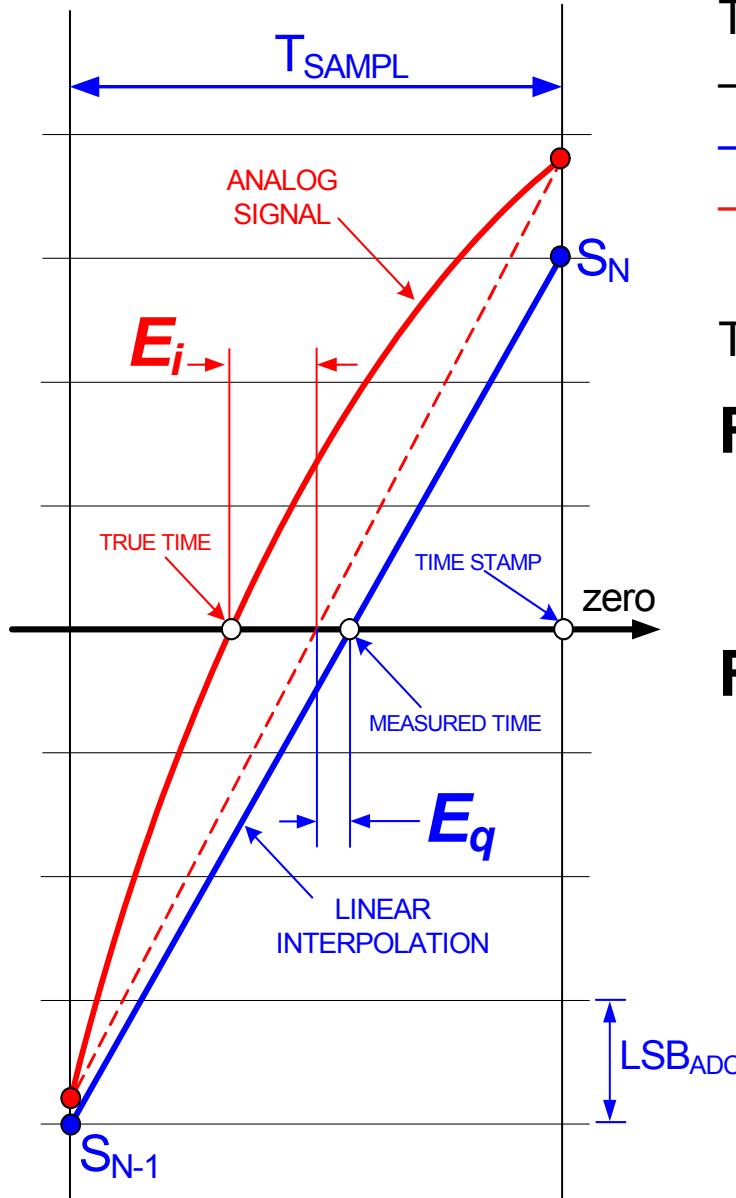
- Conventional TDC boards:
 - **V1190**: 128 channel, 100 ps Multi-Hit TDC
 - **V1290**: 32 channel, 25 ps Multi-Hit TDC
 - **V775**: 32 channel, 35 ps Start-Stop TDC
- TDC in a digitizer can't compete in terms of density and cost, but...
- There are cases where the implementation of a TDC in a digitizer is profitable:
 - *Time measurement (at medium-low resolution) combined with energy or other parameters*
 - *Extremely high timing resolution (better than 10 ps)*
 - *Bursts of very close pulses (e.g. Free Electron Lasers)*
 - *Signals unsuitable for the conventional Constant Fraction Discriminators*

Algorithms for the Time Measurements

- DPP time stamp LSB equals the sampling period (Resolution = $T_s/\sqrt{12}$);
- Interpolation between samples improves timing resolution
- It is not worth doing on-line interpolation (floating point consumes FPGA resources and has no significant data size reduction)
- DPP can make on-line digital CFD or LED and save just 2 (or more) points into the readout data; interpolation is then calculated off-line
- **The resolution is greatly depending of the rise-time and amplitude of the pulses ($\delta V / \delta T$)**



ZC timing errors



Timing resolution affected by three types of noise:

- *Electronic noise in the analog signal (here ignored)*
- *Quantization error E_q*
- *Interpolation error E_i*

There are 2 different cases:

Rise Time > 5*T_s

linear interpolation is good: $E_i \ll E_q$

The resolution is proportional to $\delta V / \delta T$ and to the number of bits of the ADC.

Rise Time < 5*T_s

approximation to a straight line is too rough:

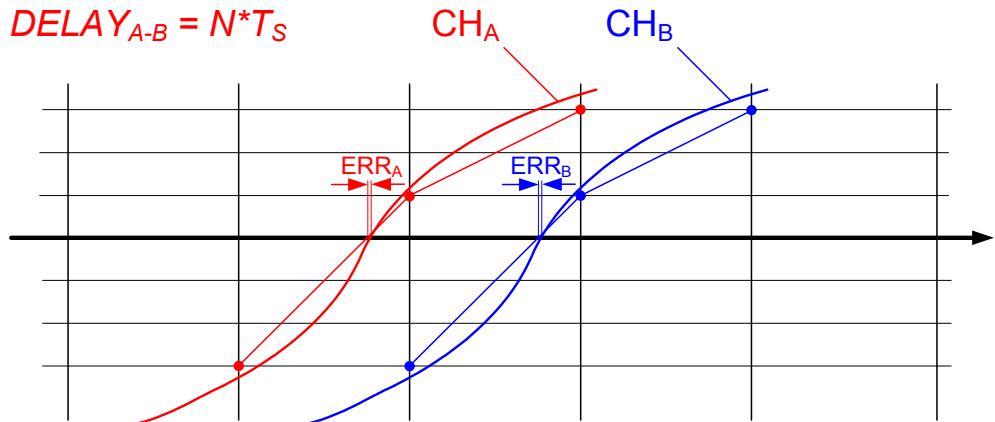
E_i is the dominant error (E_q is negligible). Such a geometric error varies with the position of the signal respect to the sampling clock giving non gaussian spectra and other non-physical effects. The resolution becomes inversely proportional to the rise time.

**Optimum Rise Time = 5*T_s
for any type of digitizer!**

Sampling Clock phase effect (RT<5Ts) (I)

When rise time < 5*Ts, the interpolation error has a big variation with the phase between the rising edge and the sampling clock.

$$\text{DELAY}_{A-B} = N * T_s$$



$$\text{DELAY}_{AB} = N * T_s:$$

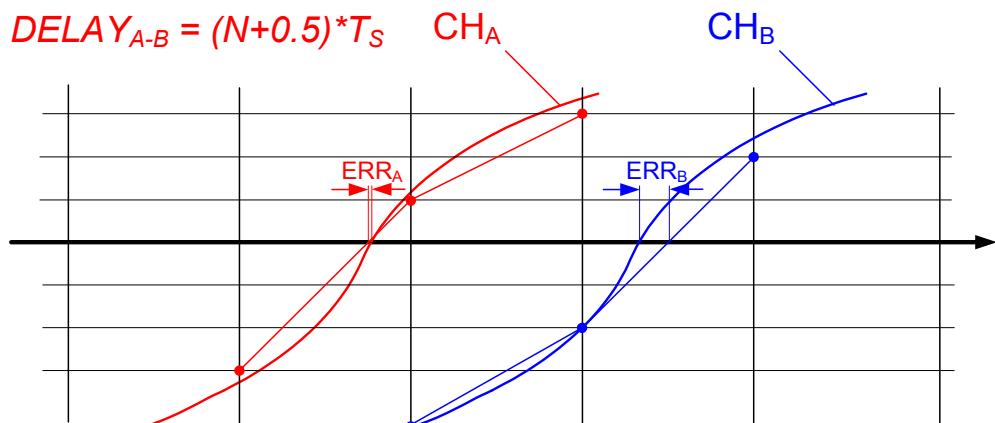
same clock phase for A and B \Rightarrow

same interpolation error \Rightarrow

$$\text{ERR}_A \approx \text{ERR}_B \Rightarrow$$

Error cancellation in calculating TIME_{AB}

$$\text{DELAY}_{A-B} = (N+0.5) * T_s$$



$$\text{DELAY}_{AB} = (N+0.5) * T_s:$$

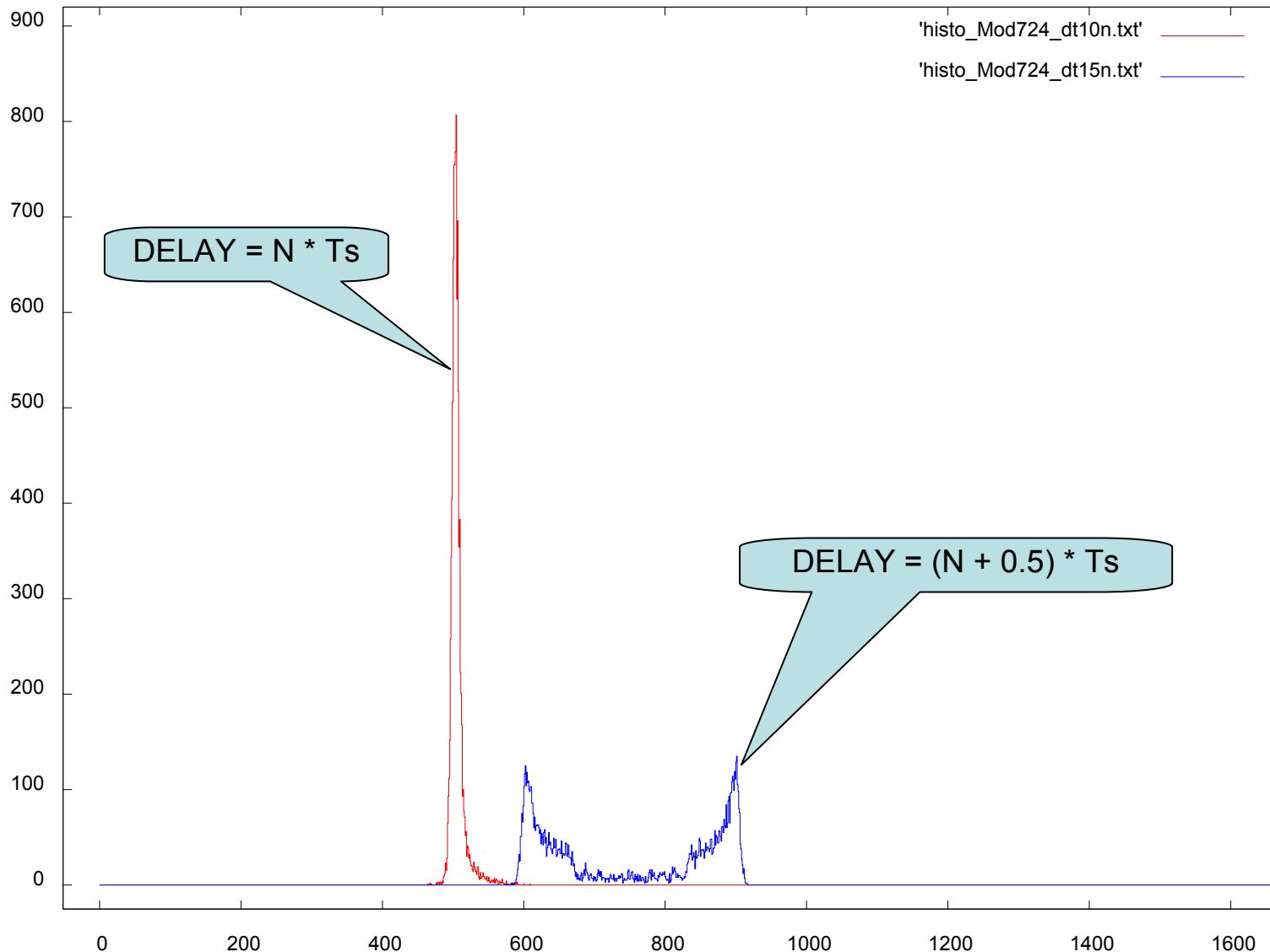
rotated clock phase for A and B \Rightarrow

different interpolation error \Rightarrow

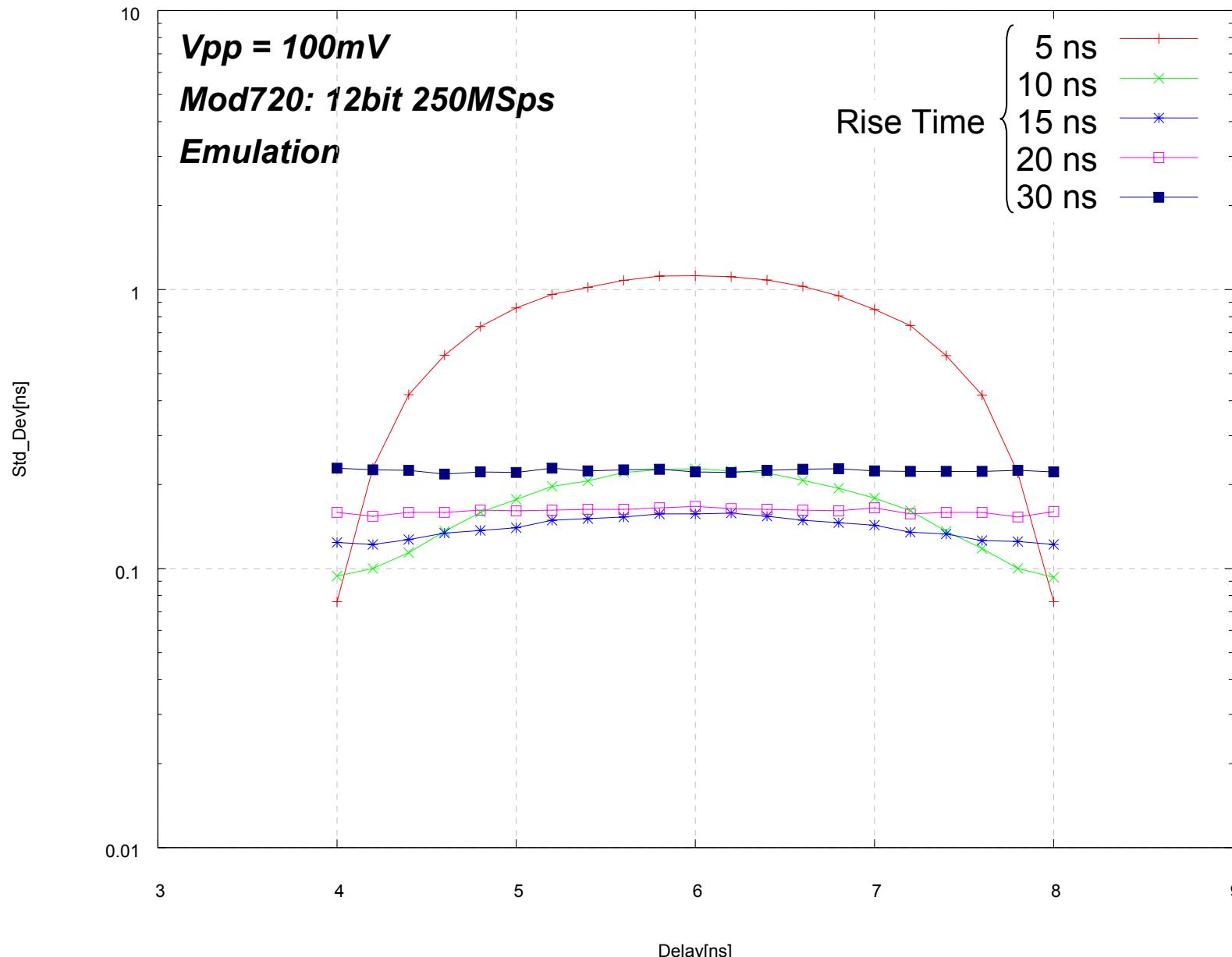
$$\text{ERR}_A \neq \text{ERR}_B \Rightarrow$$

No error cancellation. ERR_A and ERR_B are symmetric: twin peak distribution

$$\text{TIME}_{AB} = (ZC_A + \text{ERR}_A) - (ZC_B + \text{ERR}_B) = ZC_A - ZC_B + (\text{ERR}_A - \text{ERR}_B)$$

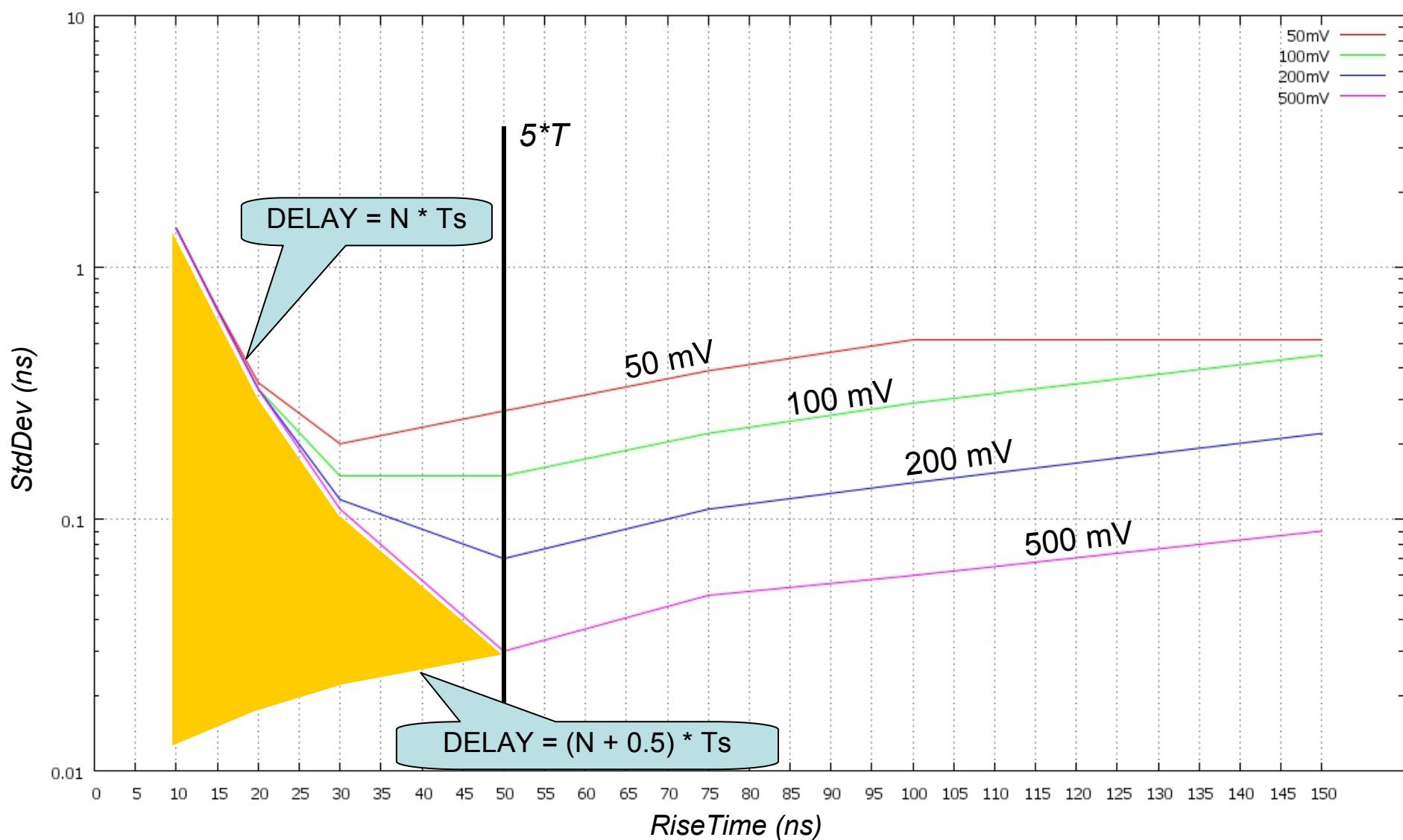


Sampling Clock phase effect (RT<5Ts) (III)



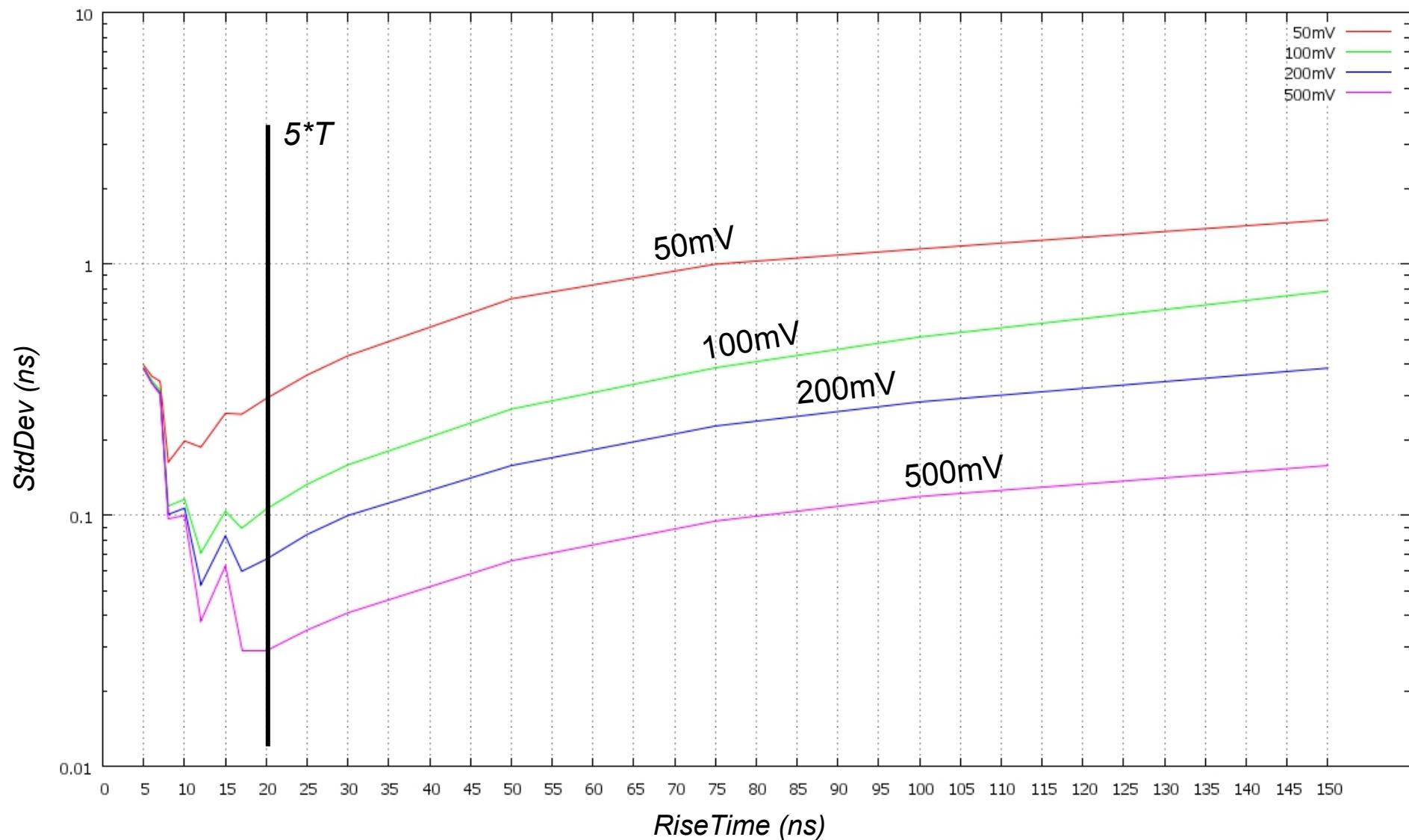
Preliminary results: Mod724

(14 bit, 100 MS/s)



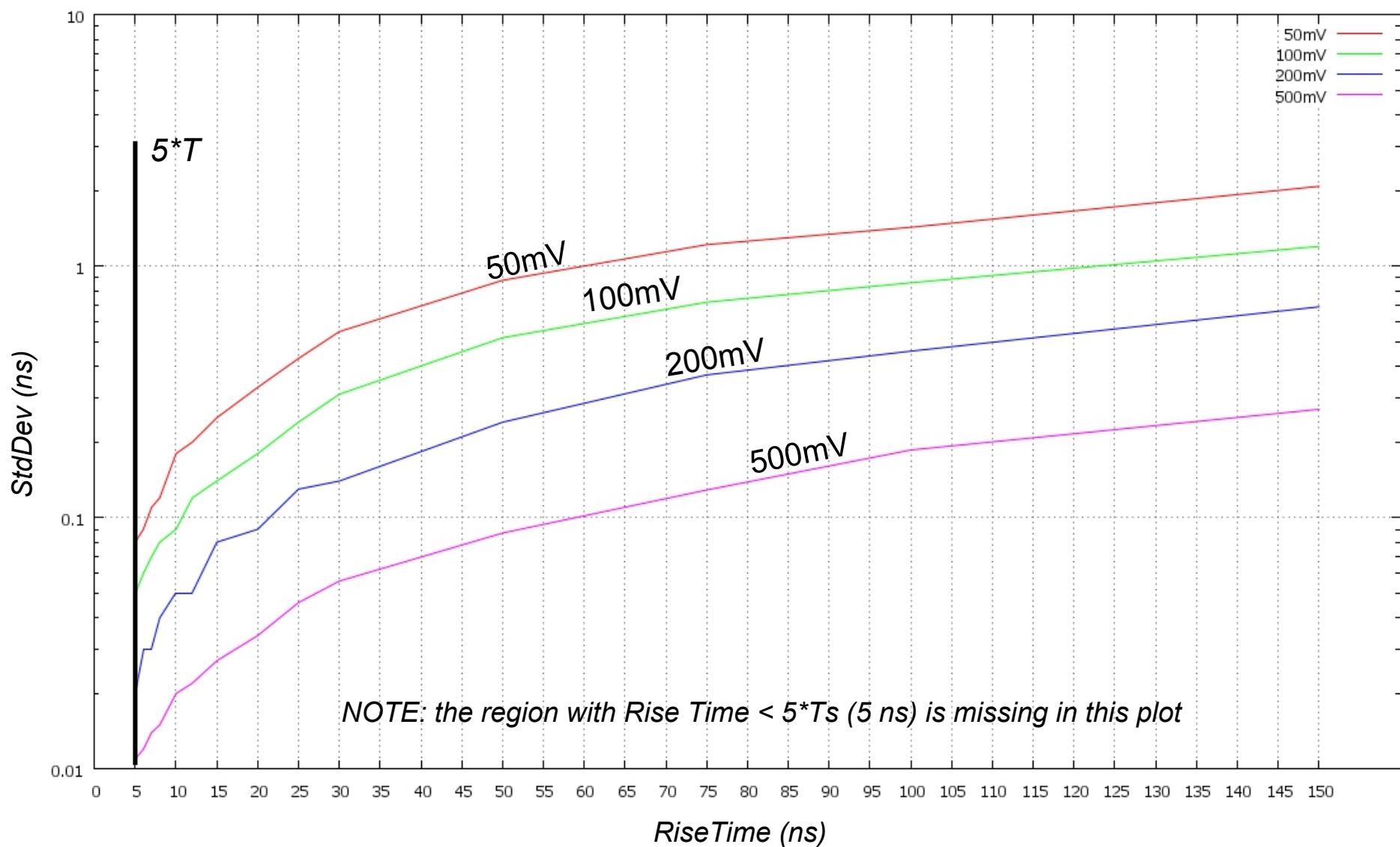
Preliminary results: Mod720

(12 bit, 250 MS/s)

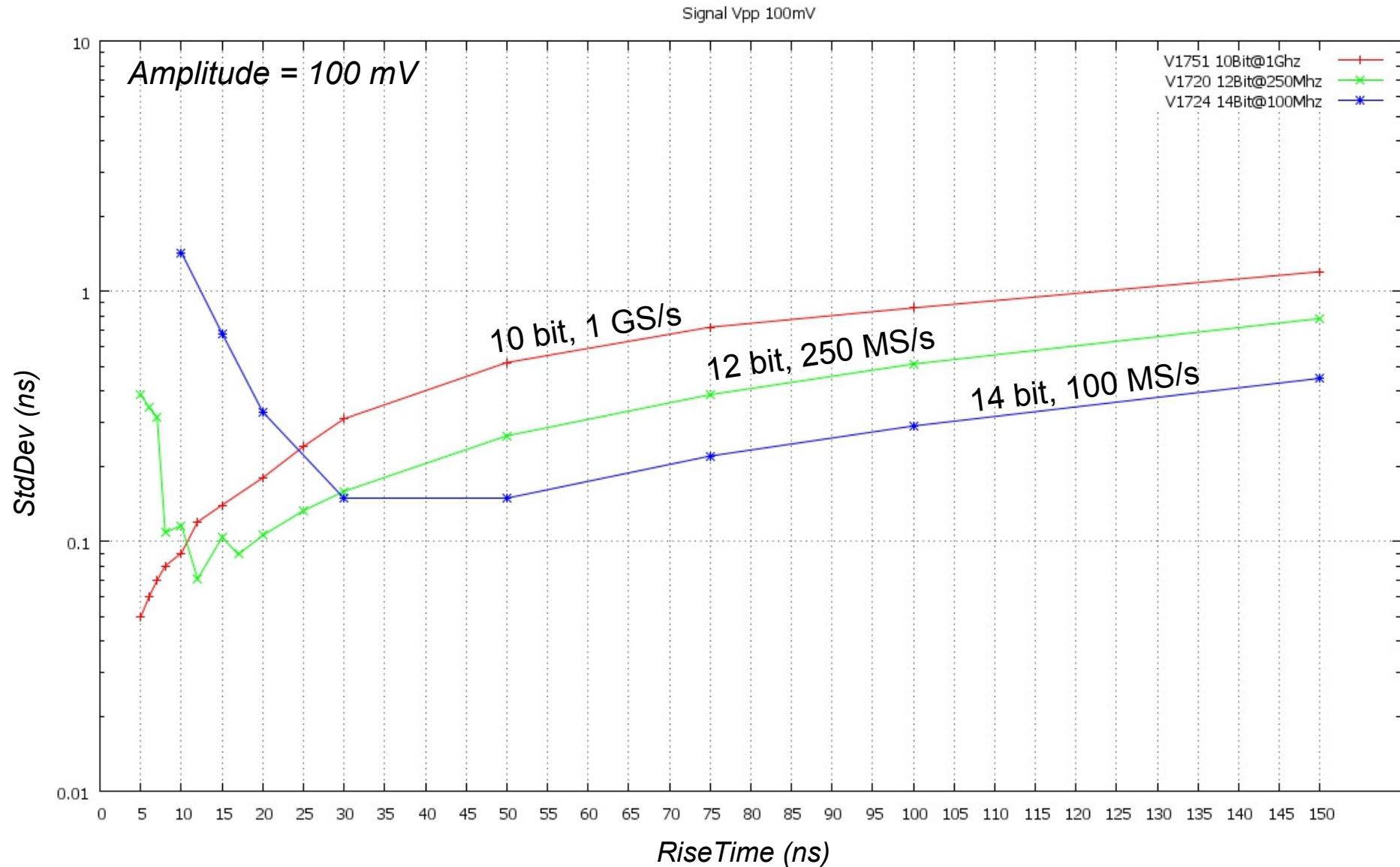


Preliminary results: Mod751

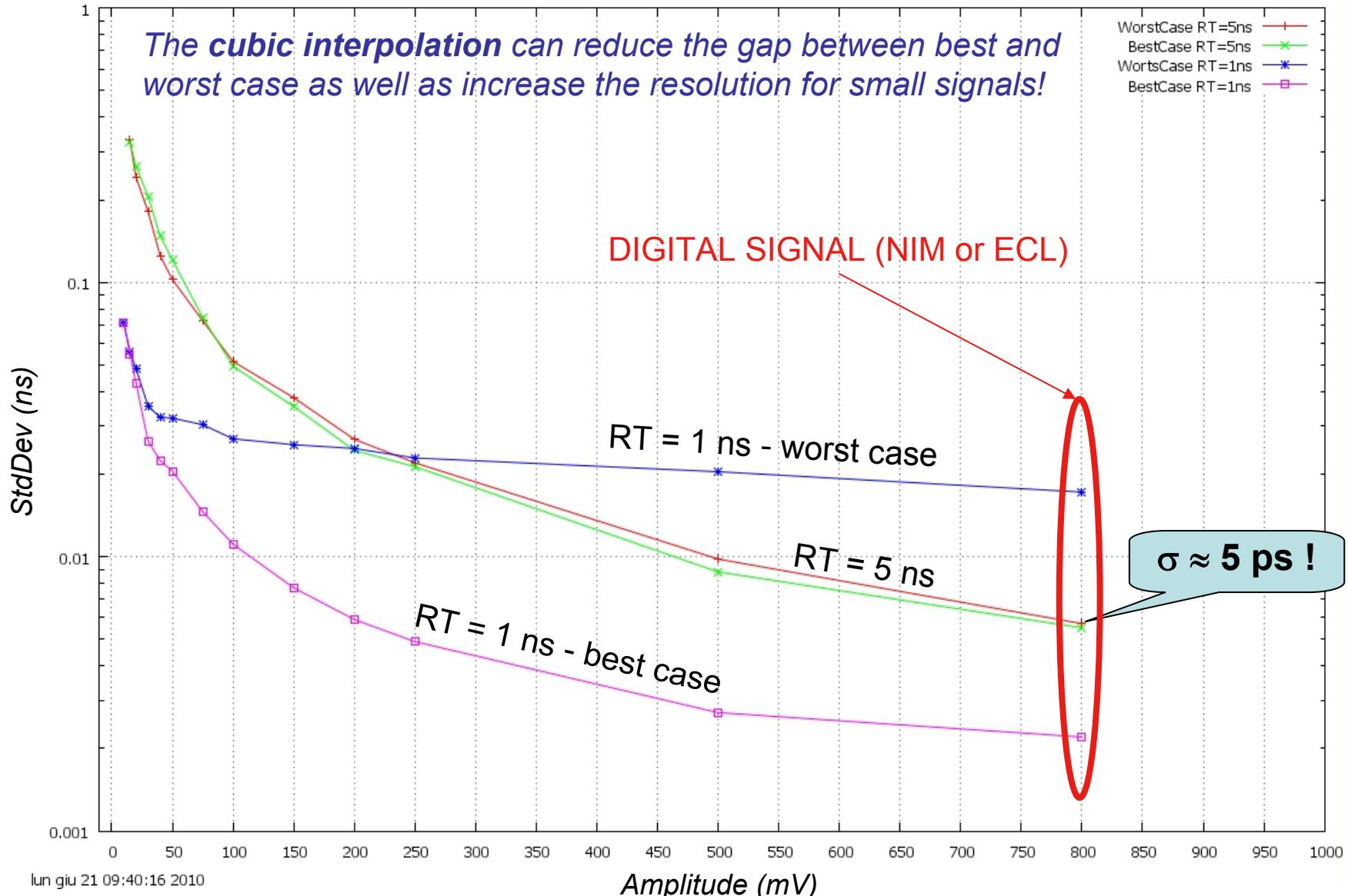
(10 bit, 1 GS/s)



Mod724 vs Mod720 vs Mod751

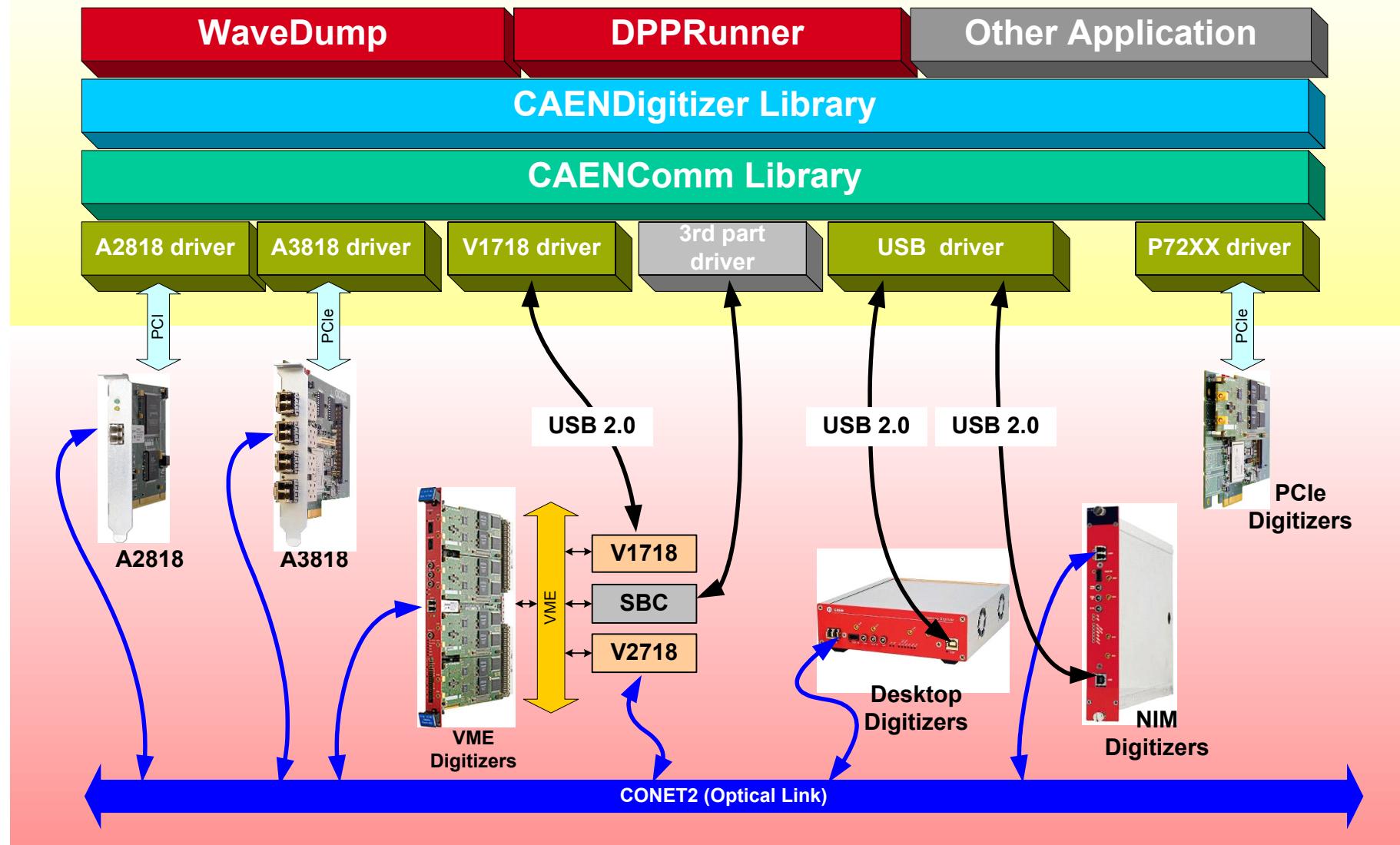


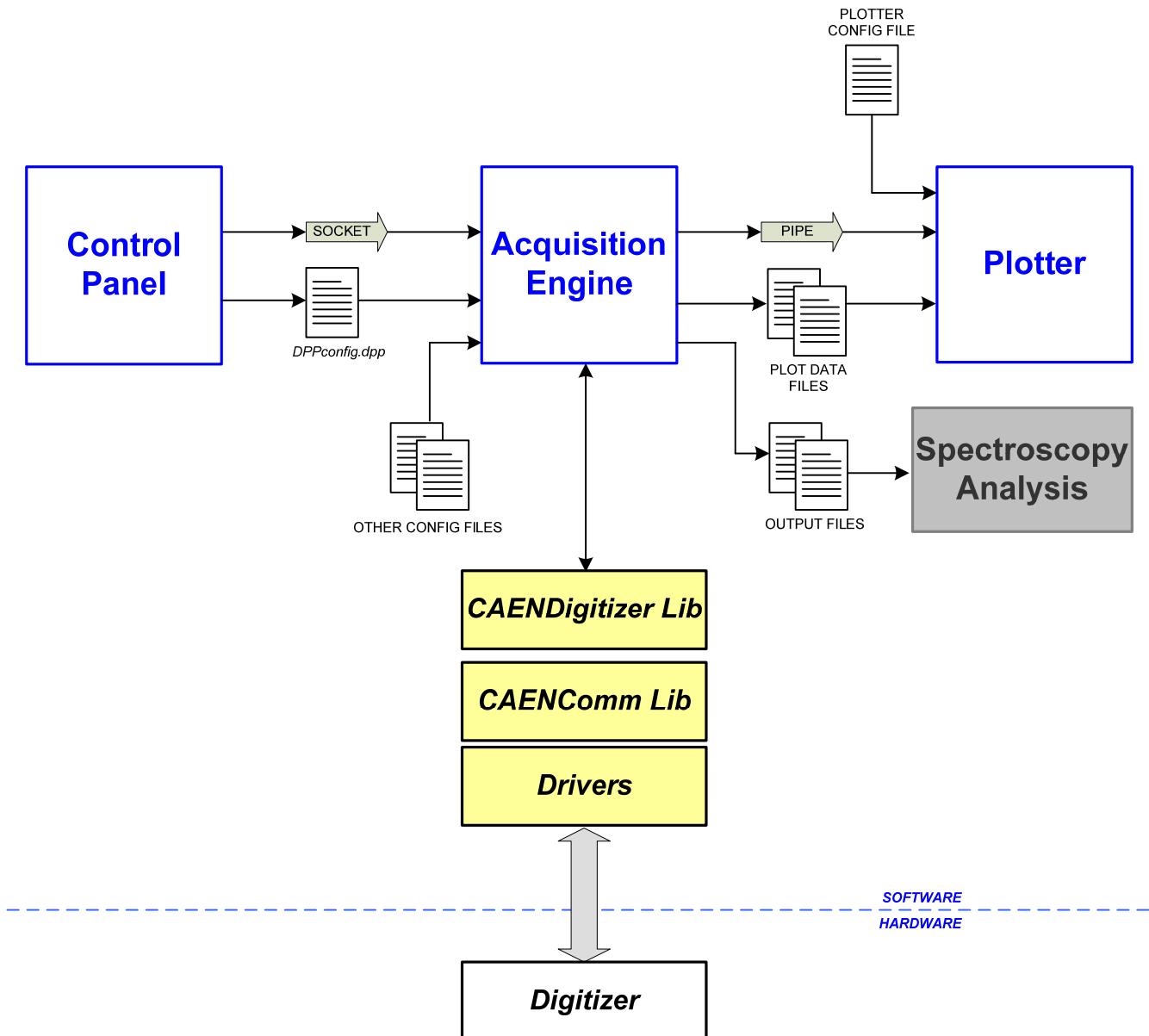
V1751 (10Bit @ 2Ghz) RiseTime = 1ns / 5ns



- We are currently making tests with the x742 series (5 GS/s, 12 bit)
- The use of the x742 is the only way to get a high density, low cost digitizer giving high energy and timing resolution in one single board
- There is no DPP on-line for the moment; however, the need of DPP for this board is less important because of the dead-time
- Timing calibration (applied off-line) seems effective
- Linear interpolation between two points gave a timing resolution of about 30 ps
- We are investigating other types of signal interpolations such as cubic (4 points) or best fit curves with a signal template

Software for Digitizers





Thank you!