



User Manual UM5698

742 Registers

Waveform Recording Firmware Registers

Rev. 0 - January 26th, 2017

Purpose of this Manual

The User Manual contains the full description of the Waveform Recording firmware registers for 742 digitizer family. The description is compliant with the firmware revision **4.13_1.01**. For future release compatibility check in the firmware history files.

Change Document Record

Date	Revision	Changes
January 26 th , 2017	00	Initial Release

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Reset and Clear

The module's registers can be set back to their default values on software reset command by writing in the Software Reset register or by system reset from backplane, in case of VME boards. In particular, the registers or buffers listed below

- Event Readout Buffer
- Buffer Occupancy
- Event Stored
- Event Size

are also be set back to their default values (registers) or emptied (buffers) by a clear issued:

- automatically by the firmware at the start of each run;
- on software command by writing in the Software Clear register
- by hardware (VME boards only), through the LVDS interface properly configured (see the section "Front Panel LVDS I/Os" of the digitizer User Manual).

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

- R **Read only.** The register can be accessed in read only mode.
W **Write only.** The register can be accessed in write only mode.
R/W **Read and write.** The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

- G **Group register.** In case of 740 and 742 digitizer families, some registers manage **groups** of channels. Group registers have M instances, where M is the total number of groups. Write access can be performed in single group mode (one group at a time) or broadcast (simultaneous write access to all groups). Read command must be in single group mode. Single group access can be performed at address 0x1nXY, where n identifies the nth group, while broadcast write can be performed at the address 0x80XY. For example:
- access to address 0x1320 to read/write register 0x1n20 for group 3 of the board. In case of 740 and 742 board, group 3 corresponds to channels from 24 to 31 (8 channels per group). The same value is applied to all channels in the same group.
 - to write the same value for all groups in the board, access to 0x8020 (broadcast write). To read the corresponding value, access to the individual address 0x1n20.
- C **Common register.** Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Event Readout Buffer	0x0000 - 0x0FFC	R	C
Post Trigger	0x1n14, 0x8014	R/W	G
Dummy32	0x1n24, 0x8024	R/W	G
Group n Channel Threshold	0x1n80, 0x8080	R/W	G
Group n Status	0x1n88	R	G
AMC Firmware Revision	0x1n8C	R	G
Group n Channel DC Offset	0x1n98, 0x8098	R/W	G
DRS4 Chip Temperature	0x1nA0	R	G
Group n Channel Selection	0x1nA4	R/W	G
Group n Channel Trigger Mask	0x1nA8, 0x80A8	R/W	G
Group n TR Trigger Threshold	0x1nD4, 0x80D4	R/W	G
Group n TR DC Offset	0x1nDC, 0x80DC	R/W	G
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Custom Size	0x8020	R/W	C
Test Mode Initial Value	0x807C	R/W	C
DRS4 Sampling Frequency	0x80D8	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Group Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Event Stored	0x812C	R	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status/ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C
Max Number of Events per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C

Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

Event Readout Buffer

This is the addressment space for the event readout. The event is a series of 32-bit words according to the event structure defined in the digitizer User Manual.

Address 0x0000 - 0x0FFC
Mode R
Attribute C

Bit	Description
[31:0]	32-bit word of the event.

Post Trigger

The post trigger corresponds to the delay between the trigger arrival and the DRS4 chip holding phase. The value written in this register must be multiplied by 8.5 ns.

NOTE: An additional latency time should be added to the post-trigger size, which depends on the trigger source. In case of TRG-IN the latency is about 115 ns (for ROC FPGA firmware less than 4.07 the latency was 255 ns); in case of TRn the latency is about 42 ns.

NOTE: also address 0x8114 can be used to broadcast write.

Address	0x1n14, 0x8014
Mode	R/W
Attribute	G

Bit	Description
[9:0]	Post Trigger value. Note: For FW rev. < 0.3, the Post Trigger value is over 7 bits.
[31:10]	Reserved

Dummy32

Writing and reading at this register can be used for debug purposes to test the local bus.

NOTE: Since this register is common to two groups, a write access to either 0x1024 or 0x1124 leads to the same setting for group 0 and group 1, and a write access to either 0x1224 or 0x1324 leads to the same setting for group 2 and group 3.

Address	0x1n24, 0x8024
Mode	R/W
Attribute	G

Bit	Description
[31:0]	Dummy32 value (default value is 0).

Group n Channel Threshold

This register manages the Trigger Threshold of all channels of the board. In particular the index n (from 0 to 3) controls the group number, and bits[15:12] control the channel index (from 0 to 7) of group n . Bits[15:12] can be used in write access only. In read access, the channel index must be set through register 0x1nA4.

For example, to set the Threshold value 0x100 for channel 15 (channel 7 of group 1), write 0x7100 at 0x1180. To read the Threshold value of channel 15, write 0x7 at 0x11A4, then read at 0x1180.

NOTE: this register is implemented from AMC FPGA firmware revision 0.4 on.

Address	0x1n80, 0x8080
Mode	R/W
Attribute	G

Bit	Description
[11:0]	Threshold value in LSB counts.
[15:12]	Channel index. From 0x0 to 0x7 it addresses a single channel of Group n , while 0xF addresses all channels of Group n .
[31:16]	Reserved

Group n Status

This register contains the status information common to all the channels of group n.

Address 0x1n88
Mode R
Attribute G

Bit	Description
[0]	Memory Full.
[1]	Memory Empty.
[2]	If 1, the SPI bus is busy.
[5:3]	Reserved
[6]	If 1, the DRS4 PLL of the even group is locked.
[7]	If 1, the DRS4 PLL of the odd group is locked.
[8]	If 1, the DRS4 chip is busy.
[9]	Mezzanine PCB revision. Options are: 0 = revision 0; 1 = revision equal or higher than 1.
[31:10]	Reserved

AMC Firmware Revision

This register contains the channel FPGA (AMC) firmware revision information.

The complete format is:

Firmware Revision = X.Y (16 lower bits)

Firmware Revision Date = Y/M/DD (16 higher bits)

EXAMPLE 1: revision 1.03, November 12th, 2007 is 0x7B120103.

EXAMPLE 2: revision 2.09, March 7th, 2016 is 0x03070209.

NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address 0x1n8C

Mode R

Attribute G

Bit	Description
[7:0]	AMC Firmware Minor Revision Number (Y).
[15:8]	AMC Firmware Major Revision Number (X).
[31:16]	AMC Firmware Revision Date (Y/M/DD).

Group n Channel DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to $2^{N_{Bit}} - 1$, where N_{Bit} is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the N_{Bit} value and the board type.

Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.

This register manages the DC Offset of all channels of the board. In particular the index n (from 0 to 3) controls the group number, and bits[19:16] control the channel index (from 0 to 7) of group n . Bits[19:16] can be used in write access only. In read access, the channel index must be set through register 0x1nA4.

For example, to set the DC Offset value 0x6C00 for channel 15 (channel 7 of group 1), write 0x76C00 at 0x1198. To read the DC Offset value of channel 15, write 0x7 at 0x11A4, then read at 0x1198.

WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	G

Bit	Description
[15:0]	DC Offset value in DAC LSB unit.
[19:16]	Channel index. From 0x0 to 0x7 it addresses a single channel of Group n , while 0xF addresses all channels of Group n .
[31:20]	Reserved

DRS4 Chip Temperature

-

Address	0x1nA0
Mode	R
Attribute	G

Bit	Description
[7:0]	DRS4 temperature from 0°C to 127°C.
[31:8]	Reserved

Group n Channel Selection

This register allows the user to select the channel of group n to read registers 0x1n80 and 0x1n98.
For example, to read the DC Offset of channel 15 (channel 7 of group 1), write 0x7 at 0x11A4, then read at 0x1198.

Address 0x1nA4
Mode R/W
Attribute G

Bit	Description
[3:0]	DAC Channel index for readout, from 0x0 to 0x7.
[31:4]	Reserved

Group n Channel Trigger Mask

This register allows to enable the channels of group n to participate at the trigger generation in logic OR. Channels enabled by this register trigger when the input pulse crosses the threshold (see register 0x1n80). Triggers of group 0 and group 1 enable the acquisition of all channels of group 0 and group 1 simultaneously, while triggers on group 2 and group 3 enable the acquisition of all channels of group 2 and group 3 simultaneously.

Note: this register is implemented from AMC FPGA firmware revision 0.4 on.

Address 0x1nA8, 0x80A8
Mode R/W
Attribute G

Bit	Description
[7:0]	Bit m corresponds to the channel m self-trigger that participates to the group n trigger generation. Options are: 0 = Channel trigger does not participate to the group trigger generation; 1 = Channel trigger participates to the group trigger generation.
[31:8]	Reserved

Group n TR Trigger Threshold

This register sets the trigger threshold of the TRn.

NOTE: Since one TRn is common to two groups, a write access to either 0x10D4 or 0x11D4 leads to the same setting for TR0 input, and a write access to either 0x12D4 or 0x13D4 leads to the same setting for TR1 input (VME only).

Few examples of possible choices of Threshold according to the input pulse are reported in the table below.

NOTE: On boards with Mezzanine PCB Rev.1 and signal on TRn higher than 2 V it is recommended to use an external attenuator.

WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address 0x1nD4, 0x80D4
Mode R/W
Attribute G

Bit	Description
[15:0]	Threshold value for TRn
[31:16]	Reserved

Mezzanine PCB Rev. ≥ 1	
ECL signal on TRn	TRn DC Offset = 0x55A0 / 21920 TRn Threshold = 0x6666 / 26214
NIM signal on TRn	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x51C6 / 20934
Negative signal on TRn: V = 0 ÷ -400mV	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x5C16 / 23574
Negative signal on TRn: V = 0 ÷ -200mV	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x613E / 24894
Bipolar signal on TRn	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x6666 / 26214
TTL on TRn or Positive signal on TRn: V = 0 ÷ ≥ 2 V	TRn DC Offset = 0xA800 / 43008 TRn Threshold = 0x6666 / 26214
Positive on TRn: V = 0 ÷ 2V	TRn DC Offset = 0x91A7 / 37287 TRn Threshold = 0x6666 / 26214

Mezzanine PCB Rev. 0	
NIM signal on TRn	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x717D / 29053
Negative signal on TRn: V = 0 ÷ -400mV	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x6E72 / 28274
Bipolar signal on TRn	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x6C80 / 27776
Positive on TRn: V = 0 ÷ 2V	TRn DC Offset = 0x4000 / 16384 TRn Threshold = 0x7158 / 29016

Group n TR DC Offset

This register sets the DC Offset for the TRn.

NOTE: Since one TRn is common to two groups, a write access to either 0x10DC or 0x11DC leads to the same setting for TR0 input, and a write access to either 0x12DC or 0x13DC leads to the same setting for TR1 input (VME only).

Few examples of possible choices of DC Offset according to the input pulse are reported in the table below.

NOTE: On boards with Mezzanine PCB Rev.1 and signal on TRn higher than 2 V it is recommended to use an external attenuator.

WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address 0x1nDC, 0x80DC
Mode R/W
Attribute G

Bit	Description
[15:0]	DC Offset in DAC LSB unit.
[31:16]	Reserved

Mezzanine PCB Rev. ≥ 1	
ECL signal on TRn	TRn DC Offset = 0x55A0 / 21920 TRn Threshold = 0x6666 / 26214
NIM signal on TRn	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x51C6 / 20934
Negative signal on TRn: $V = 0 \div -400\text{mV}$	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x5C16 / 23574
Negative signal on TRn: $V = 0 \div -200\text{mV}$	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x613E / 24894
Bipolar signal on TRn	TRn DC Offset = 0x8000 / 32768 TRn Threshold = 0x6666 / 26214
TTL on TRn or Positive signal on TRn: $V = 0 \div \geq 2\text{V}$	TRn DC Offset = 0xA800 / 43008 TRn Threshold = 0x6666 / 26214
Positive on TRn: $V = 0 \div 2\text{V}$	TRn DC Offset = 0x91A7 / 37287 TRn Threshold = 0x6666 / 26214

Mezzanine PCB Rev. 0	
NIM signal on TRn	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x717D / 29053
Negative signal on TRn: $V = 0 \div -400\text{mV}$	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x6E72 / 28274
Bipolar signal on TRn	TRn DC Offset = 0x1000 / 4096 TRn Threshold = 0x6C80 / 27776
Positive on TRn: $V = 0 \div 2\text{V}$	TRn DC Offset = 0x4000 / 16384 TRn Threshold = 0x7158 / 29016

Board Configuration

This register contains general settings for the board configuration.

Address 0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
 Mode R/W
 Attribute C

Bit	Description
[2:0]	Reserved
[3]	Test Mode (default value is 0). When the test pattern is enabled, the input samples are replaced by a sawtooth test signal. Options are: 0 = Test Mode disabled; 1 = Test Mode enabled.
[4]	Reserved: must be 1.
[5]	Reserved
[6]	TR Trigger polarity. Options are: 0 = Rising Edge (Default); 1 = Falling Edge.
[7]	Reserved
[8]	Individual trigger (default value is 0): MUST BE 1. NOTE: Despite the other digitizers running Raw Waveform Firmware, the 742 series must have this bit set to 1 to work properly.
[10:9]	Reserved: must be 0
[11]	TRn Readout Enable. When this bit is 1, the signal TRn is digitized and it is present in data readout. Options are: 0 = Signal TRn Readout disabled (Default); 1 = Signal TRn Readout enabled.
[12]	TRn Trigger Enable. When this bit is 1, the TRn signal is used as fast trigger. Options are: 0 = TRn Local Trigger disabled (Default); 1 = TRn Local Trigger enabled.
[13]	Enable the acquisition in "Transparent Mode". When this bit is 1, data in the event are referred to the ADC. Refer to the User Manual for more details. Options are: 0 = Acquisition in Output Mode (Default); 1 = Acquisition in Transparent Mode. Note: this bit is valid from AMC FPGA firmware revision 0.04.
[15]	Enable the signal on TRG-IN to gate/veto the acquisition (see also bit[17] of this register and bits[11:10] of register 0x8110). Options are: 0 = disabled (default); 1 = enabled.
[17]	Signal on TRG-IN connector is used to gate/veto the acquisition. Enable this option through bit[15] of this register. Refer also to bits[11:10] of register 0x8110. Options are: 0 = gate (default); 1 = veto.
[27:18]	Reserved
[31:28]	Select monitor signal from daughter board to TRG-OUT connector (see bits[17:16] of register 0x811C). Options are: 0000 = no signal (default); 0001 = all fast trigger TRn; 0010 = accepted fast trigger TRn; 0011 = busy of all groups in logic OR.

Custom Size

Sets the record length, which is the number of samples (Ns) of the digitized waveform in the acquisition window.

NOTE: modifying the record length does not reduce the dead-time, since all the 1024 capacitances are read anyway for each channel.

WARNING: this register must not be written while the acquisition is running.

Address 0x8020
 Mode R/W
 Attribute C

Bit	Description
[1:0]	Custom size (default value is 00). Options are: 00 = 1024 samples/ch; 01 = 520 samples/ch; 10 = 256 samples/ch; 11 = 136 samples/ch.
[31:2]	Reserved

Test Mode Initial Value

Sets the initial value for the test mode (refer to bit[3] of register 0x8000).

NOTE: This register must be read at address 0x1n7C, where n is the group index, while write access can be performed at address 0x807C only.

Address 0x807C
Mode R/W
Attribute C

Bit	Description
[11:0]	ADC value (default value is 0).
[31:12]	Reserved

DRS4 Sampling Frequency

This register sets the sampling frequency of each DRS4 chip.

WARNING: This register must not be written while the acquisition is running.

NOTE: This register must be read at address 0x1nD8, where n is the group index, while write access can be performed at address 0x80D8 only.

Address	0x80D8
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Frequency options are: 00 = 5 GS/s (default); 01 = 2.5 GS/s; 10 = 1 GS/s; 11 = 750 MS/s; NOTE: Option 11 is valid from AMC firmware revision 1.0. x742 boards bought before the introduction of this option do not have the corrections for this frequency. Please contact CAEN support for the upgrade.
[31:2]	Reserved

Acquisition Control

This register manages the acquisition settings.

Address 0x8100
Mode R/W
Attribute C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). If the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off; 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Trigger Counting Mode (default value is 0). Through this bit it is possible to count the reading requests from channels to mother board. The reading requests may come from the following options: 0 = accepted triggers from combination of channels; 1 = triggers from combination of channels, in addition to TRG-IN and SW TRG.
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Busy signal as input, or to propagate it as output. Options are: 0 = disabled; 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[9]	LVDS I/O Veto Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output. Options are: 0 = disabled (default); 1 = enabled. NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[10]	Reserved.

[11]	<p>LVDS I/O RunIn Enable Mode (VME only). Default value is 0.</p> <p>The LVDS I/Os can be programmed to accept a RunIn signal as input, or to transfer it as output.</p> <p>Options are:</p> <p>0 = starts on RunIn level (default);</p> <p>1 = starts on RunIn rising edge.</p> <p>NOTE: this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 must also be configured for nBusy/nVeto.</p>
[31:12]	Reserved.

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address 0x8104
Mode R
Attribute C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. This bit drives the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' is on).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if the board memory has reached the FULL condition (i.e. maximum number of storable events). Options are: 0 = the board is not FULL; 1 = the board is FULL.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	PLL Bypass Mode. This bit drives the front panel 'PLL BYPS' LED. Options are: 0 = PLL bypass mode is not active ('PLL BYPS' is off); 1 = PLL bypass mode is active and the VCXO frequency directly drives the clock distribution chain ('PLL BYPS' lits). WARNING: before operating in PLL Bypass Mode, it is recommended to contact CAEN for feasibility.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL hasn't had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronised). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the current logical level on TRG-IN front panel connector.
[31:17]	Reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address 0x8108
Mode W
Attribute C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address 0x810C
Mode R/W
Attribute C

Bit	Description
[29:0]	Reserved
[30]	External Trigger (default value is 1). When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger (default value is 1). When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals. Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards). Default value is 0xC0000000.

Address 0x8110
 Mode R/W
 Attribute C

Bit	Description
[3:0]	Bit n corresponds to the signal from group n which participates to the TRG-OUT (GPO) generation. Signal can be selected through bits[31:28] of register 0x8000. Options are: 0 = Signal from group n does not participate to the TRG-OUT (GPO) signal; 1 = Signal from group n participates to the TRG-OUT (GPO) signal. NOTE: In case of DT and NIM boards, only bits[1:0] are meaningful while bits[3:2] are reserved.
[7:4]	Reserved. Note: in case of DT and NIM boards bits[7:2] are reserved.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled input (bits[3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Reserved; 11 = Reserved.
[28:10]	Reserved
[29]	LVDS Trigger Enable (VME boards only). If the LVDS I/Os are programmed as outputs, they can participate in the TRG-OUT (GPO) signal generation. They are in logic OR with the other enabled signals (bits[31:30] and bits[3:0], or [1:0]). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger. When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[31] and bits[3:0] or [1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[30], bits[3:0] or [1:0]). Options are: 0 = disabled; 1 = enabled.

LVDS I/O Data

This register allows to readout the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs (REGISTER mode).

NOTE: this register is supported only by VME boards.

Address 0x8118
Mode R/W
Attribute C

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). If the LVDS I/O new features are enabled (bit[8] of 0x811C) and REGISTER mode is set (through 0x81A0), this register allows to read/write from the corresponding nth LVDS I/O according to its configuration. A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input.
[31:16]	Reserved.

Front Panel I/O Control

This register manages the front panel I/O connectors. Default value is 0x000000.

Address 0x811C
 Mode R/W
 Attribute C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	TRG-OUT Enable (VME boards only). Enables the TRG-OUT LEMO front panel connector. Options are: 0 = enabled (default); 1 = high impedance. NOTE: this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. NOTE: this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards and LVDS I/O old features only). This configuration must be enabled through bit[8] set to 0. Options are: 00 = general purpose I/O; 01 = programmed I/O; 10 = pattern mode: LVDS signals are input and their value is written into the header PATTERN field; 11 = reserved. NOTE: these bits are reserved in case of DT and NIM boards.

[8]	<p>LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0. Please, refer to the User Manual for all details. NOTE: LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. NOTE: this bit is reserved in case of DT and NIM boards.</p>
[9]	<p>LVDS I/Os Pattern Latch Mode (VME boards only). Options are: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post- trigger settings and input latching delays; 1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives. NOTE: this bit is reserved in case of DT and NIM boards.</p>
[10]	<p>TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.</p>
[11]	<p>TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. NOTE: if this bit is set to 1, then bit[10] is ignored.</p>
[13:12]	Reserved.
[14]	<p>Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.</p>
[15]	<p>TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1 = TRG-OUT (GPO) is a test logic level set via bit[14].</p>
[17:16]	<p>TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe) according to bits[31:28] of register 0x8000; 11 = S-IN (GPI) propagation.</p>
[19:18]	<p>Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN/delayedRUN: this is the RUN in case of ROC FPGA firmware rel. less than 4.12. This probe can be selected according to bit[20]. 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY/UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].</p>

[20]	<p>According to bits[19:18], this bit selects the probe to be propagated on TRG-OUT .</p> <p>If bits[19:18] = 00, then bit[20] options are:</p> <p>0 = RUN, the signal is active when the acquisition is running and it is synchronized with the start run. This option must be used to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN (GPI) daisy chain.</p> <p>1 = delayedRUN. This option can be used to debug the synchronization when the start/stop is propagated through the LVDS I/O (VME boards).</p> <p>If bits[19:18] = 11, then bit[20] options are:</p> <p>0 = Board BUSY;</p> <p>1 = PLL Lock Loss.</p> <p>NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower.</p> <p>NOTE: this bit corresponds to BUSY/UNLOCK for ROC FPGA firmware rel. less than 4.12.</p>
[22:21]	<p>Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (VME only).</p> <p>Option are:</p> <p>00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default);</p> <p>Other options are reserved.</p>
[31:23]	Reserved.

Group Enable Mask

This register enables/disables selected groups to participate in the event readout.
WARNING: this register must not be modified while the acquisition is running.

Address 0x8120
Mode R/W
Attribute C

Bit	Description
[3:0]	Group Enable Mask. Default value is 0xF. Bit n can enable/disable group n to participate in the event readout. Options are: 0: disabled; 1: enabled. NOTE: this function concerns only bits[1:0] in case of DT and NIM boards.
[31:4]	Reserved

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.

The complete format is:

Firmware Revision = X.Y (16 lower bits)

Firmware Revision Date = Y/M/DD (16 higher bits)

EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.

EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.

NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address 0x8124

Mode R

Attribute C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Event Stored

This register contains the number of events currently stored in the Output Buffer.

NOTE: the value of this register cannot exceed the maximum number of available buffers according to the register address 0x800C.

Address 0x812C
Mode R
Attribute C

Bit	Description
[31:0]	Number of the current events stored in the Output Buffer.

Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.

A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.

EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.

NOTE: this register is supported by VME boards only.

NOTE: the command must be issued starting from the first to the last board in the clock chain.

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address 0x8140
Mode R
Attribute C

Bit	Description
[7:0]	Digitizer Family Code: 0x06 = 742 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 0x01 = 128 events per channel; 0x08 = 1024 events per channel.
[23:16]	Equipped Groups Number. Options are: 0x02 = 2 groups (DT and NIM boards); 0x04 = 4 groups (VME boards). NOTE: if this number is lower than the physical group number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address 0x814C
Mode R
Attribute C

Bit	Description
[31:0]	Event Size (32-bit words).

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.

NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).

Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.

NOTE: this register is supported by Desktop (DT) boards only.

Address 0x8168
Mode R/W
Attribute C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay, expressed in trigger clock cycles between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG-IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address 0x8170
Mode R/W
Attribute C

Bit	Description
[31:0]	Delay (in steps of about 17 ns).

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.

NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address 0x8178
Mode R
Attribute C

Bit	Description
[3:0]	Internal Communication Timeout. Options are: 0000 = no error; Others = Timeout Error occurred.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).

Options are:

- 1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);
- 2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the trigger request;
- 3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In) or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun);
- 4) 0011 = LEGACY, that is to say according to the old LVDS I/O configuration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting.

Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.

NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.

NOTE: this register is supported by VME boards only.

Address 0x81A0
Mode R/W
Attribute C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration.
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	<p>This bit permits selecting whether the nTrigger signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG-OUT connector or a copy of the acquisition common trigger.</p> <p>Options are:</p> <p>0 = nTrigger output is a copy of TRG-OUT signal</p> <p>1 = nTrigger output is a copy of the acquisition common trigger.</p> <p>NOTE: this bit is reserved for ROC FPGA firmware revisions lower than 4.9.</p>
[31:17]	Reserved.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address 0xEF00
 Mode R/W
 Attribute C

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,...,7 = sets the VME interrupt level. NOTE: these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). NOTE: this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by register 0xEF0C). NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). NOTE: ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. NOTE: this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boards only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFF0 interval. NOTE: in Extended mode, the board VME Base Address is only set via the on-board [31:28] rotary switches or bits[31:28] of register 0xEF10. NOTE: this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

Readout Status

This register contains information related to the readout.

Address 0xEF04
Mode R
Attribute C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Output Buffer Status. Indicates if the Output Buffer is in Full condition. Options are: 0 = the Output Buffer is not FULL; 1 = the Output Buffer is FULL.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[31:3]	Reserved.

Board ID

The meaning of this register depends on which VME crate it is inserted in.

In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

NOTE: this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.
 NOTE: this register is supported by VME boards only.

Address 0xEF0C
 Mode R/W
 Attribute C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1), this register sets the VME Base Address of the module.

NOTE: this register is supported by VME boards only.

Address 0xEF10
Mode R/W
Attribute C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00, they set the VME Base Address of the module.
[31:16]	Reserved.

Interrupt Status/ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

NOTE: this register is supported by VME boards only.

Address 0xEF14
Mode R/W
Attribute C

Bit	Description
[31:0]	STATUS/ID (VME boards only).

Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Address 0xEF18
Mode R/W
Attribute C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER.
[31:10]	Reserved.

Max Number of Events per BLT

This register sets the maximum number of complete events which has to be transferred for each block transfer (via VME BLT/CBLT cycles, or block readout through USB or Optical Link).

Address 0xEF1C
Mode R/W
Attribute C

Bit	Description
[7:0]	MAX NUM EVENT PER BLT.
[31:8]	Reserved

Scratch

This register can be used to write/read words for test purposes.

Address 0xEF20
Mode R/W
Attribute C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address 0xEF24
Mode W
Attribute C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:

- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:

- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

Address 0xEF28
Mode W
Attribute C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address 0xEF34
Mode W
Attribute C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address 0xF000
Mode R
Attribute C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address 0xF004
Mode R
Attribute C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address 0xF008
Mode R
Attribute C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address 0xF00C
Mode R
Attribute C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address 0xF010
Mode R
Attribute C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address 0xF014
Mode R
Attribute C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address 0xF018
Mode R
Attribute C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address 0xF01C
Mode R
Attribute C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address 0xF020
Mode R
Attribute C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address 0xF024
Mode R
Attribute C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address 0xF028
Mode R
Attribute C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address 0xF02C
Mode R
Attribute C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address 0xF030
Mode R
Attribute C

Bit	Description
[7:0]	Board Version Code. Options are: 0x70 = V1742/VX1742/DT5742/N6742; 0x71 = V1740B/VX1740B/DT5742B/N6742B.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address 0xF034
Mode R
Attribute C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address 0xF038
Mode R
Attribute C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address 0xF03C
 Mode R
 Attribute C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address 0xF040
Mode R
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address 0xF044
Mode R
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address 0xF048
Mode R
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address 0xF04C
Mode R
Attribute C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on- board.

Address 0xF050
Mode R
Attribute C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address 0xF080
Mode R
Attribute C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address 0xF084
Mode R
Attribute C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address 0xF088
Mode R
Attribute C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).



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