Technical Information Manual

Revision n. 19

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MOD. V1740

64 CHANNEL 12 BIT
65 MS/S DIGITIZER
MANUAL REV.19

NPO:
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Safety Notices

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

V1740/VX1740 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004/8004A!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

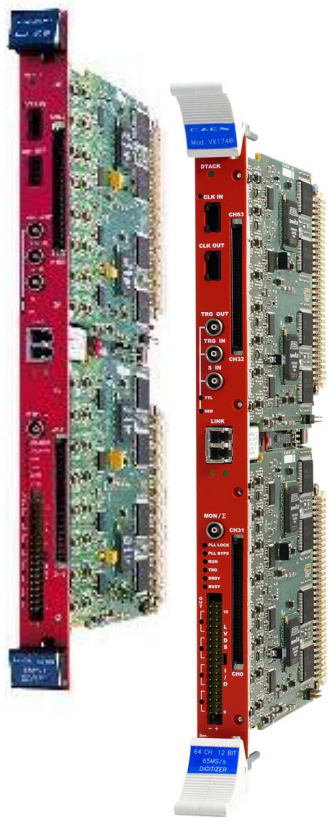
1. Introduction

This document contains the full hardware description of the V1740 and VX1740 modules, and their principle of operating as Waveform Digitizers basing on their default firmware for the waveform recording (hereafter called *default firmware*).

Referred firmware version: 4.10_0.11.

For any reference to registers in this user manual, please refer to the UM5483 - 740 Family Waveform Recording Firmware Registers document, free downloadable at the digitizer web page.

1.1. Overview



The Mod. V1740 is a 1-unit wide VME 6U module housing a 64 Channel 12 bit 62.5 MS/s (65 MS/s using external clock) Flash ADC Waveform Digitizer with 2 V_{pp} dynamic range (10 V_{pp} available on the V1740A/V1740C versions) on single ended ERNI SMC input connectors (or on LEMO connectors using A746B adapter).

The high channel density is allowed by the AD9222 Octal 12-bit 65 MSPS Analog-to-Digital Converter; therefore most channel settings are performed over “groups” of 8 channels (one group per ADC chip).

The DC offset is adjustable via a 16-bit DAC on each 8-channel group in the ±1 V (@ 2 V_{pp}) or ±5 V (@ 10 V_{pp}) range.

The ADC resolution and the sampling frequency make this digitizer well suited for mid-slow detection systems (e.g. inorganic scintillators coupled to PMTs, gaseous detectors).

Each 8-channel group has a SRAM Multi-Event Buffer divisible into 1 ÷ 1024 buffers of programmable size. Two sizes of the channel digital memory are available by ordering options: 192 kS/s or 1.5 MS/s according to the digitizer version (see **Table 1.1**).

V1740D version (EP3C40 Altera FPGA) supports special Digital Pulse Processing firmware for Charge to Digital conversion (DPP-QDC). A x740D module running DPP-QDC firmware becomes multi-channel data acquisition systems for Nuclear Physics or other applications requiring radiation detection.

A common acquisition trigger signal (common to all the channels) can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, in the default firmware, each 8-channel group can generate a trigger request when at least one of the channels goes under/over a programmable threshold. The requests from the groups are processed by the board to generate the common trigger causing all the channels to acquire an event simultaneously. In the DPP firmware, each channel can trigger independently of the others upon

the pulse under/over-threshold; the trigger request is used locally by the channel to acquire the event. The trigger from one board can be propagated to the other boards through the front panel TRG OUT connector

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer

V1740 feature a front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multi-board synchronization is supported, so all V1740 can be synchronized to a common clock source and ensuring Trigger Time Stamps alignment. Once synchronized, all data will be aligned and coherent across the multi-board system. CLK-IN / CLK-OUT connectors allow for a Daisy-chained clock distribution.

16 general purpose LVDS I/Os also FPGA-controlled can be programmed for Busy, Data Ready, Memory Full or Individual Trig-Out management. An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (see § **3.6**).

An analog output (MON/Σ) from internal 12-bit 100-MHz DAC controlled by the FPGA allows to provide out four types of information: Trigger Majority, Test Pulses, Memory Occupancy, Voltage Level (see § **3.7**).

V1740 is equipped with a VME64 interface (VM64X in case of VX1740) where the data readout can be performed in Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME. 2eSST) and 32/64-bit Chained Block Transfer (CBLT).

The module houses Optical Link interface (CAEN proprietary CONET protocol) supporting transfer rate of 80 MB/s and offers Daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller, or up to 32 using a A3818 (4-link version).

VME and Optical Link accesses take place on independent paths and are handled by the on-board controller, therefore when accessed through Optical Link the board can be operated outside the VME Crate.

Table 1.1: Available models, related products and accessories

Code	Description
WV1740XAAAAA	V1740 - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE
WV1740AXAAAA	V1740A - 10Vpp input 64 Ch. 12bit 62.5MS/s Digitizer: 1.5 MS/ch, EP3C16, SE
WV1740BXAAAA	V1740B - 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE
WV1740CXAAAA	V1740C - 10Vpp input 64 Ch. 12bit 62.5MS/s Digitizer: 192kS/ch, EP3C16, SE
WV1740DXAAA	V1740D - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE
WVX1740XAAAA	VX1740 - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE
WVX1740AXAAA	VX1740A - 10Vpp 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE
WVX1740BXAAA	VX1740B - 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE
WVX1740CXAAA	VX1740C - 10Vpp 64 Ch. 12 bit 62.5 MS/s Digitizer: 192 KS/ch, EP3C16, SE
WVX1740DXAAA	VX1740D - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE
WFWDPPQDCAAA(*)	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (x740) (*) Multi-license packs are also available. Please, refer to the Digitizer web page for the relevant ordering options.
WA746BXAAAAA	A746B - 64ch Adapter for Lemo connector
WV1718XAAAAA	V1718 - VME-USB 2.0 Bridge
WV1718LCXAAA	V1718LC - VME-USB 2.0 Bridge (Rohs Compliant)
WVX1718XAAAA	VX1718 - VME-USB 2.0 Bridge
WVX1718LCXAA	VX1718LC - VME-USB 2.0 Bridge
WV2718XAAAAA	V2718 - VME-PCI Bridge
WV2718LCXAAA	V2718LC - VME-PCI Bridge (Rohs compliant)
WK2718LCXAAA	V2718KITLC - VME-PCI Bridge (V2718)+PCI Optical Link (A2818)+Optical Fibre 5m duplex (AY2705) (Rohs)
WK2718XAAAAA	V2718KIT - VME-PCI Bridge (V2718) + PCI OpticalLink (A2818) + Optical Fibre 5m duplex (AY2705)
WK2718XBAAAA	V2718KITB - VME-PCI Bridge (V2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)
WVX2718LCXAA	VX2718LC - VME-PCI Bridge
WVX2718XAAAA	VX2718 - VME-PCI Bridge
WKX2718XAAAA	VX2718KIT - VME-PCI Bridge (VX2718) + PCI OpticalLink (A2818) + Optical Fibre 5m duplex (AY2705)
WKX2718XBAAA	VX2718KITB - VME-PCI Bridge (VX2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)
WKX2718LCXAA	VX2718KITLC - VME-PCI Bridge (VX2718) + PCI Optical Link (A2818) + Optical Fibre 5m duplex (AY2705)
WA2818XAAAAA	A2818 - PCI Optical Link
WA3818AXAAAA	A3818 - PCIe 1 Optical Link
WA3818BXAAAA	A3818 - PCIe 2 Optical Link
WA3818CXAAAA	A3818 - PCIe 4 Optical Link
WA317XAAAAAA	A317 - Clock Distribution Cable
WA318XAAAAAA	A318 - Cable Adapter Single Ended to Differential
WAI2730XAAAA	AI2730 - Optical Fibre 30 m. simplex
WAI2720XAAAA	AI2720 - Optical Fibre 20 m. simplex
WAI2705XAAAA	AI2705 - Optical Fibre 5 m. simplex
WAI2703XAAAA	AI2703 - Optical Fibre 30cm. simplex
WAY2730XAAAA	AY2730 - Optical Fibre 30 m. duplex
WAY2720XAAAA	AY2720 - Optical Fibre 20 m. duplex
WAY2705XAAAA	AY2705 - Optical Fibre 5 m. duplex

1.2. Block Diagram

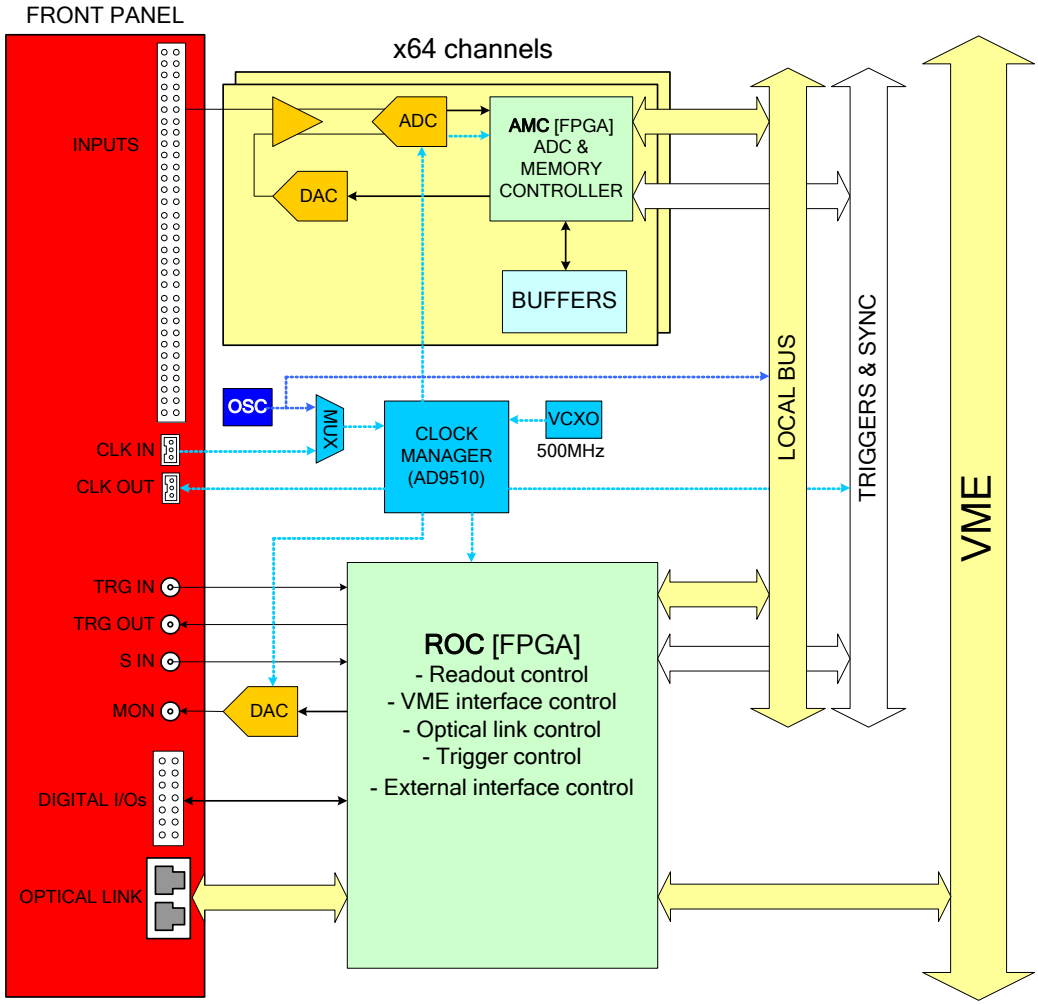


Fig. 1.1: Mod. V1740 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical Specifications

2.1. Packaging and Compliancy

V1740 is housed in a 6U-high, 1U-wide VME unit. The board hosts the VME P1 and P2 connectors, and fits into both VME/VME64 standard and V430 backplanes.
VX1740 versions fit VME64X compliant crates.
In any cases, only well ventilated crates must be used.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

V1740/VX1740 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004/8004A!

2.2. Power Requirements

The table below resumes the V1740 power consumptions per relevant power supply rail.

Table 2.1: Power requirements table

Supply Rail	V1740	V1740D
+5 V	5.6 A	4.9 A
+12 V	0.25 A	0.25 A
-12 V	*Not used*	*Not used*

NOTE: reported power requirements are different in case of old revisions of the motherboard (rev. 3 or lower). The revision can be read at 0xF04C *Configuration ROM* register. Please, contact CAEN for information (see § **8**).

2.3. Front Panel

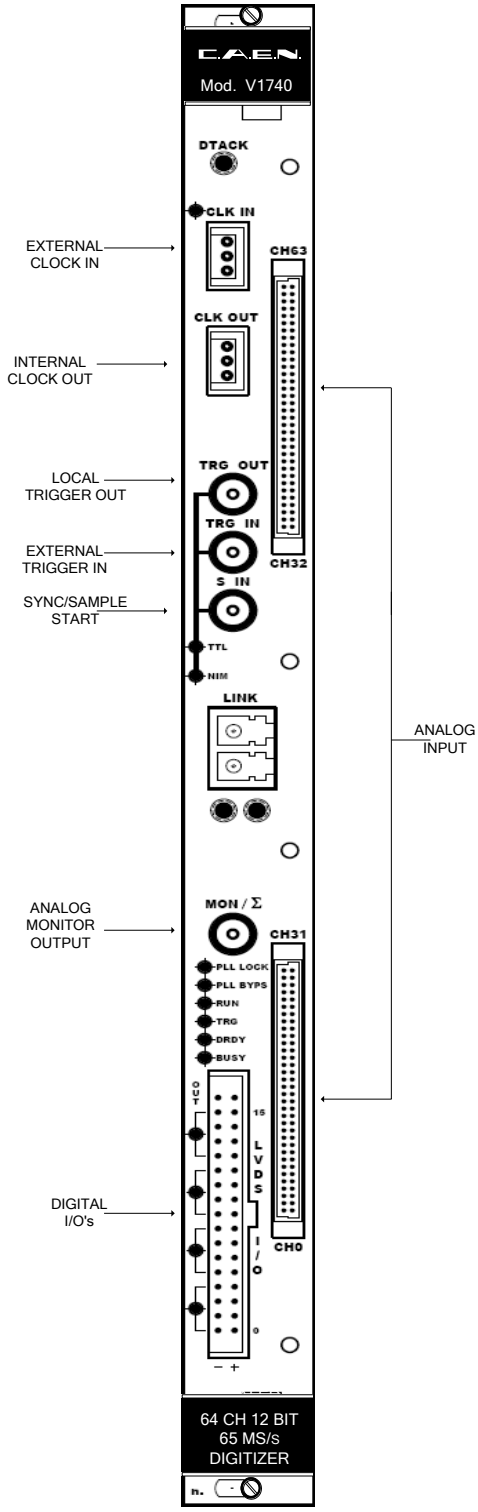


Fig. 2.1: Mod. V1740 front panel

2.4. External Connectors

2.4.1. ANALOG INPUT Connectors

The module has 64 channels on two single-ended ERNI SMC input connectors (see **Fig. 2.2**)

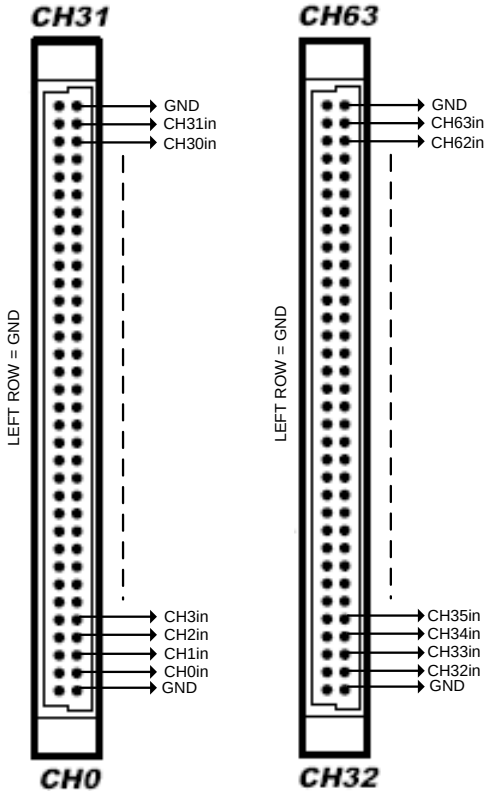


Fig. 2.2: ERNI SMC Connectors

Fig. 2.3: A746B plug to adapt from ERNI to LEMO input channels

Function: Analog input, single ended, input dynamics: $2V_{pp}$, Z_{in}=50Ω (V1740A/V1740C: $10V_{pp}$ Z_{in}=1kΩ).

Mechanical specifications:
Two ERNI SMC-114805 Dual Row 68pin connectors.

Absolute max analog input voltage = $6V_{pp}$ (with V_{rail} max to +6V or -6V) for any DAC offset value.

NOTE: Ensure that alignment is correct during insertion/extraction operations; incorrect alignment may lead to connector damage.

All 64 channels can be available on as many single-ended LEMO connectors by using the A746B adapter (see **Fig. 2.3**).

2.4.2. CONTROL Connectors

Function:

- **TRG-OUT**: digital output connector (NIM/TTL, on R_t = 50Ω) to propagate

  – the internal trigger sources;
  – the channel probes (i.e. signals from the mezzanines);
  – S-IN signal

  according to register addresses 0x8110 and 0x811C, or

  – the motherboard probes (i.e. signals from the motherboard), like the Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal or Busy signal

  according to register address 0x811C.

- **TRG-IN**: digital input connector (NIM/TTL, Z_{in}= 50Ω) for the external trigger.

- **S-IN**: SYNC/START/STOP digital input connector (NIM/TTL, Z_{in}=50Ω) configurable as reset of the time stamp (see § **3.9.3**) or to start/stop the acquisition (see § **3.3.1**)

- **MON/Σ**: 12-bit 100 MHz DAC Analog Monitor output connector ($1V_{pp}$ on R_t=50Ω) with 4 programmable modes (see § **3.7**).

  – Trigger Majority
  – Test Pulses
  – Memory Occupancy
  – Voltage Level

Mechanical specifications: 00-type LEMO connectors.

2.4.3. ADC REFERENCE CLOCK Connectors

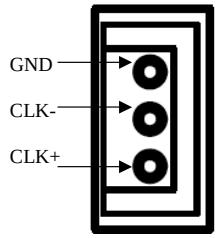


Fig. 2.4: AMP CLK IN/OUT Connector

Function:

- **CLK-IN**: External clock/reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Z_{diff} = 100Ω. CAEN provides single-ended to differential A318 cable adapter (see **Table 1.1**).

- **CLK-OUT**: Clock output, DC coupled (diff. LVDS), Z_{diff} = 100Ω.

Mechanical specifications:
AMP 3-102203-4 connector.

2.4.4. Digital I/O Connectors

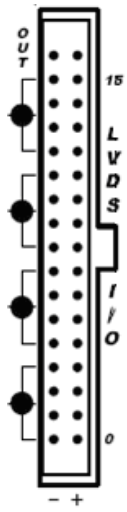


Fig. 2.5: Programmable IN/OUT Connector

Function:
16-pin connector with programmable general purpose LVDS I/O signals (differential LVDS, Z_{diff} = 100Ω) organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15 (highest couple not connected). In/Out direction is software controlled. See § **3.6** for configurable options.

Mechanical specifications:
3M-7634-5002- 34 pin Header Connector

2.4.5. Optical LINK Connector

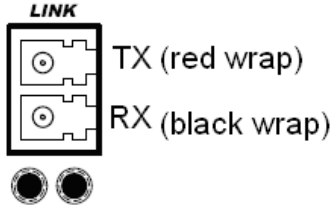


Fig. 2.6: LC Optical Connector

Function:
Optical LINK connector for data readout and flow control (up to 80 MB/s transfer rate). Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides. CAEN provides optical fiber cable selection for A3818 and A2818 Controllers (see **Table 1.1**) with duplex connector on the controller side and two simplex connectors on the digitizer side; the simplex connector with the black wrap is for the RX line (lower) and the one with the red wrap is for the TX (higher).

Mechanical specifications:
SFF Transceiver series, FTLF8519F-2KNL type (LC connectors)

2.5. Other Front Panel Components

2.5.1. Diagnostic LEDs

The front panel hosts the following LEDs:

Table 2.2 : Front panel LEDs

Name:	Colour:	Function:
DTACK	green	Indicates there is a VME read/write access to the board
CLK IN	green	Indicates that the external clock is enabled
TTL	green	Indicates that the standard TTL is set for TRG-OUT, TRG-IN and S-IN
NIM	green	Indicates that the standard NIM is set for TRG-OUT, TRG-IN and S-IN
LINK	green/yellow	The right green LED indicates the network presence; the left yellow LED signals the data transfer activity
PLL LOCK	green	Indicates that the PLL is locked to the reference clock
PLL _BYPS	green	NOT USED
RUN	green	Indicates that the acquisition is running (data taking)
TRG	green	Indicates that the trigger is accepted
DRDY	green	Indicates that the event/data is present in the Output Buffer
BUSY	red	Indicates that all the buffers are full for at least one channel
OUT_LVDS	green	Each LED close to a 4-pin group lights on if the pins are set as outputs

2.6. Internal Components

SW2,4,5,6 "Base Addr. [31:16]": Type: 4 rotary switches
Function: set the VME base address of the module

SW3 "CLOCK SOURCE INT/EXT": Type: Dip Switch
Function: selects the clock source (External or Internal)

SW1 "FW BCK/STD": Type: Dip Switch
Function: selects between the "Standard" (STD) and the "Backup" (BKP) FLASH page as the first to be read at power-on to load the FW on the FPGAs (default position is STD); see § **7**

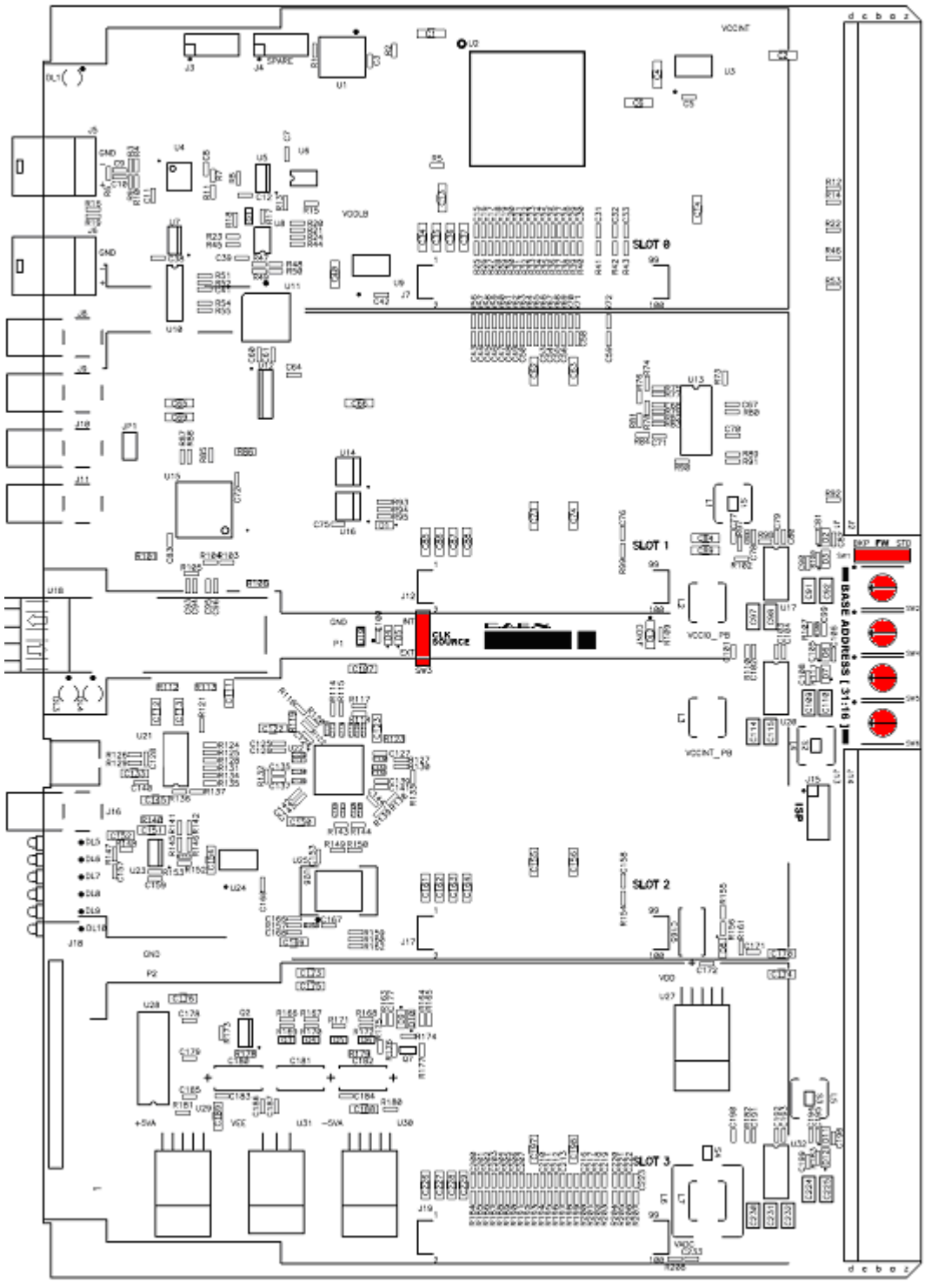


Fig. 2.7: Rotary and dip switches location

2.7. Technical Specifications Table

Table 2.3 : Mod. V1740 technical specifications

GENERAL	**Form Factor** 1-unit wide, 6U VME64 (V1740) and VME64X (VX1740)		**Weight** 535 g
ANALOG INPUT	**Channels** 64 channels Single-ended **Impedance** Z_{in} = Ω @ $2V_{pp}$ Z_{in} = 1 kΩ @ $10V_{pp}$ *(1) "size1 / size2" denotes different model versions*	**Connector** ERNI SMC Dual Row 68-pin **Full Scale Range** 2 V_{pp} / 10 V_{pp} *(1)*	**Bandwidth** 30 MHz **Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ±1 V (@2Vpp); ±0.5 V (@10Vpp)
DIGITAL CONVERSION	**Resolution** 12 bits	**Sampling Rate** 62.5 MS/s simultaneously on each channel 65 MS/s using external clock	
SYSTEM PERFORMANCE	**ENOB** 11.20 (48 kS Buffer) **SINAD** 69.20 dB (48 kS Buffer, open input)	**THD** 87.10 dB **SFDR** 94.9 dB	**SIGMA** 0.50 LSB rms
ADC CLOCK GENERATION	Clock source: internal/external; on-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (CLK-IN connector) reference		
I/O CONNECTORS	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Jitter<100ppm requested **TRG-IN (LEMO)** External trigger digital input NIM/TTL; Z_{in} = 50 Ω	**CLK-OUT (AMP Modu II)** DC coupled differential; LVDS clock output locked at ADC sampling clock **TRG-OUT (LEMO)** Trigger digital output; NIM/TTL; R_t = 50 Ω	**S-IN (LEMO)** SYNC/START front panel digital input NIM/TTL Z_{in} = 50 Ω
MEMORY	192 kS/ch or 1.5 MS/ch Multi-event Buffer divisible into 1 ÷ 1024 buffers Independent read and write access; programmable event size and pre-post trigger		
TRIGGER	**Trigger Source** *Self-trigger* channel over/under-threshold for Common (default firmware) or Individual (DPP firmware only) Trigger generation *External-trigger*: Common Trigger by TRG-IN or LVDS I/O *Software-trigger*: Common Trigger by software command	**Trigger Propagation** TRG-OUT programmable digital output **Trigger Time Stamp** *Default FW*: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension available by firmware *DPP-QDC FW:* 32-bit counter, 16 ns resolution, 68 s range; 48-bit extension by firmware; 64-bit extension by software	
SYNCHRONIZATION	**Clock Propagation** *Daisy chain*: through CLK-IN/CLK-OUT connectors *One-to-many*: clock distribution from an external clock source on CLK-IN connector Clock Cable delay compensation	**Acquisition Synchronization** Sync, Start/Stop through digital I/O (S-IN or TRG-IN input; TRG-OUT output) **Trigger Time Stamps Alignment** By S-IN input connector	
ADC & MEMORY CONTROLLER	Altera Cyclone EP3C16 or EP3C40 (V1740D and VX1740D only) One FPGA serves 4 channels		

COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)		
ANALOG MONITOR	12-bit / 125MHz DAC FPGA controlled; four operating modes: Test pulses: 1Vpp ramp generator Majority signal: proportional to the nr. Of channels under/over threshold (steps of 125 mV) Buffer Occupancy signal: proportional to the Multi Event Buffer Occupancy (1 buffer ~ 1mV) Voltage level: programmable output voltage level			
LVDS I/O	16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker			
DPP FW SUPPORTED	DPP-QDC firmware for the Charge to Digital Conversion supported only by V1740D and VX1740D versions			
FIRMWARE UPGRADE	Firmware can be upgraded via VMEbus/Optical Link			
SOFTWARE	General purpose C libraries, configuration tools, readout software (Windows and Linux support)			
POWER CONSUMPTIONS	**Mod. / Supply Rail**	**@ +5V**	**@ +12 V**	**@ -12V**
	V1740	5.6 A	250 mA	*Not used*
	V1740D	4.9 A	250 mA	*Not used*

3. Functional Description

3.1. Analog Input Stage

Input dynamic is $2V_{pp}$ (Z_{in} = 50 Ω). A $10V_{pp}$ (Z_{in} = 1 kΩ) dynamic is available on request. By means of a 16-bit DAC it is possible to add up to a ±1V DC offset (±5V @$10V_{pp}$) in order to preserve the full dynamic range also with unipolar positive or negative input signals.
The input bandwidth ranges from DC to 30 MHz by 2nd order linear phase anti-aliasing low pass filter.

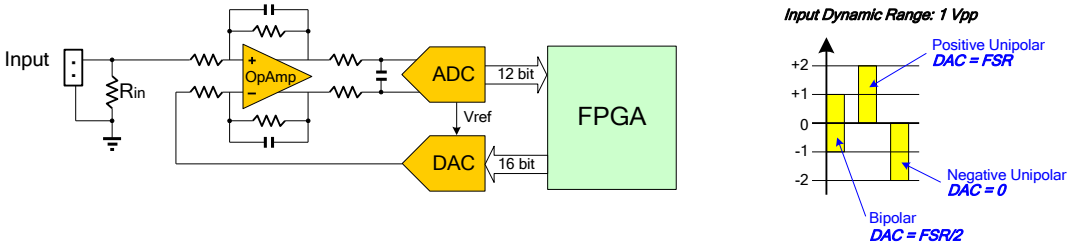


Fig. 3.1: Input diagram

3.1.1. DC Offset Common Setting

Setting the DC offset requires a write access at register addresses 0x1n98. The DC offset value will be then applied to all the 8 channels of group n.

3.1.2. DC Offset Individual Setting

It is possible to apply a 8-bit positive digital offset individually to each channel inside a group to finely correct the baseline mismatch.

The two 32-bit registers that encode the eight unsigned values for group n (n = 0..7) are:

0x10C0 + 0x100 * n -> Correction values for channel offset 0..3
0x10C4 + 0x100 * n -> Correction values for channel offset 4..7

Please, see *UM5483 - 740 Family Waveform Recording Firmware Registers* document for details.

NOTE: DC Offset individual setting is supported from the mezzanine (AMC FPGA) firmware revision **0.10** on.

3.2. Clock Distribution

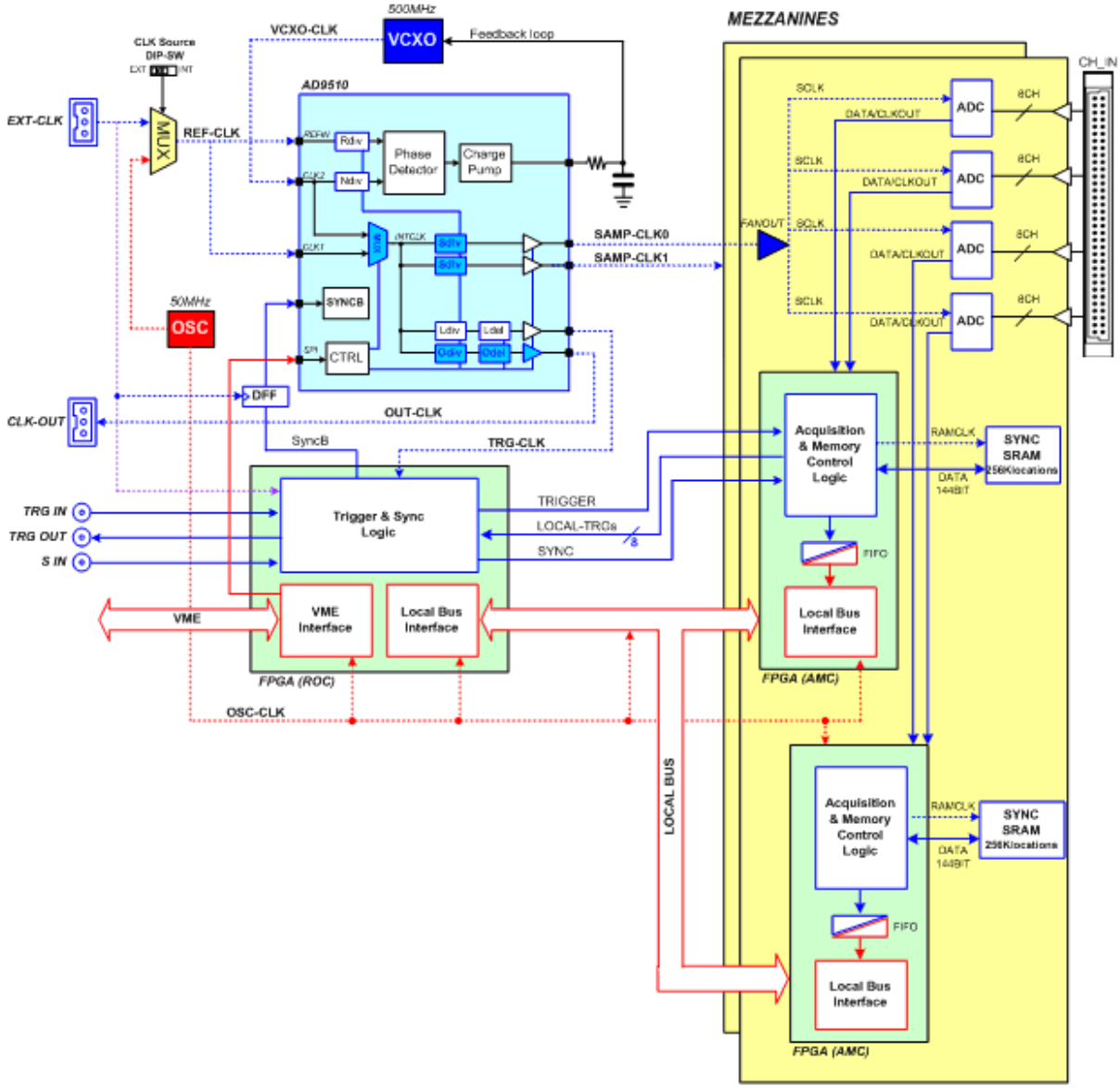


Fig. 3.2: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50-MHz clock provided by an on board oscillator, the latter provides the ADC sampling clock.

OSC-CLK handles both VME and Local Bus (communication between motherboard and mezzanine boards; see red traces in **Fig. 3.2**).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source (selection is performed via dip switch SW1, see § **2.6**); in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).

V1740 uses an integrated phase-locked-loop (PLL) and clock distribution device, AD9510. This component generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0/SAMP-CLK1), as well as the trigger logic synchronization clock (TRG-CLK).
Both clocks can be generated from the internal oscillator (50 MHz) or from external clock input. By default, the board uses the internal clock as PLL reference (REF-CLK).
The external clock can be selected by SW3 on-board switch (see **Fig. 2.7**). The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100ppm (see **Table 2.3**).
The AD9510 configuration can be changed and stored into non-volatile memory. Changing the AD9510 configuration is primarily intended to be used for external PLL reference clock frequency change.
V1740 locks to an external 50 MHz clock with default AD9510 configuration; see § **3.2.1**.

Refer to the AD9510 datasheet for more details:
http://www.analog.com/media/en/technical-documentation/data-sheets/AD9510.pdf
(in case the active link above doesn't work, copy and paste it on the internet browser)

3.2.1. PLL Mode

The Phase Detector within the AD9510 device allows to couple REF-CLK with a VCXO (500 MHz frequency) providing out the nominal ADCs frequency (62.5 MHz); for this purpose, it is necessary that REF-CLK is a submultiple of the VCXO frequency.

As introduced in § **3.2**, the source of the REF-CLK signal can be external (see **Fig. 3.2**) on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW3 (see **Fig. 2.7**).

The following options are allowed:

1. 50 MHz internal clock source – It's the standard operating mode, where the default AD9510 configuration doesn't require to be changed. OSC-CLK = REF-CLK.

2. 50 MHz external clock source – In this case, it is not required to reprogram the AD9510 dividers, as the external clock reference is identical to the frequency of the internal oscillator. CLK-IN = OSC-CLK = REF-CLK.

3. External clock source different from 50 MHz – In this case, it is necessary to re-program the AD9510 dividers in order to lock the VCXO to REF-CLK and provide the 62.5 MHz nominal sampling frequency. The allowed external frequencies are submultiples of the VCXO frequency (500 MHz). CLK-IN = REF-CLK.

The user can configure the clock parameters, generate the PLL programming file and load it on the board by using the CAENUpgrader software tool. See § **5.1** for the program description and documentation reference.

In order the board to sense the external signal on CLK-IN and use it as new reference (points 2 and 3), the user must set the on-board SW3 switch on the EXT position (see **Fig. 2.7**).

3.2.2. Reducing the Sampling Frequency

It could be required to operate the V1740 at a sampling frequency (SAMP-CLK) lower than the nominal. In principle, this can be alternatively achieved by:

1. Direct way: reprogramming the AD9510 dividers in order to lock the VCXO to REF-CLK and provide out the desired SAMP-CLK, which must be a submultiple of the VCXO frequency. REF-CLK can be configured as in § **3.2.1**. Not all the frequencies are admitted and a lower frequency limit must be considered, due to the internal electronics.
   Please, contact CAEN (see § **8**) for the feasibility of this method.

2. Indirect way: enabling the Decimation option in the firmware (see § **3.2.3**).

3.2.3. Decimation

This functionality is a firmware option based on the programmability of a decimation factor *n*. During the acquisition, the firmware processes the digitized input waveforms calculating an averaged value of the "decimated" 2^n consecutive samples. The self-trigger is then issued as soon as an averaged value exceeds the programmed threshold (see § **3.4.3**). Software trigger and external trigger are not affected by decimation option.

While the real sampling frequency doesn't change (i.e. 62.5 MS/s), the decimation effect is to change the rate the data are written into the digitizer memory. The readout data result so at a sampling frequency changed according to the formula:

$$\frac{62.5}{2^n}\text{MS/s}$$

where *n* = [0,1,…,7].
The *n* paramenter is set through the register address 0x8044 (see § **1**).

Decimation functionality is supported by:

- CAENDigitizer library **revision ≥ 2.5.0**
- WaveDump software **revision ≥ 3.6.4**

NOTE: Decimation is supported only by 740 series running a AMC FPGA firmware **revision ≥ 0.7** (see § **7**).

3.2.4. Trigger Clock

The Trigger logic (TRG-CLK) works at 125-MHz frequency (2* SAMP_CLK), while, at the motherboard level, triggers are sensed, generated and distributed at 62.5-MHz frequency. The actual trigger clock frequency is so the same as the sampling one (see also § **3.3.2**).

3.2.5. Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see § **2.4.3**). This option is particularly useful in case of multi-board synchronization to propagate the clock reference source in Daisy Chain. This option can be enabled by the user while configuring the PLL programming file in the CAENUpgrader *PLL Upgrade* GUI.

3.3. Acquisition Modes

3.3.1. Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[1:0] setting at register address 0x8100 and bit[2] of the same register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): bit[2] = 1 arms the acquisition and the Start is issued as the S-IN signal is set high and the Stop occurs when it is set low. If bit[2] = 0 (disarmed), the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bits[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see § **3.6**).

3.3.2. Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store the 31-bit counter value of the Trigger Time Tag (TTT).
  The counter (representing a time reference), like so the Trigger Logic Unit (see § **3.2**) operates at a frequency of 125 MHz (i.e. 8 ns, that is to say ½ ADC clock cycles). Due to the way the acquired data are written into the board internal memory (i.e. in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always “0”;

- increment the EVENT COUNTER;

- fill the active buffer with the pre/post-trigger samples, whose number is programmable (record length), freezing then the buffer for readout purposes, while acquisition continues on another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).
If the board is programmed to accept the overlapped triggers, as the “overlapping” trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one. In this case events will not have all the same size (see **Fig. 3.3** below).

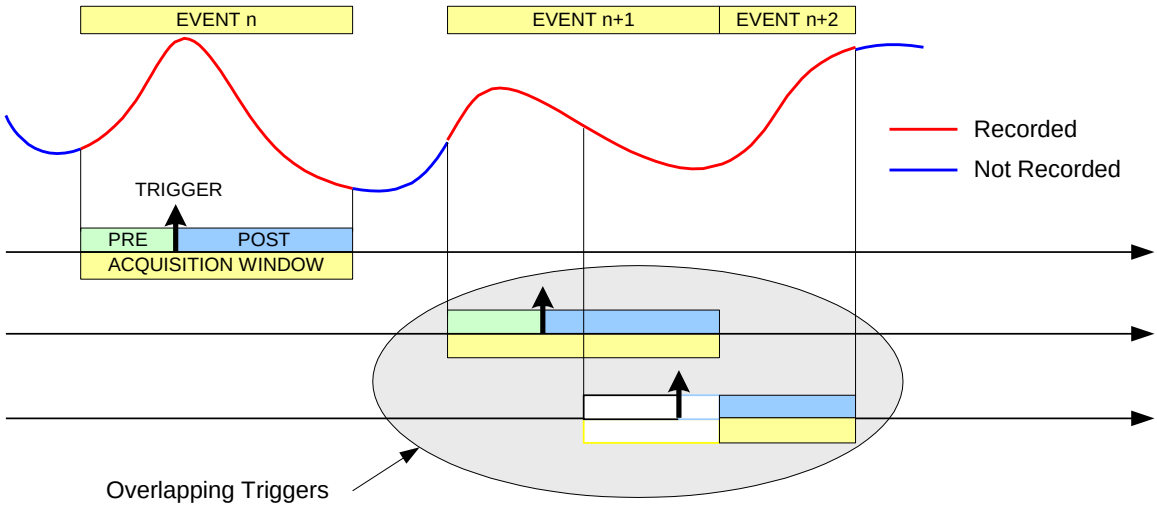


Fig. 3.3: Trigger Overlap

A trigger can be refused for the following causes:

- acquisition is not active;
- memory is FULL and therefore there are no available buffers;
- the required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the *RUN Acquisition* command (see § **3.3.1**) or with respect to a buffer emptying after a *Memory FULL* status (see § **3.3.5**);
- the trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The EVENT COUNTER can be programmed in order to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and readout.

3.3.3. *Multi-Event Memory Organization*

Each channel of the V1740 features a SRAM memory to store the acquired events. The memory size for the event storage is 192 kS/ch or 1.5 MS/ch, according to the board version (see **Table 1.1**), and it can be divided in a programmable number of buffers, N_b, (N_b from 1 up to 1024) by the register address 0x800C, as described in **Table 3.1** below.

Table 3.1: Buffer Organization

Register Value	Buffer Number (N_b)	Size of one Buffer (Samples)	
		SRAM 192kS/ch	SRAM 1.5 MS/ch
0x00	1	192k	1.5M
0x01	2	96k	750k
0x02	4	48k	384k
0x03	8	24k	192k
0x04	16	12k	96k
0x05	32	6k	48k
0x06	64	3k	24k
0x07	128	1536	12k
0x08	256	768	6k
0x09	512	384	3k
0x0A	1024	192	1536

3.3.3.1. Custom Sized Events

In case an event size minor than the buffer size is needed, the user can set the N_{LOC} value at register address 0x8020, where N_{LOC} is the number of memory locations.
The size of the event is so forced to be according to the formula:

$$3*N_{LOC} = 2*N_{Sample}$$

In consequence of that, only values that are multiples of 3 are allowed for this register (setting N_{LOC} = 0, the custom size is disabled).

NOTE: The value of N_{LOC} must be set in order that the relevant number of samples does not exceed the buffer size and it mustn't be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_{LOC}, but they are still determined by N_b

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The *Record Length* parameter defined in CAEN software (such as WaveDump and CAENScope introduced in § **5**) and the *Set/GetRecordLength()* functions of the CAENDigitizer library (see § **4.2**) rely on these concepts.

3.3.4. *Event Structure*

The event can be readout via VMEbus or Optical Link; data format is 32-bit long word (see **Fig. 3.4**).

An event is structured in:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

3.3.4.1. Header

The **Header** consists in 4 words including the following information:

- **EVENT SIZE (Bit[27:0] of 1st header word)** = It is the size of the event (number of 32-bit long words);
- **BOARD ID (Bit[31:27] of 2nd header word)** = It is the GEO address, meaningful only for VME64X modules;
- **BOARD FAIL flag (Bit[26] of 2nd header word)** = Implemented from ROC FPGA firmware revision **4.5** on (*reserved* otherwise), this bit is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading at register address 0x8104 and contact CAEN Support Service if necessary (see § **8**);
- **BIT[23:8] (2nd header word)** = It is the 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives;

  NOTE: Starting from revision **4.6** of the ROC FPGA firmware, these 16 bits can be programmed to provide trigger information according to the setting of the bits[22:21] at register address 0x811C (see **Table 3.2**).

Table 3.2: Pattern configuration table

REGISTER 0x811C Bits[22:21]	FUNCTIONAL DESCRIPTION	PATTERN INFORMATION (16 bits in the 2nd header word)
00 (default)	PATTERN	Pattern of the 16 LVDS signals
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bits[23:19] = 0000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16] = Trigger from LVDS connector Bits[15:8] = Trigger requests from the groups (refer to § **3.4.3**)
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where Bits[23:8] contributes as the 16 most significant bits together to the 32-bit TTT field (4th header word) **Note:** in the ETTT option, the overflow bit is not provided
11	*Not used*	If configured, it acts like "00" setting

- **Group mask (Bit[7:0] of the 2nd header word) =** It is the mask of the groups participating in the event (e.g. GR5 and GR7 participating → Group Mask = 0xA0). This information must be used by the software to acknowledge which group the samples are coming from (the first event contains the samples from the group with the lowest number);
- **Event Counter (Bit[23:0] of 3rd header word)** = This is the trigger counter; it can count either accepted triggers only or all triggers.
- **Trigger Time Tag (Bit[31:0] of 4th header word)** = it is the 31-bit Trigger time Tag (TTT) information (31 bit counter and 32nd bit as roll over flag), which is the trigger time reference. If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Extended Trigger Time Tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the roll over flag is no more provided. The trigger time tag is reset either at the start of acquisition, or via front panel signal on S-IN or LVDS I/O connectors, and increments with every ½ ADC clock cycles. So, TTT resolution is 16 ns and ranges up to 17 s (i.e. 8 ns*(2^{31}-1)), which can be extended to 625 h (i.e. 8 ns*(2^{48}-1)) by the Extended Trigger Time Tag option.

3.3.4.2. Data

Data are the stored samples. Data from masked channels are not read.

3.3.4.3. Event Format Examples

Fig. 3.4 shows the event format of the V1740 digitizer as described in § **3.3.4**.

NOTE: data transfer starts from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group (from 0 to 7) begins.

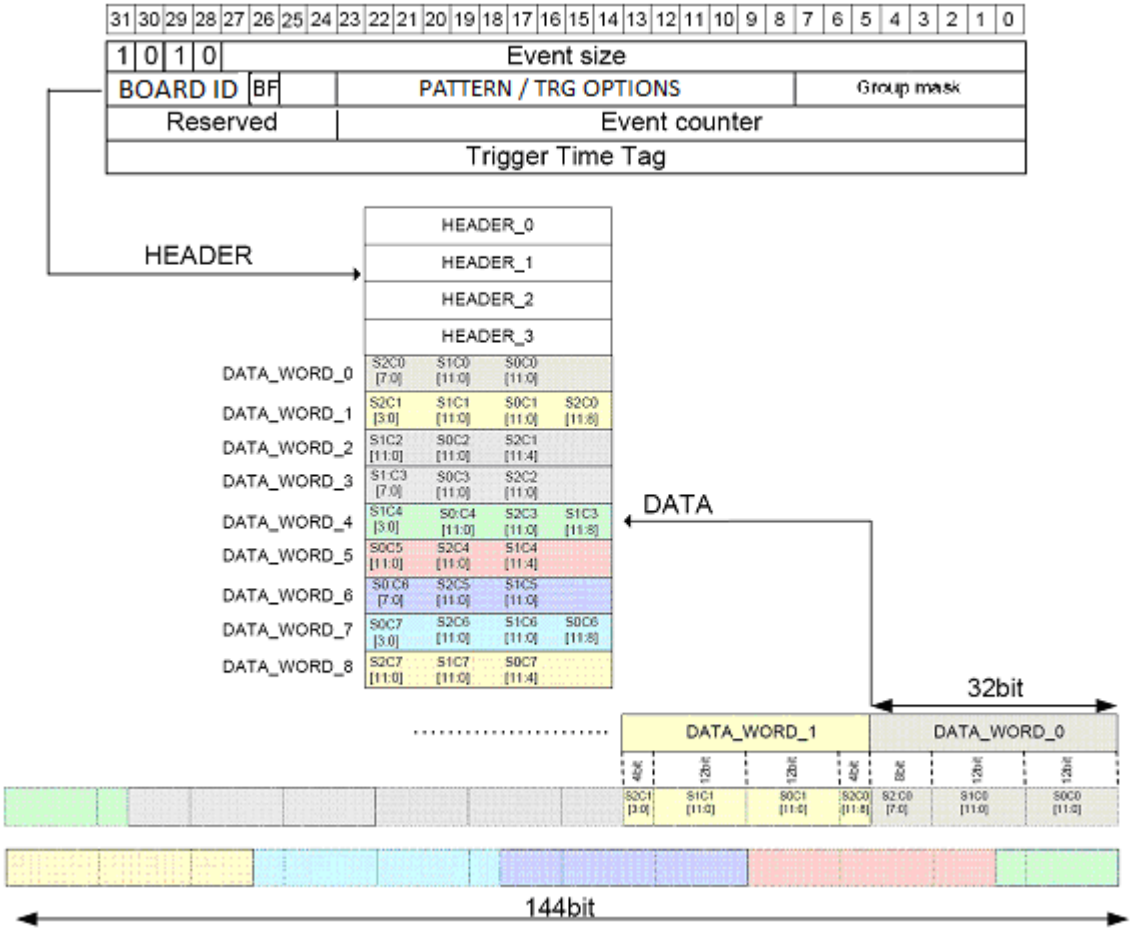


Fig. 3.4: Event format example

3.3.5. Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N_b of circular buffers (N_b = [1:1024], see **Table 3.1**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via VMEbus or Optical Link. The acquisition can continue without dead-time in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as one buffer is readout and becomes free, the board exits the FULL condition and acquisition restarts.

IMPORTANT NOTE: When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100. The board is so programmed to enter the FULL condition when N_b-1 buffers are filled: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is readout and becomes free, the boards exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).

NOTE: when bit[5] = 1, the minimum number of circular buffers to be programmed is N_b = 2.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In this cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level to “X” (register address 0x816C), the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or N_b-1, depending on bit[5] at register address 0x8100 as above described.

It is possible to provide the BUSY signal on the digitizer front panel TRG-OUT output (bit[20], bits[19:18] and bits[17:16] at register address 0x811C are involved). In case of multi-board setup, the BUSY signal can be propagated among boards through the front panel LVDS I/O connector (see § **3.6**).

3.4. Trigger Management

According to the default firmware operating, all the channels in a board share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (a determined number of samples according to buffer organization and custom size settings, and position with respect to the trigger given by the post-trigger).

NOTE: For the trigger management in the DPP-QDC firmware operating, please refer to the web available *UM4874 - DPP-QDC User Manual*.

The generation of a common acquisition trigger is based on different trigger sources (configurable at register address 0x810C):

- **Software trigger**
- **External trigger**
- **Self-trigger**
- **LVDS I/O trigger**
- **Coincidence**

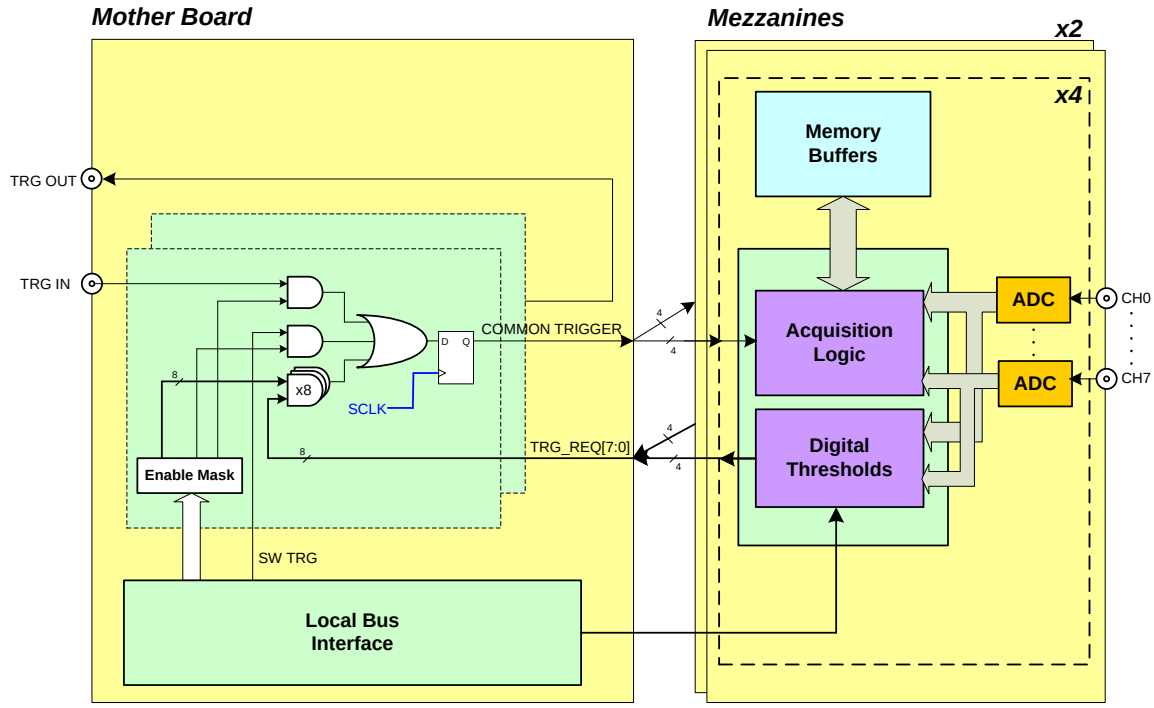


Fig. 3.5: Block diagram of the trigger management

3.4.1. Software Trigger

Software triggers are internally produced via a software command (write access at register address 0x8108) through VMEbus or Optical Link.

3.4.2. External Trigger

A TTL or NIM external signal can be provided to the front panel TRG-IN connector (configurable at register address 0x811C). If the external trigger is not synchronized with the internal clock, a 1-clock period jitter occurs.

3.4.3. Self-Trigger

In the trigger domain, the input channels of the V1740 are managed as 8-channel groups: 0÷7, 8÷15, 16÷23, 24÷31, 32÷39, 40÷47, 48÷55, 56÷63. Each channel in a group (GRx_CHy_IN) is able to generate a self-trigger signal (SELF_TRG) when the digitized input pulse goes over or under a configurable threshold, according to bit[6] of register address 0x8000 (see **Fig. 3.6**). The threshold, common to each group, is set through the register address 0x1n80. The self-triggers of each group are ORed to generate a trigger request (TRG_REQ). The trigger requests are then propagated to the central trigger logic where they are ORed to produce the board common trigger, which is finally distributed back to all channels in the groups causing the event acquisition (see **Fig. 3.5**).

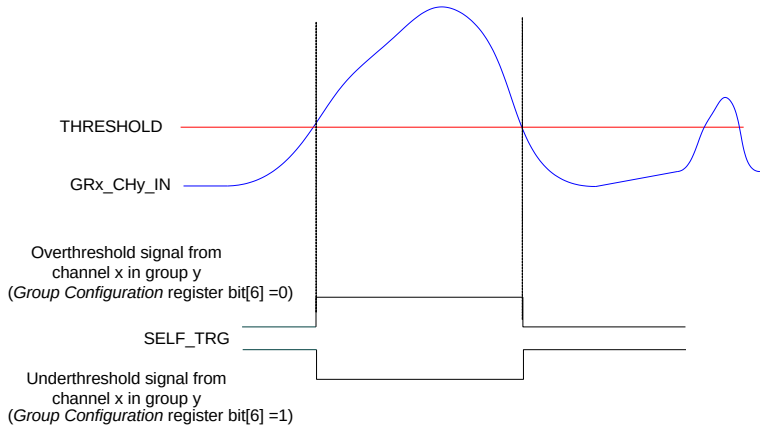


Fig. 3.6: Self-trigger generation

The FPGA, through the register address 0x1nA8, can be programmed to decide which channels in the group do participate in the trigger request generation.

Besides, the FPGA, through the register address 0x810C, can be programmed to enable those groups to participate in the board common trigger generation.

3.4.4. LVDS I/O Trigger

LVDS I/O specific pins on the front panel dedicated connector can be programmed as trigger inputs and enabled to participate in the common trigger generation with other trigger sources. Refer to § **3.6** for details.

3.4.5. Trigger Coincidence Level

Operating with the default firmware, the acquisition trigger is a board common trigger. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Enabling the coincidences is possible by writing at register address 0x810C:

- Bits[7:0] enable the trigger requests (i.e. the groups) to participate in the coincidence;
- Bits[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock (8ns);
- Bits[26:24] set the Majority (i.e. Coincidence) level; the coincidence takes place when:

Number of enabled trigger requests > Majority level

Supposing bits[7:0] = FF (i.e. all groups are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever at least two of the enabled trigger requests are in coincidence within the programmed T_{TVAW}.
The Majority level must be smaller than the number of channels groups enabled via bits[7:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the common trigger is simple OR of the enabled trigger requests.

In the following figures, to simplify the plots, only the first two groups are considered as enabled and so only one channel per group

Fig. 3.7 shows the trigger management in case the coincidences are disabled.

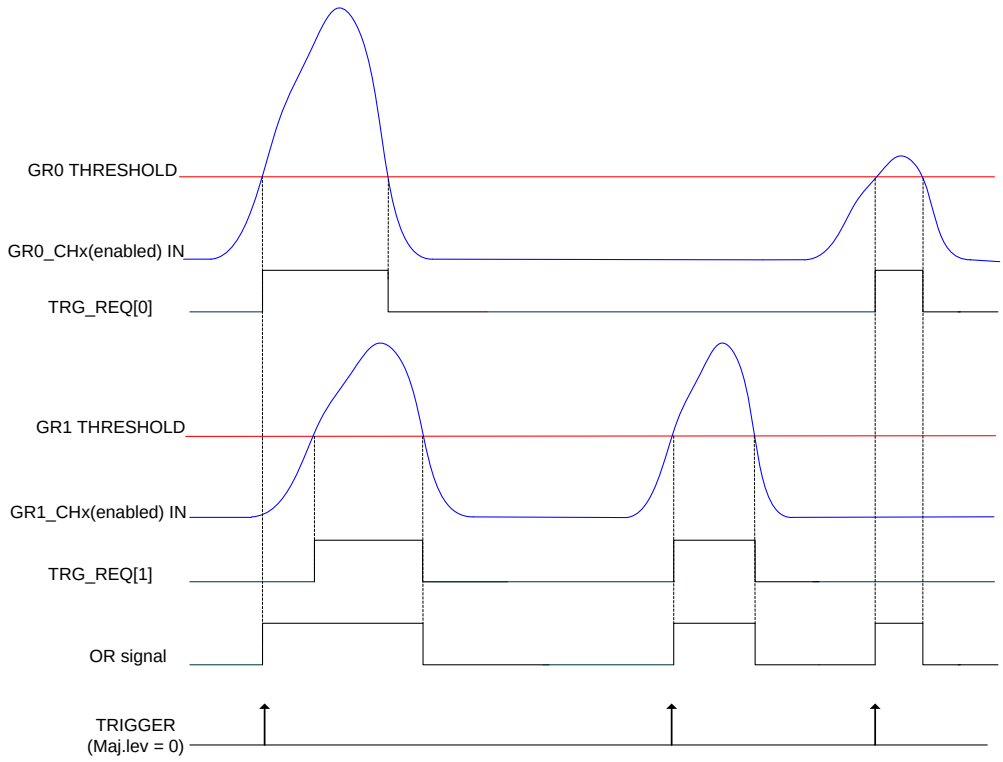


Fig. 3.7: Trigger requests relationship with Majority level = 0

Fig. 3.8 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0.

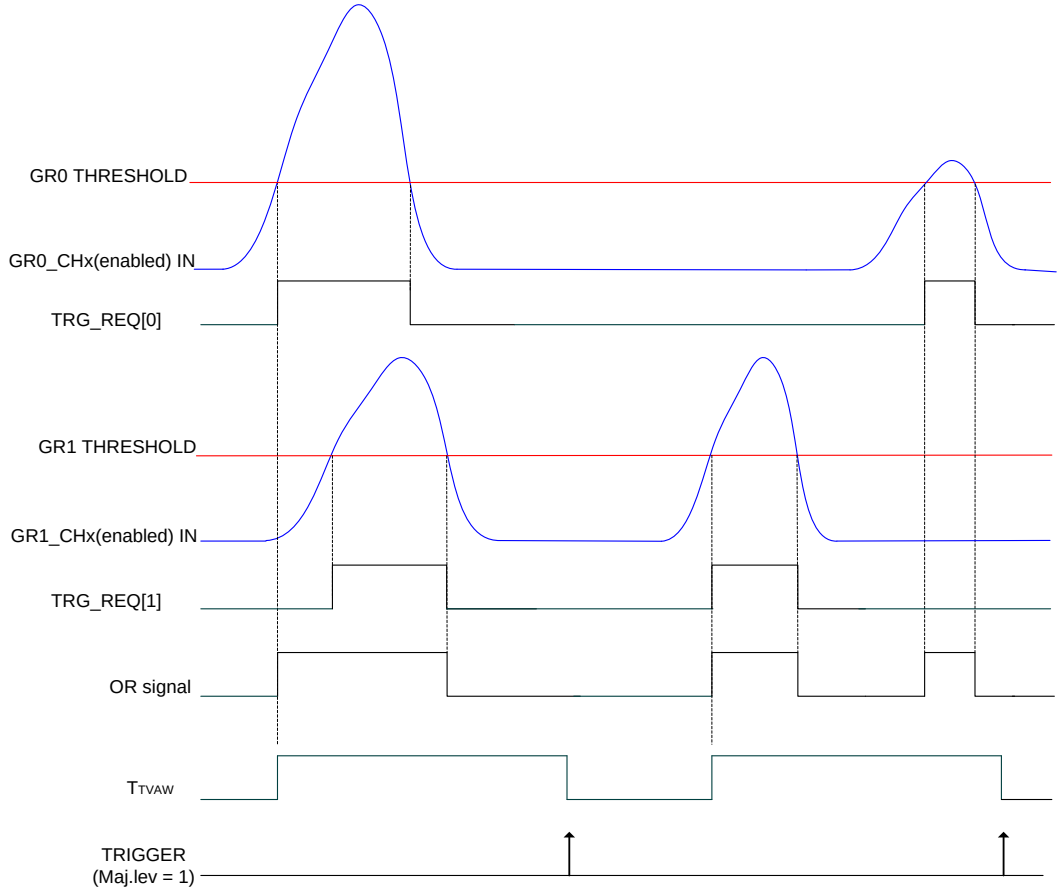


Fig. 3.8: Trigger requests relationship with Majority level = 1 and $T_{TVAW} \neq 0$

NOTE: with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

Fig. 3.9 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0.

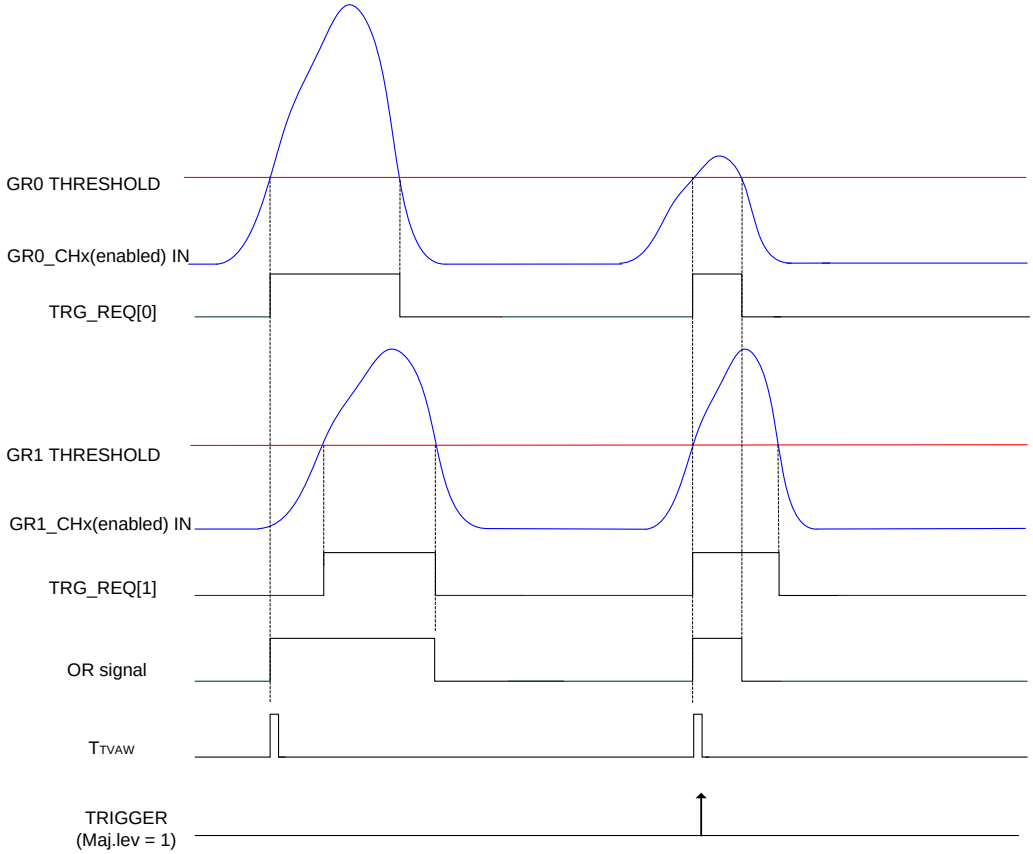


Fig. 3.9: Trigger requests relationship with Majority level = 1 and T_{TVAW} = 0

In this case, the common trigger is issued if at least two of the enabled trigger requests are instantaneously in coincidence (no T_{TVAW} is waited).

NOTE: a practical example of making coincidences with the digitizer in the standard operating is detailed in the document:

GD2817 - How to make coincidences with CAEN digitizers (web available).

3.4.6. *Trigger Distribution*

As described in § **3.4**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently provoking the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of **Fig. 3.10**).

A Trigger Out signal is also generated on the relevant front panel TRG-OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards. Thanks to its configurability, TRG-OUT can propagate out:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of **Fig. 3.10**);
- the OR, AND or MAJORITY exclusively of the trigger requests.

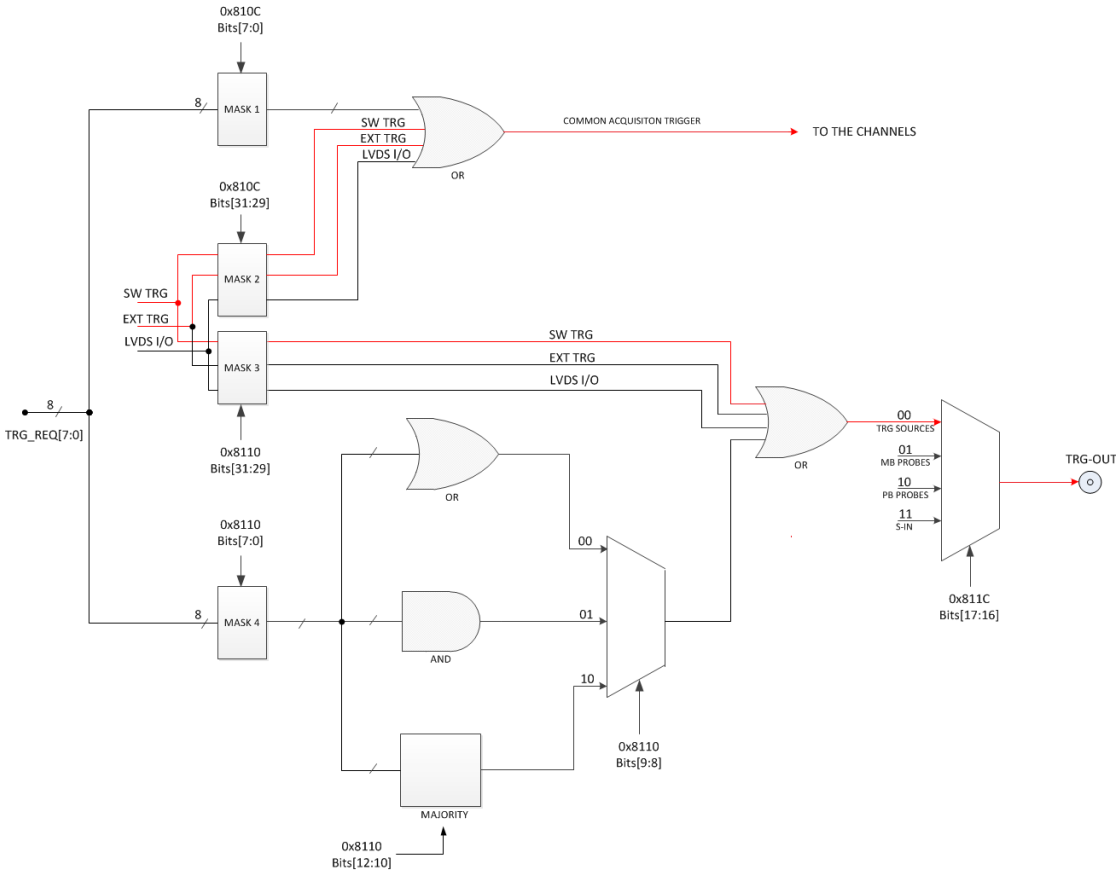


Fig. 3.10: Trigger configuration of TRG-OUT front panel connector

The registers involved in the TRG-OUT programming are:

- Register address 0x8110;
- Register address 0x811C.

3.4.6.1. Example

For instance, it could be required to start the acquisition on all the channels of a multi-board system as soon as one of the channels of a board (board "n") crosses its threshold. Trigger Out signal is then fed to an external Fan Out logic unit (e.g. CAEN V1495 board); the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to perform are following described.

1. Register 0x8110 on board "n":
   - Enable the desired trigger request as Trigger Out signal on board "n" (by bits[7:0] mask).
   - Disable Software Trigger, External Trigger and LVDS I/O Trigger as Trigger Out signal on board "n" (bits[31:29] = 000).
   - Set Trigger Out signal as the OR of the enabled trigger requests on board "n" (bits[9:8] = 00).
2. Register 0x811C on board "n":
   - Configure the digitizer to propagates on TRG-OUT the internal trigger sources according to the 0x8110 settings (i.e. the enabled trigger request, in the specific case) on board "n" (bits[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board "n"):
   - Enable External Trigger to participate in the board common acquisition trigger, disable Software Trigger, LVDS I/O Trigger and the Trigger Requests from the channels (bits[31:29] = 010; bits[7:0] = 00000000).

3.5. Multi-Board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user can acquire from N boards with Y channel each, like if they were just one board with (N * Y) channels.

The main issue in the synchronization of a multi-board system is to propagate the sampling clock among the boards. This is made through input/output daisy chain connections among the digitizers. One board has to be chosen to be the “master” board that propagates its own clock to the others. A programmable phase shift can adjust possible delays in the clock propagation. This allows to have both the same ADC sampling clock and the same time reference for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards are aligned to the same absolute time.

There are several ways to implement the trigger logic. The synchronization tool allows to propagate the trigger to all boards and acquire the events accordingly. Moreover, in case of busy state of one or more boards, the acquisition is inhibited for all boards.

For a detailed guide to multi-board synchronization, refer to the following web available Application Note:

AN2086 – Synchronization of a multi-board acquisition system with CAEN digitizers

3.6. Front Panel LVDS I/Os

The V1740 is provided with 16 general purpose programmable LVDS I/O signals (see § **2.4.4**). CAEN has developed for its VME digitizers a new and more flexible configuration management that has been introduced from the release **3.8** of the ROC FPGA firmware and allows the LVDS I/Os signals to be programmed in terms of direction (INPUT/OUTPUT) and functionality by groups of 4. Only the description of the new configuration modes is given in this paragraph.

The new management is enabled by setting to 1 the bit[8] at register address 0x811C, that is set to 0 by default.

THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES

NOTE ABOUT LVDS I/Os CONFIGURATIONS IMPLEMENTED IN ROC FW RELEASES <3.8

*THE STANDARD FIRMWARE OF V1740 MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0). USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT CAN REFER TO THE USER MANUAL OF THE RELEVANT DIGITIZER OR CAN CONTACT CAEN (see § **8**) FOR INFORMATION.*

SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS HEARTLY RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!

The direction of the signals are set by the bits[5:2] at register address 0x811C:

Bit[2] → LVDS I/O[3:0]
Bit[3] → LVDS I/O[7:4]
Bit[4] → LVDS I/O[11:8]
Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

By default, the new modes are disabled (i.e. bit[8] = 0) and the status of the LVDS I/O signals is congruent with the old Programmed I/O mode (see **Table 3.3**).

Table 3.3: Front Panel LVDS I/Os default setting

Nr.	Direction	Description
0	out	Group 0 Trigger Request
1	out	Group 1 Trigger Request
2	out	Group 2 Trigger Request
3	out	Group 3 Trigger Request
4	out	Group 4 Trigger Request
5	out	Group 5 Trigger Request
6	out	Group 6 Trigger Request
7	out	Group 7 Trigger Request
8	out	Memory Full
9	out	Event Data Ready
10	out	Channels Trigger
11	out	RUN Status
12	in	Trigger Time Tag Reset (active low)
13	in	Memory Clear (active low)
14	-	reserved
15	-	reserved

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] at register address 0x81A0):

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): OLD STYLE

Where n = 0, 4, 8, 12

NOTE: whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header's Pattern field (see § **3.3.4**); the user can then choose to readout it or not.

Table 3.4: Features description when LVDS group is configured as INPUT

	REGISTER	TRIGGER	nBUSY/nVETO	OLD STYLE
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: *reserved* 14: *reserved* 13: *reserved* 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: *reserved* 10: *reserved* 9: *reserved* 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: *reserved* 6: *reserved* 5: *reserved* 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: *reserved* 2: *reserved* 1: *reserved* 0: nClear_TTT

Table 3.5: Features description when LVDS group is configured as OUTPUT

	REGISTER	TRIGGER	nBUSY/nVETO	OLD STYLE
LVDS OUT [15:12]	Reg[15:12]	TrigOut_Gr[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS OUT [11:8]	Reg[11:8]	TrigOut_Gr[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS OUT [7:4]	Reg[7:4]	TrigOut_Gr[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS OUT [3:0]	Reg[3:0]	TrigOut_Gr[3:0]	3: nRun 2: nTrigger 1: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

3.6.1. Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read at register address 0x8118.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written at register address 0x8118

3.6.2. Mode 1: TRIGGER

Direction is INPUT: *Not available*.

Direction is OUTPUT: the TrgOut_Gr[(n+3):n] signals (n = 0, 4) are the trigger requests coming directly from the mezzanines, where a trigger request is defined in § **3.4.3**.

3.6.3. Mode 2: nBUSY/nVETO

3.6.3.1. nBusy Signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the nBusy signal (OUTPUT) as below.

The **Busy** signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR (**LVDS_BusyIn** AND **BusyIn_enable**)

where

- Almost_Full indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set at register address 0x816C;
- LVDS_BusyIn is available in nBUSY/nVETO configuration (see **Table 3.4**);
- BusyIn_enable is set at address 0x8100, bit[8].

3.6.3.2. nVETO Signal

Direction is INPUT: nVETOIn is an active low signal which, if enabled (register address 0x8100, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

Direction is OUTPUT: the nVETO signal is the copy of nVETOIn.

3.6.3.3. nTrigger Signal

Direction is INPUT: nTriggerIn is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: nTrigger signal can be either the copy of the trigger signal propagated to the TRG-OUT LEMO connector or the copy of the acquisition common trigger. This is selected by bit[16] of the 0x81A0 register.

3.6.3.4. nRun Signal

Direction is INPUT: nRunIn is an active low signal which can be used as Start for the digitizer (i.e. *Acquisition Control* register, address 0x8100, bits[1:0] = 11). It is possible to program the start on the level or on the edge of the nRunIn signal (*Acquisition Control* register, bit[11]).

Direction is OUTPUT: nRun signal is the inverse of the internal Run of the board.

3.6.4. Mode 3: LEGACY

Legacy mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than **3.8**.

3.6.4.1. nClear_TTT Signal

It is the only signal available as INPUT. It is the Trigger Time Tag (TTT) reset, like in the old configuration.

3.6.4.2. Busy Signal

The Busy signal is active high and it is exactly the inverse of the nBusy signal (see § **3.6.4.2**).
In case the *Memory Buffer Almost Full Level* register is set to 0x0 and the BusyIn signal is disabled, the Busy is the FULL signal present in the old configuration.

3.6.4.3. DataReady Signal

The DataReady is an active high signal indicating that the board has data available for readout (the same as the DataReady front panel LED does).

3.6.4.4. Trigger Signal

The active high Trigger signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector; see § **3.6.3.3**).

3.6.4.5. Run Signal

The Run signal is active high and represents the inverse of the nRun signal (see § **3.6.3.4**).

3.7. Analog Monitor

V1740 houses a 12-bit (100MHz) DAC with 0÷1 V dynamics on a 50 Ω load, whose input is controlled by the ROC FPGA, and the signal output (driving 50 Ω) is available on the MON/Σ output connector (see Errore. L'origine riferimento non è stata trovata. and § **2.4**). MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements four operating modes according to the value of bits[2:0] at register address 0x8144:

- Trigger Majority Mode (*Monitor Mode* = 000)
- Test Mode (Monitor Mode = 001)
- Buffer Occupancy Mode (*Monitor Mode* = 011)
- Voltage Level Mode (*Monitor Mode* = 100)

Note: *Monitor Mode* = 010 is reserved for future implementation.

3.7.1. Trigger Majority Mode (Monitor Mode = 000)

It is possible to generate a Majority signal with the DAC: the MON output provides a voltage signal whose amplitude is proportional to the number of "triggering groups" (the groups enabled to generate the trigger request where at least one of the enabled channels in the group has exceeded the programmed threshold); 1 step = 1.25mV. This allows, via an external discriminator, to produce a common trigger signal, as the resulting "majority" has exceeded a particular threshold.

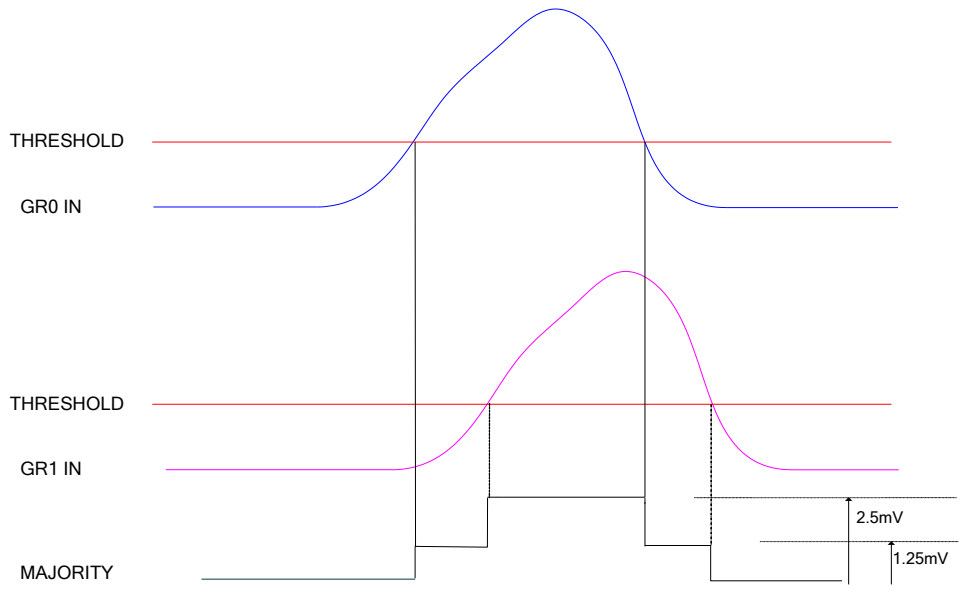


Fig. 3.11: Majority logic (2 triggering groups; "polarity" bit[6] =0 at register address 0x8000)

3.7.2. Test Mode (Monitor Mode = 001)

In this mode, the MON output provides a saw-tooth signal with 1-V amplitude and 30.518-Hz frequency.

3.7.3. Buffer Occupancy Mode (Monitor Mode = 011)

In this mode, MON output connector provides a voltage value increasing, proportionally with the number of buffers filled with events, in fixed steps of 0.976 mV given by:

$$\frac{V_{max}}{Maximum\_Number\_of\_Buffers}$$

where V_{max} ~ 1 V and *Maximum_Number_of_Buffers* = 1024 (i.e. the value of the register address 0x800C, as introduced in § **3.3.3**).

Example: if 0x800C = 0x4 (i.e. 16 buffers), the maximum Buffer Occupancy output voltage level is given by 0.976 mV * 2^4.

This mode allows to test the readout efficiency: in fact, if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

Starting from revision **4.9** of the ROC FPGA (motherboard firmware), it is possible to apply a digital gain to the fixed step, particularly when the memory is organized in a small number of buffers. The gain can be set as powers of two ranging between 2^0 = 1 (no gain, which is the default setting) and 2^A, where the exponent is the value to write at register address 0x81B4.

3.7.4. Voltage Level Mode (Monitor Mode = 100)

In this mode, MON out provides a voltage value programmable via the 12-bit 'N' parameter written in the *Set Monitor DAC* register, with: V_{mon} = 1/4096*N (Volt).

3.8. Test Pattern Generator

The AMC FPGA can emulate the ADC and write into memory a ramp (0, 1, 2, 3,…3FFF, 3FFF, 3FFE.., 0) for test purposes. It can be enabled via *Channel Configuration* register.

3.9. Reset, Clear and Default Configuration

3.9.1. Global Reset

Global Reset is performed at Power-On of the module or via software by write access at register address 0xEF24 (whatever 32-bit value can be written). It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

3.9.2. Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via either a write access at register address 0xEF28 (whatever 32-bit value can be written). In the old LVDS I/O configuration, it is also possible to perform a memory clear by sending a pulse to the front panel dedicated Memory Clear input (see **Table 3.3**).

3.9.3. Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent either to the LVDS I/O dedicated input (see **Table 3.3** and § **3.6.4.1**) or to the S-IN input (leading edge sensitive).

3.10. VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

3.10.1. Addressing capabilities

3.10.1.1. Base Address

The module works in A24/A32 mode. The Base Address of the module can be set through four rotary switches (see § **2.6**) and is written into a word of 24 or 32 bit; then, it is validated only with either a Power-ON cycle or a System Reset (see § **3.9.1**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

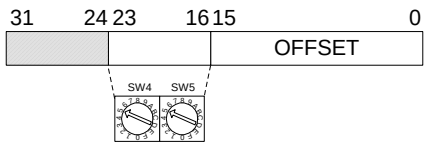


Fig. 3.12: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x000000:0xFF0000]	-

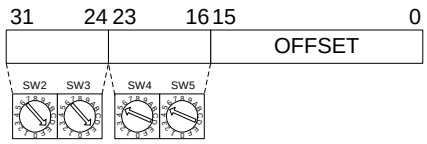


Fig. 3.13: A32 addressing

3.10.1.2. CR/CSR Address

GEO address is picked up from relevant backplane lines and written onto bits 23:19 of CR/CSR space, indicating the slot number in the crate; the recognized Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160pin connectors*.

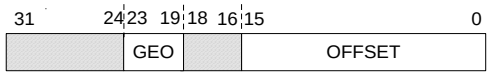


Fig. 3.14: CR/CSR addressing

3.10.1.3. Address Relocation

Register address 0xEF10 (bits[15:0]) allows to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via register address 0xEF00 (bit[6]).

The used addresses are:

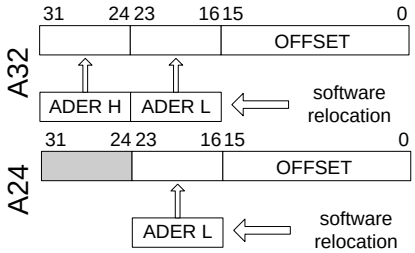


Fig. 3.15: Software relocation of base address

3.11. Data Transfer Capabilities and Event Readout

V1740 feature a multi-event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in § **3.3.3**. Once they are written in the memory, the events become available for readout via VMEbus or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers. The acquisition process is so "dead timeless" until the memory becomes full (see § **3.3.5**).
data transfer starts from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group (from 0 to 7) begins
The events are readout sequentially and completely, starting from the header of the first available event, followed by the samples from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group begins (until Group 7). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to partially readout an event.
The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C, as well as on the number of enabled channels.
The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

3.11.1. Single D32 Transfer

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § **3.3.4**.
It is suggested, after the 1st word is transferred, to check the Event Size information and then do as many D32 cycles as necessary (actually Event Size -1) in order to completely read the event.

3.11.2. Block Transfer D32/D64, 2eVME

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library (see § **4.2**).

The event is configurable as indicated in § **3.11**, namely:

[Event Size] = [8*(Block Size)] + [16 bytes]

Smaller event size can be achieved via Custom Size setting.
Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.
It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in **Fig. 3.16**).

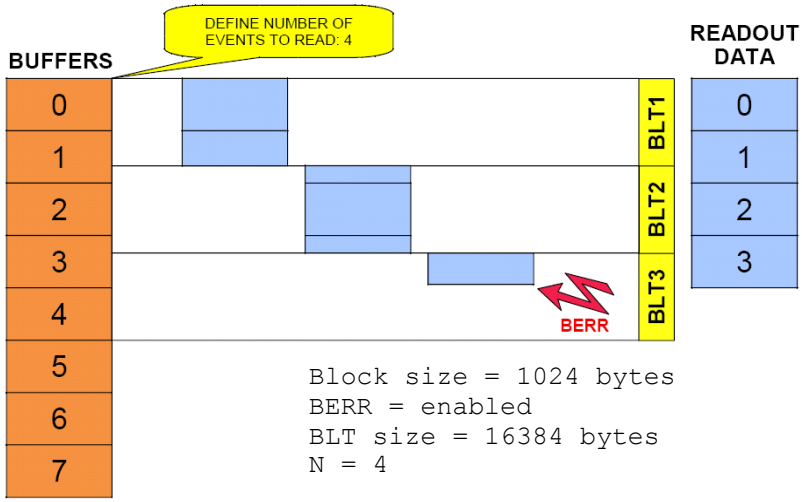


Fig. 3.16: Example of BLT readout

Since some 64 bit CPU cut off the last 32-bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit (bit[5]) at register address 0xEF00.

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64-bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

3.11.3. Chained Block Transfer D32/D64

The V1740 allows to readout events from multiple boards in Daisy chain (Chained Block Transfer mode).
The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.
Several contiguous boards, in order to be Daisy chained, must be configured as “first”, “intermediate” or “last” via register address 0xEF0C. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.
If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

3.12. Optical Link Access

The board houses a Daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s; therefore it is possible to connect up to eight V1740 to a single Optical Link Controller by using the A2818 PCI card or up to thirty-two V1740 with the A3818 PCIe card.
Detailed information on CAEN PCI/PCIe Controllers can be find at www.caen.it:

Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controller

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc.); wrong parameter settings cause a Bus Error.

Bit[3] at register address 0xEF00 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level (see § **4.2**)

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously

4. Drivers & Libraries

4.1. Drivers

In order to interface with V1740 digitizer, CAEN provides the drivers for all the different types of physical communication channels featured by the board and compliant with Windows and Linux OS:

- **CONET Optical** Link, managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the "Software/Firmware" area at the A2818 or A3818 page (**login required**).

NOTE: For the installation of the Optical Link driver, refer to the User Manual of the specific Controller.

- **USB 2.0 Drivers** are managed by the V1718 USB-to-VME Bridge. The driver installation package is available on CAEN website in the "Software/Firmware" area at the V1718 page (**login required**).

NOTE: For the installation of the USB driver, refer to the User Manual of the V1718 Bridge.

4.2. Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason**, the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

The CAENDigitizer installation package and relevant documentation are available on CAEN website in the 'Download' area at the CAENDigitizer Library page.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.

The CAENComm installation package, the relevant documentation and the link to the required CAENVMELib, are available on CAEN website in the 'Download' area at the CAENComm Library page.

CAENComm (and so the CAENDigitizer) supports the following communication channels:

PC → USB (V1718) → VMEbus → V1740
PC → PCI/PCIe (A2818/A3818) → CONET → V1740
PC → PCI/PCIe (A2818/A3818) → CONET (V2718) → VMEbus → V1740

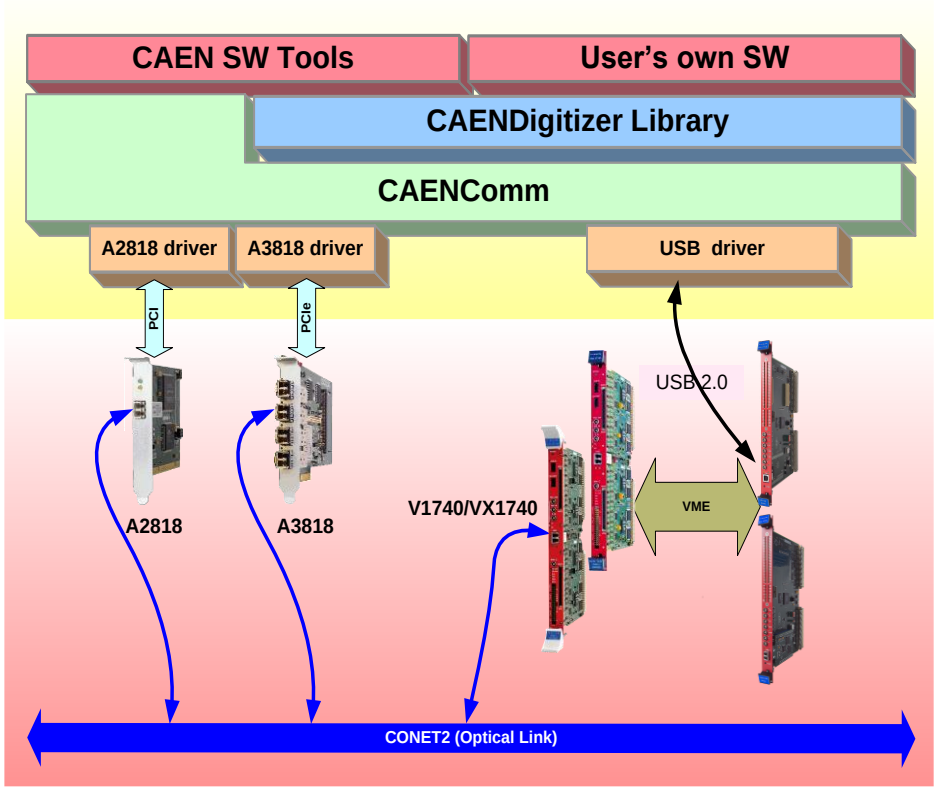


Fig. 4.1: Block diagram of the software layers

5. Software Tools

CAEN provides software tools to interface the V1740, which are available for free download on www.caen.it at:

Home / Products / Firmware/Software / Digitizer Software

5.1. CAENUpgrader

CAENUpgrader is a free software composed of command line tools together with a Java Graphical User Interface.

Specifically for the V1740, CAENUpgrader allows in few easy steps to:

- Upload different FPGA firmware versions on the board
- Read the firmware release of the board and the bridge (when used)
- Manage the firmware license, in case of pay firmware (DPP-QDC)
- Upgrade the internal PLL
- Generate a programming file to configure the internal PLL
- Get the Board Info file, useful in case of support

CAENUpgrader can operate with Windows and Linux, 32 and 64-bit OSs.

The program relies on the CAENComm and CAENVMELib libraries (see § **4.2**) and requires third-party Java SE 8 u40 (or later) to be installed.

NOTE: Windows version of CAENUpgrader is stand-alone (i.e. only the communication driver needs to be installed apart by the user, while the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be installed apart by the user.

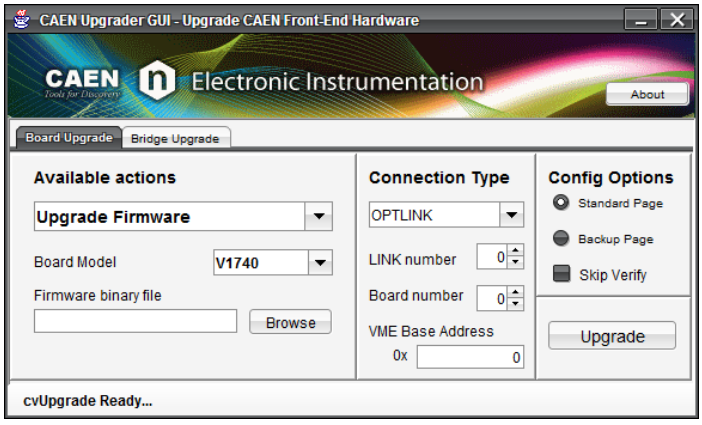


Fig. 5.1: CAENUpgrader Graphical User Interface

CAENUpgrader installation package can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader

The reference document for installation instructions and program detailed description is downloadable at the same page above, in the Documentation tab.

5.2. CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java and LabVIEW GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

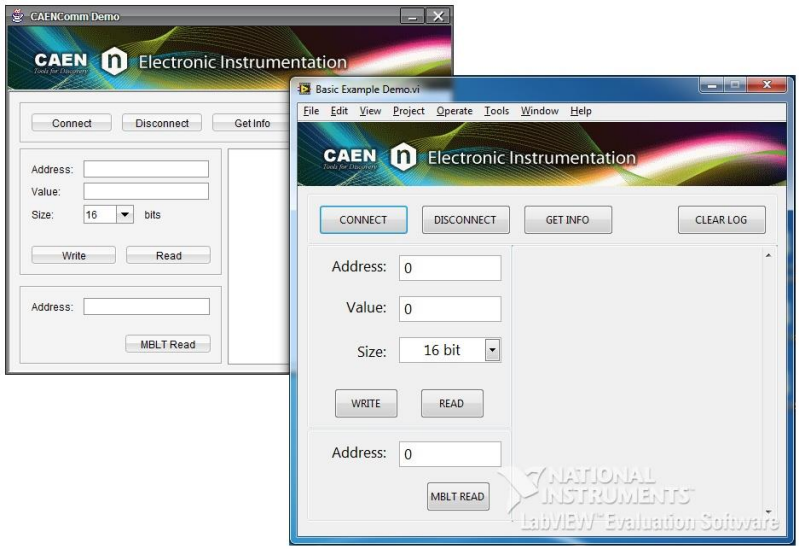


Fig. 5.2: CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo can operate with Windows OS, 32 and 64-bit. It requires CAENComm and CAEVMElib libraries as additional software to be installed (see § **4.2**).

The Demo is included in the CAENComm library Windows installation package, which can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library

5.3. CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the default firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: www.gnuplot.info).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own

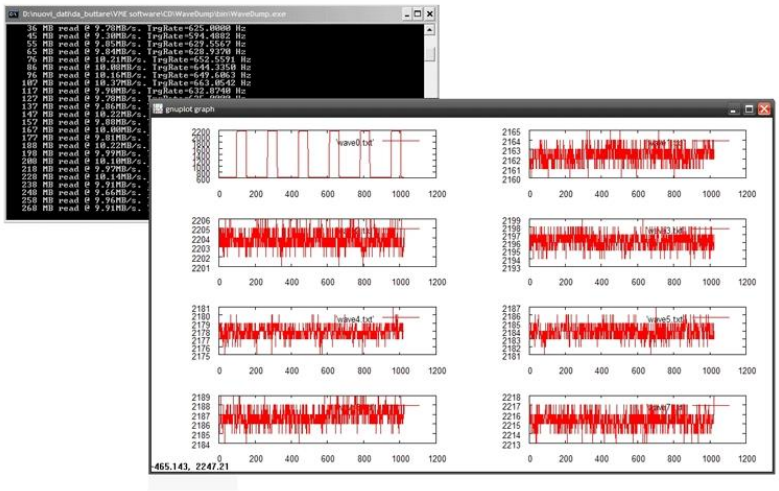


Fig. 5.3: CAEN WaveDump

CAEN WaveDump can operate with Windows and Linux OS, 32 and 64-bit.

The program relies on the CAENDigitizer, CAENComm and CAENVMELib libraries (see § **4.2**). Linux users are required to install the third-party Gnuplot.

NOTE: Windows version of WaveDump is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be installed apart by the user.

Installation packages and documentation can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Readout Software / CAEN WaveDump

5.4. DPP-QDC Demo Software

DPP-QDC Demo Software is a is C demo application that manages the communication and the data acquisition from 740D digitizer series running the DPP-QDC firmware. It is possible to set the communication parameters and DPP settings. Waveforms and histograms can also be plotted in real time for one channel at a time, and both waveforms and lists of time stamp and energy can be saved. DPP-QDC Demo Software is provided including C source files for developers

DPP-QDC Demo Software can operates with Windows OS, 32 and 64-bit.

Installation packages and documentation can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / DPP-QDC

6. HW Installation

- The V1740 fits into 6U VME crates.
- **The V1740 cannot be operated with CAEN crates VME8001/8002/8004/8004A.**
- VX1740 versions require VME64X compliant crates.
- Use only crates with forced cooling air flow.
- Turn the crate OFF before board insertion/removal.
- Remove all cables connected to the front panel before board insertion/removal.

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

V1740/VX1740 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004/8004A!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

6.1. Power-On Sequence

To power on the board, follow the steps below:

1. insert the V1740 board into the crate;
2. power up the crate.

6.2. Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration.

After power-on, only the NIM and PLL LOCK front panel LEDs must light on.

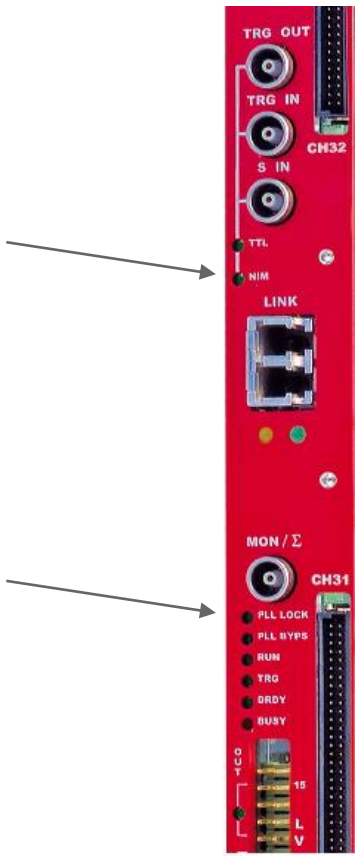


Fig. 6.1: Front panel LEDs status at power on

7. Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs on each mezzanine (i.e. one FPGA per 16 channels or two 8-channel groups). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA or MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA or MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

x740D versions mount a bigger channel FPGA.

x740D AMC FPGA or MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C40

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of default firmware, the board is usually factory equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one by default in normal operating. An on-board dedicated SW1 dip switch, set on STD position by default, allows to select the first FLASH page to be read at power-on (see § **2.6**).

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENUpgrader software (see § **5.1**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA VMEbus OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

7.1. Default Firmware Upgrade

The V1740 is delivered running a default firmware to operate the board for waveform recording.

The default firmware updates are available for download on CAEN website (www.caen.it) in the *Software/Firmware* tab at the V1740/VX1740/V1740D/VX1740D web pages (**login required**):

Home / Products / Modular Pulse Processing Electronics / VME / Digitizers / <Digitizer Model>

7.1.1. Default Firmware File Description

The extension of the programming default firmware file is CFA (CAEN Firmware Archive), which is a sort of archive format file aggregating all the default firmware files compatible with the same family of digitizers.

CFA and its name follows this general scheme:

x740_revX.Y_W.Z.CFA

where:

- x740 are all the boards supported by the file: DT5740, DT5740C, DT5740D, N6740, N6740C, N6740D, V1740, V1740A, V1740B, V1740C, V1740D, VX1740, VX1740A, VX1740B, VX1740C, VX1740D;
- X.Y is the major (X) and minor (Y) revision number of the mainboard FPGA;
- W.Z is the major (W) and minor (Z) revision number of the channel FPGA.

7.2. DPP Firmware Upgrade

CAEN can provides special DPP-QDC firmware for Physics Applications supported only by x740D versions. The digitizer running DPP-QDC firmware becomes a Gated Integrator receiving signals directly from the detector (no charge preamp required).

The DPP-QDC firmware updates are available for download on CAEN website in the Download tab (**login required**) at:

Home / Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / DPP-QDC

7.2.1. DPP Firmware File Description

The extension of the programming DPP firmware file is CFA (CAEN Firmware Archive), which is a sort of archive format file aggregating all the firmware files compatible with the same DPP firmware and family of digitizers.

CFA and its name follows this general scheme:

x740D_DPP-QDC_rev_X.Y_135.Z.CFA

where the major revision number of the channel FPGA is fixed for the specific DPP algorithm and digitizer family ("135" for DPP-QDC and 740D). The other fields have the same meaning as in the default firmware file description (see § **7.1.1**).

NOTE: DPP special firmware is a pay firmware requiring a license to be purchased. If not licensed, the firmware will run fully functional but with a time limitation per power cycle (30 minutes). Details on the license ordering procedure can be found in CAENUpgrader Quick Start Guide (see § **5.1**).

NOTE: if the x740D module is ordered together with a DPP-QDC firmware license, the customer will be delivered with the digitizer already running the licensed (i.e. unlocked) special firmware.

NOTE: once unlocked, upgrading the same kind of DPP firmware requires no further licensing.

7.3. Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system automatically programs the board from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

BECAUSE OF AN UPGRADE FAILURE, THE SW1 DIP SWITCH POSITION MAY NOT CORRESPOND TO THE FLASH PAGE FIRMWARE COPY LOADED ON THE BOARD FPGAs

NOTE THAT old versions of the digitizer motherboard (bit[7:0] = 0x00 at register address 0xF050) have a slightly different FLASH management. At power-on, the microcontroller loads exactly the firmware copy from the FLASH page selected through the SW1 dip switch (e.g. STD by default).

In this case, when a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the V1740, the user can perform the following recovering procedure as first attempt:

- Force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, power off the crate, switch the dedicated SW1 switch to BKP position and power on the crate.

- Use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is possible now to communicate again with the board.

- Use CAENUpgrader to load again the firmware on the STD page, then power-cycle in order the board to get operative again.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see § **8**).

8. Technical Support

CAEN support services are available for the user by accessing the *Support & Services* area on CAEN website at www.caen.it.

8.1. Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the *Returns and Repairs* area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.
Contacts for shipping are reported on the website at *Home / Contacts*.

8.2. Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)