CAEN
Tools for Discovery

Electronic Instrumentation

User Manual UM2749

N6743

8 Channel 12bit 3.2 GS/s Switched Capacitor Digitizer

Rev.1 - February 9th, 2016

Purpose of this Manual

This document contains the full hardware description and the principle of operating of the N6743 Digitizer.
For any detail on the library functions mentioned in the document, please consult [RD4].

Change Document Record

Date	Revision	Changes
January 12th, 2015	00	Initial release
February 9th 2016	01	Fully revised. Added Sec. **Digital Memory Buffer**, Sec. **BUSY Front Panel LED**, Sec. **Majority Level**, Sec. **Veto Gate for the Trigger Rate Counter**, Sec. **Timer Reset**, Sec. **Troubleshooting**

Symbols, abbreviated terms and notation

DLL	Delay Line Loop
INL	Integral Non-Linearity
PLL	Phase-Locked Loop
TDC	Time to Digital Converter
USB	Universal Serial Bus

Reference Documents

[RD1] GD2512 – CAENUpgrader QuickStart Guide

[RD2] GD2783 – First Installation Guide to Desktop Digitizers & MCA

[RD3] GD2812 – DeskBoot QuickStart Guide

[RD4] UM1935 - CAENDigitizer User & Reference Manual

[RD5] UM1934 - CAENComm User & Reference Manual

[RD6] UM2754 - WaveCatcher User Manual

All documents can be downloaded at: http://www.caen.it/csite/LibrarySearch.jsp

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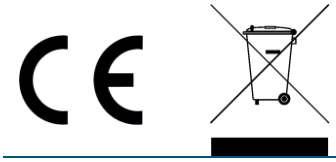

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Safety Notices

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1 Introduction

The Mod. N6743 is a NIM module housing a 8-channel 12-bit 3.2 GS/s Switched Capacitor Digitizer issued from the collaboration with CEA/IRFU & CNRS/IN2P3/LAL and based on the SAMLONG chip.

The input dynamic range is 2.5 V_{pp} (DC coupled) on single ended MCX coaxial connectors. The DC offset is adjustable in the ±1.25V range via a 16-bit DAC on each channel (see Sec. **Analog Input Stage**).

Considering the sampling frequency and the number of bits, it is well suited for very fast signals as the ones generated by fast scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others.

The analog input signals are continuously sampled inside the SAMLONG chips in a circular analog memory buffer (1024 cells) at the default sampling frequency of 3.2 GS/s (312.5 ps of sampling period); frequencies of 1.6 GS/s, 0.8 and 0.4 GS/s are also software selectable. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits into a digital memory buffer with independent read and write access. Channel digital memory with software selectable buffer organization depending on the event size allows for up to 7 full events per channel (1 event = 1024 * 12 bits) consecutively storable.

Each input channel is equipped with a discriminator with a 16-bit programmable threshold, which generates trigger requests. Requests from all channels are processed by the board to generate a global trigger causing all the channels to acquire an event simultaneously. The global trigger can also be provided externally by software command, or by the front panel TRG-IN input connector, or by any combination of the channel discriminators and/or the TRG-IN.

During analog to digital conversion process, the N6743 cannot handle other triggers, thus generating a Dead Time (maximum 125 µs, decreasing proportionally with the configurable recording depth).

Each input channel is equipped with a hit rate monitor based on its own discriminator and on two counters giving the number of hits which cross the programmed discriminator threshold (also during the Dead Time) and the time elapsed with a 1 MHz clock (see Sec. **Hit Rate Monitor**). This permits among others measuring the hit rate with respect to the signal amplitude.

Each input channel is equipped with a digital programmable charge integrator which permits a high rate measurement in charge mode (see Sec. **Running in Charge Mode**).

Each pair of channels is equipped with a 40-bit TDC (counter) tagging the trigger with the clock delivered to the SAMLONG chips (200 MHz down to 25 MHz depending on the selected sampling frequency).

N6743 houses a fixed amplitude pulser on each analog input, which permits an easy complete functionality test and the use of the module in reflectometer mode (see Sec. **Test Pattern Pulser**).

The module features front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references.

N6743 houses USB 2.0 and Optical Link interfaces. USB 2.0 allows data transfers up to 30 MB/s. The Optical Link supports transfer rate of 80 MB/s and offers Daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller, or up to 32 using a A3818 (4-link version). Optical Link and USB accesses are internally arbitrated.

Board Models	Description	Product Code
N6743	N6743 - 8 Channel 12bit 3.2 GS/s Switched Capacitor Digitizer	WN6743XAAAA
Related Products	**Description**	**Product Code**
A2818	A2818 – PCI Optical Link (Rhos compliant)	WA2818XAAAAA
A3818A	A3818A – PCIe 1 Optical Link	WA3818AXAAAA
A3818B	A3818B – PCIe 2 Optical Link	WA3818BXAAAA
A3818C	A3818C – PCIe 4 Optical Link	WA3818CXAAAA
Accessories	**Description**	**Product Code**
A318	SE to Differential Clock Cable Adapter	WA318XAAAAAA
A654	Single Channel MCX to LEMO Cable Adapter	WA654XAAAAAA
A654 KIT4	4 MCX TO LEMO Cable Adapter	WA654K4AAAAA
A654 KIT8	8 MCX TO LEMO Cable Adapter	WA654K8AAAAA
A659	A659 - Single Channel MCX to BNC Cable Adapter	WA659XAAAAAA
A659 KIT4	4 MCX TO BNC Cable Adapter	WA659K4AAAAA
A659 KIT8	8 MCX TO BNC Cable Adapter	WA659K8AAAAA
AI2730	Optical Fibre 30 m simplex	WAI2730XAAAA
AI2720	Optical Fibre 20 m simplex	WAI2720XAAAA
AI2705	Optical Fibre 5 m simplex	WAI2705XAAAA
AI2703	Optical Fibre 30 cm simplex	WAI2703XAAAA
AY2730	Optical Fibre 30 m duplex	WAY2730XAAAA
AY2720	Optical Fibre 20 m duplex	WAY2720XAAAA
AY2705	Optical Fibre 5 m duplex	WAY2705XAAAA

Tab. 1.1: Table of models and related items

2 Block Diagram

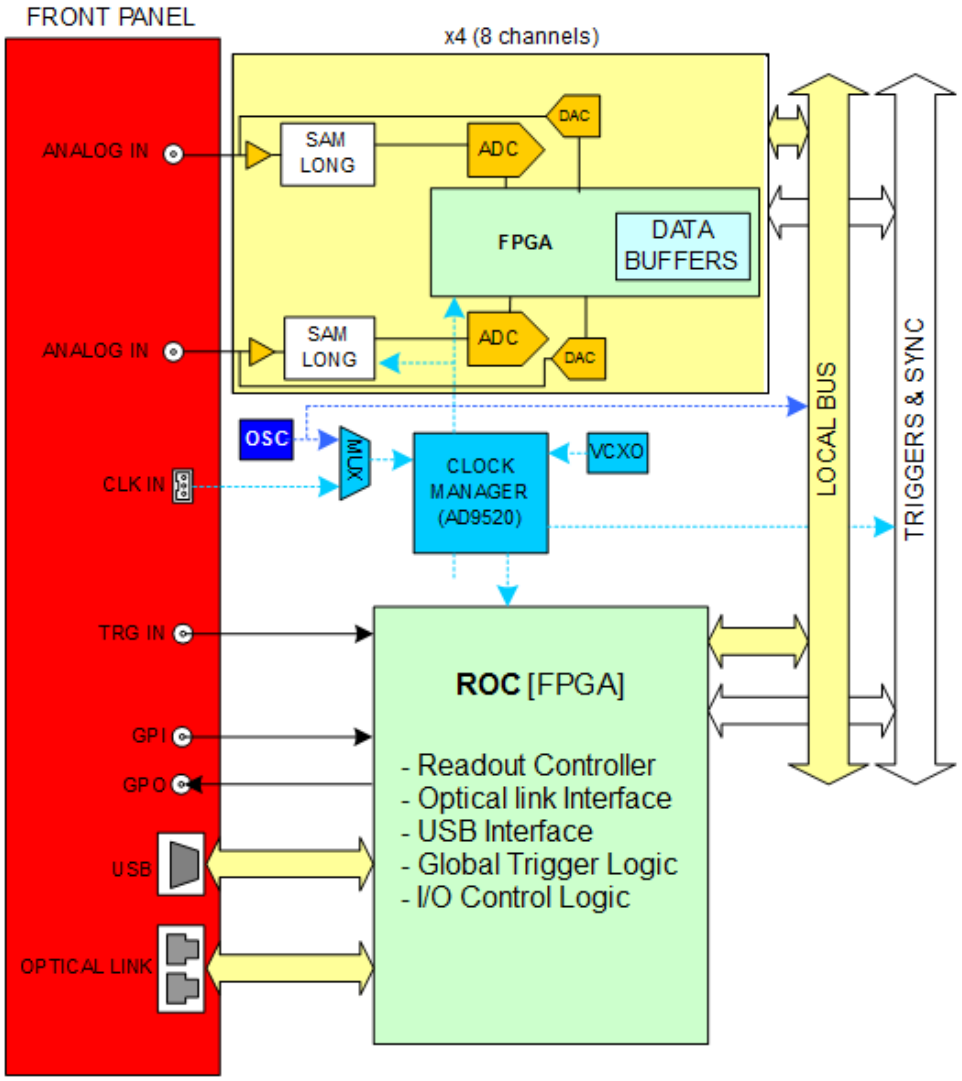

Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor** 1-unit wide NIM module		
ANALOG INPUT	**Channels** 8 channels Single ended **Impedance** Z_{in}: 50 Ω	**Connector** MCX **Full Scale Range** 2.5 V_{pp} DC coupled	**Bandwidth** 500 MHz **Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ±1.25 V
TEST FUNCTIONALITY	One pulser per channel with programmable 16-bit pattern (fixed amplitude)		
DIGITAL CONVERSION	**Analog Memory (Switched Capacitor Array)** SAMLONG Fast Analog Memory chip 2 channels, 1024 storage cells/ch 320 ns minimum recorded time/event **Sampling Rate** 3.2/1.6 /0.8/0.4 GS/s SW selectable	**Dead Time (Event A/D Conversion)** 125 µs (max. @ 1024 samples) **Note:** value decreasing proportionally with the recording depth (configurable record length) **Resolution** 12 bits	
TIMING RESOLUTION	< 20 ps RMS before time calibration < 8 ns RMS (5 ps RMS typical) after time calibration **Note:** obtained with factory calibration and dual-pulse timing measurement with pulse generator. (improved applying the recommended proper cooling) Test conditions: periodic input pulses with 1V Amplitude, 1kHz Frequency, rise time of 0.8 / 1.6 / 2.5 ns. The resolution does not change significantly when varying the delay Δt between the two pulses. **Note:** it is recommended to provide proper cooling to improve the resolution performances.		
NOISE LEVEL	0.75 mV RMS		
CLOCK GENERATION	Synchronization clock source: internal/external On-board PLL provides generation of the main board clocks from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available) Jitter<100ppm requested	**TRG-IN (LEMO)** External trigger or Start/Stop acquisition digital input: NIM/TTL, Z_{in} = 50 Ω	
	GPI (LEMO) Trigger Time Stamp reset or Start/stop acquisition digital input: NIM/TTL, Z_{in} = 50 Ω	**GPO (LEMO)** Common trigger digital output: NIM/TTL, R_t = 50 Ω	
DIGITAL MEMORY	7 event/ch Multi-Event Buffer (1024 samples per event)		
TRIGGER	**Trigger Source** • *Self-trigger*: channel over/under threshold (based on analog discriminator on each channel with DAC adjusted threshold) for common trigger generation • *External-trigger*: common trigger by TRG-IN connector • *Software-trigger:* common trigger by software command	**Trigger Propagation** GPO programmable digital output **Trigger Time Stamp** 40-bit counter, 5-ns resolution, 83-min range Timer reset by GPI input connector **Trigger Threshold** Programmable through a 16-bit DAC in the range of ±1.25 V on each channel	
ADC & MEM. CONTROLLER	Altera Cyclone EP3C16 (1 FPGA serves 4 channels)		
COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod.A2818/A3818)	**USB** USB 2.0 compliant Up to 30 MB/s transfer rate	
DIGITAL PULSE PROCESSING	Software selectable embedded Charge Mode for input pulse high rate charge integration and fast histogramming		
FIRMWARE UPGRADE	Firmware can be upgraded via USB/Optical Link		
SOFTWARE	General purpose C libraries and configuration tools (Windows® and Linux® support); WaveCatcher readout software (Windows® only)		
POWER CONSUMPTIONS	2.9 A @ +6V; 500 mA @ -6 V		

Tab. 3.1: Specifications table

4 Packaging and Compliancy

The module is housed in a single-width NIM unit.

Fig. 4.1: Front view

Fig. 4.2: Side view

CAUTION: to manage the product, consult the operating instructions provided.

A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!

CAUTION: this product needs proper cooling.

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CAUTION: this product needs proper handling.

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CAEN provides the specific document "Precautions for Handling, Storage and Installation" available in the documentation tab of the product web page that the user is mandatory to read before to operate with CAEN equipment.

5 Power Requirements

The table below resumes the N6743 power consumptions per relevant power supply rail.

SUPPLY VOLTAGE	
+6V	-6V
2.9 A	500 mA

Tab. 5.1: Power requirements table

6 Panels Description

Fig. 6.1: Front panel view

Front Panel

ANALOG INPUT

FUNCTION

Input connectors (CH0 to CH7) receiving the input analog signals.

ELECTRICAL SPECS

Sign. type: single ended.

Input dynamics: 2.5 V_{pp}.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: MCX connectors.

Type: CS 85MCX-50-0-16.

Manufacturer: SUHNER.

Suggested plug: MCX-50-2-16 type.

Suggested cable: RG174 type.

CLK IN

FUNCTION

Input for the external clock.

ELECTRICAL SPECS

Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML).

Coupling: AC.

Z_{diff}: 100 Ω.

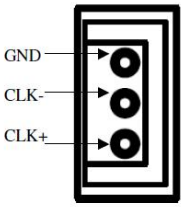
MECHANICAL SPECS

Series: AMPMODU connectors.

Type: 3-102203-4 (3-pin).

Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

GPO

FUNCTION

General purpose digital output. Configurable for Common Trigger propagation.

ELECTRICAL SPECS

Signal level: NIM or TTL.

Requires 50 Ω termination.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

TRG IN

FUNCTION

Digital input connector for external trigger signal or as Start/Stop acquisition (see Sec. **Acquisition Run/Stop**).

ELECTRICAL SPECS

Signal level: NIM or TTL.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

GPI

FUNCTION

General purpose digital input. Configurable as reset of the time stamps (see Sec. **Timer Reset**) or Start/Stop acquisition (see Sec. **Timer Reset**).

ELECTRICAL SPECS

Signal level: NIM or TTL.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

OPTICAL LINK PORT

FUNCTION

Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS

Transfer rate: up to 80 MB/s

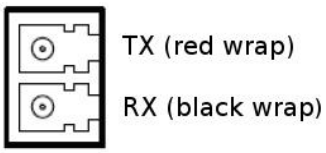
MECHANICAL SPECS

Series: SFF Transceivers

Type: FTLF8519F-2KNL (LC connectors)

Manufacturer: FINISAR

PINOUT



LINK LEDs (GREEN/YELLOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

USB PORT

FUNCTION

USB connector for data readout and flow control.

ELECTRICAL SPECS

Standard: compliant to USB 2.0 and USB 1.0.

Transfer rate: up to 30 MB/s.

MECHANICAL SPECS

Series: USB connectors.

Type: 787780-2 (B-Type).

Manufacturer: AMP Inc.

USB LINK LED (GREEN): indicates the USB communication is active.

DIAGNOSTICS LEDs

TTL (GREEN): indicates GPO, TRG IN, and GPI signals are TTL;

NIM (GREEN): indicates GPO, TRG IN, and GPI signals are NIM;

PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;

PLL BYPS (GREEN): indicates the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off;

RUN (GREEN): indicates the acquisition is running (data taking);

TRG (GREEN): indicates the trigger is accepted;

DRDY (GREEN): indicates the event/data is present in the Output Buffer;

BUSY (RED): indicates all the buffers are full for at least one channel or the board cannot accept new triggers due to the digital conversion dead time.

IDENTIFYING LABELS

A blue label on top of the NIM front panel indicates:

- Manufacturer name and functional name
- Module name and the input range information

A little silver label on the bottom of the NIM front panel reports:

- Serial Number (S/N)

7 Functional Description

Analog Input Stage

Input dynamics is 2.5 V_{pp} on single ended MCX coaxial connectors (see Chap. **Panels Description**). A 16-bit DAC allows to add up to a ±1.25 V DC offset to preserve the full dynamic range also in the extreme case of unipolar, positive or negative input signal.

The input bandwidth ranges from DC to 500 MHz (@3dB) by 2nd order linear phase anti-aliasing low pass filter.

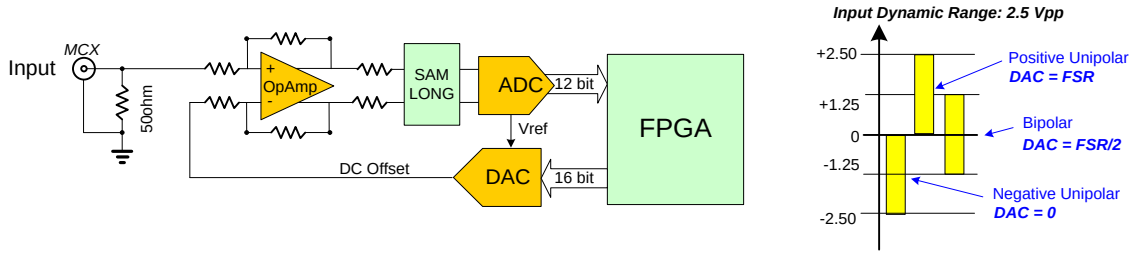


Fig. 7.1: Analog Input Diagram

Setting the DC offset can be managed by WaveCatcher software or through the Set/*GetChannelDCOffset()* functions of the CAENDigitizer library.

Sampling in the Analog Memory

The analog input signals from each pair of channels are continuously sampled into one SAMLONG chip, which consists of a matrix of Delay Line Loops (DLLs) generating a 3.2 GS/s sampling frequency from an input clock of 200 MHz; 1.6 GS/s, 0.8 and 0.4 GS/s frequencies are also software selectable (see Sec. **Changing the Sampling Frequency**).

Signals produced by the DLLs simultaneously open write switches in both sampling channels, where the differential input signals are sampled (1024 sampling capacitance cells per channel).

After being started by the so-called "Run" signal (corresponding to the WRITE signal on **Fig. 7.2**) going high, the DLLs run continuously in a circular fashion (after reaching the end of the matrix, samples are over written) until decoupled from the write switches when the Run signal goes down. This actually takes place after the arrival of a trigger signal synchronously delayed by the so-called post-trigger delay (managed by the *SetSAMPostTriggerSize()* function of the CAENDigitizer library) which finally provokes the freezing of the currently stored signal in the sampling capacitance cells.

Subsequently, the cells are multiplexed into the 12-bit ADCs whose output are stored by the FPGA into the Digital Memory Buffer and made ready for readout in the shape of events data.

A 16-bit DAC allows to add up a ±1.25 V DC offset to preserve the full dynamic range also in the extreme case of unipolar positive or negative input signals (see Sec. **Analog Input Stage**).

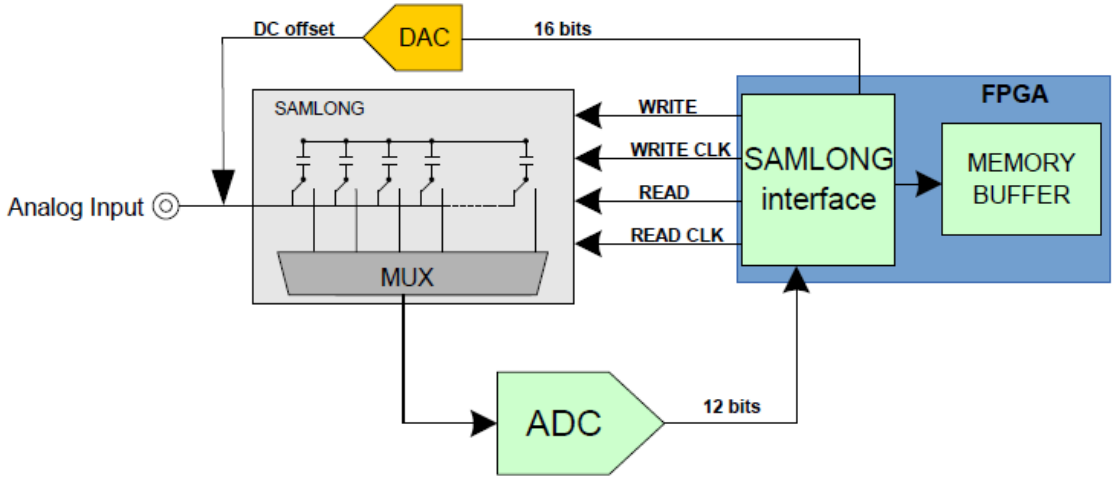


Fig. 7.2: Input Diagram

Detailed documentation of the SAMLONG chip is available at:

http://electronique.lal.in2p3.fr/echanges/USBWaveCatcher/Documentation/Boards&Chips/doc_SAMLONG_rev1.pdf

(in case the active link above doesn't work, copy and paste it on the internet browser)

Digital Memory Buffer

Each pair of input channels shares a SRAM memory in the channel FPGA (see **Fig. 2.1**) that is organized into buffers whose number depends on the event size. This Digital Memory can consecutively store up to 7 full events per channel (1 full event = 1024 samples). It is possible to configure the board to read less than 1024 samples per event, so extending the number of events consecutively storable in the Digital Memory. This option is managed by the *SetRecordLength()* function of the CAENDigitizer library **[RD4]** or by the WaveCatcher software **[RD6]**.

Clock Distribution

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50 MHz clock provided by an on-board oscillator and handles Optical Link, USB and Local Bus, which is the communication between motherboard and mezzanine boards (see red traces in the **Fig. 7.3**).

REF-CLK handles trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external source (i.e. a signal on CLK-IN front panel connector) or an internal one (via the local oscillator) source; in the latter case, OSC-CLK and REF-CLK will be synchronous (the operating mode remains the same anyway). Internal source is the default option. The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm (see **Tab. 3.1**).

REF-CLK handles trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via the front panel signal) or an internal (via the local oscillator) source; in the latter case OSC-CLK and REF-CLK will be synchronous (the operating mode remains the same anyway).

The N6743 makes use of an integrated phase-locked-loop (PLL) and clock distribution device: AD9520. REF-CLK is processed by the AD9520, which delivers 200 MHz clock signals directly to SAMLONG chips (WRITE_CLK on **Fig. 7.2**, Wr_Clk on **Fig. 7.3**) and to the mezzanine FPGA. The latter will divide it to produce the 10 MHz clock used both for the readout of the SAMLONG chips (READ_CLK on **Fig. 7.2**) and for driving the ADC conversion (ADC_Clk on **Fig. 7.3**).

The AD9520 device also provides a 100 MHz clock to the trigger logics.

Refer to the AD9520 datasheet for more details:

http://www.analog.com/static/imported-files/data_sheets/AD9520-0.pdf

(in case the active link above doesn't work, copy and paste it on the internet browser)

When running with the reduced sampling frequencies, the 200 MHz clock is divided inside the front-end FPGA before being sent to the SAMLONG chips via the clock multiplexer as shown in **Fig. 7.3**.

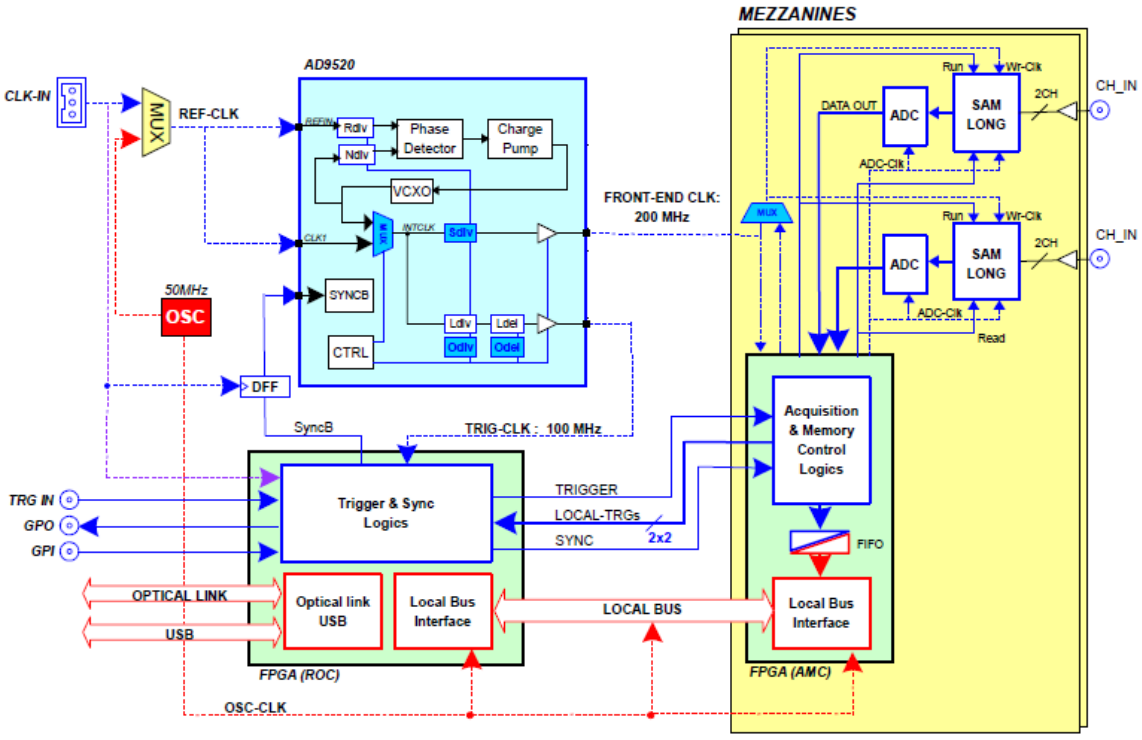


Fig. 7.3: Clock Distribution Diagram

PLL Mode

As introduced in Sec. **Clock Distribution**, the source of the REF-CLK signal can be external (see **Fig. 7.3**) on the front panel CLK-IN connector or internal from the 50 MHz local oscillator (default option). Selecting the REF-CLK source internal or external is possible by setting bit[6] of 0x8100 register address ("0" = internal reference; "1" = external reference). In case of external clock source, the CLK-IN LED must be on (see Sec. **Front Panel**).

The following options are allowed:

1. 50 MHz internal clock source – It's the standard operating mode; the default AD9520 configuration and the clock source setting do not require to be changed. OSC-CLK = REF-CLK.
2. 50 MHz external clock source – The clock source must be set to external; as the external clock reference is identical to the frequency of the internal oscillator, the AD9520 dividers must not be reprogrammed. CLK-IN = OSC-CLK = REF-CLK.
3. External clock source different from 50 MHz – – the clock source must be set to external and the AD9520 must be reprogrammed to lock at the new frequency. **Please, contact CAEN for information** (see Chap. **CAEN Support**).

PLL programming files can be loaded by the user through the CAENUpgrader software tool (see Chap. **Software Tools**).

If the digitizer is locked, the PLL-LOCK front panel LED must be on

Changing the Sampling Frequency

The sampling frequency of the SAMLONG chips can be programmed by software through the *SetSAMSamplingFrequency()* function.

The admitted values are:

3.2 GS/s (default)

1.6 GS/s

0.8 GS/s

0.4 GS/s

Data Correction

Different types of data correction are required to compensate for unavoidable construction differences among the SAMLONG chips. The data correction is not applied at FPGA level, but must be implemented runtime/offline at software level by the user. All boards are factory calibrated during production test and calibration parameters are saved on-board. Application software provided by CAEN, automatically recovers the calibration parameters and runs them in order to correct the stored data events **[RD4] [RD6]**.

The different data correction types are:

- **Line Offset Calibration:** this calibration permits reducing the baseline noise down to ~ 0.95 mV rms. With this sole calibration performed, waveform data is already directly usable with a dynamic range of 11.5 bits and a sampling time precision of ~ 20 ps rms.
- **Individual Pedestal Calibration:** this calibration permits reducing the baseline noise down to ~ 0.75 mV rms, thus increasing the dynamic range to 11.7 bits.

Note: The user is recommended to perform the Individual Pedestal Calibration once he has his setup ready.

- **Time INL Calibration:** this calibration compensates the fixed time dispersion along the sampling matrix. The eventual sampling time precision scales down to ~ 5 ps rms. The factory calibration parameters cannot be modified by the user.
- **Trigger Threshold DAC Offset Calibration:** this calibration is necessary to obtain the best precision for small signals on the trigger threshold for the channel input discriminator. The factory calibration parameters cannot be modified by the user.

Note: The user is not allowed to store his own calibration parameters on the board, except for the Individual Pedestal Calibration, which is managed by WaveCatcher software.

Line Offset Correction

The SAMLONG structure is a matrix of 16 lines and 64 columns. Whereas this structure guarantees a very stable time base, it also has the characteristic that each line is equipped with its own buffer, which provokes an offset modulo 16 in the baseline pattern. Nevertheless, this offset remains very stable. Thus, in order to compensate for it, each line of the chip is equipped with individual correction DACs.

The raw waveform before any correction (vertical scale is 20 mV/div) is shown in **Fig. 7.4**, while **Fig. 7.5** displays a zoom on one channel where the fixed pattern modulo 16 linked to the matrix structure can be distinguished.

Fig. 7.6 displays the sampled waveform after line offset correction with the same vertical scale (20 mV/div) and **Fig. 7.7** shows the same plot as **Fig. 7.6** but with a vertical scale of 2 mV/div.

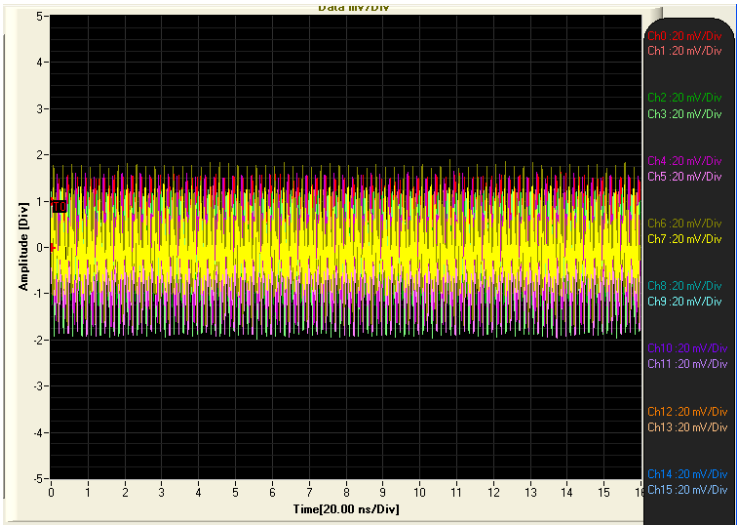


Fig. 7.4: Sampled waveform before line offset correction

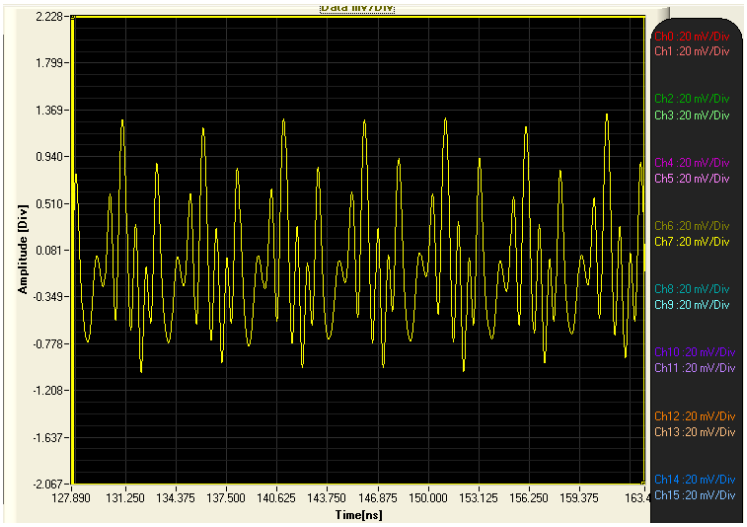


Fig. 7.5: Zoom on the sampled waveform before line offset correction

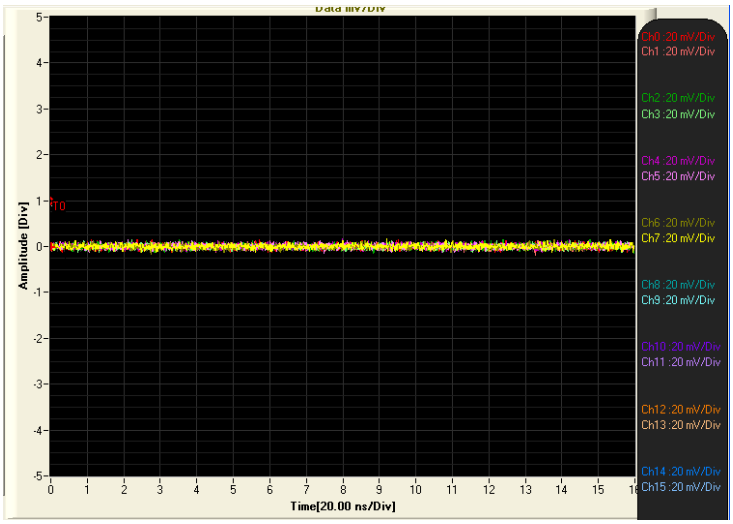


Fig. 7.6: Sampled waveform after line offset correction

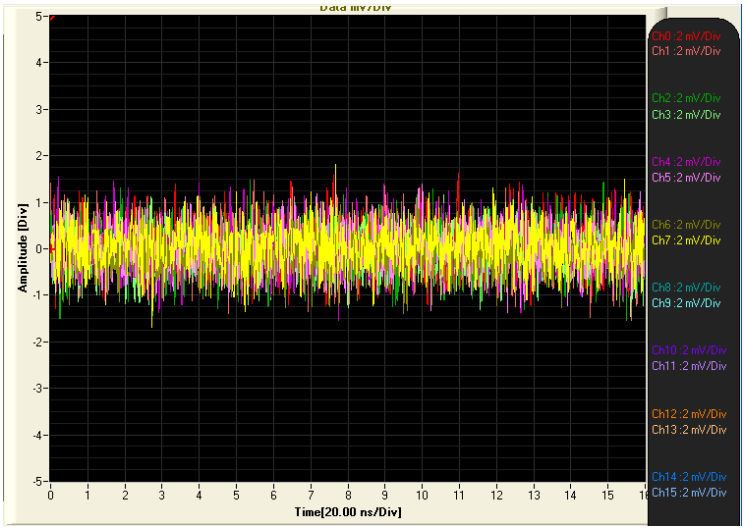


Fig. 7.7: Zoom on the sampled waveform after line offset correction

Individual Pedestal Correction

After the Line Offset correction, there is still a small residual individual offset distribution remaining on the baseline. This calibration will remove it. **Fig. 7.8** displays the waveform after this residual pedestal correction.

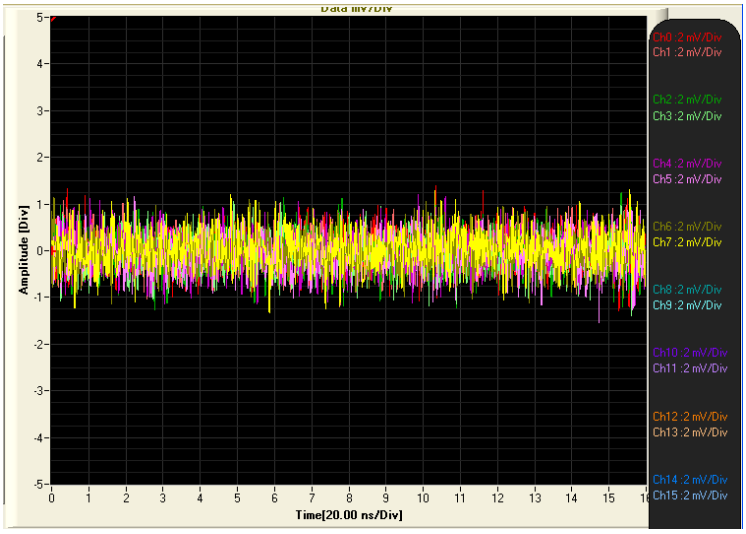


Fig. 7.8: Sampled waveform after individual pedestal correction

Individual pedestal calibration can be performed though the WaveCatcher software (see Chap. **Software Tools**) in the following conditions:

- All the board channels must be disconnected

- Calibration must be done after the board is at its thermal regime

- Calibration must be done each time the temperature conditions vary significantly

Consult the software User Manual for the specific calibration operations **[RD6]**.

Time INL Correction

The sampling sequence is handled by SAMLONG through 1024 physical delay elements spread over the sampling matrix; the unavoidable construction differences between such delay elements can be compensated through a time calibration. The following figures show an example of the integral non-linearity (INL) time profile of SAMLONG chips, before and after correction. Note the extremely low residual value on **Fig. 7.10**.

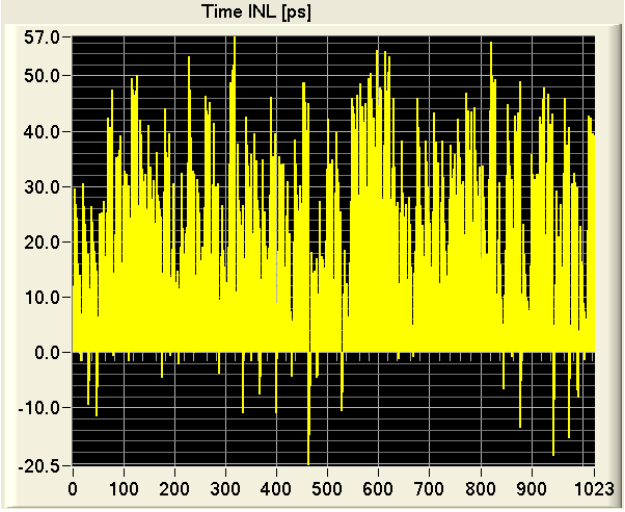


Fig. 7.9: Example of INL before time correction

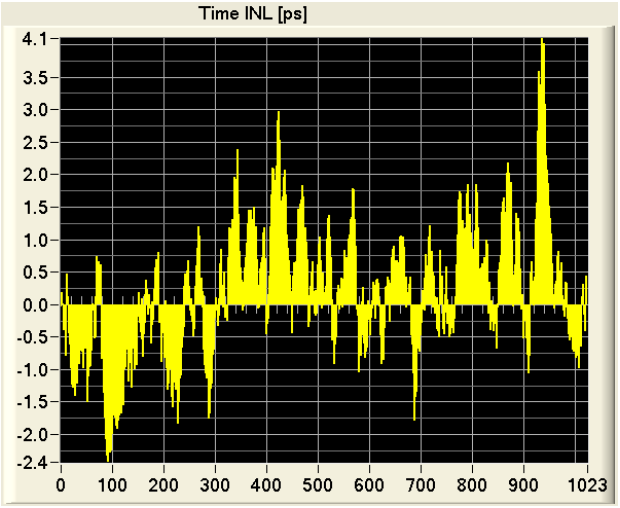


Fig. 7.10: Example of INL after time correction

Trigger Threshold DAC Offset Correction

The latter calibration permits setting the zero of the trigger discriminator threshold with a high precision, thus allowing triggering efficiently on very small signals around zero (a few mV).

Acquisition Run/Stop

The acquisition can be started and stopped in different ways configurable by the *Set/GetAcquisitionMode()*, *SWStartAcquisition()* and *SWStopAcquisition()* functions of the CAENDigitizer library:

- SW CONTROLLED: Start and Stop take place by software command.
- GPI CONTROLLED MODE: Start is issued as the GPI signal is set high and the Stop occurs when it is set low.
- FIRST TRIGGER CONTROLLED: Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled.

Note: CAEN WaveCatcher software only manages the SW Controlled mode.

Running in Charge Mode

The N6743 features an embedded Charge Mode which permits using the FPGA to calculate the charge comprised within a predefined part of each event. As the calculation is performed by the firmware, the acquisition rate can raise up to 7 kHz for full events (depending on the signal input rate). The system will start the summation at a predefined cell value (REF_CELL_FOR_CHARGE). It will last until a total number N (CHARGE_LENGTH) of cells have been summed. Then the result will be stored in a dedicated FIFO (CHARGE_FIFO) together with the physical position of the column where REF_CELL_FOR_CHARGE is located, in order to allow the concerned cells to have their pedestal corrected if necessary. The storage into the FIFO might optionally be filtered by a programmable threshold set on the charge result (CHARGE_THRESHOLD).

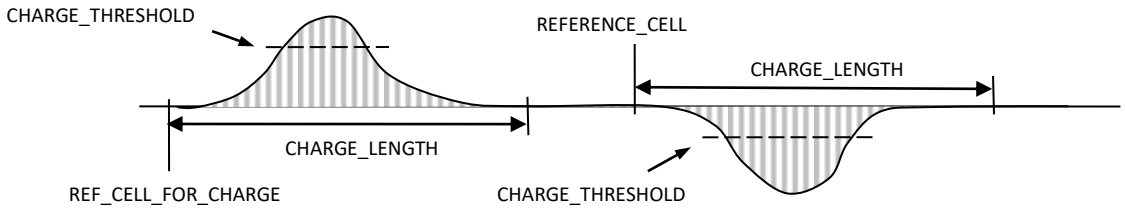


Fig. 7.11: Parameters used for the charge measurement mode

Fig. 7.11 describes the meaning of the different parameters quoted here above, for the integration of both a positive and a negative signal.

These operations are performed in parallel and independently on all channels. The event is readout only when the charge FIFOs will get full (they contain 256 events). To this end, the board front-end is automatically restarted as long as this doesn't happen.

As the number of words might be different in both channels in specific trigger modes, the charge and cell position will get forced to zero when the corresponding read FIFO is empty.

Charge mode is managed by WaveCatcher software and dedicated functions are available in the CAENDigitizer library **[RD4]**.

Event Structure

The event can be readout either via USB or Optical Link as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

Data format is 32-bit long word (see **Fig. 7.12**).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER	1	0	1	0	TOTAL EVENT SIZE (LWORDS)																											
	RESERVED						BF	RES	0	RESERVED															0	0	0	0	GROUP_MASK			
	RESERVED																EVENT COUNTER															
	EVENT TIME TAG																															
GROUP 0	GROUP HEADER							GROUP 0 CHANNEL DATA first word																								
	GROUP 0 information							GROUP 0 CHANNEL DATA																								
	GROUP TRAILER							GROUP 0 CHANNEL DATA last word																								
GROUP 1	GROUP HEADER							GROUP 1 CHANNEL DATA first word																								
	GROUP 1 information							GROUP 1 CHANNEL DATA																								
	GROUP TRAILER							GROUP 1 CHANNEL DATA last word																								
GROUP 2	GROUP HEADER							GROUP 2 CHANNEL DATA first word																								
	GROUP 2 information							GROUP 2 CHANNEL DATA																								
	GROUP TRAILER							GROUP 2 CHANNEL DATA last word																								
GROUP 3	GROUP HEADER							GROUP 3 CHANNEL DATA first word																								
	GROUP 3 information							GROUP 3 CHANNEL DATA																								
	GROUP TRAILER							GROUP 3 CHANNEL DATA last word																								

Fig. 7.12: Event Format

Note: A group is composed by 2 adjacent analog channels (GROUP 0 = channels 0 - 1, GROUP 1 = channels 2 - 3, GROUP 2 = channels 4 - 5, GROUP 3 = channels 6 - 7).

Header

The Header consists of 4 words including the following information:

- **TOTAL EVENT SIZE (Bit[27:0] of 1st header word)** is the size of the event, header included (number of 32-bit words);
- **BOARD FAIL FLAG (Bit[26] of 2nd header word)** implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user is then recommended to contact CAEN Support Service (see Chap. **CAEN Support**).
- **EVENT MODE (Bit[24] of 2nd header word)** identifies the event format; in case of 743 digitizer family, it **must be set to "1";**

Note: the bit is set to "0" by default in the firmware; WaveCatcher software automatically sets it to "1" during the board initialization, but the user must set it manually when developing a customized software.

- **GROUP MASK (Bit[3:0] of 2nd header word)** is the mask of the groups participating in the event (e.g. GROUP 0 and GROUP 1 participating → G.MSK = 0x3; this information must be used by the software to acknowledge what group the samples are coming from; the first event contains the samples from the group with the lowest number);
- **EVENT COUNTER (Bit[21:0] of 3rd header word)** is the trigger counter;
- **EVENT TIME TAG (Bit[31:0] of 4th header word):)** is a 31-bit counter and the 32nd bit as roll over flag; the counter is reset when the acquisition starts or by an external signal (see Sec. **Timer Reset**) and is incremented at each trigger clock hit (10 ns @100MHz). It corresponds to the time when the event is created in the digitizer memory and it is not related to any physical quantity. The Trigger Time Tag time reference, which gives information on when the trigger occurred, is the 40-bit counter of TDC field in the data format (see **Fig. 7.13**).

Data

Data are the stored information from each enabled group; data from masked groups are not read. The part of an event related to each group presents the format described in **Fig. 7.13** (example based on GROUP 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP HEADER = 0x69								ADC DATA CHANNEL 1 SAMPLE 0												ADC DATA CHANNEL 0 SAMPLE 0											
HIT_COUNTER CH0 LSB								ADC DATA CHANNEL 1 SAMPLE 1												ADC DATA CHANNEL 0 SAMPLE 1											
HIT_COUNTER CH0 MSB								ADC DATA CHANNEL 1 SAMPLE 2												ADC DATA CHANNEL 0 SAMPLE 2											
TIME_COUNTER CH0 LSB								ADC DATA CHANNEL 1 SAMPLE 3												ADC DATA CHANNEL 0 SAMPLE 3											
TIME_COUNTER CH0 MSB								ADC DATA CHANNEL 1 SAMPLE 4												ADC DATA CHANNEL 0 SAMPLE 4											
HIT_COUNTER CH1 LSB								ADC DATA CHANNEL 1 SAMPLE 5												ADC DATA CHANNEL 0 SAMPLE 5											
HIT_COUNTER CH1 MSB								ADC DATA CHANNEL 1 SAMPLE 6												ADC DATA CHANNEL 0 SAMPLE 6											
TIME_COUNTER CH1 LSB								ADC DATA CHANNEL 1 SAMPLE 7												ADC DATA CHANNEL 0 SAMPLE 7											
TIME_COUNTER CH1 MSB								ADC DATA CHANNEL 1 SAMPLE 8												ADC DATA CHANNEL 0 SAMPLE 8											
SAMPLING_FREQUENCY								ADC DATA CHANNEL 1 SAMPLE 9												ADC DATA CHANNEL 0 SAMPLE 9											
EVENT_ID								ADC DATA CHANNEL 1 SAMPLE 10												ADC DATA CHANNEL 0 SAMPLE 10											
FCR LSB								ADC DATA CHANNEL 1 SAMPLE 11												ADC DATA CHANNEL 0 SAMPLE 11											
FCR MSB								ADC DATA CHANNEL 1 SAMPLE 12												ADC DATA CHANNEL 0 SAMPLE 12											
TDC Byte 0 (LSB)								ADC DATA CHANNEL 1 SAMPLE 13												ADC DATA CHANNEL 0 SAMPLE 13											
TDC Byte 1								ADC DATA CHANNEL 1 SAMPLE 14												ADC DATA CHANNEL 0 SAMPLE 14											
TDC Byte 2								ADC DATA CHANNEL 1 SAMPLE 15												ADC DATA CHANNEL 0 SAMPLE 15											
TDC Byte 3								ADC DATA CHANNEL 1 SAMPLE 16												ADC DATA CHANNEL 0 SAMPLE 16											
TDC Byte 4 (MSB)								ADC DATA CHANNEL 1 SAMPLE 17												ADC DATA CHANNEL 0 SAMPLE 17											
DUMMY								ADC DATA CHANNEL 1 SAMPLE 18												ADC DATA CHANNEL 0 SAMPLE 18											
DUMMY …								ADC DATA …												ADC DATA …											
GROUP TRAILER = 0x96								ADC DATA CHANNEL 1 SAMPLE N-1												ADC DATA CHANNEL 0 SAMPLE N-1											

Fig. 7.13: Group Data Format

In the group data described above, the number of words directly corresponds to the number of columns read in the SAMLONG chips multiplied by 16 (fixed number of lines). Bits 0 to 23 always correspond to digitized event data. Both channels are grouped inside the same word. Bits 24 to 31 are used for header, trailer, and event information.

- For each channel, **HIT_COUNTER** and **TIME_COUNTER** are 16-bit counters used to calculate the hit rate linked to the activity on the channel since the last event. HIT_COUNTER counts the number of times the input discriminator has be toggling since the last event, whereas TIME_COUNTER counts the time in units of 1 µs. The first counter saturating blocks the other. Taking care of memorizing this information long enough in the software, this measurement can range from 0.1 Hz to > ~400 MHz (see Sec. **Hit Rate Monitor**).
- **SAMPLING_FREQUENCY** is common to all channels. It is coded on 2 bits as follows:

  0 => 3.2 GS/s

  1 => 1.6 GS/s

  2 => 0.8 GS/s

  3 => 0.4 GS/s

- **EVENT_ID** corresponds to the 8 lower significant bits of the event number since the beginning of the run.
- **FCR** is the address of the First Cell Read in the SAMLONG chip for the current event. It is coded on 10 bits (which corresponds to the 1024 cells).

TDC is the value of the individual channel counter and is coded over 40 bits. This is the Trigger Time Tag reference. The corresponding counter runs with the SAMLONG clock, thus covering a minimum of 1h30 at 200 MHz. It is reset at the acquisition RUN, but also by feeding an external signal on GPI input connector (see Sec. **Timer Reset**).

In case of charge readout mode (see Sec. **Running in Charge Mode**), the part of an event related to each group presents the format as in **Fig. 7.14** (example of GROUP 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 1																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 1																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 2																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 2																							
-	-	…						-	…																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 256																							
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 256																							

Fig. 7.14: Group Data Format in Charge Mode

In the group data described above, the number of words (512) corresponds to twice the charge FIFO depth per channel (256 words). Charge data is coded in two's complement over 23 bits and expressed in pC. **REF CELL COLUMN** corresponds to the number of the physical column where the charge calculation started inside the SAMLONG chip (0 to 63). It is necessary for optional software correction purpose.

Acquisition Synchronization

As introduced in Sec. **Digital Memory Buffer**, each pair of input channels share a SRAM memory in the channel FPGA that is organized into a variable number of buffers, according to the programmable event size. Up to 7 full events per channel, that is to say 7 kS/ch (1 event = 1024 samples or 1024 * 12 bits) can be consecutively stored. When the trigger occurs, the acquisition takes place as described in Sec. **Sampling in the Analog Memory**.

When the Digital Memory Buffer is filled, the board is considered FULL: no trigger is accepted and the acquisition stops. As soon as at least one buffer is readout, the board exits the FULL condition and acquisition restarts.

BUSY Front Panel LED

The BUSY red LED on the digitizer front panel lits when at least one of the following condition is reached:

- The board is not available to accept the triggers because of the conversion dead-time (SAMLONG).
- The board is FULL.

Trigger Management

All the channels of the board share the same trigger (common trigger), that is to say they acquire an event simultaneously and in the same way (a determined number of samples and position with respect to the trigger).

The common trigger is generated basing on different trigger sources:

- **Software trigger:** produced via a software command.
- **External trigger:** received via the front panel TRG-IN connector.
- **Self-trigger:** generated by the individual discriminator, with programmable threshold, placed on each analog channel. The two self-trigger signals coming from a couple of adjacent channels then generate a single trigger request. The trigger requests from all the couples finally contribute to the common board trigger generation.
- **Coincidence** between channels.
- **Programmable majority** of the trigger requests.

As a common trigger is issued, the analog buffers related to that trigger are frozen, then digitized by the 12-bit ADCs, then stored into the digital memory buffer and are available for readout (refer to Sec. **Sampling in the Analog Memory**).

The analog to digital conversion process is affected by a dead time during which the module cannot handle other triggers. This dead time depends on the number of samples to be digitized (13 µs + ($N_{samples}$ / 16) * 1.75 µs). The N6743 features a maximum dead time of 125 µs (@ 1024 samples recording).

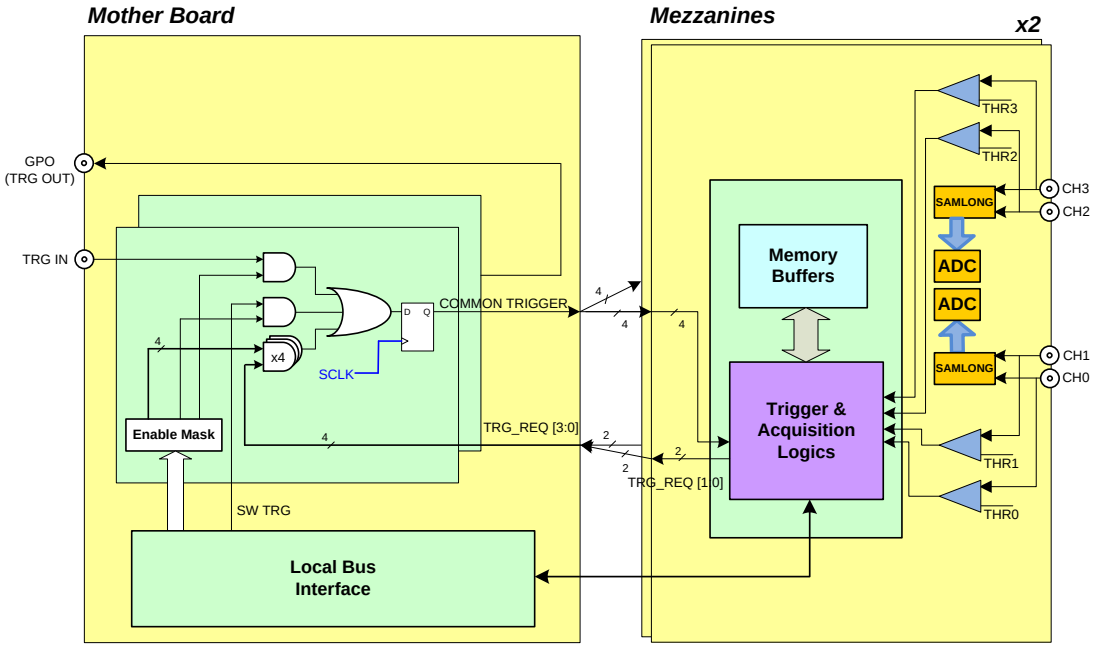


Fig. 7.15: Trigger Management block diagram

Software Trigger

Software triggers are internally generated via a software command over USB or Optical Link (through the WaveCatcher software or the *SendSWTrigger()* function of the CAENDigitizer library).

External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable through the WaveCatcher software or the *Set/GetExtTriggerInputMode()* function of the CAENDigitizer library). The external trigger is synchronized with the internal 100 MHz trigger clock.

Self-Trigger

The N6743 is equipped with a discriminator with a 16-bit programmable threshold on each channel, which permits generating a self-trigger signal when the digitized input pulse exceeds the threshold. The self-triggers of each couple of adjacent channels are then processed to provide out a single trigger request. The trigger requests are propagated to the central trigger logic to produce the global trigger, which is finally distributed back to all channels causing the event acquisition (see **Fig. 7.15**). **Fig. 7.16** schematizes the self-trigger generation, the trigger request and global trigger logic.

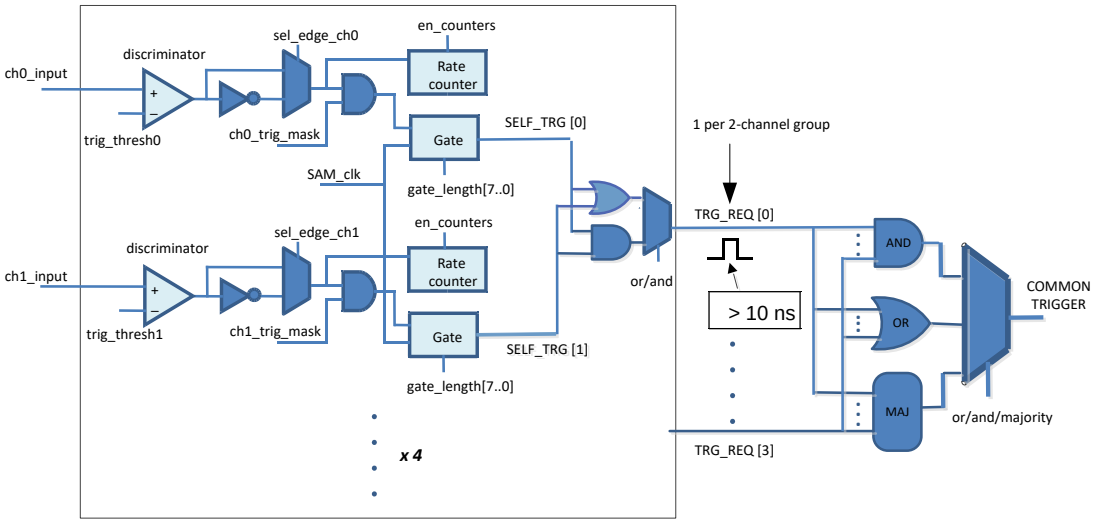


Fig. 7.16: Self-Trigger generation**,** Trigger Request and Global Trigger logic

Tab. 7.1 shows the library functions involved in the self-trigger management.

Signal/Function	Reference Library Function
Trig_thresh0/1	SetChannelTriggerThreshold()
sel_edge_ch0/ch1	SetTriggerPolarity()
ch0/ch1_trig_mask	SetChannelSelfTrigger()
gate_length[7:0]	SetChannelPairTriggerLogic()
or/and	SetChannelPairTriggerLogic()
or/and/majority	SetTriggerLogic()

Tab. 7.1: Map of available CAENDigitizer library functions for the self-trigger management

The *SetChannelPairTriggerLogic()* function of CAENDigitizer library programs the FPGA in order the self-trigger to be a pulse of configurable width (see **Fig. 7.17**).

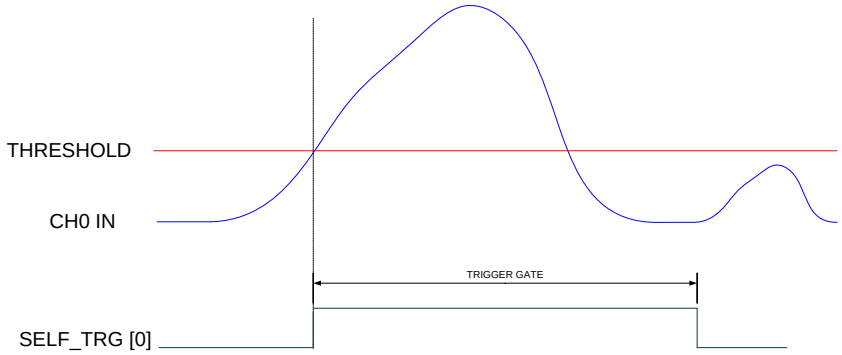


Fig. 7.17: Self-trigger generation

The *SetChannelPairTriggerLogic()* function of CAENDigitizer library programs the FPGA in order the trigger request for a couple of adjacent channels to be the AND or OR of the levant self-trigger signals (see **Fig. 7.16**).

The *SetTriggerLogic()* function of CAENDigitizer library programs the FPGA in order The global trigger can be the OR, the AND or the Majority of the enabled trigger requests (see **Fig. 7.16**).

Default Conditions: by firmware default, the FPGA is programmed so that:

- All the channels are disabled to generate trigger requests, while the external trigger and software trigger are enabled.
- Each trigger request is the OR of two pulses whose width is fixed by default depending on the board operating frequency: 15 ns (@3.2 GS/s); 20 ns (@1.6 GS/s); 30 ns (@0.8 GS/s); 50 ns (@0.4 GS/s).
- The global trigger is generated as the OR of the enabled trigger requests.

Trigger Coincidence Level

T. b. d.

Majority Level

According to the scheme of **Fig. 7.16**, it is possible to configure the board for the global trigger to be the result of the majority operation among the trigger requests coming from the channel couples. This option and the majority level are configurable through the *SetTriggerLogic()* library function and supported by the WaveCatcher software.

The majority level can be set in the range:

[0 : (number of couples -1)]

where majority level = 0 means the global trigger is issued when at least the trigger request from one couple arrives.

Trigger Distribution

As described in Sec. **Trigger Management**, the OR of all the enabled trigger sources (only software trigger and external trigger by default firmware), synchronized with the internal clock, becomes the global trigger of the board and is fed in parallel to all channels, which consequently provokes the capture of an event.

A Trigger Out signal is also generated on the relevant front panel GPO connector (NIM or TTL) for the common trigger signal external propagation. Trigger Out logic is described in **Fig. 7.18**, where only the software trigger is propagated out by firmware default (red path).

Library functions involved are:

- *SetSWTriggerMode()*
- *SetExtTriggerInputMode()*
- *SetChannelSelfTrigger()*

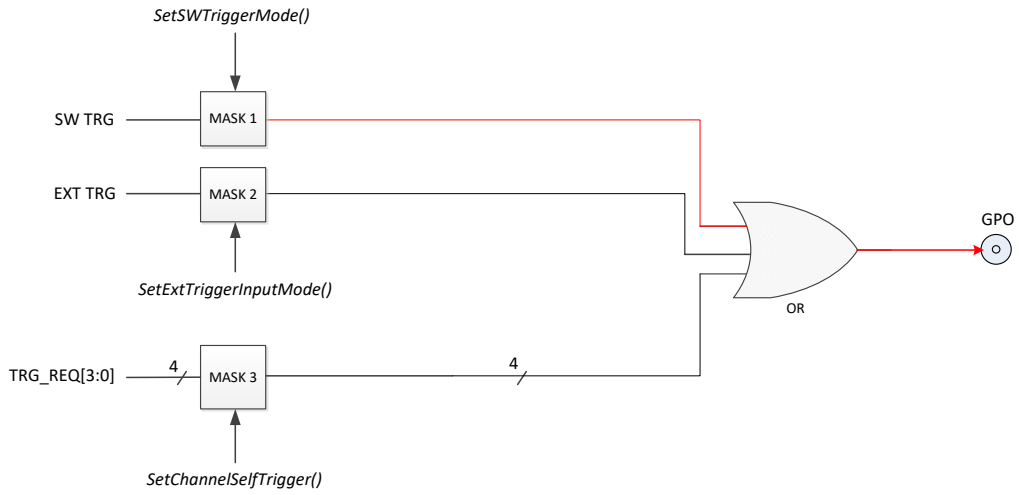


Fig. 7.18: Trigger configuration of GPO front panel connector

Test Pattern Pulser

Each input channel is equipped with an individual pulser. Whereas the pulse amplitude is fixed (~0.7 V with no cable plugged, half this value otherwise), the pattern can be programmed over 16 consecutive bits of the SAMLONG main clock and will be sent every 3.5 µs (see example on **Fig. 7.19**). This permits an easy testing of the board functionality, as well as it gives the possibility to use the board as a reflectometer. As this pulse pattern is produced from an autonomous clock source, trigger can be set on the discriminators.

Pulser function is fully managed by WaveCacther software. Reference CAENDigitizer library functions for this feature are: *Enable / DisableSAMPulseGen()*, *SendSAMPulse()*

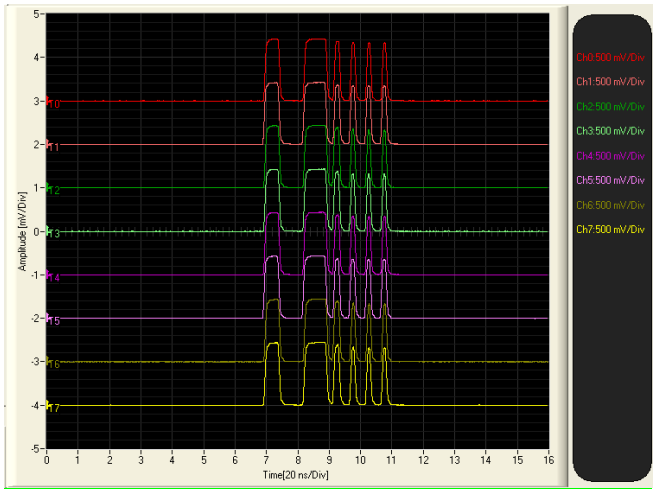


Fig. 7.19: FPGA Test Pulse with 0xC755 pattern

Each channel can make use of his pulser as a reflectometer. An example of this application is shown on **Fig. 7.20**, where a 40-ns wide square pulse produced internally is sent to a 1-meter open cable connected to the board.

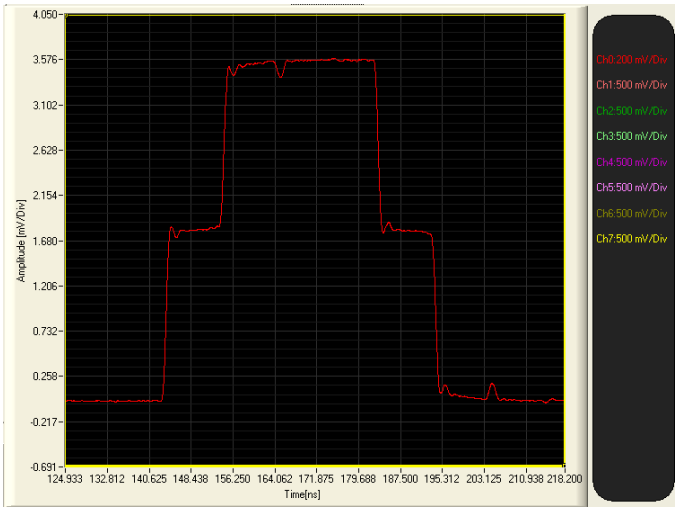


Fig. 7.20: FPGA Test Pulse in reflectometer mode

Hit Rate Monitor

Each input channel is equipped with an individual hit rate monitor. As shown on **Fig. 7.21**, the latter is based on two counters, one counting the number of hits crossing the programmed discriminator threshold (TRIG_COUNT), the other counting the time elapsed with a 1-MHz clock (TIME_COUNT). These counters are reset and restarted after each read access. Their content is stored into the event data (see Sec. **Event Structure**). As soon as any of them saturates, both are frozen, and thus their values are always valid. The rate counters work up to ~400 MHz and, if this information is memorized long enough in the software along events, rate measurement can work as low as ~0.1 Hz.

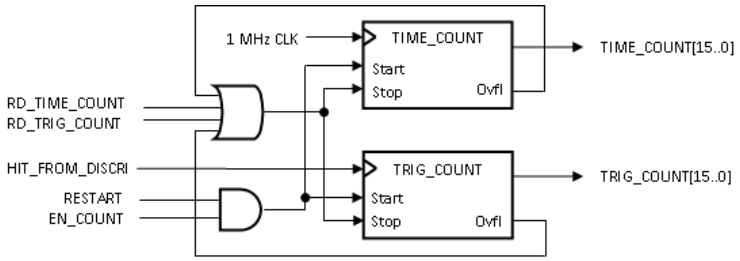


Fig. 7.21: Principle of the Hit Rate Monitor

Veto Gate for the Trigger Rate Counter

It is possible to configure the board to inhibit the trigger counting within an adjustable time window after the digitization starts. This option can be used to reject unwanted after-pulses and is configurable through the *SetSAMTriggerCountVetoParam()* function of CAENDigitizer library.

Reset, Clear and Default Configuration

Global Reset

Global Reset is performed at Power ON of the module or via software by the *SendSWtrigger()* function of CAENDigitizer library. It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded by the *ClearData()* library function of CAENDigitizer library.

Timer Reset

The Timer Reset allows to initialize the timers which allows to tag an event (Event Time Tag and TDC described at Sec. **Event Structure**). The Timer Reset can be forwarded with a pulse sent to the front panel GPI input (leading edge sensitive).

Data Transfer Capabilities

In the N6743, each pair of input channels share a SRAM memory in the channel FPGA that is organized into buffers. Once they are written in the memory, events become available for readout via USB or Optical Link. During the memory readout, the board can continue to store more events (independently from the readout) on the free buffers. This guarantees that no dead time due to the acquisition process (i.e. readout) occurs until the memory becomes full. The only dead time the board remains affected, is due to the A/D conversion.

Although the memories are SRAMs, addresses are taken from a FIFO. Therefore, data are read from the memories sequentially, according to the selected Readout Logic, from a memory space mapped on 4 Kb (0x0000÷0x0FFC).

The events are readout sequentially and completely, starting from the Header of the first available event, followed by the Trigger Time Tag, the Event Counter and all the samples of the group channels (from 0 to 1). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

The board supports 32-bit single data readout and block transfers.

Block Transfers

The Block Transfer readout mode allows to read N complete events sequentially, where N is set by using the *SetMaxNumEventsBLT()* function of the CAENDigitizer library.

When developing programs, the readout process can be implemented on different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link **(not supported by USB)**.
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of the *SetMaxNumEventsBLT()* function above mentioned. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the *ReadData()* function in the CAENDigitizer Library).

Whatever the method from above, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite of a greater memory allocation required on the host station side that is actually not a real drawback, considering the features of the personal computers available on the market.

Single Data Transfer

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **Event Structure**.

It is suggested, after the 1st word is transferred, to check the TOTAL EVENT SIZE information and then do as many cycles as necessary (actually TOTAL EVENT SIZE -1) in order to read completely the event.

Optical Link and USB Access

The board houses a USB2.0 compliant port, providing a transfer rate up to 30 MB/s, and a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) providing transfer rate up to 80 MB/s. Therefore, it is possible to connect up to eight (8) N6743 boards to a single A2818 PCI Optical Link Controller or up to thirty-two (32) boards to a single A3818 PCIe Optical Link Controller (4-link A3818C version). Detailed information on CAEN PCI/PCIe Controllers can be find on CAEN website at the path:

Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controllers

The parameters for read/write accesses via optical link are Address Modifier, Base Address, data Width, etc.; wrong parameter settings cause Bus Error.

It is possible to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed. Interrupts are managed at the CAENDigitizer library level (see “Interrupt Configuration” in **[RD4]**).

8 Drivers & Libraries

Drivers

To interface with the N6743, CAEN provides the drivers for all the different types of physical communication channels featured by the board and compliant with Windows® and Linux® OS:

- **USB 2.0 Drivers** are downloadable on CAEN website (www.caen.it) in the "Software/Firmware" tab at the N6743 web page (**login required**).

Note: For Microsoft Windows® OS, the USB driver installation is detailed in **[RD2]**.

- **Optical Link Drivers** are managed by the A2818 PCI controller or the A3818 PCIe controller. The driver installation package is available on CAEN website in the "Software/Firmware" area at the A2818 or A3818 page (**login required**)

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific Controller.

Libraries

CAEN libraries are a set of middleware software required by CAEN software tools (including WaveCatcher) for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason, **the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

  The CAENDigitizer installation package is available on CAEN website in the 'Download' area at the CAENDigitizer Library page. Reference document **[RD4]**.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.

  The CAENComm installation package, and the link to the required CAENVMELib, is available on CAEN website in the 'Download' area at the CAENComm Library page. Reference document **[RD5]**.

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® compliant CAEN software = NOT. *CAEN software for Windows® OS are stand-alone, which means the program locally installs the DLL files of the required libraries.*

LINUX ® compliant CAEN software = YES. *CAEN software for Linux® OS is not stand-alone. The user must install the required libraries apart to run the software.*

WINDOWS® and LINUX® compliant customized software = YES. *The user must install the required libraries apart in case of custom software development.*

The CAENComm (and so the CAENDigitizer) supports the following communication channels:

PC → USB → N6743

PC → PCI (A2818) → CONET → N6743

PC → PCIe (A3818) → CONET → N6743

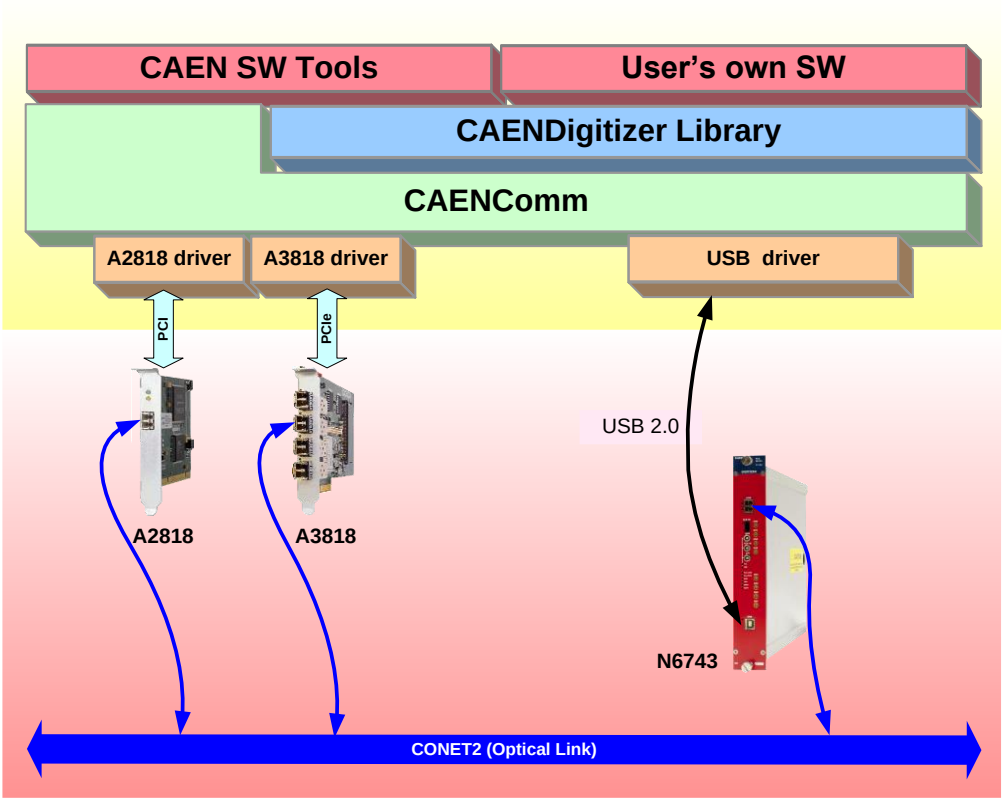


Fig. 8.1: Required libraries and drivers

9 Software Tools

CAEN provides software tools to interface the N6743, which are available for free download on CAEN website (www.caen.it) at:

Home / Products / Firmware/Software / Digitizer Software

WaveCatcher

The N6743 can be fully controlled through the WaveCatcher software.

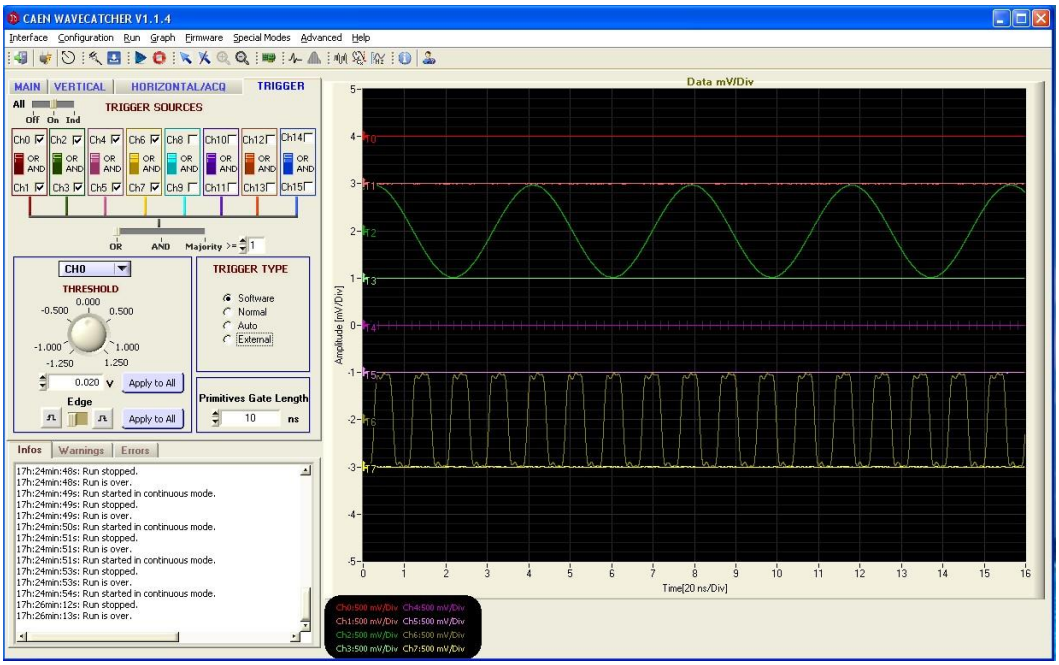


Fig. 9.1: WAVECatcher software for N6743

WaveCatcher is a complete tool made by CNRS/IN2P3/LAL and capable to control a single board of the 743 Digitizer series.

This tool offers a graphical user friendly interface which permits to take benefit of all the functionalities of the hardware: sampling frequency, different trigger modes, waveforms and charge data acquisition, channel pulses, etc.

WaveCatcher also features different tools for on-line measurements and histograms plotting: graphical cursors, noise level, raw hit rates, charge amplitude and time measurements, time distance histograms between channels (fixed threshold and digital CFD methods), charge histograms, FFT, etc.

All acquired data and computed measurements can be saved to files for further replay or off-line analysis.

The software installation package can be downloaded on CAEN web site **(login required)** at:

Home / Products / Firmware/Software / Digitizer Software / Readout Software / WaveCatcher

Find the program detailed description and usage descripted in **[RD6].**

Note: WaveCatcher is available for Windows® platforms (32 and 64-bit) as a stand-alone version (all the required CAEN libraries are installed locally with the program). Only the drivers for the specific communication link must be installed apart by the user.

CAENUpgrader

CAENUpgrader is a software composed of command line tools together with a Java Graphical User Interface.

With a N6743, CAENUpgrader allows in few easy steps to:

- Upload different firmware versions on the digitizer
- Select which copy of the stored firmware must be loaded at power-on
- Read the firmware release of the board and the bridge (if included in the communication chain)
- Upgrade the internal PLL
- Get the board info file, useful in case of support

Note: CAENUpgrader locally stores a set of ready-to-use basic PLL programming files. Special files must be generated by CAEN upon user's specifications by contacting the Support Service (see Chap. **12**)

The program relies on CAENComm and CAENVMELib libraries (see Chap. **8**), and requires the third-party Java SE 8 update 40 (or higher).

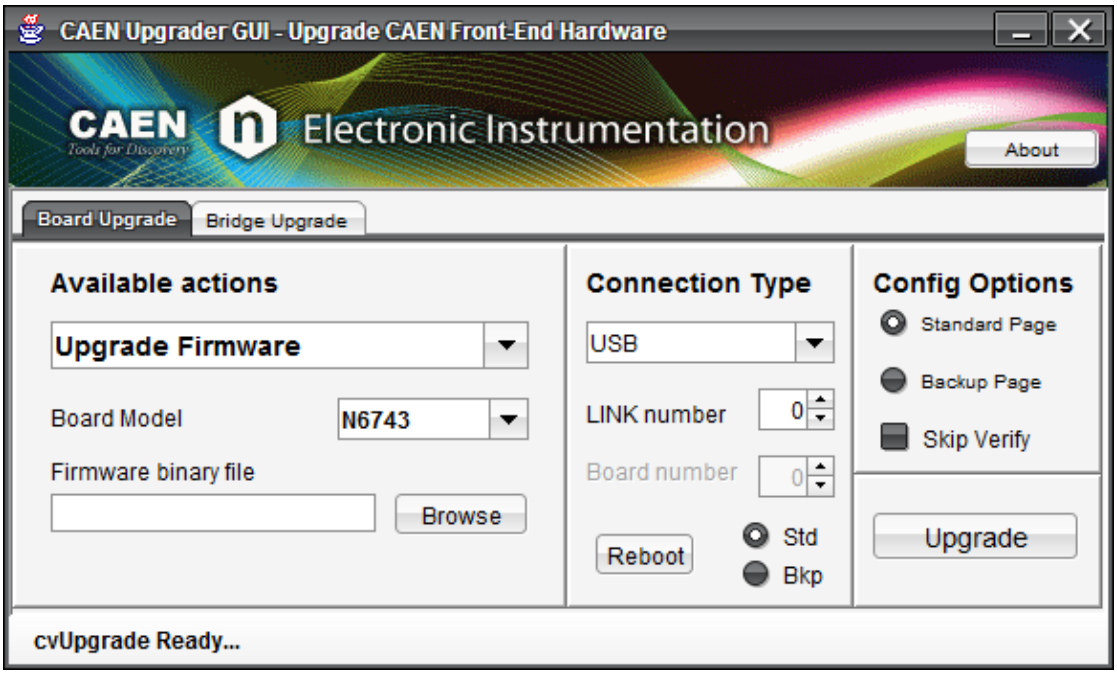


Fig. 9.2: CAENUpgrader Graphical User Interface

The software installation package can be downloaded on CAEN web site **(login required)** at:

Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader

The reference document for installation instructions and program detailed description is **[RD1]**.

Note: the CAENUpgrader is available for Windows® platforms (32 and 64-bit) as a stand-alone version (all the required CAEN libraries are installed locally with the program). Only the drivers for the specific communication link must be installed apart by the user. The CAENUpgrader version for Linux® platform is not stand-alone, so it needs the required libraries to be installed apart by the user.

CAENComm Demo

CAENComm Demo is a simple software developed in C/C++ source code and provided both with with Java™ and LabVIEW™ GUI interfaces. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

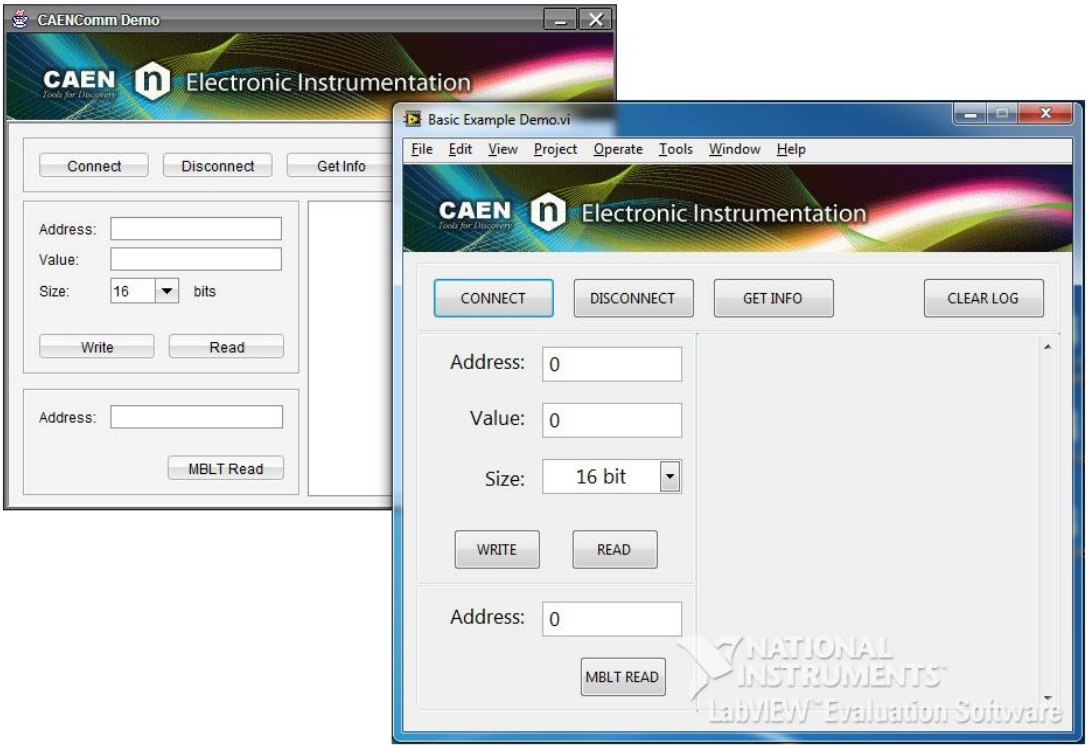


Fig. 9.3: CAENComm Demo Java and LabVIEW graphical interface

The Demo is included in the CAENComm library installation Windows® package, which can be downloaded on CAEN web site (**login required**) at

Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library

The reference document for installation instructions and program detailed description is **[RD5].**

Note: the CAENComm Demo is available for Windows® platforms (32 and 64-bit) and requires CAENComm and CAEVMElib libraries as additional software to be installed apart by the user (see Chap. **8**).

10 HW Installation

- The Module fits into all NIM crates.
- **Use only crates with forced cooling air flow**
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: this product needs proper cooling:

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

Power-on Sequence

To power on the board, follow this procedure:

1. Insert the module into the crate
2. Power up the crate

Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration.

After the power-on, the front panel LEDs status is that only the NIM and PLL LOCK remain ON (see **Fig. 10.1)**.

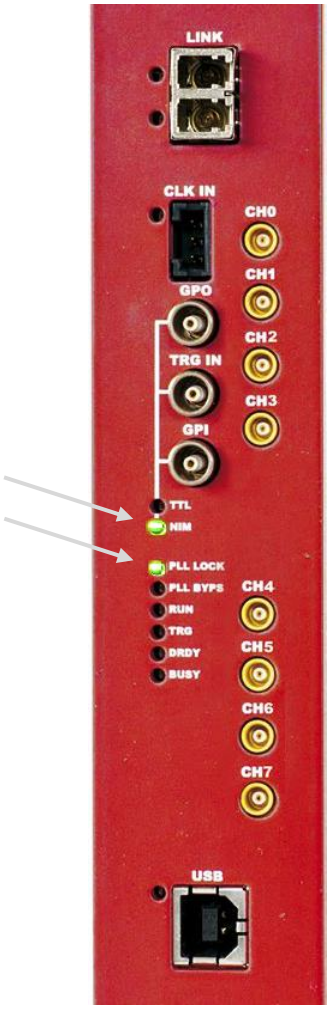


Fig. 10.1: Front panel LEDs status at power ON

11 Firmware and Upgrades

The board hosts one FPGA on the mainboard and one FPGAs on each mezzanine (i.e. one FPGA per 4 channels). The channel FPGAs firmware is identical. A unique file is provided, that will updated all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA CHANNEL FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

The firmware is stored onto on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). The board is usually factory equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy.

Firmware Upgrades

Firmware updates are available for download on CAEN website in the “Software/Firmware” tab at the N6743 web page **(login required)**:

Home / Products / Modular Pulse Processing Electronics / VME / Digitizers / N6743

It is possible to upgrade the board firmware via USB or Optical Link by writing the FLASH with the CAENUpgrader software (see Chap. **9**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

Firmware File Description

The extension of the programming firmware file is CFA (CAEN Firmware Archive), which is a sort of archive format file aggregating all the firmware files compatible with the same family of digitizers.

The firmware file name follows this general scheme:

x743_revX.Y_W.Z.CFA

where:

- x743 are all the boards the file is compliant to: N6743, N6743, V1743, VX1743
- X.Y is the major/minor revision number of the mainboard FPGA
- W.Z is the major/minor revision number of the channel FPGA

Troubleshooting

In case of upgrading failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system automatically programs the board from the alternative FLASH page (e.g. BKP page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

NOTE THAT old versions of the digitizer motherboard have a slightly different FLASH management. Use CAENUpgrader 1.6.0 or higher to get the Board Info file from the board ("Get Information" function) and check if FLASH Type = 0..

In this case, at power-on the microcontroller loads the firmware copy from the STD page of the FLASH.

When a failure occurs while upgrading the STD page, which compromises the communication with the N6743, the user can perform the following recovering procedure as first attempt:

- Force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, the Reboot option in CAENUpgrader software tool (see **Fig. 9.2**).

- Use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is possible now to communicate again with the board.

- Use CAENUpgrader to load again the firmware on the STD page, then power-cycle in order the board to get operative again.

If neither of the procedures here described succeeds, the board needs to be sent back to CAEN in repair (see Chap. **12**).

12 CAEN Support

CAEN support services are available for the user by accessing the *Support & Services* area on CAEN website at www.caen.it.

Returns and Repairs

Users who need for product(s) return and repair must fill and send the Product Return Form (PRF) in the *Returns and Repairs* area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.

Contacts for shipping are reported on the website at *Home / Contacts*.

Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)

CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Standards for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

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