CAEN
Tools for Discovery

Electronic Instrumentation

User Manual UM4295

N6742

16+1 Channel 12bit 5 GS/s Switched Capacitor Digitizer

Rev. 8 - January 30th, 2017

Purpose of this Manual

This document contains the full hardware description of the N6742 CAEN digitizer and its principle of operating as Waveform Recording Digitizer (basing on the hereafter called ”default firmware”).

The reference firmware revision is: **4.13_1.01**.

For any reference to registers in this user manual, please refer to document [RD1] at the digitizer web page.

Change Document Record

Date	Revision	Changes
-	00-07	N/A
January 30th, 2017	08	Revised text layout. Improved text description to make it clearer.

Symbols, Abbreviated Terms and Notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
LVDS	Low-Voltage Differential Signal
PLL	Phase-Locked Loop
ROC	ReadOut Controller
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

[RD1] CAEN User Manual UM5698. *742 Register Description*.

[RD2] CAEN User Guide GD2512. *CAENUpgrader QuickStart Guide*.

[RD3] CAEN User Manual UM2091. *CAEN WaveDump User Manual*.

[RD4] CAEN User Manual UM1935. *CAENDigitizer User & Reference Manual*.

[RD5] CAEN User Manual. *V1718 & VX1718 User & Reference Manual*.

[RD6] CAEN User Manual. *V2718 & VX2718 User & Reference Manual*.

[RD7] CAEN User Manual UM1934. *CAENComm User & Reference Manual*.

[RD8] CAEN User Guide GD5695. *742 Quick Start Guide*.

[RD9] CAEN User Guide GD2783. *First Installation Guide to Desktop Digitizers & MCA*.

All documents can be downloaded at: *http://www.caen.it/csite/LibrarySearch.jsp*

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MADE IN ITALY: We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked ”MADE IN ITALY”, we cannot attest to the manufacturing process of ”third party” boards).

Index

List of Figures

List of Tables

Safety Notices

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1 Introduction

The Mod. N6742 is a Desktop module housing 16+1 Channels 12 bit 5 GS/s Switched Capacitor Digitizer. The input dynamic range is 1 V_{pp} on single-ended MCX coaxial connectors (16-bit DAC on each channel to control the DC Offset).
The digitizer is based on the Switched Capacitor Array DRS4 chip[1] (Domino Ring Sampler). This technology relies on a series of 1024 capacitors (analog memory) in which the analog input signal is continuously sampled in a circular way. The sampling frequency is 5 GHz by default and it can be programmed to 2.5 GHz, 1GHz, and 750 MHz. The analog to digital conversion is not simultaneous with the chip sampling phase, and it starts as soon as the trigger condition is met. When the trigger stops the DRS4 chip sampling (holding phase), the analog memory buffer is frozen, and the cell content is made available to the 12 bit ADC for the digital conversion. The digital memory allows to store subsequent events, even if the readout is not yet started. Moreover, since the digital memory buffers work like FIFOs, the readout activity from USB or Optical Link does not affect write operations of subsequent events.
The chip functioning has two major consequences:

1. there is an unavoidable dead-time when the DRS4 chip stops its acquisition and the ADC converts the capacitances (110 µs in case only the analog inputs are digitized, 181 µs when also TR0 is digitized).
2. the acquisition window is fixed to 1024 samples, that in case of 5 GHz corresponds to a maximum of about 200 ns. Refer to **Sect. Domino Ring Sampling**.

Moreover, the trigger processing introduces a latency between the trigger arrival and the DRS4 holding phase that varies according to the trigger source. The user must consider it when choosing the proper trigger source for its setup and the type of signal. Four possible trigger sources are available:

1. **Software Trigger**, common to all enabled groups, mainly intended for debug purposes. Refer to **Sect. Software Trigger**.
2. **External Trigger**, trigger on TRG-IN connector, common to all enabled groups. The external trigger latency makes this mode difficult to use at 5 GHz, while all other frequencies can be used with no problem. Refer to **Sect. External Trigger**.
3. **Fast (Low Latency) Local Trigger**, trigger on TR0 connector, common to all enabled groups. This mode is called “Fast” or “Low Latency” since the trigger latency is reduced with respect to the external trigger. This trigger mode is convenient for high precision timing measurements, since the TR0 can be digitized and reported in the output data to be used as time reference. Refer to **Sect. Fast (”Low Latency”) Trigger**.
4. **Self-trigger**, common to all enabled groups. For each group is possible to select combination of channels (logic OR) that provide a trigger whenever the input crosses the threshold. This mode cannot be used at 5 GHz due to the trigger latency and one of the other options must be used. Refer to **Sect. Self-Trigger** for additional details.

The module features a PLL for clock synthesis with a selectable internal reference (50 MHz oscillator) or external reference on CLK-IN connector.
By ordering options (see **Tab. 1.1**), the module is available with digital memory sizes of 128 event/ch or 1024 event/ch.
The board houses a daisy chainable Optical Link able to transfer data at 80 MB/s, thus it is possible to connect up to 8 ADC boards (128+8 ADC channels) to a single Optical Link Controller; a USB2.0 compliant port is also featured. Optical Link and USB access are internally arbitrated.

[1] Designed at Paul Scherrer Institute, PSI. Detailed documentation of the DRS4 chip is available at http://drs.web.psi.ch/

Board Model	Description	Product Code
N6742	16+1 Ch. 12 bit 5 GS/s Switched-CapacitorDigitizer: 128 events/ch (1kS/event), EP3C16, SE	WN6742XAAAAA
N6742B	16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16,SE	WN6742BXAAAA
Related Products	**Description**	**Product Code**
A2818	A2818 – PCI Optical Link (Rhos compliant)	WA2818XAAAAA
A3818A	A3818A – PCIe 1 Optical Link	WA3818AXAAAA
A3818B	A3818B – PCIe 2 Optical Link	WA3818BXAAAA
A3818C	A3818C – PCIe 4 Optical Link	WA3818CXAAAA
Accessories	**Description**	**Product Code**
A317	Clock Distribution Cable	WA317XAAAAAA
A318	SE to Differential Clock Adapter	WA318XAAAAAA
A654	Single Channel MCX to LEMO Cable Adapter	WA654XAAAAAA
A654 KIT4	4 MCX TO LEMO Cable Adapter	WA654K4AAAAA
A654 KIT8	8 MCX TO LEMO Cable Adapter	WA654K8AAAAA
A659	Single Channel MCX to BNC Cable Adapter	WA659XAAAAAA
A659 KIT4	4 MCX TO BNC Cable Adapter	WA659K4AAAAA
A659 KIT8	8 MCX TO BNC Cable Adapter	WA659K8AAAAA
AI2730	Optical Fibre 30 m simplex	WAI2730XAAAA
AI2720	Optical Fibre 20 m simplex	WAI2720XAAAA
AI2705	Optical Fibre 5 m simplex	WAI2705XAAAA
AI2703	Optical Fibre 30 cm simplex	WAI2703XAAAA
AY2730	Optical Fibre 30 m duplex	WAY2730XAAAA
AY2720	Optical Fibre 20 m duplex	WAY2720XAAAA
AY2705	Optical Fibre 5 m duplex	WAY2705XAAAA

Tab. 1.1: Table of models and related items

2 Block Diagram

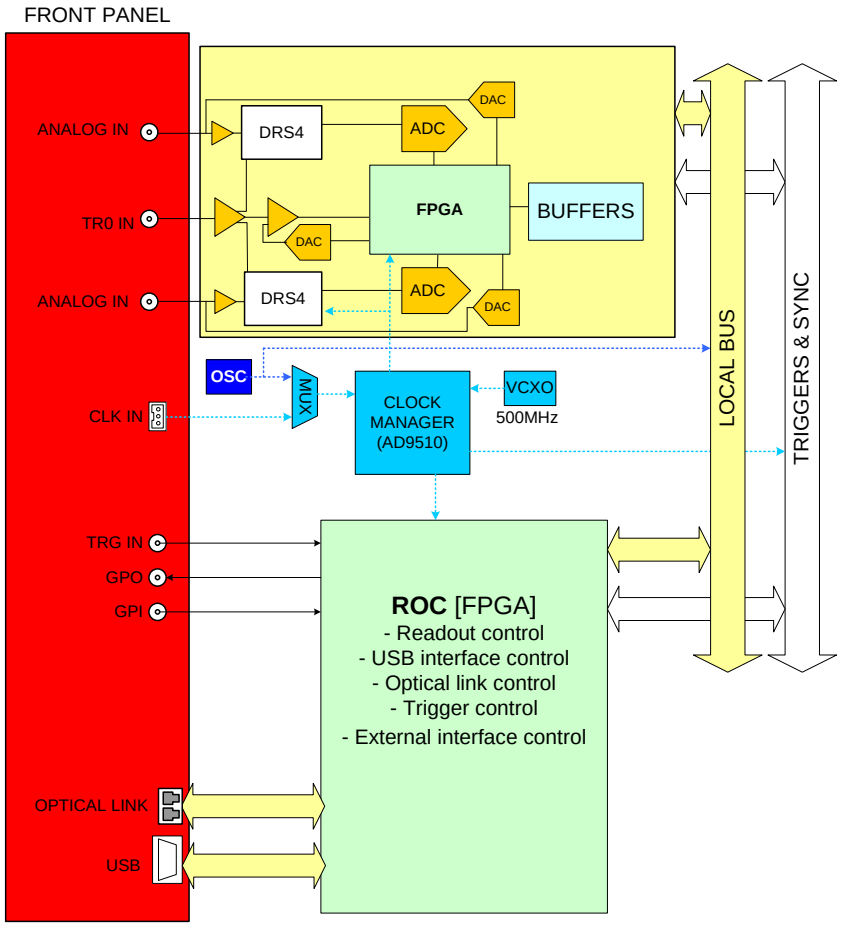

Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor**: 1-unit wide NIM		
ANALOG INPUT	**Channels** 16 channels 1 special channel (TR0) Single ended **Impedance** Z_{in} = 50 Ω	**Connector** MCX **Full Scale Range (FSR)** 1 V_{pp}	**Bandwidth** 500 MHz **Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ± 1 V
DIGITAL CONVERSION	**Resolution** 12 bits **Switched Capacitor Array** Domino Ring Sampler chip (DRS4), 8+1 channels with 1024 storage cells each	**Sampling Rate** 5 GS/s - 2.5 GS/s - 1 GS/s - 0.75 GS/s SW selectable, simultaneously on each channel	**Dead Time (A/D Conversion)** 110 µs, analog inputs only 181 µs, digitizing TR0
ADC CLOCK GENERATION	Clock source: internal/external. On-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Jitter < 100 ppm requested	**GPO (LEMO)** Trigger digital output NIM/TTL Z_{in} = 50 Ω **TRG-IN (LEMO)** External trigger digital input NIM/TTL Z_{in} = 50 Ω	**GPI (LEMO)** SYNC/START front panel digital input NIM/TTL Z_{in} = 50 Ω
MEMORY	128 events/ch or 1024 events/ch (1024 S/event) Multi-event Buffer Independent read and write access; programmable event size and pre/post-trigger		
TRIGGER	**Trigger Source** - *Fast (Low Latency) trigger*: Common trigger by programmable threshold on TR0 - *Self-trigger*: Common trigger by combination of channels over/under threshold in logic OR - *External-trigger*: Common trigger by TRG IN connector - *Software-trigger*: Common trigger by software command		**Trigger Propagation** GPO programmable digital output **Trigger Time Stamp** 30-bit counter 8.5 ns resolution 9 s range
SYNCHRONIZATION	**Clock Propagation** *One-to-many*: clock distribution from an external clock source on CLK-IN connector		**Acquisition Synchronization** Sync, Start/Stop through digital I/O (GPI or TRG-IN input / GPO output) **Trigger Time Stamps Alignment** By GPI input connector
ADC & MEMORY CONTR.	Altera Cyclone EP3C16 (one FPGA manages 16+1 channels)		
COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)		**USB** USB 2.0 compliant Up to 30 MB/s transfer rate
FIRMWARE UPGRADE	Firmware can be upgraded via USB/Optical Link		

SOFTWARE UPGRADE	General purpose C libraries, configuration tools, readout software (Windows and Linux support)
POWER CONSUMPTIONS	3.9 A @ +6V, 90 mA @ -6V

Tab. 3.1: Specification table

4 Packaging and Compliancy

The module is housed in a single-width NIM unit.

Fig. 4.1: Front view

Fig. 4.2: Size view

CAUTION: to manage the product, consult the operating instructions provided.

A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!

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CAEN provides the specific document “Precautions for Handling, Storage and Installation”, available in the documentation tab of the product’s web page, that the user is mandatory to read before to operate with CAEN equipment.

5 Power Requirements

The table below resumes the N6742 power consumptions per relevant power supply rail.

MODULE	SUPPLY VOLTAGE	
	+6 V	-6 V
N6742	3.9 A	90 mA

Tab. 5.1: Power requirements table

6 Panels Description

Fig. 6.1: Front panel view

Front Panel

ANALOG INPUT

FUNCTION
Input connectors from CH0 to CH15 receive the input analog signals.
TR0 connector receives the fast (low latency) trigger, and it can also be digitized

MECHANICAL SPECS
Series: MCX connectors.
Type: CS 85MCX-50-0-16.
Manufacturer: SUHNER
Suggested plug: MCX-50-2-16 type.
Suggested cable: RG174 type.

ELECTRICAL SPECS
Input dynamics:
- 1 V_{pp} for CH0-CH15;
- 2 V_{pp} for TR0 (PCB Rev $\geq$ 1);
- 3 V_{pp} for TR0 (PCB Rev = 0)

Input impedance (Zin): 50 Ω.
Absolute max analog input voltage (for 1Vpp FSR): 3Vpp (with Vrail max +3V or - 3V) for any DAC offset in single ended configuration.

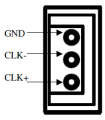
CLOCK IN

FUNCTION
Input connector for the external clock.

ELECTRICAL SPECS
Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML). CAEN provides single ended-to-differential A318 cable adapter (see **Tab. 1.1**) for CLK-IN.
Coupling: AC (CLK-IN); DC (CLK-OUT).
Z_{diff}: 100 Ω.

MECHANICAL SPECS
Series: AMPMODU connectors.
Type: 3-102203-4 (3-pin).
Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

GPO

FUNCTION
General purpose programmable digital output connector to propagate:

- the internal trigger sources;
- the channel probes (i.e. signals from the mezzanines);
- GPI signal

according to register addresses 0x8110 and 0x811C, or

- the motherboard probes (i.e. signals from the motherboard), like the Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal or Busy signal

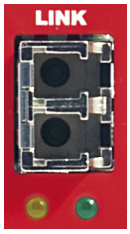
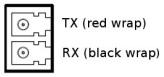
according to register address 0x811C.

ELECTRICAL SPECS
Signal level: NIM or TTL.
Requires 50 Ω termination.

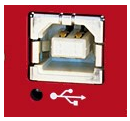
MECHANICAL SPECS
Series: 101 A 004 connectors.
Type: DLP 101 A 004-28.
Manufacturer: FISCHER.
Alternatively:
Type: EPL 00 250 NTN.
Manufacturer: LEMO.

TRG-IN		
	**FUNCTION** Digital input connector for the external trigger. **ELECTRICAL SPECS** Signal level: NIM or TTL. Input impedance (Z_{in}): 50 Ω.	**MECHANICAL SPECS** Series: 101 A 004 connectors. Type: DLP 101 A 004-28. Manufacturer: FISCHER. **Alternatively**: Type: EPL 00 250 NTN. Manufacturer: LEMO.

GPI		
	**FUNCTION** General purpose programmable input connector. Can be used to reset the time stamp (see **Sect. Timer Reset**) or to start/stop the acquisition. **ELECTRICAL SPECS** Signal level: NIM or TTL. Input impedance (Z_{in}): 50 Ω.	**MECHANICAL SPECS** Series: 101 A 004 connectors. Type: DLP 101 A 004-28. Manufacturer: FISCHER. **Alternatively**: Type: EPL 00 250 NTN. Manufacturer: LEMO.

OPTICAL LINK PORT		
	**FUNCTION** Optical LINK connector for data readout and flow control. Daisy chainable. Compliant with Multimode 62.5/125 µm cable featuring LC connectors on both sides. **ELECTRICAL SPECS** Transfer rate: up to 80 MB/s.	**MECHANICAL SPECS** Series: SFF Transceivers. Type: FTLF8519F-2KNL (LC connectors). Manufacturer: FINISAR. **PINOUT** 

LINK LEDs (GREEN/YELOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

USB PORT		
	**FUNCTION** USB connector for data readout and flow control. **ELECTRICAL SPECS** Standard: compliant with USB 2.0 and USB 1.0. Transfer rate: up to 30 MB/s.	**MECHANICAL SPECS** Series: USB connectors. Type: 787780-2 (B-Type). Manufacturer: AMP Inc.

USB LINK LED (GREEN): indicates the USB communication is active.

DIAGNOSTICS LEDs	
	**TTL (GREEN)**: indicates the standard TTL is set for GPO, TRG IN, GPI; **NIM (GREEN)**: indicates the standard NIM is set for GPO, TRG IN, GPI; **PLL LOCK (GREEN)**: indicates the PLL is locked to the reference clock; **PLL BYPS (GREEN)**: indicates the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off; **RUN (GREEN)**: indicates the acquisition is running (data taking). See **Sect. Acquisition Run/Stop**; **TRG (GREEN)**: indicates the trigger is accepted; **DRDY (GREEN)**: indicates the event/data is present in the Output Buffer; **BUSY (RED)**: indicates all the buffers are full for at least one channel.

LABELS	
	A blue label on top of the NIM front panel indicates: - Manufacturer name and functional name - Module name and the input range information
	A little silver label on the bottom of the NIM front panel reports: - Serial Number (S/N)

7 Functional Description

Analog Input Stage

The input dynamic is 1 V_{pp} on single ended MCX coaxial connectors (Z_{in} = 50 Ω). A 16-bit DAC allows to add up to ± 1 V DC offset in order to preserve the full dynamic range also with uni-polar, positive, and negative input signal. The input bandwidth ranges from DC to 500 MHz.

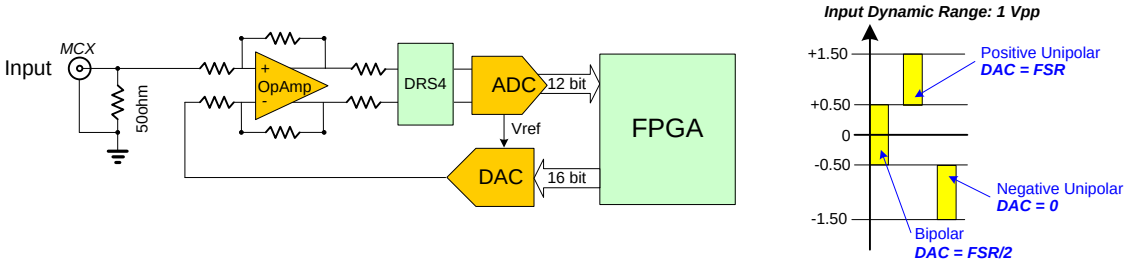


Fig. 7.1: Analog input diagram

An additional channel is available on the TR0 connector. The TR0 can act as a fast trigger (refer to **Sect. TR0 Input**) and it can also be digitized and saved into memory. The TR0 appears as the ninth channel of each group in the final readout. The TR0 input dynamics is 2 V_{pp} for Mezzanine PCB revision ≥ 1, and 3 V_{pp} for Mezzanine PCB revision = 0[1]. The input dynamics is then attenuated by a factor of 2 (3 in the latter case) to make it compliant with the 1 V_{pp} dynamics of the other channels. The 16-bit DAC then allows the user to adjust the DC offset making the TR0 suitable for uni-polar, positive, and negative signals.

Domino Ring Sampling

The analog input signals are continuously sampled by the DRS4 (Domino Ring Sampler) chip[2] which consists of an on-chip inverter chain (domino wave circuit) generating a maximum of 5 GS/s sampling frequency; 2.5 GS/s, 1 GS/s, and 750 MS/s frequencies can be also programmed. The board has one chip per group, and each chip consists of 1024 capacitor cells per channel, which perform the analog sampling of the input (high frequency analog sampling). The record length of the acquisition is constrained by the cell number, and it is fixed to 1024 samples. Options 512, 256, and 136 can be selected by software to reduce the amount of data to be transferred, but all the 1024 cells are converted anyway (no dead-time reduction)
The DRS4 chip continuously samples the input in a circular way (samples are overwritten) until a trigger signal stops its acquisition (holding phase). Then the cells release their capacitances at a readout frequency controlled by the FPGA (Output Mode).
The analog samples are digitized by the 12-bit ADC at a frequency of 29.296 MHz (low frequency digital sampling). The ADC output is stored by the FPGA into the Digital Memory Buffer. Data is then available for readout (for the data format refer to **Sect. Event structure**).
The single TR0 is split into the two DRS4 chips (see also **Sect. TR0 Input**). Delay lines are equal in the two paths, anyway small differences in the digitized samples are possible due to differences in the chips and in the ADCs. When the digitization of the TR0 is enabled, there is a double conversion that increases the dead-time from 110 µs when only the inputs are converted to 181 µs when also the TR0 is converted.

[1] To check the PCB revision number, read bit[9] of register 0x1n88 **[RD1]**
[2] Detailed documentation of the DRS4 is available at http://drs.web.psi.ch/

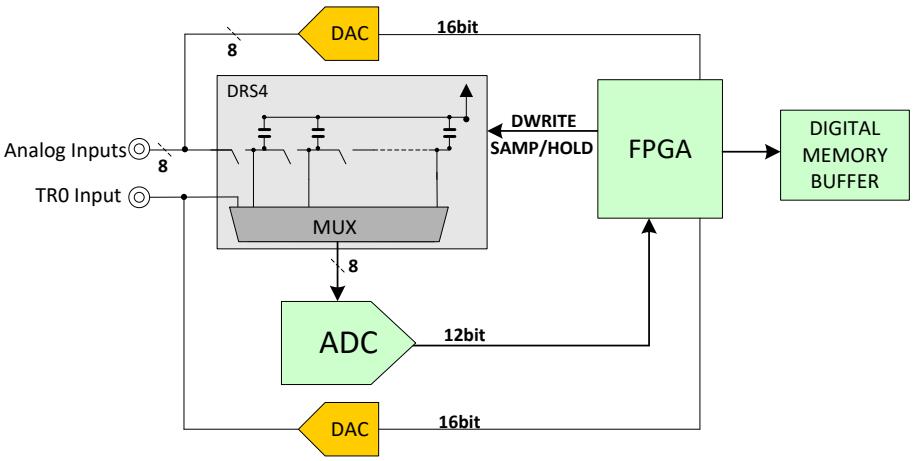


Fig. 7.2: Input Diagram

TR0 Input

The module features one fast trigger input TR0 with extended level amplitude (NIM/LVTTL compliant); TR0 is common to group 0 (ch[7..0]) and group 1 (ch[15..8]). TR0 signal can be used as external trigger (see **Sect. Trigger Management**). Moreover it can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required; this is achieved by setting bit[11]=1 of register 0x8000.

> **IMPORTANT**: The TR0 input is attenuated by a factor of 2 (PCB revision ≥ 1), or 3 (PCB revision 0) to make it compliant with the 1 V_{pp} dynamics of the DRS4 chip. For signals higher than 2 V_{pp} (3 V_{pp}) it is recommended to use an external attenuator.

To properly handle bipolar signals and also unipolar positive or negative signal, a 16-bit DAC allows the user to add a DC offset to TR0; offset value can be programmed via register 0x1nDC.
When the TR0 signal is used as trigger it is processed by an internal comparator, whose threshold can be programmed via register 0x1nD4: when the TR0 crosses the threshold, the FPGA stops the DRS4 acquisition and controls the sample digitalization. Examples of TR0 DC Offset and Threshold are reported in **Sect. Fast ("Low Latency") Trigger**

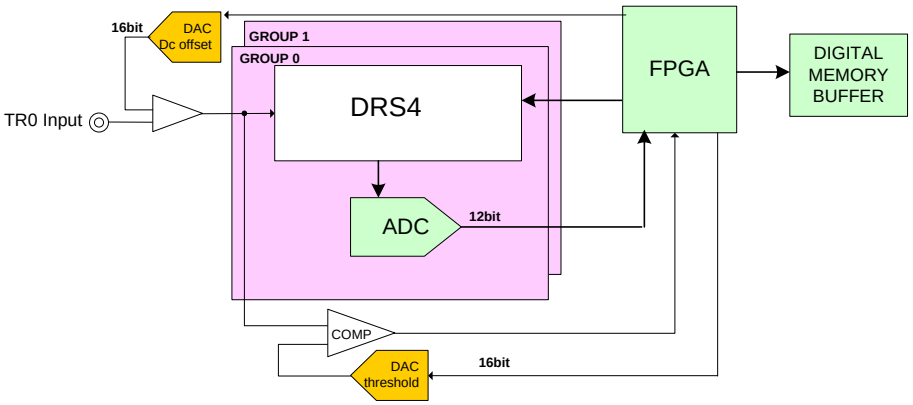


Fig. 7.3: TR0 logic block diagram

Clock Distribution

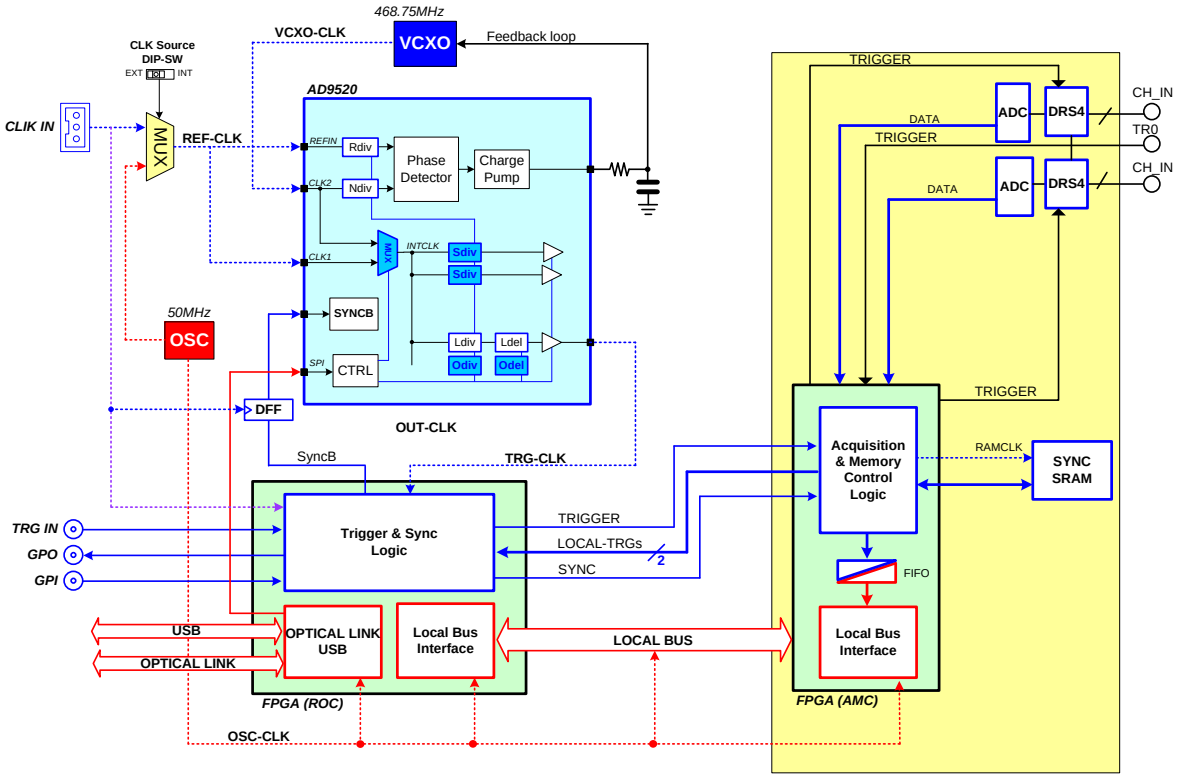


Fig. 7.4: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK, where OSC-CLK is a fixed 50-MHz clock provided by an on-board oscillator, and REF-CLK provides the ADC sampling clock. OSC-CLK handles Local Bus (communication between motherboard and mezzanine boards; see red traces in the above figure).
REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (fed via front panel signal on CLK-IN) or an internal (via local oscillator) source; in the latter case, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).
The board uses an integrated phase-locked-loop (PLL) with a selectable internal or external reference clock source, and a clock distribution device, AD9520, which manages the REF-CLK, and generates the trigger logic synchronization clock (TRG-CLK) and the clock output (OUT-CLK).
Both clocks can be generated from the internal oscillator (50 MHz) or from external clock input. By default, the board uses the internal clock as PLL reference (REF-CLK).
The external clock can be selected by write access at register address 0x8100 (**[RD1]**). The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100ppm (see **Tab. 3.1**).
AD9520 configuration can be changed and stored into non-volatile memory. Changing the AD9520 configuration is primarily intended to be used for external PLL reference clock frequency change.
N6742 locks to an external 50 MHz clock with default AD9520 configuration (see **Sect. PLL Mode**). Refer to the AD9520 datasheet for more details:
http://www.analog.com/static/imported-files/data_sheets/AD9520-3.pdf
(in case the active link above does not work, copy and paste it on the internet browser)

PLL Mode

The Phase Detector within the AD9520 device allows to couple REF-CLK with a VCXO (500 MHz frequency) providing out the nominal ADCs frequency; for this purpose, it is necessary that REF-CLK is a submultiple of the VCXO frequency.
As introduced in **Sect. Clock Distribution**, the source of the REF-CLK signal (see **Fig. 7.4**) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator. The following options are allowed:

1. 50 MHz internal clock source – This is the standard operating mode, where the default AD9520 configuration does not require to be changed. OSC-CLK = REF-CLK.
2. 58.594 MHz external clock source – In this case, the user is required to program the AD9520 dividers to lock the VCXO to REF-CLK. CLK-IN = REF-CLK. Please contact CAEN (**Sect. Technical Support**) to receive the PLL programming file. The PLL programming can be achieved through the CAENUpgrader tool **[RD2]**.
3. External clock source different from 58.594 MHz – In this case, the user is required to program the AD9520dividers to lock the VCXO to REF-CLK. In principle, the allowed external frequencies are submultiples of the VCXO frequency (468.75 MHz). CLK-IN = REF-CLK. Please contact CAEN (see **Sect. Technical Support**) indicating the required reference clock frequency to check its feasibility and receive the PLL programming file.

Data correction

The DRS4 chip needs data corrections because of the unavoidable differences in the chip construction process. The corrections are managed at software level, since the firmware on-board retrieves the raw data. There are three available corrections:

1. Cell Index Offset correction, which compensates the signal offset for the differences in cell amplitudes;
2. Sample Index Offset correction, which corrects the signal offset for a noise over the last 30 samples;
3. Time correction, which compensates the differences of the delay line of the chips.

The default correction tables are provided by CAEN in the memory flash of the board. Wavedump software **[RD3]** (and the underlying CAENDigitizer library **[RD4]**) then can retrieve the tables and make the appropriate corrections.
The user can leave the software automatically apply all the corrections, or decide which correction applies to which group through the CORRECTION_LEVEL function of WaveDump.
If the user wants to apply its own corrections, he/she can use the CAENDigitizer function GetCorrectionTable **[RD4]** to retrieve the default correction files from the board and modify them with his/her own values.
The list of CAENDigitizer functions to be used on-line are:

- **LoadDRS4CorrectionData**, loads the correction parameters stored on board. The correction parameters to load depend on the operating sampling frequency.
- **DecodeEvent**, decode the event and apply the correction to data if LoadDRS4CorrectionData has been previously called.
- **Enable/Disable DRS4Correction**, enables/disables the data correction in the x742 series. When enabled, the data correction through the DecodeEvent function only applies if LoadDRS4CorrectionData has been previously called, otherwise the DecodeEvent runs the same, but data will be provided out not compensated.
- **GetCorrectionTables**, reads the correction tables from the x742 digitizer flash memory, related to the selected sampling frequency, and fills in a structure with the read values. In this way, the stored correction table become available for the user.

Finally, it is also possible to save the raw data and apply the corrections off-line. An example code is available in the CAENDigitizer library. To access the code, download and install the CAENDigitizer library (the prior installation of CAENVMElib **[RD5]**, **[RD6]**and CAENComm library **[RD7]** are required) and include the examples in the installation. Then access to the subfolder called ”x742_DataCorrection”.
C:/Program Files/CAEN/Digitizers/Library/Samples/x742_DataCorrection
Here the list of CAENDigitizer functions **[RD4]** to be used off-line.

- **LoadCorrectionTables**, loads the correction tables stored onto the board into a user defined structure.
- **ApplyDataCorrection**, applies the desired correction data (configured through a mask) to the raw data acquired by the user.
- **GetNumEvents**, gets the current number of events stored in the acquisition buffer.
- **GetEventPtr**, retrieves the event pointer of a specified event in the acquisition buffer.
- **X742_DecodeEvent**, decodes a specified event stored in the acquisition buffer writing data in Evt memory.

Cell Index Offset correction

The analog capacitors of the DRS4 chip might have small differences between each other due to the construction processes. According to the cell index where the stop acquisition arrives, the same input signal can be reconstructed in different ways. For this reason it is required a cell amplitude calibration to compensate for the amplitude differences in the capacitors. The correction adjusts the baseline of the input (i.e. its offset).
Taking into account the internal noise of each channel, **Fig. 7.5** shows the sampled waveform on the left and the noise distribution histogram on the right, measured as the occurrence of the ADC counts. Plots are made before the correction. **Fig. 7.6** shows the same quantities after the correction. As expected, the noise in **Fig. 7.6** is flatter with no patterns, and its distribution has a smaller RMS.

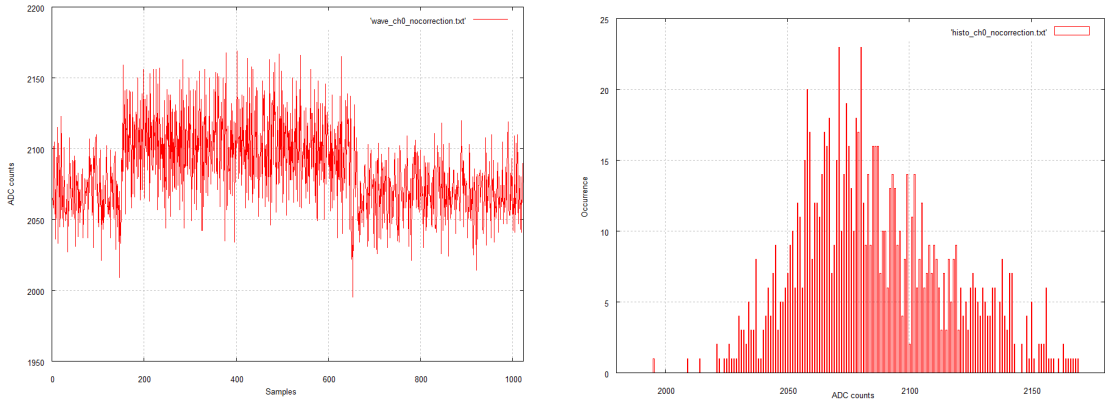


Fig. 7.5: Sampled waveform (left) and noise histogram (right) before cell index offset correction

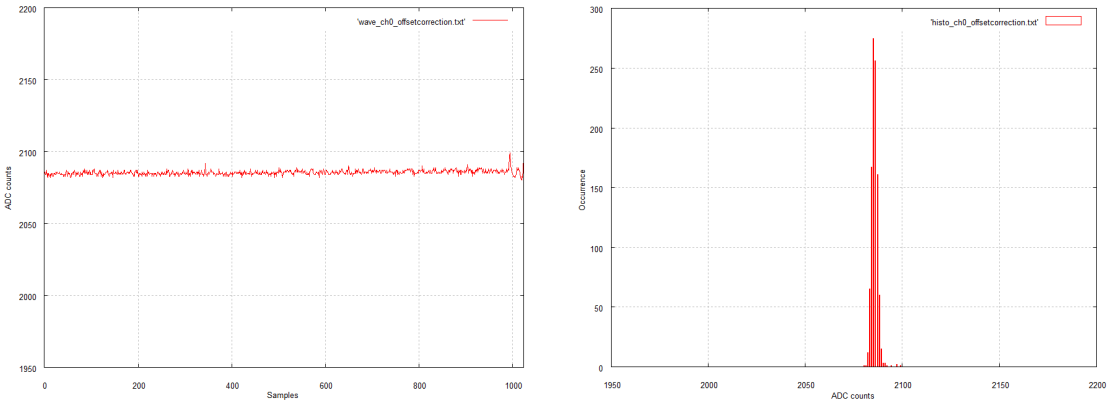


Fig. 7.6: Sampled waveform (left) and noise histogram (right) after cell index offset correction

Sample Index Offset correction

From **Fig. 7.6** it is possible to see a fixed pattern over the last about 30 samples of the waveform. Therefore it is required to perform an additional calibration, called ”Sample Index”, that corrects for the latest samples.
Fig. 7.7 shows the result on the baseline after the correction, where the pattern on the latest samples has been corrected.

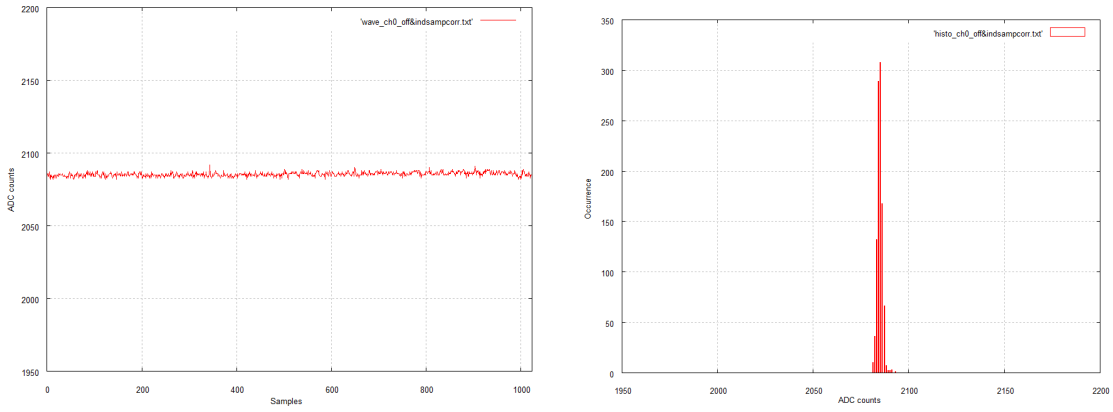


Fig. 7.7: Sampled waveform (left) and noise histogram (right) after sample index offset correction

Time correction

The sampling sequence is handled by the DRS4 through 1024 physical delay lines; the unavoidable construction differences between such delay lines must be compensated through a time calibration.
Fig. 7.8 and **Fig. 7.9** show the fast trigger signal (TR0) sampled by the DRS4 chip related to Group 0 and Group 1, before and after the time correction respectively. High discrepancies can be seen before the correction, while the differences after the correction are extremely reduced.
To measure the differences between the data and the ideal time value of the DRS4 chip, the Integral Non-Linearity (INL) has been calculated and reported in **Fig. 7.10** and **Fig. 7.11** before and after the correction respectively. As expected, the INL shows a better agreement after the correction.

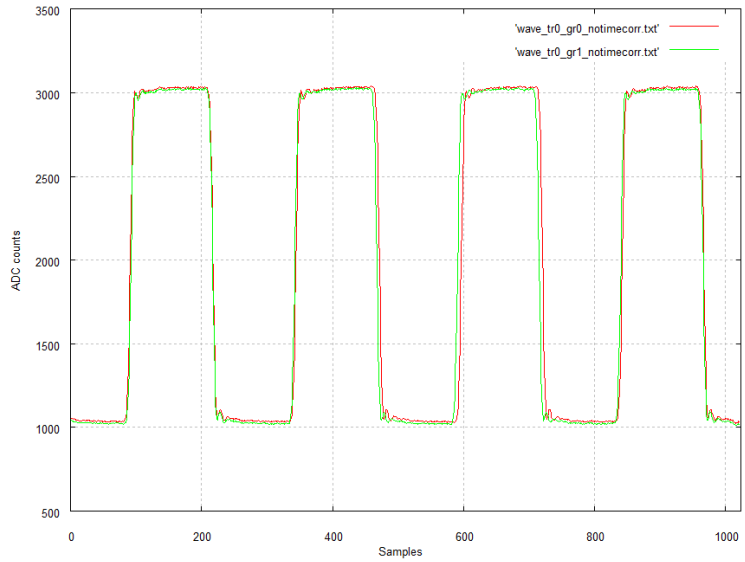


Fig. 7.8: Sampled TR0 signal in GR0 and GR1 before time correction

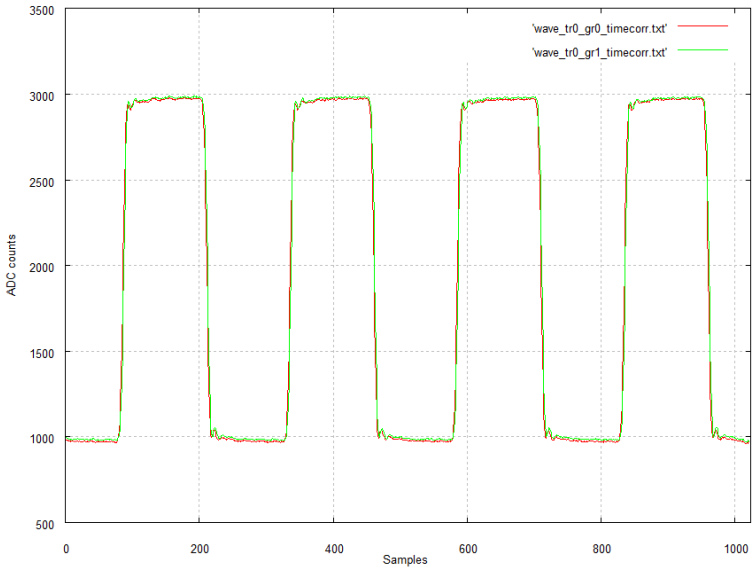


Fig. 7.9: Sampled TR0 signal in GR0 and GR1 after time correction

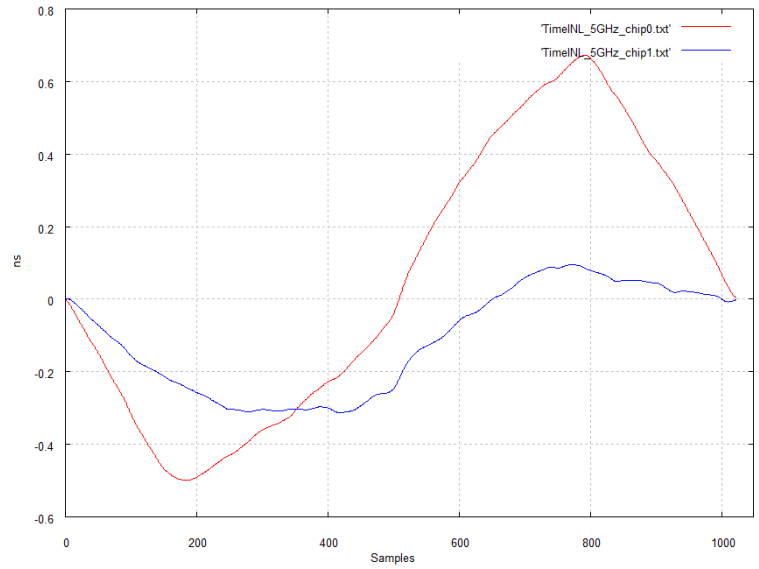


Fig. 7.10: INL time profile of DRS4 chips 0 and 1 before time correction

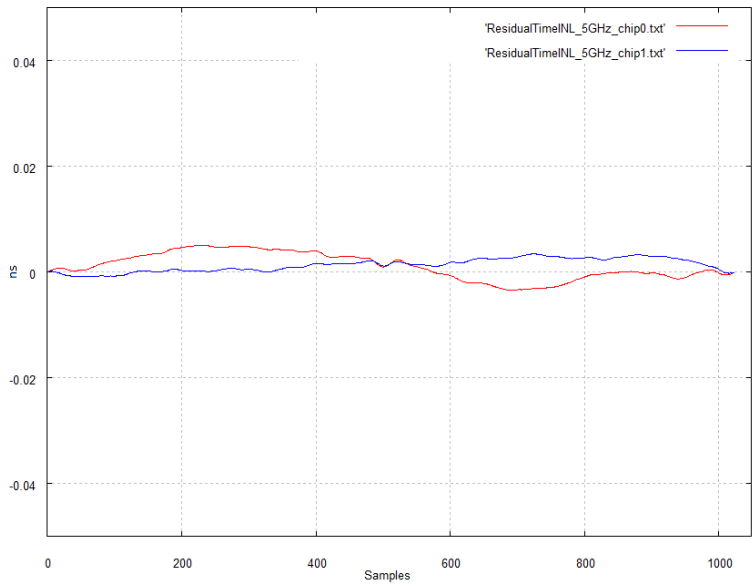


Fig. 7.11: INL time profile of DRS4 chips 0 and 1 after time correction

Acquisition Modes

Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[2:0] of register 0x8100:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): bit[2] = 1 arms the acquisition and the Start is issued as the S-IN signal is set high and the Stop occurs when it is set low. If bit[2] = 0 (disarmed), the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).

Event structure

The event can be readout via USB or Optical Link; data format is 32-bit long word (see **Fig. 7.12**).
An event is structured as:

- Header (four 32-bit words)
- Data (variable size and format)

The Header is composed by four words, namely:

- **TOTAL EVENT SIZE** (Bit[27:0] of 1st header word), this is the total size of the event, i.e. the number of 32-bit long words to be read;
- **BOARD FAIL FLAG** (Bit[26] of 2nd header word) = Implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), this bit is set to "1" in consequence of a hardware problem (e.g. PLL unlocking or over-temperature condition). The user can collect more information about the cause by reading at register address 0x8104 and contact CAEN Support Service if necessary (see **Sect. Technical Support**);
- **GROUP MASK** (Bit[1:0] of the 2nd header word) = It is the mask of the groups participating to the event. This information must be used by the software to retrieve from which groups the samples belong. For example, in case of events from GR1, GROUP MASK = 0x2, in case of events from GR0 and GR1, GROUP MASK = 0x3.
- **EVENT COUNTER** (Bit[23:0] of 3rd header word) : It is the trigger counter; it can count either accepted triggers only, or all triggers.
- **EVENT TIME TAG** (4th header word): it is a 31-bit counter and the 32nd bit as roll over flag; the counter is reset when the acquisition starts or by an external signal (see **Sect. Timer Reset**) and it is incremented at each trigger clock hit. It corresponds to the time when the event is created in the digitizer memory and it does not correspond to any physical quantity.

Note: The physical time of arrival of the pulse can be read in the Group Trigger Time Tag.

After the header, the data from the enabled groups is reported consecutively. The group data format for group 0 is reported in **Fig. 7.13**.

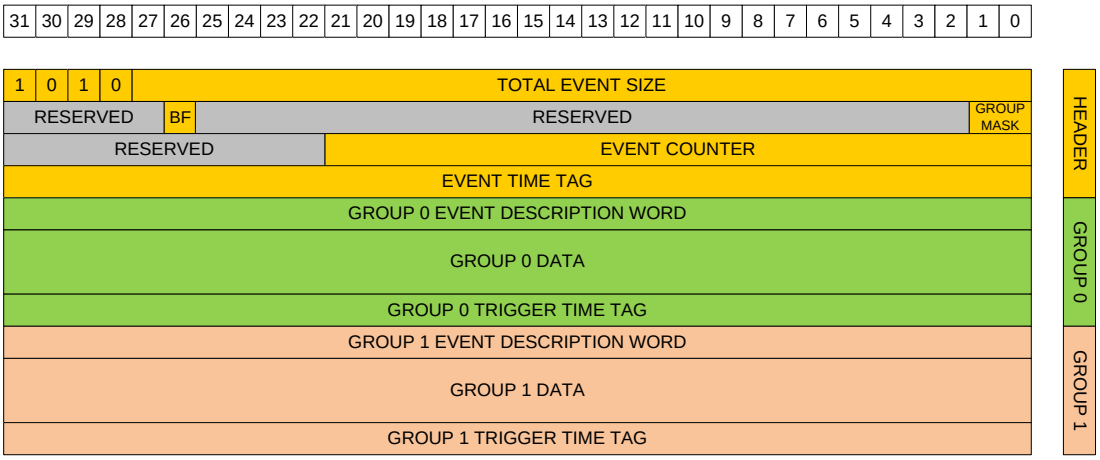


Fig. 7.12: Event Format

Each group is composed by 8 channels (group 0 = channel 0 – 7, group 1 = channel 8 – 15) and by the special channel TR0: such signal is common to two groups; it can be used as Local Trigger or "digitized" and stored with the data for high resolution timing analysis between the ADC channels and the TR0 itself (refer to **Sect. TR0 Input**).

Note: TR0 is split into the two DRS4 of the mezzanine and follows two different path (two different ADCs and two memory buffers). This might imply that the digitized samples of TR0 might have small differences from one group to the other.

TR0 can trigger both Group 0 and Group 1 and it is stored in both group data (referring to **Fig. 7.13** the label $TR0_0$ indicates that the TR0 is saved into group 0).

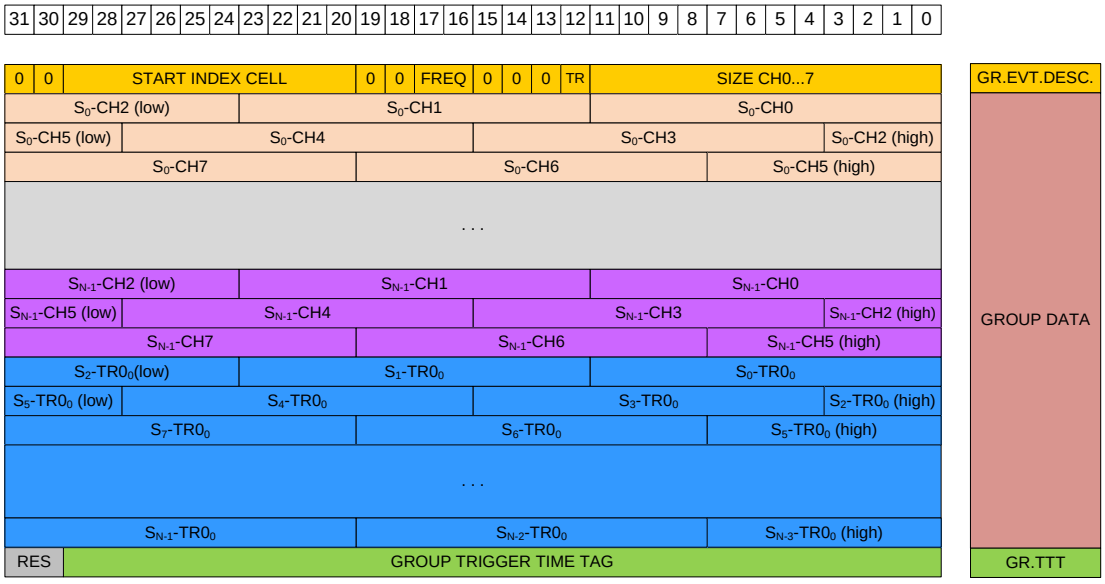


Fig. 7.13: Group Data Format

In the **Group Event Description** word (yellow in the figure) the following fields are shown:

- **START INDEX CELL** (Bits[29:20]), it is the index cell of the DRS4 chip, corresponding to the first sample of the event;
- **FREQ** (Bit[17:16]), it is the sampling frequency of the DRS4 chip, whose options are:
  - 00 = 5 GS/s;
  - 01 = 2.5 GS/s;
  - 10 = 1 GS/s;
  - 11 = 750 MS/s.
- **TR** (Bit[12]), indicates whether the TR0 has been digitized and it is available in the readout. Options are:
  - 0 = TR0 signal not present in the readout
  - 1 = TR0 signal present in the readout
- **SIZE CH0...7** (Bit[11:0]). It is the number of words to be read for the CH0...7 samples. Considering that each channel has 1024 samples, and that one sample is written in three words, “SIZE CH0...7” is 0xC00.

The **GROUP DATA** corresponds to the waveform samples, where each sample is reported from the lowest channel index to the highest.
If the readout of TR0 is disabled, data related to such channel (light blue in **Fig. 7.13**) are not present in the event; if readout of TR0 is enabled, data size related to such channel is Size TR0 = (SIZE CH0...7)/8.
The **GROUP TRIGGER TIME TAG** records the Trigger arrival time into a 30-bit number (steps of 8.5 ns). This is the physical trigger information of the event.

Trigger Management

Once a trigger condition is met, the DRS4 chip stops its sampling phase and the analog capacitances are converted (holding phase) by a 12-bit ADC. There are four possible trigger sources:

- **Software Trigger** (common to all enabled groups). The trigger is issued through a software write on the relevant FPGA register. This mode is mainly used for debugging purposes.
- **External Trigger** (trigger on TRG-IN connector, common to all enabled groups). The TRG-IN connector accepts NIM and TTL input logic, which can be programmed via software. More details are in **Sect. External Trigger**.
- **Fast (Low Latency) Local Trigger** (trigger on TR0 connector, common to all enabled groups). This mode is called “Fast” or “Low Latency” since the latency from the trigger arrival and the DRS4 stop acquisition is significantly reduced with respect to the External Trigger mode. See **Sect. Fast (”Low Latency”) Trigger**.
- **Self-trigger** (common to all enabled groups), the acquisition is controlled by combinations in logic OR of the channel self-triggers. See **Sect. Self-Trigger**.

During the analog to digital conversion process, the board cannot handle other triggers. The corresponding dead-time is equal to 110 µs when only the inputs are digitized, and 181 µs when also the TR0 is digitized. **Fig. 7.14** shows the block diagram of the 742 trigger management.

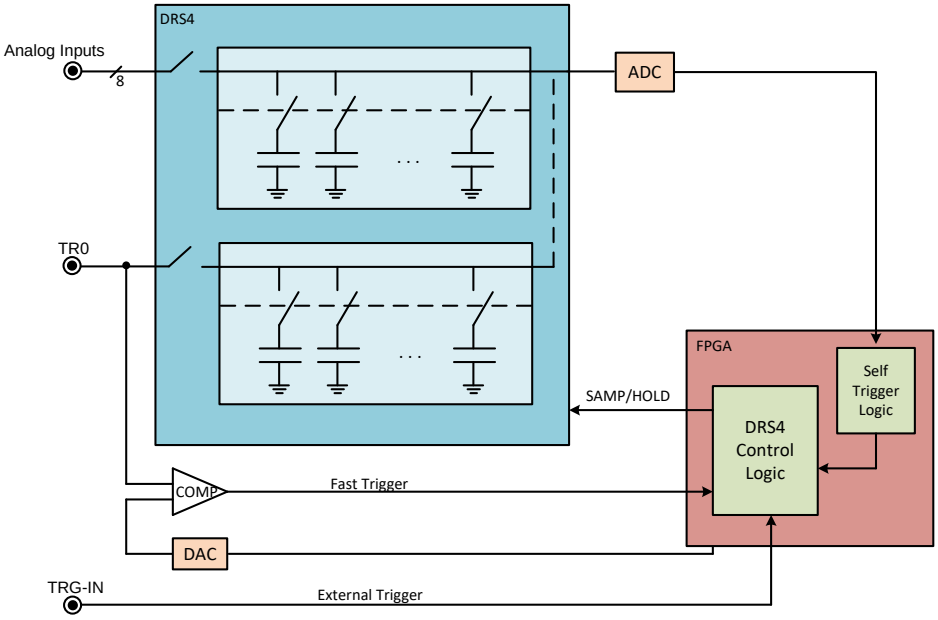


Fig. 7.14: Block diagram of Trigger management

Software Trigger

Software triggers are internally produced via a software command (write access at register address 0x8108) through USB or Optical Link.

External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable at register address 0x811C).
The TRG-IN signal is first processed by the mother board with a clock of about 58 MHz, and sent to the DRS4 to stop its acquisition with a latency of about 115 ns and a jitter of about 17 ns[3]. The latency of the external trigger makes this mode difficult to use at 5 GHz, where the maximum acquisition window is about 200 ns (1024 samples of 200 ps).

Fast ("Low Latency") Trigger

The trigger signal is fed into TR0 connector, and it is common to all enabled groups. The TR0 connector accepts signals with maximum amplitude of 2 V_{pp} in case of Mezzanine PCB revision ≥ 1 (3 V_{pp} in case of Mezzanine PCB revision = 0)[4].

IMPORTANT: The TR0 input is attenuated by a factor of 2 (PCB revision ≥ 1), or 3 (PCB revision 0) to make it compliant with the 1 V_{pp} dynamics of the DRS4 chip. For signals higher than 2 V_{pp} (3 V_{pp}) it is recommended to use an external attenuator.

This mode is called "Fast" or "Low Latency" since the latency from the trigger arrival and the DRS4 holding phase is reduced to about 42 ns with a jitter of about 8.5 ns. The signal on TR0 is sent to a comparator with programmable threshold (no mother-board processing) whose output is sampled at about 117 MHz (twice the external trigger processing). When the TR0 signal crosses the threshold, the acquisition of the DRS4 chip is stopped and the digitalization process starts.
This trigger mode is convenient for high precision timing measurements, since the TR0 can be digitized as the other analog inputs and reported in the output data as channel number 8 of each group. The trigger can therefore be used as a time reference for the input. The DRS4 sampling period becomes the time jitter of the trigger with respect to an input of the same group, which can reach 200 ps in case of sampling at 5 GHz. The resolution in a time of flight measurement reaches up to 50 ps in case of signals and TR0 in the same TR0 group.

Note: TR0 is split into the two DRS4 of the mezzanine and follows two different path (two different ADCs and two memory buffers). This might imply that the digitized samples of TR0 might have small differences from one group to the other.

Since the TR0 acts as an input signal, it is possible to adjust its baseline position (i.e. the 0 Volt) to cover the full scale. This permits the use of several types of signals, bi-polar, negative, and positive. A list of accepted signals is reported in **Tab. 7.1** and **7.2**. The TR0 signal is then sent to a comparator that compares the TR0 to the Trigger Threshold. When TR0 crosses the threshold the trigger is issued.
Tab. 7.1 and **7.2** report few examples of DC Offset and Threshold values (hexadecimal / decimal) for typical signals that can be fed into the TR0 connector. The reported Threshold values allow the user to trigger at half of the signal height.
An example on how to set the TR0 triggering mode is reported in **[RD8]**.

[3] The TRG-IN latency has been reduced to 115 ns from ROC firmware revision 4.07, while for firmware revisions less than 4.07 the latency was 255 ns with a jitter of about 34 ns.

[4] To check the PCB revision number, read bit[9] of register 0x1n88 **[RD1]**

Mezzanine PCB Rev. ≥ 1	
ECL signal on TR0	TR0 DC Offset = 0x55A0 / 21920 TR0 Threshold = 0x6666 / 26214
NIM signal on TR0	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x51C6 / 20934
Negative signal on TR0: V = 0 ÷ -400mV	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x5C16 / 23574
Negative signal on TR0: V = 0 ÷ -200mV	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x613E / 24894
Bipolar signal on TR0	TR0 DC Offset = 0x8000 / 32768 TR0 Threshold = 0x6666 / 26214
TTL on TR0 or Positive signal on TR0: V = 0 ÷ ≥ 2V	TR0 DC Offset = 0xA800 / 43008 TR0 Threshold = 0x6666 / 26214
Positive on TR0: V = 0 ÷ 2V	TR0 DC Offset = 0x91A7 / 37287 TR0 Threshold = 0x6666 / 26214

Tab. 7.1: Examples of DC Offset and Trigger Threshold (in hexadecimal / decimal) for typical signals on TR0 connector. Values are valid for mezzanine PCB revision ≥ 1.

Mezzanine PCB Rev. 0	
NIM signal on TR0	TR0 DC Offset = 0x1000 / 4096 TR0 Threshold = 0x717D / 29053
Negative signal on TR0: V = 0 ÷ -400mV	TR0 DC Offset = 0x1000 / 4096 TR0 Threshold = 0x6E72 / 28274
Bipolar signal on TR0	TR0 DC Offset = 0x1000 / 4096 TR0 Threshold = 0x6C80 / 27776
Positive on TR0: V = 0 ÷ 2V	TR0 DC Offset = 0x4000 / 16384 TR0 Threshold = 0x7158 / 29016

Tab. 7.2: Examples of DC Offset and Trigger Threshold (in hexadecimal / decimal) for typical signals on TRn connector. Values are valid for mezzanine PCB revision 0.

Self-Trigger

The self-trigger mode is available on 742 series from AMC firmware revision 0.4. In self-trigger mode each channel can self-trigger on its own input – leading edge discrimination – and logic OR combinations of the self-triggers enable the groups to acquire at the same time. Refer to register 0x1nA8 **[RD1]** for more details.
The DRS4 chip has two operating modes: "Transparent" and "Output". In Transparent mode (see **Fig. 7.15**), the input pulse is both sampled by the DRS4 capacitors (analog sampling) at high frequency, and made available at the output for the ADC digital sampling at a smaller rate, about 30 MHz. In transparent mode, the output stage is not a pure differential, since it has an offset and it is attenuated with respect to the signal correctly shaped. Transparent mode is the standard operating mode of the DRS4 chip, which continuously samples the input.
In Output mode (see **Fig. 7.16**), the input is no longer sampled and the capacitors hold the acquired samples and send them one at a time to the ADC at a frequency controlled by the FPGA (readout frequency). The Output mode starts when a trigger condition is met (see **Fig. 7.14**). Samples in Output mode are those available in the readout for the user and they are correctly shaped.

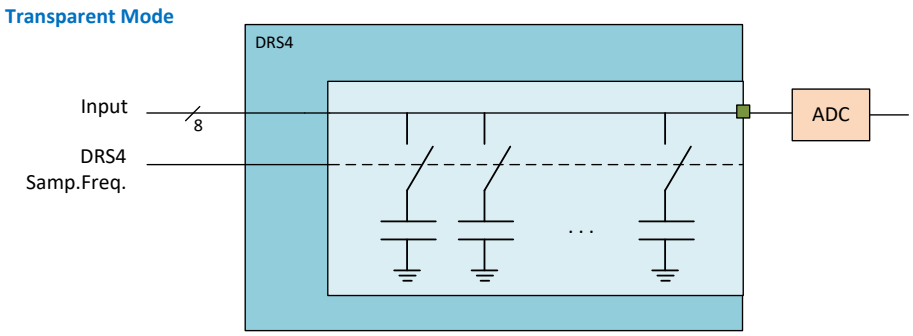


Fig. 7.15: Diagram showing the "Transparent Mode" functioning. The analog input is both sampled by the DRS4 capacitors (analog sampling) and made available at the output for the ADC digital sampling at a smaller rate. The output stage is distorted with respect to the Output mode.

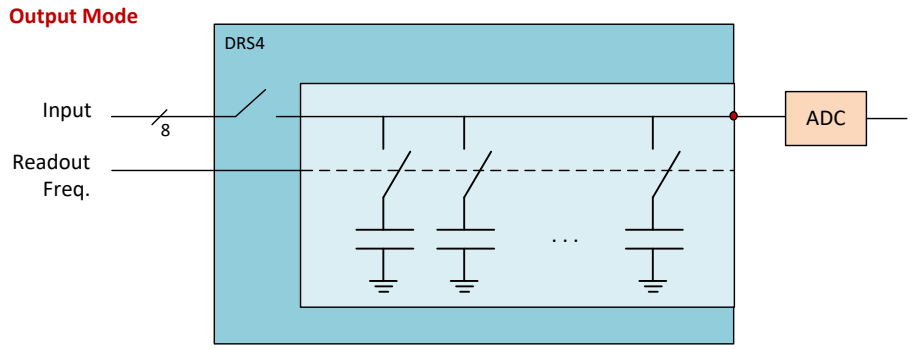


Fig. 7.16: Diagram showing the "Output Mode" functioning. the input is no longer sampled and the capacitors hold the acquired samples and send them one at a time to the ADC at a frequency controlled by the FPGA (readout frequency). The output stage is correctly differential.

Since the Self-Trigger Logic inside the FPGA reads data from the ADC while the DRS4 chip works in Transparent mode, the Trigger Threshold has to be referred to the values read in Transparent mode itself, rather to the values reported in Output mode.
To correctly set the threshold value, it is first required to make an acquisition in Transparent mode to visualize the waveform as sampled by the ADC.

Considering that the ADC frequency is about 30 MHz, it is important that the input can be sampled by the ADC itself. In particular, the pulse width should be greater than 30 ns, and the input frequency should be high enough to visualize some pulses.

IMPORTANT: The procedure of reading from the ADC and processing data by the FPGA introduces a latency of about 250 ns before the DRS4 holding phase. This mode is therefore not compliant with the DRS4 frequency = 5 GHz, but it can be useful when the board works at 2.5 GS/s, 1 GS/s, or 750 MS/s.

How to work with Self-Trigger

To work with the channel self-trigger feature, the board must be configured appropriately according to the following steps.

- Set the DC offset of each channel (at least those which are required to acquire) to ensure that the entire input signal is within the input dynamics of the board. To verify this, it is suggested to make acquisitions in the standard mode ("Output Mode") using the SW trigger.
- Set the board to perform the acquisition in "Transparent Mode" (set bit[13] = 1 of register 0x8000).
- Make acquisitions in "Transparent Mode" using the SW trigger. No corrections are made in Transparent mode. For each channel of interest, check the value of the signal in this acquisition mode and choose the threshold for triggering.
- Set the threshold value for each channel of interest via register 0x1n80, where n is the group index.
- Enable the channels of interest to generate a Channel Trigger via register 0x1nA8.
- Set the board to perform the acquisition in "Output Mode" (set back bit[13] = 0 of register0x8000).

The board is so ready to acquire data when triggers are generated by the channels.
Refer also to **[RD8]** for a practical example and **[RD1]** for the registers description:

Test Pattern Generator

The FPGA can emulate the ADC and write into memory a saw tooth signal for test purposes. It can be enabled via Group Configuration register.
The following figure shows the test waveforms for even and odd groups respectively.

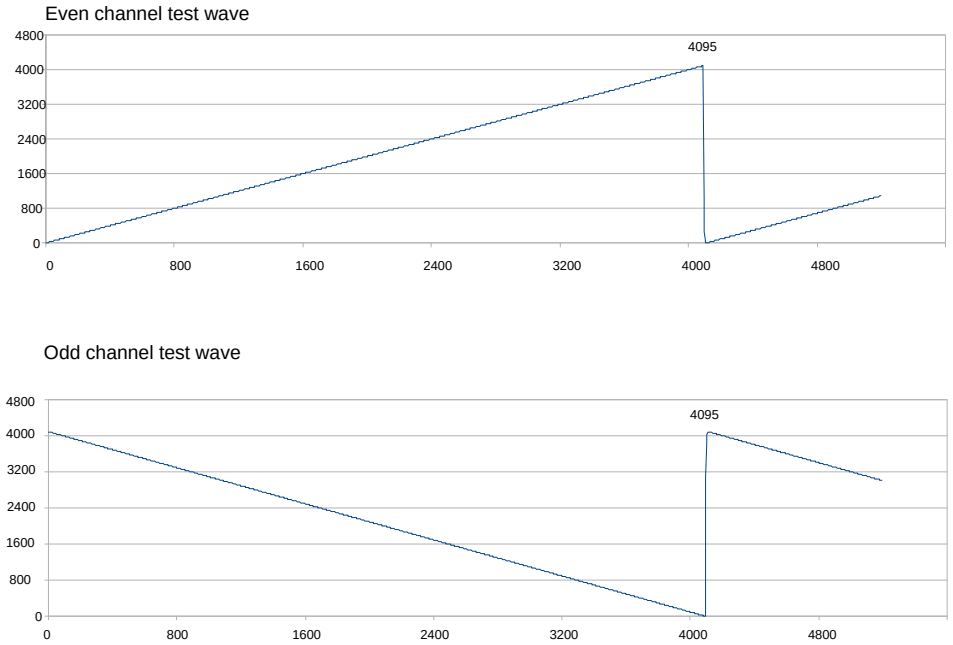


Fig. 7.17: FPGA test waveform

Since an event is made up of up to 1024 samples, the test event samples only a “portion” of the saw tooth; the start point of the sampling can be programmed via Initial Test Wave Value register; for example if this register is set to 0x0FF then the channels in the even groups sample the ramp between 255 and 1278; the channels in the odd groups instead sample the complementary value, therefore between 3840 and 2817.

Reset, Clear and Default Configuration

Global Reset

Global Reset is performed at Power-ON of the module or via software by write access at register address 0xEF24 (whatever 32-bit value can be written). It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Memory Reset

The Memory Reset clears the data off the Output Buffer. The Memory Reset can be forwarded via a write access at register address 0xEF28 (whatever 32-bit value can be written).

Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to the front panel GPI input (leading edge sensitive).

Data Transfer Capabilities and Events Readout

The event, once it is written in the memory, becomes available for the readout via USB or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.
The events are readout sequentially and completely, starting from the Header of the first available event, followed by the samples of the enabled groups as reported in **Fig. 7.12**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.
The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 **[RD1]**, as well as on the number of enabled groups.

Block Transfer

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C **[RD1]**, or by using the SetMaxNumEventsBLT function of the CAENDigitizer library (refer to **[RD4]**).
When developing programs, the readout process can be implemented on different basis :

- Using Interrupts: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link (not supported by USB).
- Using Polling (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using Continuous Read (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C **[RD1]**, or the library function SetMaxNumEventsBLT mentioned above **[RD4]**. If the board is empty, the BLT access is immediately terminated and the "Read Block" function will return 0 bytes (it is the ReadData function in the CAENDigitizer Library, refer to **[RD4]**).

Whatever the method from above, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite of a greater memory allocation required on the host station side that is actually not a real drawback, considering the features of the personal computers available on the market.

Single Data Transfer

This mode allows the user to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in **Sect. Event structure**.
It is suggested, after the 1st word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to read completely the event.

Optical Link and USB Access

The board houses a USB2.0 compliant port, providing a transfer rate up to 30 MB/s, and a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight N6742 to a single Optical Link Controller by using the A2818 PCI card or up to thirty-two N6742 with the A3818 PCIe card. Detailed information on CAEN PCI/PCIe Controllers can be find at www.caen.it:
Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controller
The parameters for read/write accesses via optical link are Address Modifier, Base Address, data Width, etc.; wrong parameter settings cause Bus Error.
Bit[3] at register address 0xEF00 **[RD1]** allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level (see “Interrupt Configuration” in **[RD4]**).

8 Drivers & Libraries

Drivers

In order to interface with the board, CAEN provides the drivers for all the different types of physical communication channels featured by the board and compliant with Windows and Linux OS:

- **USB 2.0** Drivers are downloadable on CAEN website (www.caen.it) in the “Software/Firmware” tab at the N6742 web page (**login required**).

Note: For Microsoft Windows OS, the USB driver installation is detailed in **[RD9]**.

- **CONET Optical Link**, managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the “Software/Firmware” area at the A2818 or A3818 page (**login required**)

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific Controller.

Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason, **the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.
  The CAENDigitizer installation package and relevant documentation are available on CAEN website in the ‘Download’ area at the CAENDigitizer Library page.
- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.
  The CAENComm installation package, the relevant documentation and the link to the required CAENVMELib, are available on CAEN website in the ‘Download’ area at the CAENComm Library page.

CAENComm (and so the CAENDigitizer) supports the following communication channels (**Fig. 8.1**):
PC → USB → N6742
PC → PCI (A2818) → CONET → N6742
PC → PCIe (A3818) → CONET → N6742

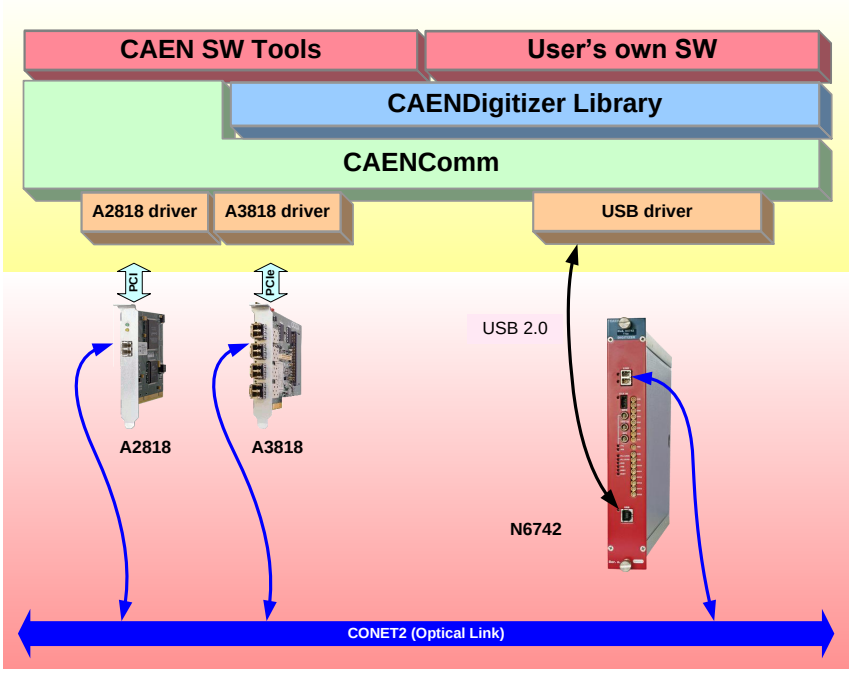


Fig. 8.1: Drivers and software layers

If required to be installed apart by the user (see **Sect. Software Tools**), CAEN Libraries are available for download on CAEN web site (www.caen.it) in the "Download" tab at the library web page:
Home / Products / Firmware/Software / Digitizer Software / Software Libraries / <CAEN Library>
Install first CAENVMELib, then CAENComm library, finally CAENDigitizer library.

9 Software Tools

CAEN provides software tools to interface the 742 digitizer series, which are available for free download on www.caen.it at:
Home / Products / Firmware/Software / Digitizer Software

CAENUpgrader

CAENUpgrader is a free software composed of command line tools together with a Java Graphical User Interface.
Specifically for the x742, CAENUpgrader allows in few easy steps to:

- Upload different FPGA firmware versions on the board
- Read the firmware release of the board and the bridge (when used)
- Manage the firmware license, in case of paid firmware
- Upgrade the internal PLL
- Get the Board Info file, useful in case of support

CAENUpgrader can operate with Windows and Linux, 32 and 64-bit OSs.
The program relies on the CAENComm and CAENVMELib libraries (see **Chapt. Drivers & Libraries**) and requires third-party Java SE6 (or later) to be installed.

Note: Windows version of CAENUpgrader is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be already installed apart by the user.

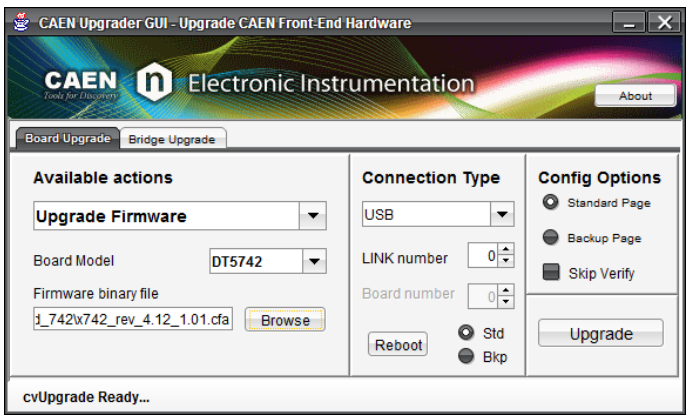


Fig. 9.1: CAENUpgrader Graphical User Interface

CAENUpgrader installation package can be downloaded on CAEN web site (**login required**) at:
Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader
The reference document for installation instructions and program detailed description is **[RD2]**, downloadable at the same page above, in the Documentation tab.

CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java and LabVIEW GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

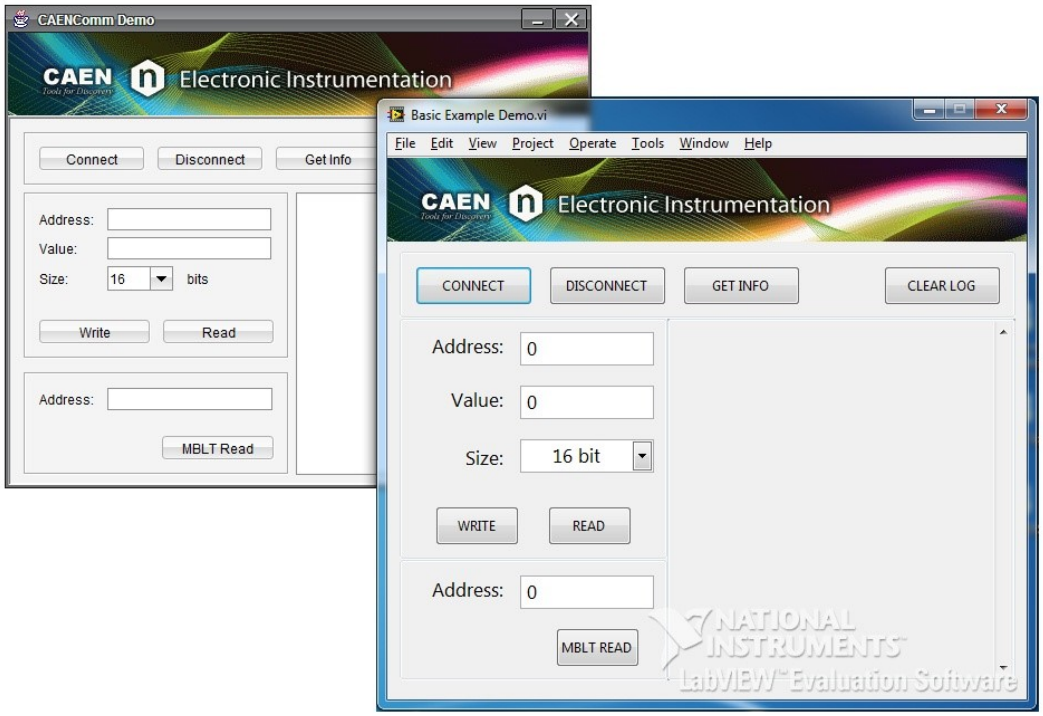


Fig. 9.2: CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo can operate with Windows OSs, 32 and 64-bit. It requires CAENComm and CAEVMElib libraries as additional software to be installed (see **Sect. Drivers** & **Libraries**).
The Demo is included in the CAENComm library installation Windows package, which can be downloaded on CAEN web site (**login required**) at:
Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library

CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the default firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: www.gnuplot.info).
WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

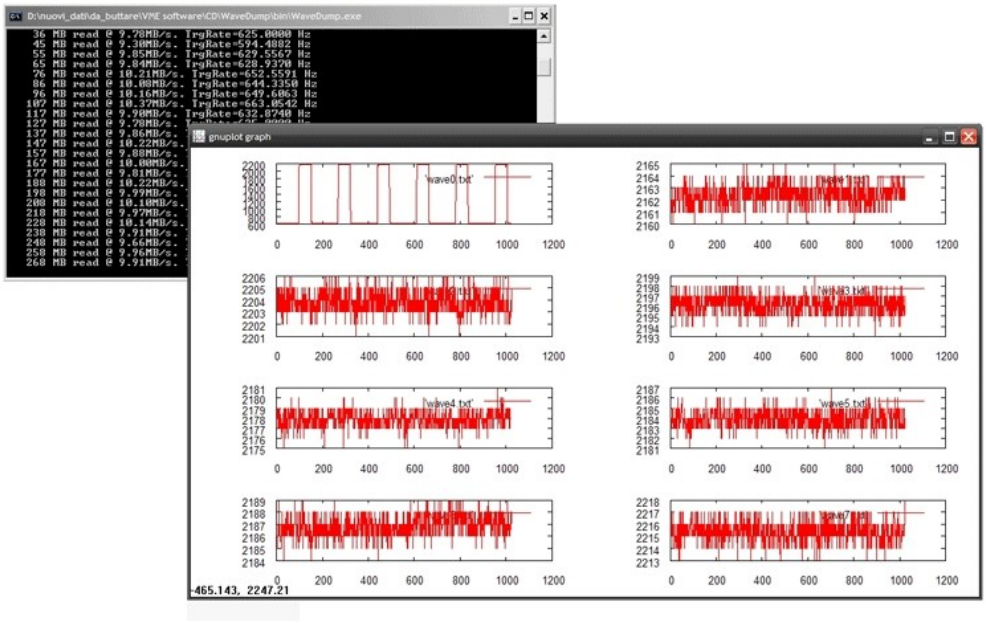


Fig. 9.3: CAEN WaveDump

CAEN WaveDump can operate with Windows and Linux, 32 and 64-bit OSs.
The program relies on the CAENDigitizer, CAENComm and CAENVMELib libraries (see **Sect. Drivers** & **Libraries**). Linux users are required to install the third-party Gnuplot.

Note: Windows version of WaveDump is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be previously installed by the user.

The installation packages can be downloaded on CAEN web site (**login required**) at:
Home / Products / Firmware/Software / Digitizer Software / Readout Software / CAEN WaveDump
The reference documents for installation instructions and program detailed description are **[RD3]**, downloadable at the same page above, in the Documentation tab.

10 HW Installation

- The Module fits into all NIM crates
- **Use only crates with forced cooling air flow**
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

Power-on Sequence

To power on the board, follow this procedure:

1. Insert the N6742 into the crate;
2. power up the crate.

Power-on Status

At power-on the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

After the power-on, the front panel LEDs status is that only the NIM and PLL LOCK remain ON (see **Fig. 10.1**).

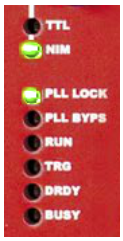


Fig. 10.1: Front panel LEDs status at power ON

11 Firmware and Upgrades

The board hosts one FPGA on the mainboard and four FPGAs on the mezzanine (i.e. one FPGA per 4 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.
ROC FPGA MAINBOARD FPGA (Readout Controller + Communication Interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP4CE30

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of default firmware, the board is delivered equipped with the same firmware version on both pages.
At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one by default in normal operating.
It is possible to upgrade the board firmware via USB or Optical Link by writing the FLASH with the CAENUpgrader software (see **Sect. Software Tools**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!

Default Firmware Upgrade

The N6742 is delivered running a default firmware to operate the board for waveform recording.
The default firmware updates are available for download on CAEN website www.caen.it in the Software/Firmware tab of the N6742 web page (**login required**):
Home / Products / Modular Pulse Processing Electronics / NIM / Digitizers / N6742

Default Firmware File Description

The programming file has the extension .CFA (CAEN Firmware Archive) and is a sort of archive format file aggregating all the default firmware files compatible with one or more digitizer families.
CFA and its name follow this general scheme:

x742_revX.Y_W.Z.CFA

where:

- x742 are all the supported boards: DT5742, N6742, V1742, VX1742
- X.Y is the major/minor revision number of the mainboard FPGA
- W.Z is the major/minor revision number of the channel FPGA

12 Technical Support

CAEN support services are available for the user by accessing the *Support* & *Services* area on CAEN website at *http://www.caen.it*.

Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the *Returns and Repairs* area at *Home / Support* & *Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.
Contacts for shipping are reported on the website at *Home / Contacts*.

Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)

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CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Standards for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

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