Technical Information Manual

Revision n. 12

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MOD. N6740

32 CHANNEL 12 BIT
65 MS/S DIGITIZER

MANUAL REV.12

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Safety Notices

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1. Introduction

This document contains the full hardware description of the N6740 module, and the principle of operating as Waveform Digitizer basing on its default firmware for the waveform recording (hereafter called default firmware).

Referred firmware version: 4.10_0.11.

For any reference to registers in this user manual, please refer to the UM5483 - 740 Family Waveform Recording Firmware Registers document, free downloadable at the digitizer web page.

1.1. Overview

The N6740 is a 1-unit wide NIM module housing a 32 Channel 12 bit 62.5 MS/s (65 MS/s using external clock) Flash ADC Waveform Digitizer with 2 V_{pp} dynamic range (10 V_{pp} available in the version N6740C) on a single ended ERNI SMC input connector.

The A746D Adapter is required for all the 32 channels to be available on as many single-ended LEMO connectors (see § **2.4.1)**.

Because of the high channel density, provided by the AD9222 Octal 12-bit 65 MSPS Analog-to-Digital Converter, most channel settings are performed over “groups” of 8 channels (one group per ADC chip).

The DC offset is adjustable via a 16-bit DAC on each 8-channel group in the ±1 V (@ 2 V_{pp}) or ±5 V (@ 10 V_{pp}) range.

The ADC resolution and the sampling frequency make this digitizer well suited for mid-slow detection systems (e.g. inorganic scintillators coupled to PMTs, gaseous detectors).

Each 8-channel group has a SRAM Multi-Event Buffer divisible into 1 ÷ 1024 buffers of programmable size.

N6740D version (EP3C40 Altera FPGA) supports special Digital Pulse Processing firmware for Charge to Digital conversion (DPP-QDC). A x740D module running DPP-QDC firmware becomes multi-channel data acquisition systems for Nuclear Physics or other applications requiring radiation detection.

A common acquisition trigger signal (common to all the channels) can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, in the default firmware, each 8-channel group can generate a trigger request when at least one of the channels goes under/over a programmable threshold. The requests from the groups are processed by the board to generate the common trigger causing all the channels to acquire an event simultaneously (in the DPP firmware, each channel can trigger independently of the others upon the pulse under/over-threshold; the trigger request is used locally by the channel to acquire the event).

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer

N6740 features a front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multiple N6740 boards can be synchronized to a common clock source ensuring Trigger time stamps alignment. The fan-in of an external clock signal to each CLK-IN is required. Once synchronized, all data will be aligned and coherent across the multi-board system.

The module houses USB 2.0 and Optical Link interfaces. USB 2.0 allows data transfers up to 30 MB/s. The Optical Link (CAEN proprietary CONET protocol) supports transfer rate of 80 MB/s and offers Daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller, or up to 32 using a A3818 (4-link version). Optical Link and USB accesses are internally arbitrated.

Table 1.1: Available items

Code	Description
WN6740XAAAAA	N6740 - 32 Ch. 12 bit 65 MS/s Digitizer: 192kS/ch, EP3C16, SE
WN6740CXAAAA	N6740C - 10Vpp input 32 Ch 12 bit 65 MS/s Digitizer: 192kS/ch, EP3C16, SE
WN6740DXAAAA	N6740D - 32 Ch. 12 bit 65 MS/s Digitizer: 192kS/ch, EP3C40, SE
WFWDPPQDCAAA(*)	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (x740) (*) Multi-license packs are also available. Please, refer to the Digitizer web page for the relevant ordering options.
WA746DXAAAAA	A746D - 32 Ch. Adapter for Lemo connector
WA2818XAAAAA	A2818 - PCI Optical Link
WA3818AXAAAA	A3818 - PCIe 1 Optical Link
WA3818BXAAAA	A3818 - PCIe 2 Optical Link
WA3818CXAAAA	A3818 - PCIe 4 Optical Link
WA318XAAAAAA	A318 - Cable Adapter Single Ended to Differential
WAI2740XAAAA	AI2740 - Optical Fibre 40 m. simplex
WAI2730XAAAA	AI2730 - Optical Fibre 30 m. simplex
WAI2720XAAAA	AI2720 - Optical Fibre 20 m. simplex
WAI2705XAAAA	AI2705 - Optical Fibre 5 m. simplex
WAI2703XAAAA	AI2703 - Optical Fibre 30cm. simplex
WAY2730XAAAA	AY2730 - Optical Fibre 30 m. duplex
WAY2720XAAAA	AY2720 - Optical Fibre 20 m. duplex
WAY2705XAAAA	AY2705 - Optical Fibre 5 m. duplex

1.2. Block Diagram

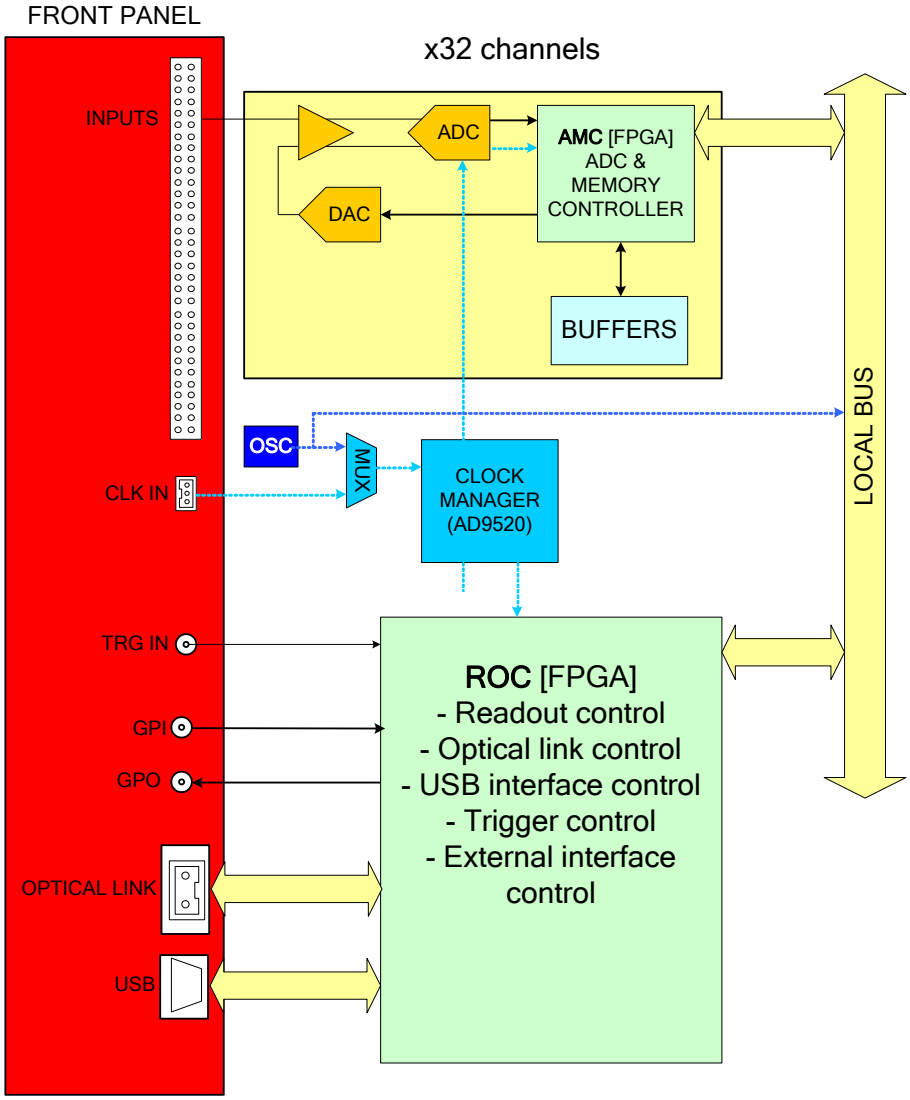

Fig. 1.1: Mod. N6740 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical Specifications

2.1. Packaging and Compliancy

N6740 is housed in a 1-unit wide NIM unit.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

2.2. Power Requirements

The table below resumes the N6740 power consumptions per relevant power supply rail.

Table 2.1: Power requirements

Supply Rail	N6740	N6740D
+6 V	3.9A	*n.a.*
-6 V	420 mA	*n.a.*

2.3. Front Panel

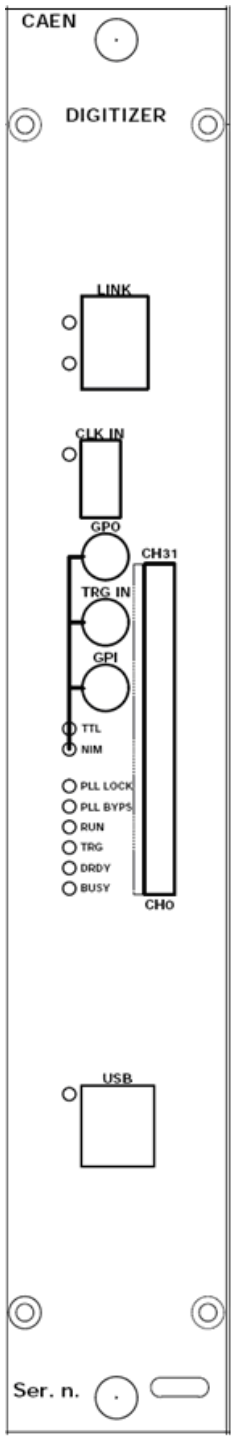

Fig. 2.1: Mod. N6740 front panel

2.4. External Connectors

2.4.1. ANALOG INPUT Connectors

The module has 32 channels on single ended ERNI SMC input connector (see **Fig. 2.2**).

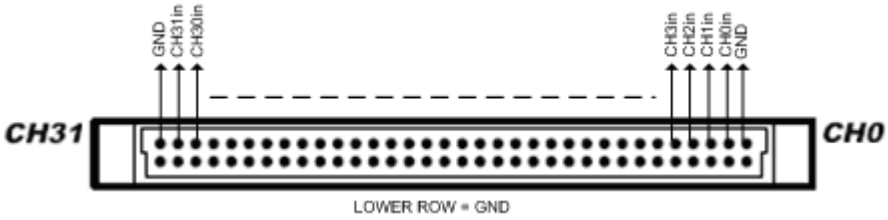

Fig. 2.2: ERNI SMC Connector

Function:
Analog input, single ended, input dynamics: $2V_{pp}$, Z_{in} = 50 Ω (N6740C: $10V_{pp}$, Z_{in} = 1 kΩ).

Mechanical specifications:
ERNI SMC-114805 Dual Row 68pin connector

All 64 channels can be available on as many single-ended LEMO connectors by using the A746D adapter (see **Table 1.1**).

Absolute max analog input voltage (@$2V_{pp}$ FSR) = $6V_{pp}$ (with V_{rail} max to +6V or -6V) for any DAC offset value.

NOTE: ensure that alignment is correct during insertion/extraction operations; incorrect alignment may lead to connector damage.

2.4.2. CONTROL Connectors

Function:

- **GPO:** digital output connector (NIM/TTL, on R_t = 50Ω) to propagate
  - the internal trigger sources;
  - the channel probes (i.e. signals from the mezzanines);
  - GPI signal

  according to register addresses 0x8110 and 0x811C, or
  - the motherboard probes (i.e. signals from the motherboard), like the Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal or Busy signal

  according to register address 0x811C.

- **TRG-IN:** digital input connector (NIM/TTL, Z_{in} = 50Ω) for the external trigger.

- **GPI:** SYNC/START/STOP digital input connector (NIM/TTL, Z_{in} = 50Ω) configurable as time stamp reset (see § **3.5.3**) or acquisition start/stop (see § **3.3.1**).

Mechanical specifications:
00-type LEMO connectors.

2.4.3. ADC REFERENCE CLOCK Connectors

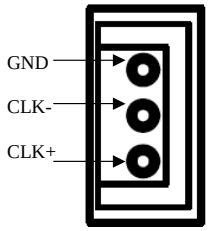

Fig. 2.3: AMP CLK IN Connector

Function:
CLK IN: External clock/Reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Z_{diff} = 100 Ω. CAEN provides single-ended to differential A318 cable adapter (see **Table 1.1**).

Mechanical specifications:
AMP 3-102203-4 AMP MODUII.

2.4.4. Optical LINK Connector

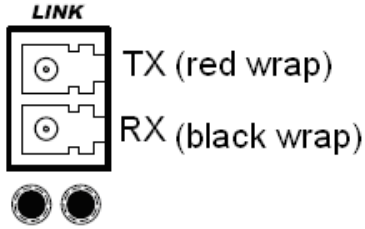

Fig. 2.4: LC Optical Connector

Function:
Optical LINK connector for data readout and flow control (up to 80 MB/s transfer rate). Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides. CAEN provides optical fiber cable selection for A3818 and A2818 Controllers (see **Table 1.1**) with duplex connector on the controller side and two simplex connectors on the digitizer side; the simplex connector with the black wrap is for the RX line (lower) and the one with the red wrap is for the TX (higher).

Mechanical specifications:
SFF Transceiver series, FTLF8519F-2KNL type (LC connectors).

2.4.5. USB Port

Function:
USB connector for data readout and flow control (up tp 30 MB/s transfer rate). Compliant to USB 2.0 and USB 1.1.

Mechanical specifications:
B-type 787780-2 USB connector.

2.5. Other Components

2.5.1. Diagnostic LEDs

The front panel hosts the following LEDs:

Table 2.2: Front panel LEDs

Name:	Colour:	Function:
CLK IN	green	Indicates that the external clock is enabled
TTL	green	Indicates that the standard TTL is set for GPO, TRG-IN and GPI
NIM	green	Indicates that the standard NIM is set for GPO, TRG-IN and GPI
LINK	green/yellow	Network present; Data transfer activity
USB	green	The right green LED indicates the network presence; the left yellow LED signals the data transfer activity
PLL LOCK	green	Indicates that the PLL is locked to the reference clock
PLL BYPS	green	NOT USED
RUN	green	Indicates that the acquisition is running (data taking)
TRG	green	Indicates that the trigger is accepted
DRDY	green	Indicates that the event/data is present in the Output Buffer
BUSY	red	Indicates that all the buffers are full for at least one channel

2.6. Technical Specifications Table

Table 2.3: Mod. N6740 technical specifications

GENERAL	**Form Factor** 1-unit wide NIM module		**Weight** *n.a.*
ANALOG INPUT	**Channels** 32 channels Single-ended **Impedance** Z_{in} = Ω @ $2V_{pp}$ Z_{in} = 1 kΩ @ $10V_{pp}$ *(1) "size1 / size2" denotes different model versions*	**Connector** ERNI SMC Dual Row 68-pin **Full Scale Range** 2 V_{pp} / 10 V_{pp} *(1)*	**Bandwidth** 30 MHz **Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ±1 V (@$2V_{pp}$); ±0.5 V (@$10V_{pp}$)
DIGITAL CONVERSION	**Resolution** 12 bits	**Sampling Rate** 62.5 MS/s simultaneously on each channel 65 MS/s using external clock	
SYSTEM PERFORMANCE	**ENOB** 11.20 (48 kS Buffer) **SINAD** 69.20 dB (48 kS Buffer, open input)	**THD** 87.10 dB **SFDR** 94.9 dB	**SIGMA** 0.50 LSB rms
ADC CLOCK GENERATION	Clock source: internal/external; on-board programmable PLL provides generation of the main board clocks from internal (50 MHz local Oscillator) or external (CLK-IN connector) reference		
I/O CONNECTORS	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter) Jitter<100ppm requested **TRG-IN (LEMO)** External trigger digital input NIM/TTL; Z_{in} = 50 Ω	**GPO (LEMO)** General purpose digital output; NIM/TTL; R_t = 50 Ω **GPI (LEMO)** General purpose digital input NIM/TTL Z_{in} = 50 Ω	
MEMORY	192 kS/ch Multi-event Buffer divisible into 1 ÷ 1024 buffers Independent read and write access; programmable event size and pre-post trigger		
TRIGGER	**Trigger Source** *Self-trigger* channel over/under-threshold for Common (default firmware) or Individual (DPP firmware only) Trigger generation *External-trigger*: Common Trigger by TRG-IN or individual by LVDS (DPP firmware only) connector *Software-trigger*: Common Trigger by software command	**Trigger Propagation** GPO programmable digital output **Trigger Time Stamp** *Default FW*: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension available by firmware *DPP-QDC FW:* 32-bit counter, 16 ns resolution, 68 s range; 48-bit extension by firmware; 64-bit extension by software	
SYNCHRONIZATION	**Clock Propagation** *One-to-many*: clock distribution from an external clock source on CLK-IN connector	**Acquisition Synchronization** Sync, Start/Stop through digital I/O (GPI or TRG-IN input; GPO output) **Trigger Time Stamps Alignment** By GPI input connector	
ADC & MEMORY CONTROLLER	Altera Cyclone EP3C16 or EP3C40 (N6740D only) One FPGA serves 4 channels		

COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)	**USB** USB 2.0 compliant Up to 30 MB/s transfer rate	
DPP FW SUPPORTED	DPP-QDC firmware for the Charge to Digital Conversion supported only by N6740D version		
FIRMWARE UPGRADE	Firmware can be upgraded via USB/Optical Link		
SOFTWARE	General purpose C libraries, configuration tools, readout software (Windows and Linux support)		
POWER CONSUMPTIONS	**Mod. / Supply Rail**	**@ +6V**	**@ -6 V**
	N6740	3.9 A	420 mA
	N6740D	*n.a.*	*n.a.*

3. Functional Description

3.1. Analog Input

Input dynamic is $2V_{pp}$ (Z_{in}= 50 Ω). A $10V_{pp}$ (Z_{in} = 1 kΩ) dynamic is available on request. By means of a 16-bit DAC it is possible to add up to a ±1V DC offset (±5V @$10V_{pp}$) in order to preserve the full dynamic range also with unipolar positive or negative input signals.

The input bandwidth ranges from DC to 30 MHz by 2nd order linear phase anti-aliasing low pass filter.

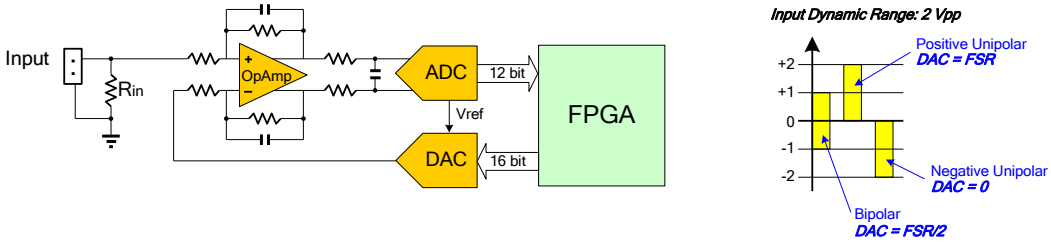

Fig. 3.1: Input diagram

3.1.1. DC Offset Common Setting

Setting the DC offset requires a write access at register addresses 0x1n98. The DC offset value will be then applied to all the 8 channels of group n.

3.1.2. DC Offset Individual Setting

It is possible to apply a 8-bit positive digital offset individually to each channel inside a group to finely correct the baseline mismatch.

The two 32-bit registers that encode the eight unsigned values for group n (n = 0..7) are:

0x10C0 + 0x100 * n -> Correction values for channel offset 0..3
0x10C4 + 0x100 * n -> Correction values for channel offset 4..7

Please, see *UM5483 - 740 Family Waveform Recording Firmware Registers* document for details.

NOTE: DC Offset individual setting is supported from the mezzanine (AMC FPGA) firmware revision **0.10** on.

3.2. Clock Distribution

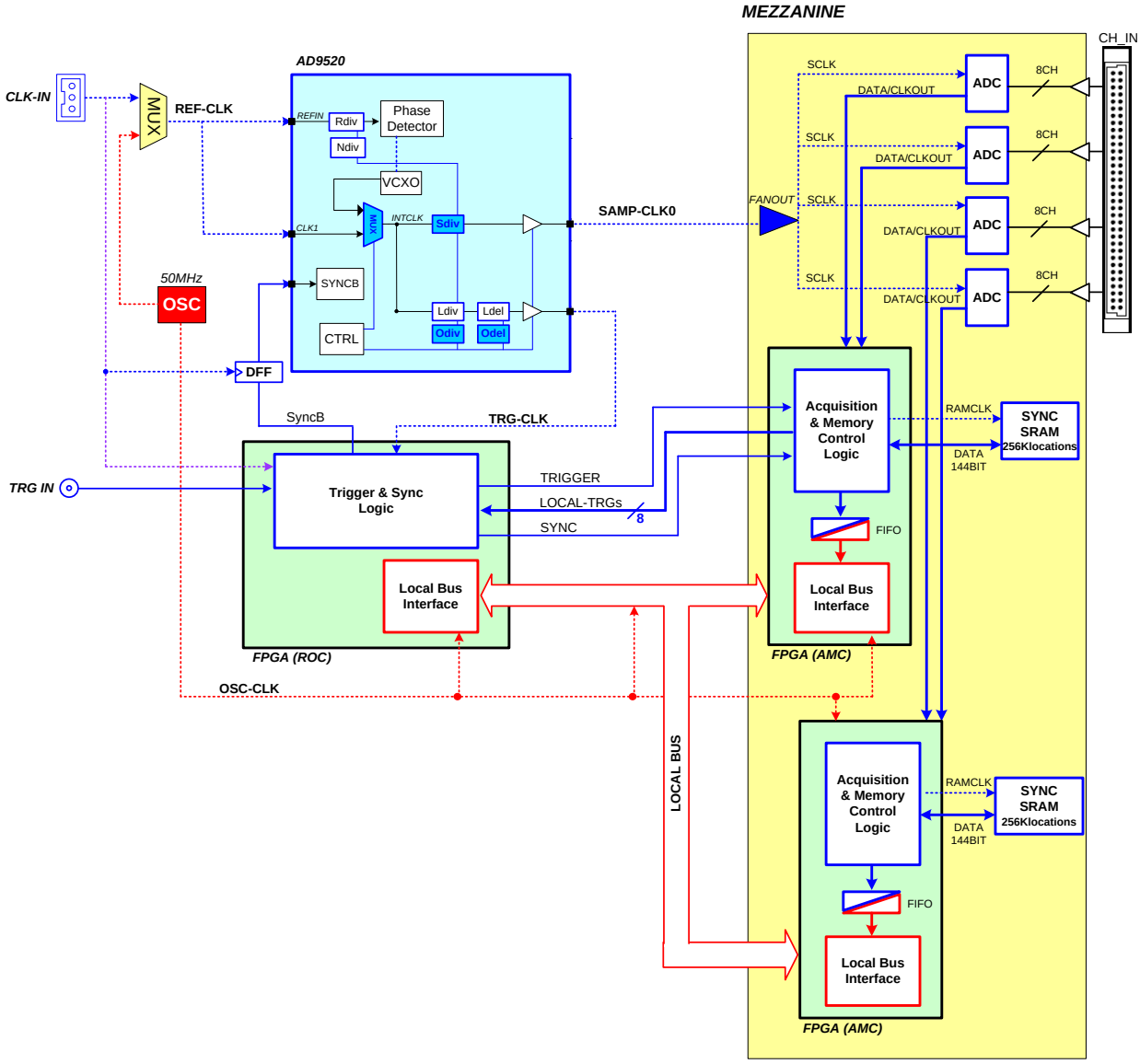

Fig. 3.2: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50MHz clock provided by an on board oscillator, the latter provides the ADC sampling clock. OSC-CLK handles Local Bus (communication between motherboard and mezzanine boards; see red traces in **Fig. 3.2**).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source, in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).

N6740 uses an integrated phase-locked-loop (PLL) and clock distribution device (AD9520). It is used to generate the sampling clock for ADCs (SAMP-CLK0/SAMP-CLK1) and trigger logic synchronization clock (TRG-CLK).

Both clocks can be generated from the internal oscillator or from external clock input (CLK IN). By default, board uses the internal clock as PLL reference (REF-CLK). External clock can be selected by register access (bit[6] of 0x8100). The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100ppm (see **Table 2.3**).
AD9520 configuration can be changed and stored into non-volatile memory. AD9520 configuration change is primarly intended to be used for external PLL reference clock frequency change:
N6740 locks to an external 50 MHz clock with default AD9520 configuration (see § **3.2.1**).

Please contact CAEN technical support (see § **8**) for more information and configuration tools.

Refer also to AD9520 data sheet for more details:
http://www.analog.com/static/imported-files/data_sheets/AD9520-3.pdf
(in case the active link above doesn't work, copy and paste it on the internet browser)

3.2.1. PLL Mode

As introduced in § **3.2**, the source of the REF-CLK signal can be external (see **Fig. 3.2**) on CLK-IN front panel connector or internal from the 50 MHz local oscillator.

The user can configure the board to sense the external clock by setting bit[6] of the register address 0x8100.

The following options are allowed:

1. 50 MHz internal clock source – It's the standard operating mode, where the default AD9520 configuration doesn't require to be changed. OSC-CLK = REF-CLK.

2. 50 MHz external clock source – In this case, it is not required to reprogram the AD9520 dividers, as the external clock reference is identical to the frequency of the internal oscillator. CLK-IN = OSC-CLK = REF-CLK.

3. External clock source different from 50 MHz – In this case, it is necessary to re-program the AD9520 dividers.

NOTE: please, contact CAEN (§ **8**) for the feasibility of point 3 and to receive the PLL programming file.

PLL programming files can then be loaded by the user by using the CAENUpgrader software tool. See § **5.1** for the program description and documentation reference.

3.2.2. Reducing the Sampling Frequency

It could be required to operate the N6740 at a sampling frequency (SAMP-CLK) lower than the nominal. In principle, this can be alternatively achieved by:

1 Direct way: reprogramming the AD9520 dividers. REF-CLK can be configured as in § **3.2.1**. Not all the frequencies are admitted and a lower frequency limit must be considered, due to the internal electronics.

NOTE: please, contact CAEN (§ **8**) for the feasibility of this method and to receive the PLL programming file.

2 Indirect way: enabling the Decimation option in the firmware (see § **3.2.3**).

3.2.3. Decimation

This functionality is a firmware option based on the programmability of a decimation factor *n*. During the acquisition, the firmware processes the digitized input waveforms calculating an averaged value of the "decimated" 2^n consecutive samples. The self-trigger is then issued as soon as an averaged value exceeds the programmed threshold (see § **3.4.3**). Software trigger and external trigger are not affected by decimation option.

While the real sampling frequency doesn't change (i.e. 62.5 MS/s), the decimation effect is to change the rate the data are written into the digitizer memory. The readout data result so at a sampling frequency changed according to the formula:

$$\frac{62.5}{2^n}\text{MS/s}$$

where *n* = [0,1,…,7].
The *n* paramenter is set through the *Decimation Factor* register (see § **1**).

Decimation functionality is supported by:

- CAENDigitizer library **revision ≥ 2.5.0**
- WaveDump software **revision ≥ 3.6.4**

NOTE: Decimation is supported only by 740 series running a AMC FPGA firmware **revision ≥ 0.7** (see § **7**).

3.2.4. Trigger Clock

The Trigger logic (TRG-CLK) works at 125-MHz frequency (2* SAMP_CLK), while, at the motherboard level, triggers are sensed, generated and distributed at 62.5-MHz frequency. The actual trigger clock frequency is so the same as the sampling one (see also § **3.3.2**).

3.3. Acquisition Modes

3.3.1. Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[1:0] setting of *Acquisition Control* register (address 0x8100) and bit[2] of the same register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- GPI CONTROLLED MODE (bits[1:0] = 01): If the acquisition is armed (i.e. bit[2] = 1), then Run starts when GPI is asserted and stops when GPI returns inactive. If bit[2] = 0, the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).

3.3.2. Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store the 31 bit counter of the Trigger Time Tag (TTT).
  The counter (representing a time reference), like so the Trigger Logic Unit (see § **3.2**) operates at a frequency of 125 MHz (i.e. 8 ns, that is to say ½ ADC clock cycles). Due to the way the acquired data are written into the board internal memory (i.e in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always "0";

- increment the EVENT COUNTER;

- fill the active buffer with the pre/post-trigger samples, whose number is programmable (record length), freezing then the buffer for readout purposes, while acquisition continues on another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between "acquisition windows" may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).

If the board is programmed to accept the overlapped triggers, as the "overlapping" trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one. In this case events will not have all the same size (see **Fig. 3.3** below).

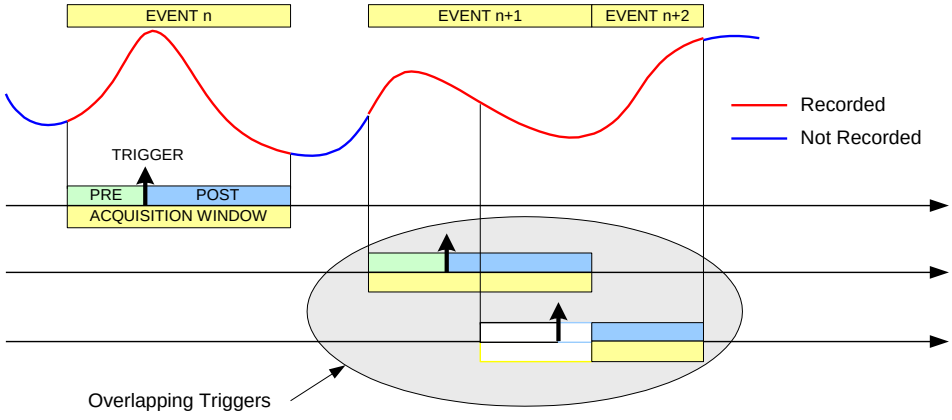

Fig. 3.3: Trigger Overlap

A trigger can be refused for the following causes:

- acquisition is not active
- memory is FULL and therefore there are no available buffers
- the required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the *RUN_ACQUISITION* command (see § **3.3.1**) or with respect to a buffer emptying after a *MEMORY_FULL* status (see § **3.3.5**);
- the trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The Event Counter can be programmed in order to be either incremented or not. If this function is enabled, the Event Counter value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the Event Counter value coincides with the sequence of buffers saved and readout.

3.3.3. Multi-Event Memory Organization

Each channel of the N6740 features a SRAM memory to store the acquired events. The memory size for the event storage is 192 kS/ch and it can be divided in a programmable number, N_b, of buffers (N_b from 1 up to 1024) by the register address 0x800C, as described in **Table 3.1** below.

Table 3.1: Buffer Organization

Register Value	Buffer Number (N_b)	SIZE of one BUFFER (samples)
		SRAM 192kS/ch
0x0	1	192k
0x1	2	96k
0x2	4	48k
0x3	8	24k
0x4	16	12k
0x5	32	6k
0x6	64	3k
0x7	128	1536
0x8	256	768
0x9	512	384
0xA	1024	192

3.3.3.1. Custom Size Events

It is possible to make events with a number of samples, which depends on 0x8020 register setting, smaller than the default value. This register's value is given in number of memory locations. According to the formula:

$$3*N_{LOC} = 2*N_S$$

only values that are multiples of 3 are allowed for this register.

NOTE: The value of N_{LOC} must be set in order that the relevant number of samples does not exceed the buffer size and it mustn't be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_{LOC}, but they are still determined by N_b.

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The *Record Length* parameter defined in CAEN software (such as WaveDump and CAENScope introduced in § **5**) and the *Set/GetRecordLength()* functions of the CAENDigitizer library (see § **4.2**) rely on these concepts.

3.3.4. *Event Structure*

The event can be readout via Optical Link and/or USB as:

An event is strucured in:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

3.3.4.1. Header

The **Header** consists in 4 words including the following information:

- **EVENT SIZE (Bit[27:0] of 1st header word)** = it is the size of the event (number of 32-bit long words);
- **BOARD FAIL flag (Bit[26] of 2nd header word)** = implemented from ROC FPGA firmware revision **4.5** on (*reserved* otherwise), this bit is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading at register address 0x8104 and contact CAEN Support Service if necessary (see § **8**);
- **EVENT MODE (Bit[24] of 2nd header word)** = this bit identifies the event format; with the default firmware, it is reserved and must be 0;
- **TRIGGER OPTIONS (Bit[23:8] of 2nd header word)** = starting from revision **4.6** of the ROC FPGA firmware, these 16 bits can be programmed to provide different trigger information according to the setting of the bits[22:21] at registeraddress 0x811C (**Table 3.2**);

  NOTE: or ROC FPGA firmware revisions lower than 4.6. these bits are reserved.

Table 3.2: Pattern configuration table

REGISTER 0x811C Bits[22:21]	FUNCTIONAL DESCRIPTION	Bit[23:8] (16 bits in the 2nd header word)
00 (default)	*Not used*	Must be 0
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bits[23:19] = 00000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[15:12] = 0000 Bits[11:8] = Trigger requests from the groups (refer to § **3.4.3**)
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where Bits[23:8] contributes as the 16 most significant bits together to the 32-bit TTT field (4th header word) **NOTE:** in the ETTT option, the overflow bit is not provided
11	*Not used*	If configured, it acts like "00" setting

- **GROUP MASK (Bit[7:0] of the 2nd header word) =** it is the mask of the groups participating in the event (e.g. GR1 and GR3 participating → Group Mask = 0xA). This information must be used by the software to acknowledge which group the samples are coming from (the first event contains the samples from the group with the lowest number);
- **EVENT COUNTER (Bit[23:0] of 3rd header word)** = it is the trigger counter; it can count either accepted triggers only, or all triggers.
- **TRIGGER TIME TAG (Bit[31:0] of 4th header word)** = It is the 31-bit Trigger Time Tag information (31-bit counter and 32nd bit as roll over flag), which is the trigger time reference. If the ETTT option is enabled, then this field becomes the 32 less significant bits of the extended 48-bit trigger time tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the roll over flag is no more provided. The trigger time tag is reset either as the acquisition starts or via front panel signal on GPI connector, and increments every ½ ADC clock cycles. So, TTT resolution is 16 ns and ranges up to 17 s (i.e. 8 ns*(2^{31}-1)), which can be extended to 625 h (i.e. 8 ns*(248-1)) by the Extended Trigger Time Tag option.

3.3.4.2. Data

Data are the stored samples. Data from masked channels are not read.

3.3.4.3. Event Format Examples

Fig. 3.4 shows the event format of the N6740 digitizer as described in § **3.3.4**.

NOTE: data transfer starts from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group (from 0 to 3) begins.

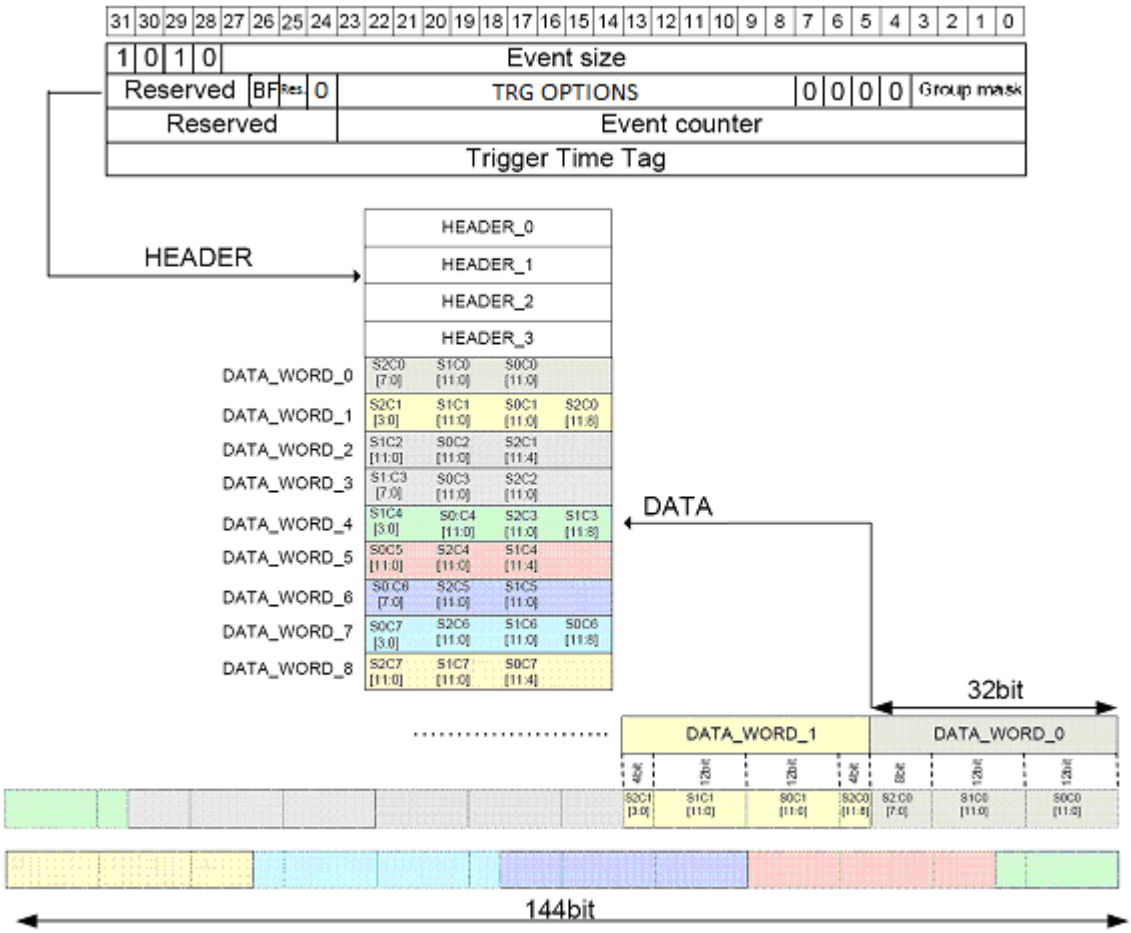

Fig. 3.4: Event Organization

3.3.5. Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N_b of circular buffers (N_b = [1:1024], see **Table 3.1**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via VMEbus or Optical Link. The acquisition can continue without dead-time in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as one buffer is readout and becomes free, the board exits the FULL condition and acquisition restarts.

IMPORTANT NOTE: When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100. The board is so programmed to enter the FULL condition when N_b-1 buffers are filled: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is readout and becomes free, the boards exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).

NOTE: when bit[5] = 1, the minimum number of circular buffers to be programmed is N_b = 2.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In this cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level to “X” (register address 0x816C), the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or N_b-1, depending on bit[5] at register address 0x8100 as above described.

It is possible to provide the BUSY signal on the digitizer front panel GPO output (bit[20], bits[19:18] and bits[17:16] at register address 0x811C are involved).

3.4. Trigger Management

According to the default firmware operating, all the channels in a board share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (a determined number of samples according to buffer organization and custom size settings, and position with respect to the trigger given by the post-trigger).

NOTE: For the trigger management in the DPP-QDC firmware operating, please refer to the web available *UM4874 - DPP-QDC User Manual*.
The generation of a common acquisition trigger is based on different trigger sources (configurable at register address 0x810C):

- **Software Trigger**
- **External Trigger**
- **Self-Trigger**
- **Coincidence**

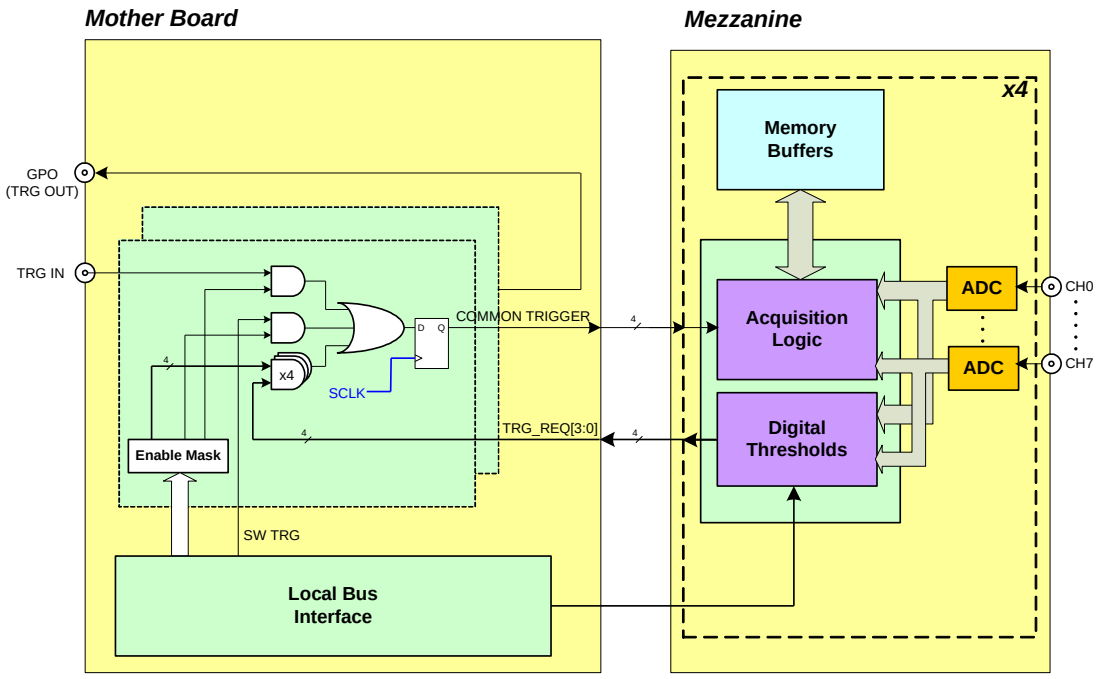

Fig. 3.5: Block diagram of Trigger management

3.4.1. Software Trigger

Software triggers are internally produced via a software command (write access at register address 0x8108) through USB or Optical Link.

3.4.2. External Trigger

A TTL or NIM external signal can be provided to the front panel TRG-IN connector (configurable at register address 0x811C). If the external trigger is not synchronized with the internal clock, a 1-clock period jitter occurs.

3.4.3. Self-Trigger

In the trigger domain, the input channels of the N6740 are managed as 8-channel groups: Group 0 = 0÷7 Ch, Group 1 = 8÷15 Ch, Group 2 = 16÷23 Ch and Group 3 = 24 ÷31 Ch. Each channel in a group (GRx_CHy_IN) is able to generate a self-trigger signal (SELF_TRG) when the digitized input pulse goes over or under a configurable threshold, according to bit[6] of register address 0x8000 (see **Fig. 3.6**). The threshold, common to each group, is set is set through the register address 0x1n80 (n is the group number). The self-triggers of each group are ORed to generate a trigger request (TRG_REQ). The trigger requests are then propagated to the central trigger logic where they are ORed to produce the board common trigger, which is finally distributed back to all channels in the groups causing the event acquisition (see **Fig. 3.5**).

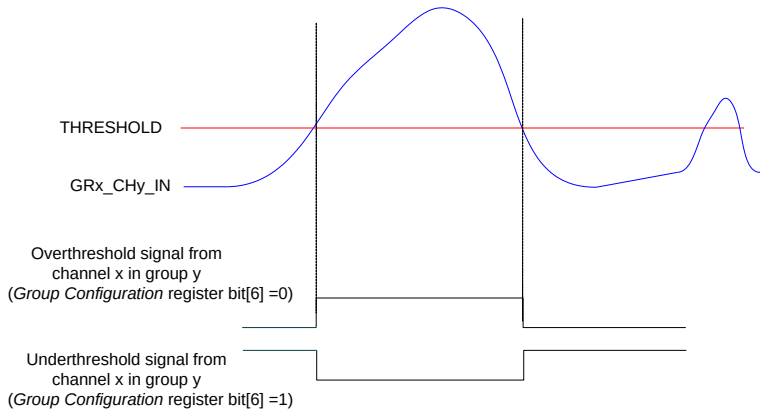

Fig. 3.6: Self-trigger generation

The FPGA, through the register address 0x1nA8, can be programmed to decide which channels in the group do participate in the trigger request generation.

Besides, the FPGA, through the register address 0x810C can be programmed to enable those groups participating in the board common trigger generation.

3.4.4. Trigger Coincidence Level

Operating with the default firmware, the acquisition trigger is a board common trigger. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Enabling the coincidences is possible by writing at register address 0x810C:

- Bits[3:0] enable the specific trigger request (i.e. the group) to participate in the coincidence;
- Bits[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock (8ns);
- Bits[26:24] set the Majority (i.e. Coincidence) level; the coincidence takes place when:

Number of enabled trigger requests > Majority level

Supposing bits[3:0] = FF (i.e. all groups are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever at least two of the enabled trigger requests are in coincidence within the programmed T_{TVAW}.
The Majority level must be smaller than the number of trigger requests enabled via bits[3:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the common trigger is simple OR of the enabled trigger requests.
Fig. 3.7 shows the trigger management in case the coincidences are disabled. To simplify the plot, only the first two groups are considered as enabled and so only one channel per group.

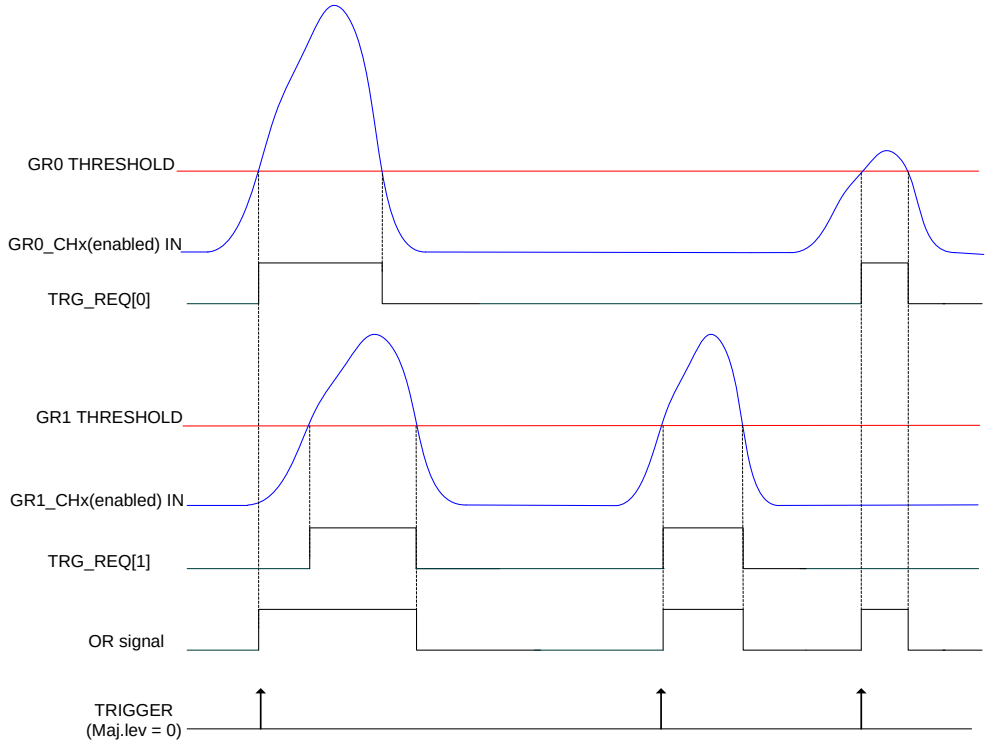

Fig. 3.7: Trigger requests relationship with Majority level = 0

Fig. 3.8 and shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0.

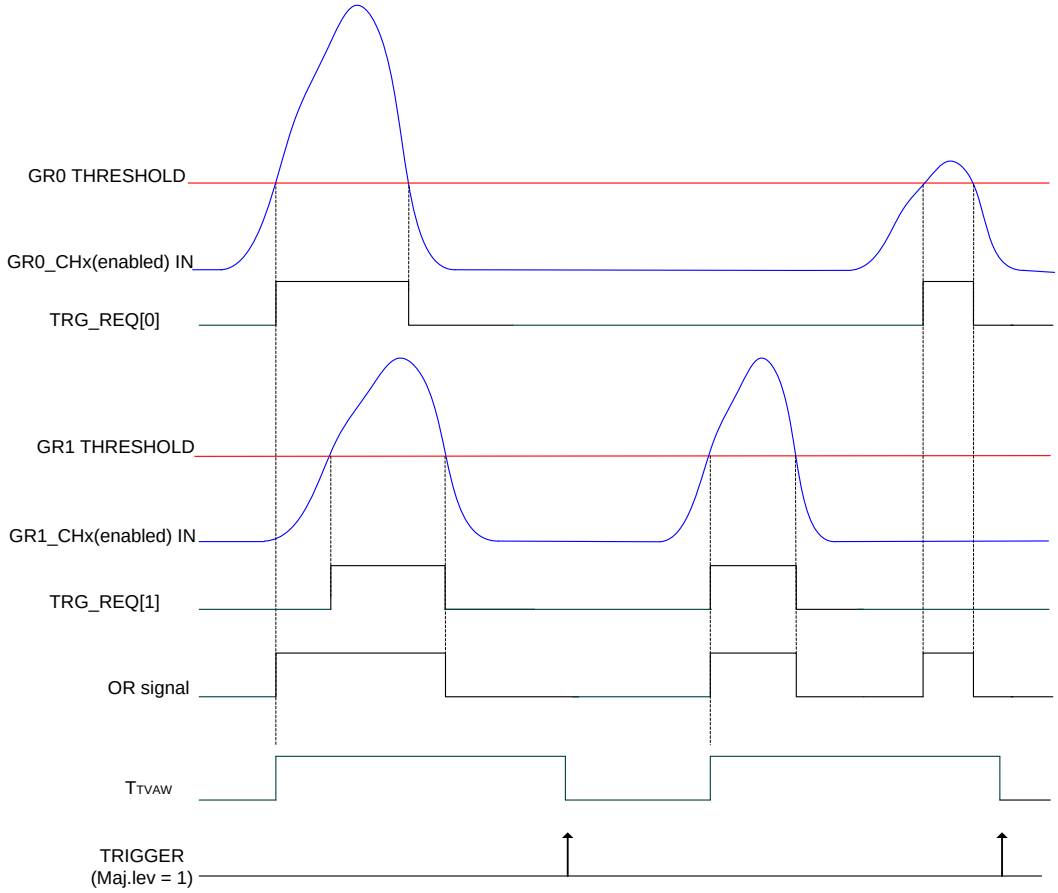

Fig. 3.8: Trigger requests relationship with Majority level = 1 and $T_{TVAW} \neq 0$

NOTE: with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post-trigger setting.

Fig. 3.9 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0.

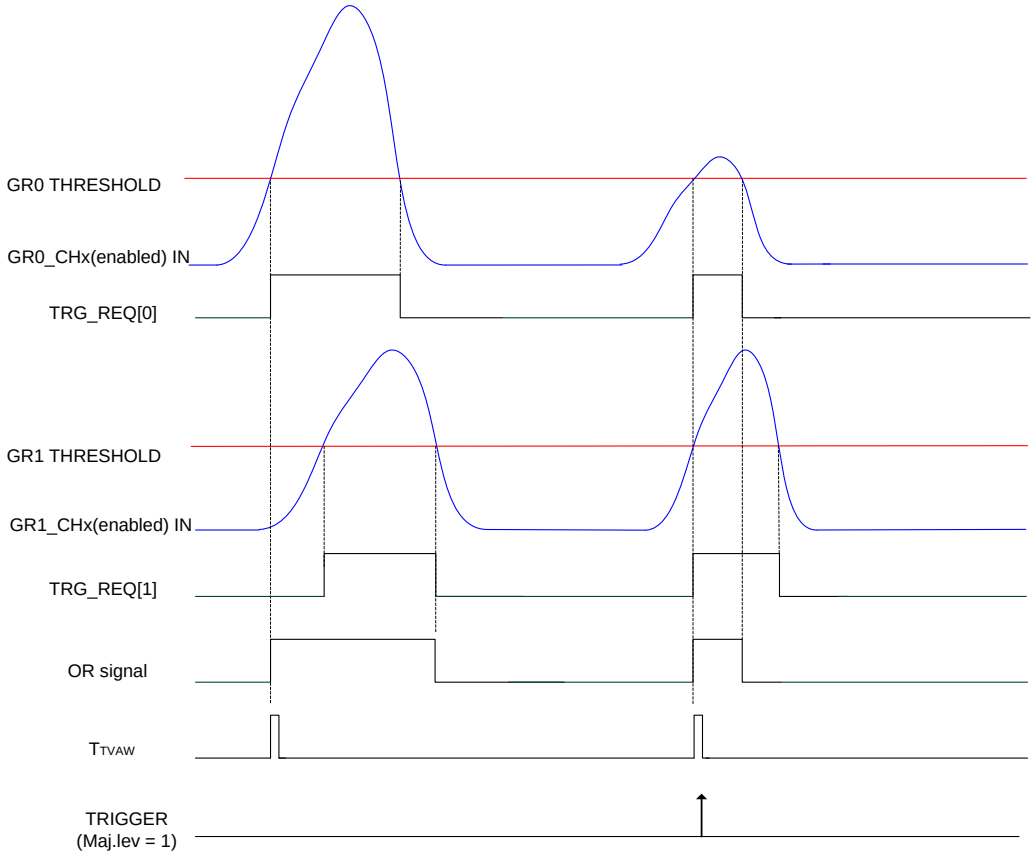

Fig. 3.9: Trigger requests relationship with Majority level = 1 and T_{TVAW} = 0

In this case, the common trigger is issued if at least two of the enabled trigger requests are instantaneously in coincidence (no T_{TVAW} is waited).

NOTE: a practical example of making coincidences with the digitizer in the standard operating is detailed in the document:

GD2817 - How to make coincidences with CAEN digitizers (web available).

3.4.5. Trigger Distribution

As described in § **3.4**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently provoking the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of **Fig. 3.10**).

A Trigger Out signal is also generated on the relevant front panel GPO connector (NIM or TTL), and allows to extend the trigger signal to other boards. Thanks to its configurability (see **Fig. 3.10**), GPO can propagate out:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of **Fig. 3.10**);

- the OR, AND or MAJORITY exclusively of the channel trigger requests

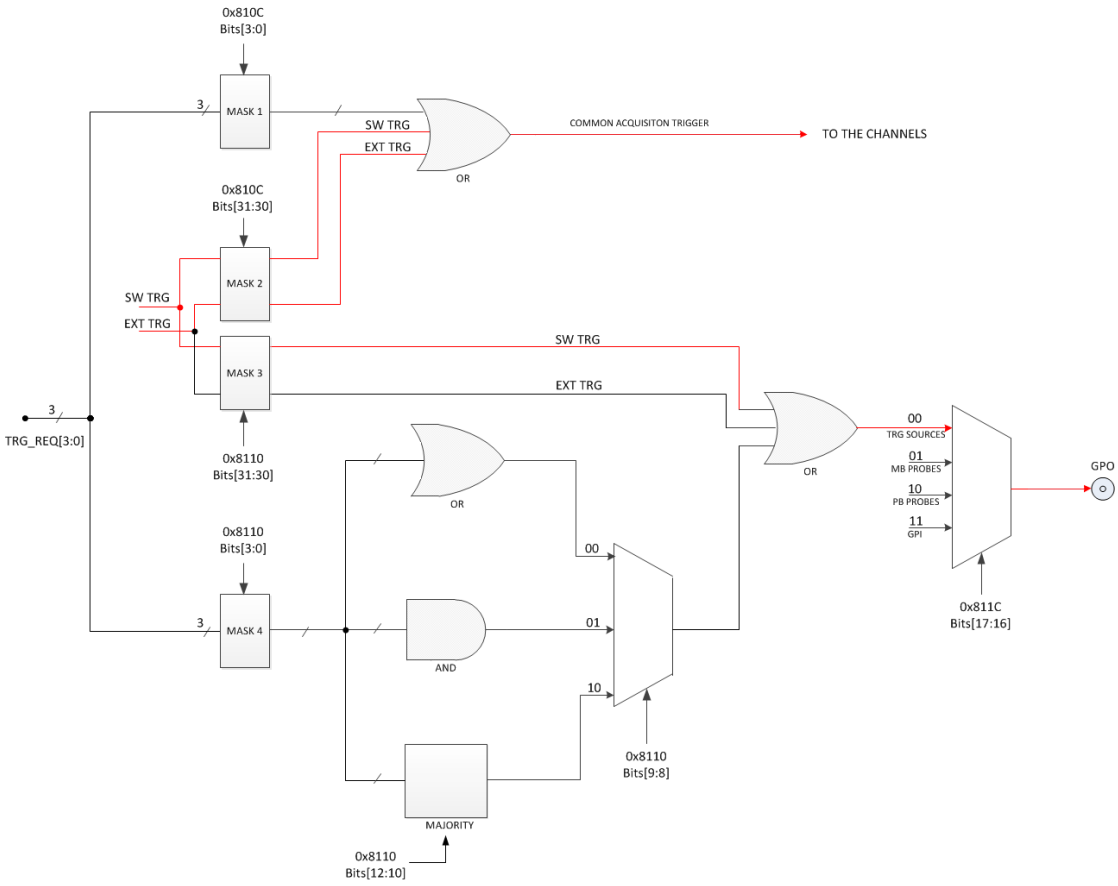

Fig. 3.10: Trigger configuration on GPO front panel output connector

The registers involved in the GPO programming are:

- Register address 0x8110;
- Register address 0x811C.

3.4.5.1. Example

For instance, it could be required to start the acquisition on all the channels of a multi-board system as soon as one of the channels of a board (board “n”) crosses its threshold. Trigger Out signal is then fed to an external Fan Out logic unit; the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal).

In this case, the programming steps to perform are following described:

1. Register 0x8110 on board “n”:
   - Enable the desired trigger request as Trigger Out signal on board “n” (by bits[3:0] mask);
   - Disable Software Trigger and External Trigger as Trigger Out signal on board “n” (bits[31:30] = 00);
   - Set Trigger Out signal as the OR of the enabled trigger requests on board “n” (bits[9:8] = 00).
2. Register 0x811C on board “n”:
   - Configure the digitizer to propagates on GPO the internal trigger sources according to the 0x8110 settings (i.e. the enabled trigger request, in the specific case) on board “n” (bits[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board “n”):
   - Enable External Trigger to participate in the board’s common acquisition trigger, disable Software Trigger and the Trigger Requests from the channels (bits[31:30] = 01; bits[3:0] = 0000).

3.5. Reset, Clear and Default Configuration

3.5.1. Global Reset

Global Reset is performed at Power-On of the module or via software by write access at register address 0xEF24 (whatever 32-bit value can be written). It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

3.5.2. Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via either a write access at register address 0xEF28 (whatever 32-bit value can be written).

3.5.3. Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to the front panel GPI input (leading edge sensitive).

3.6. Data Transfer Capabilities

N6740 features a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in § **3.3.3**. Once they are written in the memory, the events become available for readout via USB or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers. The acquisition process is so "dead timeless" until the memory becomes full (see § **3.3.5**).

The events are readout sequentially and completely, starting from the Header of the first available event, followed by the data of the enabled groups (from 0 to 3) as reported in **Fig. 3.4**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C, as well as on the number of enabled channels.

3.6.1. Block Transfer

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the *SetMaxNumEventsBLT()* function of the CAENDigitizer library (refer to § **4.2**).

When developing programs, the readout process can be implemented on different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link (not supported by USB).
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of the *Block Transfer Event Number* register or the library function *SetMaxNumEventsBLT()* mentioned above. If the board is empty, the BLT access is immediately terminated and the "Read Block" function will return 0 bytes (it is the *ReadData()* function in the CAENDigitizer Library).

Whatever the method from above, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite of a greater memory allocation required on the host station side that is actually not a real drawback, considering the features of the personal computers available on the market.

3.6.2. Single Data Transfer

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § **3.3.4**.

It is suggested, after the 1st word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to completely read the event.

3.7. Optical Link and USB Access

The board houses a USB2.0 compliant port, providing a transfer rate up to 30 MB/s, and a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) providing transfer rate up to 80 MB/s. The latter allows to connect up to 8 N6740 boards to a single A2818 PCI Optical Link Controller or up to 32 boards to a single A3818 PCIe Optical Link Controller.

Detailed information on CAEN PCI/PCIe Controllers can be find at www.caen.it:

Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controllers

The parameters for read/write accesses via optical link are Address Modifier, Base Address, data Width, etc.; wrong parameter settings cause Bus Error.

Bit[3] at register address 0xEF00 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.
Interrupts can also be managed at the CAENDigitizer library level (see “Interrupt Configuration” in the library User Manual)

4. Drivers & Libraries

4.1. Drivers

In order to interface with the N6740, CAEN provides the drivers for all the different types of physical communication channels featured by the board and compliant with Windows and Linux OS:

- **USB 2.0 Drivers** are downloadable on CAEN website (www.caen.it) in the "Software/Firmware" tab at the N6740 web page (**login required**).

NOTE: For Microsoft Windows OS, the USB driver installation is detailed in the *GD2783 - First Installation Guide to Desktop Digitizers & MCA* (search on the website in the Document Library section).

- **Optical Link Drivers** are managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the "Software/Firmware" area at the A2818 or A3818 page (**login required**)

NOTE: For the installation of the Optical Link driver, refer to the User Manual of the specific Controller.

4.2. Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason**, the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

CAENDigitizer installation package and the relevant documentation are available on CAEN website at the CAENDigitizer Library page.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.

The CAENComm installation package, the relevant documentation and the link to the required CAENVMELib are available on CAEN website in the 'Download' area at the CAENComm Library page.

CAENComm (and so the CAENDigitizer) supports the following communication channels:

PC → USB → N6740

PC → PCI/PCIe (A2818/A3818) → CONET → N6740

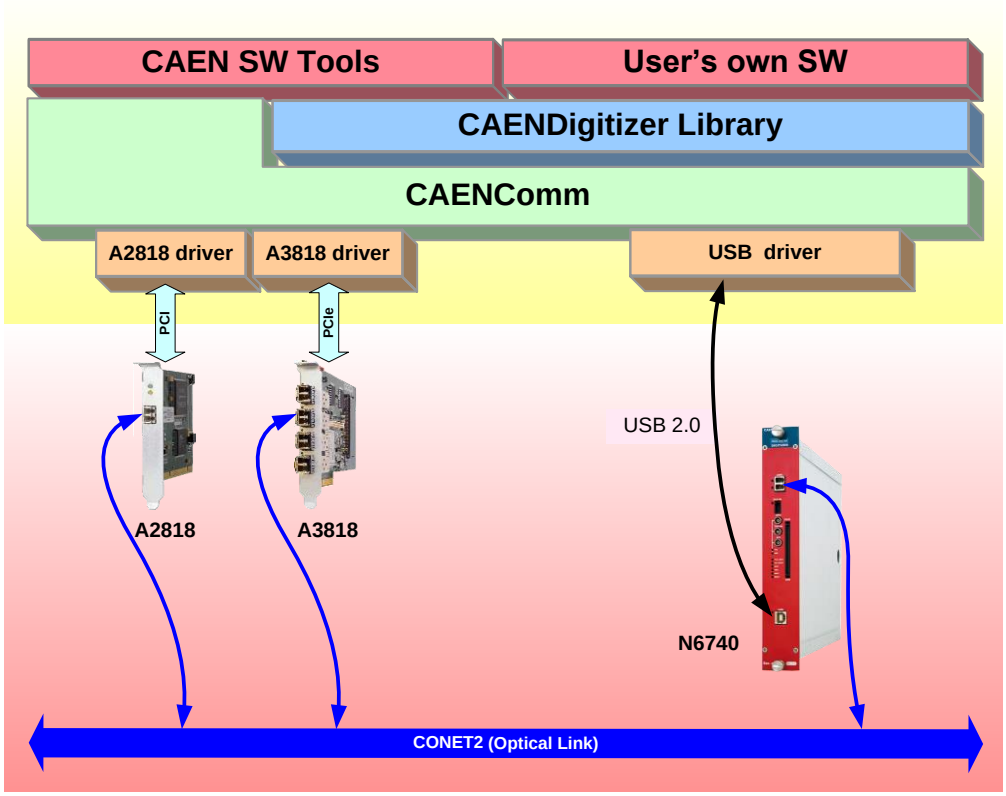

Fig. 4.1: Block diagram of the software layers

5. Software Tools

CAEN provides software tools to interface the N6740, which are available for free download on www.caen.it at:

Home / Products / Firmware/Software / Digitizer Software

5.1. CAENUpgrader

CAENUpgrader is a free software composed of command line tools together with a Java Graphical User Interface.

Specifically for the N6740, CAENUpgrader allows in few easy steps to:

- Upload different firmware versions on the board
- Select which copy of the stored firmware must be loaded at power-on
- Read the firmware release of the board and the bridge (when used)
- Manage the firmware license, in case of pay firmware
- Upgrade the internal PLL
- Get the Board Info file, useful in case of support

CAENUpgrader can operate with Windows and Linux, 32 and 64-bit OSs.

The program relies on the CAENComm and CAENVMELib libraries (see § **4.2**) and requires third-party Java SE 8 u40 (or later) to be installed.

NOTE: Windows version of CAENUpgrader is stand-alone (i.e. only the communication driver needs to be installed apart by the user, while the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be previously installed by the user.

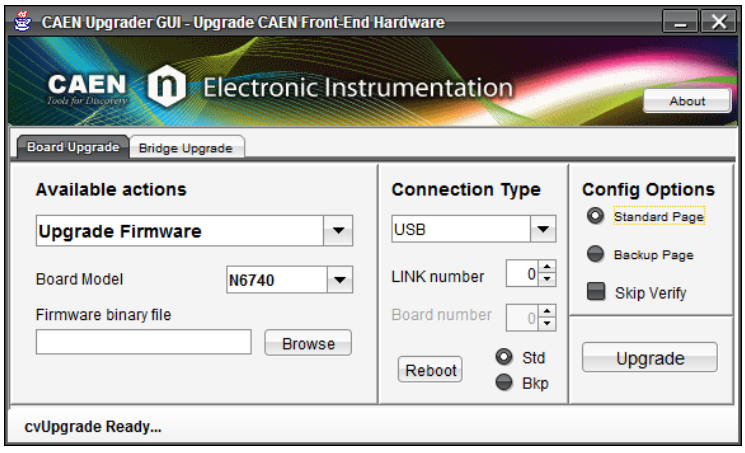

Fig. 5.1: CAENUpgrader Graphical User Interface

CAENUpgrader installation package can be downloaded on CAEN web site (login required) at:

Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader

The reference document for installation instructions and program detailed description is downloadable at the same page above, in the Documentation tab.

5.2. CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java and LabVIEW GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

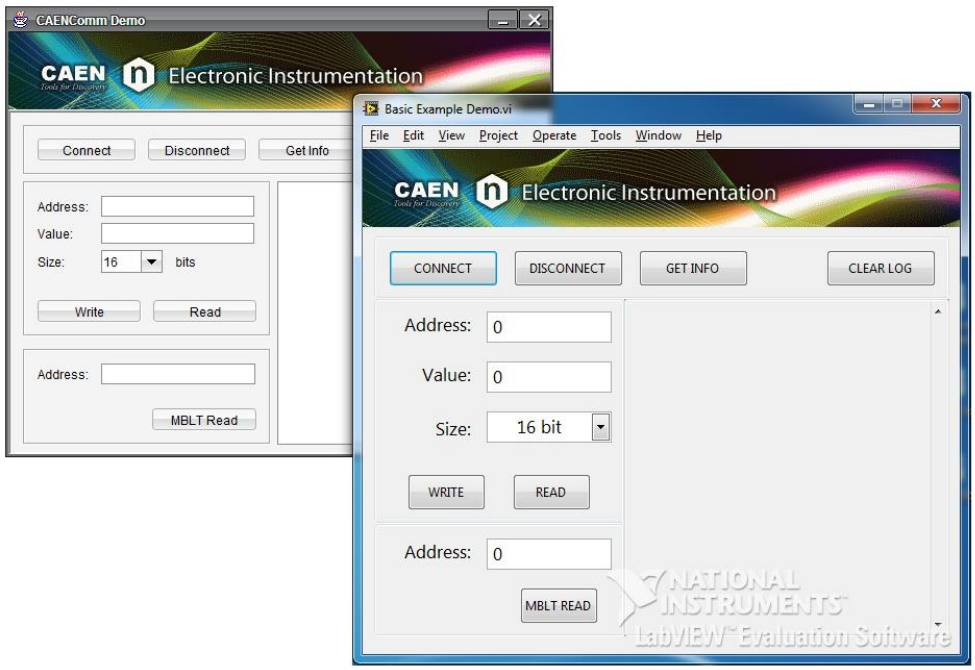

Fig. 5.2: CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo can operate with Windows OS, 32 and 64-bit. It requires CAENComm and CAEVMElib libraries as additional software to be installed (see § **4.2**).

The Demo is included in the CAENComm library Windows installation package, which can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library

5.3. CAEN WaveDump

WaveDump is a basic console application, with no Graphical User Interface, developed to control CAEN digitizers running standard firmware. The program demonstrates the use of libraries and methods for an efficient readout and data analysis. Users who want to develop their own acquisition software can take advantage of the included C source files and Visual Studio project.

The user can program a single board (multi-board management is not supported), according to a text configuration file containing a list of parameters and instructions, to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot third-party graphing utility (www.gnuplot.info).

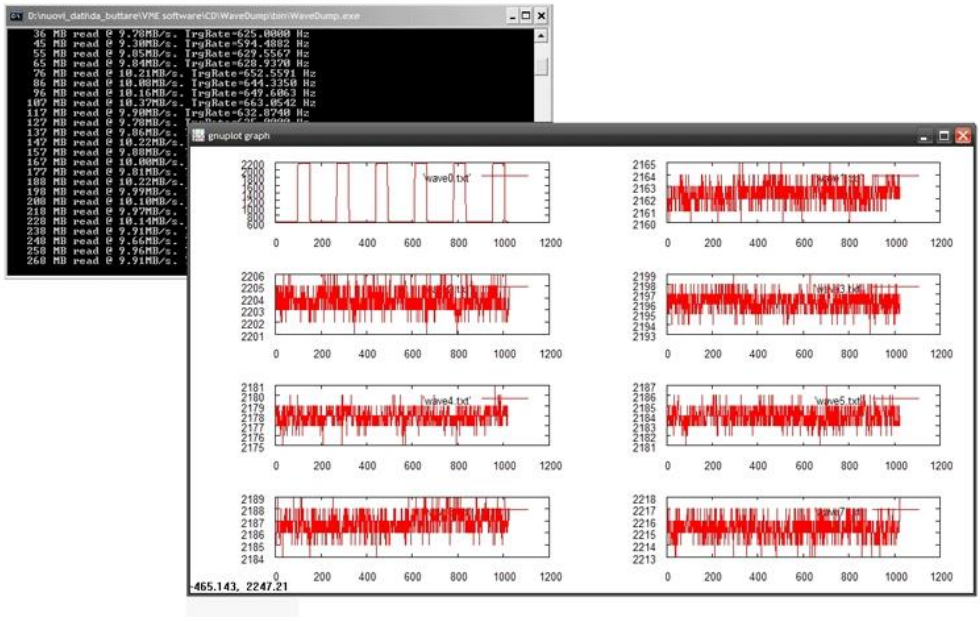

Fig. 5.3: CAEN WaveDump

CAEN WaveDump can operate with Windows and Linux OS, 32 and 64-bit.

The program relies on the CAENDigitizer, CAENComm and CAENVMELib libraries (see § **4.2**). Linux users are required to install the third-party Gnuplot.

NOTE: Windows version of WaveDump is stand-alone (the required libraries are installed locally with the program), while the version for Linux needs the required libraries to be previously installed by the user.

Installation packages and documentation can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Readout Software / CAEN WaveDump

5.4. DPP-QDC Demo Software

DPP-QDC Demo Software is a is C demo application that manages the communication and the data acquisition from 740D digitizer series running the DPP-QDC firmware. It is possible to set the communication parameters and DPP settings. Waveforms and histograms can also be plotted in real time for one channel at a time, and both waveforms and lists of time stamp and energy can be saved. DPP-QDC Demo Software is provided including C source files for developers

DPP-QDC Demo Software can operates with Windows OS, 32 and 64-bit.

Installation packages and documentation can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / DPP-QDC

6. HW Installation

- The Module fits into all NIM crates.
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: this product needs proper cooling:

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: this product needs proper handling:

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

6.1. Power-ON Sequence

To power on the board follow this procedure:

1. insert the N6740 into the crate
2. power up the crate

6.2. Power-on Status

At Power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration.

After the power-on, only the NIM and PLL LOCK front panel LEDs must light on.

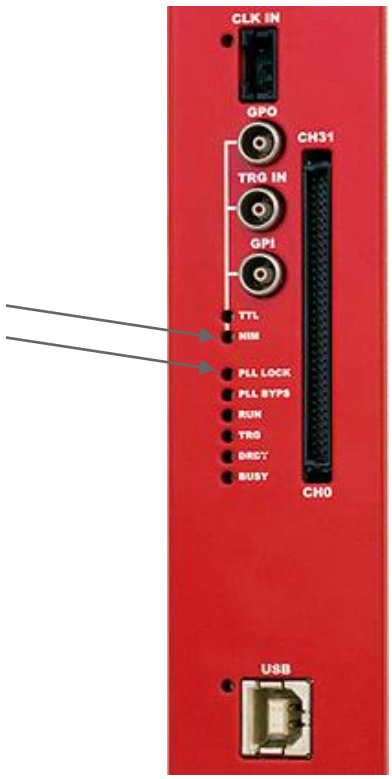

Fig. 6.1: Front panel LEDs status at power-on

7. Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs on the mezzanine (i.e. one FPGA per 16 channels or two 8-channel groups). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA or MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA or MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

x740D versions mount a bigger mezzanine FPGA.

x740D AMC FPGA or MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C40

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as *Standard* (STD) and *Backup* (BKP). In case of default firmware, the board is usually factory equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy.

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENUpgrader software (see § **5.1**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

7.1. Default Firmware Upgrade

The N6740 is delivered running a default firmware to operate the board for waveform recording.

The default firmware updates are available for download on CAEN website (www.caen.it) in the *Software/Firmware* tab at the N6740/N6740D web pages (**login required**):

Home / Products / Modular Pulse Processing Electronics / VME / Digitizers / <Digitizer Model>

7.1.1. Default Firmware File Description

The extension of the programming default firmware file is CFA (CAEN Firmware Archive), which is a sort of archive format file aggregating all the default firmware files compatible with the same family of digitizers.

CFA and its name follows this general scheme:

x740_revX.Y_W.Z.CFA

where:

- x740 are all the boards supported by the file: DT5740, DT5740C, DT5740D, N6740, N6740C, N6740D, V1740, V1740A, V1740B, V1740C, V1740D, VX1740, VX1740A, VX1740B, VX1740C, VX1740D;
- X.Y is the major (X) and minor (Y) revision number of the mainboard FPGA;
- W.Z is the major (W) and minor (Z) revision number of the channel FPGA.

7.2. DPP Firmware Upgrade

CAEN can provides special DPP-QDC firmware for Physics Applications supported only by x740D versions. The digitizer running DPP-QDC firmware becomes a Gated Integrator receiving signals directly from the detector (no charge preamp required).

The DPP-QDC firmware updates are available for download on CAEN website in the Download tab (**login required**) at:

Home / Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / DPP-QDC

7.2.1. DPP Firmware File Description

The extension of the programming DPP firmware file is CFA (CAEN Firmware Archive), which is a sort of archive format file aggregating all the firmware files compatible with the same DPP firmware and family of digitizers.

CFA and its name follows this general scheme:

x740D_DPP-QDC_rev_X.Y_135.Z.CFA

where the major revision number of the channel FPGA is fixed for the specific DPP algorithm and digitizer family ("135" for DPP-QDC and 740D). The other fields have the same meaning as in the default firmware file description (see § **7.1.1**).

NOTE: DPP special firmware is a pay firmware requiring a license to be purchased. If not licensed, the firmware will run fully functional but with a time limitation per power cycle (30 minutes). Details on the license ordering procedure can be found in CAENUpgrader Quick Start Guide (see § **5.1**).

NOTE: if the x740D module is ordered together with a DPP-QDC firmware license, the customer will be delivered with the digitizer already running the licensed (i.e. unlocked) special firmware.

NOTE: once unlocked, upgrading the same kind of DPP firmware requires no further licensing.

7.3. Troubleshooting

In case of upgrading failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system will try to program the board automatically from the alternative FLASH page (e.g. BKP FLASH page) if this is not corrupted as well. The user can perform a further upgrade attempt on the STD page to restore the firmware copy.

7.3.1. PCB revision 0

NOTE THAT old versions of the digitizer motherboard (bit[7:0] = 0x00 at register address 0xF050) have a slightly different FLASH management. At power-on, the microcontroller loads exactly the firmware copy from the STD page of the FLASH.

In this case, when a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the N6740, the user can perform the following recovering procedure as first attempt:

- Force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, make sure to connect by USB link and use the *Reboot* function in CAENUpgrader software by checking “Bkp” option

- Use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is possible now to communicate again with the board.

- Use CAENUpgrader to load again the firmware on the STD page, then power-cycle in order the board to get operative again.

If neither of the procedures described at § **7.3** and § **7.3.1** succeeds, it is recommended to send the board back to CAEN in repair (see § **8**).

8. Technical Support

CAEN support services are available for the user by accessing the Support & Services area on CAEN website at www.caen.it.

8.1. Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the Returns and Repairs area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.
Contacts for shipping are reported on the website at *Home / Contacts*.

8.2. Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)