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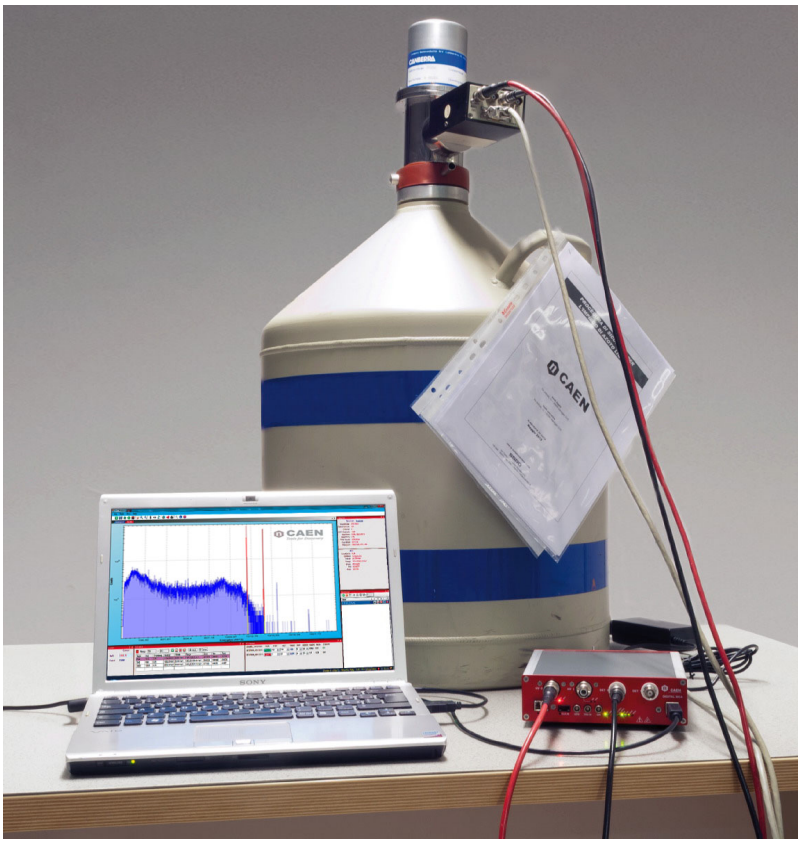

User Manual UM5469

780 DPP-PHA Registers

Register Description for 780 DPP-PHA

Rev. 0 - September 22nd, 2016

Purpose of this Manual

The User Manual contains the full description of the DPP-PHA firmware registers for 780 family series. The description is compliant with the DPP-PHA firmware revision **4.11_128.33**. For future release compatibility check the firmware history files.

Change Document Record

Date	Revision	Changes
September 22nd, 2016	00	Initial Release

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
LVDS	Low-Voltage Differential Signal
MCA	Multi-Channel Analyzer
ROC	ReadOut Controller
USB	Universal Serial Bus

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R **Read only**. The register can be accessed in read only mode.
W **Write only**. The register can be accessed in write only mode.
R/W **Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

I **Individual register**. This kind of register has N instances, where N is the total number of channels in the board. Individual registers can be written either in single mode (individual setting) or broadcast (simultaneous write access to all channels). Read command must be individual.
Single access can be performed at address 0x1nXY, where n is the channel number, while broadcast write can be performed at the address 0x80XY. For example:

- access to address 0x1570 to read/write register 0x1n70 for channel 5 of the board;
- to write the same value for all channels in the board, access to 0x8070 (broadcast write). To read the corresponding value, access to the individual address 0x1n70.

C **Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

H **HV register**. In case of 780 series and DT5790 some registers manage the HV channels of the boards. Read and write access can be performed at address 0x1nXY only, where n=2 corresponds to the HV channel 0 and n=3 corresponds to the HV channel 1.

Register Name	Address	Mode	Attribute
High Voltage VSet	0x1n20 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage ISet	0x1n24 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Ramp Up	0x1n28 (n=2 for HV-ch0, n=3 for HV- ch1)	R/W	H
High Voltage Ramp Down	0x1n2C (n=2 for HV-ch0, n=3 for HV- ch1)	R/W	H
High Voltage VMax	0x1n30 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
High Voltage Control	0x1n34 (n=2 for HV-ch0, n=3 for HV-ch1)	R/W	H
Number of Events per Aggregate	0x1n34, 0x8034	R/W	I
High Voltage Status/A639 Firmware Release	0x1n38 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
Pre Trigger	0x1n38, 0x8038	R/W	I
Data Flush	0x1n3C, 0x803C	W	I
High Voltage VMon/Analog In	0x1n40 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
Channel n Stop Acquisition	0x1n40, 0x8040	R/W	I
High Voltage IMon/Temperature In	0x1n44 (n=2 for HV-ch0, n=3 for HV-ch1)	R	H
RC-CR2 Smoothing Factor	0x1n54, 0x8054	R/W	I
Input Rise Time	0x1n58, 0x8058	R/W	I
Trapezoid Rise Time	0x1n5C, 0x805C	R/W	I
Trapezoid Flat Top	0x1n60, 0x8060	R/W	I
Peaking Time	0x1n64, 0x8064	R/W	I
Decay Time	0x1n68, 0x8068	R/W	I
Trigger Threshold	0x1n6C, 0x806C	R/W	I
Rise Time Validation Window	0x1n70, 0x8070	R/W	I
Trigger Hold-Off	0x1n74, 0x8074	R/W	I
Peak Hold-Off	0x1n78, 0x8078	R/W	I
Baseline Hold-Off	0x1n7C, 0x807C	R/W	I
DPP Algorithm Control	0x1n80, 0x8080	R/W	I
Shaped Trigger Width	0x1n84, 0x8084	R/W	I
Channel n Status	0x1n88	R	I
AMC Firmware Revision	0x1n8C	R	I
DC Offset	0x1n98, 0x8098	R/W	I
Input Dynamic Range	0x1nB4, 0x80B4	R/W	I
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Aggregate Organization	0x800C	R/W	C
Record Length	0x8020	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Channel Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Event Size	0x814C	R	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C

Disable External Trigger	0x817C	R/W	C
Trigger Validation Mask	0x8188 (ch0), 0x818C (ch1)	R/W	I
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Aggregate Number per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C
Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

High Voltage VSet

Set the channel voltage value (V)

Address	0x1n20 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[15:0]	Channel voltage value in steps of 0.1 V. For example to set 2500 V write 25000.
[31:16]	Reserved

High Voltage ISet

Set the maximum current limit that can be supplied by a channel

Address	0x1n24 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[15:0]	Set the maximum current in steps of 10 nA (780 series) and 50 nA (DT5790). For example to set 2000 uA, write 40000 for DT5790 and 200000 for 780 series.
[31:16]	Reserved

High Voltage Ramp Up

Set the ramp up voltage value in V/s

Address	0x1n28 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[8:0]	Ramp up in V/s.
[31:9]	Reserved

High Voltage Ramp Down

Set the ramp down voltage value in V/s

Address	0x1n2C (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[8:0]	Ramp down in V/s.
[31:9]	Reserved

High Voltage VMax

VMax is the hardware value that can be programmed by the user to limit the maximum voltage of a channel. If a value VSet > VMax is erroneously programmed, the HV channels supplies up to VMax and marks bit[6] of register High Voltage Status 0x1n38.

Address	0x1n30 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[7:0]	Maximum voltage value in steps of 20 V for 780 series and DT5790, and 2 V for 780SD boards. Note: the VMax resolution of 2 V is supported for HV firmware release greater than 2.2. For HV firmware release less than 2.2 the VMax resolution is 20 V.
[31:8]	Reserved

High Voltage Control

This register manages the high voltage power and monitor mode

Address	0x1n34 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R/W
Attribute	H

Bit	Description
[0]	Manages the Power ON/OFF of the HV channel. Options are: 0: HV channel OFF; 1: HV channel ON.
[1]	Manages how the channel shuts down. This setting applies both when the user shuts the channel down and when the channel automatically shuts down due to an alarm (see register High Voltage Status 0x1n38). Options are: 0: kill mode, the HV channel shuts down instantaneously; 1: ramp mode, the HV channel shuts down with a rate of V/s as defined by the HV Ramp Down register, 0x1n2C.
[6:2]	Reserved
[7]	Manages the monitor mode of the HV channel. Options are: 0: Register 0x1n40 used to monitor the HV Channel VMon, register 0x1n44 used to monitor the HV Channel IMon, register 0x1n38 used to monitor the HV Channel Status; 1: Register 0x1n40 used to monitor the Analog In, register 0x1n44 used to monitor the Temperature In, register 0x1n38 used to monitor the A639 Firmware Release.
[31:8]	Reserved

Number of Events per Aggregate

Each couple of channels has a fixed amount of RAM memory to save the events. The memory is divided into a programmable number of buffers, called ”aggregates”, whose number of events can be programmed by this register. The maximum number of events per aggregate depends on the aggregate size (which is defined by the number of aggregates per memory, 0x800C), and the event size (which is defined by the record length, 0x1n20, the acquisition mode and the event format, 0x8000).
Note: it is usually recommended to keep this value high to optimize the readout, except in case of small input rate, where it is recommended to use a smaller value (even 1). Since the memory cannot be read until the aggregate is full, setting a a small number of events per aggregate makes the events ready to be read in a shorter time scale. Users can also force the readout through the flush register, 0x1n3C.

Address	0x1n34, 0x8034
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Number of events per aggregate.
[31:10]	Reserved.

High Voltage Status/A639 Firmware Release

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, HV channel status (see the bit description for more details). NOTE: in case of bit[3], bit[9], bit[10] or bit[14] = 1 the HV channel is turned off according to Power Down Mode (see HV Channel Control register, 0x1n34);
2. monitor mode = 1, A639 firmware release. For example, for a firmware release 1.03, the register value is 0x103, where 1 corresponds to the register word high byte, and 3 corresponds to the register word low byte.

Address	0x1n38 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[0]	1 = HV power ON
[1]	1 = HV channel rump up
[2]	1 = HV channel rump down
[3]	1 = HV channel is in Over Current (IMon > ISet)
[4]	1 = HV channel is in Over Voltage (VMon > VSet + 2%)
[5]	1 = HV channel is in Under Voltage (VMon < VSet - 2%)
[6]	1 = HV channel is over Maximum Voltage (Vout > VMax)
[7]	1 = HV channel is over Maximum Current (IMon > hardware maximum IOut)
[8]	1 = Temperature warning. The temperature of the HV channel is greater than 80°C.
[9]	1 = Over Temperature. The temperature of the HV channel is greater than 125°C.
[10]	1 = HV channel is disabled for an active external inhibit.
[11]	1 = Calibration error. There is a calibration error on the HV channel.
[12]	1 = Alarm Reset. The HV channel is resetting the alarms.
[13]	1 = HV channel is shutting down
[14]	1 = Maximum Power. The HV output power is greater than 4 W.
[15]	1 = Fan speed high
[31:16]	Reserved

Pre Trigger

The Pre Trigger defines the number of samples before the trigger in the waveform saved into memory.

Address	0x1n38, 0x8038
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Number of pre trigger samples according to the formula Ns = N * 2, where Ns is the pre trigger and N is the register value. For example, write N = 10 to set 20 samples of pre trigger. Each sample corresponds to 10 ns.
[31:10]	Reserved

Data Flush

Data events are grouped into aggregates of N events each, where N can be programmed through register 0x1n34. As soon as an aggregate reaches N events then it is ready to be read. An aggregate containing a number of events smaller than N cannot be read and must be forced to flush its current data. This is for example the case of low input rate, where the board might appear empty (no data) even if a small amount of events is already stored in the buffer, or at the end of the run where the last aggregate might be incomplete. A write access to this register forces the read of the current incomplete aggregate.

Address	0x1n3C, 0x803C
Mode	W
Attribute	I

Bit	Description
[31:0]	A write access to this register causes the flush of the current aggregate.

High Voltage VMon/Analog In

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, HV channel VMon;
2. monitor mode = 1, voltage between Pin 3 (EXT_ANALOG) and Pin 1 (GND) of the DB9 connector related to the selected channel.

Address	0x1n40 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[15:0]	If monitor mode = 0, these bits read the HV channel VMon. VMon is equal to the content of the register multiplied by the resolution of 0.1 V. For example, if the register value is 10238, VMon = 1023.8 V. If monitor mode = 1, these bits read the voltage between Pin 3 (EXT_ANALOG) and Pin 1 (GND) of the DB9 connector related to the selected channel. The voltage value is equal to the content of the register multiplied by the inverse of the resolution of 0.001 V.
[31:16]	Reserved

Channel n Stop Acquisition

This register performs the stop acquisition of a single channel n. If bit[0] = 0, then channel n starts the acquisition as the global run is active, together with any other enabled channel. Note that if the global run is not active, writing 0 in this register does not produce any effect. If bit[0] = 1 and the global run is active, then channel n stops the acquisition independently on the other enabled channels.
It is possible to drive the start/stop acquisition independently on each channel by the following steps:
1. Set the individual stop acquisition on each desired channel (bit[0] = 1).
2. Enable the global run through register Acquisition Control 0x8100 (no channel will start the acquisition);
3. Set bit[0] = 0 to start the individual acquisition, then bit[0] = 1 to stop it.
4. When all channels are individually stopped, disable the global run.

Address	0x1n40, 0x8040
Mode	R/W
Attribute	I

Bit	Description
[0]	Options are: 0: Run; 1: Stop.
[31:1]	Reserved

High Voltage IMon/Temperature In

According to the monitor mode value (bit[7] of register High Voltage Control 0x1n34) this register corresponds to:
1. monitor mode = 0, this register provides the monitored current value;
2. monitor mode = 1, this register is used to read the value of the resistance between Pin 8 (EXT_TEMP) and Pin 1 (GND) of the DB9 connector related to the selected channel.

Address	0x1n44 (n=2 for HV-ch0, n=3 for HV-ch1)
Mode	R
Attribute	H

Bit	Description
[15:0]	If monitor mode = 0, these bits provide the monitored current value. The value of Imon is equal to the content of the register multiplied by the resolution (780 series: 10 nA; DT5790: 50 nA). For example, if Imon Reg = 10238 then IMon = 102.38 uA (DT5780). If Imon Reg = 10238 then IMon = 511.9 uA (DT5790). If Monitor Mode = 1, these bits are used to read the value of the resistance between Pin 8 (EXT_TEMP) and Pin 1 (GND) of the DB9 connector related to the selected channel. The resistance value is that of a temperature probe PT100 or PT1000. The resistance value is equal to the content of the register multiplied by the resolution of 0.1 Ohm. For example, if Reg value = 1234, then the resistance value = 123.4 Ohm.
[31:16]	Reserved

RC-CR2 Smoothing Factor

Defines the number of samples of a moving average filter used for the RC-CR2 signal formation.

Address	0x1n54, 0x8054
Mode	R/W
Attribute	I

Bit	Description
[5:0]	Write the desired number of samples. Options are: 0x1: 1 sample; 0x2: 2 samples; 0x4: 4 samples; 0x8: 8 samples; 0x10: 16 samples; 0x20: 32 samples.
[31:6]	Reserved

Input Rise Time

This register defines the time constant of the derivative component of the PHA fast discriminator filter.
In case of RC-CR2 this value must be equal (or 50% more) to the input rising edge, in such a way the RC-CR2 peak value corresponds to the height of the input signal.

Address	0x1n58, 0x8058
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Rise Time expressed in sampling clock units (10 ns)
[31:8]	Reserved

Trapezoid Rise Time

Sets the Trapezoid Rise Time, i.e. the Shaping Time of the energy filter.
Note: the sum of Trapezoid Rise Time and Trapezoid Flat Top (see register 0x1n60) should not exceed 15 us for 724 series. Values are x2, x4, x8 according to the decimation factor (bits[9:8] of 0x1n80).

Address	0x1n5C, 0x805C
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Trapezoid Rise Time value expressed in sampling clock unit (10 ns).
[31:10]	Reserved

Trapezoid Flat Top

Sets the Trapezoid Flat Top width.
Note: the sum of the Trapezoid Rise Time (see register 0x1n5C) and Trapezoid Flat Top should not exceed 15 us for 724 series. Values are x2, x4, x8 according to the decimation factor (bits[9:8] of 0x1n80).

Address	0x1n60, 0x8060
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Trapezoid Flat Top duration expressed in sampling clock unit (10 ns).
[31:10]	Reserved

Peaking Time

Position in the flat top region where the samples are used for the calculation of the peak height. The peaking time is referred to the trigger position or to the trigger validation signal according to the trigger mode. Check the User Manual for further details.

Address	0x1n64, 0x8064
Mode	R/W
Attribute	I

Bit	Description
[10:0]	Peaking time expressed in sampling clock unit (10 ns).
[31:11]	Reserved

Decay Time

This register corresponds to the trapezoid pole-zero cancellation. The user must set this register equal to the decay time of the pre-amplifier.

Address	0x1n68, 0x8068
Mode	R/W
Attribute	I

Bit	Description
[15:0]	Decay time expressed in sampling clock unit (10 ns).
[31:16]	Reserved

Trigger Threshold

Threshold of the Trigger and Timing filter of the DPP-PHA algorithm. The threshold arms the RC-CR2 signal and the event is identified (trigger) on the RC-CR2 zero crossing.

Address	0x1n6C, 0x806C
Mode	R/W
Attribute	I

Bit	Description
[13:0]	Trigger Threshold value expressed in LSB unit.
[31:14]	Reserved

Rise Time Validation Window

The Rise Time Validation Window is used by the rise time discriminator (RTD) to reject pulses that overlap in the rise time. Such events are identified by a longer RC-CR2 signal (the RC-CR2 gets longer to reach the zero crossing and therefore to trigger) than the RC-CR2 of a single pulse. The rise time validation window starts in correspondence with the RC-CR2 threshold crossing and lasts for the duration written in this register. If no trigger occurs within this acceptance window, the algorithm consider the event as a pile-up and reject it.

Address	0x1n70, 0x8070
Mode	R/W
Attribute	I

Bit	Description
[9:0]	Rise Time Validation Window expressed in sampling clock unit (10 ns). When 0, the RTD is disabled.
[31:10]	Reserved

Trigger Hold-Off

The Trigger Hold-Off is a logic signal of programmable width generated by the trigger logic in correspondence of the fast discriminator output. Other triggers are inhibited for the overall Trigger Hold-Off duration.

Address	0x1n74, 0x8074
Mode	R/W
Attribute	I

Bit	Description
[5:0]	Trigger Hold-Off width expressed in steps of 80 ns.
[31:6]	Reserved

Peak Hold-Off

The Peak Hold-off starts at the end of the trapezoid flat top and defines how close must be two trapezoids to be considered piled-up. Zero is the case where the flat top of one trapezoid starts exactly at the end of the flat top of the previous one.

Address	0x1n78, 0x8078
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Peak hold-off expressed in steps of 80 ns.
[31:8]	Reserved

Baseline Hold-Off

The Baseline Hold-off defines how long the baseline is kept frozen beyond the end of the trapezoid; after that time, the baseline starts to be calculated again. Depending on the baseline mean value, the baseline itself might take some time to recover after the hold-off.

Address	0x1n7C, 0x807C
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Baseline Hold-Off expressed in steps of the sampling clock unit (10 ns).
[31:8]	Reserved

DPP Algorithm Control

Management of the DPP algorithm features

Address	0x1n80, 0x8080
Mode	R/W
Attribute	I

Bit	Description
[5:0]	Trapezoid Rescaling: the trapezoid generated by the energy filter in the FPGA is k*M times higher than the input pulse, where k is the trapezoid rise time and M is the input signal decay time. This value is internally represented over 48 bits and must be rescaled to 15 bit (i.e. 32K channels) before it is used to calculate the energy value (=pulse height). The trapezoid rescaling SHF defines how many bits are right shifted (i.e. division by 2^{SHF}) before applying the mask with 0x3FFF and extract the 15 bit value of the pulse height. Use a value for SHF such that $2^{SHF} <= M*k < 2^{SHF+1}$.
[7:6]	Reserved
[9:8]	Decimation: the input signal samples can be averaged within the number of samples defined by the decimation. This has the analogous effect of reducing the sampling frequency of the board. Options are: 00: Decimation disabled; 01: 2 samples (50 MSps); 10: 4 samples (25 MSps); 11: 8 samples (12.5 MSps).
[11:10]	Decimation Gain. This gain can be used in conjunction with the decimation (see bits[9:8]) to multiply the input samples by the same factor of the decimation and avoid losses in the resolution. Decimation gain is added to the trapezoid rescaling (bits[5:0]). Options are: 00: Digital Gain = 1; 01: Digital Gain = 2 (only with decimation >= 2 samples); 10: Digital Gain = 4 (only with decimation >= 4 samples); 11: Digital Gain = 8 (only with decimation = 8 samples).
[13:12]	Peak Mean: corresponds to the number of samples for the averaging window of the trapezoid height calculation. Note: for a correct energy calculation the Peak Mean should be contained in the flat region of the Trapezoid Flat Top. Options are: 00: 1 sample; 01: 4 samples; 10: 16 samples; 11: 64 samples.
[14]	Reserved
[15]	Enable Spike Rejection. When this bit is enabled triggers are inhibited until the ”Input Rise Time” duration is reached (register 0x1n58). In case of noisy signals this feature is quite useful to avoid triggering on spikes on the rise time of the RC-CR2 signal, which do not corresponds to real signals. This feature allows also the use to set lower values of the trigger threshold. Options are: 0: disabled; 1: enabled.
[16]	Invert Input: Individual setting for the input signal inversion. The DPP-PHA algorithm is designed to work with positive signals. In case of negative polarity the signal is inverted in the FPGA to make it positive. Options are: 0: positive polarity; 1: negative polarity.
[17]	Pulse Identification on RC-CR or RC-CR2 signal. Events are usually identified on the zero crossing of the RC-CR2 signal. For fast input signals it is possible to trigger on the zero crossing of the RC-CR signal (which becomes bipolar for fast signals). Options are: 0: Trigger on RC-CR2; 1: Trigger on RC-CR.

[19:18]	Trigger Mode. Options are: 00: Normal mode. Each channel self-triggers independently from the other channels; 01: Neighbour mode. Each channel can self-trigger independently from the other channels and it saves the event also when either the previous or the consecutive channel triggers as well; 10: Coincidence mode. Each channel can self-trigger independently from the other channels and it saves the event only when a validation signal occurs within its coincidence window (register 0x1n84); 11: Anti-coincidence mode. Each channel can self-trigger independently from the other channels and it saves the event only when no validation signal occurs within its coincidence window (register 0x1n84).
[22:20]	Baseline averaging window: number of samples for the baseline average calculation. Options are: 000: the baseline is not evaluated, and the energy values are not subtracted by the baseline; 001: 16 samples; 010: 64 samples; 011: 256 samples; 100: 1024 samples; 101: 4096 samples; 110: 16384 samples; 111: reserved.
[23]	Reserved
[24]	Disable Self Trigger. When disabled, the self-trigger (fast discriminator output) is still propagated to the mother board for coincidence logic and TRG- OUT front panel connector, though it is not used by the channel to acquire the event. Options are: 0: self-trigger used to acquire and propagated to the trigger logic; 1: self-trigger only propagated to the trigger logic.
[25]	Fake Event in case of Time Reset signal from GPI (S-IN in case of VME form factor). Set this bit to 1 to enable a fake-event write in case of reset from GPI. The fake event is tagged by bit[3] of the EXTRAS word of the Channel Aggregate data format. Check the User Manual for further details. Options are: 0: disabled; 1: enabled.
[26]	Fake Event in case of Time Stamp roll over. Set this bit to 1 to enable a fake-event saving in case of internal time stamp roll over. The fake event is tagged from bit[3] of the EXTRAS word of the Channel Aggregate data format. Check the User Manual for further details. Options are: 0: disabled; 1: enabled.
[27]	Energy calculation in case of piled-up events. When a pile-up occurs the board returns energy = 0; set this bit if you want the energy evaluated also for piled-up events. Events are flagged as pile-up though bit[16] of the last word of the Channel Aggregate data format. The energy value is anyway not corrected. Check the User Manual for further details. Options are: 0: disabled; 1: enabled.
[31:29]	Reserved

Shaped Trigger Width

The Shaped Trigger (i.e. Fast Discriminator Output) is a logic signal generated by a channel in correspondence with its local self- trigger. It is used to propagate the trigger to the other channels of the board and to other external boards, as well as to feed the coincidence trigger logic.

Address	0x1n84, 0x8084
Mode	R/W
Attribute	I

Bit	Description
[7:0]	Shaped Trigger (Fast Discriminator Output) width in steps of 10 ns.
[31:8]	Reserved

Channel n Status

This register contains the status information of channel n.

Address	0x1n88
Mode	R
Attribute	I

Bit	Description
[1:0]	Reserved
[2]	If 1, the SPI bus is busy, and it is not possible to access registers 0x1nB4 and 0x1nB8
[31:3]	Reserved

AMC Firmware Revision

Returns the DPP firmware revision (mezzanine level).
To control the mother board firmware revision see register 0x8124.
For example: if the register value is 0xC3218303:
- Firmware Code and Firmware Revision are 131.3;
- Build Day is 21;
- Build Month is March;
- Build Year is 2012.

Note: since 2016 the build year started again from 0.

Address	0x1n8C
Mode	R
Attribute	I

Bit	Description
[7:0]	Firmware revision number
[15:8]	Firmware DPP code. Each DPP firmware has a unique code.
[19:16]	Build Day (lower digit)
[23:20]	Build Day (upper digit)
[27:24]	Build Month. For example: 3 means March, 12 is December.
[31:28]	Build Year. For example: 0 means 2000, 12 means 2012. Note: since 2016 the build year started again from 0.

DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to 2^{NBit} - 1, where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.
Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.
WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	I

Bit	Description
[15:0]	DC Offset value in DAC LSB unit
[31:16]	Reserved

Input Dynamic Range

The analog input stage of 780 series has 4 programmable gains. This register modifies the analog gains of channel n and therefore its input dynamics.

Address	0x1nB4, 0x80B4
Mode	R/W
Attribute	I

Bit	Description
[3:0]	Selects the channel input range of 780 series. Options are: 0x5: 0.6 Vpp; 0x6: 1.4 Vpp; 0x9: 3.7 Vpp; 0xA: 9.5 Vpp.
[31:4]	Reserved

Board Configuration

This register contains general settings for the board configuration.

Address	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode	R/W
Attribute	C

Bit	Description
[0]	Reserved: must be 0.
[1]	Reserved: must be 0
[2]	Trigger Propagation: enables the propagation of the individual trigger from mother board individual trigger logic to the mezzanine. This is required in case of coincidence trigger mode
[3]	Reserved: must be 0
[4]	Reserved: must be 1.
[7:5]	Reserved: must be 0
[8]	Individual trigger: must be 1
[9]	Reserved: must be 0
[10]	Reserved: must be 0
[11]	Dual Trace: in oscilloscope or mixed mode, it is possible to plot two different waveforms. When the dual trace is enabled, the samples of the two signals are interleaved, thus each waveform is recorded at half of the ADC frequency. The two analog probes can be selected from bits[13:12] and bits[15:14] respectively.
[13:12]	Analog Probe 1: Selects which signal is associated to the Analog trace 1 in the readout data. Options are: 00: Input; 01: RC-CR (input 1st derivative); 10: RC-CR2 (input 2nd derivative); 11: Trapezoid (output of the trapezoid filter).
[15:14]	Analog Probe 2: Selects which signal is associated to the Analog trace 2 in the readout data. Options are: 00: Input; 01: Threshold, which is referred to the RC-CR2 signal; 10: Trapezoid - Baseline; 11: Baseline (of the trapezoid).
[16]	Waveform Recording: enables the data recording of the waveform. The user must define the number of samples to be saved in the Record Length (register 0x1n20). According to the Analog Probe option one or two waveforms are saved. Options are: 0: disabled; 1: enabled.
[17]	Energy Mode: When enabled, the height of the trapezoid (which corresponds to the peak amplitude of the pulses) is saved into the event data (last word of the event). Options are: 0: Energy Mode disabled. 1: Energy Mode enabled.
[18]	Time Stamp Recording: When enabled, the time stamp of the event (which corresponds to the zero crossing in the RC-CR2 timing filter) is saved into the event data (first word of the event). 0: Time Stamp recording disabled. 1: Time Stamp recording enabled.
[19]	Reserved: must be 0

[23:20]	Digital Virtual Probe 1: when the mixed (or oscilloscope) mode is enabled, the following digital virtual probes can be selected. Check the User Manual for further details. 0000: shows the RT Discrimination Width; 0001: ”Armed”, digital input showing where the RC-CR2 crosses the Threshold; 0010: ”Peak Run”, starts with the trigger and last for the whole event; 0011: ”Peak Abort”, corresponds to the time interval when the energy calculation is disabled due to the pile-up event; 0100: ”Peaking”, shows where the energy is calculated; 0101: ”Trg Validation Win”, digital input showing the trigger validation acceptance window TVAW; 0110: ”BSL Holdoff”, shows the baseline hold-off parameter; 0111: ”TRG Holdoff”, shows the trigger hold-off parameter; 1000: ”Trg Validation”, shows the trigger validation signal TRG_VAL ; 1001: ”Acq Veto”, this is 1 when either the input signal is saturated or the memory board is full.
[24]	Enable the FORMAT Word in the aggregate data. It must be 1.
[31:25]	Reserved

Aggregate Organization

The internal memory of the digitizer can be divided into a programmable number of aggregates, where each aggregate contains a specific number of events. This register defines how many aggregates can be contained in the memory. Note: this register must not be modified while the acquisition is running.

Address	0x800C
Mode	R/W
Attribute	C

Bit	Description
[3:0]	Aggregate Organization Nb: the number of aggregates is equal to N_aggr = 2^{Nb}. The corresponding values of Nb and N_aggr are: Nb: N_aggr 0x0 - 0x1: Not used 0x2 : 4 0x3 : 8 0x4 : 16 0x5 : 32 0x6 : 64 0x7 : 128 0x8 : 256 0x9 : 512 0xA : 1024
[31:4]	Reserved: must be 0

Record Length

Sets the record length for the waveform acquisition

Address	0x8020
Mode	R/W
Attribute	C

Bit	Description
[15:0]	Number of samples in the waveform according to the formula Ns = N * 2, where Ns is the record length and N is the register value. For example, write N = 10 to acquire 20 samples. Each sample corresponds to 10 ns.
[31:16]	Reserved

Acquisition Control

This register manages the acquisition settings.

Address	0x8100
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). If the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off; 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Trigger Counting Mode. Through this bit it is possible to count the reading requests from channels to mother board. The reading requests may come from the following options: 0 = accepted triggers from combination of channels; 1 = triggers from combination of channels, in addition to TRG-IN and SW TRG.
[5:4]	Reserved
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. NOTE: this bit is reserved in case of VME boards.
[31:7]	Reserved

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address	0x8104
Mode	R
Attribute	C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. This bit drives the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' is on).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. NOTE: the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if at least one channel has reached the FULL condition. Options are: 0 = no channel has reached the FULL condition; 1 = the maximum number of events to be read is reached.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	PLL Bypass Mode. This bit drives the front panel 'PLL BYPS' LED. Options are: 0 = PLL bypass mode is not active ('PLL BYPS' is off); 1 = PLL bypass mode is active and the VCXO frequency directly drives the clock distribution chain ('PLL BYPS' lits). WARNING: before operating in PLL Bypass Mode, it is recommended to contact CAEN for feasibility.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL hasn not had any unlock condition since the last register read access. NOTE: flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronised). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. NOTE: this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the current logical level on TRG-IN front panel connector.
[31:17]	Reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address	0x810C
Mode	R/W
Attribute	C

Bit	Description
[0]	Enables the trigger request from channel 0 to participate to the global trigger logic. Options are: 0 = disabled; 1 = enabled.
[1]	Enables the trigger request from channel 1 to participate to the global trigger logic. Options are: 0 = disabled; 1 = enabled.
[19:2]	Reserved
[23:20]	Majority Coincidence Window. Sets the time window (10 ns steps) for the majority coincidence. Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [1:0]) .
[29:27]	Reserved
[30]	External Trigger. When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals (bit[31] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals (bit[30] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[0]	Enables the trigger request from channel 0 to participate to the TRG-OUT logic. Options are: 0 = disabled; 1 = enabled.
[1]	Enables the trigger request from channel 1 to participate to the TRG-OUT logic. Options are: 0 = disabled; 1 = enabled.
[3:2]	Reserved
[7:4]	Reserved
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = Reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [1:0]) .
[29:14]	Reserved
[30]	External Trigger. When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[31] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[30] and bits[1:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel I/O Control

This register manages the front panel I/O connectors.

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[9:1]	Reserved
[9:1]	Reserved
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. NOTE: if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1= TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN: the signal is active when the acquisition is running. This option can be used with VME boards to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN daisy chain; 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY_UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].

[20]	BUSY_UNLOCK Select. Selects the BUSY_UNLOCK signal type to be propagated on TRG-OUT (GPO) when bits[19:18] = 11. Options are: 0 = Board BUSY; 1 = PLL Lock Loss. NOTE: this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower.
[22:21]	Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (TRG OPTIONS field in case of DT and NIM boards). Option are: 00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default); NOTE: 00 is meaningless in case of DT and NIM boards. 01 = EVENT TRIGGER SOURCE: 16-bit PATTERN/TRG OPTIONS indicates the trigger source causing the event acquisition; 10 = EXTENDED TRIGGER TIME TAG: enables the Trigger Time Tag information over 48 bits. The 16 most significant bits are given by the 16-bit PATTERN/TRG OPTIONS field, while the remaining 32 ones are given by the TRIGGER TIME TAG information in the header of the event format (roll-over bit is not managed). 11 = NOT USED: if configured, it acts like 00 setting. NOTE: Refer to the Event Structure section of the digitizer User Manual for a complete information.
[31:23]	Reserved.

Channel Enable Mask

This register enables/disables selected channels to participate in the event readout. Disabled channels are not operative.
WARNING: this register must not be modified while the acquisition is running.

Address	0x8120
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Bit n can enable/disable selected channel n to participate to the event readout. Options are: 0: disabled; 1: enabled.
[31:2]	Reserved

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:
Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)
EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.
EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.
NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.
A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.
EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.
NOTE: this register is supported by VME boards only.
NOTE: the command must be issued starting from the first to the last board in the clock chain.
NOTE: if a Sync command is intentionally issued, the user must consider that a new channels calibration procedure is needed for a correct board operating (see 0x809C).

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Digitizer Family Code: 0x7: 780 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 1: each channel is equipped with 512 kS acquisition memory; 8: each channel is equipped with 4 MS acquisition memory. For x780 and x781 this is always 1.
[23:16]	Equipped Channels Number, i.e. 2.
[31:24]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event Size (32-bit words).

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay, expressed in trigger clock cycles between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG-IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[31:0]	RUN/START/STOP Delay (expressed in trigger clock cycles, i.e. 10 ns).

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.
NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Internal Communication Timeout. Options are: 0000 = no error; Others = Timeout Error occurred.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved

Disable External Trigger

The External Trigger on TRG-IN connector can be disabled through this register. Any functionality related to TRG-IN is disabled as well.

Address	0x817C
Mode	R/W
Attribute	C

Bit	Description
[0]	Options are: 0: external trigger enabled; 1: external trigger disabled.
[31:1]	Reserved

Trigger Validation Mask

Sets the trigger validation logic

Address	0x8188 (ch0), 0x818C (ch1)
Mode	R/W
Attribute	I

Bit	Description
[3:0]	Sets the trigger request that participates to the generation of the trigger validation signal. Options are: 0000: reserved; 0010: reserved; 0100: channel 0; 1000: channel 1.
[7:4]	Reserved
[9:8]	Operation Mask. Sets the logic operation among the enabled trigger request signals. Options are: 00: OR; 01: AND; 10: majority; 11: reserved.
[12:10]	Majority Level. Allowed level values are 0 and 1. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [3:0]) .
[29:13]	Reserved
[30]	External Trigger: when enabled the external trigger from TRG-IN front panel connector participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.
[31]	Software Trigger: when enabled the software trigger participates to the trigger validation generation (in logic OR). Options are: 0: disabled; 1: enabled.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address	0xEF00
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved
[3]	Optical Link Interrupt Enable. Options are: 0 = Optical Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[31:4]	Reserved

Readout Status

This register contains information related to the readout.

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Output Buffer Status. Indicates if the Output Buffer is in Full condition. Options are: 0 = the Output Buffer is not FULL; 1 = the Output Buffer is FULL.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). NOTE: this bit is reset after register readout at 0xEF04.
[31:3]	Reserved.

Aggregate Number per BLT

This register sets the maximum number of complete aggregates which has to be transferred for each block transfer (via VME BLT/CBLT cycles or block readout through Optical Link).

Address	0xEF1C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Number of complete aggregates to be transferred for each block transfer (BLT).
[31:8]	Reserved

Scratch

This register can be used to write/read words for test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:
- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command does not change the registers actual value, except for resetting the following registers:
- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

This register contains information on 8-bit checksum of Configuration ROM space.

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options for 780 digitizer family are: x780M: 0x90; x780N: 0x91; x780P: 0x92.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on- board.

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: Reserved (value = 0).

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