CAEN
Tools for Discovery

Electronic Instrumentation

User Manual UM5483

740 Family

Waveform Recording Firmware Registers

Rev. 0 - 28 October 2016

Purpose of this Manual

The User Manual contains the full description of the Waveform Recording firmware registers for 740 digitizer family. The description is compliant with the firmware revision **4.10_0.11**. For future release compatibility, check in the firmware history files.

Change Document Record

Date	Revision	Changes
28 October 2016	00	First release unified for 740 digitizer family

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

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MADE IN ITALY: We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked "MADE IN ITALY", we cannot attest to the manufacturing process of "third party" boards).

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1 Registers and Data Format

All registers described in the User Manual are 32-bit wide. In case of VME access, **A24** and **A32** addressing mode can be used.

Reset and Clear

The module's registers can be set back to their default values on software reset command by writing in the Software Reset register or by system reset from backplane, in case of VME boards. In particular, the registers or buffers listed below

- Event Readout Buffer
- Buffer Occupancy
- Event Stored
- Event Size

are also be set back to their default values (registers) or emptied (buffers) by a clear issued:

- automatically by the firmware at the start of each run;
- on software command by writing in the Software Clear register
- by hardware (VME boards only), through the LVDS interface properly configured (see the section "Front Panel LVDS I/Os" of the digitizer User Manual).

Register Address Map

The table below reports the complete list of registers that can be accessed by the user. The register names in the first column can be clicked to be redirected to the relevant register description. The register address is reported on the second column as a hex value. The third column indicates the allowed register access mode, where:

R	**Read only**. The register can be accessed in read only mode.
W	**Write only**. The register can be accessed in write only mode.
R/W	**Read and write**. The register can be accessed both in read and write mode.

According to the attribute reported in the fourth column, the following choices are available:

G **Group register**. In case of 740 and 742 digitizer families, some registers manage **groups** of channels. Group registers have M instances, where M is the total number of groups. Write access can be performed in single group mode (one group at a time) or broadcast (simultaneous write access to all groups). Read command must be in single group mode. Single group access can be performed at address 0x1nXY, where n identifies the n^{th} group, while broadcast write can be performed at the address 0x80XY. For example:

- access to address 0x1320 to read/write register 0x1n20 for group 3 of the board. In case of 740 and 742 board, group 3 corresponds to channels from 24 to 31 (8 channels per group). The same value is applied to all channels in the same group.
- to write the same value for all groups in the board, access to 0x8020 (broadcast write). To read the corresponding value, access to the individual address 0x1n20.

C **Common register**. Register with this attribute has a single instance, therefore read and write access can be performed at address 0x80XY only.

Register Name	Address	Mode	Attribute
Event Readout Buffer	0x0000 - 0x0FFC	R	C
Dummy32	0x1n24, 0x8024	R/W	G
Group n Trigger Threshold	0x1n80, 0x8080	R/W	G
Group n Status	0x1n88	R	G
AMC Firmware Revision	0x1n8C	R	G
DC Offset	0x1n98, 0x8098	R/W	G
Channel Enable Mask of Group n	0x1nA8, 0x80A8	R/W	G
Group n Low Channels DC Offset Individual Correction	0x1nC0, 0x80C0	R/W	G
Group n High Channels DC Offset Individual Correction	0x1nC4, 0x80C4	R/W	G
Board Configuration	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)	R/W	C
Buffer Organization	0x800C	R/W	C
Custom Size	0x8020	R/W	C
Decimation Factor	0x8044	R/W	C
Acquisition Control	0x8100	R/W	C
Acquisition Status	0x8104	R	C
Software Trigger	0x8108	W	C
Global Trigger Mask	0x810C	R/W	C
Front Panel TRG-OUT (GPO) Enable Mask	0x8110	R/W	C
Post Trigger	0x8114	R/W	C
LVDS I/O Data	0x8118	R/W	C
Front Panel I/O Control	0x811C	R/W	C
Group Enable Mask	0x8120	R/W	C
ROC FPGA Firmware Revision	0x8124	R	C
Event Stored	0x812C	R	C
Set Monitor DAC	0x8138	R/W	C
Software Clock Sync	0x813C	W	C
Board Info	0x8140	R	C
Monitor DAC Mode	0x8144	R/W	C
Event Size	0x814C	R	C
Fan Speed Control	0x8168	R/W	C
Memory Buffer Almost Full Level	0x816C	R/W	C
Run/Start/Stop Delay	0x8170	R/W	C
Board Failure Status	0x8178	R	C
Front Panel LVDS I/O New Features	0x81A0	R/W	C
Buffer Occupancy Gain	0x81B4	R/W	C
Readout Control	0xEF00	R/W	C
Readout Status	0xEF04	R	C
Board ID	0xEF08	R/W	C
MCST Base Address and Control	0xEF0C	R/W	C
Relocation Address	0xEF10	R/W	C
Interrupt Status/ID	0xEF14	R/W	C
Interrupt Event Number	0xEF18	R/W	C
Max Number of Events per BLT	0xEF1C	R/W	C
Scratch	0xEF20	R/W	C
Software Reset	0xEF24	W	C
Software Clear	0xEF28	W	C
Configuration Reload	0xEF34	W	C
Configuration ROM Checksum	0xF000	R	C
Configuration ROM Checksum Length BYTE 2	0xF004	R	C
Configuration ROM Checksum Length BYTE 1	0xF008	R	C
Configuration ROM Checksum Length BYTE 0	0xF00C	R	C
Configuration ROM Constant BYTE 2	0xF010	R	C
Configuration ROM Constant BYTE 1	0xF014	R	C

Configuration ROM Constant BYTE 0	0xF018	R	C
Configuration ROM C Code	0xF01C	R	C
Configuration ROM R Code	0xF020	R	C
Configuration ROM IEEE OUI BYTE 2	0xF024	R	C
Configuration ROM IEEE OUI BYTE 1	0xF028	R	C
Configuration ROM IEEE OUI BYTE 0	0xF02C	R	C
Configuration ROM Board Version	0xF030	R	C
Configuration ROM Board Form Factor	0xF034	R	C
Configuration ROM Board ID BYTE 1	0xF038	R	C
Configuration ROM Board ID BYTE 0	0xF03C	R	C
Configuration ROM PCB Revision BYTE 3	0xF040	R	C
Configuration ROM PCB Revision BYTE 2	0xF044	R	C
Configuration ROM PCB Revision BYTE 1	0xF048	R	C
Configuration ROM PCB Revision BYTE 0	0xF04C	R	C
Configuration ROM FLASH Type	0xF050	R	C
Configuration ROM Board Serial Number BYTE 1	0xF080	R	C
Configuration ROM Board Serial Number BYTE 0	0xF084	R	C
Configuration ROM VCXO Type	0xF088	R	C

Event Readout Buffer

This is the addressment space for the event readout. The event is a series of 32-bit words according to the event structure defined in the digitizer User Manual.

Address	0x0000 - 0x0FFC
Mode	R
Attribute	C

Bit	Description
[31:0]	32-bit word of the event.

Dummy32

Writing and reading at this register can be used for debug purposes.

Address	0x1n24, 0x8024
Mode	R/W
Attribute	G

Bit	Description
[31:0]	Dummy32 value (default value is 0).

Group n Trigger Threshold

Each 8-channel group (Group 0 = Ch0..7, Group 1 = Ch8..15, etc.) is able to generate a trigger request signal when the input pulse exceeds a configurable threshold Vth on at least one of the enabled channels. This register allows to set Vth common to all the channels of the group.

Address	0x1n80, 0x8080
Mode	R/W
Attribute	G

Bit	Description
[11:0]	Vth = Trigger Threshold Value expressed in LSB (default value is 0). 1LSB = InputDynamicRange/2^{12bit}
[31:12]	Reserved.

Group n Status

This register contains the status information common to all the channels of group n.

Address	0x1n88
Mode	R
Attribute	G

Bit	Description
[0]	Memory Full.
[1]	Memory Empty.
[2]	Group n DAC Busy. Options are: 0 = DC offset updated; 1 = Busy.
[31:3]	Reserved.

AMC Firmware Revision

This register contains the channel FPGA (AMC) firmware revision information.
The complete format is:

Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)

EXAMPLE 1: revision 1.03, November 12th, 2007 is 0x7B120103.

EXAMPLE 2: revision 2.09, March 7th, 2016 is 0x03070209.

NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x1n8C
Mode	R
Attribute	G

Bit	Description
[7:0]	AMC Firmware Minor Revision Number (Y).
[15:8]	AMC Firmware Major Revision Number (X).
[31:16]	AMC Firmware Revision Date (Y/M/DD).

DC Offset

This register allows to adjust the baseline position (i.e. the 0 Volt) of the input signal on the ADC scale. The ADC scale ranges from 0 to $2^{NBit} - 1$, where NBit is the number of bits of the on-board ADC. The DAC controlling the DC Offset has 16 bits, i.e. it goes from 0 to 65535 independently from the NBit value and the board type.
Typically a DC Offset value of 32K (DAC mid-scale) corresponds to about the ADC mid-scale. Increasing values of DC Offset make the baseline decrease. The range of the DAC is about 5% (typ.) larger than the ADC range, hence DAC settings close to 0 and 64K correspond to ADC respectively over and under range.

WARNING: before writing this register, it is necessary to check that bit[2] = 0 at 0x1n88, otherwise the writing process will not run properly!

Address	0x1n98, 0x8098
Mode	R/W
Attribute	G

Bit	Description
[15:0]	DC Offset value in DAC LSB unit (default value is 32K).
[31:16]	Reserved.

Channel Enable Mask of Group n

Enable/disable selected channels of group n to participate to the event readout.

NOTE: this register must not be modified while the acquisition is running.

Address	0x1nA8, 0x80A8
Mode	R/W
Attribute	G

Bit	Description
[7:0]	Bit m enables/disables channel m of group n to participate to the event readout. Options are: 0 = disabled; 1 = enabled.
[31:8]	Reserved.

Group n Low Channels DC Offset Individual Correction

The DC Offset set through the 0x1n98 register applies commonly to all the channels of the group, but the channel baselines usually result misaligned due to intrinsic offset. In order to align the baselines and so guarantee a trigger threshold setting (0x1n80) effective on all the channels, this register allows to apply a 8-bit positive offset correction to the ADC output value individually for the four low channels of group n.

EXAMPLE: applying a 255 offset value (FF) to channel 2 of group 3 implies writing 0x00FF0000 at register address 0x13C0.

NOTE: this register is supported from AMC FPGA default firmware revision 0.10 on.

Address	0x1nC0, 0x80C0
Mode	R/W
Attribute	G

Bit	Description
[31:0]	Individual DC Offset Mask. Options are: 0x000000FF = applies a FF (255) DC offset to the first channel of group n; 0x0000FF00 = applies a FF (255) DC offset to the second channel of group n; 0x00FF0000 = applies a FF (255) DC offset to the third channel of group n; 0xFF000000 = applies a FF (255) DC offset to the fourth channel of group n.

Group n High Channels DC Offset Individual Correction

According to what described for 0x1nC0, this register allows to apply a 8-bit positive offset correction to the ADC output value individually for the four high channels of group n.

EXAMPLE: applying a 255 offset correction (FF) to channel 6 of group 5 implies writing 0x0000FF00 at register address 0x16C4.

NOTE: this register is supported from AMC FPGA default firmware revision 0.10 on.

Address	0x1nC4, 0x80C4
Mode	R/W
Attribute	G

Bit	Description
[31:0]	Individual DC Offset Mask. Options are: 0x000000FF = applies a FF (255) offset correction to the fifth channel of group n; 0x0000FF00 = applies a FF (255) offset correction to the sixth channel of group n; 0x00FF0000 = applies a FF (255) offset correction to the seventh channel of group n; 0xFF000000 = applies a FF (255) offset correction to the eighth channel of group n.

Board Configuration

This register contains general settings for the board configuration.

Address	0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Mode	R/W
Attribute	C

Bit	Description
[0]	Reserved: must be 0.
[1]	Trigger Overlap Setting (default value is 0). When two acquisition windows are overlapped, the second trigger can be either accepted or rejected. Options are: 0 = Trigger Overlapping Not Allowed (no trigger is accepted until the current acquisition window is finished); 1 = Trigger Overlapping Allowed (the current acquisition window is prematurely closed by the arrival of a new trigger). **NOTE:** it is suggested to keep this bit cleared in case of using a DPP firmware.
[2]	Reserved: must be 0.
[3]	Test Pattern Enable (default value is 0). This bit enables a triangular (0<-->3FFF) test wave to be provided at the ADCs input for debug purposes. Options are: 0 = disabled; 1 = enabled.
[4]	Reserved: must be 1.
[5]	Reserved: must be 0.
[6]	Self-trigger Polarity (default value is 0). Options are: 0 = Positive (the self-trigger is generated upon the input pulse overthreshold); 1 = Negative (the self-trigger is generated upon the input pulse underthreshold).
[8:7]	Reserved: must be 0.
[9]	Reserved.
[10]	Reserved: must be 0.
[22:11]	Reserved.
[23]	Reserved: must be 0.
[31:24]	Reserved.

Buffer Organization

Sets the number of buffers in which the channel memory can be divided. A write access to this register causes a software clear.
According to the BUFFER_CODE value written in the register, the number of buffers Nb is given by 2^{BUFFER_CODE}:

BUFFER_CODE	Nr.Buffers (Nb)	Buffer Size (Samples)
0x0	1	192k (SRAM 192kS/ch), 1.5M (SRAM 1.5MS/ch)
0x1	2	96k (SRAM 192kS/ch), 750k (SRAM 1.5MS/ch)
0x2	4	48k (SRAM 192kS/ch), 384k (SRAM 1.5MS/ch)
0x3	8	24k (SRAM 192kS/ch), 192k (SRAM 1.5MS/ch)
0x4	16	12k (SRAM 192kS/ch), 96k (SRAM 1.5MS/ch)
0x5	32	6k (SRAM 192kS/ch), 48k (SRAM 1.5MS/ch)
0x6	64	3k (SRAM 192kS/ch), 24k (SRAM 1.5MS/ch)
0x7	128	1536 (SRAM 192kS/ch), 12k (SRAM 1.5MS/ch)
0x8	256	768 (SRAM 192kS/ch), 6k (SRAM 1.5MS/ch)
0x9	512	384 (SRAM 192kS/ch), 3k (SRAM 1.5MS/ch)
0xA	1024	192 (SRAM 192kS/ch), 1536 (SRAM 1.5MS/ch)

To obtain a number of samples per buffer (referring to one channel) different from the table above, it is necessary to use the register address 0x8020. In this case, the BUFFER_CODE must be set to have the closest buffer size with a number of samples per buffer larger than the one set by 0x8020.

EXAMPLE: to have a desired number of samples per buffer of 900 (set through 0x8020), the BUFFER_CODE must be 0x07 in case of 192-kS/ch memory or 0x0A if 1.5-MS/ch one.

WARNING: this register must not be written while acquisition is running.

Address	0x800C
Mode	R/W
Attribute	C

Bit	Description
[3:0]	BUFFER_CODE
[31:4]	Reserved.

Custom Size

Writing the number of memory locations per event (N_LOC) in this register, the user can set the record length, which is the number of samples (Ns) of the digitized waveform in the acquisition window.

WARNING: this register must not be written while acquisition is running.

Address	0x8020
Mode	R/W
Attribute	C

Bit	Description
[31:0]	Number of Memory Locations per Event (N_LOC). Options are: 0 = Custom Size disabled (record length is given by the register address 0x800C); N_LOC = the number of samples of the record length is this given by the formula: 3*N_LOC = 2*Ns (3 locations = 2 samples) So, only values that are multiples of 3 are allowed for this register. **EXAMPLE:** to have 900 samples per buffer, the value to write is N_LOC = 0x258.

Decimation Factor

This register permits to program the decimation factor to be applied to the acquired waveforms, according to the formula:

$$(62.5/2^{n})MS/s$$

where n = [0,1,...,7].
Please, refer to the digitizer User Manual for details on this functionality.

NOTE: developers not using CAEN software must consider that this register setting affects the post- trigger (0x8114) and the acquisition window, that is to say the record length based on the buffer organization and the custom size settings (0x800C and 0x8020).

Address	0x8044
Mode	R/W
Attribute	C

Bit	Description
[3:0]	n parameter
[31:4]	Reserved.

Acquisition Control

This register manages the acquisition settings.

Address	0x8100
Mode	R/W
Attribute	C

Bit	Description
[1:0]	Start/Stop Mode Selection (default value is 00). Options are: 00 = SW CONTROLLED. Start/stop of the run takes place on software command by setting/resetting bit[2] of this register; 01 = S-IN/GPI CONTROLLED (S-IN for VME, GPI for Desktop/NIM). If the acquisition is armed (i.e. bit[2] = 1), then the acquisition starts when S-IN/GPI is asserted and stops when S-IN/GPI returns inactive. If bit[2] = 0, the acquisition is always off; 10 = FIRST TRIGGER CONTROLLED. If the acquisition is armed (i.e. bit[2] = 1), then the run starts on the first trigger pulse (rising edge on TRG-IN); this pulse is not used as input trigger, while actual triggers start from the second pulse. The stop of Run must be SW controlled (i.e. bit[2] = 0); 11 = LVDS CONTROLLED (VME only). It is like option 01 but using LVDS (RUN) instead of S-IN. The LVDS can be set using registers 0x811C and 0x81A0.
[2]	Acquisition Start/Arm (default value is 0). When bits[1:0] = 00, this bit acts as a Run Start/Stop. When bits[1:0] = 01, 10, 11, this bit arms the acquisition and the actual Start/Stop is controlled by an external signal. Options are: 0 = Acquisition STOP (if bits[1:0]=00); Acquisition DISARMED (others); 1 = Acquisition RUN (if bits[1:0]=00); Acquisition ARMED (others).
[3]	Trigger Counting Mode Selection. Options are: 0 = only accepted triggers are counted (default); 1 = all triggers are counted.
[4]	Reserved.
[5]	Memory Full Mode Selection (default value is 0). Options are: 0 = NORMAL. The board is full whenever all buffers are full; 1 = ONE BUFFER FREE. The board is full whenever Nb-1 buffers are full, where Nb is the overall number of buffers in which the channel memory is divided.
[6]	PLL Reference Clock Source (Desktop/NIM only). Default value is 0. Options are: 0 = internal oscillator (50 MHz); 1 = external clock from front panel CLK-IN connector. **NOTE:** this bit is reserved in case of VME boards.
[7]	Reserved.
[8]	LVDS I/O Busy Enable (VME only). Default value is 0. The LVDS I/Os can be programmed to accept a Busy signal as input, or to propagate it as output. Options are: 0 = disabled; 1 = enabled. **NOTE:** this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.

[9]	LVDS I/O Veto Enable (VME only). The LVDS I/Os can be programmed to accept a Veto signal as input, or to transfer it as output. Options are: 0 = disabled (default); 1 = enabled. **NOTE:** this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 should also be configured for nBusy/nVeto.
[10]	Reserved.
[11]	LVDS I/O RunIn Enable Mode (VME only). The LVDS I/Os can be programmed to accept a RunIn signal as input, or to transfer it as output. Options are: 0 = starts on RunIn level (default); 1 = starts on RunIn rising edge. **NOTE:** this bit is supported only by VME boards and meaningful only if the LVDS new features are enabled (bit[8]=1 of register 0x811C). Register 0x81A0 must also be configured for nBusy/nVeto.
[31:12]	Reserved.

Acquisition Status

This register monitors a set of conditions related to the acquisition status.

Address	0x8104
Mode	R
Attribute	C

Bit	Description
[1:0]	Reserved.
[2]	Acquisition Status. This bit drives the front panel 'RUN' LED. Options are: 0 = acquisition is stopped ('RUN' is off); 1 = acquisition is running ('RUN' is on).
[3]	Event Ready. Indicates if any events are available for readout. Options are: 0 = no event is available for readout; 1 = at least one event is available for readout. **NOTE:** the status of this bit must be considered when managing the readout from the digitizer.
[4]	Event Full. Indicates if the board memory has reached the FULL condition (i.e.maximum number of storable events). Options are: 0 = the board memory is not FULL; 1 = the board memory is FULL.
[5]	Clock Source. Indicates the clock source status. Options are: 0 = internal (PLL uses the internal 50 MHz oscillator as reference); 1 = external (PLL uses the external clock on CLK-IN connector as reference).
[6]	PLL Bypass Mode. This bit drives the front panel 'PLL BYPS' LED. Options are: 0 = PLL bypass mode is not active ('PLL BYPS' is off); 1 = PLL bypass mode is active and the VCXO frequency directly drives the clock distribution chain ('PLL BYPS' lits). **WARNING:** before operating in PLL Bypass Mode, it is recommended to contact CAEN for feasibility.
[7]	PLL Unlock Detect. This bit flags a PLL unlock condition. Options are: 0 = PLL has had an unlock condition since the last register read access; 1 = PLL hasn't had any unlock condition since the last register read access. **NOTE:** flag can be restored to 1 via read access to register 0xEF04.
[8]	Board Ready. This flag indicates if the board is ready for acquisition (PLL and ADCs are correctly synchronised). Options are: 0 = board is not ready to start the acquisition; 1 = board is ready to start the acquisition. **NOTE:** this bit should be checked after software reset to ensure that the board will enter immediately in run mode after the RUN mode setting; otherwise, a latency between RUN mode setting and Acquisition start might occur.
[14:9]	Reserved.
[15]	S-IN (VME boards) or GPI (DT/NIM boards) Status. Reads the current logical level on S-IN (GPI) front panel connector.
[16]	TRG-IN Status. Reads the current logical level on TRG-IN front panel connector.
[31:17]	Reserved.

Software Trigger

Writing this register causes a software trigger generation which is propagated to all the enabled channels of the board.

Address	0x8108
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a software trigger.

Global Trigger Mask

This register sets which signal can contribute to the global trigger generation.

Address	0x810C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Bit n corresponds to the trigger request from group n that participates to the global trigger generation (n = 0,...,3 for DT and NIM; n = 0,...,7 for VME boards). Options are: 0 = trigger request is not sensed for global trigger generation; 1 = trigger request participates in the global trigger generation. **NOTE:** in case of DT and NIMboards, only bits[3:0] are meaningful, while bits[7:4] are reserved.
[19:8]	Reserved. **NOTE:** in case of DT and NIM boards, bits[19:4] are reserved.
[23:20]	Majority Coincidence Window. Sets the time window (in units of the trigger clock) for the majority coincidence. Majority level must be set different from 0 through bits[26:24].
[26:24]	Majority Level. Sets the majority level for the global trigger generation. For a level m, the trigger fires when at least m+1 of the enabled trigger requests (bits[7:0] or [3:0]) are over-threshold inside the majority coincidence window (bits[23:20]). **NOTE:** the majority level must be smaller than the number of trigger requests enabled via bits[7:0] mask (or [3:0]).
[28:27]	Reserved.
[29]	LVDS Trigger (VME boards only). When enabled, the trigger from LVDS I/O participates to the global trigger generation (in logic OR). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger. When enabled, the external trigger on TRG-IN participates to the global trigger generation in logic OR with the other enabled signals (bit[31] and bits[7:0] or [3:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger participates to the global trigger signal generation in logic OR with the other enabled signals (bit[30] and bits[7:0] or [3:0]). Options are: 0 = disabled; 1 = enabled.

Front Panel TRG-OUT (GPO) Enable Mask

This register sets which signal can contribute to generate the signal on the front panel TRG-OUT LEMO connector (GPO in case of DT and NIM boards).

Address	0x8110
Mode	R/W
Attribute	C

Bit	Description
[7:0]	This mask sets the trigger requests participating in the TRG-OUT (GPO). Bit n corresponds to the trigger request from group n. Options are: 0 = Trigger request does not participate to the TRG-OUT (GPO) signal; 1 = Trigger request participates to the TRG-OUT (GPO) signal. **NOTE:** in case of DT and NIM boards, only bits[3:0] are meaningful while bis[7:4] are reserved.
[9:8]	TRG-OUT (GPO) Generation Logic. The enabled trigger requests (bits [7:0] or [3:0]) can be combined to generate the TRG-OUT (GPO) signal. Options are: 00 = OR; 01 = AND; 10 = Majority; 11 = reserved.
[12:10]	Majority Level. Sets the majority level for the TRG-OUT (GPO) signal generation. Allowed level values are between 0 and 7 for VME boards, and between 0 and 3 for DT and NIM boards. For a level m, the trigger fires when at least m+1 of the trigger requests are generated by the enabled channels (bits [7:0] or [3:0]) .
[28:13]	Reserved.
[29]	LVDS Trigger Enable (VME boards only). If the LVDS I/Os are programmed as outputs, they can participate in the TRG-OUT (GPO) signal generation. They are in logic OR with the other enabled signals (bits[31:30] and bits[7:0], or [3:0]). Options are: 0 = disabled; 1 = enabled.
[30]	External Trigger. When enabled, the external trigger on TRG-IN can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[31] and bits[7:0] or [3:0]). Options are: 0 = disabled; 1 = enabled.
[31]	Software Trigger. When enabled, the software trigger can participate in the TRG-OUT (GPO) signal generation in logic OR with the other enabled signals (bit[30], bits[7:0] or [3:0]). Options are: 0 = disabled; 1 = enabled.

Post Trigger

The value of this register is used to set the number of post-trigger samples, that is the number of further samples that are written by the FPGA in the channel memory, when a trigger occurs, before to freeze the buffer. The number of post trigger samples is:

$$Npost = PostTriggerValue + ConstantLatency$$

where:

Npost = number of post trigger samples.
PostTriggerValue = content of this register.
ConstantLatency = constant number of added samples due to the latency associated to the trigger processing logic in the ROC FPGA. This value is constant, but the exact value may change between different firmware revisions.

Address	0x8114
Mode	R/W
Attribute	C

Bit	Description
[31:0]	PostTriggerValue.

LVDS I/O Data

This register allows to readout the logic level of the LVDS I/Os if the LVDS pins are configured as outputs, and to set the logic level of the LVDS I/Os if the pins are configured as inputs (REGISTER mode).

NOTE: this register is supported only by VME boards.

Address	0x8118
Mode	R/W
Attribute	C

Bit	Description
[15:0]	LVDS I/O Data (VME boards only). If the LVDS I/O new features are enabled (bit[8] of 0x811C) and REGISTER mode is set (through 0x81A0), this register allows to read/write from the corresponding nth LVDS I/O according to its configuration. A write operation sets the corresponding pin logic state if configured as output, while a read operation returns the logic state of the corresponding pin if configured as input.
[31:16]	Reserved.

Front Panel I/O Control

This register manages the front panel I/O connectors.

Address	0x811C
Mode	R/W
Attribute	C

Bit	Description
[0]	LEMO I/Os Electrical Level. This bit sets the electrical level of the front panel LEMO connectors: TRG-IN, TRG-OUT (GPO in case of DT and NIM boards), S-IN (GPI in case of DT and NIM boards). Options are: 0 = NIM I/O levels; 1 = TTL I/O levels.
[1]	TRG-OUT Enable (VME boards only). Enables the TRG-OUT LEMO front panel connector. Options are: 0 = enabled (default); 1 = high impedance. **NOTE:** this bit is reserved in case of DT and NIM boards.
[2]	LVDS I/O [3:0] Direction (VME boards only). Sets the direction of the signals on the first 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. **NOTE:** this bit is reserved in case of DT and NIM boards.
[3]	LVDS I/O [7:4] Direction (VME boards only). Sets the direction of the second 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. **NOTE:** this bit is reserved in case of DT and NIM boards.
[4]	LVDS I/O [11:8] Direction (VME boards only). Sets the direction of the third 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. **NOTE:** this bit is reserved in case of DT and NIM boards.
[5]	LVDS I/O [15:12] Direction (VME boards only). Sets the direction of the fourth 4-pin group of the LVDS I/O connector. Options are: 0 = input; 1 = output. **NOTE:** this bit is reserved in case of DT and NIM boards.
[7:6]	LVDS I/O Signal Configuration (VME boards and LVDS I/O old features only). This configuration must be enabled through bit[8] set to 0. Options are: 00 = general purpose I/O; 01 = programmed I/O; 10 = pattern mode: LVDS signals are input and their value is written into the header PATTERN field; 11 = reserved. **NOTE:** these bits are reserved in case of DT and NIM boards.

[8]	LVDS I/O New Features Selection (VME boards only). Options are: 0 = LVDS old features; 1 = LVDS new features. The new features options can be configured through register 0x81A0. Please, refer to the User Manual for all details. **NOTE:** LVDS I/O New Features option is valid from motherboard firmware revision 3.8 on. **NOTE:** this bit is reserved in case of DT and NIM boards.
[9]	LVDS I/Os Pattern Latch Mode (VME boards only). Options are: 0 = Pattern (i.e. 16-pin LVDS status) is latched when the (internal) global trigger is sent to channels, in consequence of an external trigger. It accounts for post- trigger settings and input latching delays; 1 = Pattern (i.e. 16-pin LVDS status) is latched when an external trigger arrives. **NOTE:** this bit is reserved in case of DT and NIM boards.
[10]	TRG-IN control. The board trigger logic can be synchronized either with the edge of the TRG-IN signal, or with its whole duration. Note: this bit must be used in conjunction with bit[11] = 0. Options are: 0 = trigger is synchronized with the edge of the TRG-IN signal; 1 = trigger is synchronized with the whole duration of the TRG-IN signal.
[11]	TRG-IN to Mezzanines (channels). Options are: 0 = TRG-IN signal is processed by the motherboard and sent to mezzanine (default). The trigger logic is then synchronized with TRG-IN; 1 = TRG-IN is directly sent to the mezzanines with no mother board processing nor delay. This option can be useful when TRG-IN is used to veto the acquisition. **NOTE:** if this bit is set to 1, then bit[10] is ignored.
[13:12]	Reserved.
[14]	Force TRG-OUT (GPO). This bit can force TRG-OUT (GPO in case of DT and NIM boards) test logical level if bit[15] = 1. Options are: 0 = Force TRG-OUT (GPO) to 0; 1 = Force TRG-OUT (GPO) to 1.
[15]	TRG-OUT (GPO) Mode. Options are: 0 = TRG-OUT (GPO) is an internal signal (according to bits[17:16]); 1= TRG-OUT (GPO) is a test logic level set via bit[14].
[17:16]	TRG-OUT (GPO) Mode Selection. Options are: 00 = Trigger: TRG-OUT/GPO propagates the internal trigger sources according to register 0x8110; 01 = Motherboard Probes: TRG-OUT/GPO is used to propagate signals of the motherboards according to bits[19:18]; 10 = Channel Probes: TRG-OUT/GPO is used to propagate signals of the mezzanines (Channel Signal Virtual Probe); 11 = S-IN (GPI) propagation.
[19:18]	Motherboard Virtual Probe Selection (to be propagated on TRG- OUT/GPO). Options are: 00 = RUN: the signal is active when the acquisition is running. This option can be used with VME boards to synchronize the start/stop of the acquisition through the TRG-OUT->TR-IN or TRG-OUT->S-IN daisy chain; 01 = CLKOUT: this clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards; 10 = CLK Phase; 11 = BUSY_UNLOCK: this is the board BUSY in case of ROC FPGA firmware rel. 4.5 or lower. This probe can be selected according to bit[20].

[20]	BUSY_UNLOCK Select. Selects the BUSY_UNLOCK signal type to be propagated on TRG-OUT (GPO) when bits[19:18] = 11. Options are: 0 = Board BUSY; 1 = PLL Lock Loss. **NOTE:** this bit is reserved in case of ROC FPGA firmware rel. 4.5 or lower.
[22:21]	Pattern Configuration. Configures the information given by the 16-bit PATTERN field in the header of the event format (TRG OPTIONS field in case of DT and NIM boards). Option are: 00 = PATTERN: 16-bit pattern latched on the 16 LVDS signals as one trigger arrives (default); 01 = EVENT TRIGGER SOURCE: 16-bit PATTERN/TRG OPTIONS indicates the trigger source causing the event acquisition; 10 = EXTENDED TRIGGER TIME TAG: enables the Trigger Time Tag information over 48 bits. The 16 most significant bits are given by the 16-bit PATTERN/TRG OPTIONS field, while the remaining 32 ones are given by the TRIGGER TIME TAG information in the header of the event format (roll-over bit is not managed). 11 = NOT USED: if configured, it acts like 00 setting. **NOTE:** 00 is meaningless in case of DT and NIM boards. **NOTE:** refer to the Event Structure section of the digitizer User Manual for a complete information.
[31:23]	Reserved.

Group Enable Mask

This register enables/disablea selected groups to participate in the event readout.

WARNING: this register must not be modified while the acquisition is running.

Address	0x8120
Mode	R/W
Attribute	C

Bit	Description
[7:0]	Group Enable Mask. Bit n can enable/disable group n to participate in the event readout. Options are: 0: disabled; 1: enabled. **NOTE:** this function concerns only bits[3:0] in case of DT and NIM boards.
[31:8]	Reserved. **NOTE:** bits[31:4] are reserved in case of DT and NIM boards.

ROC FPGA Firmware Revision

This register contains the motherboard FPGA (ROC) firmware revision information.
The complete format is:

Firmware Revision = X.Y (16 lower bits)
Firmware Revision Date = Y/M/DD (16 higher bits)

EXAMPLE 1: revision 3.08, November 12th, 2007 is 0x7B120308.

EXAMPLE 2: revision 4.09, March 7th, 2016 is 0x03070409.

NOTE: the nibble code for the year makes this information to roll over each 16 years.

Address	0x8124
Mode	R
Attribute	C

Bit	Description
[7:0]	ROC Firmware Minor Revision Number (Y).
[15:8]	ROC Firmware Major Revision Number (X).
[31:16]	ROC Firmware Revision Date (Y/M/DD).

Event Stored

This register contains the number of events currently stored in the Output Buffer.

NOTE: the value of this register cannot exceed the maximum number of available buffers according to the register address 0x800C.

Address	0x812C
Mode	R
Attribute	C

Bit	Description
[31:0]	Number of the current events stored in the Output Buffer.

Set Monitor DAC

When the Voltage Level Mode is enabled (through 0x8144), this register sets the DAC value to be provided on the front panel MON/Sigma output LEMO connector: 1 LSB = 0.244 mV, terminated on 50 Ohm.

NOTE: this register is supported only by VME boards.

Address	0x8138
Mode	R/W
Attribute	C

Bit	Description
[11:0]	DAC Voltage Setting (VME boards only). The corresponding output value is multiplied by 0.244 mV.
[31:12]	Reserved

Software Clock Sync

At power-on, a Sync command is issued by the firmware to the ADCs to synchronize all of them to the clock of the board. In the standard operating, this command is not required to be repeated by the user.
A write access to this register (any value) forces the PLL to re-align all the clock outputs with the reference clock.

EXAMPLE: in case of Daisy chain clock distribution among VME boards, during the initialization and configuration, the reference clocks along the Daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLK-IN and the internal clocks.

NOTE: this register is supported by VME boards only.

NOTE: the command must be issued starting from the first to the last board in the clock chain.

Address	0x813C
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to generate a Sync command.

Board Info

This register contains the specific information of the board, such as the digitizer family, the channel memory size and the channel density.

Address	0x8140
Mode	R
Attribute	C

Bit	Description
[7:0]	Digitizer Family Code: 0x04 = 740 digitizer family.
[15:8]	Channel Memory Size Code. Options are: 0x02: each channel is equipped with 192 kS acquisition memory; 0x10: each channel is equipped with 1.5 MS acquisition memory.
[23:16]	Equipped Groups Number. Options are: 0x04 = 4 groups (DT and NIM boards) ; 0x08 = 8 groups (VME boards) . **NOTE:** if this number is lower than the physical group number, there could be a communication problem with some of the mezzanines.
[31:24]	Reserved.

Monitor DAC Mode

This register sets the output DAC mode of the MON/Sigma front panel LEMO connector.

NOTE: this register is supported by VME boards only.

Address	0x8144
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Monitor DAC Mode (VME boards only). Options are: 000 = Trigger Majority mode; 001 = Test mode; 010 = reserved; 011 = Buffer Occupancy mode; 100 = Voltage Level mode; Others = reserved. Please, refer to the digitizer User Manual for a detailed description.
[31:3]	Reserved.

Event Size

This register contains the current available event size in 32-bit words. The value is updated after a complete readout of each event.

Address	0x814C
Mode	R
Attribute	C

Bit	Description
[31:0]	Event Size (32-bit words).

Fan Speed Control

This register manages the on-board fan speed in order to guarantee an appropriate cooling according to the internal temperature variations.

NOTE: from revision 4 of the motherboard PCB (see register 0xF04C of the Configuration ROM), the automatic fan speed control has been implemented, and it is supported by ROC FPGA firmware revision greater than 4.4 (see register 0x8124).

Independently of the revision, the user can set the fan speed high by setting bit[3] = 1. Setting bit[3] = 0 will restore the automatic control for revision 4 or higher, or the low fan speed in case of revisions lower than 4.

NOTE: this register is supported by Desktop (DT) boards only.

Address	0x8168
Mode	R/W
Attribute	C

Bit	Description
[2:0]	Reserved: Must be 0.
[3]	Fan Speed Mode. Options are: 0 = slow speed or automatic speed tuning; 1 = high speed.
[5:4]	Reserved: Must be 1.
[31:6]	Reserved: Must be 0.

Memory Buffer Almost Full Level

This register allows to set the level for the Almost Full generation. The written value (ALMOST FULL LEVEL) represents the number of buffers that must be full of data before to assert the BUSY signal. This register takes part in the BUSY propagation among multiple boards.

NOTE: if this register is set to 0, the ALMOST FULL is a FULL.

For the Almost Full description, please refer to the Acquisition Synchronization section of the digitizer User Manual.

Address	0x816C
Mode	R/W
Attribute	C

Bit	Description
[10:0]	ALMOST FULL LEVEL.
[31:11]	Reserved.

Run/Start/Stop Delay

When the start of Run is given synchronously to several boards connected in Daisy chain, it is necessary to compensate for the delay in the propagation of the Start (or Stop) signal through the chain. This register sets the delay, expressed in trigger clock cycles between the arrival of the Start signal at the input of the board (either on S-IN/GPI or TRG-IN) and the actual start of Run. The delay is usually zero for the last board in the chain and rises going backwards along the chain.

Address	0x8170
Mode	R/W
Attribute	C

Bit	Description
[31:0]	Delay (in units of 8 ns).

Board Failure Status

This register monitors a set of board errors. In case of a failure, bit[26] in the second word of the event format header is set to 1 during data readout (refer to the digitizer User Manual for event structure description). Reading at this register checks which kind of error occurred.

NOTE: in case of problems with the board, the user is recommended to contact CAEN for support.

Address	0x8178
Mode	R
Attribute	C

Bit	Description
[3:0]	Internal Communication Timeout. Options are: 0000 = no error; Others = Timeout Error occurred.
[4]	PLL Lock Loss. Options are: 0 = no error; 1 = PLL Lock Loss occurred.
[31:5]	Reserved.

Front Panel LVDS I/O New Features

If the LVDS I/O new features are enabled (bit[8] = 1 of 0x811C), this register programs the functions of the front panel LVDS I/O 16-pin connector. It is possible to configure the LVDS I/O pins by group of four (4).
Options are:

1) 0000 = REGISTER, where the four LVDS I/O pins act as register (read/write according to the configured input/output option);

2) 0001 = TRIGGER, where each group of four LVDS I/O pins can be configured to receive an input trigger for each channel (DPP Firmware only), or to propagate out the trigger request;

3) 0010 = nBUSY/nVETO, where each group of four LVDS I/O pins can be configured as inputs (0 = nBusyIn, 1 = nVetoIn, 2 = nTrigger In, 3 = nRun In) or as outputs (0 = nBusy, 1 = nVeto, 2 = nTrigger Out, 3 = nRun);

4) 0011 = LEGACY, that is to say according to the old LVDS I/O confguration (i.e. ROC FPGA firmware revisions lower than 3.8), where the LVDS can be configured as 0 = nclear TTT, and 1 = 2 = 3 = reserved in case of input LVDS setting, while they can be configured as 0 = Busy, 1 = Data ready, 2 = Trigger, 3 = Run in case of output LVDS setting.
Please refer to the Front Panel LVDS I/Os section of the digitizer User Manual for detailed description.

NOTE: LVDS I/O new features are supported from ROC FPGA firmware revision 3.8 on.

NOTE: this register is supported by VME boards only.

Address	0x81A0
Mode	R/W
Attribute	C

Bit	Description
[3:0]	LVDS I/O pins[3:0] Configuration.
[7:4]	LVDS I/O pins[7:4] Configuration.
[11:8]	LVDS I/O pins[11:8] Configuration
[15:12]	LVDS I/O pins[15:12] Configuration.
[16]	This bits permits selecting whether the nTrigger signal, when configured as output (in nBusy/nVeto LVDS I/O mode), is a copy of the signal sent on the TRG-OUT connector or a copy of the acquisition common trigger. Options are: 0 = nTrigger output is a copy of TRG-OUT signal 1 = nTrigger output is a copy of the acquisition common trigger. **NOTE:** this bit is reserved for ROC FPGA firmware revisions lower than 4.9.
[31:17]	Reserved.

Buffer Occupancy Gain

If the Buffer Occupancy Mode is selected (bit[2:0] = 011 of 0x8144), The LEMO MON/Sigma output connector provides a voltage level whose amplitude increases in fixed steps exactly with the number of events in the event buffer. Each step of the output voltage level is 0.976 mV. A gain can be applied to the step by this register. Allowed values are in the range [0:A]. The default value, 0, means no gain applied while writing 0xn means that the fixed step is $0.976*2^n$ mV.

NOTE: this register is supported from ROC FPGA firmware revision 4.9 on.

NOTE: this register is supported only by VME boards.

Address	0x81B4
Mode	R/W
Attribute	C

Bit	Description
[31:4]	Reserved.
[0:3]	Buffer Occupancy Gain.

Readout Control

This register is mainly intended for VME boards, anyway some bits are applicable also for DT and NIM boards.

Address	0xEF00
Mode	R/W
Attribute	C

Bit	Description
[2:0]	VME Interrupt Level (VME boards only). Options are: 0 = VME interrupts are disabled; 1,..,7 = sets the VME interrupt level. **NOTE:** these bits are reserved in case of DT and NIM boards.
[3]	Optical Link Interrupt Enable. Options are: 0 = Optikal Link interrupts are disabled; 1 = Optical Link interrupts are enabled.
[4]	VME Bus Error / Event Aligned Readout Enable (VME boards only). Options are: 0 = VME Bus Error / Event Aligned Readout disabled (the module sends a DTACK signal until the CPU inquires the module); 1 = VME Bus Error / Event Aligned Readout enabled (the module is enabled either to generate a Bus Error to finish a block transfer or during the empty buffer readout in D32). **NOTE:** this bit is reserved (must be 1) in case of DT and NIM boards.
[5]	VME Align64 Mode (VME boards only). Options are: 0 = 64-bit aligned readout mode disabled; 1 = 64-bit aligned readout mode enabled. **NOTE:** this bit is reserved (must be 0) in case of DT and NIM boards.
[6]	VME Base Address Relocation (VME boards only). Options are: 0 = Address Relocation disabled (VME Base Address is set by the on-board rotary switches); 1 = Address Relocation enabled (VME Base Address is set by register 0xEF0C). **NOTE:** this bit is reserved (must be 0) in case of DT and NIM boards.
[7]	Interrupt Release mode (VME boards only). Options are: 0 = Release On Register Access (RORA): this is the default mode, where interrupts are removed by disabling them either by setting VME Interrupt Level to 0 (VME Interrupts) or by setting Optical Link Interrupt Enable to 0; 1 = Release On Acknowledge (ROAK). Interrupts are automatically disabled at the end of a VME interrupt acknowledge cycle (INTACK cycle). **NOTE:** ROAK mode is supported only for VME interrupts. ROAK mode is not supported on interrupts generated over Optical Link. **NOTE:** this bit is reserved (must be 0) in case of DT and NIM boards.
[8]	Extended Block Transfer Enable (VME boarsd only). Selects the memory interval allocated for block transfers. Options are: 0 = Extended Block Transfer Space is disabled, and the block transfer region is a 4kB in the 0x0000 - 0x0FFC interval; 1 = Extended Block Transfer Space is enabled, and the block transfer is a 16 MB in the 0x00000000 - 0xFFFFFFFC interval. **NOTE:** in Extended mode, the board VME Base Address is only set via the on- board [31:28] rotary switches or bits[31:28] of register 0xEF10. **NOTE:** this register is reserved in case of DT and NIM boards.
[31:9]	Reserved.

Readout Status

This register contains information related to the readout.

Address	0xEF04
Mode	R
Attribute	C

Bit	Description
[0]	Event Ready. Indicates if there are events stored ready for readout. Options are: 0 = no data ready; 1 = event ready.
[1]	Output Buffer Status. Indicates if the Output Buffer is in Full condition. Options are: 0 = the Output Buffer is not FULL; 1 = the Output Buffer is FULL.
[2]	Bus Error (VME boards) / Slave-Terminated (DT/NIM boards) Flag. Options are: 0 = no Bus Error occurred (VME boards) or no terminated transfer (DT/NIM boards); 1 = a Bus Error occurred (VME boards) or one transfer has been terminated by the digitizer in consequence of an unsupported register access or block transfer prematurely terminated in event aligned readout (DT/NIM). **NOTE:** this bit is reset after register readout at 0xEF04.
[31:3]	Reserved.

Board ID

The meaning of this register depends on which VME crate it is inserted in.
In case of VME64X crate versions, this register can be accessed in read mode only and it contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).
In case of other crate versions, this register can be accessed both in read and write mode, and it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the Board ID field of the Event header (see the User Manual for further details).

NOTE: this register is supported by VME boards only.

Address	0xEF08
Mode	R/W
Attribute	C

Bit	Description
[4:0]	GEO Address (VME boards only).
[31:5]	Reserved.

MCST Base Address and Control

This register configures the board for the VME Multicast Cycles.

NOTE: this register is supported by VME boards only.

Address	0xEF0C
Mode	R/W
Attribute	C

Bit	Description
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, that is the address used in MCST/CBLT operations.
[9:8]	Board Position in Daisy chain. Options are: 00 = board disabled; 01 = last board; 10 = first board; 11 = intermediate board.
[31:10]	Reserved.

Relocation Address

If address relocation is enabled through register 0xEF00 (bit[6] = 1), this register sets the VME Base Address of the module.

NOTE: this register is supported by VME boards only.

Address	0xEF10
Mode	R/W
Attribute	C

Bit	Description
[15:0]	These bits contain the A31...A16 bits of the address of the module. If bit[6] = 1 of 0xEF00, this they set the VME Base Address of the module.
[31:16]	Reserved.

Interrupt Status/ID

This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle.

NOTE: this register is supported by VME boards only.

Address	0xEF14
Mode	R/W
Attribute	C

Bit	Description
[31:0]	STATUS/ID (VME boards only).

Interrupt Event Number

This register sets the number of events that causes an interrupt request. If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of Events > INTERRUPT EVENT NUMBER.

Address	0xEF18
Mode	R/W
Attribute	C

Bit	Description
[9:0]	INTERRUPT EVENT NUMBER.
[31:10]	Reserved.

Max Number of Events per BLT

This register sets the maximum number of complete events which has to be transferred for each block transfer (via VME BLT/CBLT cycles, or block readout through USB or Optical Link).

Address	0xEF1C
Mode	R/W
Attribute	C

Bit	Description
[15:0]	MAX NUM EVENT PER BLT.
[31:16]	Reserved.

Scratch

This register can be used to write/read words for test purposes.

Address	0xEF20
Mode	R/W
Attribute	C

Bit	Description
[31:0]	SCRATCH.

Software Reset

All the digitizer registers can be set back to their default values on software reset command by writing any value at this register, or by system reset from backplane in case of VME boards.

Address	0xEF24
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location issues a software reset. All registers are set to their default values (actual settings are lost).

Software Clear

All the digitizer internal memories are cleared:

- automatically by the firmware at the start of each run;
- on software command by writing at this register;
- by hardware (VME boards only) through the LVDS interface properly configured.

A clear command doesn't change the registers actual value, except for resetting the following registers:

- Event Stored;
- Event Size;
- Channel / Group n Buffer Occupancy.

Address	0xEF28
Mode	W
Attribute	C

Bit	Description
[31:0]	Whatever value written at this location generates a software clear.

Configuration Reload

A write access of any value at this location causes a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Address	0xEF34
Mode	W
Attribute	C

Bit	Description
[31:0]	Write whatever value to perform a software reset, a reload of Configuration ROM parameters and a PLL reconfiguration.

Configuration ROM Checksum

Thi register contains information on 8-bit checksum of Configuration ROM space.

Address	0xF000
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum.
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 2

This register contains information on the third byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF004
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[23:16].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 1

This register contains information on the second byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF008
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[15:8].
[31:8]	Reserved.

Configuration ROM Checksum Length BYTE 0

This register contains information on the first byte of the 3-byte checksum length (i.e. the number of bytes in Configuration ROM to checksum).

Address	0xF00C
Mode	R
Attribute	C

Bit	Description
[7:0]	Checksum Length: bits[7:0].
[31:8]	Reserved.

Configuration ROM Constant BYTE 2

This register contains the third byte of the 3-byte constant.

Address	0xF010
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[23:16] = 0x83.
[31:8]	Reserved.

Configuration ROM Constant BYTE 1

This register contains the second byte of the 3-byte constant.

Address	0xF014
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[15:8] = 0x84.
[31:8]	Reserved.

Configuration ROM Constant BYTE 0

This register contains the first byte of the 3-byte constant.

Address	0xF018
Mode	R
Attribute	C

Bit	Description
[7:0]	Constant: bits[7:0] = 0x01.
[31:8]	Reserved.

Configuration ROM C Code

This register contains the ASCII C character code (identifies this as CR space).

Address	0xF01C
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'C' Character Code.
[31:8]	Reserved.

Configuration ROM R Code

This register contains the ASCII R character code (identifies this as CR space).

Address	0xF020
Mode	R
Attribute	C

Bit	Description
[7:0]	ASCII 'R' Character Code.
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 2

This register contains information on the third byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF024
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[23:16].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 1

This register contains information on the second byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF028
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[15:8].
[31:8]	Reserved.

Configuration ROM IEEE OUI BYTE 0

This register contains information on the first byte of the 3-byte IEEE Organizationally Unique Identifier (OUI).

Address	0xF02C
Mode	R
Attribute	C

Bit	Description
[7:0]	IEEE OUI: bits[7:0].
[31:8]	Reserved.

Configuration ROM Board Version

This register contains the board version information.

Address	0xF030
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Version Code. Options are: 0x50 = V1740/VX1740/DT5740/N6740; 0x51 = V1740B/VX1740B; 0x52 = V1740C/VX1740C/DT5740C/N6740C; 0x53 = V1740A/VX1740A; 0x54 = V1740D/VX1740D/DT5740D/N6740D.
[31:8]	Reserved.

Configuration ROM Board Form Factor

This register contains the information of the board form factor.

Address	0xF034
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Form Factor CAEN Code. Options are: 0x00 = VME64; 0x01 = VME64X; 0x02 = Desktop; 0x03 = NIM.
[31:8]	Reserved.

Configuration ROM Board ID BYTE 1

This register contains the MSB of the 2-byte board identifier.

Address	0xF038
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board ID BYTE 0

This register contains the LSB information of the 2-byte board identifier.

Address	0xF03C
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Number ID: bits[7:0].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 3

This register contains information on the fourth byte of the 4-byte hardware revision.

Address	0xF040
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[31:24].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 2

This register contains information on the third byte of the 4-byte hardware revision.

Address	0xF044
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[23:16].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 1

This register contains information on the second byte of the 4-byte hardware revision.

Address	0xF048
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[15:8].
[31:8]	Reserved.

Configuration ROM PCB Revision BYTE 0

This register contains information on the first byte of the 4-byte hardware revision.

Address	0xF04C
Mode	R
Attribute	C

Bit	Description
[7:0]	PCB Revision: bits[7:0].
[31:8]	Reserved.

Configuration ROM FLASH Type

This register contains information on which FLASH type (storing the FPGA firmware) is present on- board.

Address	0xF050
Mode	R
Attribute	C

Bit	Description
[7:0]	FLASH Type. Options are: 0x00 = 8 Mb FLASH; 0x01 = 32 Mb FLASH.
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 1

This register contains information on the MSB of the board serial number.

Address	0xF080
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[15:8].
[31:8]	Reserved.

Configuration ROM Board Serial Number BYTE 0

This register contains information on the LSB of the board serial number.

Address	0xF084
Mode	R
Attribute	C

Bit	Description
[7:0]	Board Serial Number: bits[7:0].
[31:8]	Reserved.

Configuration ROM VCXO Type

This register contains information on which type of VCXO is present on-board.

Address	0xF088
Mode	R
Attribute	C

Bit	Description
[31:0]	VCXO Type Code. Options for VME Digitizers are: 0 = AD9510 with 1 GHz; 1 = AD9510 with 500 MHz (not programmable); 2 = AD9510 with 500 MHz (programmable). Options for Desktop/NIM Digitizers are: 0 = Reserved.

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