CAEN Nuclear Physics

WP2081 Digital Pulse Processing in Nuclear Physics

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Index

List of Figures

List of Tables

Glossary and Acronyms

CFD: Constant Fraction Discriminator

PSA: Pulse Shape Analysis

DPP: Digital Pulse Processing

WD: Waveform Digitizer

MCA: Multi Channel Analyzer

TDC: Time to Digital Converter

QDC: Charge to Digital Converter

ADC: Analog to Digital Converter

PMT: PhotoMultiplier Tube

SiPM: Silicon PhotoMultiplier

1 Measurements in Nuclear Physics

1.1 Introduction

The function of the Front End electronics for nuclear physics applications is to acquire the electrical charge pulses generated by a radiation detector, to extract the quantities of interest and to convert them into a digital format that are then acquired, saved and analyzed by a computer. In most applications, the quantities of interest are the particle energy (proportional to the charge released by the particle in the detector) and the time of arrival; in some cases the acquisition is restricted to the simple pulse counting, actually a "selective" counting, meaning that one or more energy intervals or other criteria are used to select which particles must be counted. In some other cases, it is necessary to discriminate the type of the particle by means of the pulse shape; for example, the **γ-n** discrimination is based on the time variation of the detector response when stimulated by a gamma or a neutron; this variation leads to a different rise and/or decay time of the pulse.

The acquisition system is usually completed by digital logic units whose purpose is to make coincidences, generate triggers, vetoes and other signals that take into account the correlation between different channels and may give further information such as the particle position or trajectory.

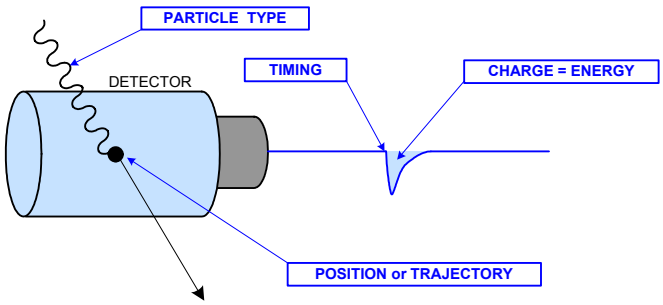


Fig. 1.1:Electrical charge pulse generated by a detector

1.2 Traditional Analog Chains

Traditionally, the electronic readout systems for the particle detectors have been made of almost all-analog chains, like the one represented in Fig. 1.2 and Fig. 1.4. Each block of the chain has a specific function, so that you need to interconnect several blocks in order to make a system able to extract all the quantities of interest. With this approach, the A to D conversion is performed at the end of the acquisition chain, just before the readout interface connected to the computer.

In most cases, the first stage of the chain is the **preamplifier** that is usually located close to the detector. The preamplifier is a very low noise analog circuit that receives the weak signal generated by the detector and produces an output signal with an S/N ratio suitable for the transmission through a cable up to the readout electronics. The latter is normally housed in a crate or a rack and can be as far as ten or hundred meters from the detector. There are many types of preamplifier, but for the purpose of this document we can consider them divided into two families: **charge sensitive preamplifier** and **current sensitive preamplifier** (or **fast amplifier** or **wideband amplifier**).

The charge sensitive preamplifier integrates the signal coming from the detector, thus it converts the charge into a voltage amplitude. Ideally, it is just made of a simple capacitor; however, in order to avoid saturation, the integrating capacitor is put in parallel with a discharging resistor, so that the preamplifier output will have pulses with a fast rise time and an exponential decay (see Fig. 1.3). The charge information (energy) is here represented by the pulse height.

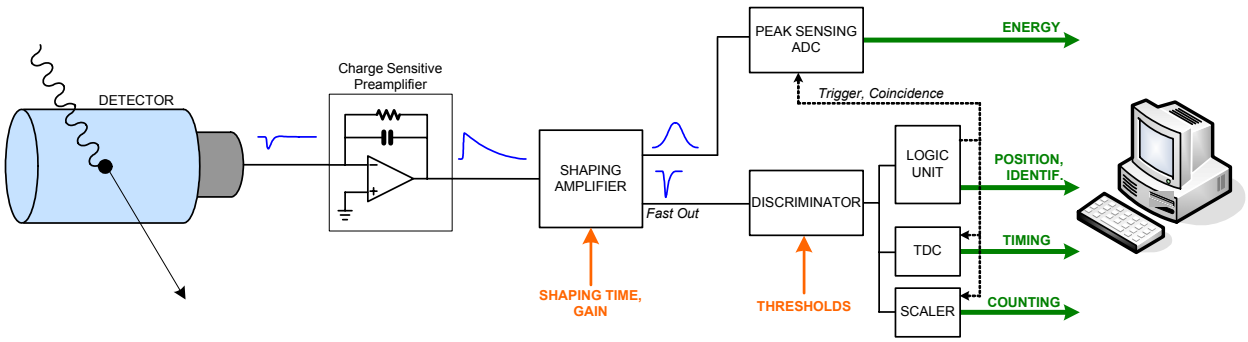


Fig. 1.2: Block diagram of a traditional acquisition system for spectroscopy

In order to preserve the timing information, the fast component of the signal (rising edge) is usually treated by a **fast amplifier** (or **timing amplifier**) that derivates the signal; the output of the timing amplifier usually feeds a chain made out of a discriminator, a TDC and/or a scaler for the timing/counting acquisition. Further modules can be present in order to implement logic units, make coincidences (giving the position and the trajectory of the particles), generate triggers or give information about the pulse shape (time over threshold, zero crossing, etc) for the particle identification. Usually the fast amplifier is included in the shaping amplifier module and the relevant signal is provided as a separate fast output (or timing output).

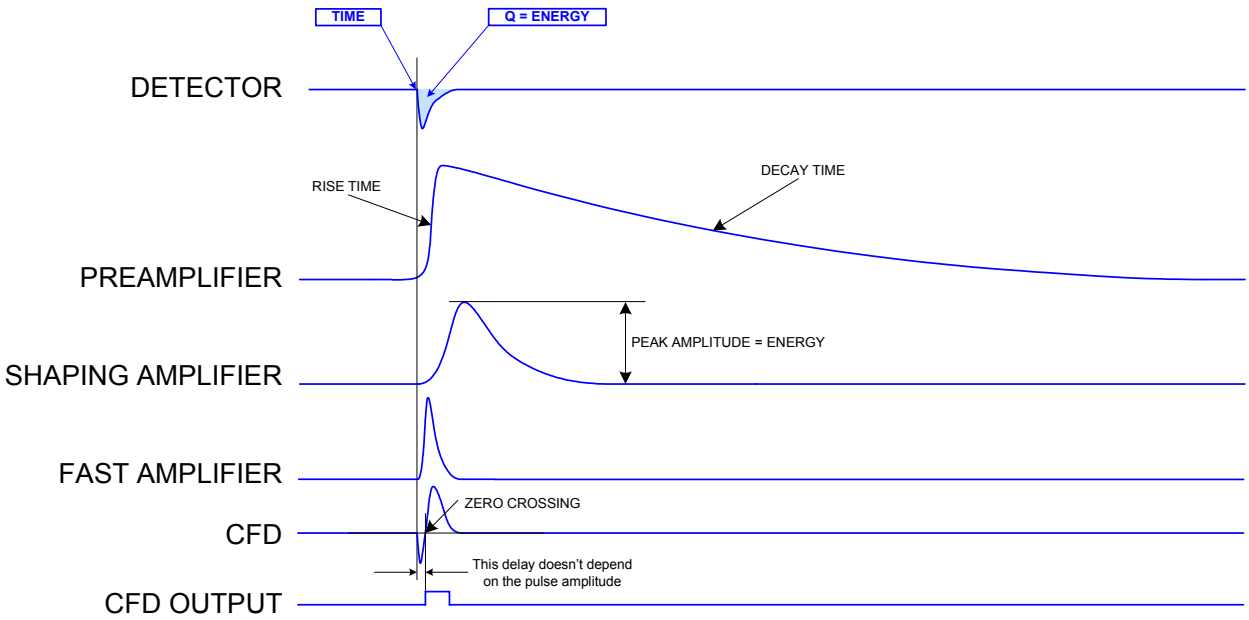


Fig. 1.3: Signals in the traditional analog chain

Unlike the charge sensitive preamplifier, the current sensitive preamplifier is a linear fast amplifier that doesn't change the shape of the signal. Its output is normally a very short pulse (some tens of ns or even less) and is particularly used where the high precision timing information is an issue. Another advantage of this type of preamplifier is that, it minimizes the effect of the pile-up. Sometimes the preamplifier is even unnecessary, like in the case of some PMTs that give a signal sufficiently strong to be fed directly into the readout electronics. In any case, when the shape of the detector signal is unchanged, the energy information is represented by the area below the pulse and this is normally measured by a Charge ADC (QDC), as shown in Fig. 1.4. The QDC is a pure integrator that requires a gate signal to define the integrating window. In some applications (most likely in beam experiments) the gate is provided by the system that knows in advance when the signals have to be integrated. Unfortunately, when this is not the case, it is necessary to generate the gate from the detector signals; to do that, you need to split the signals, send one branch to the discriminators and use a coincidence logic. It is also necessary to add a

delay line (typically a long cable) on the signal path to the QDC input in order to match the pulses with the gate (which arrives with some latency respect to the analog pulses that produced it).

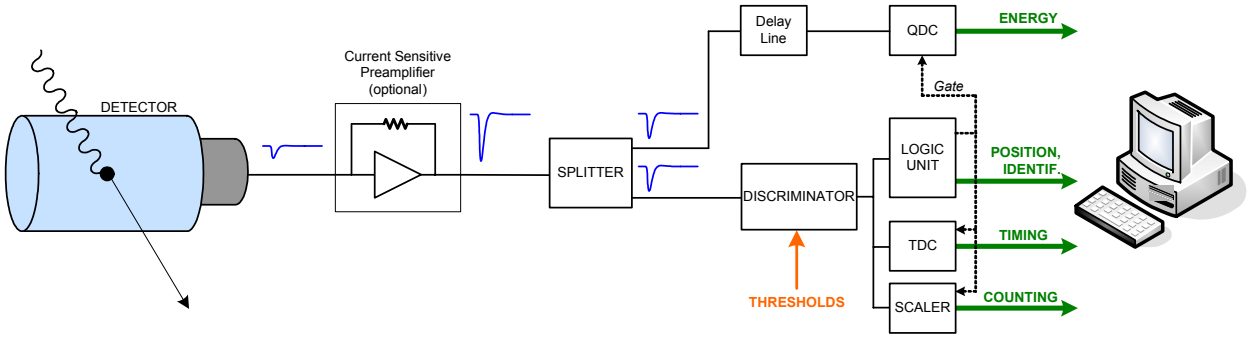


Fig. 1.4: Block diagram of another acquisition system based on the QDC

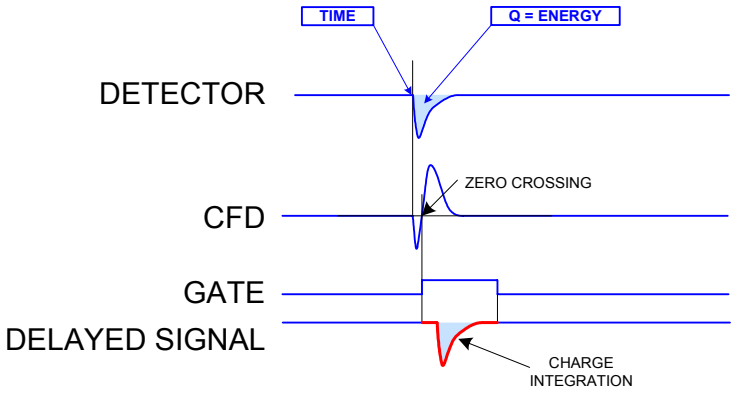


Fig. 1.5: Signals in the QDC based chain

The table below reports some products available in the CAEN catalog for the traditional acquisition systems.

Model	***Function***	***Format***	***Comments***
A422	PREAMPLIFER	BOX	
N968	SHAPING AMPLIFIER	NIM	1 channel
N568	SHAPING AMPLIFIER	NIM	16 channels
N842 N843	CFD	NIM	8/16 channels
N1145	SCALER	NIM	Quad Scaler
N957	PEAK SENSING ADC	NIM	1 channel, 13 bit (8K) MCA
V812	CFD	VME	16 channels
V1190	TDC	VME	128 channels, 100 ps LSB
V1290	TDC	VME	32 channels, 25 ps LSB
V775	TDC	VME	32 channels, 35 ps LSB
V830	SCALER	VME	32 channels, up to 200MHz
V785	PEAK SENSING ADC	VME	32 channels, 12 bit. Peak stretcher + ADC
V1785	PEAK SENSING ADC	VME	8 channels, 12/15 bit. Dual Range Peak stretcher + ADC
V792	QDC	VME	32 channels, 12 bit
V965	QDC	VME	16 channels, 12/15 bit Dual Range

Tab. 1.1: Some CAEN catalog products for the traditional acquisition chain

1.3 Digital Pulse Processing: a new approach

Nowadays, the availability of very fast and high precision flash ADCs permits to design acquisition systems in which the A to D conversion occurs as close as possible to the detector. In theory, this acquisition system is information lossless, provided that the Nyquist criteria is respected. Actually, the acquisition will be affected by errors due to the quantization noise and to other sources of electronic noise. In general, the applications that require precise timing measurements are more oriented to the use of high sample frequency digitizers (500 MS/s or more), while the 12-14 bit digitizers are well suited for acquisitions where high energy resolution is a pre-requisite.

The principle of operation of a *Waveform Digitizer* (also known as *Transient Recorder* or *Flash ADC*) is the same as the digital oscilloscope: when the trigger occurs, a certain number of samples (acquisition window) is saved into one memory buffer.

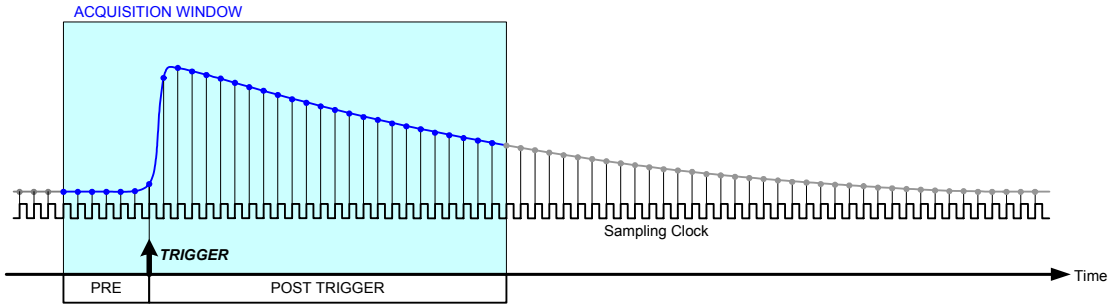


Fig. 1.6: Signal digitization and acquisition window defined by the trigger

However, the digitizers present some important differences:

- Thanks to the Multi Event Memory, there is no dead-time between the triggers[1], at least until the readout rate allows the memory buffers to be read and freed on average faster than they are written, thus avoiding the memory to go full;
- They allow for multi-board synchronization and system scalability. Growing up from one or few channels to thousands is possible by means of the clock, trigger and sync distribution features;
- Normally, they have high bandwidth data readout links (VME, optical links, etc…);
- They have FPGAs or DSPs that permits to do on-line data processing and data reduction.

CAEN has developed a complete family of waveform digitizers best suited for physics, medical, homeland security and industrial applications. They are available in different form factors (VME, Desktop, NIM and PCI Express) as showed in the table below.

[1] With the exception of the digitizers that are based on the switching capacitor arrays, like the V1742 or the V1729. These boards have a fixed dead-time between the triggers.

Waveform Digitizers Selection Table

								Form factor / Interfaces / Channels			
								VME	NIM	Desktop	PCI Express
Series	Full scale Range (V)	AMC FPGA(1)	Input Type	Max. Sampling Rate	Bandwidth (MHz)	Resolution (bits)	Memory (MS/ch)	VME64 Opt. link	USB2.0 Opt. link	USB2.0 Opt. link	PCI Express
724	± 1.125 /± 5	EP1C4/ EP1C20	Single Ended Differential	100 MS/s	40	14	0.5/4	8 ch	4 ch	4/2 ch	2 ch
720	± 1	EP1C4	Single Ended Differential	250 MS/s	125	12	1.25/10	8 ch	4 ch	4/2 ch	2 ch
721	± 0.5	EP1C4	Single Ended Differential	500 MS/s	250	8	2	8 ch	-	-	-
731	± 0.5	EP1C4	Single Ended Differential	0.5-1 GS/s	250/500	8	2-4	8-4 ch	-	-	2-1 ch
740	± 1/± 5	EP3C16	Single Ended	65 MS/s	30	12	0.19/1.5	64 ch	32 ch	32 ch	-
751	± 0.5	EP3C16	Single Ended Differential	1-2 GS/s	500	10	1.8-3.6/ 14.4-28.8	8-4 ch	4-2 ch	4-2 ch	-
761	± 0.5	EP3C16	Single Ended Differential	4 GS/s	Tdb	10	7.2/57.6	2 ch	1 ch	1 ch	-
742(2)	± 0.5	EP3C16	Single Ended	5 GS/s	Tbd	12	0.128	32+2 ch	16+1 ch	16+1 ch	-

(1) AMC: ADC & Memory controller FPGA. ALTERA models available: EP1C4: Cyclone (4.000 LEs), EP1C20: Cyclone (20.000 LEs), EP3C16: Cyclone III (16.000 LEs).
(2) Switched capacitor.

Tab. 1.2: CAEN Waveform Digitizers

The major problem of the fully digital approach is that the amount of data to readout is extremely high. It is no possible to sustain a continuous acquisition, transfer row data to the computers and make the analysis off-line. Therefore, it is necessary to implement on-line digital data processing (Zero Suppression and/or Digital Pulse Processing) able to transform the row sequence of samples into a compressed data packet that preserves the information required by the physics, minimizing the event data size.

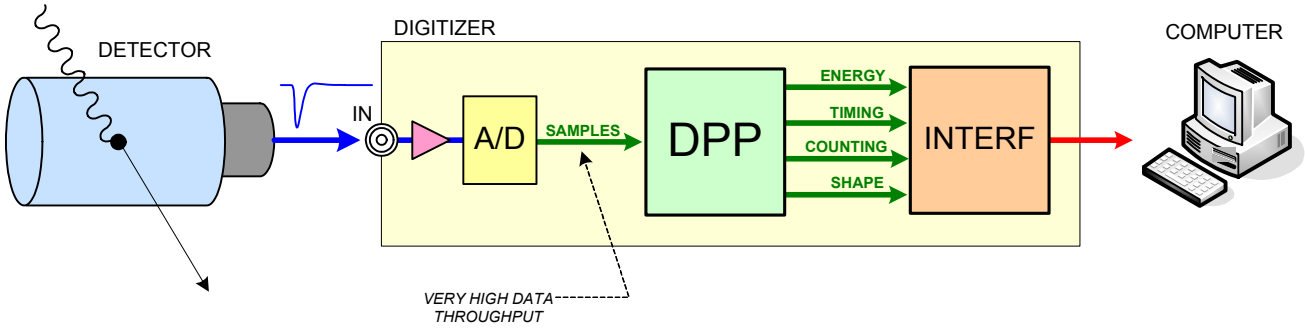


Fig. 1.7: Block diagram of the digital solution

Just to make an example with a digitizer of the family, the following table (Tab. 1.3) shows the readout bandwidth required for the series 720 (12 bit @ 250 MS/s) in a hypothetical continuous mode and in a realistic triggered acquisition (~2μs acquisition windows at 10 KHz).

	1 channel	***4 channel (1 NIM / Desktop board)***	***8 channel (1 VME board)***
Continuous acquisition	375 MB/s	1.5 GB/s	3 GB/s
Triggered acquisition Record length: 512 samples Trigger rate: 10 KHz<	7.68 MB/s	30.5 MB/s	61 MB/s

Tab. 1.3: examples of readout rates for Waveform digitizer series 720 (12 bit @ 250 MS/s)

interface	*bandwidth*	*VME Board*	*NIM / Desktop Board*
VME with MBLT	60 MB/s	✓	
VME with 2eSST	150 MB/s	✓	
Optical Link:	70 MB/s	✓	✓
USB 2.0	30 MB/s		✓

Tab. 1.4: Readout bandwidth of CAEN digitizer

1.4 Acquisition modes with the Waveform Digitizer

In a digitizer with DPP capabilities, there are different acquisition modes. Let's suppose, for the sake of simplicity, that we want to use the DPP only to measure the energy of the pulses (but it would be the same for the timing or other quantities).

1. **Oscilloscope Mode:** this is the "standard" acquisition mode (the only possible when the digitizer doesn't feature any DPP): for each trigger (either external or internal), the digitizer saves the sequence of samples (waveform) that belong to the acquisition window into one local memory buffer. This mode is normally used to monitor the signals (including the internal signals at the output of the digital filter stages), set the parameters and see their effect on the filters output and, in general, tune and debug the acquisition system. Moreover, the user can readout the raw data from the digitizer and apply the digital algorithms off-line in the software (for example using C programs or Mathlab), comparing the results to those obtained with the processing on-line. This is particularly useful when the algorithms have to be developed and tested.
2. **List Mode**: In this case, the DPP algorithms are applied runtime by the FPGA that operates on a continuous data stream; whenever a pulse is found, the relevant energy (or other quantities) is calculated and written in the memory buffers, thus making a list of energies. As soon as the list reaches a certain size, the data buffer is made available for the readout while the acquisition continues in another buffer without any dead-time. Thanks to the extremely reduced number of data to save and transfer, this mode is normally able to sustain a continuous acquisition, even in the case where the pulse rate is very high.
3. **Mixed Mode**; both the waveforms (samples) and the energy values (result of the DPP algorithms) are saved into the memory buffers. Like in mode 1, only the part of the signal that belongs to the acquisition window (defined by the trigger) is saved. Therefore, only the energy of the peaks that fall within that window will be saved among the waveform samples. The user should run in this mode whenever it is necessary to see how the DPP algorithm works on a specific waveform and it is important to have both the energies and the samples at the same time. It is care of the software readout program to separate the energy values form the samples (there is a tag for this purpose) and fill the missing points of the waveform with an estimated value.
4. **Histogram mode (NOT IMPLEMENTED)**: the acquisition is the same as the list mode, with the difference that the memory buffer is used to accumulate the energy values in a histogram that grows continuously until the user decide to stop it or the maximum counting range is reached (2^{32}). The histogram can be readout at any time without stopping the acquisition. For the moment, the DPP firmware versions developed by CAEN don't provide this option.

The Fig. 1.8 shows the difference in the buffer occupancy when running in oscilloscope mode (all the samples are saved), in energy list mode (saving only the energy value in the memory buffer) or in mixed mode.

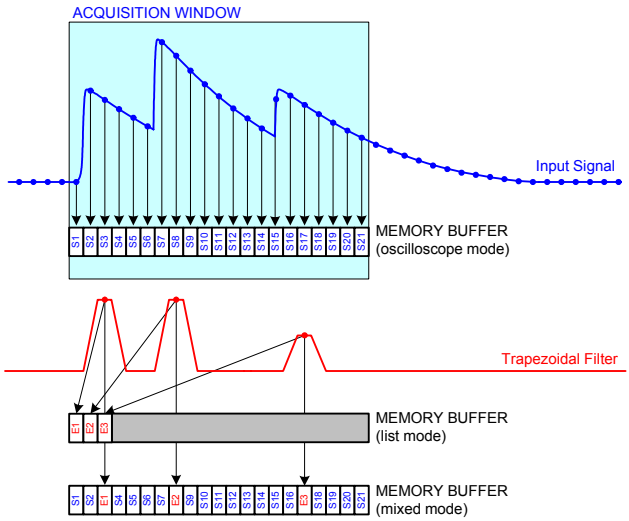


Fig. 1.8: Buffer occupancy in oscilloscope, mixed and list modes

1.5 Comparison between analog and digital signal treatment

ADVANTAGES:

- One single board can do energy, timing and pulse shape analysis => low cost and reliability
- All in digital => good linearity and stability => reproducibility
- Wider dynamic range and uniformity of the performances over the range
- Digital techniques allow better correction of pile-up, ballistic deficit and baseline fluctuation effects
- Preserve pulse information
- You can easily keep synchronized and correlated several channels and make coincidence/anticoincidence after the acquisition (off-line)
- Low dead-time in the acquisition => high counting rate
- Flexibility (all in FPGAs) => you change and adapt the algorithms => easy tailoring to the application
- Tuning and calibration: register programming instead of manual regulations => faster and automatic

DISADVANTAGES:

- Setting up the system requires a deep knowledge of the digital algorithms and the relevant parameters. It takes more time for the beginners.
- Customization requires VHDL knowledge and/or CAEN support

2 Digital Pulse Processing algorithms

2.1 Pulse Triggering and Timing Filters

Usually, the digitizers and the oscilloscopes feature a self-trigger based on a programmable voltage threshold; the trigger is generated as soon as the input signal crosses that threshold. Unfortunately, this technique is not suitable for most physics application because of the baseline fluctuation, pulse pile-up, noise, etc... However, the ability in finding all the good pulses and discriminating them from the noise is very important. In fact, missing pulses or false triggers can cause loss of important events, bad pile-up rejection, errors in the statistics and other unwanted effects. The digital filters are able to reject the noise, cancel the baseline and to do shape and timing analysis for this purpose.

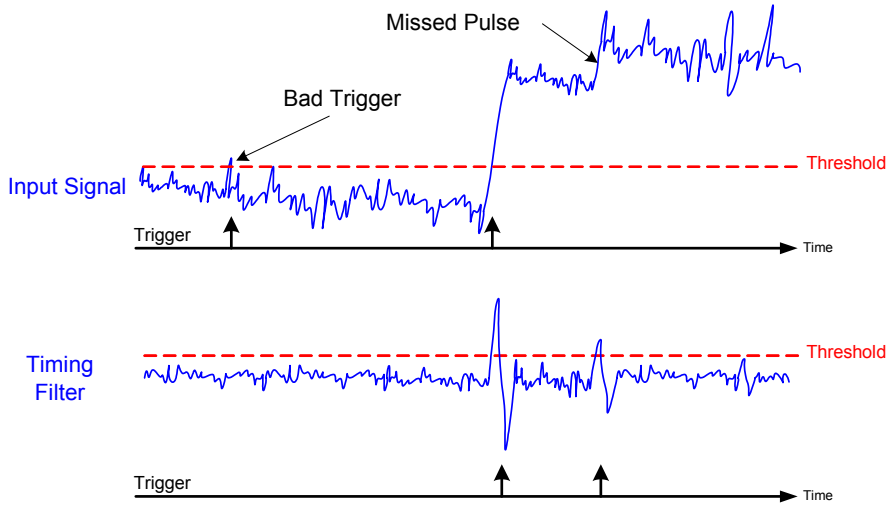


Fig. 2.1: Triggering before and after the timing filter

There are many types of timing and triggering filters. CAEN has developed RC-$(CR)^N$ filters able to reject the high frequency noise (*RC filter = mean filter*), restore the baseline and cancel the low frequency fluctuations (CR^N *filter = derivative*) and transform the pulses into bipolar signals whose zero crossing (pulse amplitude independent) can be used for the determination of the Time Stamp. For this purpose, it is also possible to implement a digital Constant Fraction Discriminator based on the same concept of the analog CFD (delay – attenuation - subtraction).

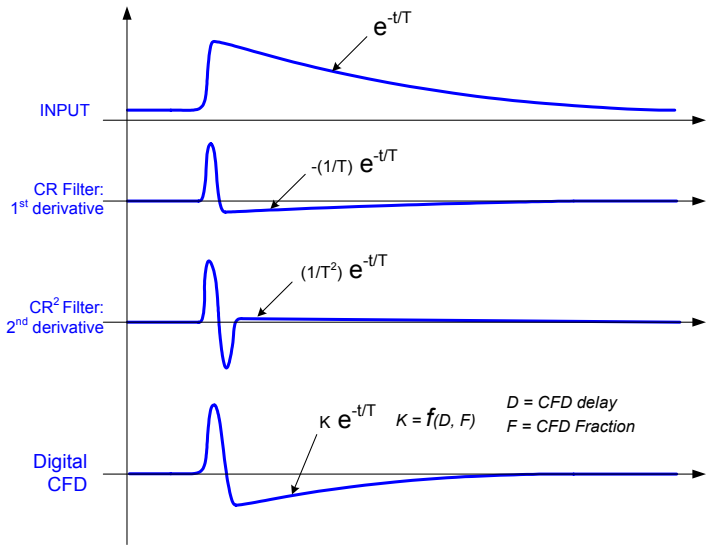


Fig. 2.2: Timing filters

2.2 Pulse Height Analysis (DPP-TF): Digital MCA

The aim of this DPP is to implement a digital version of the analog chain made of Shaping Amplifier + Peak Sensing ADC (Multi Channel Analyzer). The DPP-TF is implemented in the Mod. 724 (14 bit, 100MS/s). It is mainly used for high resolution spectroscopy (Germanium and Silicon detectors); the output of he charge sensitive preamplifier is directly connected to the input of the digitizer.

The energy calculation (pulse height) is done by means of the **Trapezoidal Filter**; there are many articles that describe the principle of operation as well as the relevant equations and implementation techniques of this filter (for example *NIM A 345 (1994) 337: "Digital Synthesis of pulse shapes in real time for high resolution radiation spectroscopy" by V.T. Jordanov and G.F. Knoll*). For the purpose of this document, the trapezoidal filter can be shortly described as a filter able to transform the typical exponential decay signal generated by a charge sensitive preamplifier into a trapezoid that presents a flat top whose height is proportional to the amplitude of the input pulse (that is to the energy released by the particle in the detector). This trapezoid plays more or less the same role of the shaping amplifier in a traditional analog acquisition system. We want to highlight the analogy between the two systems: both have a "shaping time" constant and must be calibrated for the pole-zero cancellation. For both, a long shaping time gives a better resolution but has higher probability of pile-up. Both are AC coupled with respect to the output of the preamplifier whose baseline is hence removed, but both have their own output DC offset and this constitutes another baseline for the peak detection.

Setting the parameters of the trapezoidal filter is like operating on the potentiometer of the shaping amplifier. This analogy makes the understanding of the DPP parameters easier for the physicist used to the tradition spectroscopy chain.

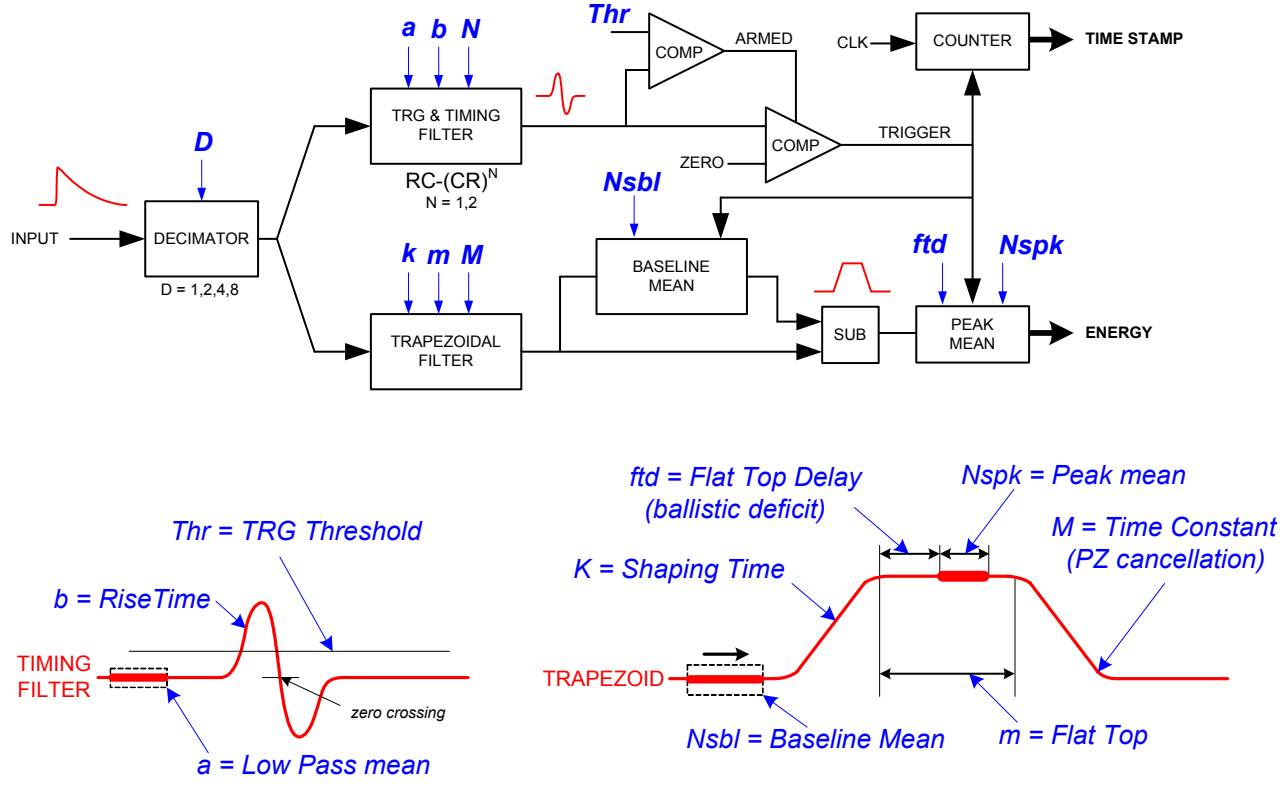


Fig. 2.3: Block Diagram and parameters of the DPP-TF

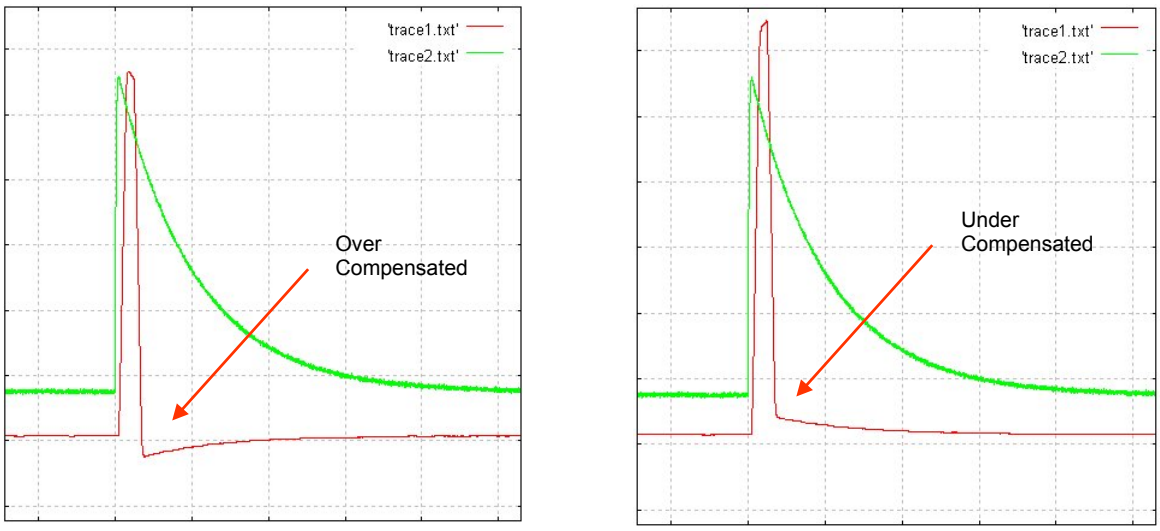


Fig. 2.4: Examples of incorrect pole-zero cancellation in the trapezoidal filter

2.3 Charge Integration (DPP-CI): Digital QDC

It is the digital version of the analog chain made of Charge Integrating ADC (QDC), Discriminator and Gate generator. The DPP-CI is implemented in the Mod. 720 (12 bit, 250MS/s) and will be implemented in the Mod. 751 (10 bit, 1GS/s or 2GS/s).

The main advantage of the digital approach is that it is very easy to implement delay lines (it is sufficient to move back the pointer in the memory buffer that contains the samples). Thus, making the integrating gate and move it back and forth to match the position of the pulse is as simple as to change a number. Moreover, the digital processing can calculate the baseline of the signal and subtract it (pedestal cancellation). The extremely high dynamic range is another advantage of the digital approach; in fact, unlike the analog ADC in which the integrating capacitor can saturate, here the charge is represented by the sum of a set of samples (accumulator) and it can be as large as you like just changing the number of bit of the accumulator.

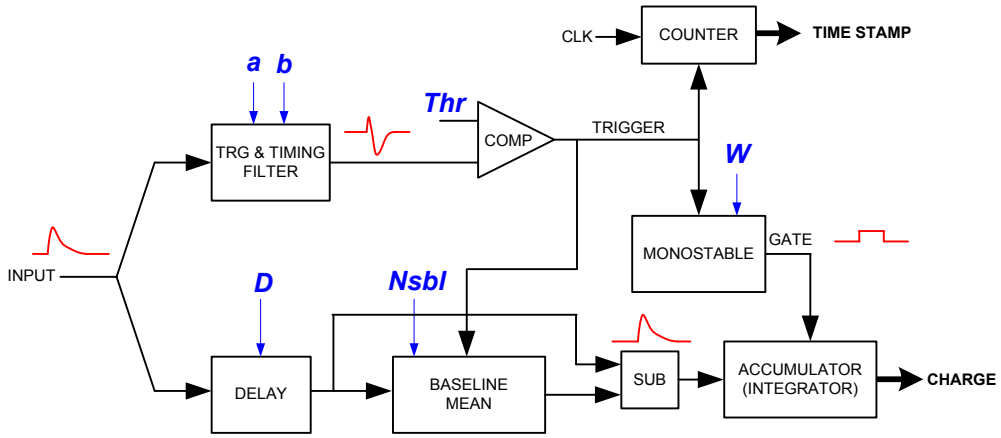


Fig. 2.5: Block Diagram of the DPP-CI

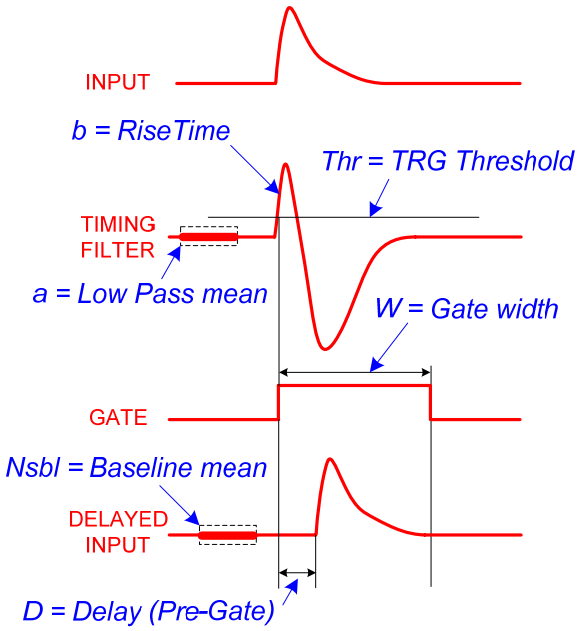


Fig. 2.6: Signals and parameters of the DPP-CI

2.4 Time measurement

Traditionally, the time measurements in physics (typically the arrival time of the pulses respect to a common time reference) is done using a discriminator that receives the analog pulses and generates a digital signal followed by a TDC (Time to Digital Converter). Conventional TDCs have high resolution (up to 25 ps), high channel density (up to 128), multi-hit capabilities and other powerful features. However, there are applications for which the conventional TDCs might be unsatisfactory. For example, in certain beam experiments it is necessary to acquire the arrival times of many pulses in a burst; in the multi-hit TDCs, the maximum number of hits that can be recorded before reading them out is normally rather low. The traditional chain for the time measurement can also suffer from the jitter and walk introduced by the discriminator. Finally, there are applications where the time information must be correlated to other quantities like the charge, the pulse height or shape, etc. In all these cases, the use of a digitizer for the time measurement can be a suitable solution. It is also noteworthy to say that the recent development of ultra fast A/D converter allows the timing resolution of the digitizers to exceed that one of the conventional TDCs. Most applications that require 10ps resolution (or even better) are based on digitizers.

Like in the other DPP algorithms, there is an analogy between traditional analog chain and digital filters: the input pulse (usually unipolar) is transformed into a bipolar signal whose zero crossing determines the arrival time. This makes the timing information independent by the pulse amplitude. This is the purpose of the timing filters (see 2.1).

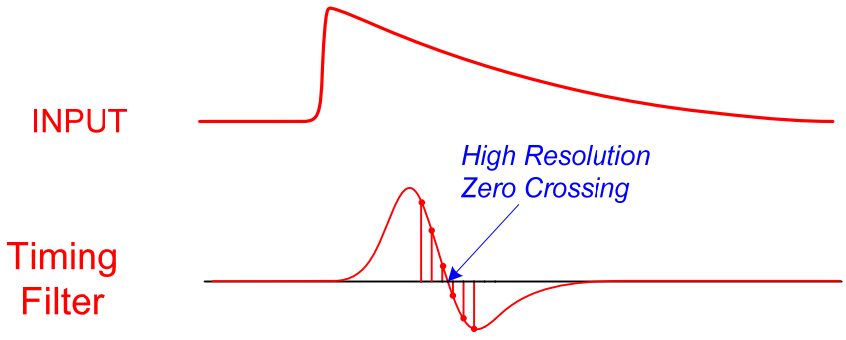


Fig. 2.7: Timing filter and zero crossing

In order to increase the timing resolution beyond the granularity given by the sampling period of the ADC, it is necessary to use two or more samples around the zero crossing and make some kind of interpolation. Right now CAEN is studying different interpolation techniques applied to the digitizers of the family. We are presenting here the results of the linear interpolation (segment between two points).

The timing resolution is affected by the sampling rate of the ADC, by the number of bits and by the shape of the signal (especially the slope in the zero crossing) in a way that is not intuitive at the first glance. Both experimental tests and simulation show that, depending on the rise time of the signal, there are two different regions: when the rise time is greater than 5*Ts (Ts = sampling period), the error in the calculation of the zero crossing is mainly due to the A/D quantization error, thus the number of bits of the digitizer has a dominant effect in the timing resolution (we don't take into account the noise in the analog signal that is supposed ideal). When the rise time is smaller that 5*Ts, the approximation of the curve to a linear segment is too rough and the most important contribution to the timing error is due to the inaccuracy of the zero crossing determination. Furthermore, the position of the zero crossing calculated with a linear interpolation respect to the actual one varies with the sampling clock phase. Therefore, if we consider the typical case in which the time distance between two signals A and B has to be measured, the resolution is strongly dependent on the delay between A and B ($DELAY_{AB}$ later on). In fact, the resolution is significantly better when $DELAY_{AB}$ is a multiple of Ts since the two signals A and B cross the zero in the same position respect to the sampling clock, hence they have almost the same error in the determination of the zero crossing. Conversely, the worst case is when the A to B delay is a multiple of Ts plus ½ Ts.

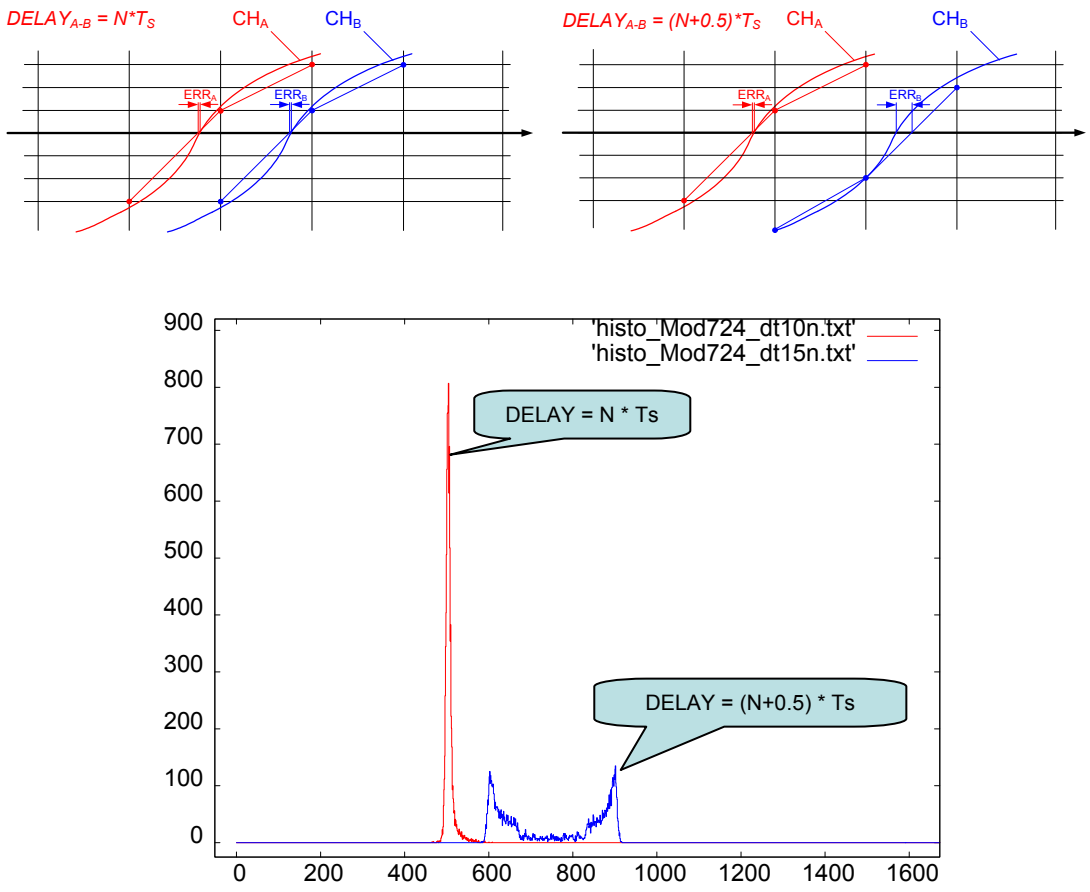


Fig. 2.8: Effect of the clock phase in the calculation of the delay between two signals A and B

The next figure shows the timing resolution that can be obtained using three different digitizers with an input pulse of 100mV having a rise time equal to the sampling period. It is evident the effect due to the variation of the delay between A and B.

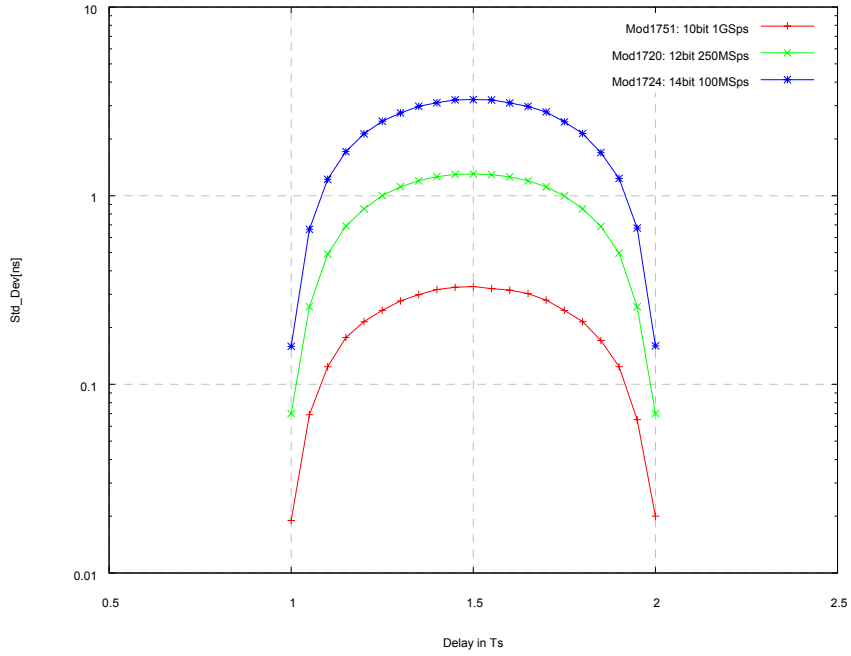


Fig. 2.9: Resolution as a function of $DELAY_{AB}$ (Mod. 724, 720, 751)

When the rise time increases, the effect due to the clock phase gets less evident, as shown in the next figure which is referred to the Mod. 720 only:

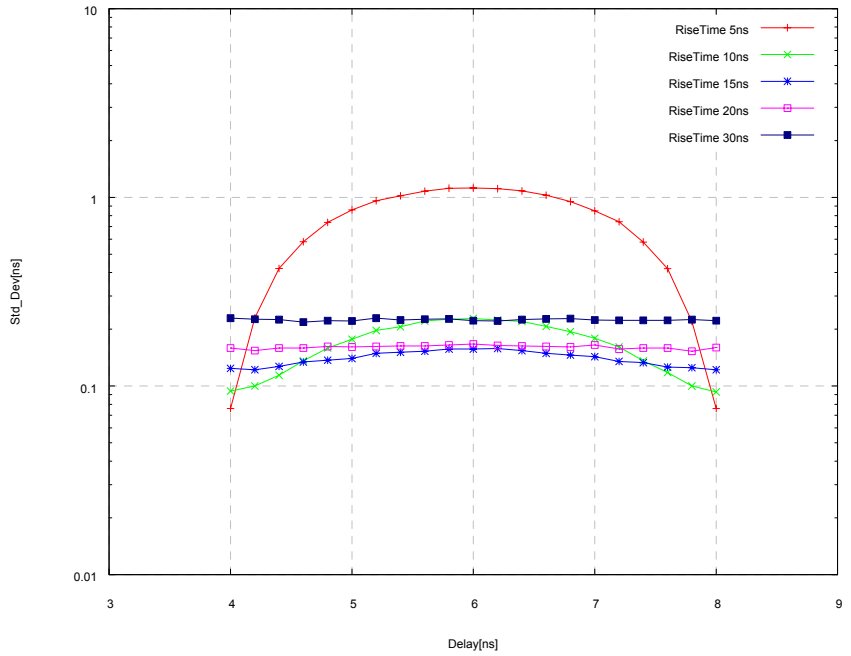


Fig. 2.10: Resolution as a function of $DELAY_{AB}$ for different signal amplitude (Mod. 720)

Obviously, both the A/D quantization error and the effect of the clock phase are influenced by the pulse amplitude, that is by the slope of the timing filter output signal in the zero crossing. In general, the higher the pulse amplitude, the better the resolution.

The next plots show the results obtained with three different types of digitizer; we used a pulse generator with programmable rise time and amplitude; the delay between A and B has been done with cables.

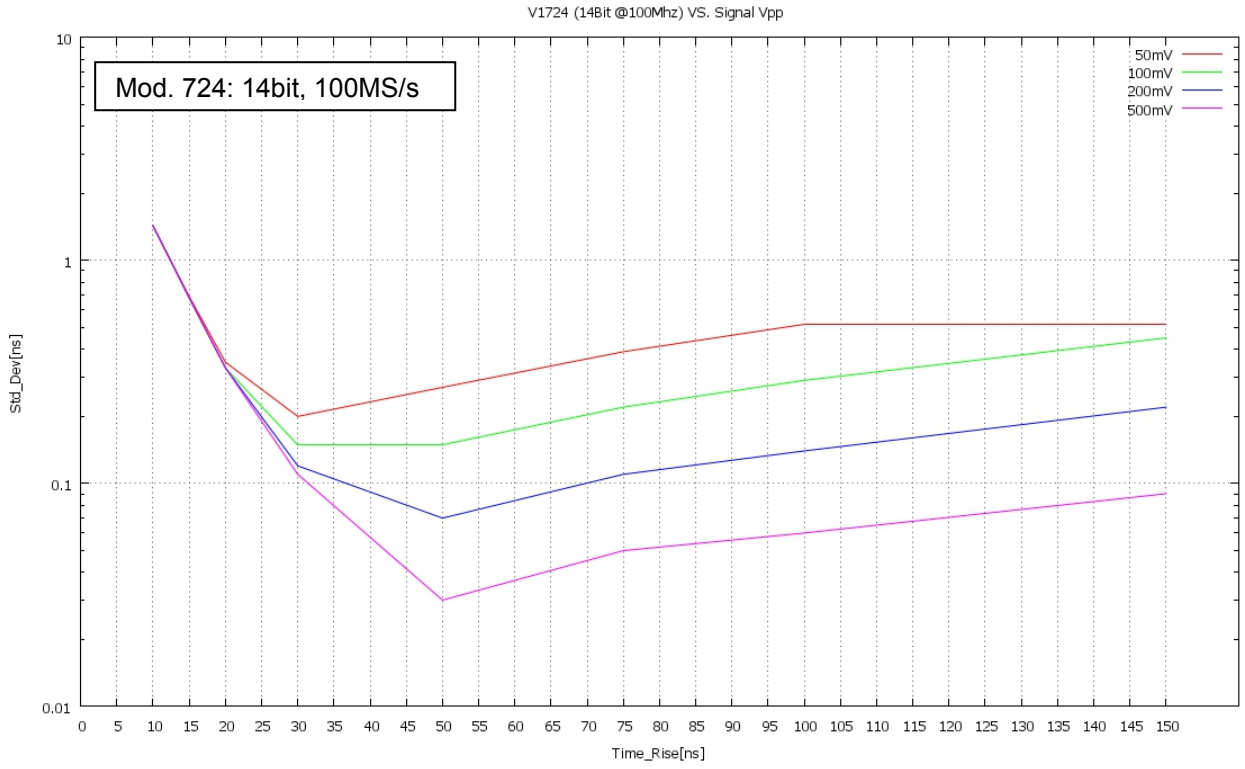


Fig. 2.11: Resolution as a function of the rise time for different signal amplitude (Mod. 724)

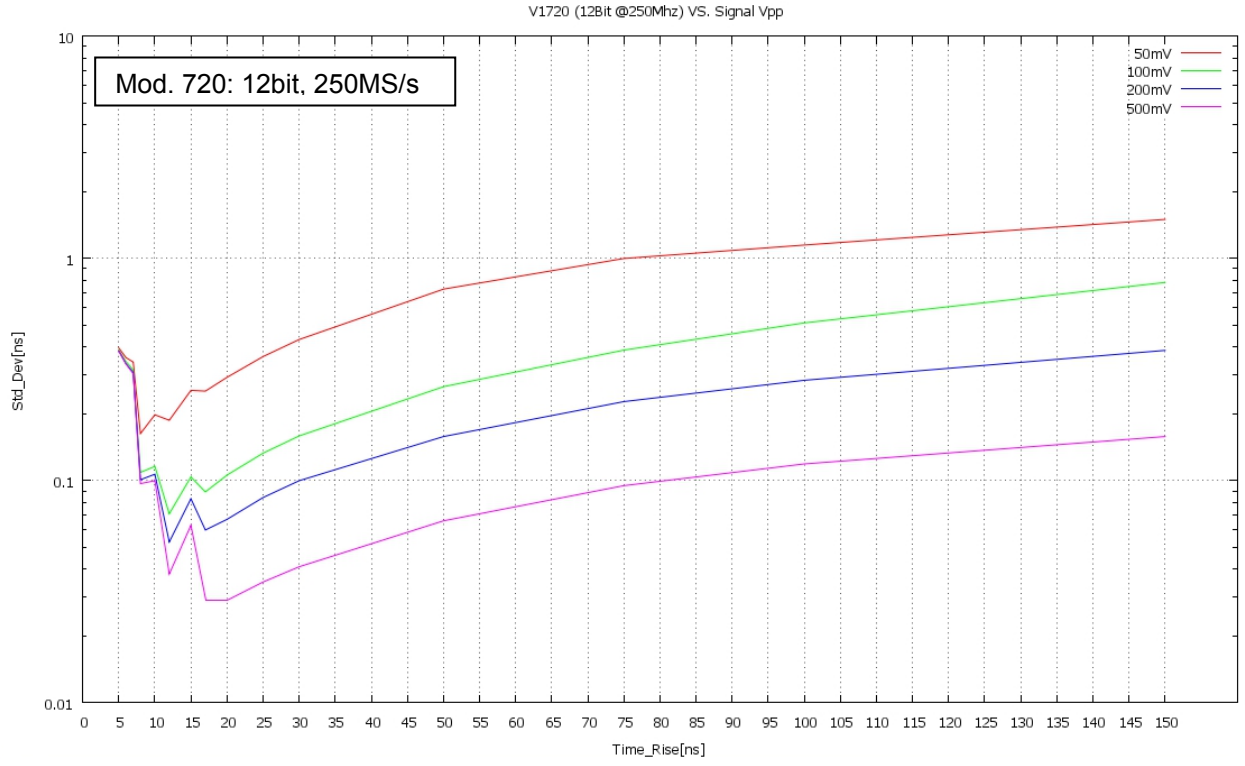


Fig. 2.12: Resolution as a function of the rise time for different signal amplitude (Mod. 720)

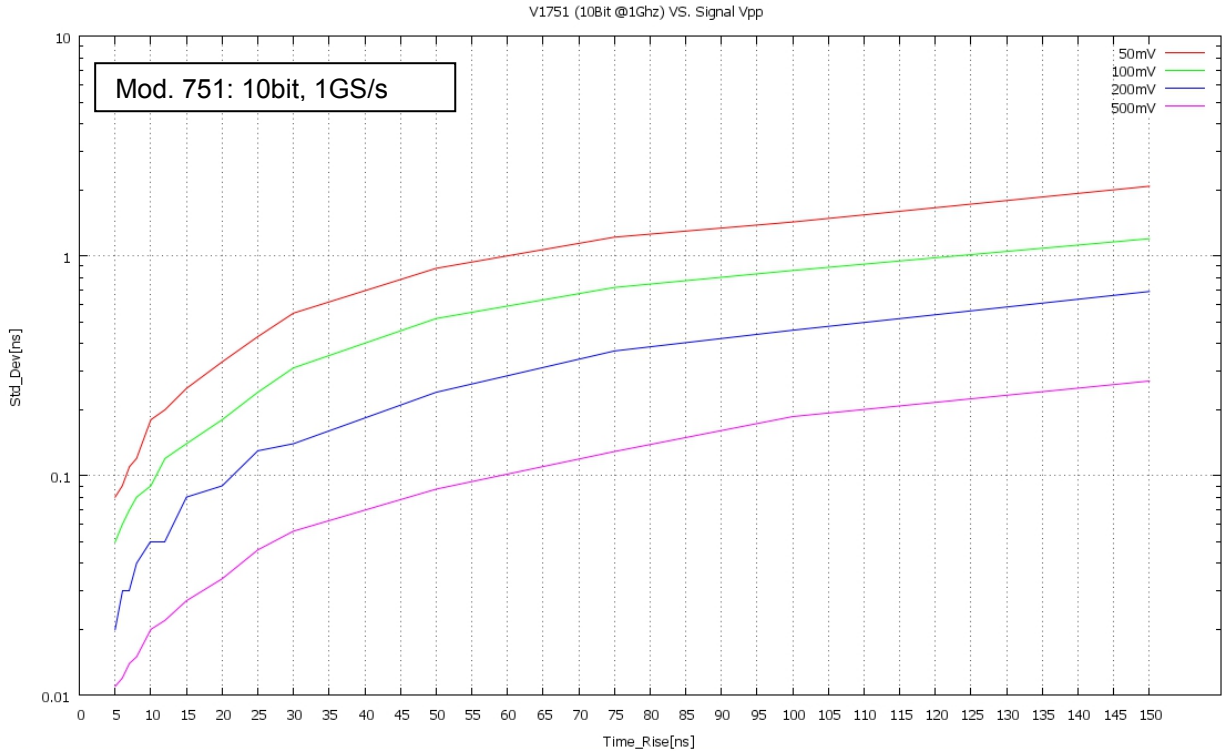


Fig. 2.13: Resolution as a function of the rise time for different signal amplitude (Mod. 751 running at 1GS/s)

Please notice that in the Fig. 2.14 the region with Rise Time < 5*Ts is missing.

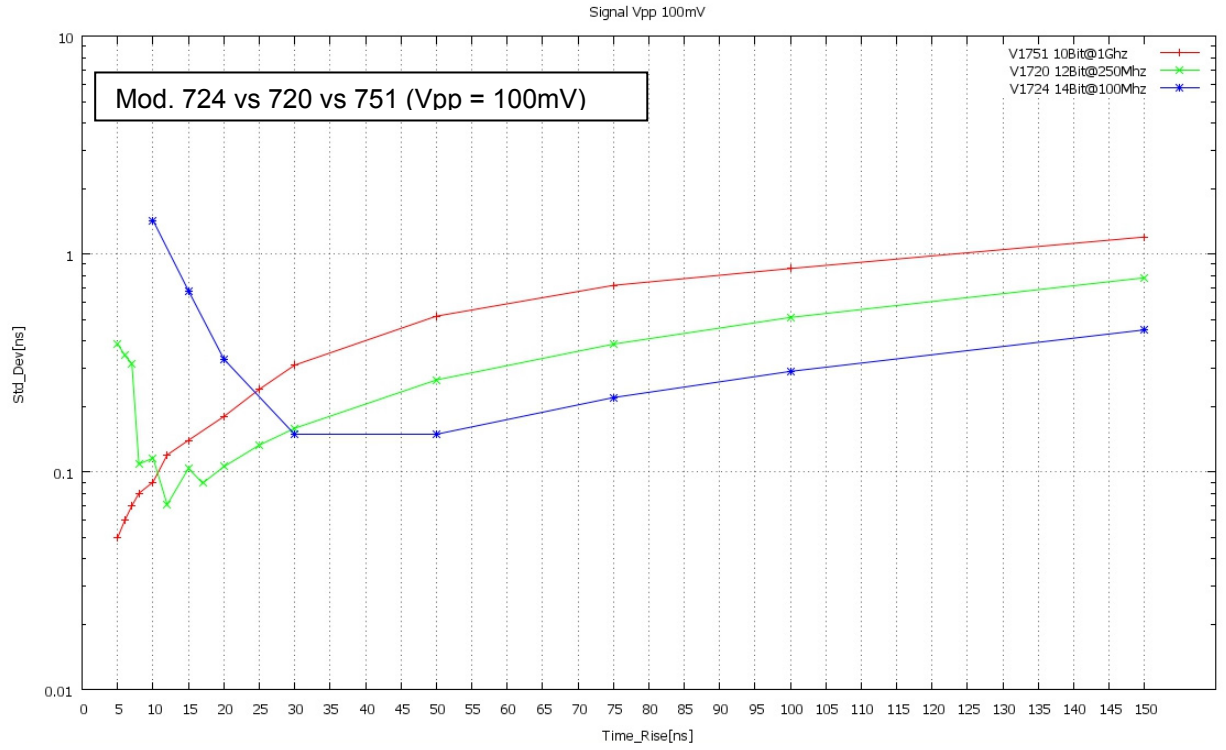
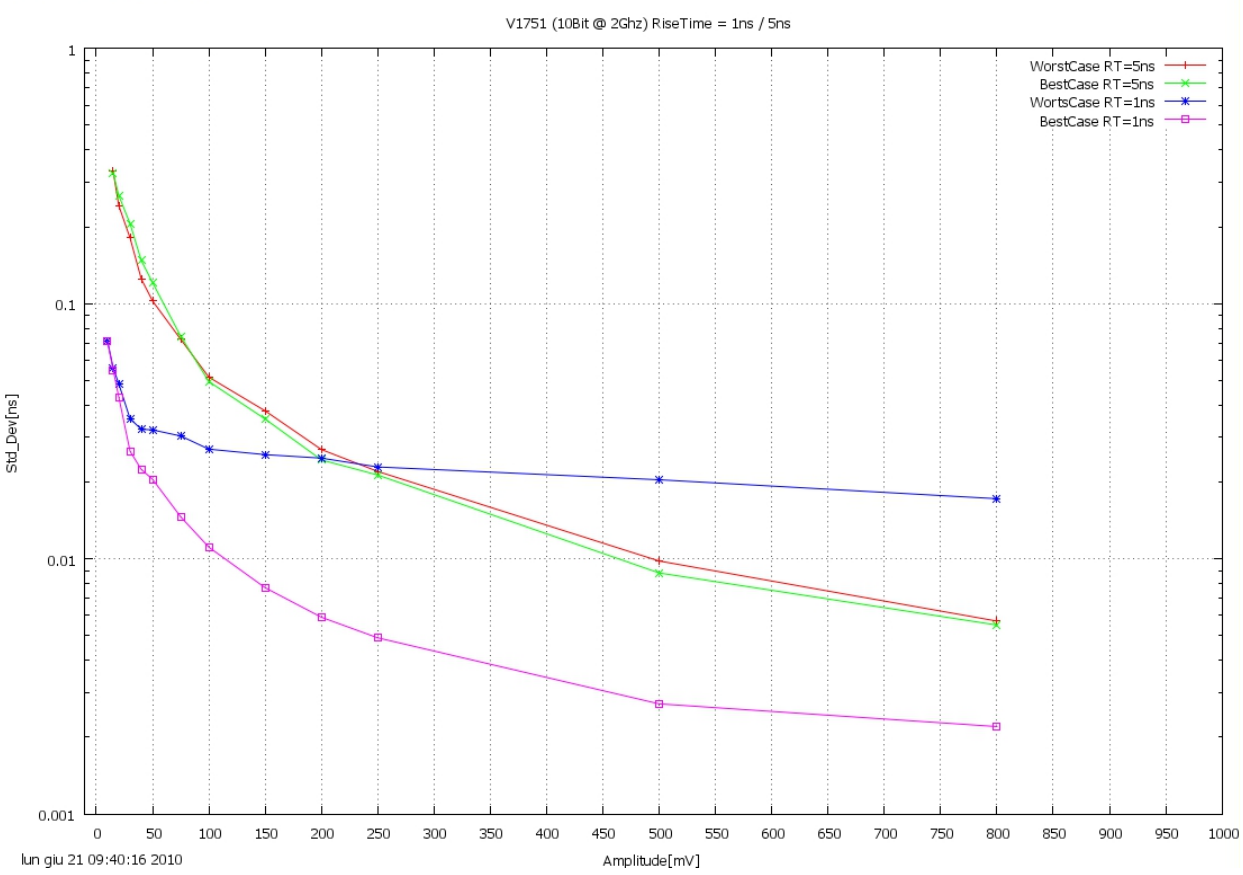


Fig. 2.14: Comparison between Mod. 724, 720 and 751 (signal amplitude = 100mV)

The next plot represents two acquisitions made with a very fast signal (1 ns and 5 ns rise time) in the worst and best cases (that is with $DELAY_{AB}$ = *(N+0.5)*Ts* and $DELAY_{AB}$ = *N*Ts* respectively) using a Mod. 751 running at 2 GS/s. The plots confirms that the difference between the best and the worst cases becomes almost negligible when the rise time is greater than 5*Ts (2.5 ns in this case), while the resolution is very sensitive to the interpolation error variation due to sampling clock phase in the region with rise time < 5*Ts. It is also clear that for small signals (amplitude < 50mV), the quantization error surpasses the interpolation error, thus best and worst cases get closer.



2.5 Particle Identification

A typical example of particle identification is the neutron-gamma discrimination in the acquisition with organic liquid detectors. The shape of the signal presents two exponential decay having different time constants. The ratio between the fast and the slow components gives information about the type of the particle. In both analog and digital acquisition systems, there are two main different approaches: rise-time (or zero crossing) versus energy correlation or ΔE/E correlation (double gate charge integration). The block diagram shown in the following figure shows how both approaches can be implemented in the FPGA of the digitizer reusing blocks already implemented for the DPP-TF and DPP-CI.

Right now CAEN is making some simulations and tests using these algorithms.

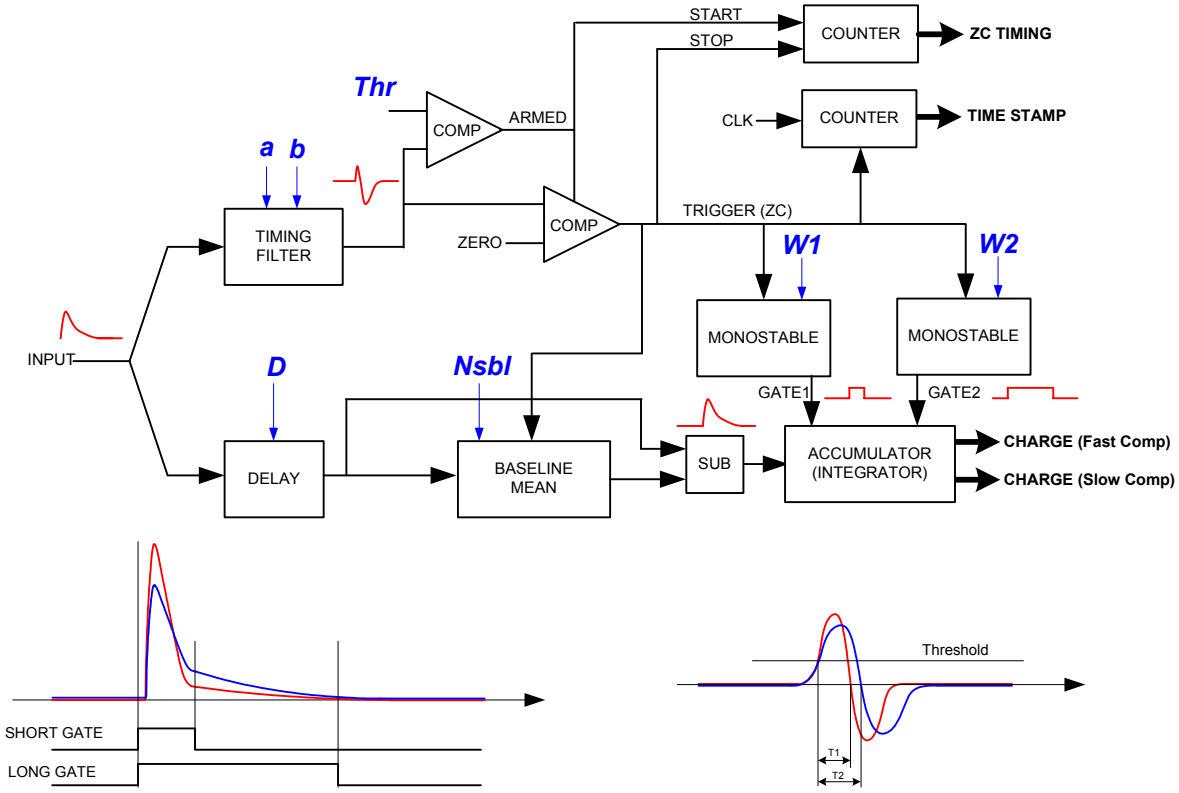


Fig. 2.15: Block Diagram of the firmware for the n-g discrimination

2.6 Pulse Counting (Multi Channel Scaler)

There are applications where it is not necessary to measure the energy nor the timing of the particles; it is only required to count all them or just those whose energy stays within a certain range (energy windowing). The traditional acquisition chains designed for this purpose are made out of a discriminator and a scaler. Also in this case, it is possible to do the same job with a single digitizer. CAEN has plans for doing this firmware in the high density digitizer Mod. 740; for example, in a VME board V1740 it would be possible to implement 64 Multi Channel Scalers that can be connected directly to the detectors.

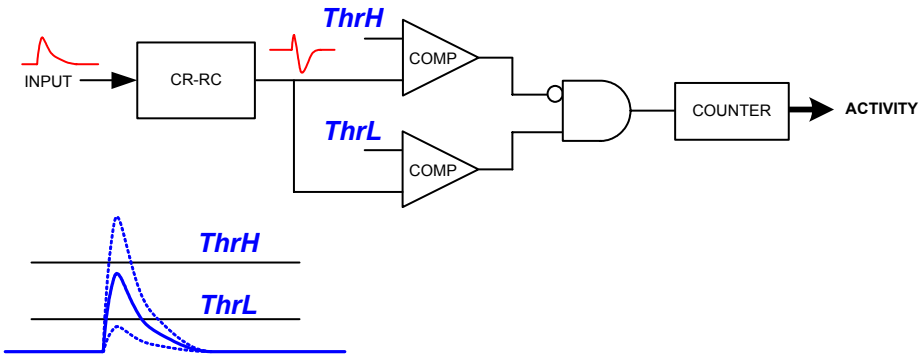


Fig. 2.16: Block Diagram of the firmware for the Multi Channel Scaler

3 Software Interface:

For the control of DPP Algorithms CAEN provides two demo Programs:

Program Name	*DPP algorithm*	*Waveform digitizer models*
DPP_TF_Runner	DPP with trapezoidal filters and digital CFD	724 series (14 bit 100 MS/s): • V1724/VX1724 (VME) • DT5274 (Desktop) • N6724 (NIM)
DPP_CI_ Runner	DPP for Charge to Digital Conversion	720 series (12 bit 250 MS/s): • V1720/VX1720 (VME) • DT5270 (Desktop) • N6720 (NIM)

Tab. 3.1: Software Demo Programs for DPP algorithms

DPP_XX_Runner are applications that manages the acquisition in the digitizers that have a DPP firmware installed on it. The program is made of different parts: there is a GUI whose purpose is to set all the parameters for the DPP and for the acquisition; the GUI generates a textual configuration file that contains all the parameters. This file is read by the Acquisition Engine, which is a C console application that programs the digitizer according to the parameters, starts the acquisition and manage the data readout. The data, that can be waveforms, time stamps, energies or other quantities of interest, can be saved to output files or plotted using gnuplot as an external plotting tool, exactly like in WaveDump.

NOTE: DPPRunner-TF works only with Mod. 724 and DPP-TF while DPPRunner-CI works only with Mod. 720 and DPP-CI

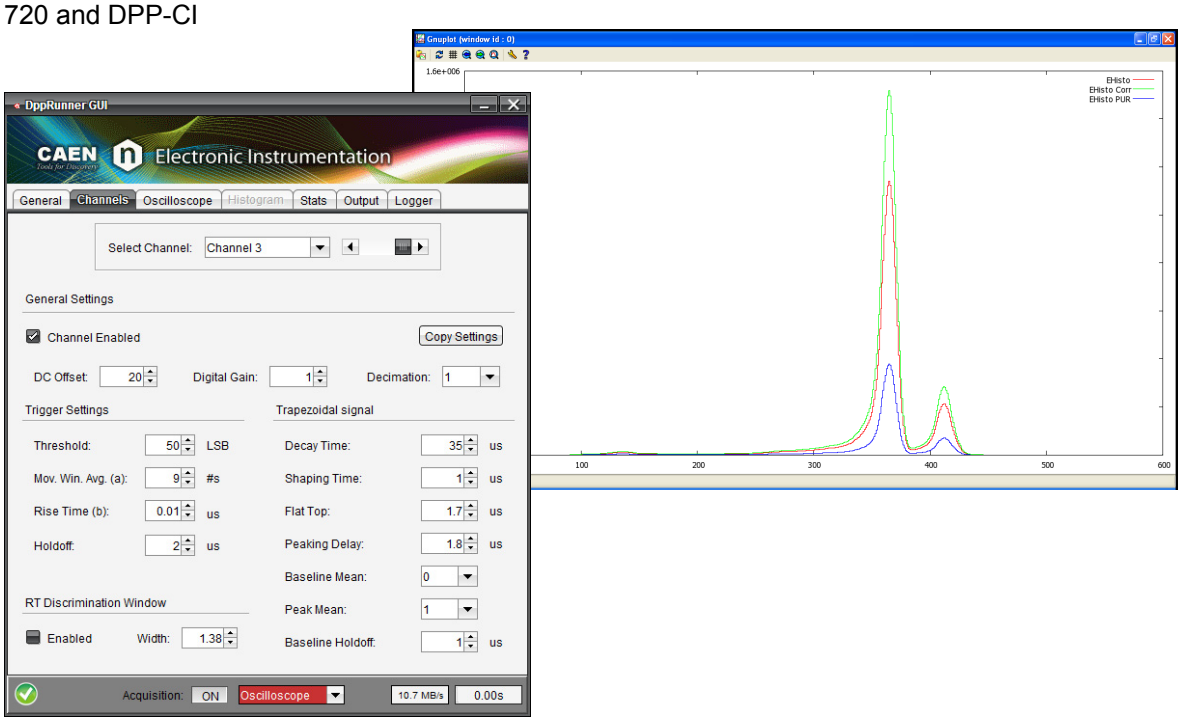


Fig. 3.1: Screenshot of DPPrunner Control Panel and plotter (gnuplot)