
MZTIO

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If you need firmware, please contact Hongyi Wu(wuhongyi@qq.com)

If you want to know how PKU uses MZTIO, please click on the link below: [PKUMZTIO](#)

XIA SUPPORT: [XIA Blog](#)

The Pixie-16 MZ-TrigIO is designed to route signals from the backplane (rear connectors) to the front panel (front connectors) and make logical combinations between them in FPGA fabric. It has the following features and capabilities:

- Ethernet programmable trigger/coincidence control module for the Pixie-16
 - 48+ Pixie-16 backplane trigger connections to local Zynq processor
 - 48 front panel LVDS connections to local Zynq processor
 - MicroZed Zynq processor with embedded Linux, acting as a standalone PC with built-in SD card drive, USB host, 10/100 Ethernet, webserver, etc
 - 1588 PTP and SyncE clock synchronization
 - Open source user access to software and firmware
 - Use as standalone desktop unit or in 6U PXI chassis
 - Custom I/O standards via daughtercards
-

1.1 Safety

Please take a moment to review these safety precautions. They are provided both for your protection and to prevent damage to the Pixie module and connected equipment. This safety information applies to all operators and service personnel.

- Power Source
 - The Pixie-16 MZ-TrigIO module is powered through an AC/DC wall adapter or a PXI backplane. The default adapter has a variety of AC plug attachments for different localities.

- Please remember to shut down the Linux OS before removing the power plug from the Pixie-16 MZ-TrigIO or powering down the PXI chassis.
 - User Adjustments/Disassembly
 - To avoid personal injury, and/or damage, always disconnect power before accessing the module's interior. There are a few jumpers related to clocking on the board that experienced users may want to use.
 - Voltage Ratings
 - Signals on the inputs and outputs must not exceed $\pm 3.3V$. Please review the pinout in the appendix before making any connections.
 - Daughtercards
 - Daughtercards can be used as alternatives to front panel and rear inputs, which requires caution to avoid conflicts from FPGA outputs and standard connector inputs.
 - Servicing and Cleaning
 - To avoid personal injury, and/or damage to the Pixie module or connected equipment, do not attempt to repair or clean the inside of these units.
 - Linux Passwords
 - The Pixie-16 MZ-TrigIO Linux OS comes with default user IDs and passwords for 1) SSH login, 2) SMB file sharing, and 3) Web Operations as described below. Users should immediately change these passwords, especially when the Pixie-16 MZ-TrigIO is connected to external networks. Don't let hackers take over your Pixie-16 MZ-TrigIO!
 - Linux Backup
 - The Pixie-16 MZ-TrigIO Linux OS is stored on a removable SD card. SD cards' file systems can become corrupted, which would crash the Linux system and make the Pixie-16 MZ-TrigIO unable to operate. Therefore periodic backup of the SD card is recommended, for example using Win32DiskImager. (Byte for byte copy is required).
 - Note that all Linux passwords are stored on the SD card.
-

1.2 Logic programming

In order to meet the needs of medium and low energy experimental nuclear physics, we have developed the following basic functions.

- signal delay
- signal extend
- coincidence
- multiplicity
- scaler/counter
- down scale
- remote parameter adjustment
-

2.1 register

The user can easily adjust the experimental logic by modifying the control registers in the settings.ini file.

Of course, for different types of experiments, we have specialized software, please refer to the manual of the experiment for the specific register control method.

```

settings.ini - Hongyi Wu @ Peking University (于 PixieNet)
File Edit Options Buffers Tools Conf Help
1 0x000 0 CSR[15:0] (R)
2 0x001 0 VERSION (R)
3 0x002 0 D18[2:0] (W/R)
4 0x003 0 outblock[1:0] (W/R)
5 0x00A 0 numtrig (R)
6 0x00B 0 numtrig (R)
7 0x00C 0 runticks (R)
8 0x00D 0 runticks (R)
9 0x100 0x6666 FrontIO_Aena (W/R)
10 0x105 0x6666 LVDSIO_Aena (W/R)
11 0x101 0x6666 FrontIO_Bena (W/R)
12 0x106 0x6666 LVDSIO_Bena (W/R)
13 0x102 0x6600 FrontIO_Cena (W/R)
14 0x107 0x6666 LVDSIO_Cena (W/R)
15 0x103 0x00000000 TriggerAllena (W/R)
16 0x104 0x0000 EB_Dataena (W/R)
17 0x108 0xFFFF frontA_coincidence_mask (W/R)
18 0x109 0xFFFF frontB_coincidence_mask (W/R)
19 0x10A 0xFFFF frontC_coincidence_mask (W/R)
20 0x10B 0xFFFFFFFF TriggerAll_coincidence_mask (W/R)
21 0x10C 0xFFFF EB_Data_coincidence_mask (W/R)
22 0x110 0xFFFF frontA_multiplicity_mask (W/R)
23 0x111 0xFFFF frontB_multiplicity_mask (W/R)
24 0x112 0xFFFF frontC_multiplicity_mask (W/R)
25 0x113 0xFFFFFFFF TriggerAll_multiplicity_mask (W/R)
26 0x114 0xFFFF EB_Data_multiplicity_mask (W/R)
27 0x118 0x0000 frontA_coincidence_pattern (W/R)
28 0x119 0x0000 frontB_coincidence_pattern (W/R)
29 0x11A 0x0000 frontC_coincidence_pattern (W/R)
30 0x11B 0x00000000 TriggerAll_coincidence_pattern (W/R)
31 0x11C 0x0000 EB_Data_coincidence_pattern (W/R)
32 0x120 2 frontA_multiplicity_threshold (W/R)
33 0x121 2 frontB_multiplicity_threshold (W/R)
34 0x122 2 frontC_multiplicity_threshold (W/R)
35 0x123 2 TriggerAll_multiplicity_threshold (W/R)
36 0x124 2 EB_Data_multiplicity_threshold (W/R)
37 0x128 0 frontA_output_select (W/R)
38 0x129 0 frontB_output_select (W/R)
39 0x12A 0 frontC_output_select (W/R)
40 0x12B 0 TriggerAll_output_select (W/R)
41 0x12C 0 EB_Data_output_select (W/R)
42 0x030 0x00320028 DelayAndExtend1 (W/R)
43 0x031 0x000A DownScale1 (W/R)
44 0x040 0 LEMO output mode (W/R)
1 -:--- settings.ini All (1,0) (Conf[Space]) 07:49 0.20
Package assoc is obsolete!


```

2.2 web pages

2.2.1 main page


The main page of the web, it will provide basic information and precautions for the module.

不安全 | 222.29.111.225/index.html



Pixie-16 MZ Trigger IO

Thank you for using PKUXIADAQ



[Main](#)
[Status](#)
[Log](#)
[Support](#)

The Pixie-16 MZ-TrigIO is designed to route signals from the backplane (rear connectors) to the front panel (front connectors) and make logical combinations between them in FPGA fabric. It has the following features and capabilities:

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- Custom I/O standards via daughtercards

Do not visit the Status page while execute other tasks.


When you access the Status page, the page will automatically refresh every 5 seconds.

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2.2.2 control page


The control register is used to change the experimental trigger mode, delay and stretch of logic signals, and so on.

222.29.111.140/control.html



Pixie-16 MZ Trigger IO

Thank you for using GDDAQ



[Main](#)
[Control](#)
[Status](#)
[Log](#)
[Support](#)

System Initialization

When you turn on MZTIO, it should be initialized immediately.

Initialize: [Program FPGA](#)

Oscilloscope Monitoring

The expansion board has 4 channel outputs. Please connect them to the oscilloscope in turn. Then select the output for each channel through the following.

[Read](#) [Change](#)

LEMO output mode	ch 1	ch 2	ch 3	ch 4
Vaule	<input type="text" value="28"/>	<input type="text" value="29"/>	<input type="text" value="30"/>	<input type="text" value="31"/>

00:A1_I 01:A1_I 02:A2_I 03:A2_I 04:A3_I 05:A3_I 06:A4_I 07:A4_I 08:B1_I 09:B1_I 10:B2_I 11:B2_I 12:B3_I 13:B3_I 14:B4_I 15:B4_I 16:C1_I 17:C1_I 18:C2_I 19:C2_I 20:C3_I 21:C3_I 22:C4_I 23:C4_I 24:DPMFULLOUT 25:SYNCOUT 26:ETLOCAL 27:FTLOCAL 28:DEBUG0 29:DEBUG1 30:DEBUG2 31:DEBUG3

Settings

Control register to change experimental trigger mode, delay and stretch of logic signal

Register: Value: [Read](#) [Write](#)

0x30-0x3F: DelayAndExtend, 0x44: DownScale

Others

Run executables as if typed in terminal:

- [progflippi](#)
- [clockprog](#)

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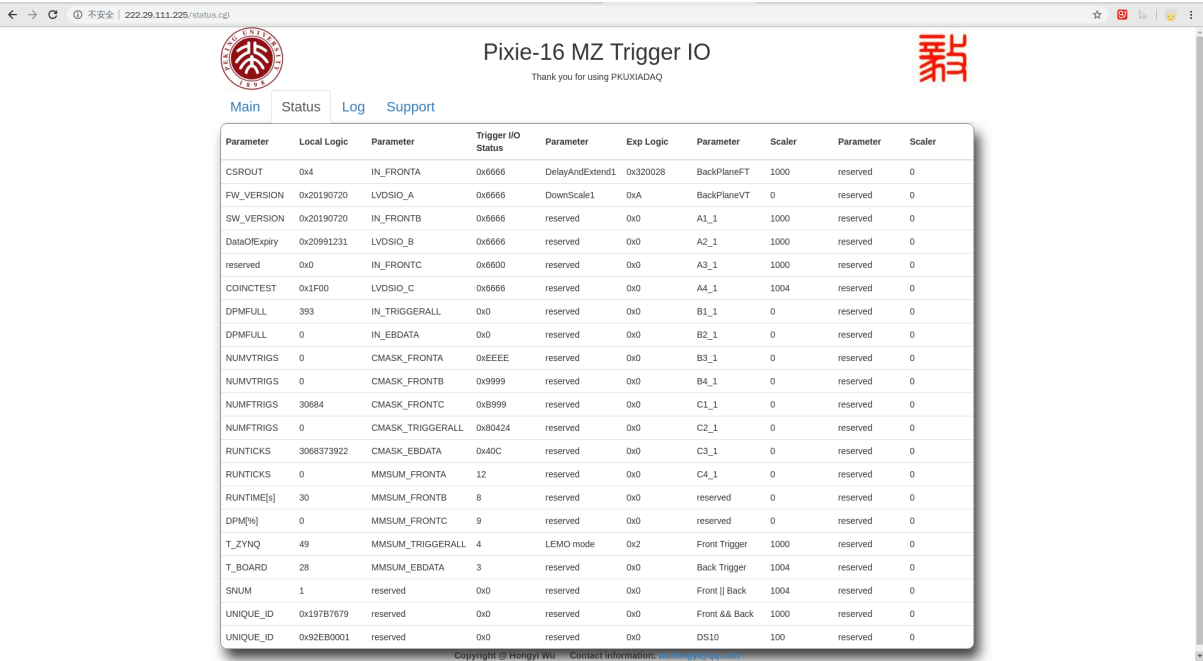
2.2.3 status page

When you access the status page, the page will automatically refresh every 5 second.

There are currently five columns of monitorable parameters on this page.

- The fourth row of the first column indicates the date the solid is allowed to be used.
- The fifteenth line of the first column indicates the running time of the current round of DAQ.
- The first column, line 16, represents the percentage of DPMFULL and total runtime.

The parameters of the third column, the fourth column and the fifth column are determined by the settings of each experiment. For details, please refer to the manual of the specific experiment settings.



2.2.4 log page

In development, this page will save the status parameters and read the historical parameters.

2.2.5 support page

This page provides some basic instructions, including XIA instructions, PKU instructions, and more.

2.3 Oscilloscope

Output signals to the oscilloscope through the MZTIO daughter board.

Most oscilloscopes have only 4 channels, so our monitor settings are set by default for 4 channels. If you want to monitor 8 channels at the same time, you can do it with 2 oscilloscopes.

Of course, the monitored signal can be switched by modifying the control register. For instructions on how to monitor different signals, please read the instructions for the specific experiment.

The following figure is an example of oscilloscope monitoring. Line 1 represents the trigger signal, line 2 is the down scale 10, line 3 represents the signal after line 1 is delayed by 400 ns, and line 4 represents line 3 is extend to 500 ns.



2.4 FIFO IP code limits

The figure below shows the settable range of the FIFO IP core parameters.

Component Name
fifo_delay512

Basic
Native Ports
Status Flags
Data Counts
Summary

Optional Flags

☐ Almost Full Flag
☐ Almost Empty Flag

Handshaking Options

Write Port Handshaking

☐ Write Acknowledge
Active High
☐ Overflow
Active High

Read Port Handshaking

☐ Valid Flag
Active High
☐ Underflow Flag
Active High

Programmable Flags

Programmable Full Type	No Programmable Full Threshold	
Full Threshold Assert Value	511	[6 - 511]
Full Threshold Negate Value	510	[5 - 510]
Programmable Empty Type	No Programmable Empty Threshold	
Empty Threshold Assert Value	4	[4 - 510]
Empty Threshold Negate Value	5	[5 - 511]

Due to the limitation of the FIFO IP core, the delay is set to a minimum of 4 clocks.

Connect the USB cable to your computer to get the IP
Serial communication software(minicom) can be used in Linux OS

```
+-----[configuration]-----+
| Filenames and paths          |
| File transfer protocols      |
| Serial port setup           |
| Modem and dialing           |
| Screen and keyboard         |
| Save setup as dfl            |
| Save setup as..             |
| Exit                         |
| Exit from Minicom           |
+-----+-----+
```

- Enter *Serial port setup* , modify Serial Device to */dev/ttyUSB0* . Bps/Par/Bits change to *115200 8N1*, the bottom two options are *NO*
- Enter *Modem and dialing* , delete A, B, and K items
- Then select *Save setup as df1* to save the settings
- Finally, select *Exit* to exit the configuration mode and enter the control mode

The password is the default, so users can log in.

```
ssh -Y root@222.29.111.80
```

3.2 static IP setting

Because Ubuntu 18.04 uses netplan to manage the network. So you can create a file ending in yaml in the /etc/netplan/ directory. For example, the 01-netplan.yaml file.

Then write the following configuration under this file(You need to modify the IP address and gateway):

```
network:
  version: 2
  renderer: networkd
  ethernets:
    enp3s0:
      dhcp4: no
      addresses: [192.168.1.110/24]
      gateway4: 192.168.1.1
      nameservers:
        addresses: [8.8.8.8, 114.114.114.114]
```

It is important to note that the spaces in each line must be there, otherwise the error will be reported and the setting will fail!

```
network:
  version: 2
  renderer: networkd
  ethernets:
    eth0:
      addresses: [10.10.6.33/24]
      gateway4: 10.10.6.10
      dhcp4: no
```

The above parameters are the configurations used by the CIAE experiment.

Finally, use `sudo netplan apply` to restart the network service. Use `ip a` to see if your static IP is set up successfully!

4.1 basic configuration

4.1.1 ubuntu 18

If the operating system is the latest version, no additional source configuration is required.

If you want to install CERN ROOT, add the following line to `/etc/apt/sources.list`

```
deb http://ports.ubuntu.com/ xenial main universe multiverse
```

4.1.2 ubuntu 12

If the operating system version is the previous version, you need to modify the source configuration as follows.

Edit source list file

```
vim /etc/apt/sources.list
```

change into:

```
deb http://old-releases.ubuntu.com/ubuntu vivid main restricted universe multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-security main restricted universe↵
↵multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-updates main restricted universe↵
↵multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-proposed main restricted universe↵
↵multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-backports main restricted universe↵
↵multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid main restricted universe↵
↵multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid-security main restricted↵
↵universe multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid-updates main restricted↵
↵universe multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid-proposed main restricted↵
↵universe multiverse
```

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(续上页)

```
deb-src http://old-releases.ubuntu.com/ubuntu vivid-backports main restricted_
↪universe multiverse

deb http://mirrors.ustc.edu.cn/ubuntu/ vivid main universe
deb-src http://mirrors.ustc.edu.cn/ubuntu/ vivid main universe
```

4.1.3 software upgrade

```
apt-get update
```

```
#install firefox
apt-get install firefox
# install emacs
apt-get install emacs

# ROOT dependent library
apt-get install cmake
apt-get install libx11-dev
apt-get install libxpm-dev
apt-get install libxft-dev
apt-get install libxext-dev
apt-get install gfortran
apt-get install libssl-dev
apt-get install xlibmesa-glu-dev
apt-get install libglew1.5-dev
apt-get install libftgl-dev
apt-get install libmysqlclient-dev
apt-get install libfftw3-dev
apt-get install libcfitsio-dev
apt-get install graphviz-dev
apt-get install libavahi-compat-libdnssd-dev
apt-get install libxml2-dev
apt-get install libkrb5-dev
apt-get install libgsl0-dev
apt-get install libqt4-dev

#install django
apt install python3-pip
pip3 install django==2.2
```

```
apt-get install root-system-bin
```

Ubuntu color configuration, place the color configuration file `.dircolors` in the personal directory, the file name is `.dir_colors` in the readhat system.

4.1.4 Time zone select

```
#First check the current system time
date -R
#Check the displayed time zone. If it is not consistent with the local time zone,
↪you can modify it in the following ways:

tzselect
#The figure below shows how Chinese users can modify the local time zone. Users in
↪other regions can make corresponding selections.
cp /usr/share/zoneinfo/Asia/Shanghai /etc/localtime
```

(下页继续)

(续上页)

```
#Check if the modification is successful  
date -R
```

```
root@ubuntu:/# tzselect
Please identify a location so that time zone rules can be set correctly.
Please select a continent, ocean, "coord", or "TZ".
 1) Africa
 2) Americas
 3) Antarctica
 4) Asia
 5) Atlantic Ocean
 6) Australia
 7) Europe
 8) Indian Ocean
 9) Pacific Ocean
10) coord - I want to use geographical coordinates.
11) TZ - I want to specify the time zone using the Posix TZ format.
#? 4
Please select a country whose clocks agree with yours.
 1) Afghanistan      18) Israel           35) Palestine
 2) Armenia          19) Japan            36) Philippines
 3) Azerbaijan       20) Jordan           37) Qatar
 4) Bahrain          21) Kazakhstan       38) Russia
 5) Bangladesh       22) Korea (North)    39) Saudi Arabia
 6) Bhutan           23) Korea (South)    40) Singapore
 7) Brunei           24) Kuwait           41) Sri Lanka
 8) Cambodia         25) Kyrgyzstan       42) Syria
 9) China            26) Laos             43) Taiwan
10) Cyprus           27) Lebanon          44) Tajikistan
11) East Timor       28) Macau            45) Thailand
12) Georgia          29) Malaysia         46) Turkmenistan
13) Hong Kong        30) Mongolia         47) United Arab Emirates
14) India            31) Myanmar (Burma)  48) Uzbekistan
15) Indonesia        32) Nepal            49) Vietnam
16) Iran             33) Oman             50) Yemen
17) Iraq            34) Pakistan

#? 9
Please select one of the following time zone regions.
 1) Beijing Time
 2) Xinjiang Time
#? 1
The following information has been given:

      China
      Beijing Time

Therefore TZ='Asia/Shanghai' will be used.
Local time is now:      Tue Jan 16 09:29:44 CST 2018.
Universal Time is now:  Tue Jan 16 01:29:44 UTC 2018.
Is the above information OK?
 1) Yes
 2) No
#? 1
You can make this change permanent for yourself by appending the line
      TZ='Asia/Shanghai'; export TZ
to the file '.profile' in your home directory; then log out and log in again.

Here is that TZ value again, this time on standard output so that you
can use the /usr/bin/tzselect command in shell scripts:
Asia/Shanghai
root@ubuntu:/#
```

4.2 Restore SD card space

In order to speed up the installation speed of the image, only the SD card space of about 8/16G is actually formatted. The 16/32G SD card and the 8/16G space are not used. In order to be able to use, the following operations are performed.

```
fdisk /dev/mmcblk0
# Then enter: d [ENTER],2 [ENTER],n[ENTER] [ENTER],[ENTER],[ENTER],[ENTER],
↪w[ENTER]. Then reboot the OS. If there is a problem, please refer to *Getting_
↪started with Xillinux for Zynq-7000 EPP*
```

```
# Execute the following command
resize2fs /dev/mmcblk0p2

# Use the following command to view the result
df -h
```

4.3 update the boot files

To mount the SD card boot partition to a folder /mnt/sd, execute

```
mount /dev/mmcblk0p1 /mnt/sd
```

this is useful to update the boot files without removing the SD card. The Pixie-16 MZ-TrigIO has to be rebooted before the new boot files become effective.

So the procedure would be:

- generate FW files on a desktop PC
- copy to shared Linux folder on the SD card (/var/www)
- mount boot partition mount /dev/mmcblk0p1 /mnt/sd (create /mnt/sd if not already there)
- copy files e.g. cp /var/www/xillydemo.bit /mnt/sd
- reboot or power cycle (reboot)

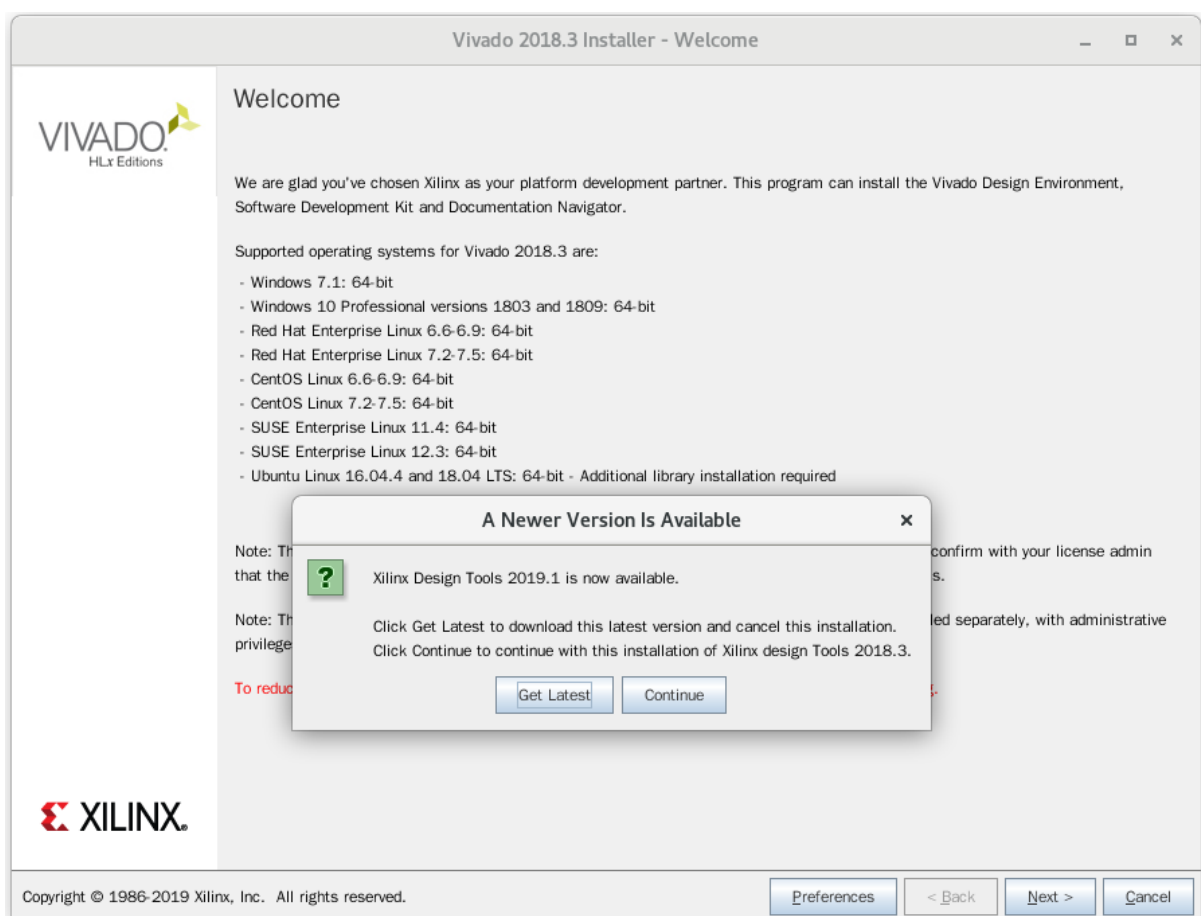
```
scp xillydemo.bit root@222.29.111.157:~
```

4.4 /dev/mmcblk0p1

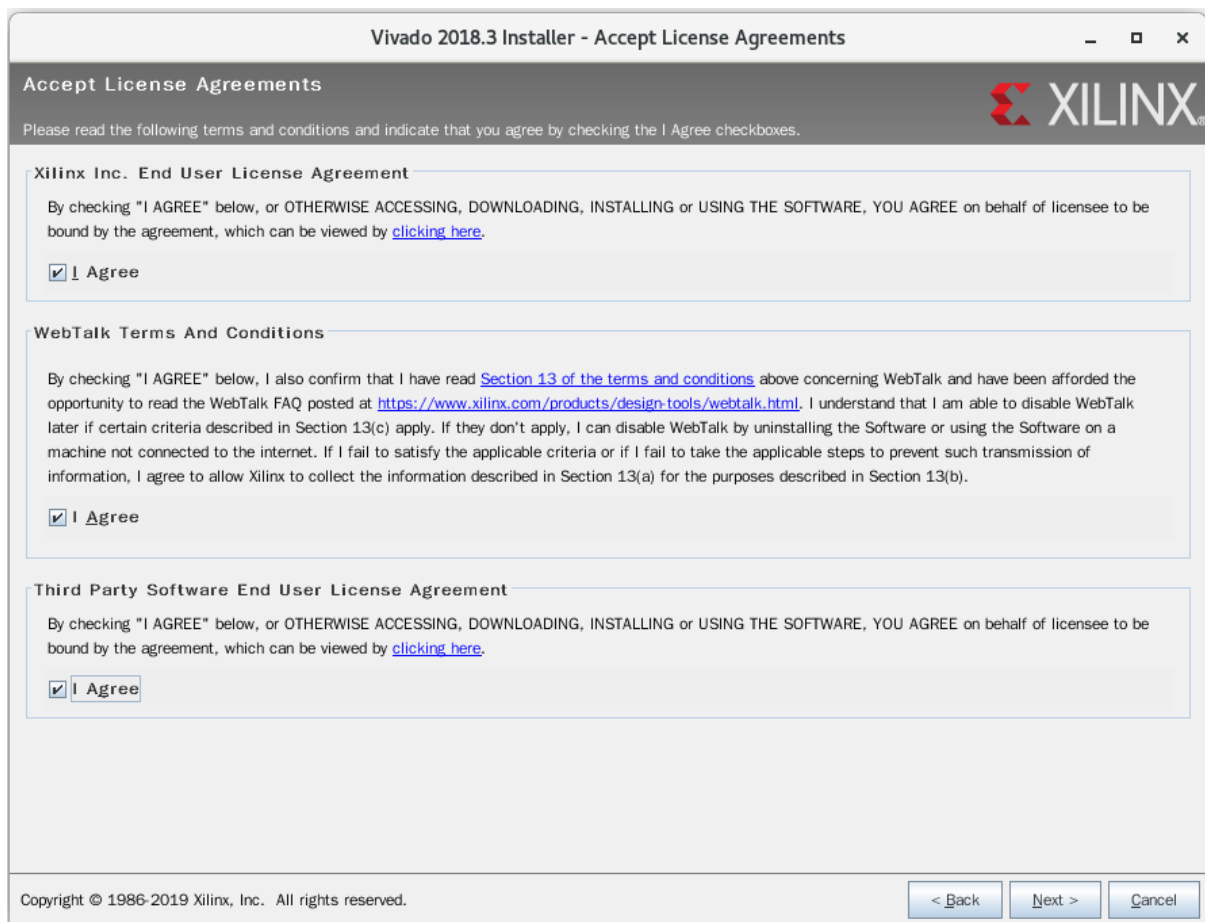
```
boot.bin  devicetree.dtb  uImage  xillydemo.bit
```


5.1 Install

```
tar -zxvf Xilinx_Vivado_SDK_2018.3_1207_2324.tar.gz
cd Xilinx_Vivado_SDK_2018.3_1207_2324
./xsetup
```



Click “continue” to choose not to download the latest version, then click “Next” to go to the next step

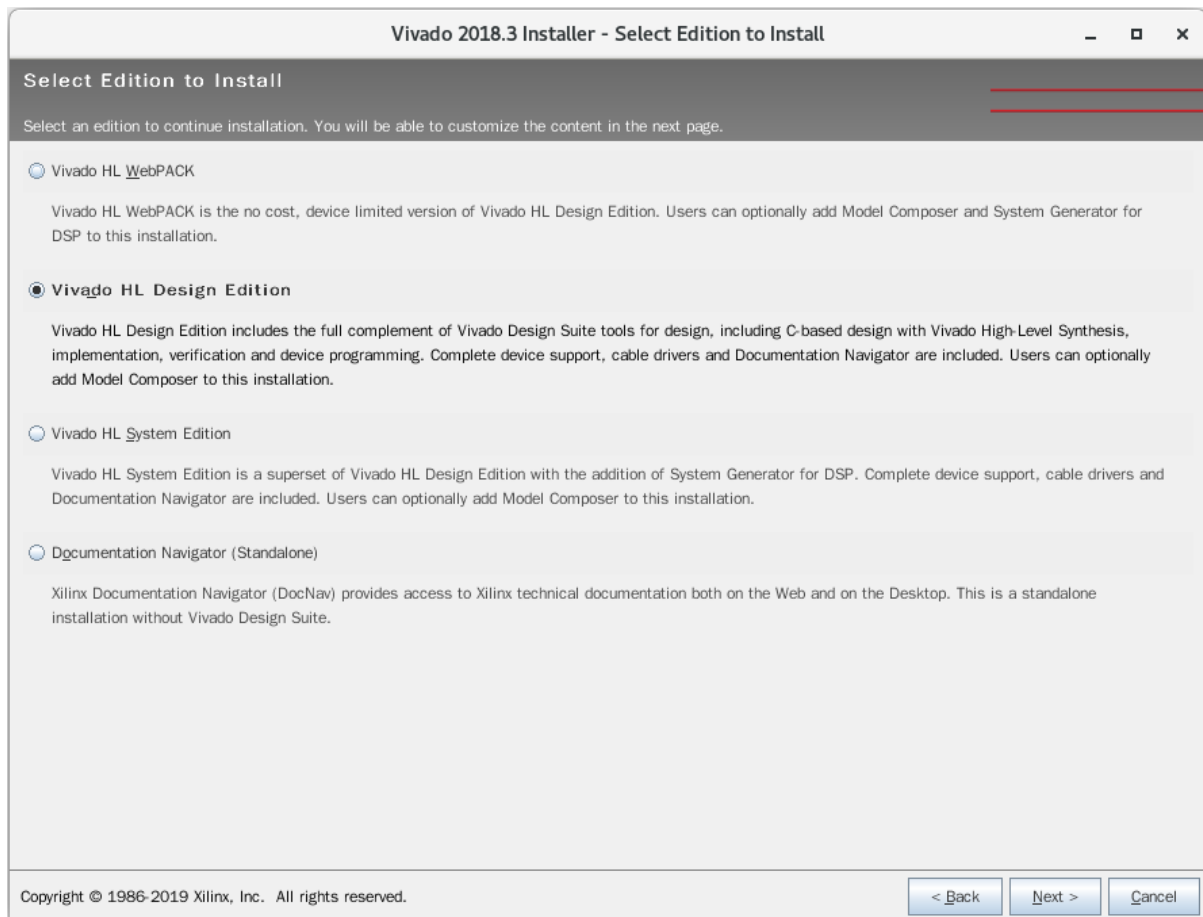


The image shows a screenshot of the "Vivado 2018.3 Installer - Accept License Agreements" window. The window has a title bar with standard Windows window controls. Below the title bar, there is a header section with the text "Accept License Agreements" and the Xilinx logo. A paragraph of text reads: "Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes." The main content area is divided into three sections, each with a title and a paragraph of text, followed by an "I Agree" checkbox:

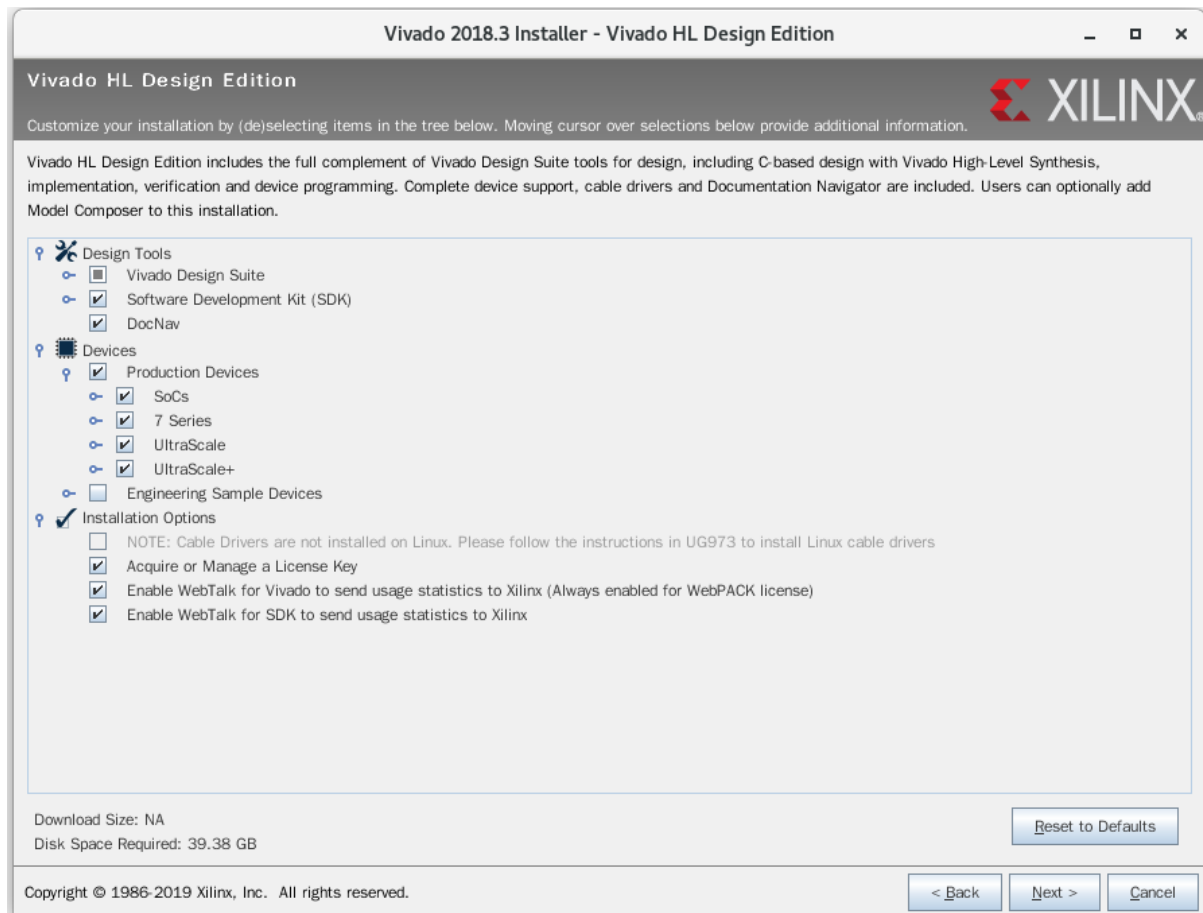
- Xilinx Inc. End User License Agreement**
By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).
☒ I Agree
- WebTalk Terms And Conditions**
By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).
☒ I Agree
- Third Party Software End User License Agreement**
By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).
☒ I Agree

At the bottom of the window, there is a footer with the text "Copyright © 1986-2019 Xilinx, Inc. All rights reserved." and three buttons: "< Back", "Next >", and "Cancel".

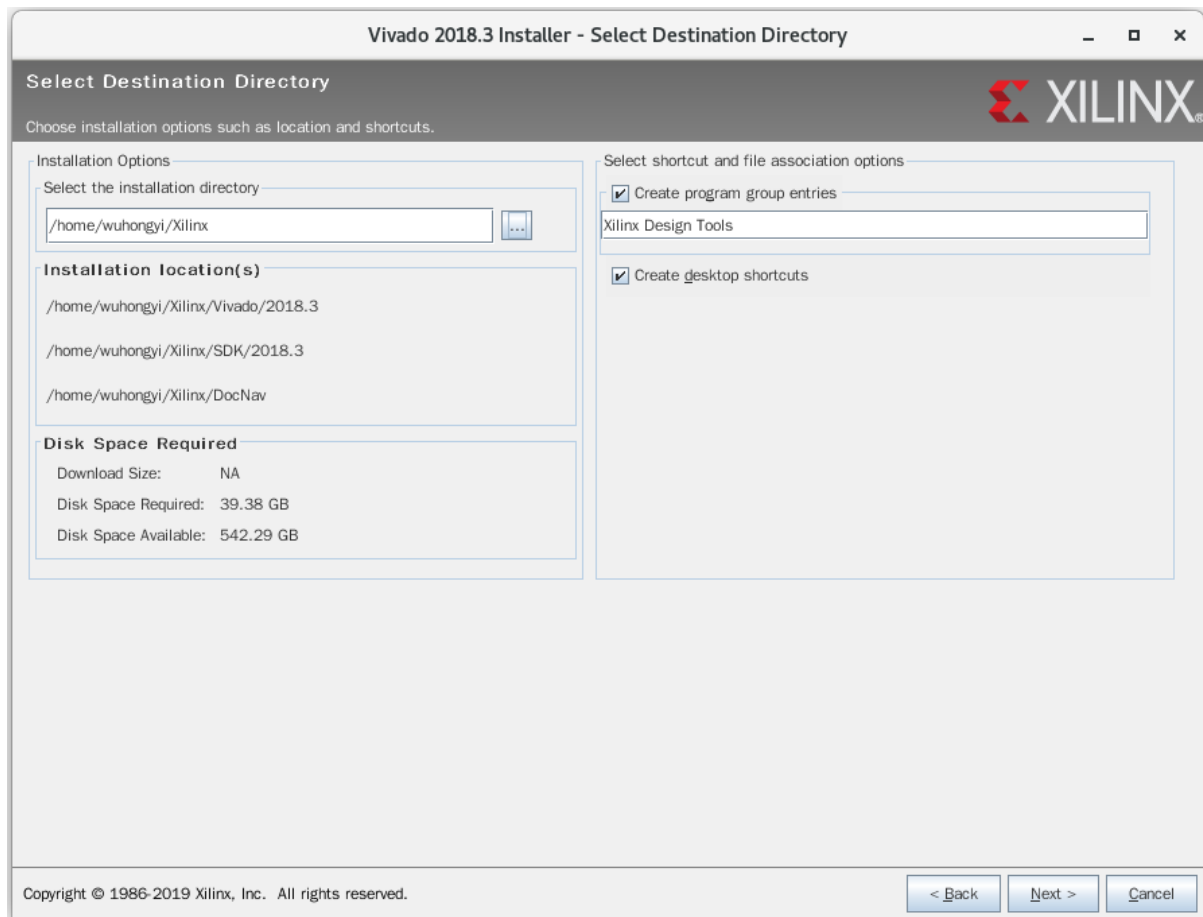
Click on the three optional boxes and then click “Next” to go to the next step



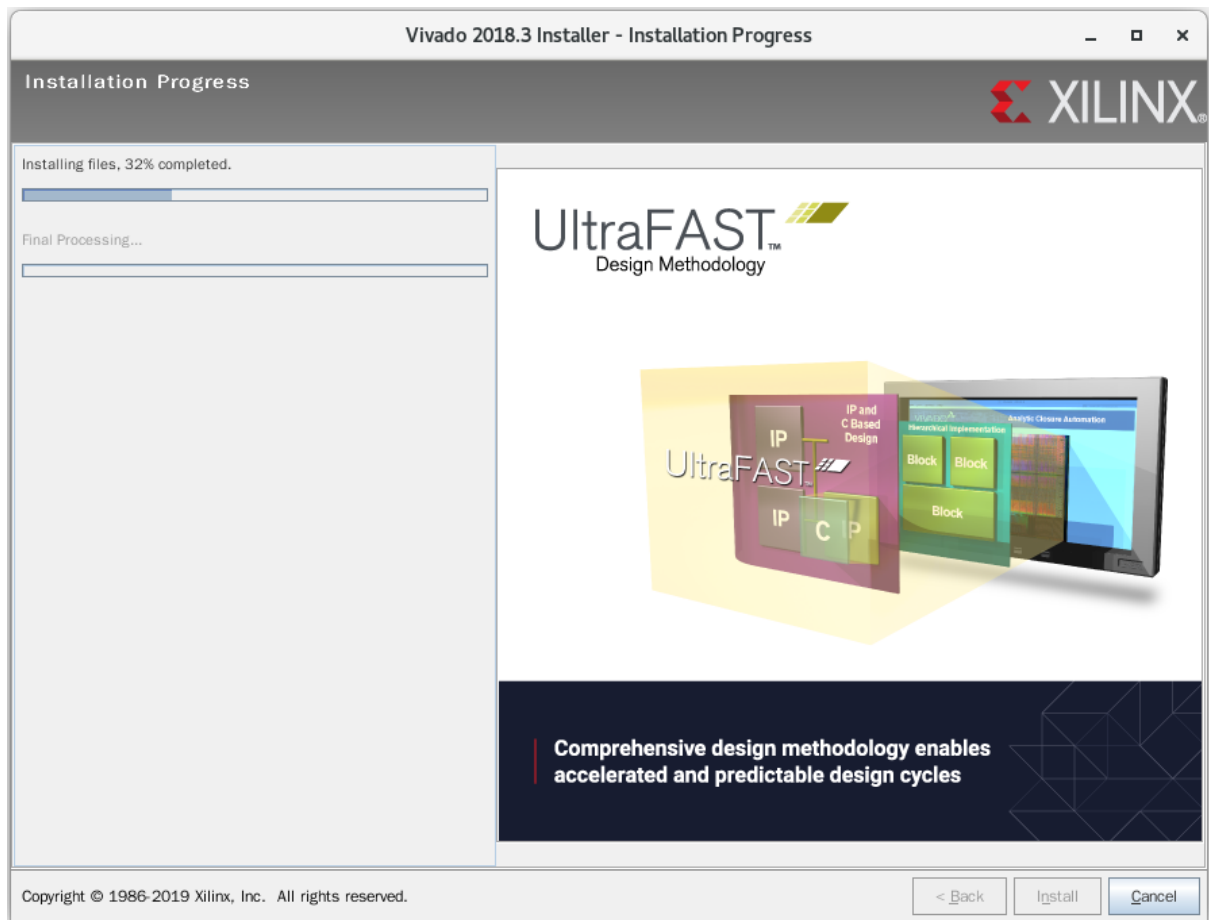
Select “Vivado HL Design Edition” and click “Next” to go to the next step



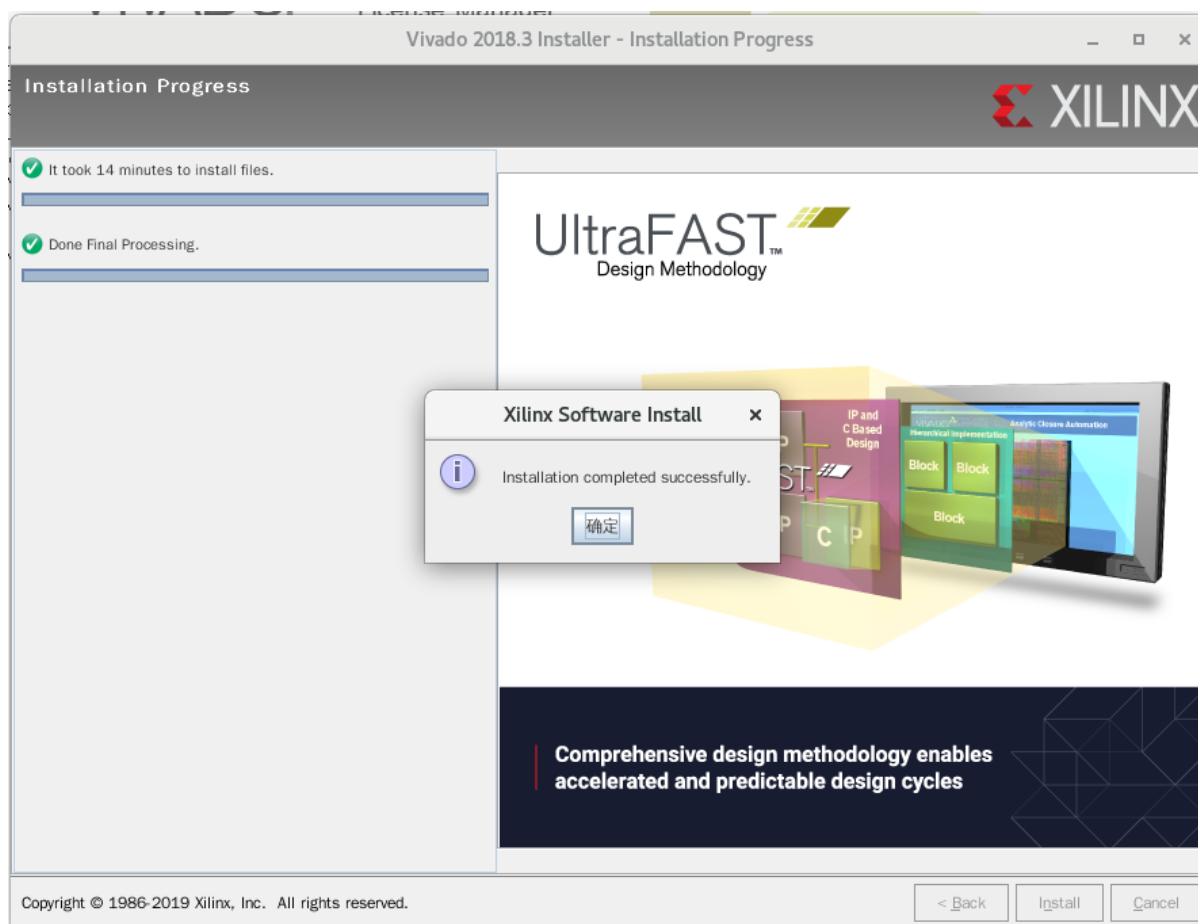
Click “Next” directly to enter the next step



Select the installation directory, here I choose to install to “/home/wuhongyi/Xilinx” , and then click “Next” to enter the next step



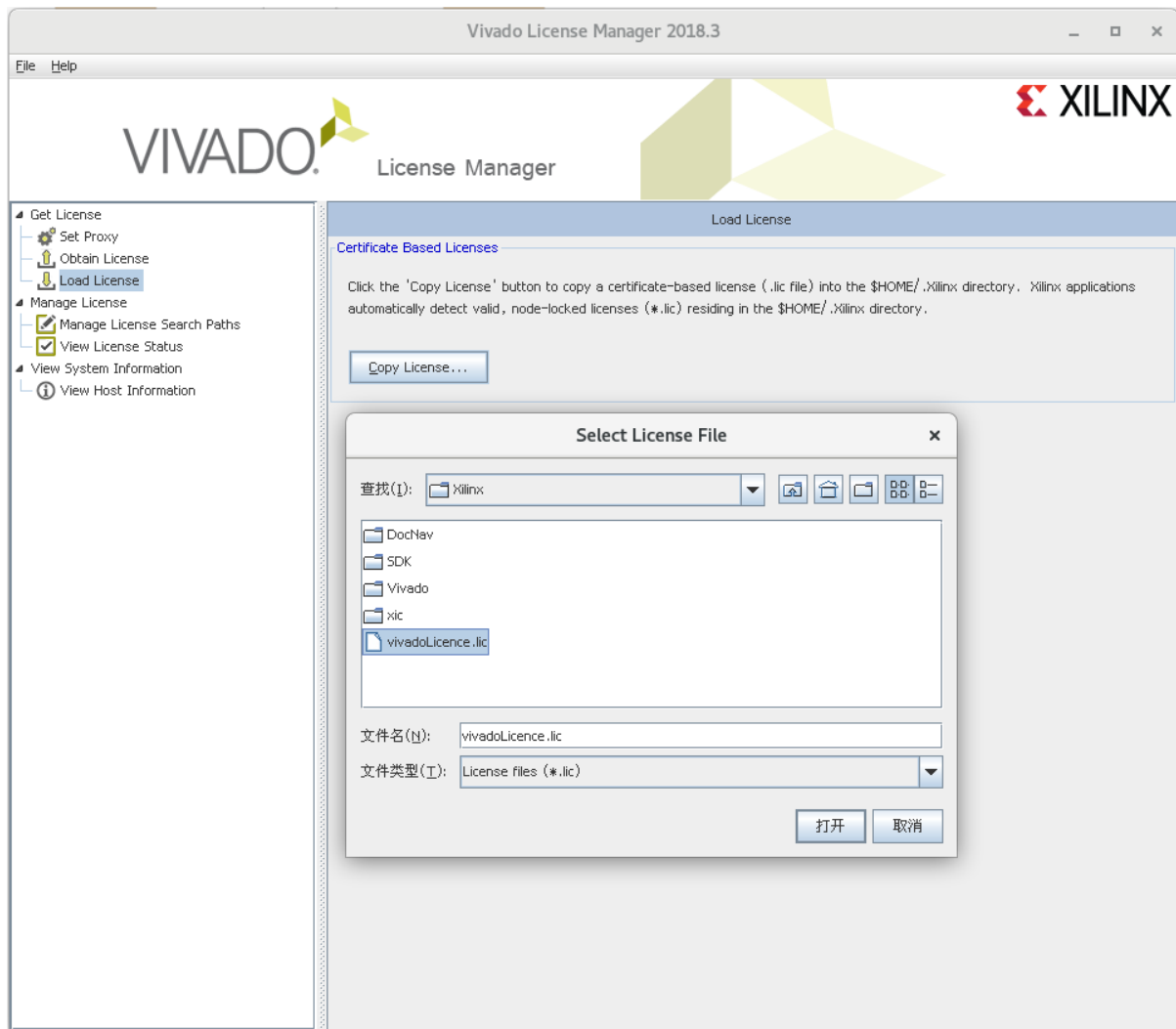
Wait for the installation to complete



The following two steps are not necessary.

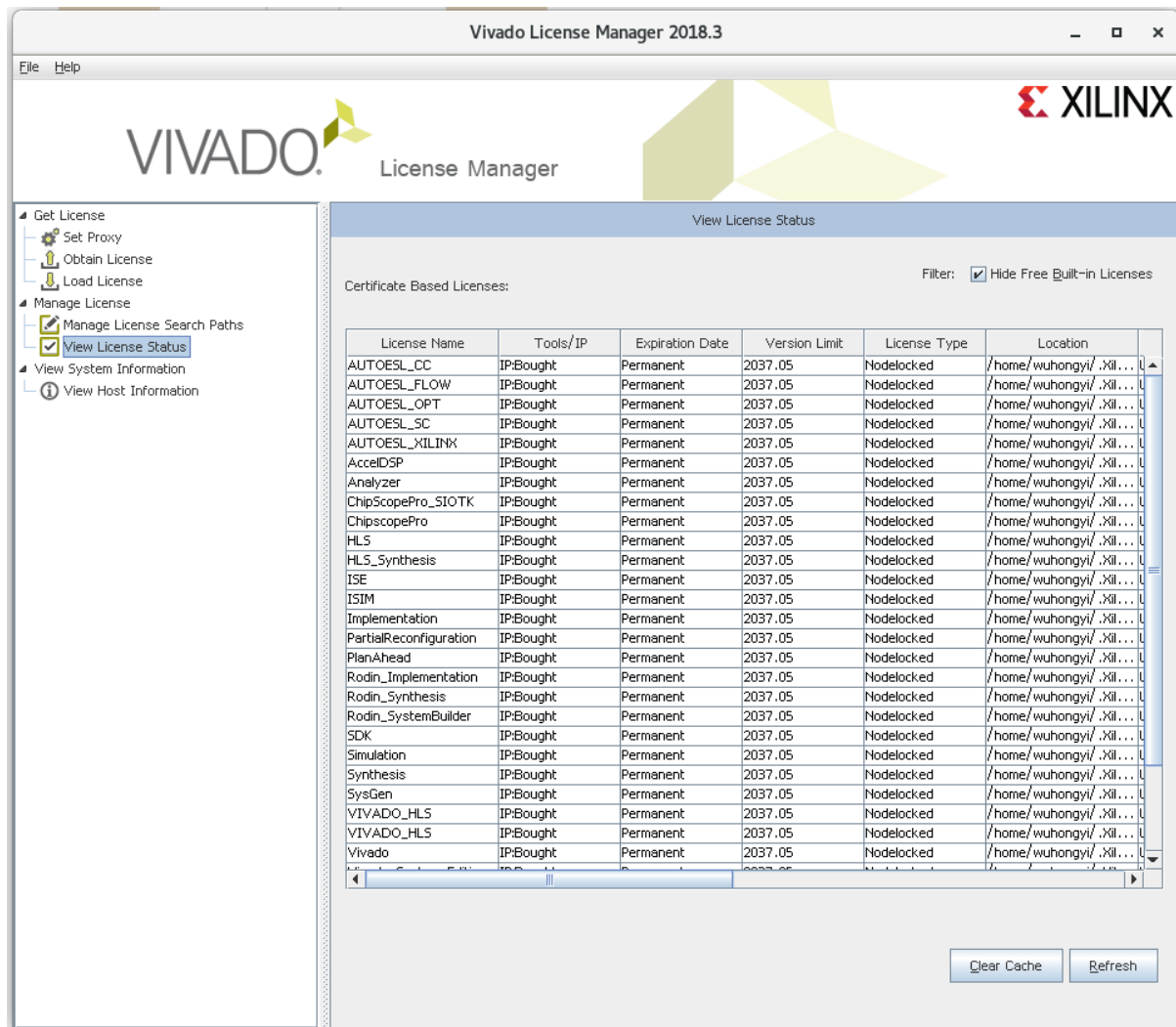
Copy the “vivadoLicence.lic” file to the installation directory, here is “/home/wuhongyi/Xilinx”

After the installation is complete, the following interface will pop up



Click on the “Load License” in the upper left and select our “vivadoLicence.lic” file

Then click “View License Status” in the upper left to view the authorized IP core



5.2 Compile

When you open it for the first time, you need to clear the P16_MZTIO_FW_0p01/build folder.

- Open Vivado. Use Tools > Run Tcl Script to run project generating script `.../verilog/xillydemo-vivado.tcl`. The resulting project file is in `...verilogvivado`
- There have been cases where the script crashes Vivado, and then the compile has ~100 pin property critical warnings. In such cases, start over.
- Compile demo project (generate bitstream). Ignore warnings and critical warnings.
- Check `build/xillydemo.runs/impl_1/xillydemo.bit`

5.3 In system debug

Is possible???

About multiplicity output in RJ45 in PKU firmware

- when setting multiplicity==0, output high level
- when setting multiplicity>=1, the default output is low level, and it is high when triggered.

When the MSRB bit 6 is 1

- the synchronization indication signal can be obtained
- have the DPMFULL output information
- have back plane FT, VT information

6.1 online monitor

After modifying the parameter configuration file `settings.ini`, you need to run the following program to modify the register settings.

```
./progfippi
```

It should be noted that the program is not allowed to be executed when DAQ running

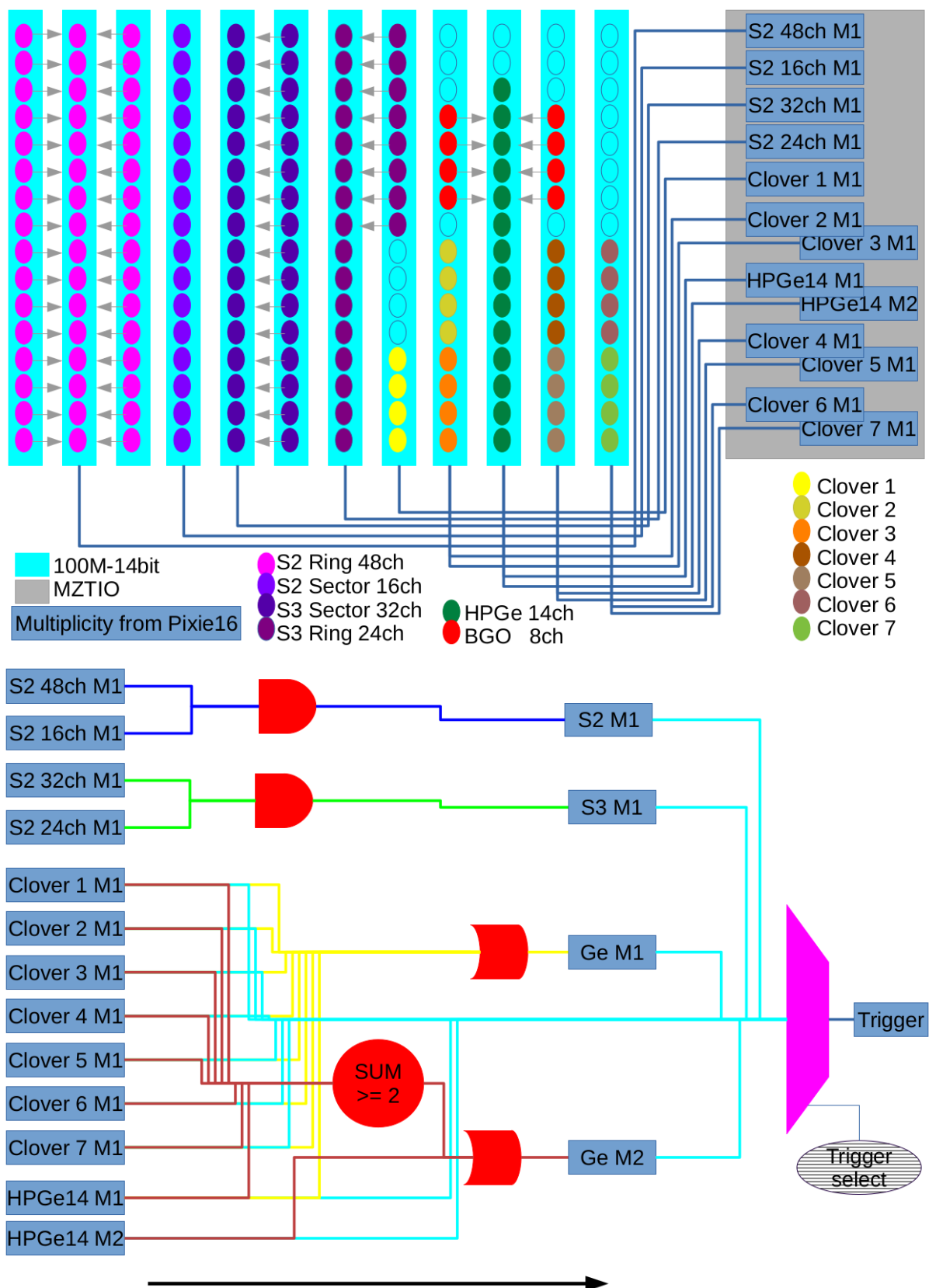
You can view the parameters settings in the web page, and the scaler counter and so on.

6.2 experiment mode

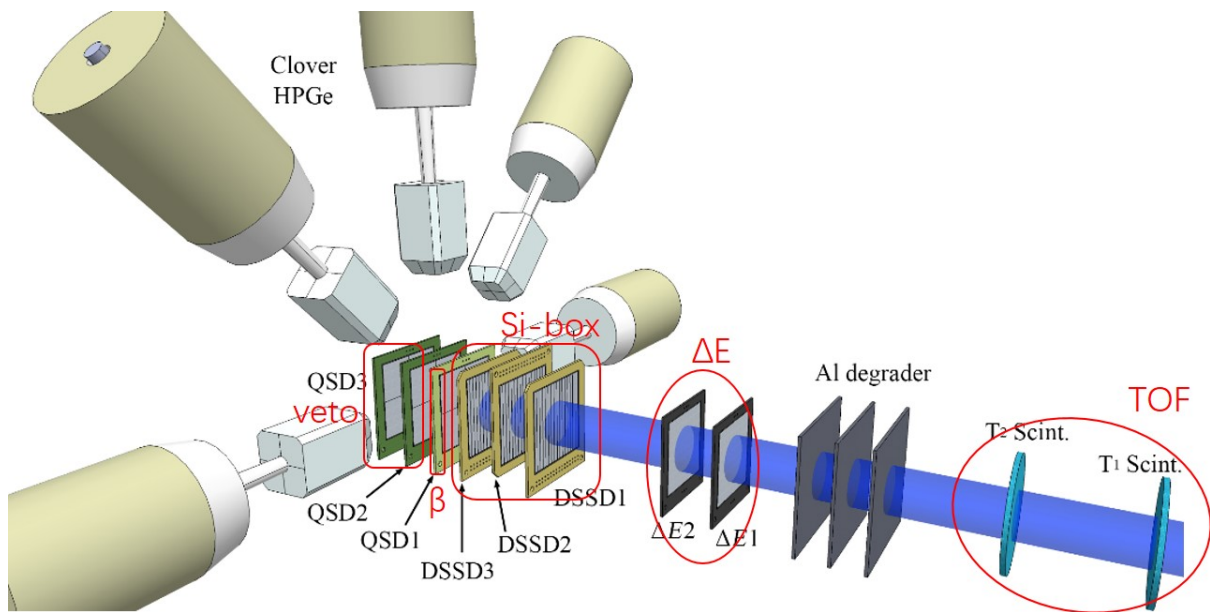
We will provide a common combination of firmware and software for the following four types of experiments.

6.2.1 in beam gamma

designing...



6.2.2 beta decay

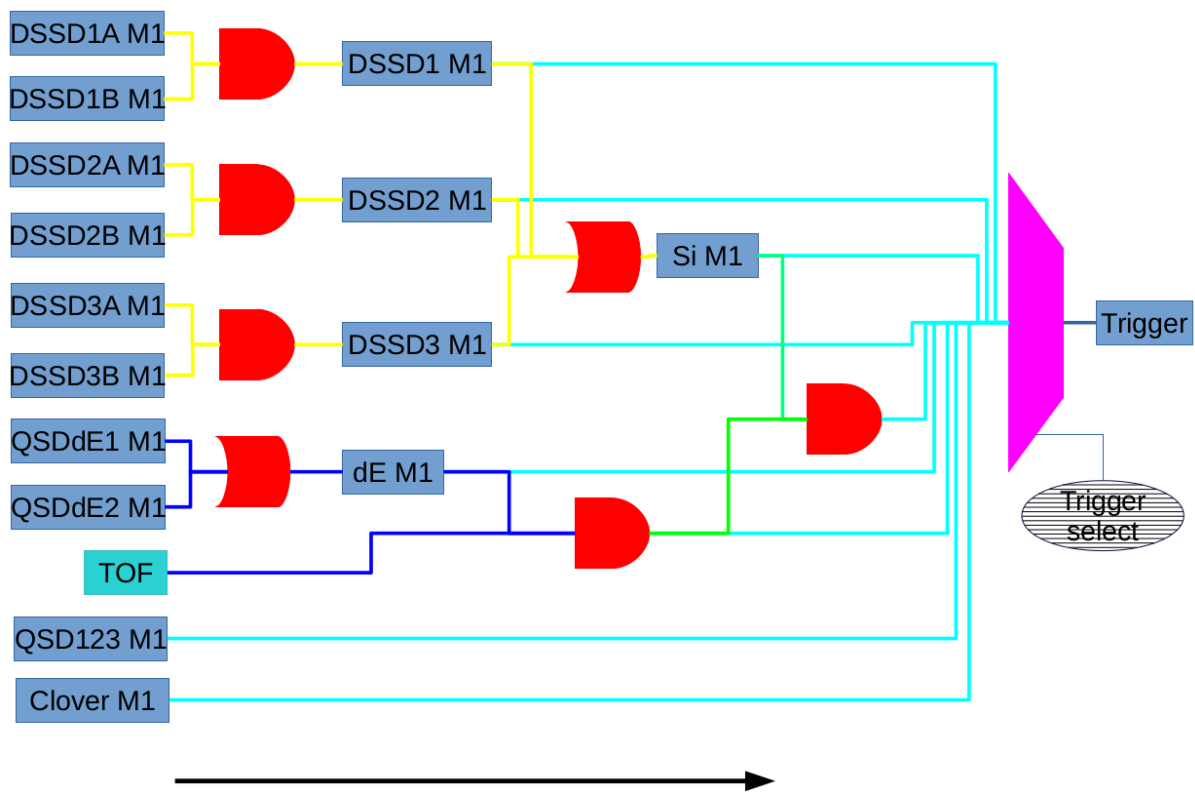
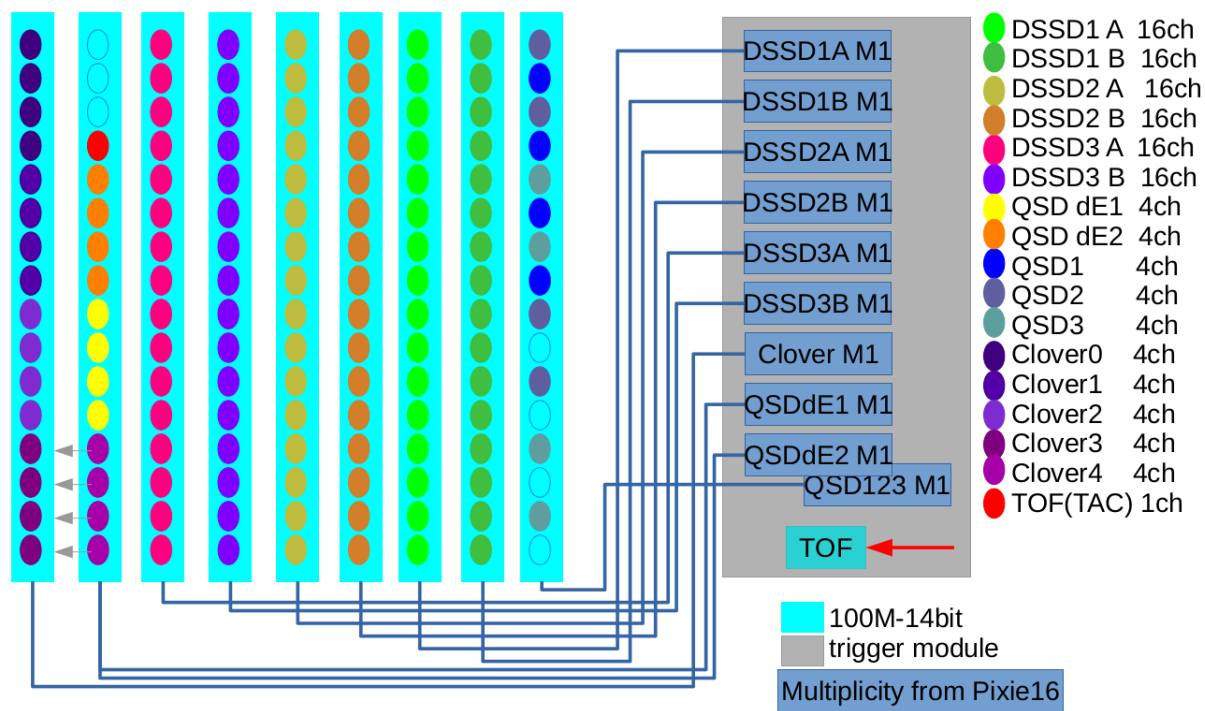


Listed below is the silicon detector information in the detection array:

- **QSDΔE1**
 - MICRON MSQ25, Junction 4, 50.0mm x 50.0mm, 309um
- **QSDΔE2**
 - CIAE Q300, Junction 4, 50.0mm x 50.0mm, 300um
- **DSSD1**
 - MICRON W1, Junction 16, Ohmic 16, 49.5mm x 49.5mm, 142um
- **DSSD2**
 - MICRON W1, Junction 16, Ohmic 16, 49.5mm x 49.5mm, 142um
- **DSSD3**
 - MICRON W1, Junction 16, Ohmic 16, 49.5mm x 49.5mm, 142um
- **QSD1**
 - MICRON MSQ25, Junction 4, 50.0mm x 50.0mm, 1546um
- **QSD2**
 - CIAE Q300, Junction 4, 50.0mm x 50.0mm, 300um
- **QSD3**
 - CIAE Q300, Junction 4, 50.0mm x 50.0mm, 300um

The signals of the plastic scintillator T1 and T2 are converted into pulse amplitude information by TAC, which can be collected using 100MSPS module.

designing...

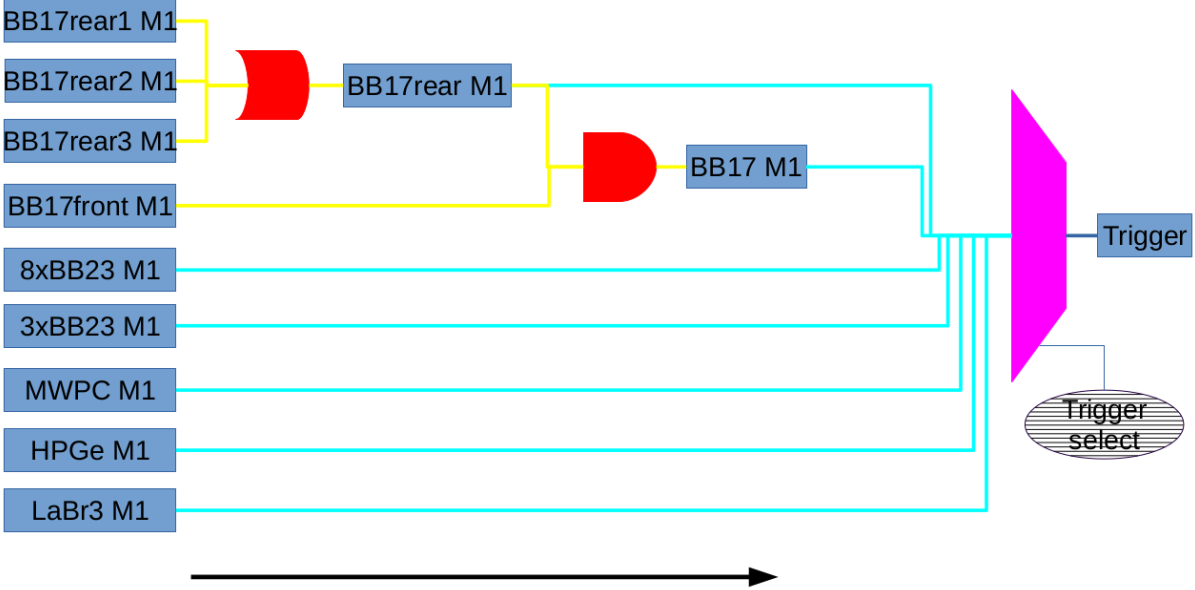
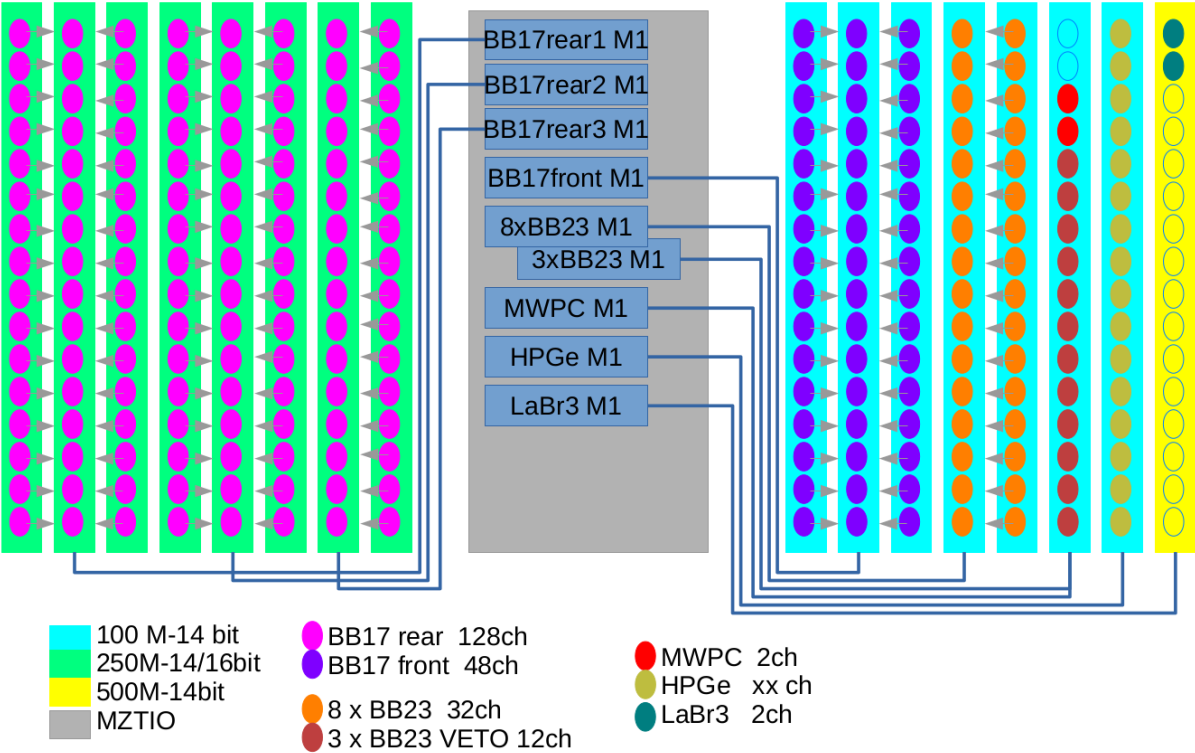


6.2.3 nuclear reaction

designing...

6.2.4 Super heavy nucleus

designing...



7.1 PS code

```
docs      #PKU MZTIO GUIDES
static    # css js
webops

Pixie16_MZTrigIO_Manual.pdf

MZTIOCommon.c
MZTIOCommon.h
MZTIODefs.h
clockprog.c
progfippi.cc
settings.ini
status.c
status.cgi
makefile

pkulogo100.jpg
why.jpg
webopspasswords
index.html
log.html
status.html
support.html
```

7.2 PL code

7.2.1 downscale

```
module downscale
(
```

(下页继续)

(续上页)

```
din,
dout,
down,
clk
);

parameter DATA_W = 16;
input [DATA_W-1:0] down;
input din;
output dout;
reg dout;
input clk;
endmodule
```

7.2.2 scaler

```
module scaler
(
    din,
    dout ,
    endcount,
    clk
);

parameter DATA_W = 32;
output [DATA_W-1:0] dout;
reg [DATA_W-1:0] dout;

input din;
input endcount;
input clk;
endmodule
```

7.2.3 signaldelay512

```
module signaldelay512
(
    din,
    dout,
    delay,
    clk
);

output dout;
reg dout;
input [9:0] delay;
input din;
input clk;
endmodule
```

7.2.4 signalextend512

```
module signalextend512
(
    din,
```

(下页继续)

(续上页)

```

dout,
extend,
clk
);

input din;
output dout;
reg      dout;
input [9:0] extend;
input clk;
endmodule

```

7.2.5 IP core

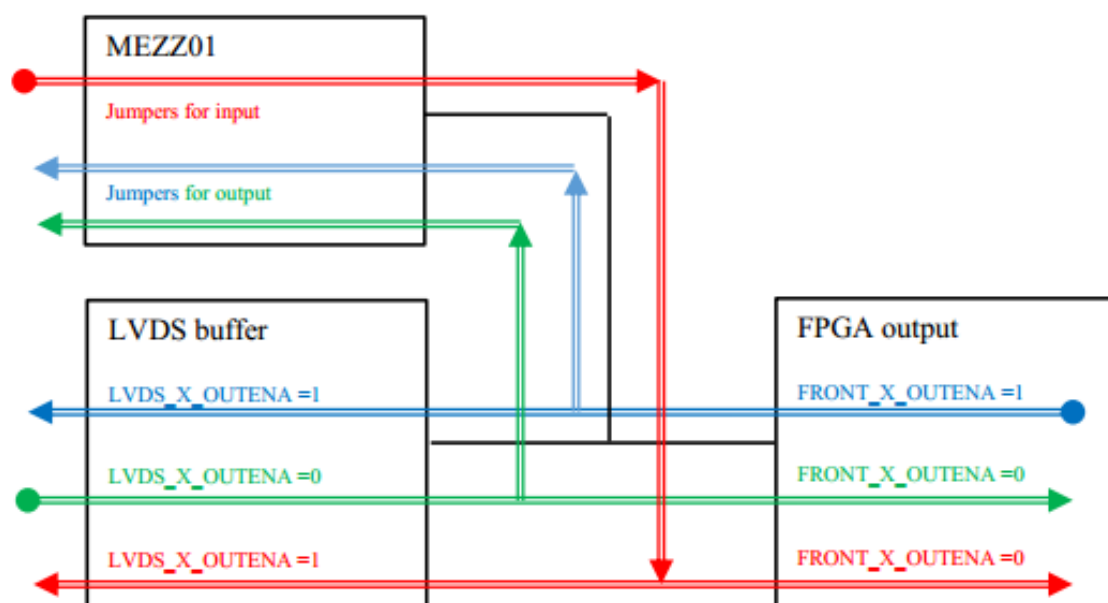
FIFO

```

module fifo_delay512(clk, srst, din, wr_en, rd_en, dout, full, empty,
data_count)
/* synthesis syn_black_box black_box_pad_pin="clk,srst,din[0:0],wr_en,rd_en,
↪dout[0:0],full,empty,data_count[9:0]" */;
input clk;
input srst;
input [0:0]din;
input wr_en;
input rd_en;
output [0:0]dout;
output full;
output empty;
output [9:0]data_count;
endmodule

```

7.3 xillydemo



```
// The configuration of the FrontIO_A/B/C is completely flexible. For example, if
→you connect the RJ-45 of a Pixie-16 to FrontI/O A 0-3 (the upper RJ-45 on the
→trigger board), signals will connect
// FO5 - Front I/O A 3      FrontIO_Aena==0
// FO1 - Front I/O A 0      FrontIO_Aena==0
// FI5 - Front I/O A 1      FrontIO_Aena==1
// FI1 - Front I/O A 2      FrontIO_Aena==1

// F0  5p/5n  synchronization status / multiplicity result channel 0(pku firmware)
// FO  1p/1n  not used / multiplicity result channel 1(pku firmware)
// FI  5p/5n  external fast trigger
// FI  1p/1n  external validation trigger

// FrontIO_Aout [3] [0] [7] [4] [11] [8] [15] [12]
// FrontIO_Ain  [1] [2] [5] [6] [9] [10] [13] [14]
```

• FRONT_X_OUTENA

- == 1 表示从 MZ 往前面板驱动输出，代码里面操作 out
- == 0 表示从前面板往 MZ 驱动输入，代码里面操作 in

• LVDS_X_OUTTENA

- == 1 表示驱动网口向外输出
- == 0 表示驱动网口向里输入

如果 MEZZ01 开启输入模式，则必须设置 FRONT_X_OUTENA==0 && LVDS_X_OUTTENA==1，其余模式下，MEZZ01 跳针全部设置成输出模式，此时网口可用于输入或者输出模式。

当前，在前面板 C 口配置一个 MEZZ01 模块，其中前四通道设置为信号输入，分别连接 [1]/[2]/[5]/[6]，后四个通道设置为信号输出，分别连接 [9]/[10]/[13]/[14]。该配置模式下，C 口对应的四个网口仍然可用于多重性的输入，此时参数 FrontIO = 0x6600, LVDSIO = 0x6666。如果不使用 MEZZ01 模块，只连接网口与 P16 模块，则参数 FrontIO/LVDSIO 均设置为 0x6666。

