MZTIO

发布 *0.0*

Hongyi Wu(吴鸿毅)

2019 年 07 月 20 日

Contents:

CHAPTER 1

README

If you need firmware, please contact Hongyi Wu(wuhongyi@qq.com)

如果你需要固件，请联系吴鸿毅 (wuhongyi@qq.com)

https://support.xia.com/default.asp?W372

The Pixie-16 MZ-TrigIO is designed to route signals from the backplane (rear connectors) to the front panel (front connectors) and make logical combinations between them in FPGA fabric. It has the following features and capabilities:

- Ethernet programmable trigger/coincidence control module for the Pixie-16
- 48+ Pixie-16 backplane trigger connections to local Zynq processor
- 48 front panel LVDS connections to local Zynq processor
- MicroZed Zynq processor with embedded Linux, acting as a standalone PC with built-in SD card drive, USB host, 10/100 Ethernet, webserver, etc
- 1588 PTP and SyncE clock synchronization
- Open source user access to software and firmware
- Use as standalone desktop unit or in 6U PXI chassis
- Custom I/O standards via daughtercards

1.1 Safety

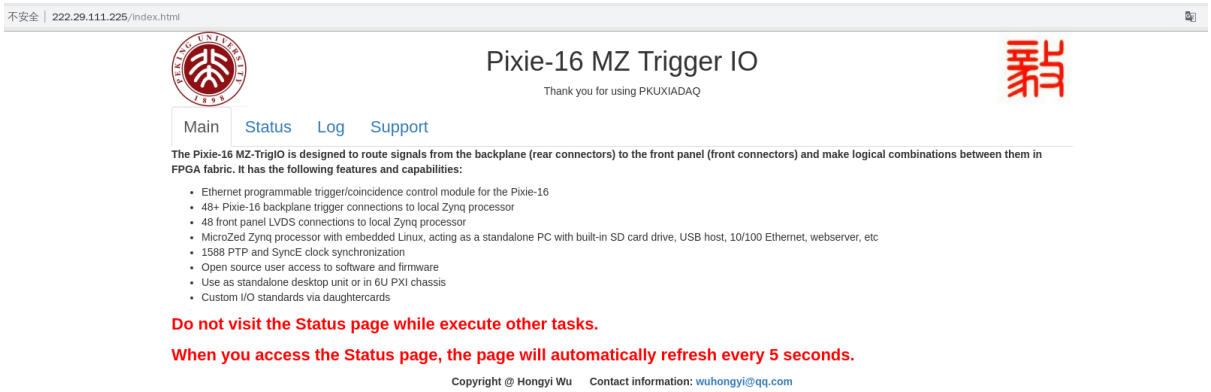
Please take a moment to review these safety precautions. They are provided both for your protection and to prevent damage to the Pixie module and connected equipment. This safety information applies to all operators and service personnel.

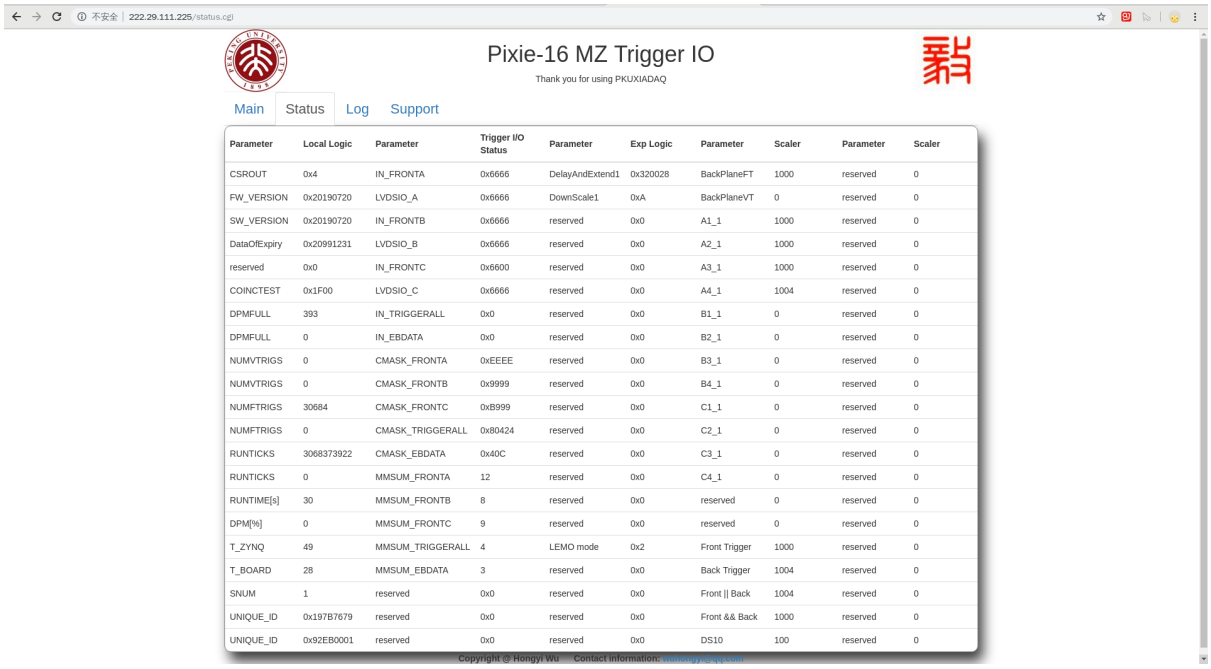
- Power Source
  - The Pixie-16 MZ-TrigIO module is powered through an AC/DC wall adapter or a PXI backplane. The default adapter has a variety of AC plug attachments for different localities.
  - Please remember to shut down the Linux OS before removing the power plug from the Pixie-16 MZ-TrigIO or powering down the PXI chassis.

- User Adjustments/Disassembly
  - To avoid personal injury, and/or damage, always disconnect power before accessing the module ' s interior. There are a few jumpers related to clocking on the board that experienced users may want to use.
- Voltage Ratings
  - Signals on the inputs and outputs must not exceed ± 3.3V. Please review the pinout in the appendix before making any connections.
- Daughtercards
  - Daughtercards can be used as alternatives to front panel and rear inputs, which requires caution to avoid conflicts from FPGA outputs and standard connector inputs.
- Servicing and Cleaning
  - To avoid personal injury, and/or damage to the Pixie module or connected equipment, do not attempt to repair or clean the inside of these units.
- Linux Passwords
  - The Pixie-16 MZ-TrigIO Linux OS comes with default user IDs and passwords for 1) SSH login, 2) SMB file sharing, and 3) Web Operations as described below. Users should immediately change these passwords, especially when the Pixie-16 MZ-TrigIO is connected to external networks. Don ' t let hackers take over your Pixie-16 MZ-TrigIO!
- Linux Backup
  - The Pixie-16 MZ-TrigIO Linux OS is stored on a removable SD card. SD cards ' file systems can become corrupted, which would crash the Linux system and make the Pixie-16 MZ-TrigIO unable to operate. Therefore periodic backup of the SD card is recommended, for example using Win32DiskImager. (Byte for byte copy is required).
  - Note that all Linux passwords are stored on the SD card.

CHAPTER 2

WEB Control GUI





CHAPTER 3

remote control

3.1 minicom

将 USB 线连接电脑，获取系统 IP

在 linux 中可以采用串口通讯软件 minicom

```
minicom -s
```

```
+-----[configuration]------+
| Filenames and paths       |
| File transfer protocols   |
| Serial port setup         |
| Modem and dialing         |
| Screen and keyboard       |
| Save setup as dfl         |
| Save setup as..           |
| Exit                      |
| Exit from Minicom         |
+---------------------------+
```

- 进入 Serial port setup，修改 Serial Device 为 /dev/ttyUSB0。Bps/Par/Bits 采用默认的 115200 8N1，底部两个选项均为 NO
- 进入 Modem and dialing ，将 A、B、K 项内容删除
- 然后选择 Save setup as dfl 保存设置
- 最后选择 Exit 退出配置模式，进入控制模式

user：root password: xia17pxn

密码采用默认的，方便使用者都能登陆

```
ssh -Y root@222.29.111.80
```

3.2 静态 IP 设置

因为 Ubuntu18.04 采用的是 netplan 来管理 network。所以可以在 /etc/netplan/ 目录下创建一个以 yaml 结尾的文件。比如 01-netplan.yaml 文件。

然后在此文件下写入以下配置：

```
network:
  version: 2
  renderer: networkd
  ethernets:
    enp3s0:
      dhcp4: no
      addresses: [192.168.1.110/24]
      gateway4:  192.168.1.1
      nameservers:
        addresses: [8.8.8.8, 114.114.114.114]
```

特别要注意的是这里的每一行的空格一定要有的，否则会报错误而设置失败！

```
network:
  version: 2
  renderer: networkd
  ethernets:
    eth0:
      addresses: [10.10.6.33/24]
      gateway4: 10.10.6.10
      dhcp4: no
```

以上参数为 CIAE 实验使用的配置。

最后使用 `sudo netplan apply` 来重启网络服务就可以了。使用 `ip a` 查看你的静态 IP 是否设置成功了！

CHAPTER 4

ubuntu

4.1 基本配置

4.1.1 ubuntu 18

如果操作系统是当前最新版本，则不需要进行额外的源配置。

如果要安装 CERN ROOT，则在 /etc/apt/sources.list 中添加以下行

```
deb http://ports.ubuntu.com/ xenial main universe multiverse
```

4.1.2 ubuntu 12

如果操作系统版本是之前的老版本，则需要按照以下进行源的修改配置。

编辑源列表文件

```
vim /etc/apt/sources.list
```

修改为

```
deb http://old-releases.ubuntu.com/ubuntu vivid main restricted universe multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-security main restricted universe␣
↪multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-updates main restricted universe␣
↪multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-proposed main restricted universe␣
↪multiverse
deb http://old-releases.ubuntu.com/ubuntu vivid-backports main restricted universe␣
↪multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid main restricted universe␣
↪multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid-security main restricted␣
↪universe multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid-updates main restricted␣
↪universe multiverse
deb-src http://old-releases.ubuntu.com/ubuntu vivid-proposed main restricted␣
↪universe multiverse
```

(下页继续)

(续上页)

```
deb-src http://old-releases.ubuntu.com/ubuntu vivid-backports main restricted␣
↪universe multiverse

deb http://mirrors.ustc.edu.cn/ubuntu/ vivid main universe
deb-src http://mirrors.ustc.edu.cn/ubuntu/ vivid main universe
```

4.1.3 软件升级

运行

```
apt-get update
```

```
# 安装 firefox
apt-get install firefox
# 安装 emacs
apt-get install emacs

# ROOT 依赖库文件
apt-get install cmake
apt-get install libx11-dev
apt-get install libxpm-dev
apt-get install libxft-dev
apt-get install libxext-dev
apt-get install gfortran
apt-get install libssl-dev
apt-get install xlibmesa-glu-dev
apt-get install libglew1.5-dev
apt-get install libftgl-dev
apt-get install libmysqlclient-dev
apt-get install libfftw3-dev
apt-get install libcfitsio-dev
apt-get install graphviz-dev
apt-get install libavahi-compat-libdnssd-dev
apt-get install libxml2-dev
apt-get install libkrb5-dev
apt-get install libgsl0-dev
apt-get install libqt4-dev
```

```
apt-get install root-system-bin
```

ubuntu 颜色配置，个人目录下放置颜色配置文件.dircolors，该文件在 readhat 系统中文件名为.dir_colors

---

4.2 恢复 SD 卡原始空间

为了加快镜像装载速度，实际上只格式化了 8/16G 左右的 SD 卡空间，我 16/32G 的 SD 卡还有 8/16G 多的空间都没用到，为了能够进行使用进行如下操作

fdisk /dev/mmcblk0 然后分别输入: d [ENTER],2 [ENTER],n[ENTER] [ENTER],[ENTER],[ENTER],[ENTER],w[ENTER]，若中间出现问题详细参考 Getting started with Xillinux for Zynq-7000 EPP ，然后重启 linux 开机后

resize2fs /dev/mmcblk0p2 并使用

df -h 查看最后追加的结果

4.3 update the boot files

To mount the SD card boot partition to a folder /mnt/sd, execute

```
mount /dev/mmcblk0p1 /mnt/sd
```

this is useful to update the boot files without removing the SD card. The Pixie-16 MZ-TrigIO has to be rebooted before the new boot files become effective.

So the precedure would be

- generate FW files on a desktop PC
- copy to shared Linux folder on the SD card (/var/www)
- mount boot partition mount /dev/mmcblk0p1 /mnt/sd (create /mnt/sd if not already there)
- copy files e.g. cp /var/www/xillydemo.bit /mnt/sd
- reboot or power cycle (reboot)

```
 scp xillydemo.bit root@222.29.111.157:~
```

4.4 /dev/mmcblk0p1

```
boot.bin  devicetree.dtb  uImage  xillydemo.bit
```

CHAPTER 5

Vivado

首次打开时，需要清空 `P16_MZTIO_FW_0p01/build` 文件夹

- Open Vivado. Use Tools > Run Tcl Script to run project generating script …/verilog/xillydemo-vivado.tcl. The resulting project file is in …\verilog\vivado There have been cases where the script crashes Vivado, and then the compile has ~100 pin property critical warnings. In such cases, start over.
- Compile demo project (generate bitstream). Ignore warnings and critical warnings.
- Check build/xillydemo.runs/impl_1/xillydemo.bit

CHAPTER 6

experiment

- 当多重性为 0 时，输出高电平
- 当多重性大于等于 1 时，默认输出低电平，有触发时为高电平
- MSRB bit6 为 1 时，才能有同步指示信号，才能 DPM 的输出信息，才有 FT，VT 信息

6.1 在线监视

修改好参数配置文件 settings.ini

执行

```
progfippi
```

写入设置参数

需要注意的是，当获取采集时候，不允许执行该程序

在网页中即可查看参数设置情况，scale 计数情况

CHAPTER 7

程序说明

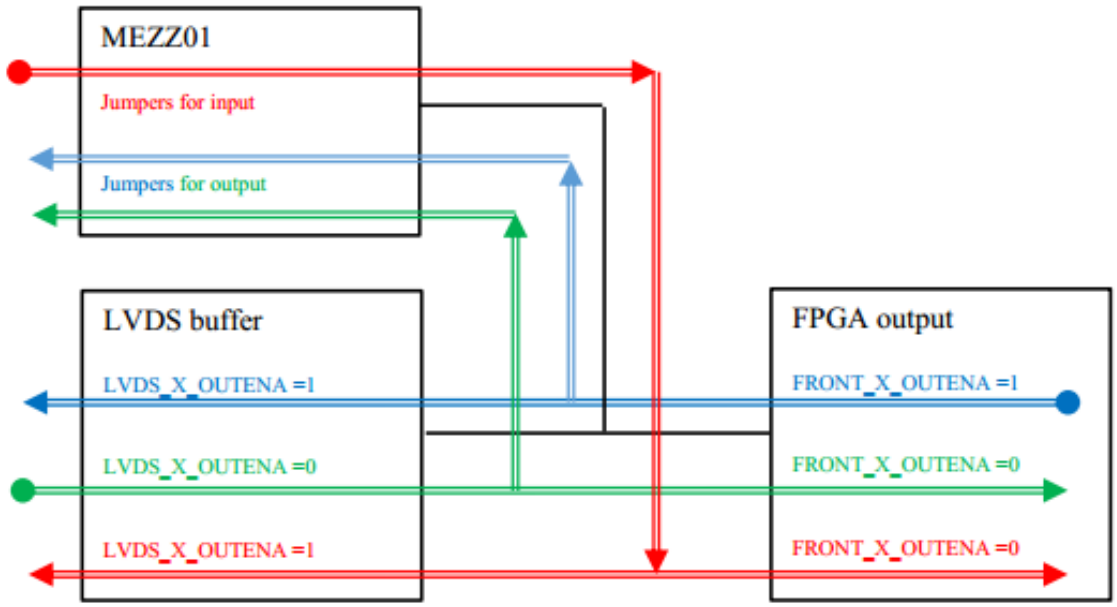
```
PixieNetCommon.c
PixieNetCommon.h
PixieNetConfig.cpp
PixieNetConfig.h
PixieNetDefs.h

makefile
cgistats.c
clockprog.c
monitordaq.c
progfippi.c
runstats.c
writeI2C.c

d3.v3.min.js
defaults.ini
settings.ini

Xia_LLC_web_header.jpg
dygraph-combined.js
index.html
plotly-latest.min.js
rspage.html
webopspasswords 存放网页密码
```

7.1 xillydemo



DB

```
   // The configuration of the FrontIO_A/B/C is completely flexible. For example,␣
↪if you connect the RJ-45 of a Pixie-16 to FrontI/O A 0-3 (the upper RJ-45 on the␣
↪trigger board), signals will connect
   // FO5 - Front I/O A 3      FrontIO_Aena==0
   // FO1 - Front I/O A 0      FrontIO_Aena==0
   // FI5 - Front I/O A 1      FrontIO_Aena==1
   // FI1 - Front I/O A 2      FrontIO_Aena==1

   // F0  5p/5n  synchronization status / multiplicity result channel 0(pku␣
↪firmware)
   // FO  1p/1n  not used / multiplicity result channel 1(pku firmware)
   // FI  5p/5n  external fast trigger
   // FI  1p/1n  external validation trigger

   // FrontIO_Aout [3] [0]  [7] [4]  [11] [8]  [15] [12]
   // FrontIO_Ain  [1] [2]  [5] [6]  [9] [10]  [13] [14]
```

- FRONT_X_OUTENA
  - == 1 表示从 MZ 往前面板驱动输出，代码里面操作 out
  - == 0 表示从前面板往 MZ 驱动输入，代码里面操作 in
- LVDS_X_OUTTENA
  - == 1 表示驱动网口向外输出
  - == 0 表示驱动网口向里输入

  如果 MEZZ01 开启输入模式，则必须设置 `FRONT_X_OUTENA==0 && LVDS_X_OUTTENA==1` ，其余模式下，MEZZ01 跳针全部设置成输出模式，此时网口可用于输入或者输出模式。

当前，在前面板 C 口配置一个 MEZZ01 模块，其中前四通道设置为信号输入，分别连接 [1]/[2]/[5]/[6]，后四个通道设置为信号输出，分别连接 [9]/[10]/[13]/[14]。该配置模式下，C 口对应的四个网口仍然可用于多重性的输出，此时参数 FrontIO = 0x6600, LVDSIO = 0x6666。如果不使用 MEZZ01 模块，只连接网口与 P16 模块，则参数 FrontIO/LVDSIO 均设置为 0x6666。