# 8-bit successive approximation register analog-to-digital-converter

\# Signal interface
uio_out[0] : When the output DFFs sample SAR output. If it does not come, then clock is too fast
uo_out[7:0] : Digital output. Two's complement
ui_in[0] : Enable ADC. Useful to measure current consumption
clk : Clock, ~ 4 MHz

TIE_L1    uio_out[7:1]

uio_out[7:0]

TIE_L

R3
1 * 0.3 / 0.3
R=0.047
res_generic_m4

R2[7:1]
1 * 0.3 / 0.3
R=0.047
res_generic_m4

uio_in[7:0]

TIE_L2    uio_oe[7:1]

R4
1 * 0.3 / 0.3
R=0.047
res_generic_m4

R1[7:1]
1 * 0.3 / 0.3
R=0.047
res_generic_m4

uio_oe[7:0]

VPWR

uio_oe[0]

DONE

uio_out[0]

AVDD
AVSS    Y
x5
SUNTR_TAPCELLB_CV
AVSS

AVDD
Y
x4
SUNTR_TIEH_CV

VGND

AVDD
A    Y
x3
SUNTR_BFX1_CV
AVSS

VPWR

## Power decoupling

c0  C2[8:0]
cap_mim_m3_1
C=6.617e-13    18 / 18
c1  MF=1

uo_out[7:0]

VPWR

ua[7:0]

ena

clk

rst_n

area=2.025e11
pj=1.8e6

d1
diode_pw2nd_05v5
diode
D2
d0

VGND

## Output capture

x2
CKS
ENABLE
CK_SAMPLE
CK_SAMPLE_BSSW
EN
D<7>
D<6>
D<5>
D<4>
D<3>
D<2>
D<1>
D<0>
DO<7>
DO<6>
DO<5>
DO<4>
DO<3>
DO<2>
DO<1>
DO<0>
DONE
AVDD
AVSS
TIE_L

SUNSAR_CAPT8B_CV

## SAR core

x1
SAR_IP
SAR_IN
SARN
SARP
DONE
D<7>
D<6>
D<5>
D<4>
D<3>
D<2>
D<1>
D<0>
EN
CK_SAMPLE
CK_SAMPLE_BSSW
VREF
AVDD
AVSS

SUNSAR_SAR8B_CV

clk
ui_in[0]
CK_SAMPLE
CK_SAMPLE_BSSW
EN
D<7>
D<6>
D<5>
D<4>
D<3>
D<2>
D<1>
D<0>

ua[1]
ua[0]
SARN
SARP
DONE
D<7>
D<6>
D<5>
D<4>
D<3>
D<2>
D<1>
D<0>
EN
CK_SAMPLE
CK_SAMPLE_BSSW
VPWR
VPWR
VGND

ui_in[0]

area=2.025e11
pj=1.8e6

d1
diode_pw2nd_05v5
diode
D3
d0

VGND

uo_out[7]
uo_out[6]
uo_out[5]
uo_out[4]
uo_out[3]
uo_out[2]
uo_out[1]
uo_out[0]
DONE
VPWR
VGND
TIE_L

d1
diode_pw2nd_05v5
diode
D1
d0
area=2.025e11
pj=1.8e6

VGND

ui_in[7:0]

VGND

| | |
|---|---|
| Designer | Carsten Wulff |
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Library/Cell    tt_um_TT06_SAR_wulffern