date: 2025-01-23

TFE4188 - Introduction to Lecture 2

ICs and ESD

Goal

Understand the **real-world** constraints on our IC

Understand why you must **always handle ESD** on an IC

The **real world** constrains our IC

What blocks must our IC include?

A BJT-based CMOS Temperature Sensor with Duty-cycle-modulated Output and ±0.54 °C (3-sigma) Inaccuracy from -40 °C to 125 °C.

Pin	Function	in/out	Value	Unit
VDD_3V3	analog supply	in	3.0	V
VDD_1V2	digital supply	in	1.2	V
VSS	ground	in	0	V
CLK_1V2	clock	in	20	MHz
RST_1V2	digital	out	0 or 1.2	V
I_C	bias	in	?	uA?
PHI1_1V2	digital	out	0 or 1.2	V
PHI2_1V2	digital	out	0 or 1.2	V
DCM_1V2	digital	out	0 or 1.2	V

course plan

One more thing

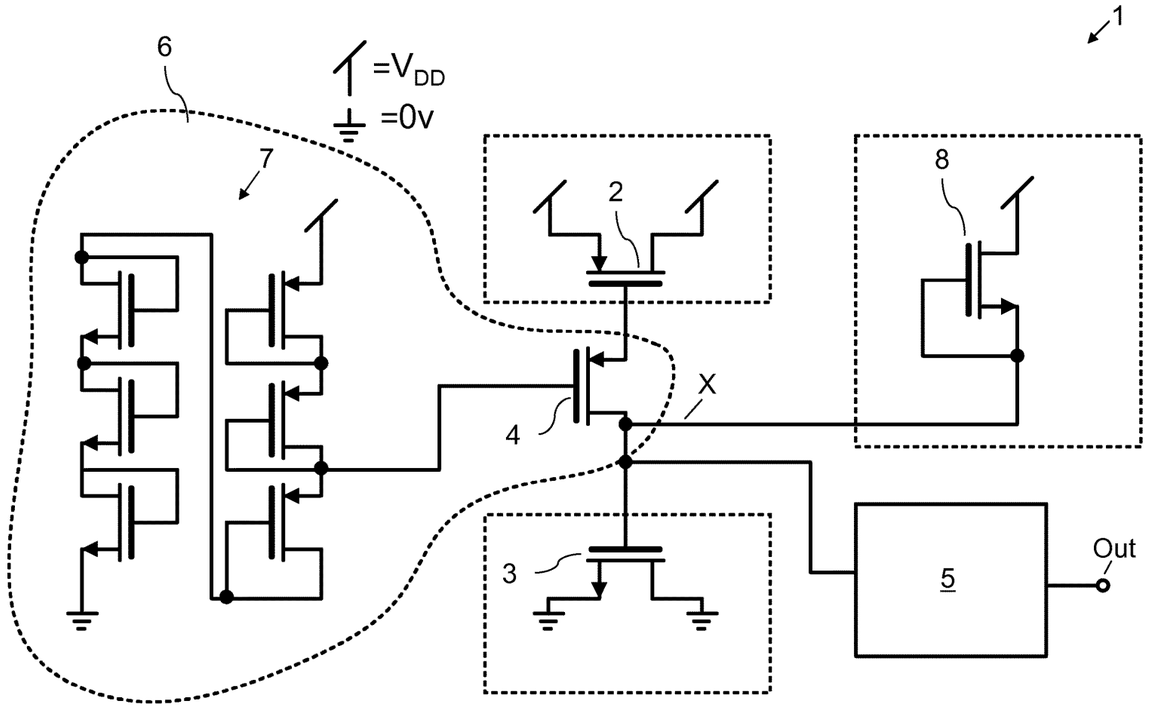


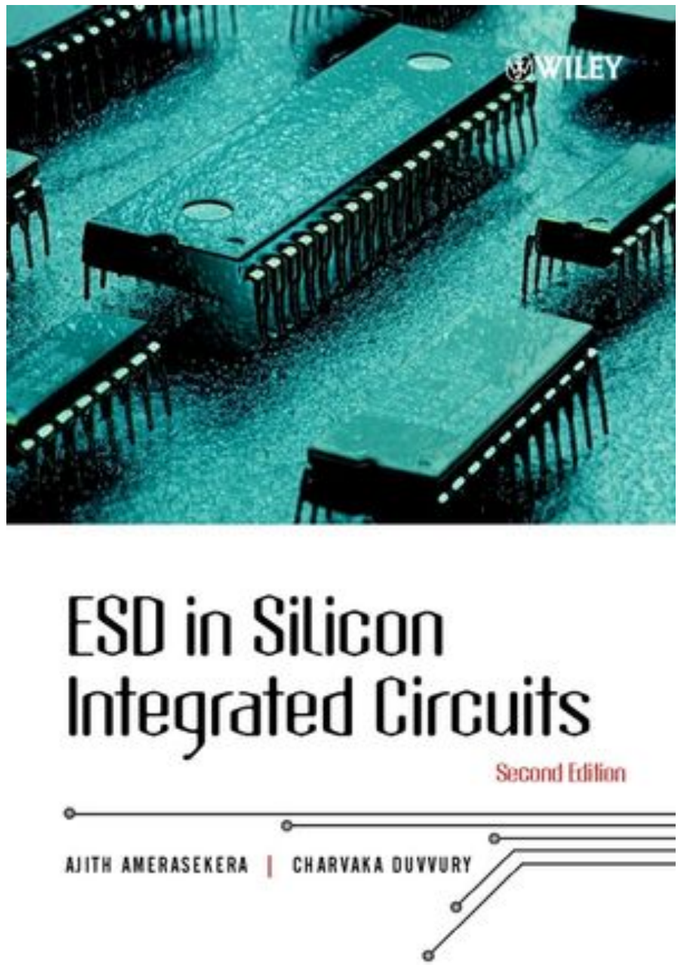
Figure 1

ESD

Electrostatic Discharge

If you make an IC, you must consider Electrostatic Discharge (ESD) Protection circuits

Standards for testing at JEDEC



When do ESD events occur?

Before/during PCB

Human body model (HBM)

Charged device model (CDM)

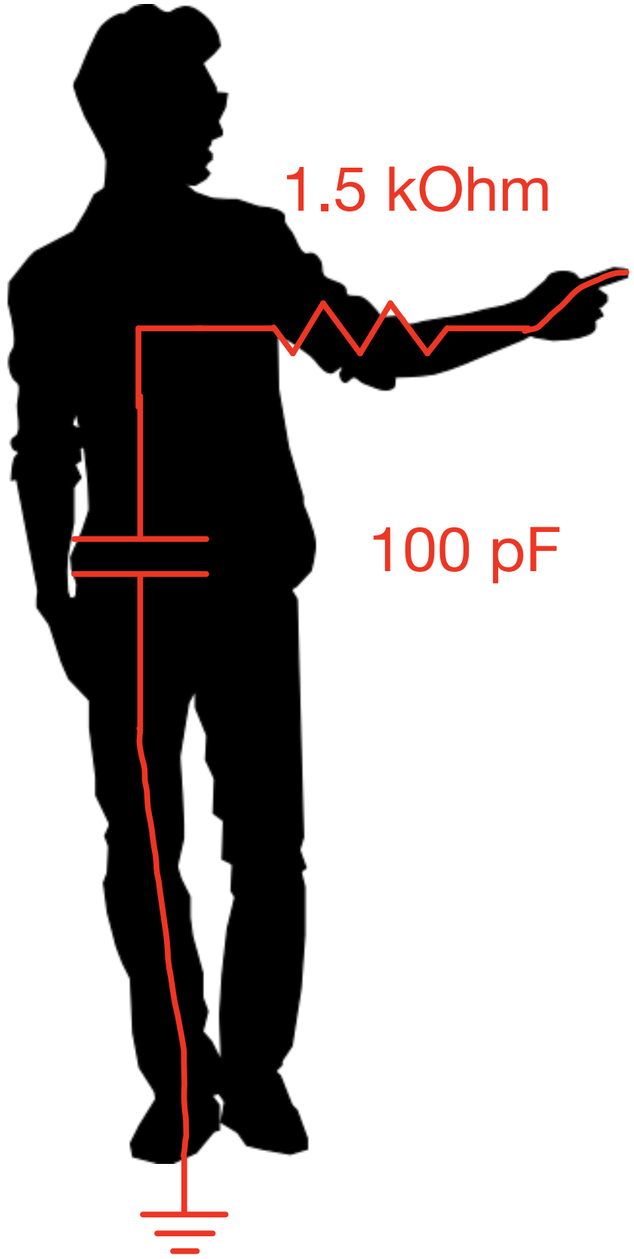
After PCB

Human body model (HBM)

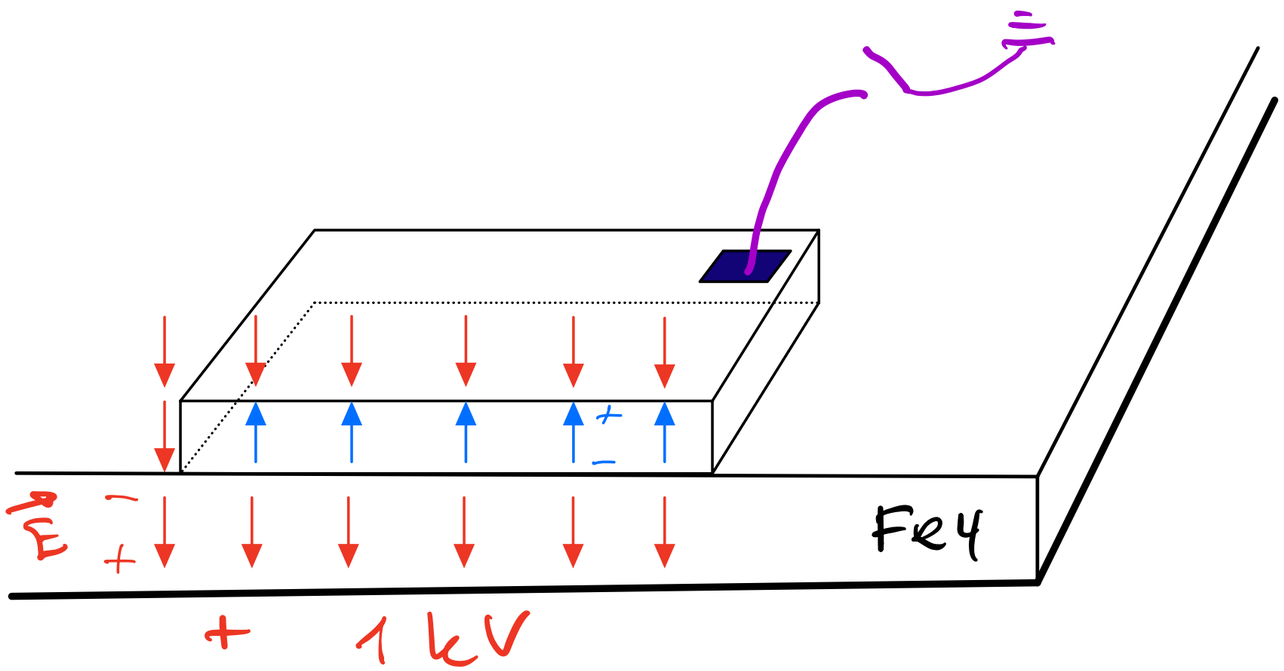
System level ESD

Human body model (HBM)

- Models a person touching a device with a finger
- **Long** duration (around 100 ns)
- Acts like a current source into a pin
- Can usually be handled in the I/O ring
- 4 kV HBM ESD is 2.67 A peak current

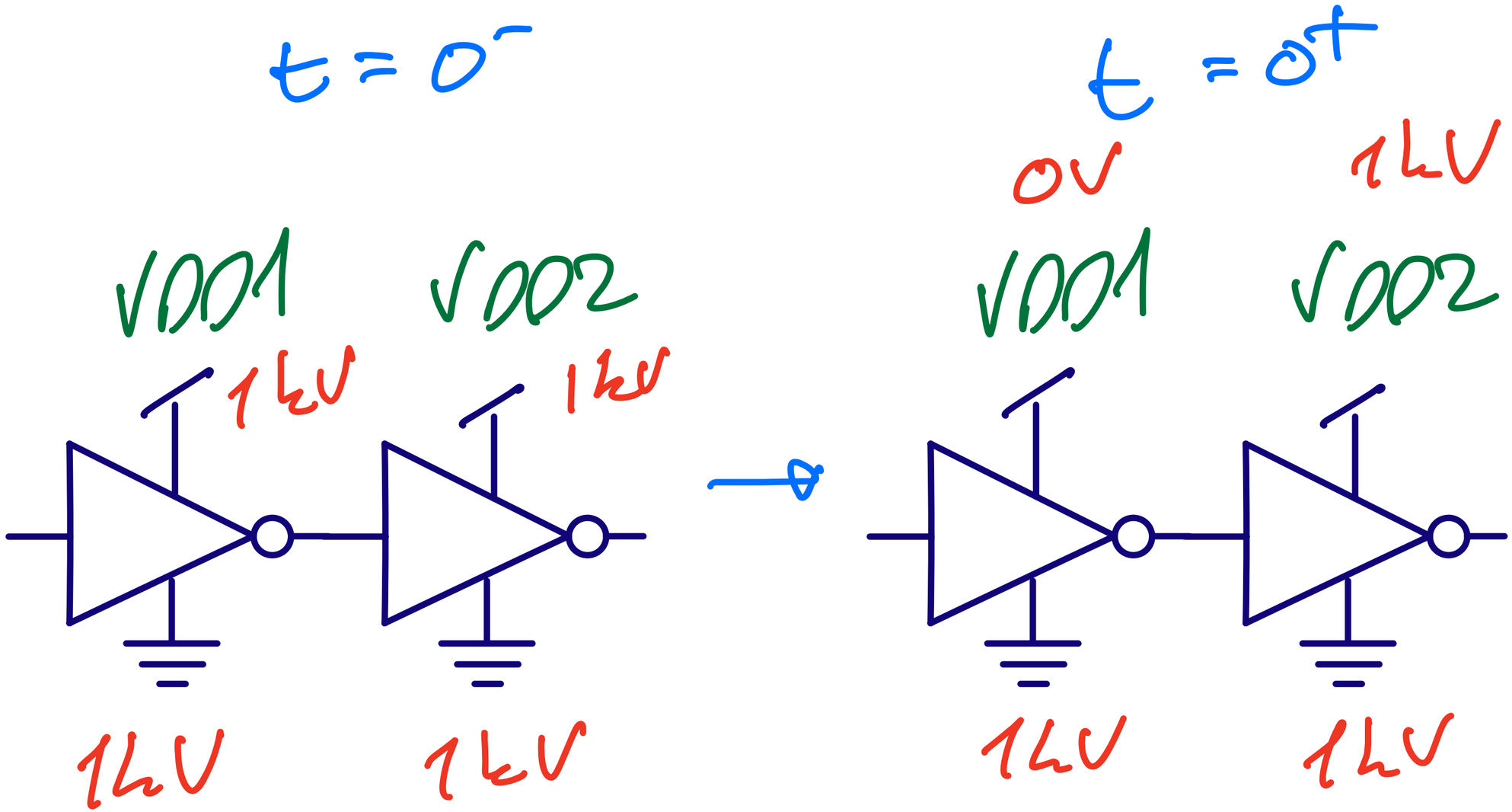


Charged device model (CDM)

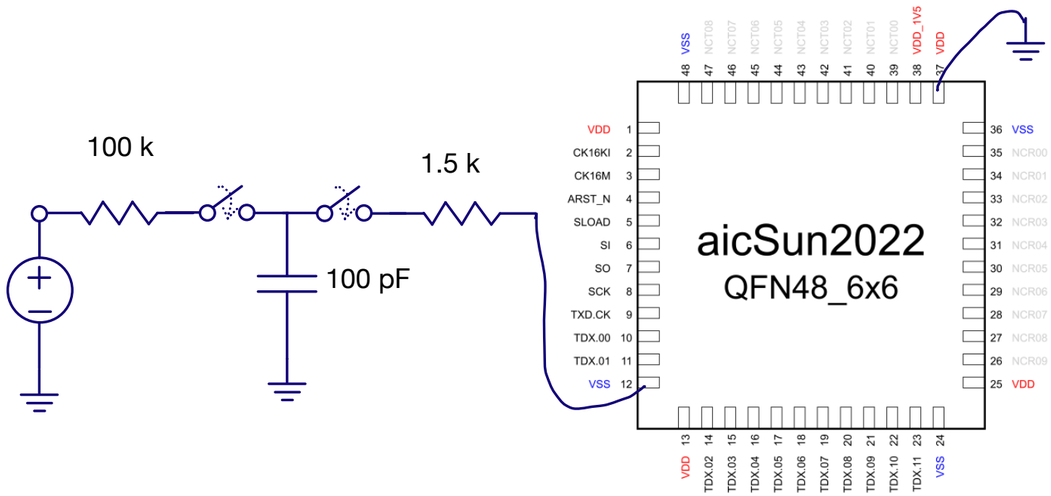


Assume there is an equal number of electrons and protons on the IC. According to Gauss' law

$$\oint_{\partial\Omega} \mathbf{E} \cdot d\mathbf{S} = \frac{1}{\epsilon_0} \iiint_V \rho \cdot dV$$


t = 0⁻
V001
V002
1kV
1kV
1kV
1kV
t = 0⁺
0V
1kV
V001
V002
1kV
1kV

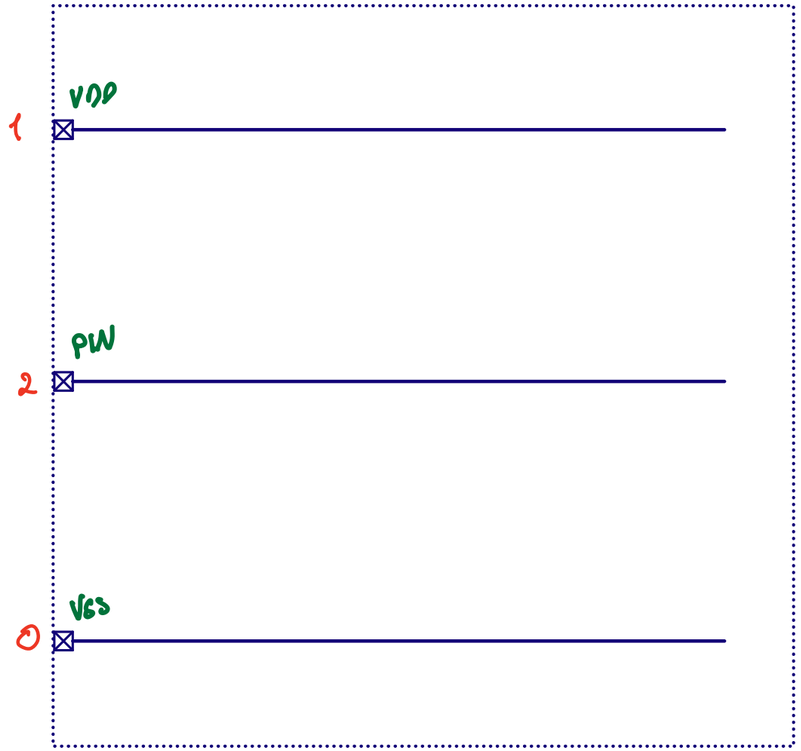
An HBM ESD zap example

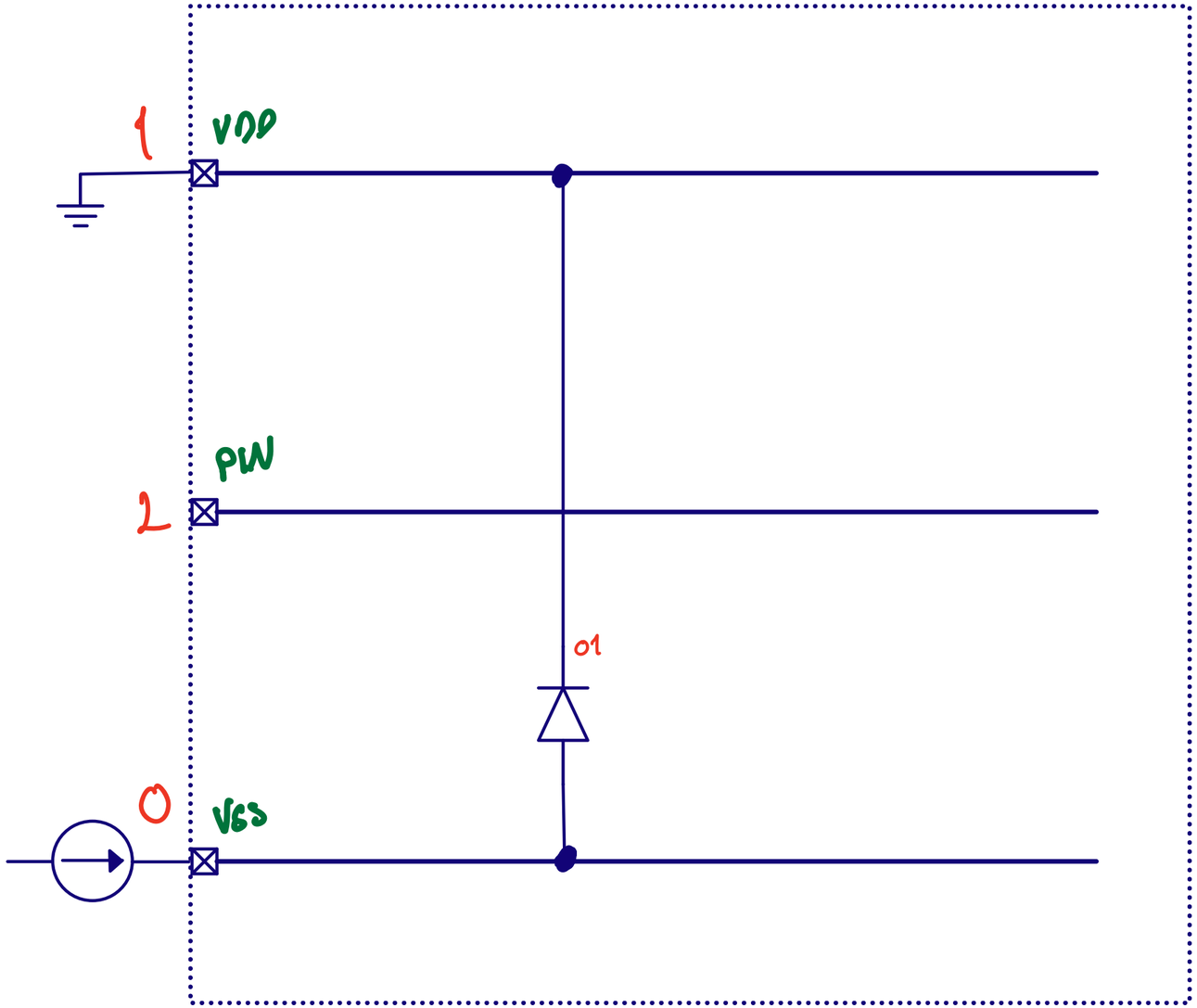


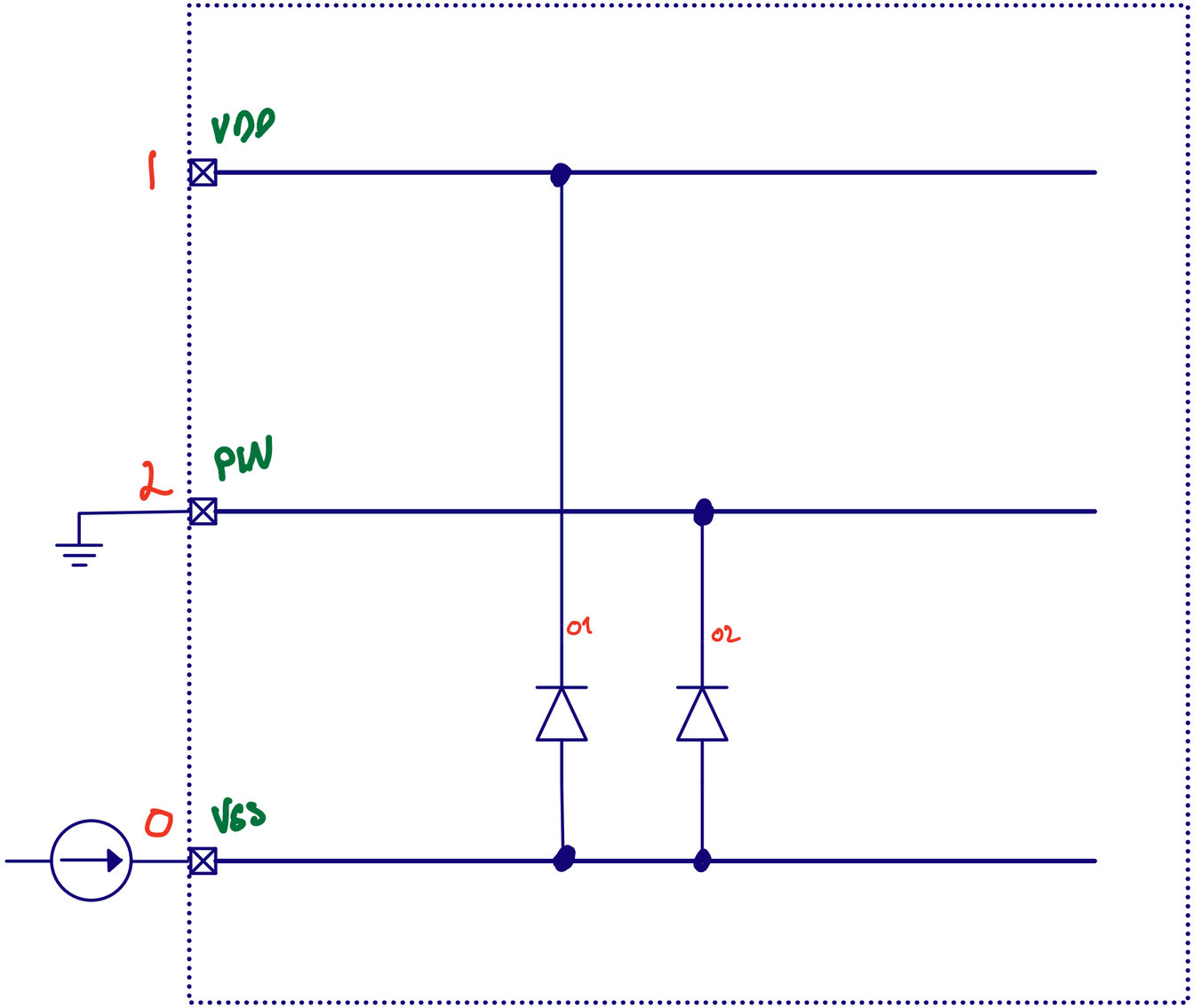
Imagine a ESD zap between VSS and VDD. How can we protect the device?

Permutations

0 → 1 VSS → VDD
1 → 0 VDD → VSS
0 → 2 VSS → PIN
2 → 0 PIN → VSS
1 → 2 VDD → PIN
2 → 1 PIN → VDD




1
VDD
PW
2
D1
0
VSS


VDD
1
PW
2
D1
D2
0
VSS

0 → 1 = 01

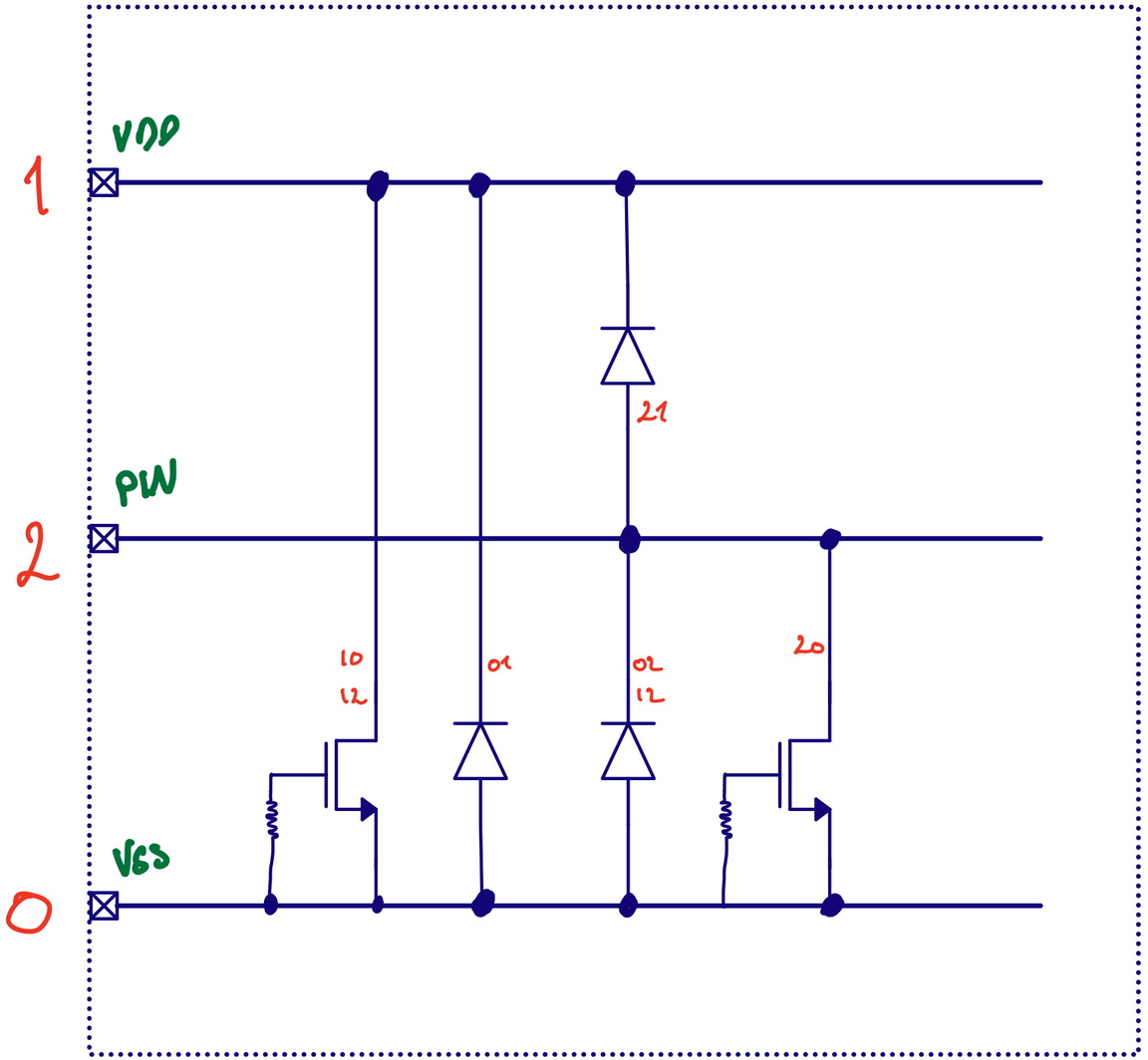
1 → 0 = 10

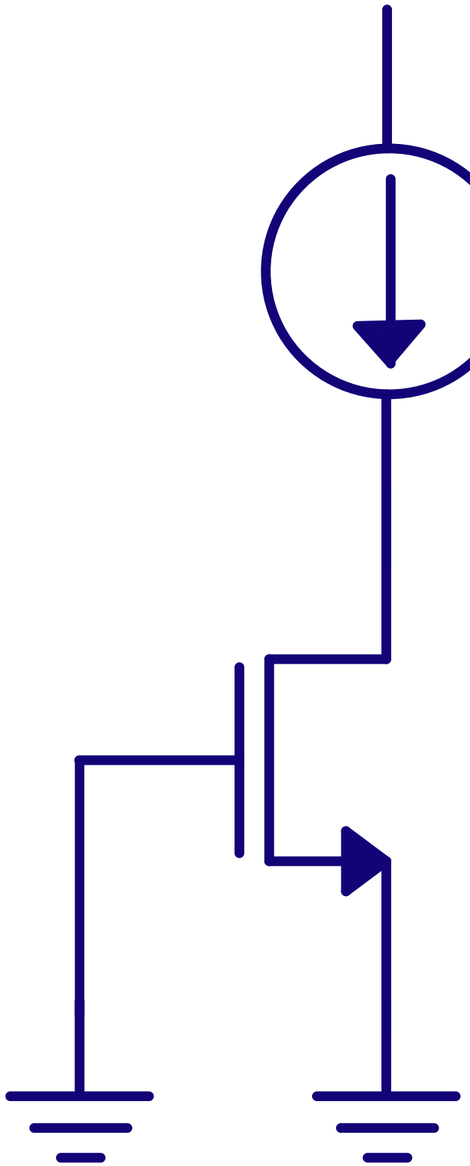
0 → 2 = 02

2 → 0 = 20

1 → 2 = 12

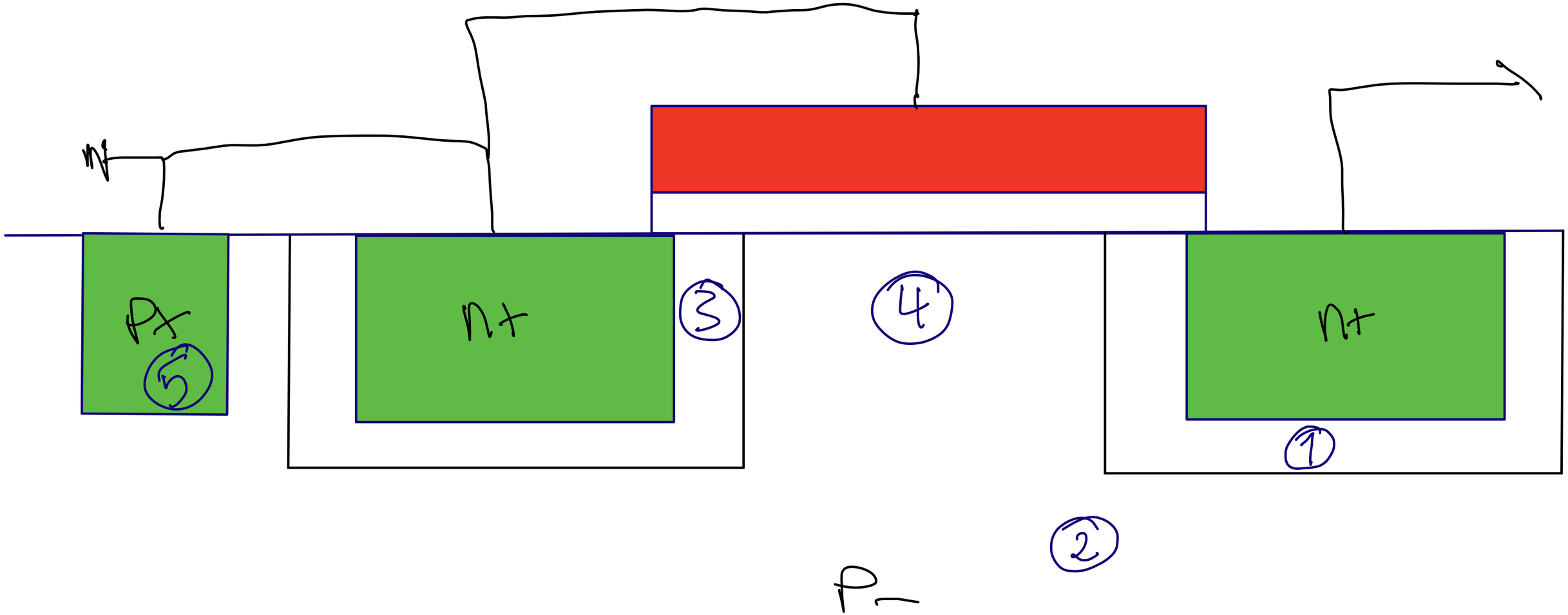
2 → 1 = 21





2,6A

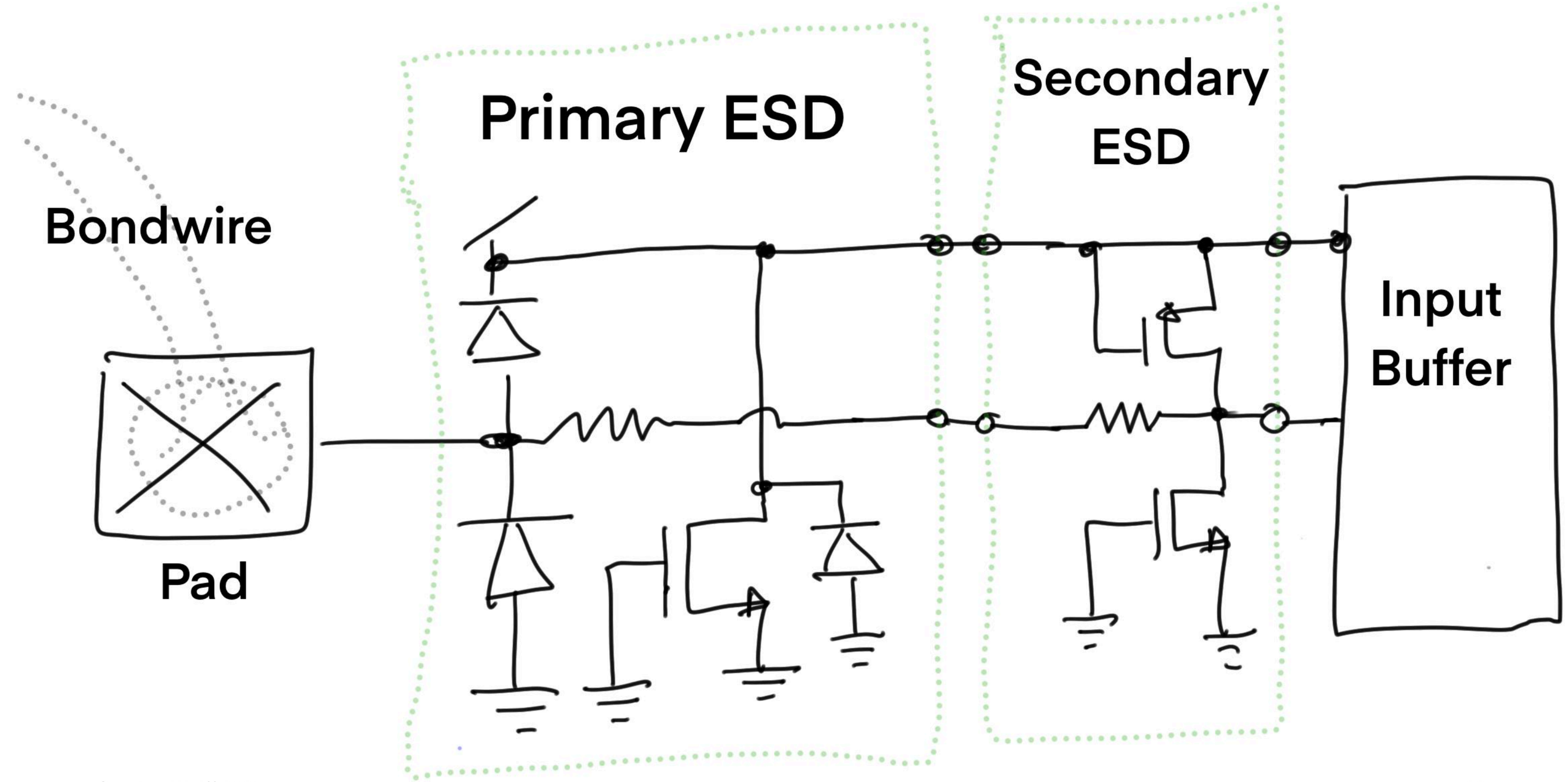
Why does this work?


n
p+
5
n+
3
4
n+
1
2
p−

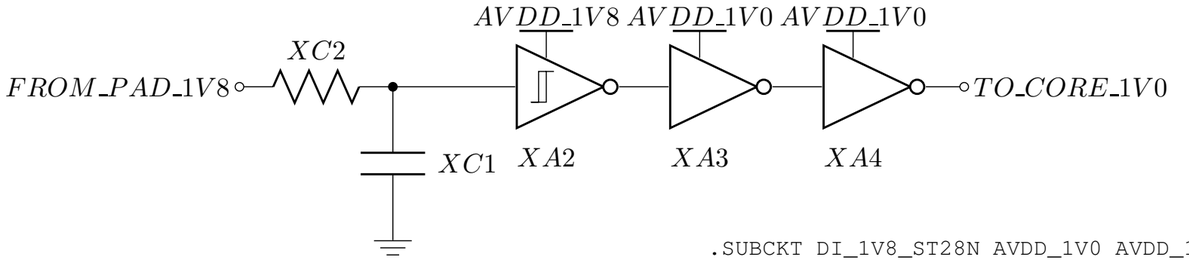
If you don't do the layout right

New Ballasting Layout Schemes to Improve ESD Robustness of I/O Buffers in Fully Silicided CMOS Process

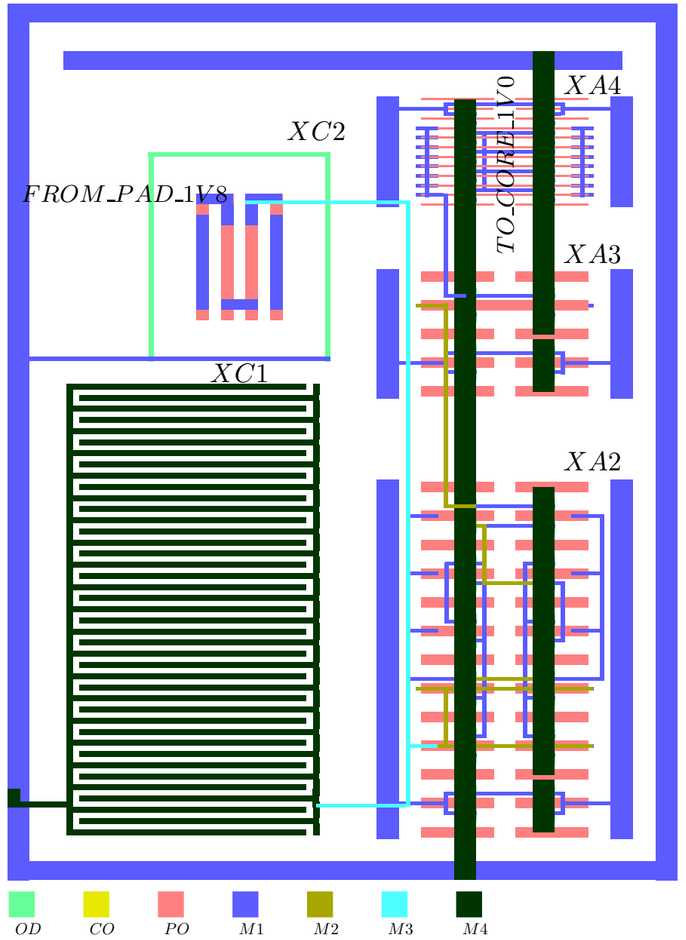
But I just want a digital input, what do I need?


Primary ESD
Secondary ESD
Bondwire
Input Buffer
Pad

Input buffer



(a)



(c)

```
.SUBCKT DI_1V8_ST28N AVDD_1V0 AVDD_1V8
+ AVSS FROM_PAD_1V8 TO_CORE_1V0
XC1 FILT_O AVSS  CAPX10_CV angle=180
XC2 FROM_PAD_1V8 FILT_O AVSS  RPPO_S0
+ xoffset=25 yoffset=15

XA5  AVSS  TAPCELL_EV xoffset=20
XA2 FILT_O SCHMITT_O AVDD_1V8 AVSS SCX1_EV

XA5a  AVSS  TAPCELL_EV  yoffset=20
XA3 SCHMITT_O INV_O AVDD_1V0 AVSS  IVX1_EV

XA4 INV_O TO_CORE_1V0 AVDD_1V0 AVSS IVX8_CV
+ yoffset=15
XA6  AVSS  TAPCELL_CV

.ENDS
```

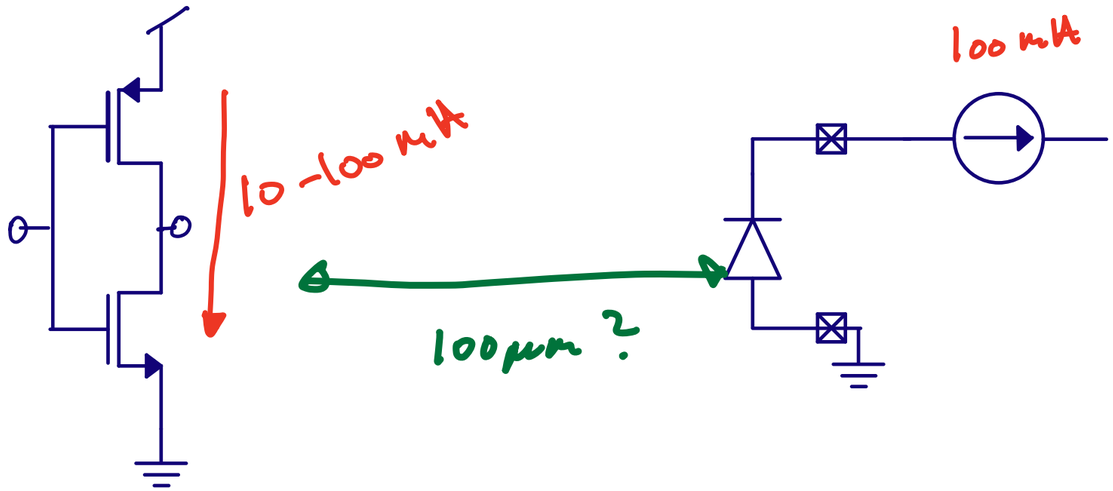
(b)

```
{ "name" : "DI_1V8_ST28N",
  "boundaryIgnoreRouting" : 0,
  "composite" : 1,  "noPowerRoute" : 1,
  "schematic" : 0,
  "class" : "Layout::LayoutDigitalCell",
  "afterPlace" :{
      "addPowerRings" :[
          ["M1","AVDD_1V0","t"],
          ["M1","AVSS","btrl"]
      ]
  },
  "beforeRoute" : {
      "addPowerConnections" : [
          ["AVDD_1V0","XA","top"],
          ["AVSS","XC","left"],
          ["AVSS","XA4|XA2","bottom"]
      ],
      "addConnectivityRoutes" : [
          ["M3","FILT_O","--|-","onTopR"],
          ["M2","SCHMITT_O","-|--"],
          ["M1","INV_O","-|--"]

      ]
  }
}
```

(d)

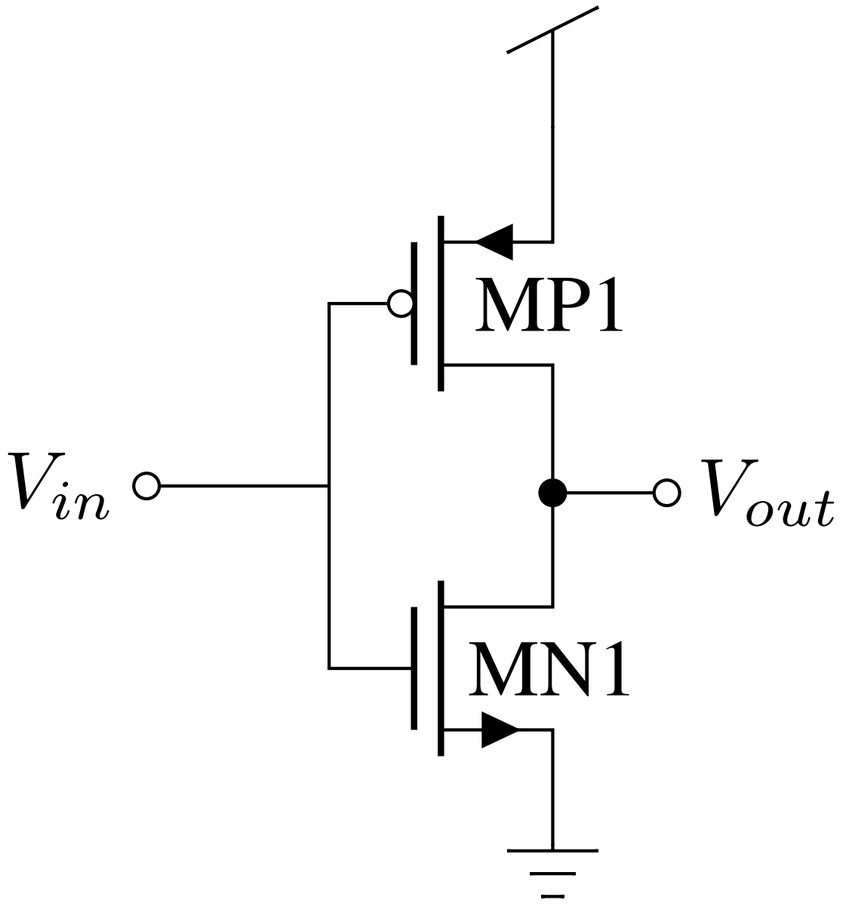
Latch-up



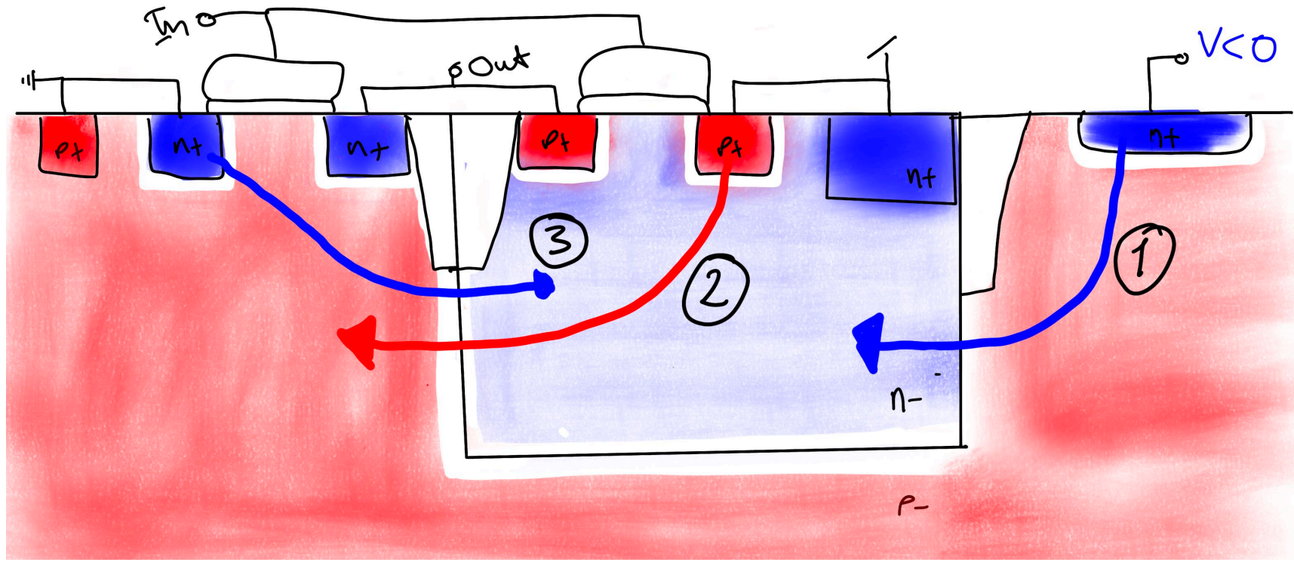
How can current in one place lead to a current somewhere else?

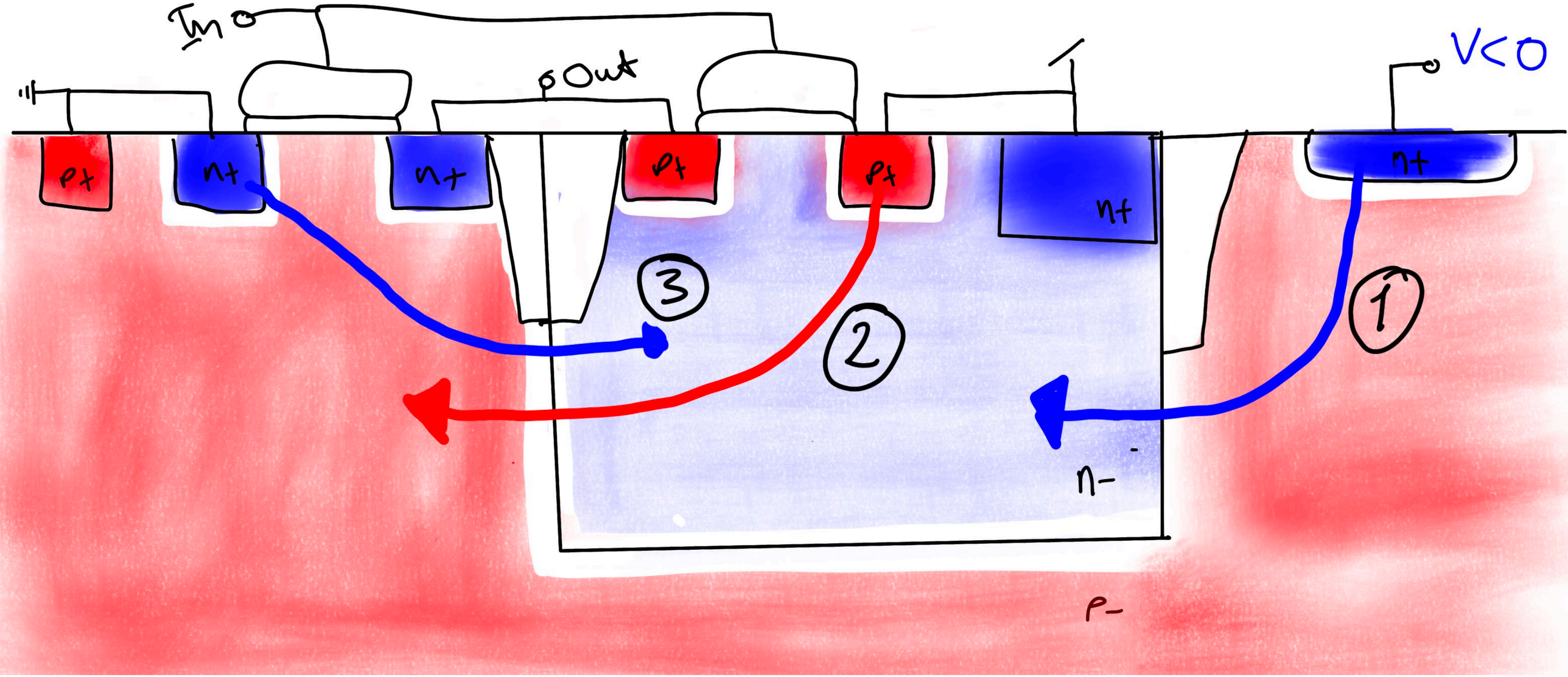
Logic cells close to large NMOS pad drivers are prone to latch-up.

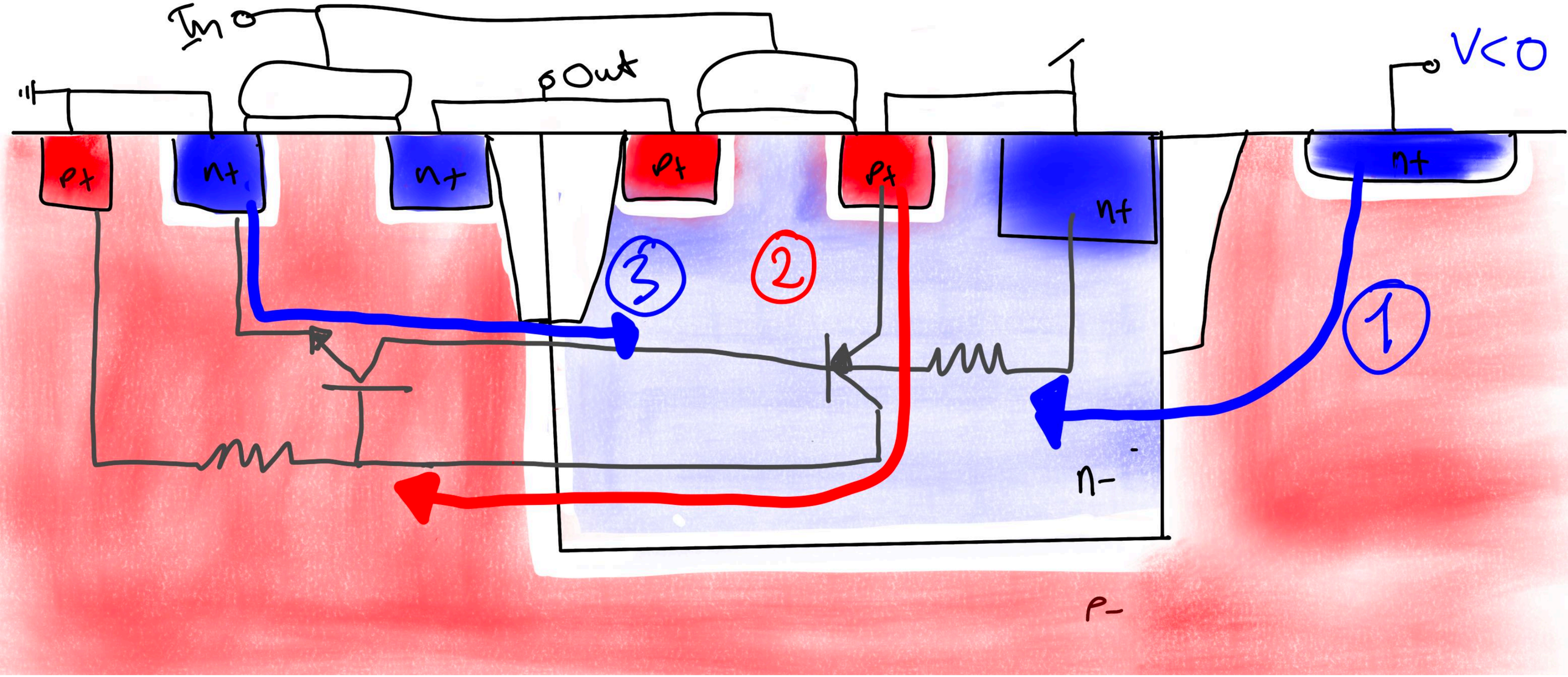
The latch-up process can start with electrons injected into the p-type substrate.



1. Electrons injected into substrate, diffuse around, but will be accelerated by n-well to p-substrate built in voltage. Can end up in n-well
2. PMOS drain can be forward biased by reduced n-well potential. Hole injection into n-well. Holes diffuse around, but will be accelerated by n-well to p-substrate built in voltage. Can end up in p-substrate under NMOS
3. NMOS source pn-junction can be forward biased. Electrons injected into p-substrate. Diffuse around, but will be accelerated by n-well to p-substrate built in voltage.
4. Go to 2 (latch-up)




In
pOut
V<0
p+
n+
n+
p+
p+
n+
n+
3
2
1
n-
p-


In
pOut
V<0
p+
n+
n+
p+
p+
n+
n+
3
2
1
n-
p-

You must **always handle ESD** on an IC

- Do everything yourself
- Use libraries from foundry
- Get help www.sofics.com

Thanks!