TFE4152 - Lecture 4

MOSFET's

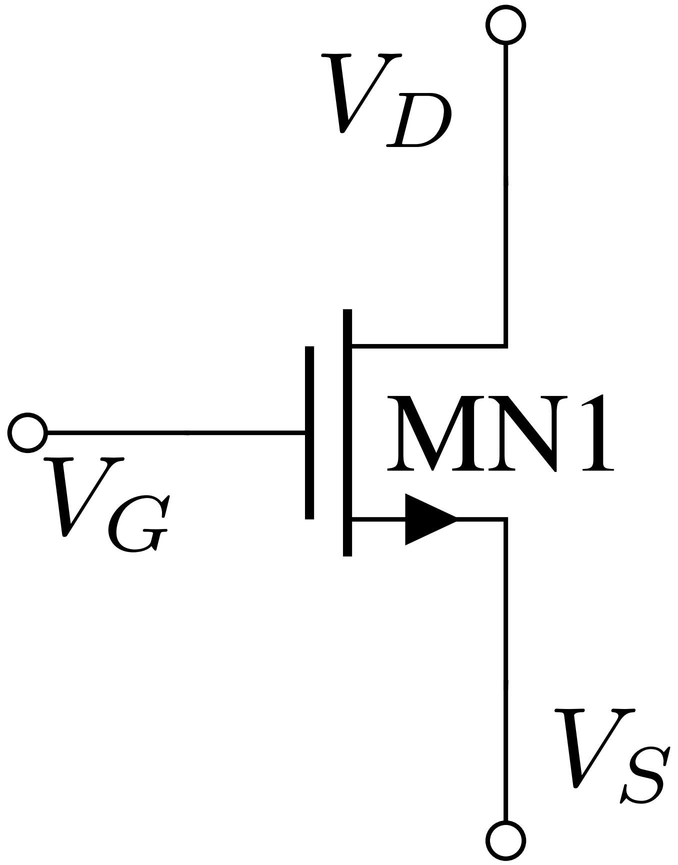
Source

Goal for today

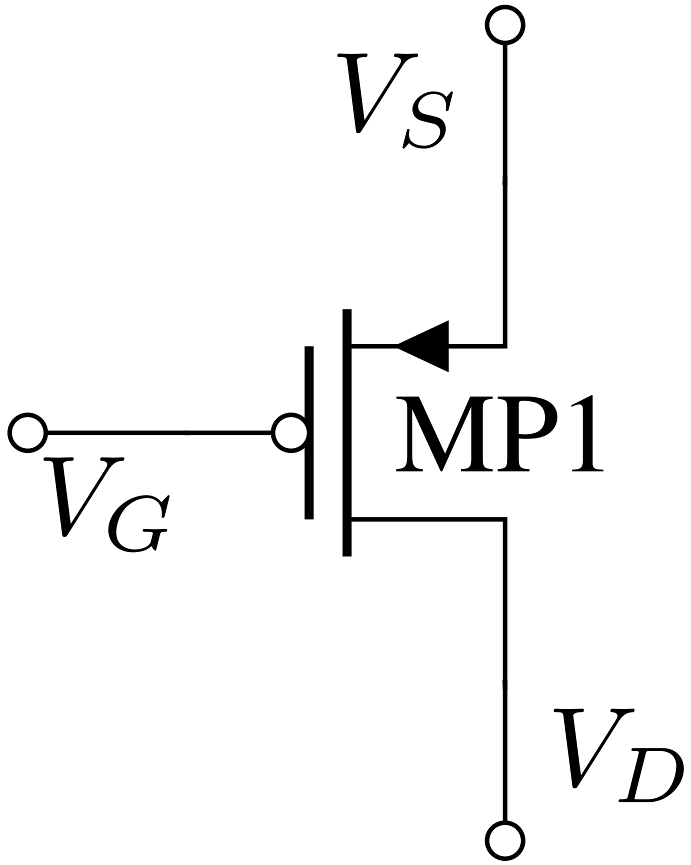
- Symbols
- Current characteristics
- Operating regions
- The square-law model
- Channel length modulation
- The small signal model (low frequency)
- Bulk Effect

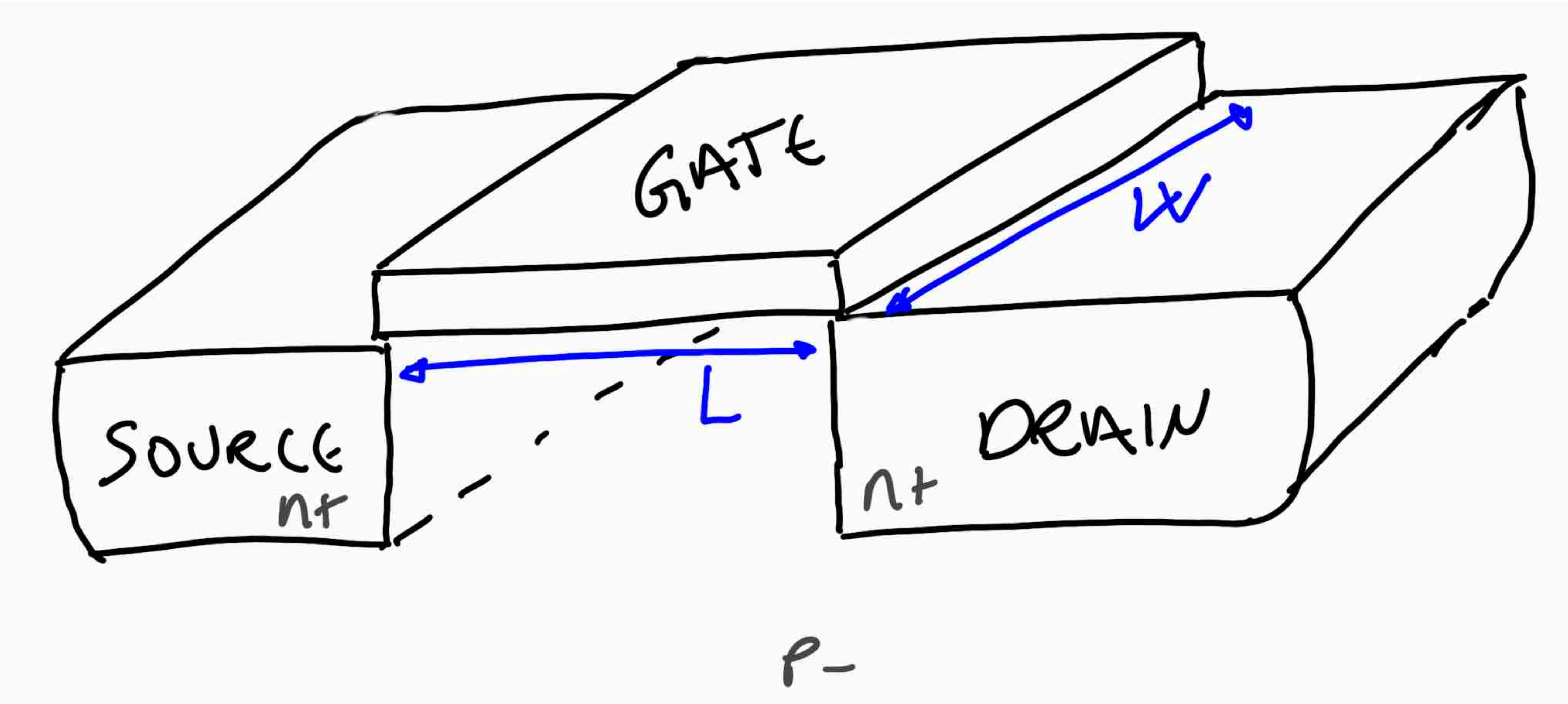
Metal-Oxide-Semiconductor (MOS) Transistors

NMOS conduct for positive gate-to-source voltage



PMOS conduct for negative gate-to-source voltage



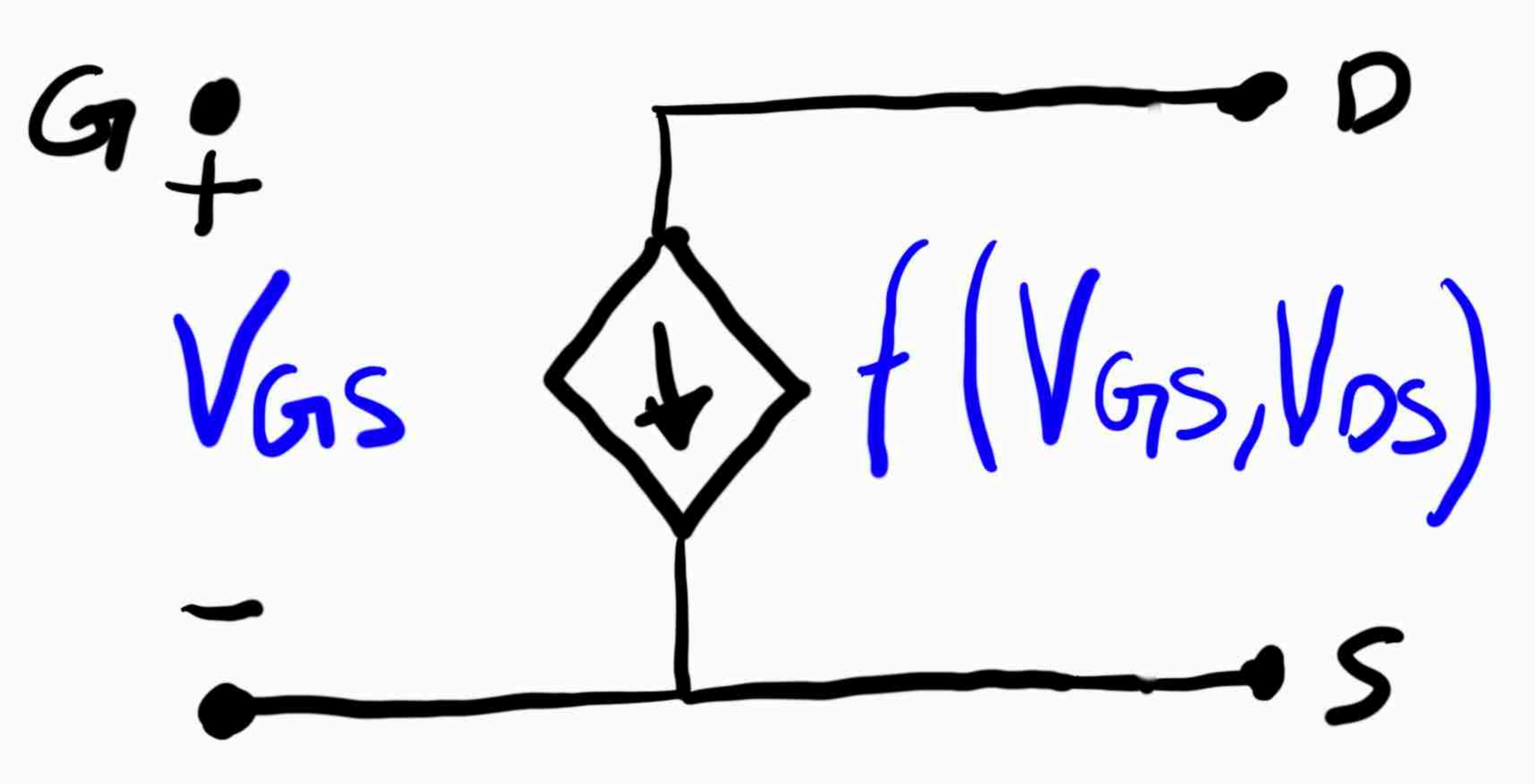

GATE
W
L
SOURCE
n+
n+
DRAIN
p-

Drain Source Current (I_{DS})

dicex/sim/spice/NCHIO

Large signal model

$$I_{DS} = f(V_{GS}, V_{DS}, \ldots)$$



Gate Source Voltage (V_{GS})

dicex/sim/spice/vgate.cir:

```
.include ../../../lib/SUN_TRIO_GF130N.spi
.include ../../../models/ptm_130.spi

vdrain  D  0  dc  1
vgate   G  0  dc  0.5

vbulk   B  0  dc  0
vcur    S  0  dc  0

X1 D G S B NCHIO

.dc vgate 0 1.8 0.01

.plot I(vcur)
```

dicex/lib/SUN_TRIO_GF13N.spi:

```
.SUBCKT NCHIO D G S B
M1   D   G   S   B  nmos   w=1.08u    l=0.6u
.ENDS
```

dicex/models/ptm_130.spi

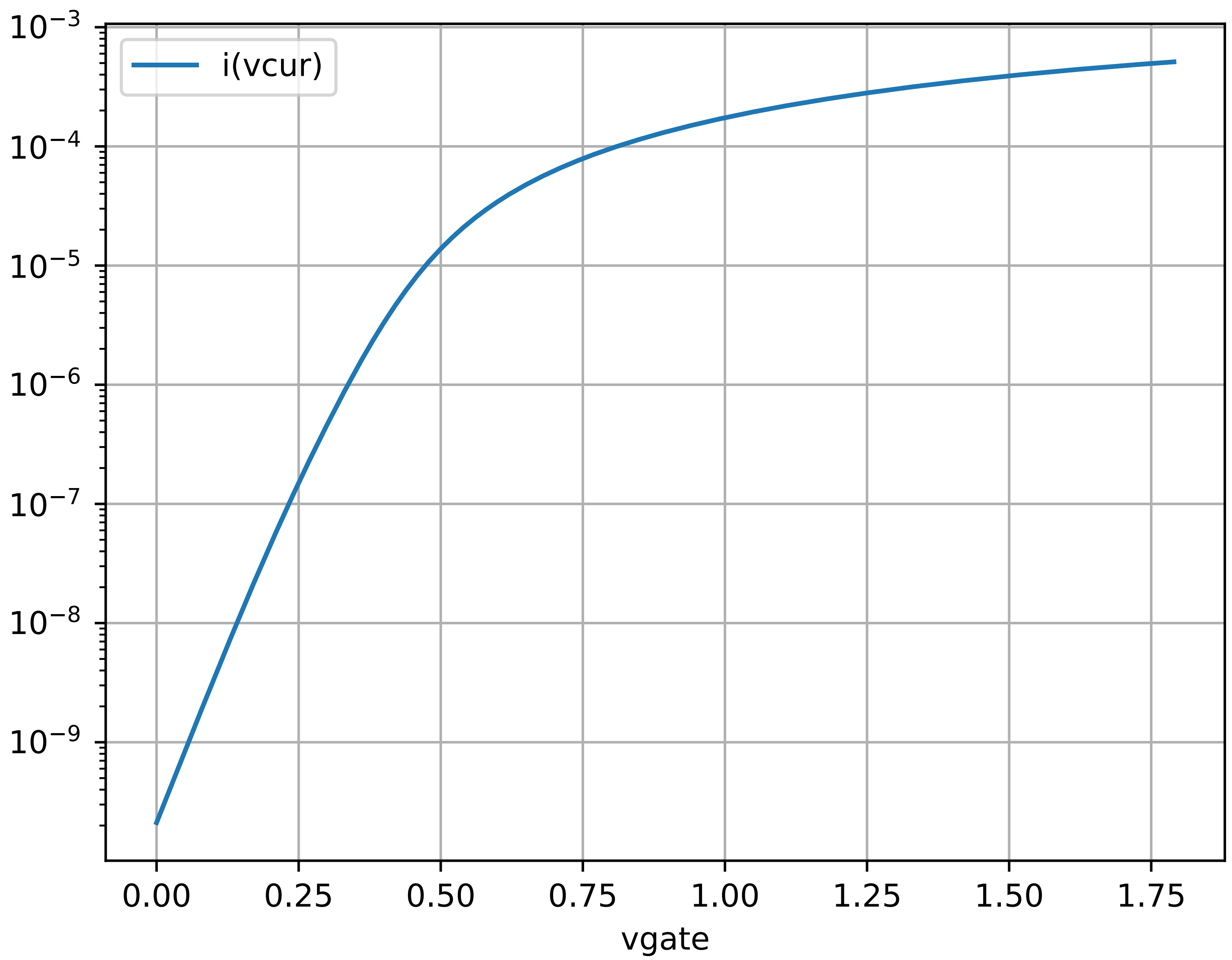
```
.model  nmos  nmos  level = 21
+version = 4.0          binunit = 1            paramchk= 1            mobmod  = 0
+capmod  = 2            igcmod  = 1            igbmod  = 1            geomod  = 1
+diomod  = 1            rdsmod  = 0            rbodymod= 1            rgatemod= 1
+permod  = 1            acnqsmod= 0            trnqsmod= 0

+tnom    = 27           toxe    = 2.25e-9      toxp    = 1.6e-9       toxm    = 2.25e-9
+dtox    = 0.65e-9      epsrox  = 3.9          wint    = 5e-009       lint    = 10.5e-009
...(about 60 more lines)
```

Gate-source voltage

Param	Voltage [V]
V_{GS}	0 to 1.8
V_{DS}	1.0
V_S	0
V_B	0

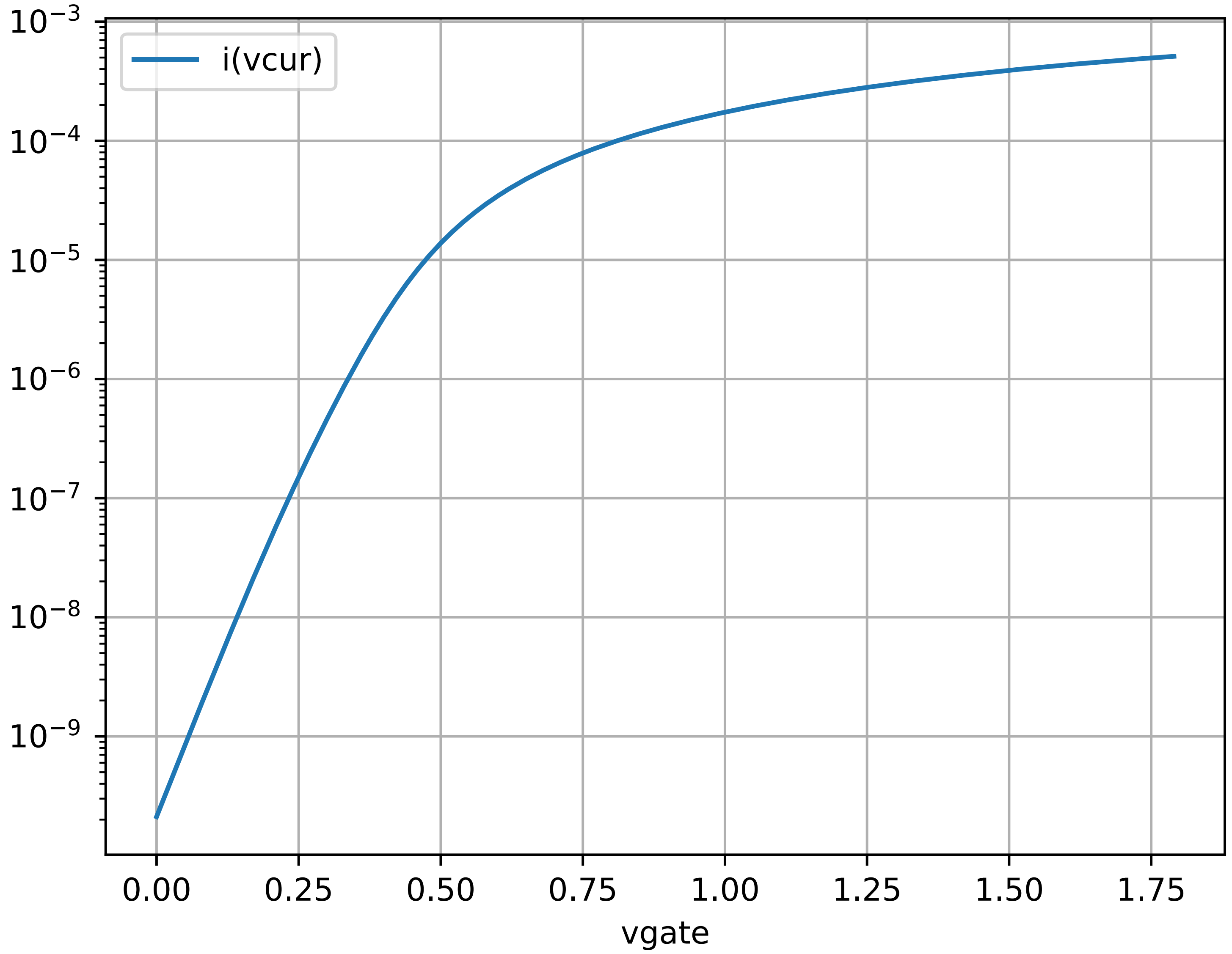
$$i(vcur) = I_{DS}$$



Inversion level

Define $V_{eff} \equiv V_{GS} - V_{tn}$, where V_{tn} is the "threshold voltage"

V_{eff}	**Inversion level**
< 0	weak inversion or subthreshold
0	moderate inversion
> 100 mV	strong inversion

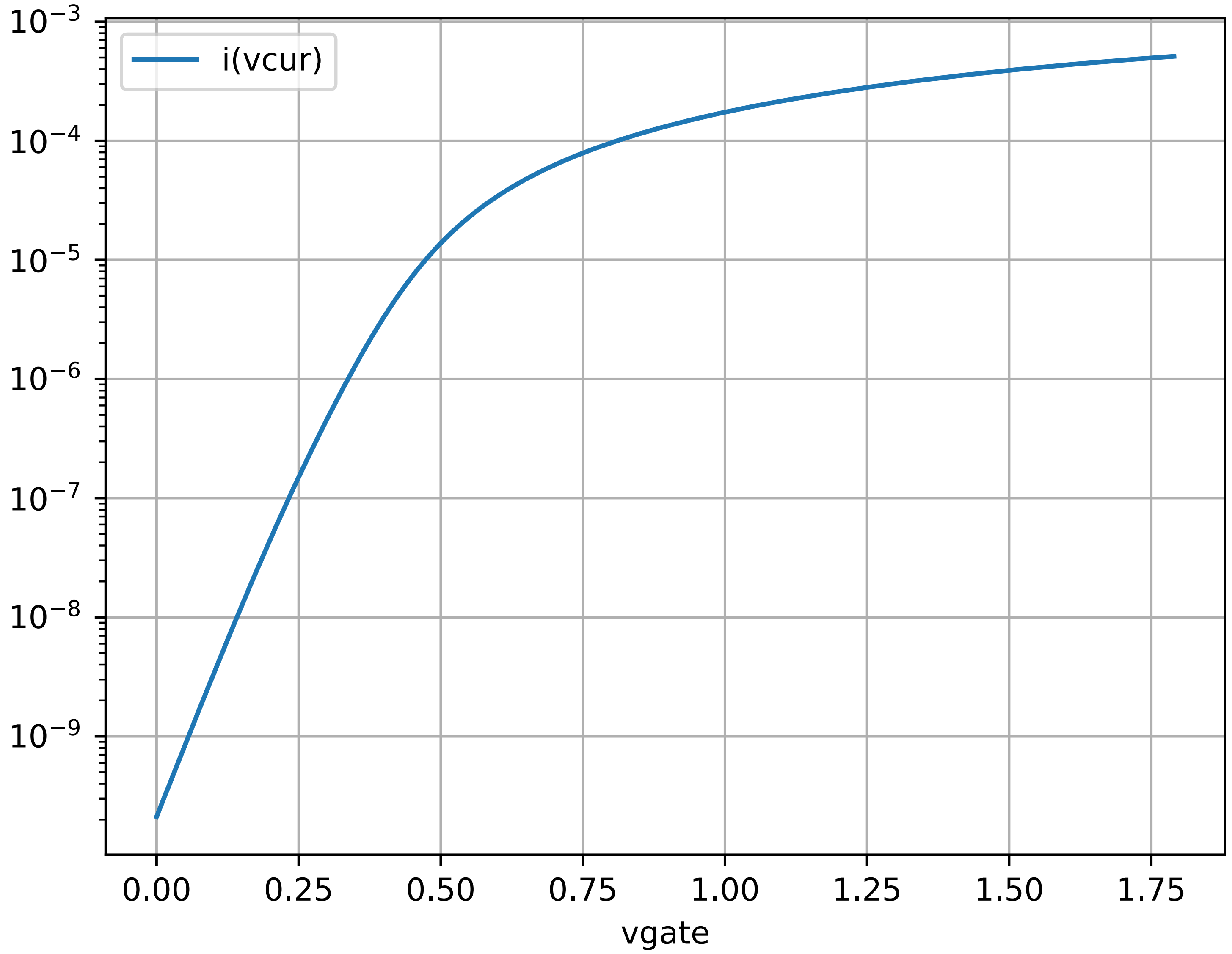


Weak inversion

The drain current is low, but not zero, when $V_{eff} << 0$

$$I_{DS} \approx I_{D0}\frac{W}{L}e^{V_{eff}/nV_T} \text{ if } V_{DS} > 3V_T$$

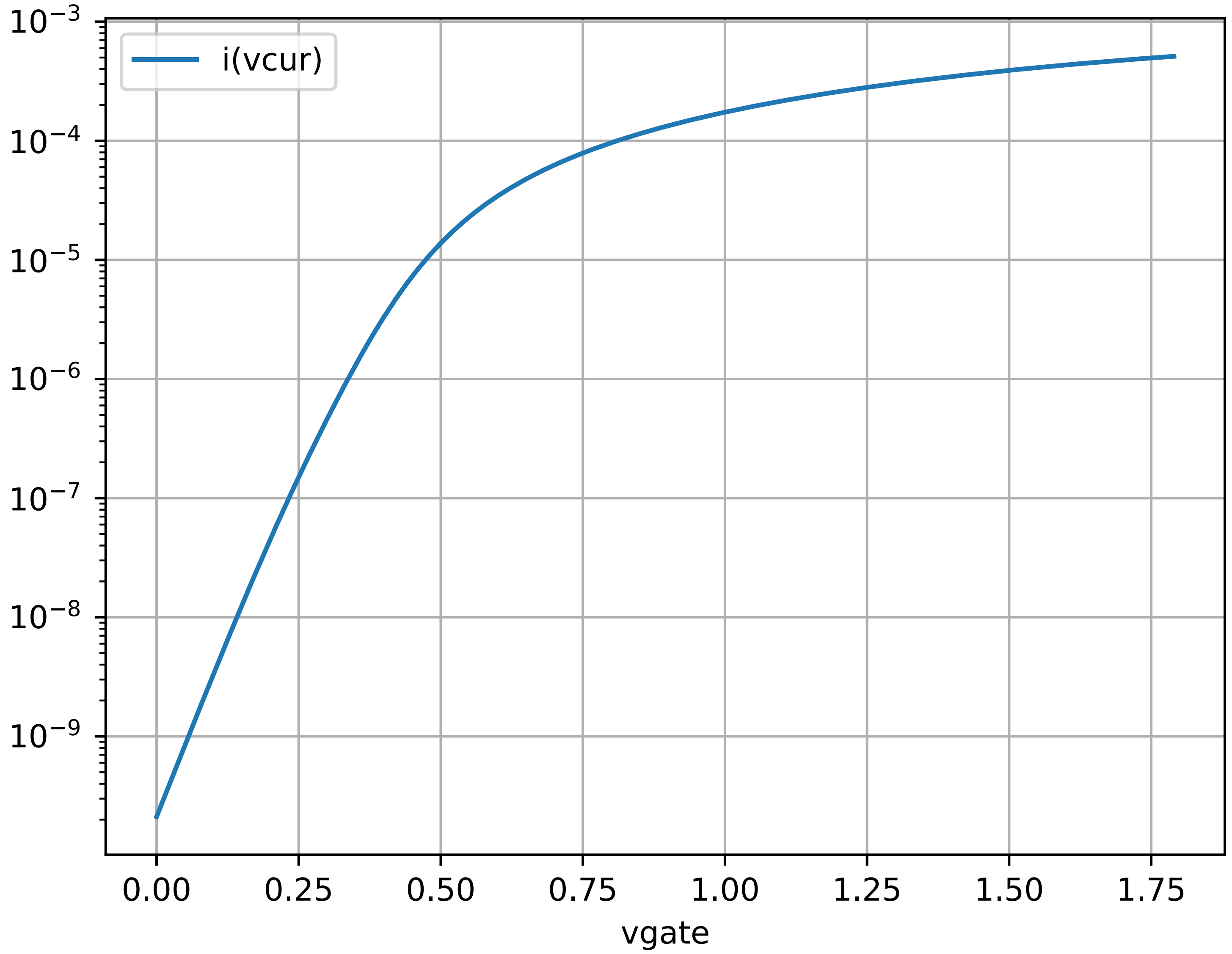
$$n \approx 1.5$$



Moderate inversion

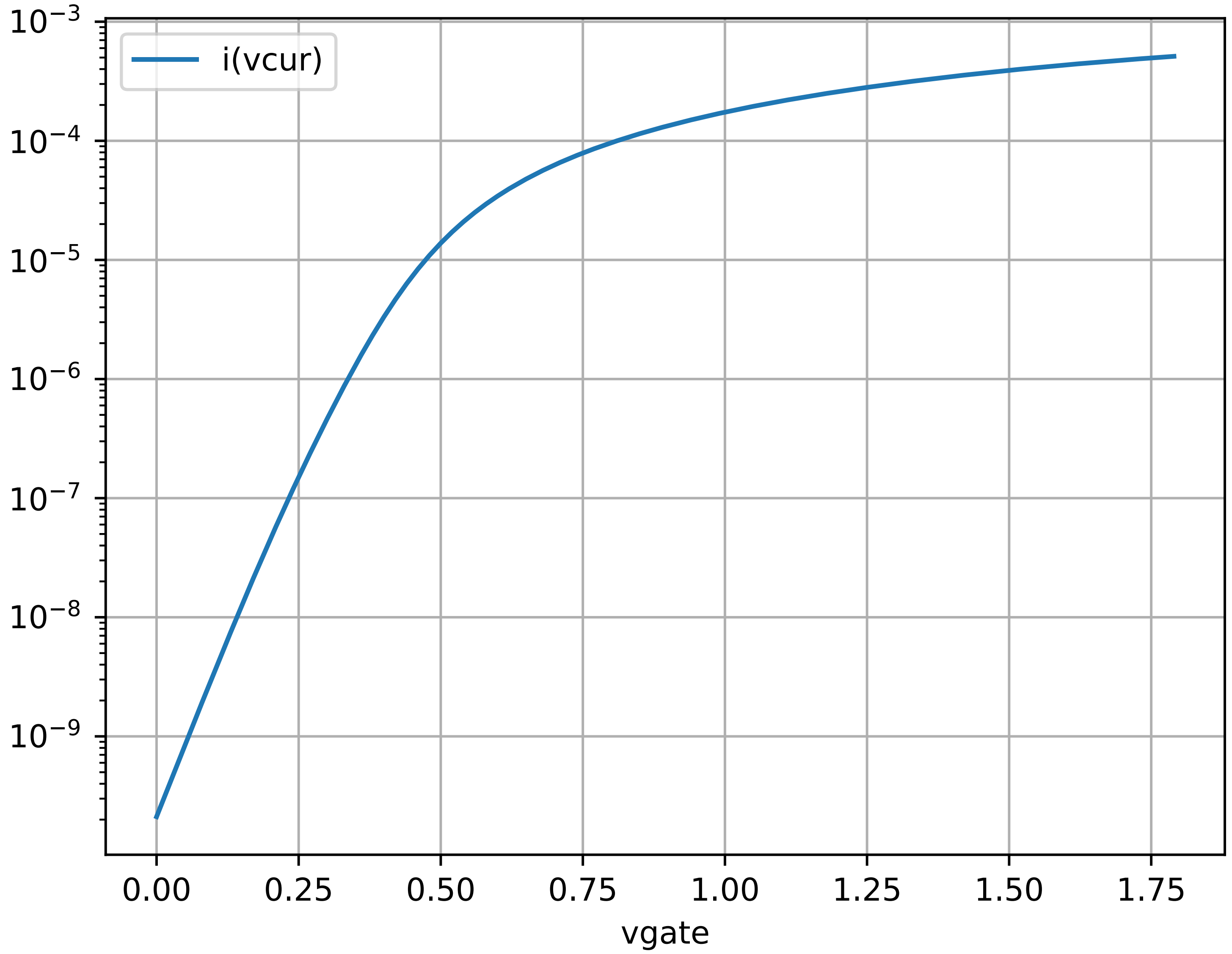
Stay away from moderate inversion for analog design.

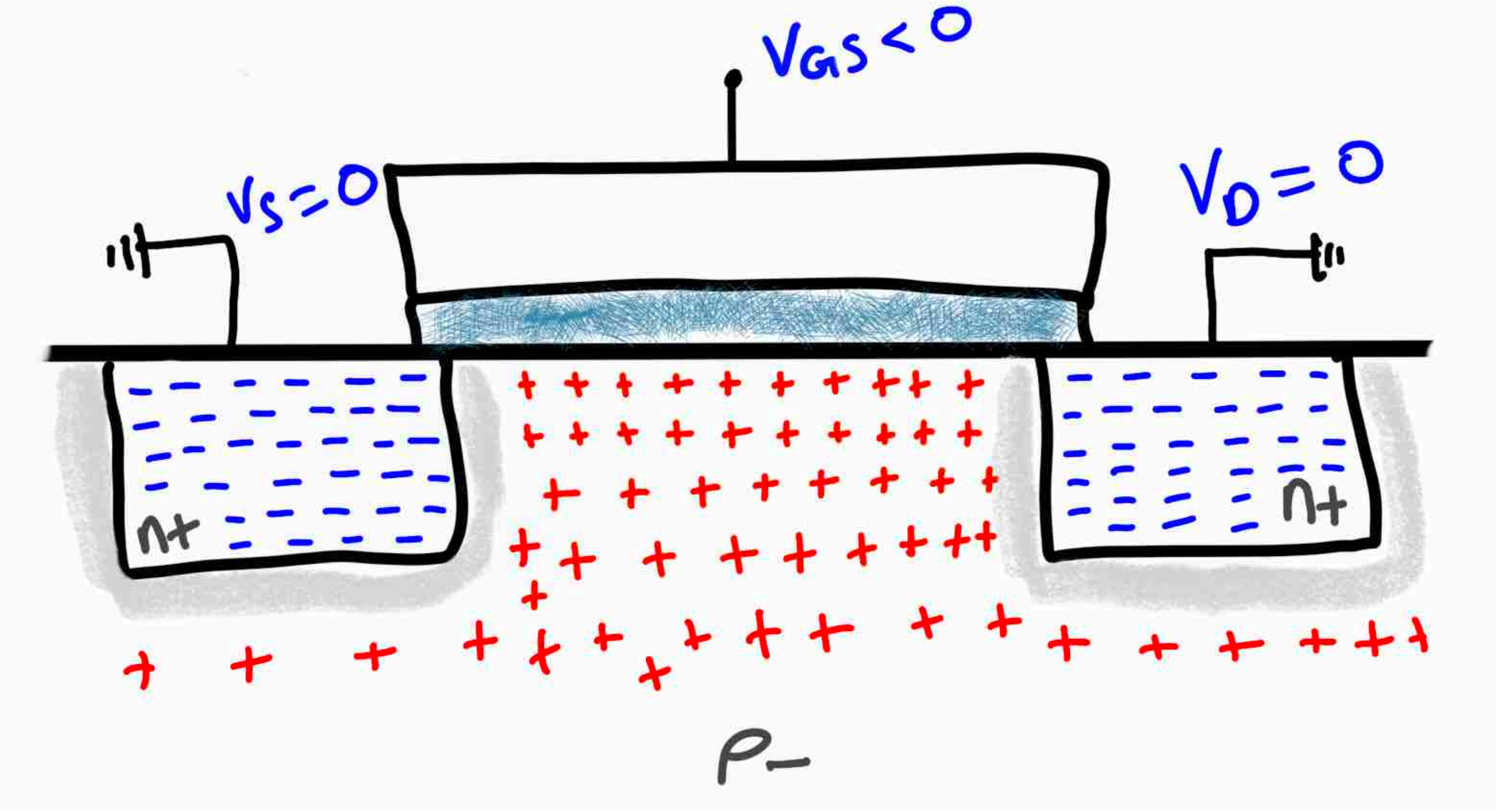
If you can't, then trust the model



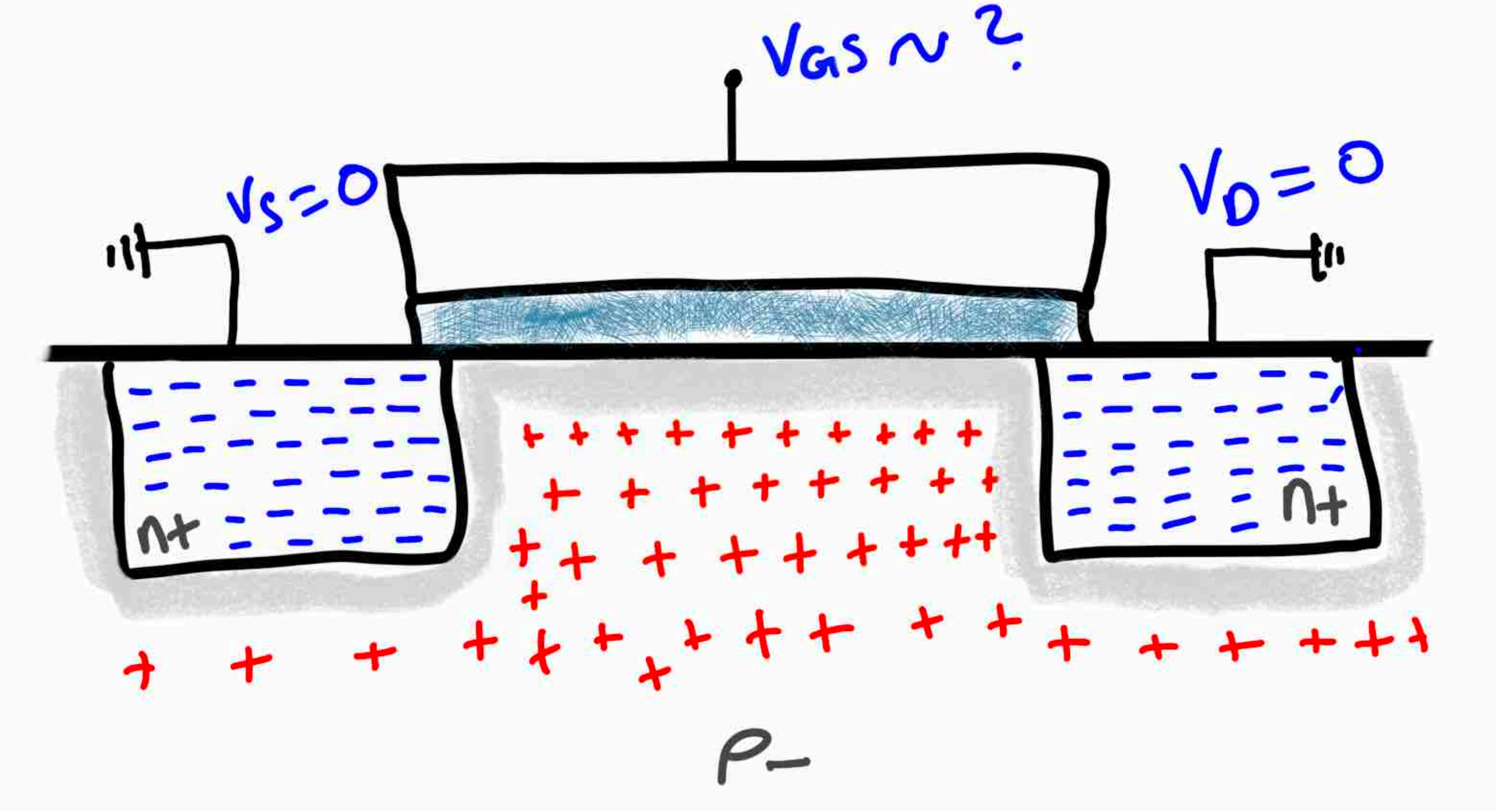
Strong inversion

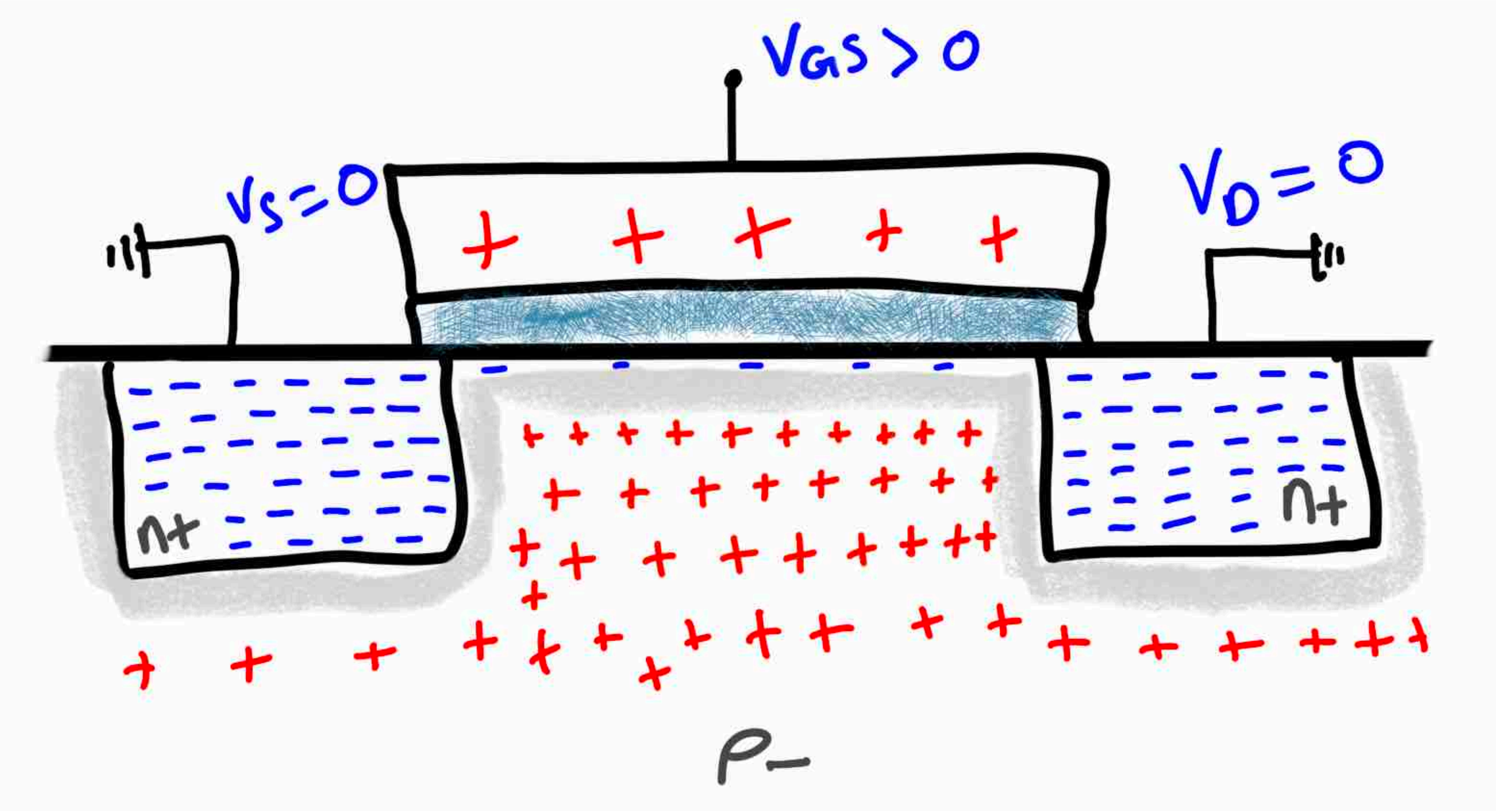
$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \begin{cases} V_{eff} V_{DS} & \text{if } V_{DS} << V_{eff} \\ V_{eff} V_{DS} - V_{DS}^2/2 & \text{if } V_{DS} < V_{eff} \\ \frac{1}{2} V_{eff}^2 & \text{if } V_{DS} > V_{eff} \end{cases}$$

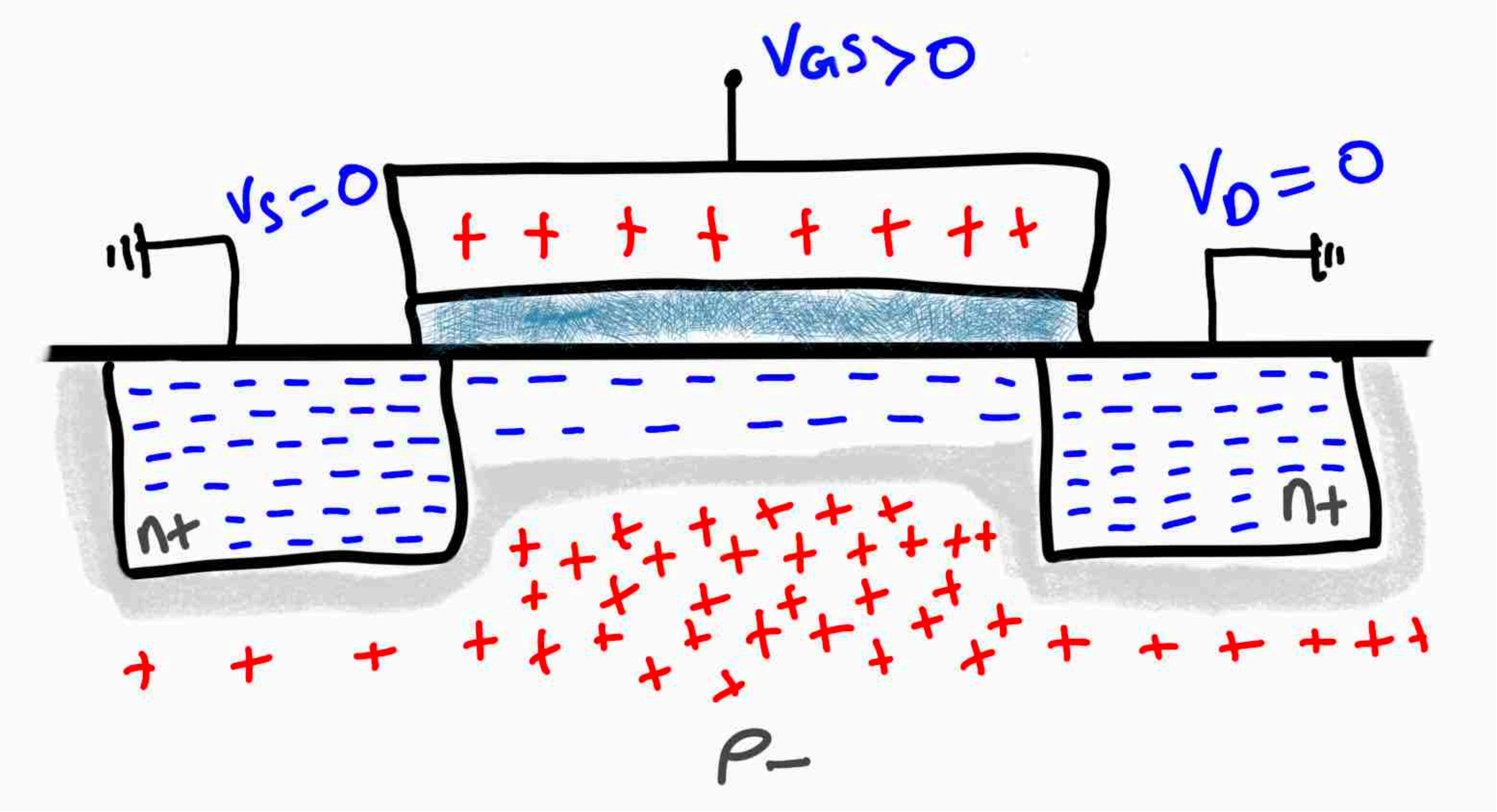




VGS<0
Vs=0
VD=0
n+
n+
p−


VGS ~ 2
VS=0
VD=0
n+
n+
P-


VGS > 0
VS = 0
VD = 0
n+
n+
p-



VGS>0
Vs=0
VD=0
n+
n+
p-

The threshold voltage (V_{tn}) is defined as $p_p = n_{ch}$

Gate Source Capacitance (C_{GS})

C_{GS} for $V_{DS} = 0, V_S = 0$

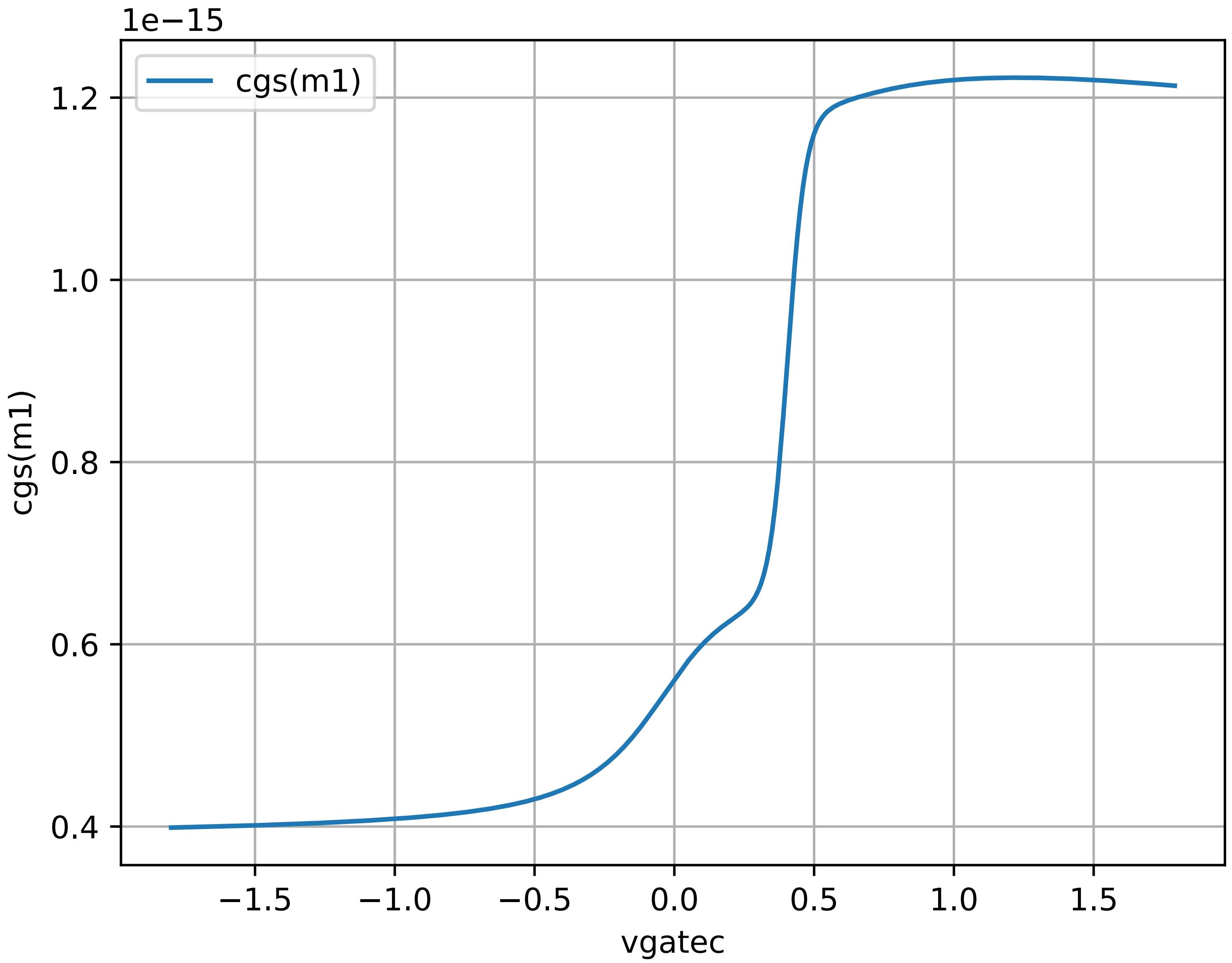
In strong inversion

$$C_{GS} = WLC_{ox}$$

where

$$C_{ox} = \frac{K_{ox}\epsilon_0}{t_{ox}}$$

$$Q_{ch} = WLC_{ox}V_{eff}$$

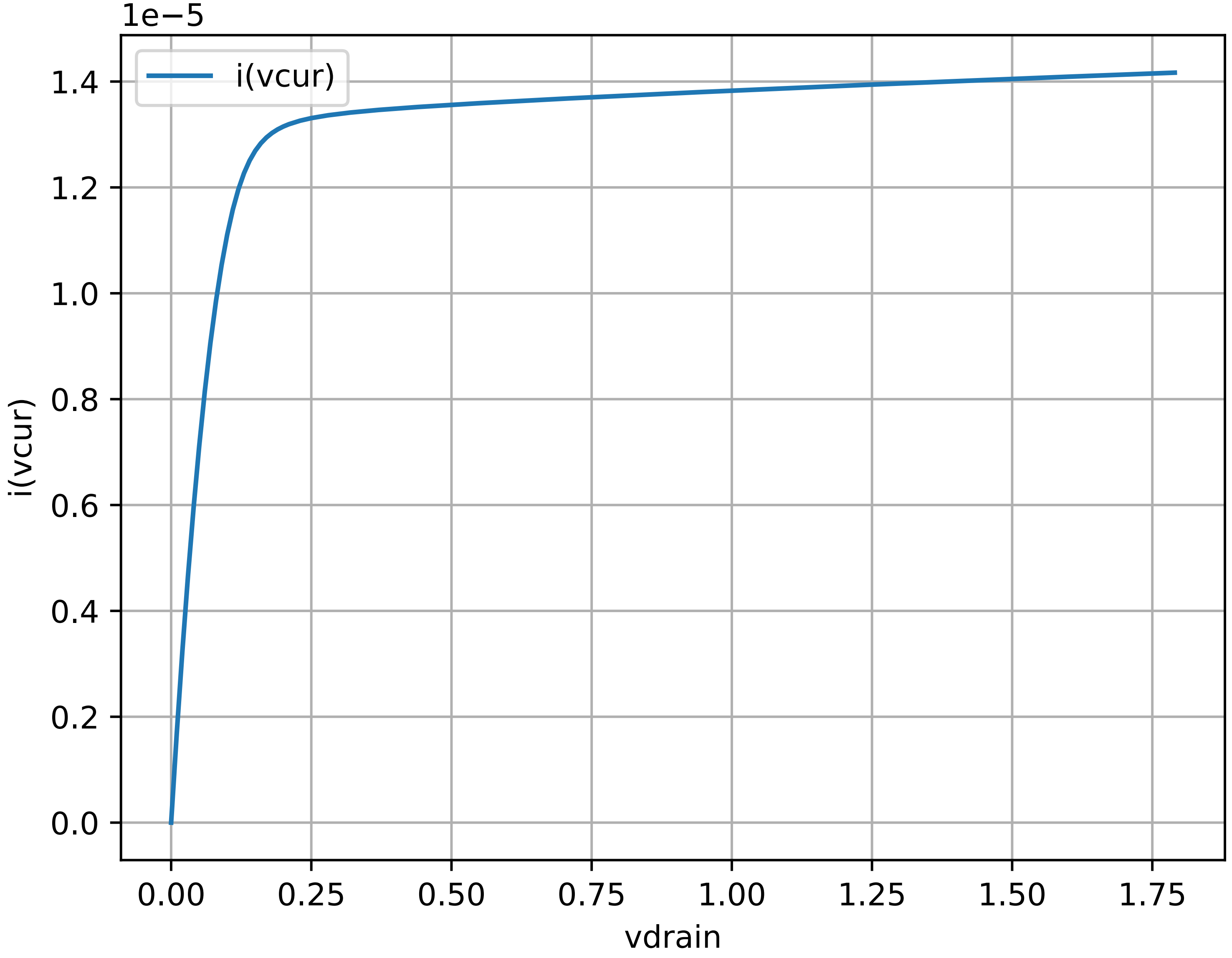


Drain Source Voltage (V_{DS})

Drain-source voltage

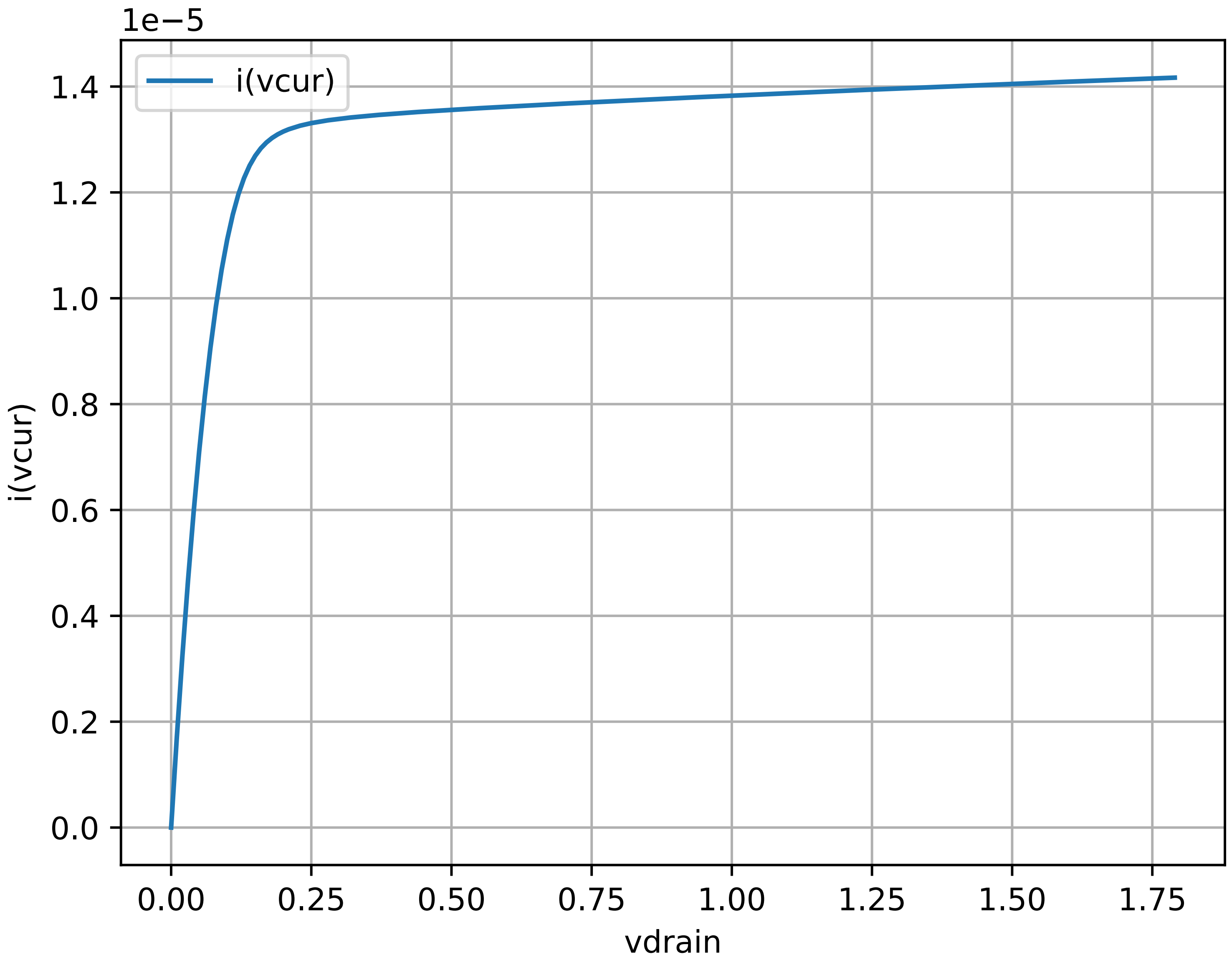
Param	Voltage [V]
V_{GS}	0.5
V_{DS}	0 to 1.8
V_S	0
V_B	0

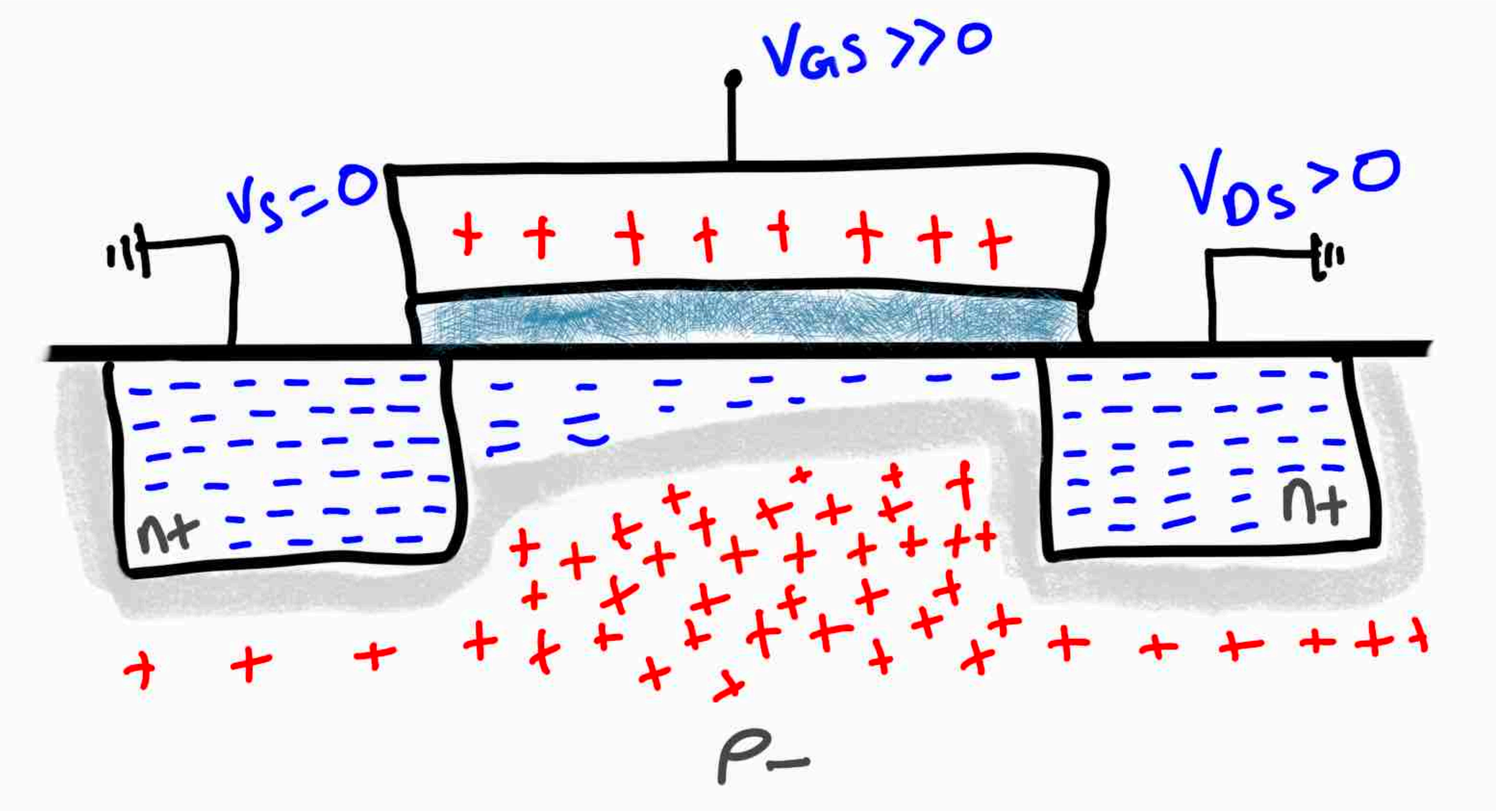
$$i(vcur) = I_{DS}$$



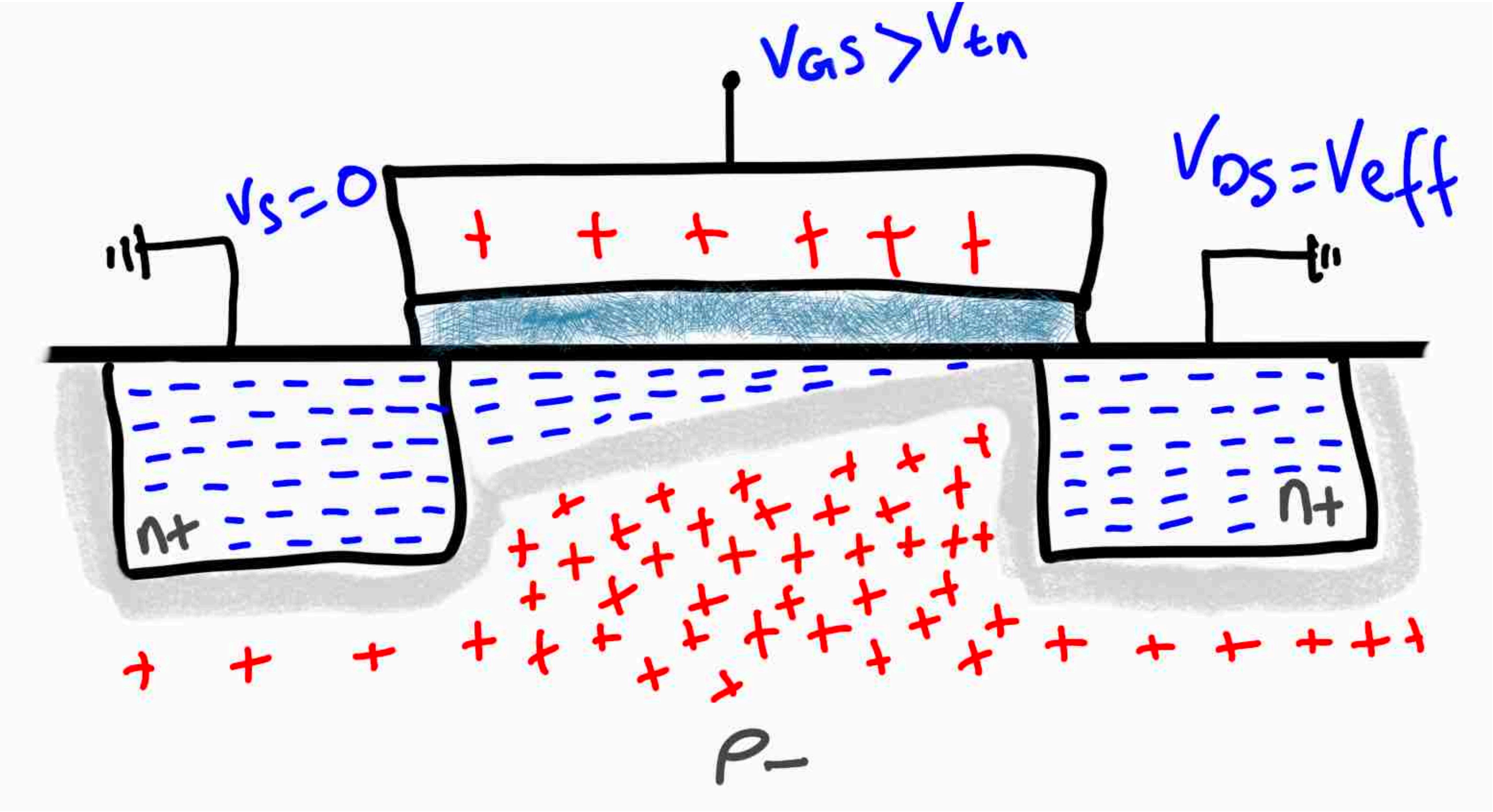
Strong inversion

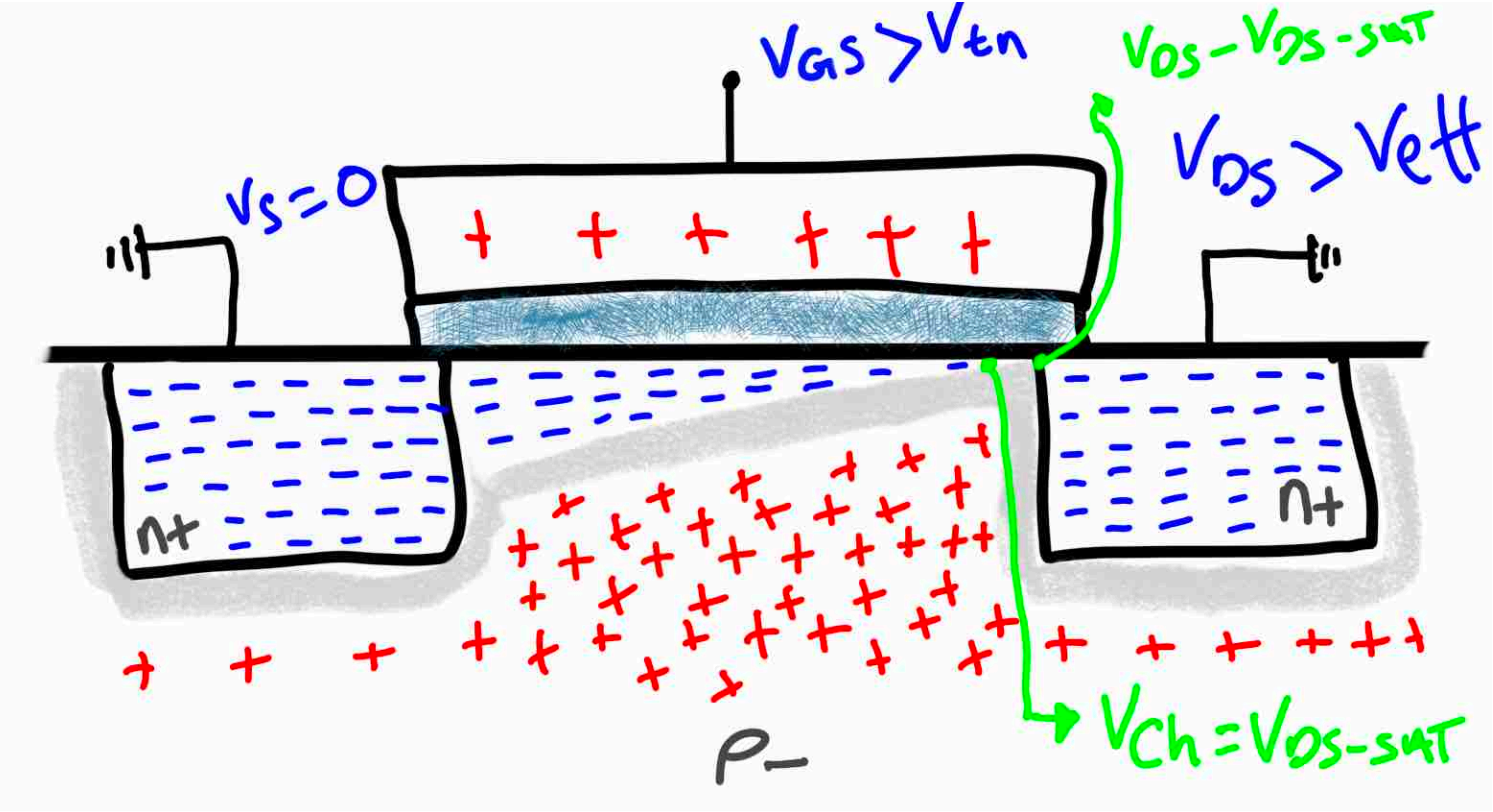
$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \begin{cases} V_{eff} V_{DS} & \text{if } V_{DS} << V_{eff} \\ V_{eff} V_{DS} - V_{DS}^2/2 & \text{if } V_{DS} < V_{eff} \\ \frac{1}{2} V_{eff}^2 & \text{if } V_{DS} > V_{eff} \end{cases}$$



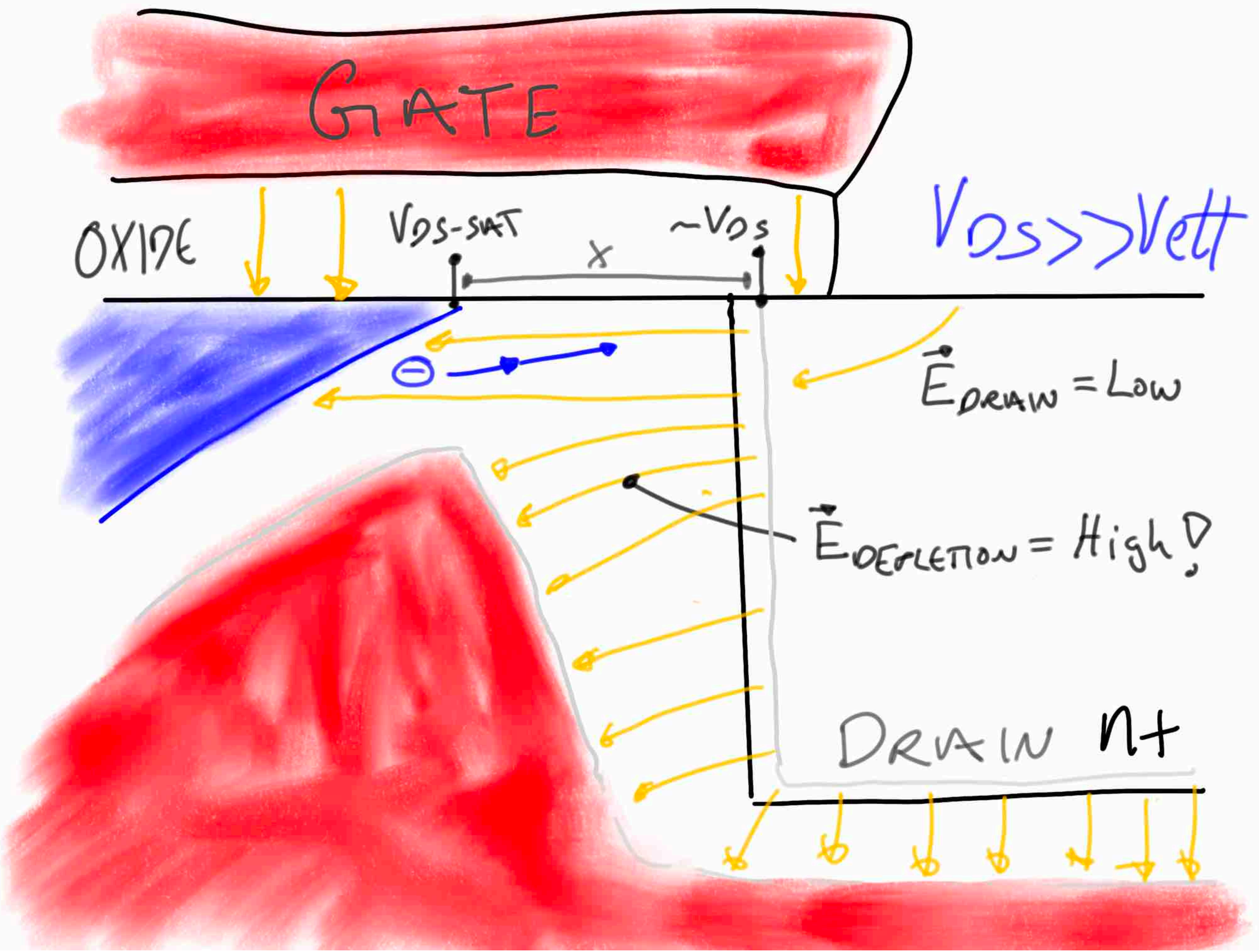


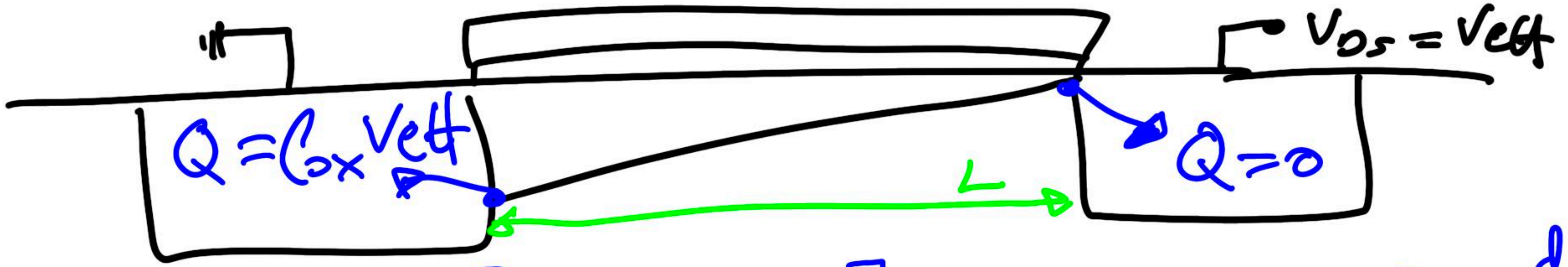
VGS >> 0
Vs = 0
VDS > 0
n+
n+
p-


VGS > Vtn
VS = 0
VDS = Veff
n+
n+
p-



VGS > Vtn
VDS - VDS-SAT
VDS > Veff
Vs = 0
n+
n+
p-
VCh = VDS-SAT


GATE
OXIDE
VDS-SAT
x
~VDS
VDS>>Veff
EDRAIN = Low
EDEPLETION = High!
DRAIN n+



$$Q(x) = C_{ox}\left[V_{eff} - V(x)\right] \qquad v = \text{speed} = \mu_n E = \mu_n \frac{dV}{dx}$$

$$I_D = W \cdot Q(x) \cdot v = \underbrace{\mu_n C_{ox} W}_{\ell} \left[V_{eff} - V(x)\right] \frac{dV}{dx}$$

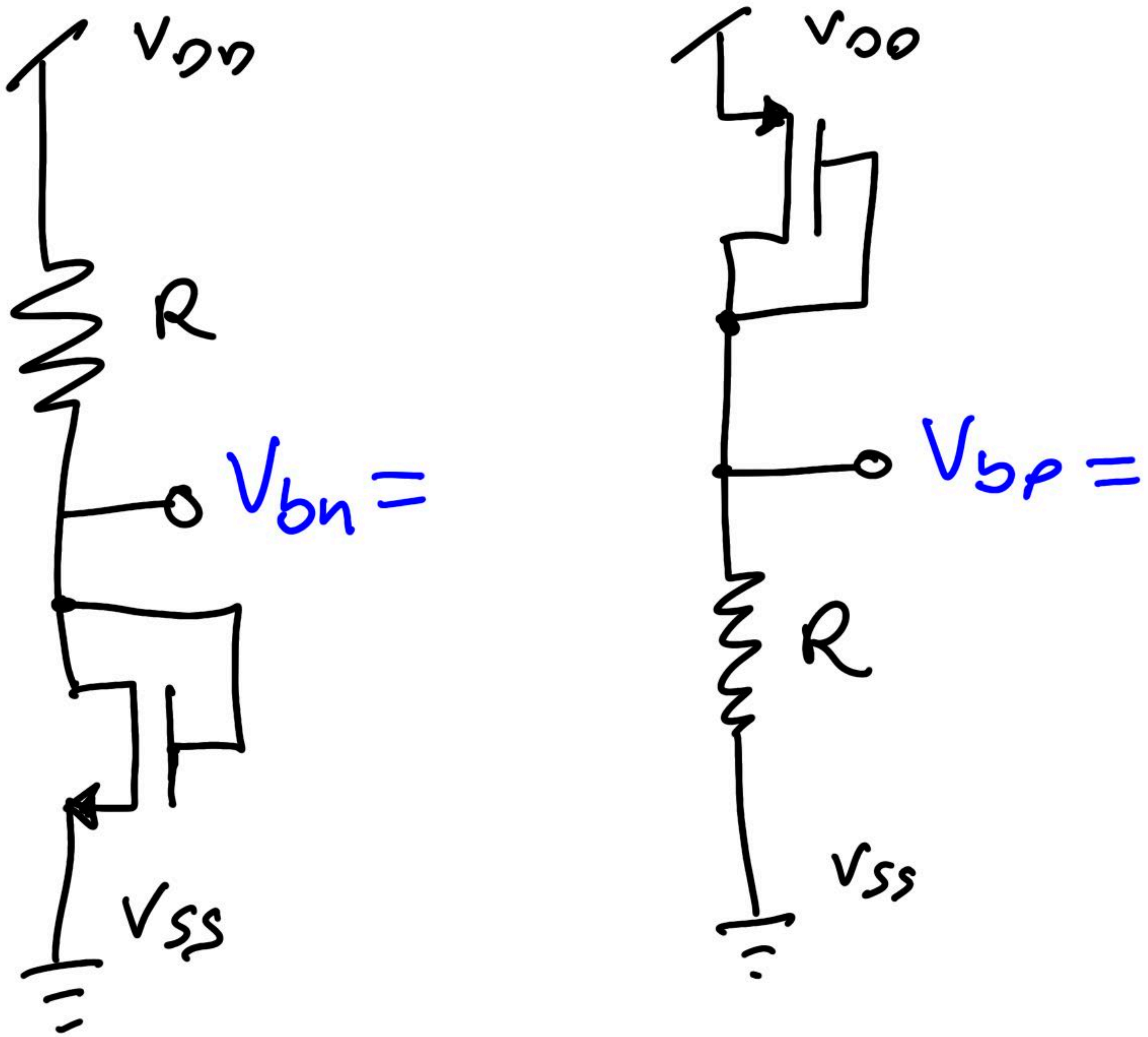
$$I_D \, dx = \ell \left[V_{eff} - V(x)\right] dV$$

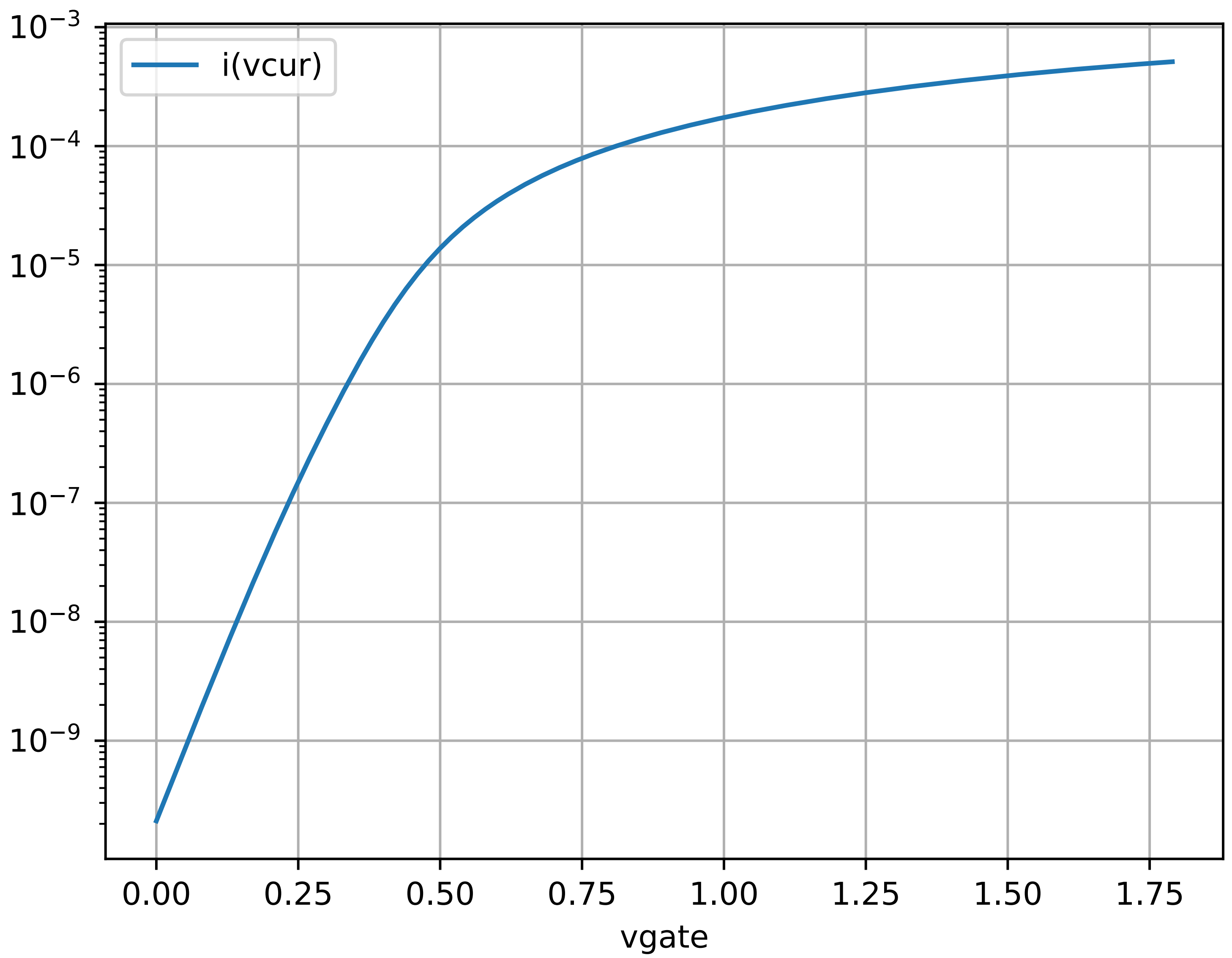
$$I_D \int_0^L dx = \ell \int_0^{V_{ds}} \left[V_{eff} - V(x)\right] dV$$

$$I_D L = \mu_n C_{ox} W \left[V_{eff} V_{ds} - \frac{V_{ds}^2}{2}\right]$$

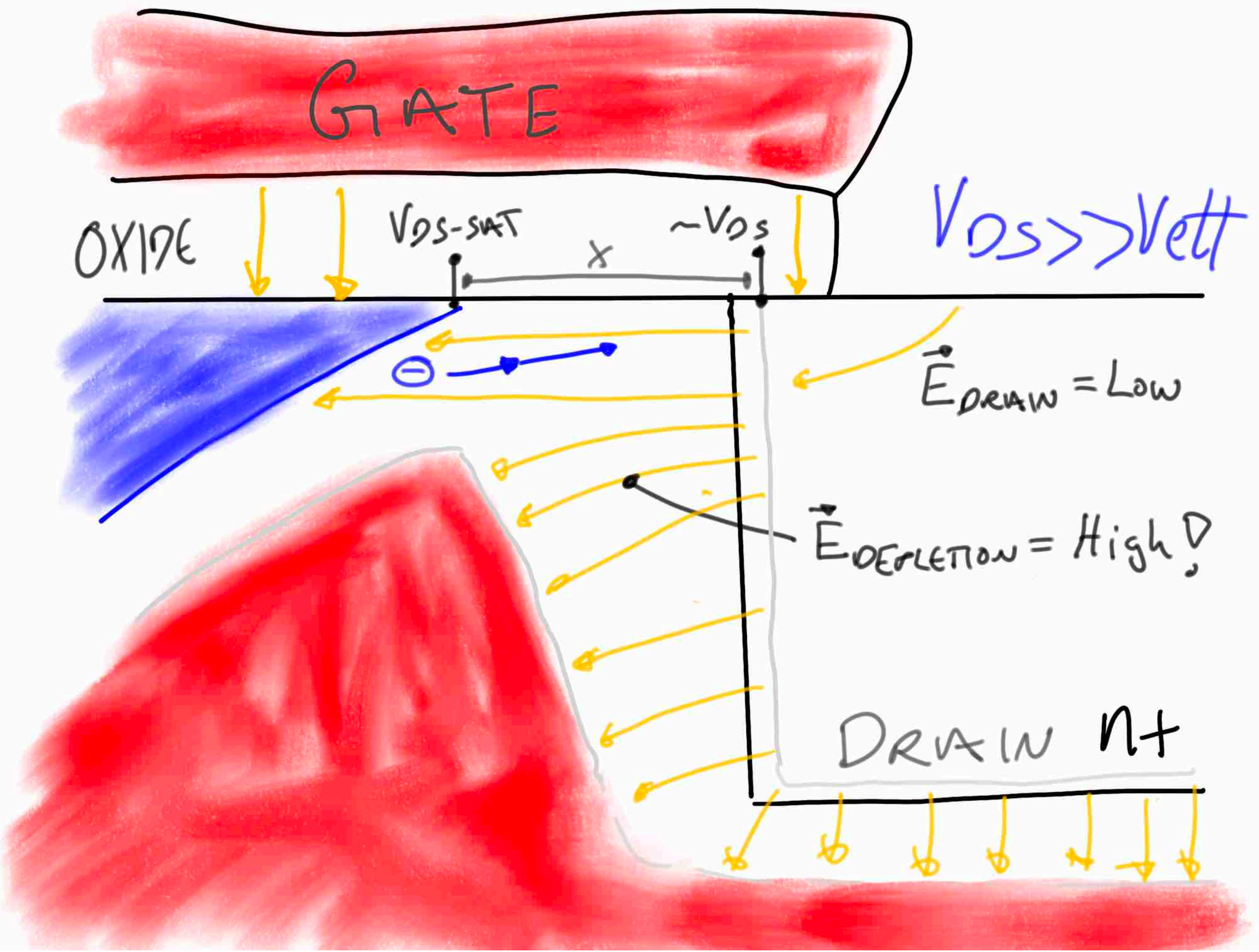
$$@\, V_{ds} = V_{eff} \Rightarrow \underline{\underline{I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{eff}^2}}$$

Head simulation


VDD
R
Vbn =
VSS
VDD
Vbp =
R
VSS


i(vcur)
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75
vgate

Channel length modulation



GATE
OXIDE
VDS-SAT
x
~VDS
VDS>>Veff
EDRAIN = Low
EDEPLETION = High!
DRAIN n+

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \begin{cases} V_{eff} V_{DS} & \text{if } V_{DS} << V_{eff} \\ V_{eff} V_{DS} - V_{DS}^2/2 & \text{if } V_{DS} < V_{eff} \\ \frac{1}{2} V_{eff}^2 [1 + \lambda(V_{DS} - V_{eff})] & \text{if } V_{DS} > V_{eff} \end{cases}$$

$$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{eff} + \Phi_0}}, \text{ where } k_{ds} = \sqrt{\frac{2K_s \epsilon_0}{qN_A}}$$

Thanks!