

TFE4152 - Lecture 2

Manufacture Integrated Circuits

Source

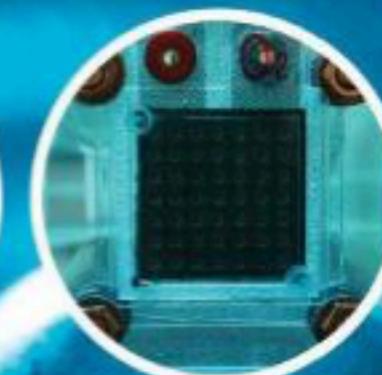
Goal for today

- Why
- How
- What

W A W h n y

FOURTH EDITION

Linden's Handbook of
Batteries



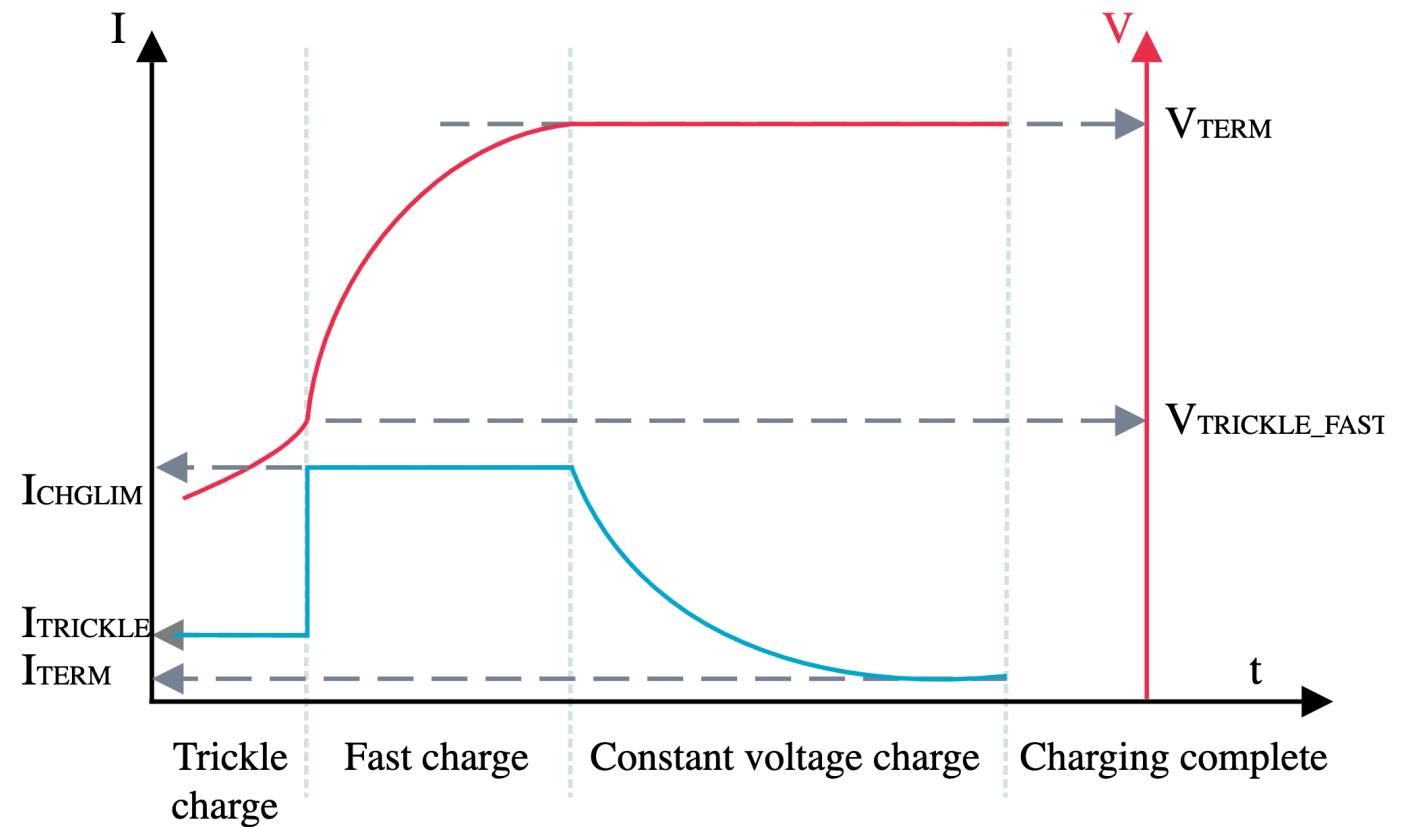
Carsten Wulff 2021

EDITED BY
THOMAS B. REDDY

Let's make a
battery charger

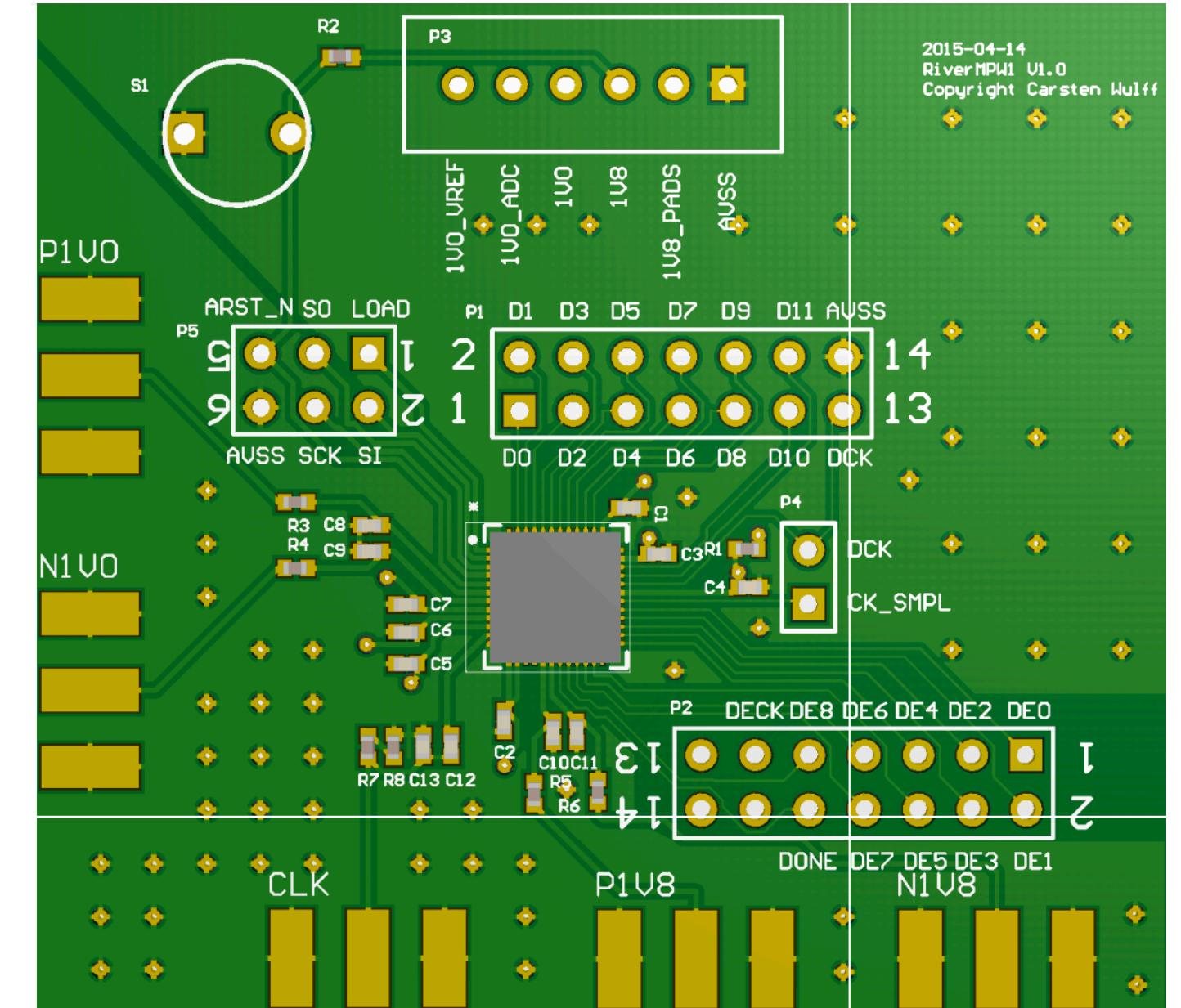
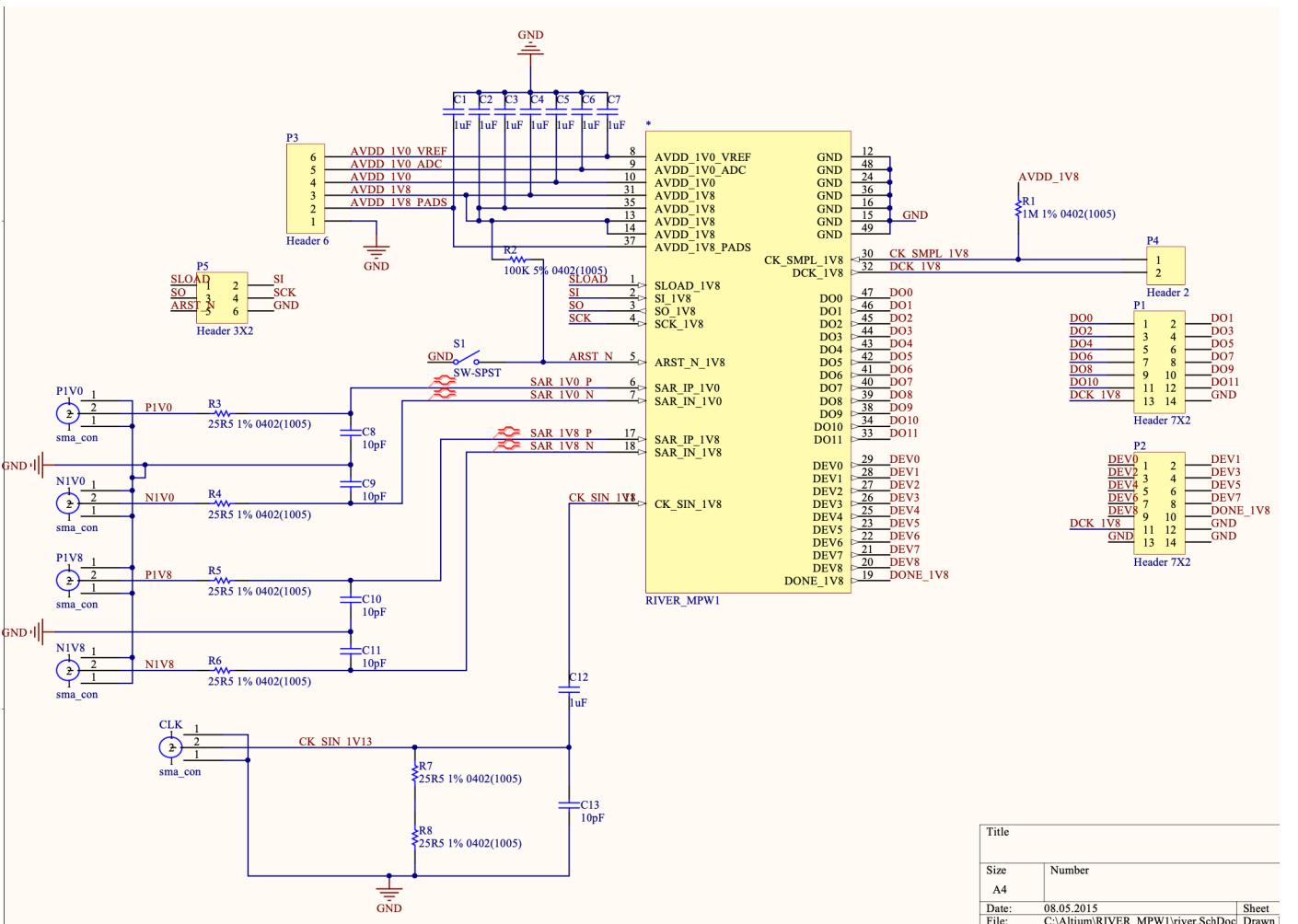
How

- What does the use case require?
- What IC do we need?
- How is it connected to the real world?
- What pins do we need?
- What states are there?



HOW

Printed Circuit Board (PCB)



- Many, many vendors
- I know Ph.D that students have used [PCBway](#)
- Omega Verksted probably know best option
- Use [Altium](#) to design the PCB

Package and Test

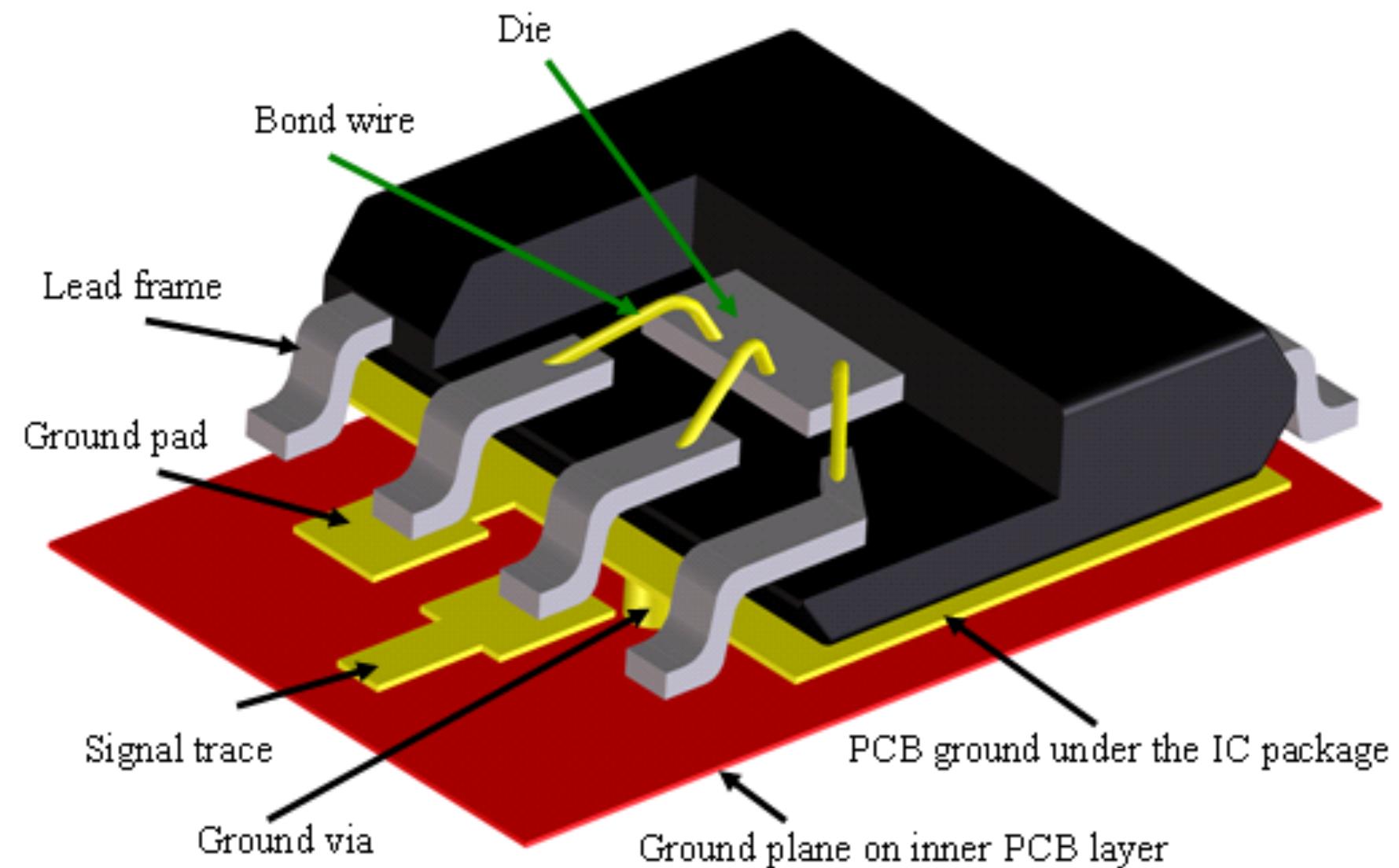


Many package options

Usually done by OSATS (Outsourced Semiconductor Assembly and Test)

www.amkor.com

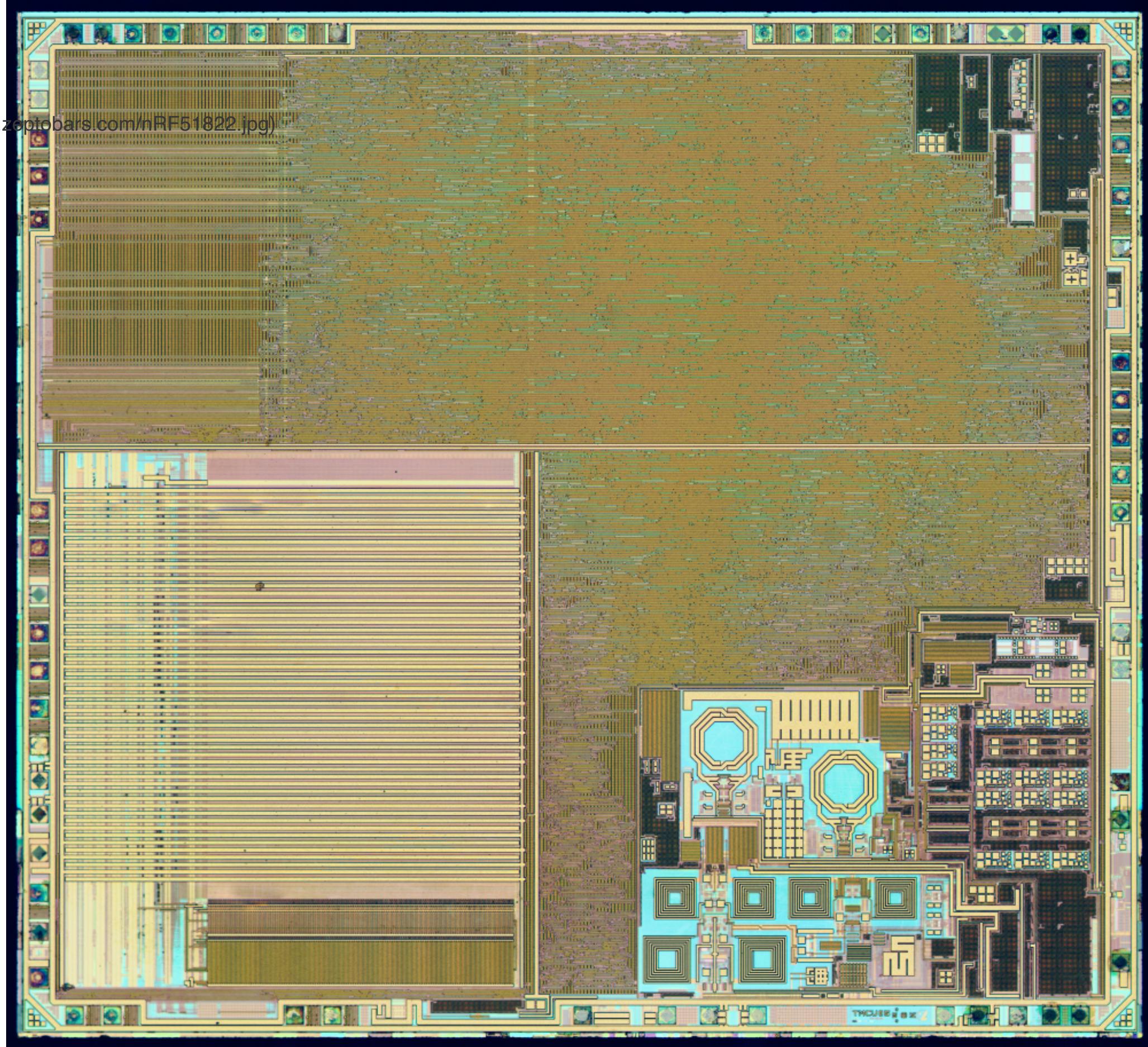
ase.aseglobal.com



Online, <https://www.iue.tuwien.ac.at/phd/poschalko/img410.png>

Die

Picture: nRF51822 (<https://s.zeptobars.com/nRF51822.jpg>)

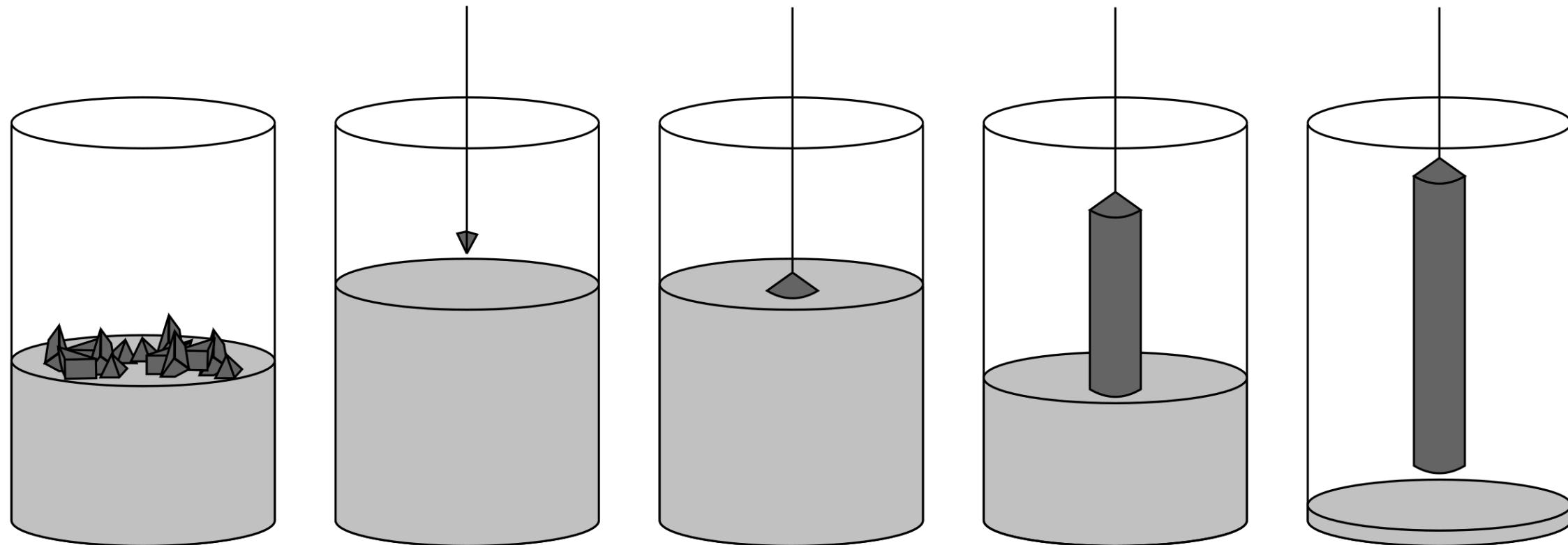


Who makes dies?

- TSMC, Globalfoundries, Samsung, UMC, SMIC ...
- Extremely high initial cost (k\$ to M\$)
- Low production cost (<< \$ per mm²)
- Sam Zeloof, made one in his garage <https://www.youtube.com/watch?v=IS5ycm7VfXg&t=3>

Wafer

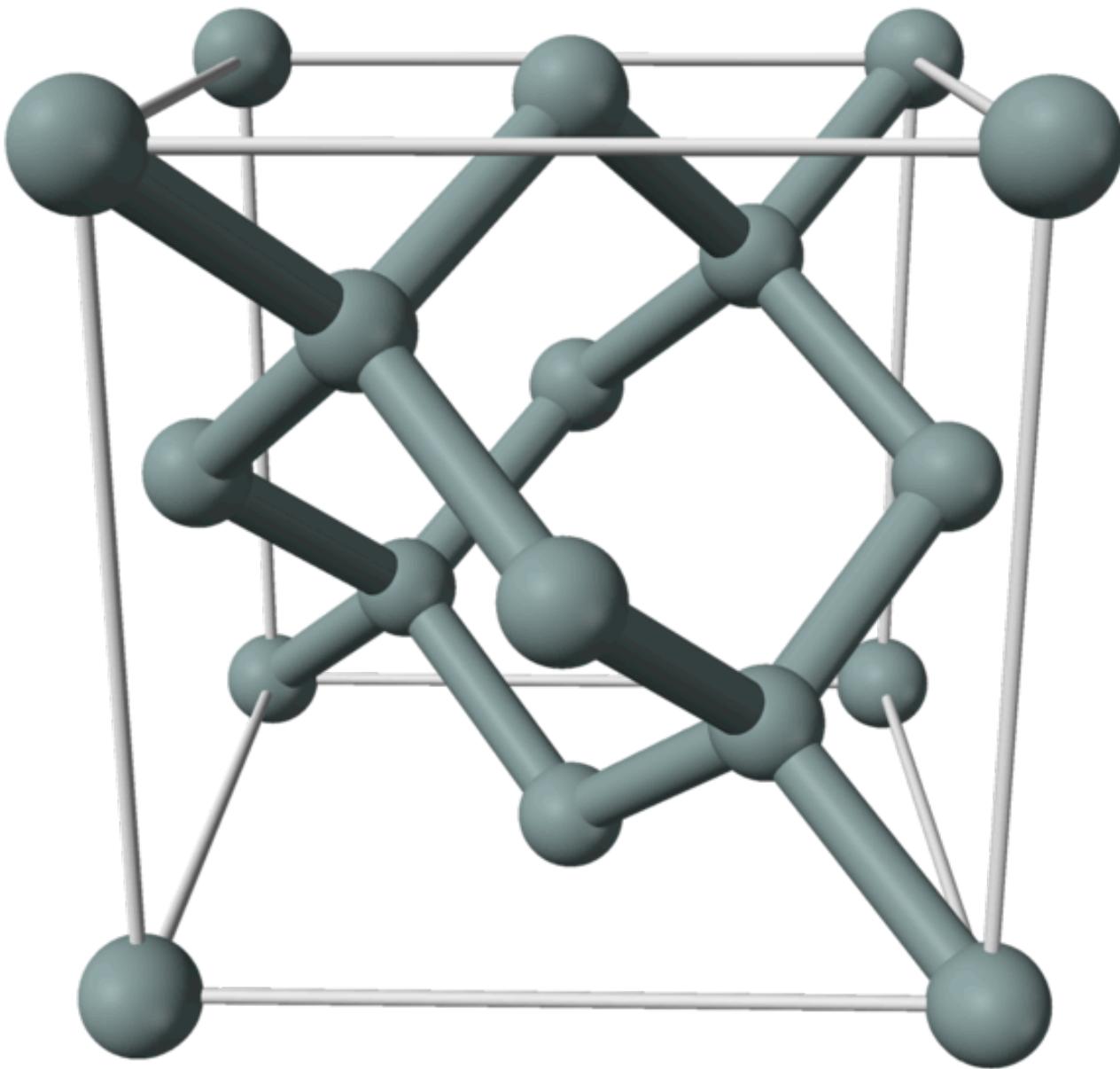
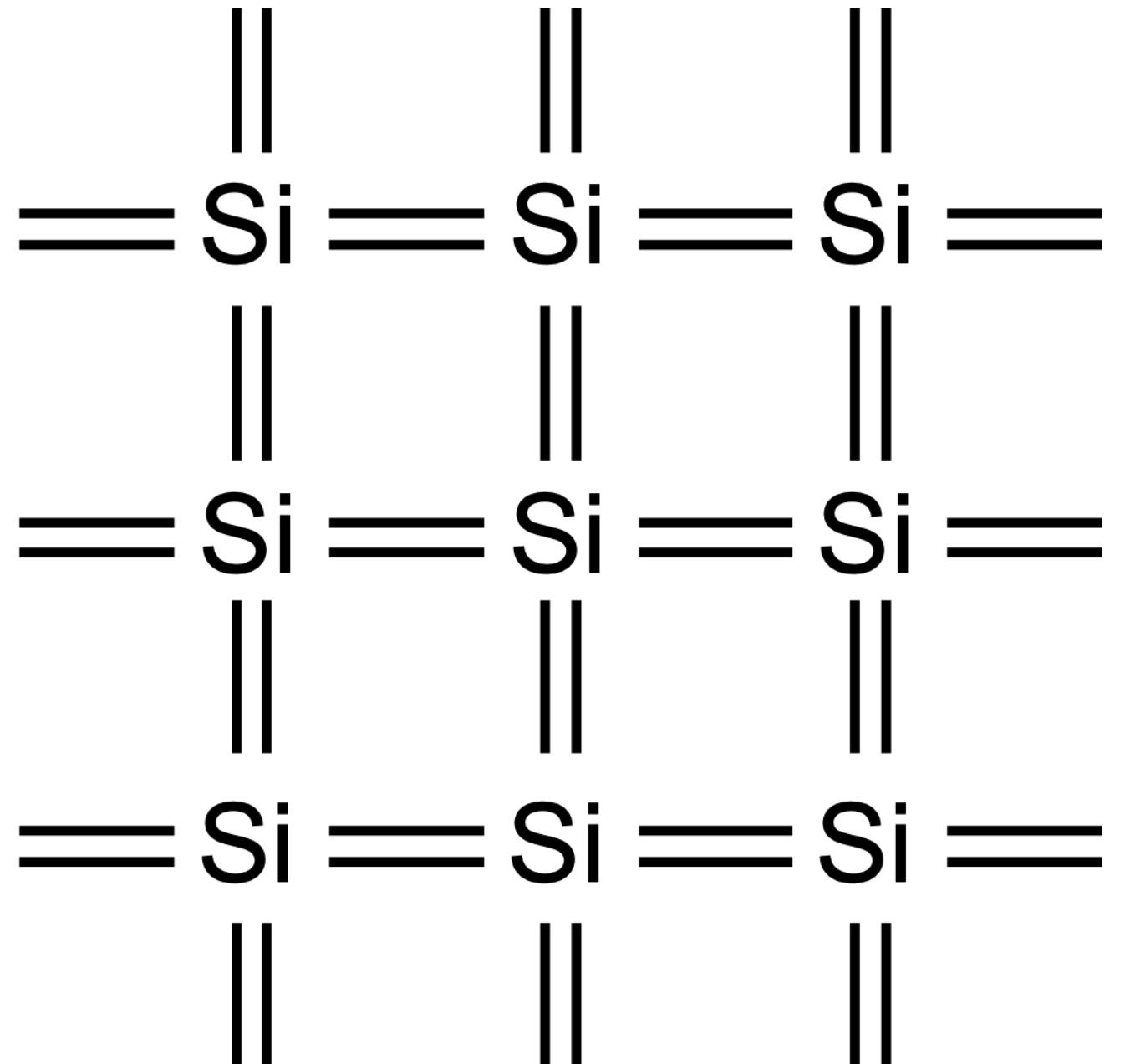
Ingot created with Czochralski Process



Quantum Bound States

Everything should be made as simple as possible, but no simpler. (A. Einstein)

Crystal lattice



Photolithography



ArFr light source: 193 nm

Resolution: < 38 nm

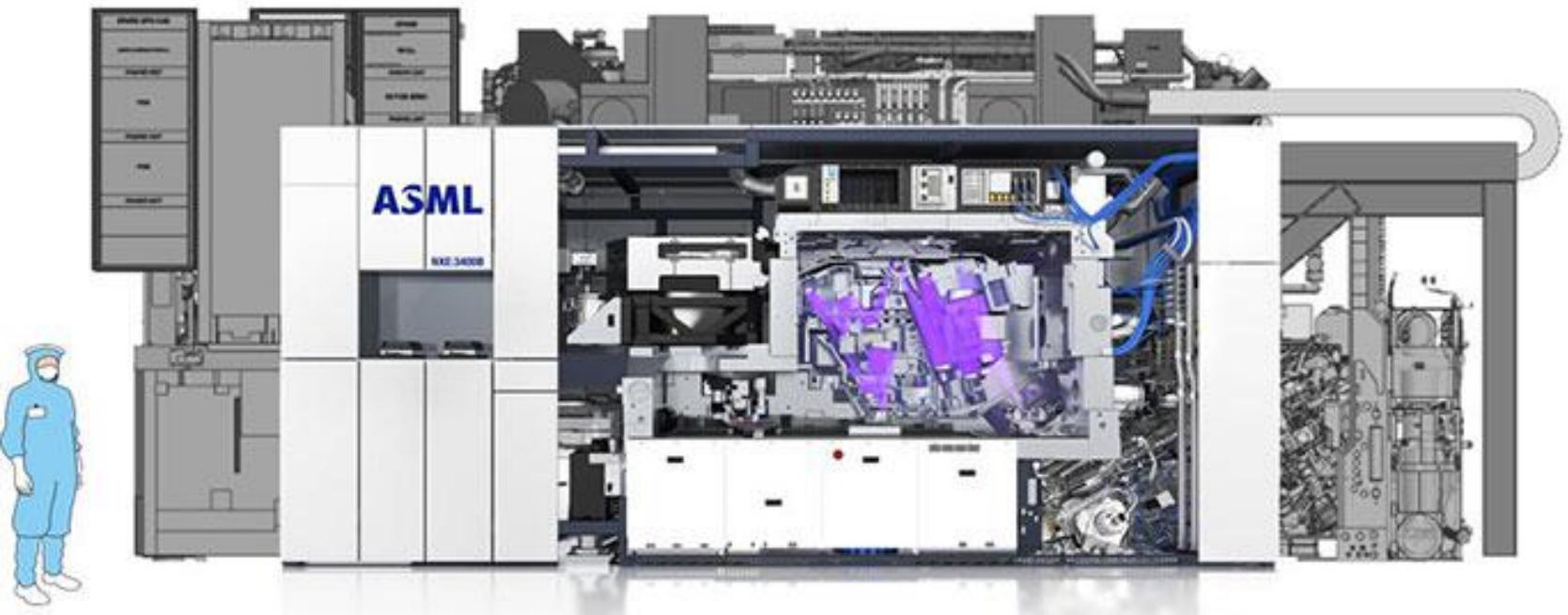
Wafers per hour: > 250

Overlay: < 2.0 nm

Price: Don't know. Maybe 100 M\$?

[https://www.youtube.com/watch?
v=ShYWUIJ2FZs](https://www.youtube.com/watch?v=ShYWUIJ2FZs)

EUV lithography



Light source : 13.5 nm

Resolution : ??

Wafers per hour : 100 ??

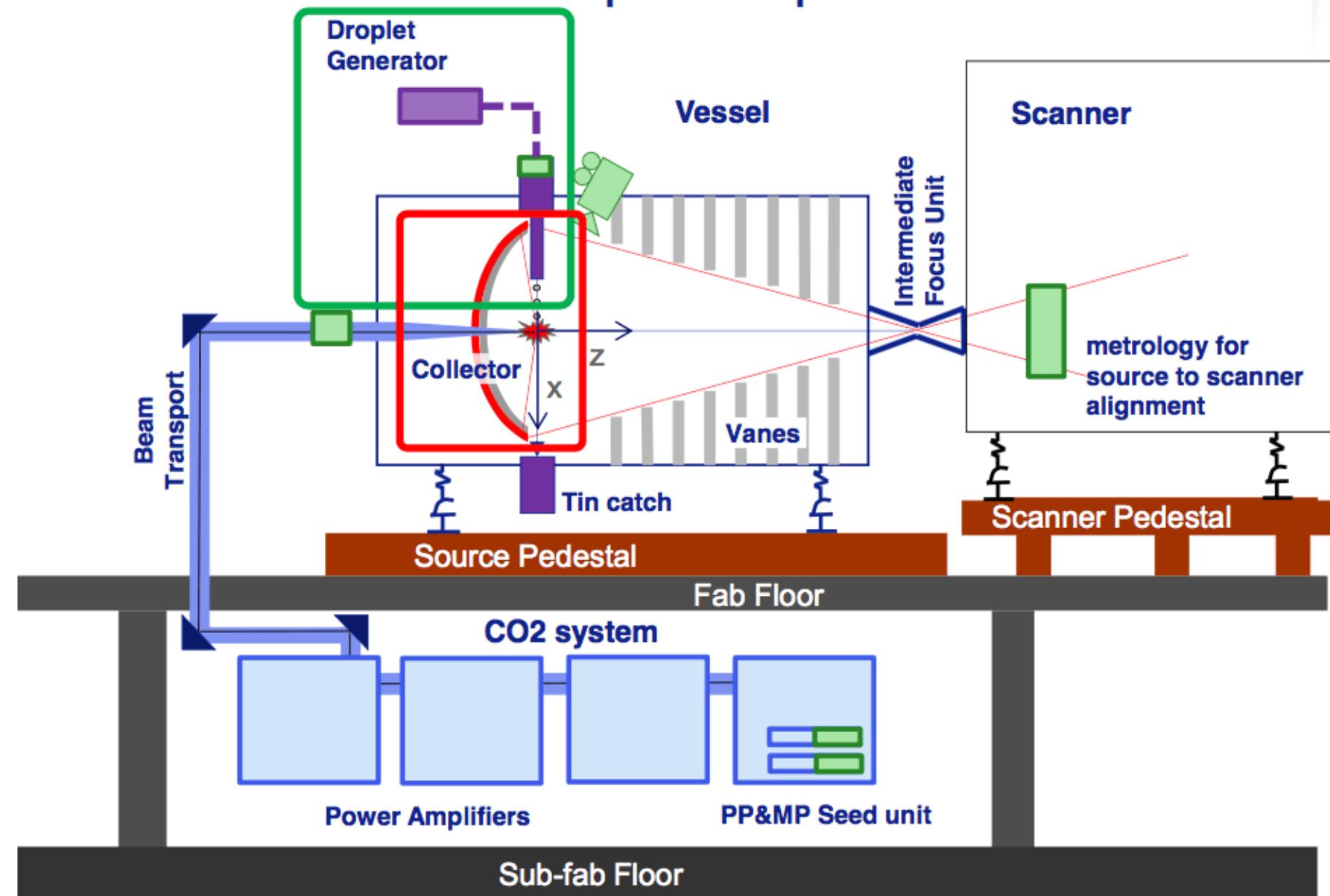
Price: ???

$$E = hf = hc/\lambda, \text{ where } h = 4.1e - 15eV/Hz \text{ and } c = 3e8$$

Wavelength [nm]	Energy [eV]
1000	1.2
240	5.1
193	6.4
90	13.6
13.5	91.1

Seems like the highest known band gap is about 13.5 eV (Lithium Fluoride)

EUV Source - Principle of operation



Online, <https://i1.wp.com/semiengineering.com/wp-content/uploads/2016/11/Screen-Shot-2016-11-15-at-4.04.00-PM.png?w=953&ssl=1>

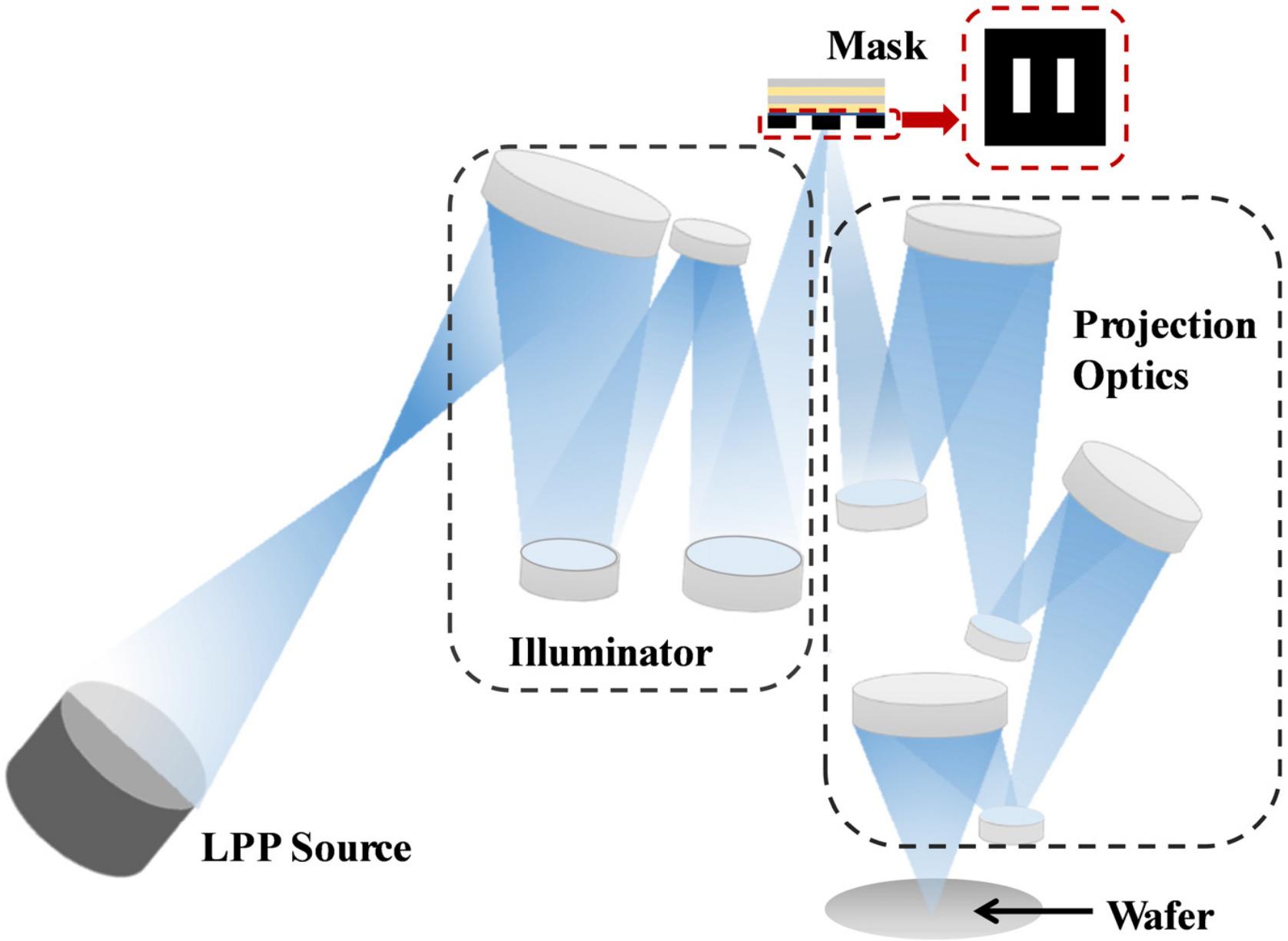


Fig. 1

Citation

Jiaxin Lin, Lisong Dong, Taian Fan, Xu Ma, Yayı Wei, Tianchun Ye, "Learning-based compressive sensing method for EUV lithographic source optimization," *Opt. Express* **27**, 22563-22581 (2019);

<https://www.osapublishing.org/oe/abstract.cfm?URI=oe-27-16-22563>

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Add stuff

Thermal oxidation

Chemical vapor deposition

Atomic layer deposition

Ion implantation

Diffusion

Electroplating

Remove stuff

Etching

Chemical Mechanical Polish

RCA clean

Diffusion

Diffusion Selfaligned MOST; A New Approach to High Speed Devices, 1969

Complementary DMOS Process for LSI

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 4, AUGUST 1976

4-1 Diffusion Selfaligned MOST; A New Approach for High Speed Device.

電試 (田無)

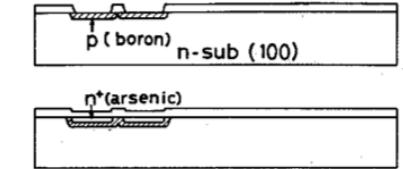
垂井 康夫・林 豊・関川 敏弘

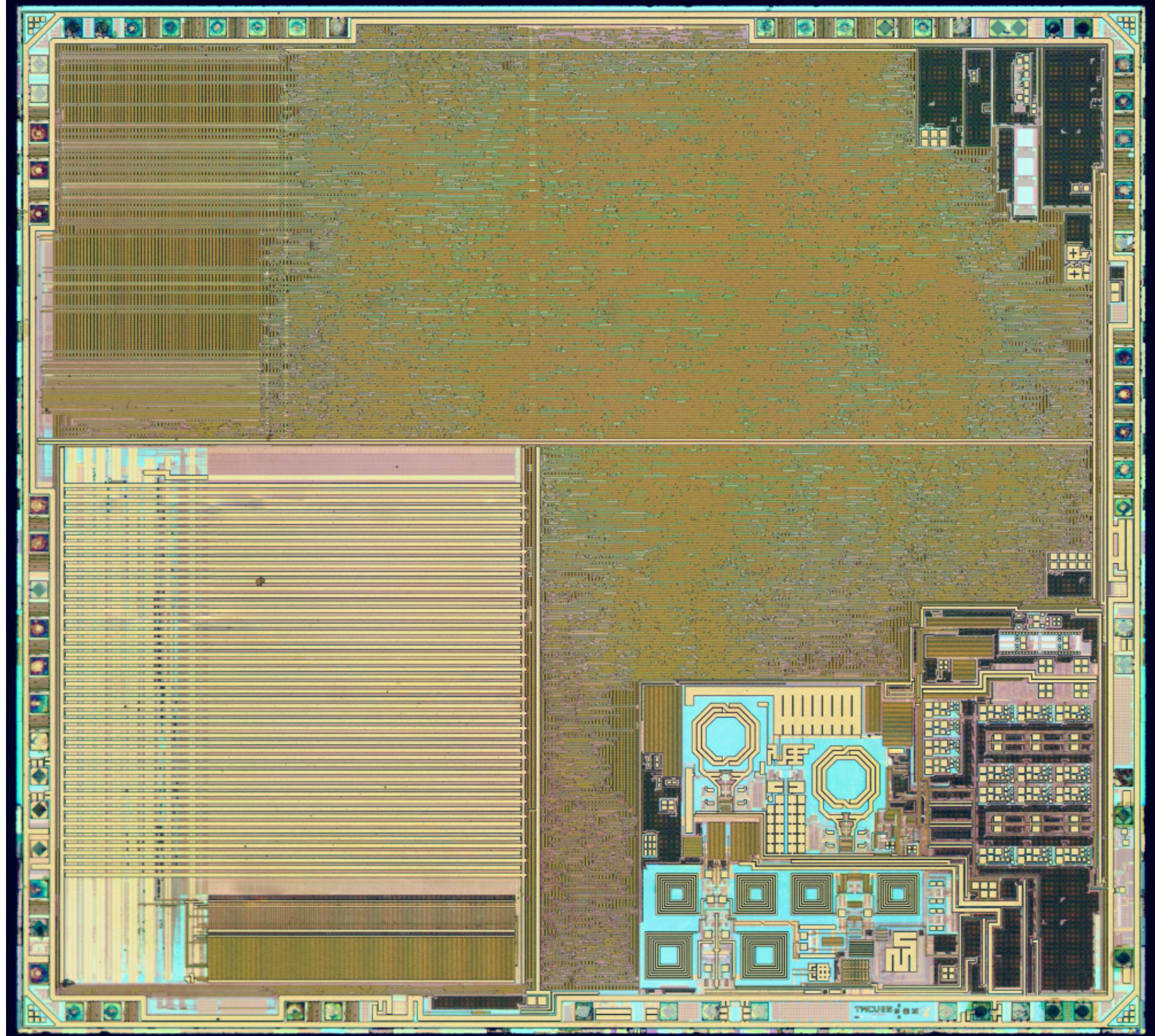
電界効果型トランジスタは現在ではその動作周波数はバイポーラ型トランジスタ
に比べてはるかに遅い。そこで著者は、自らの開発した新しい方法によって、
この問題を解決するための新しい技術を開発した。

Complementary DMOS Process for LSI

TOSHIAKI MASUHARA, MEMBER, IEEE, AND RICHARD S. MULLER, SENIOR MEMBER, IEEE

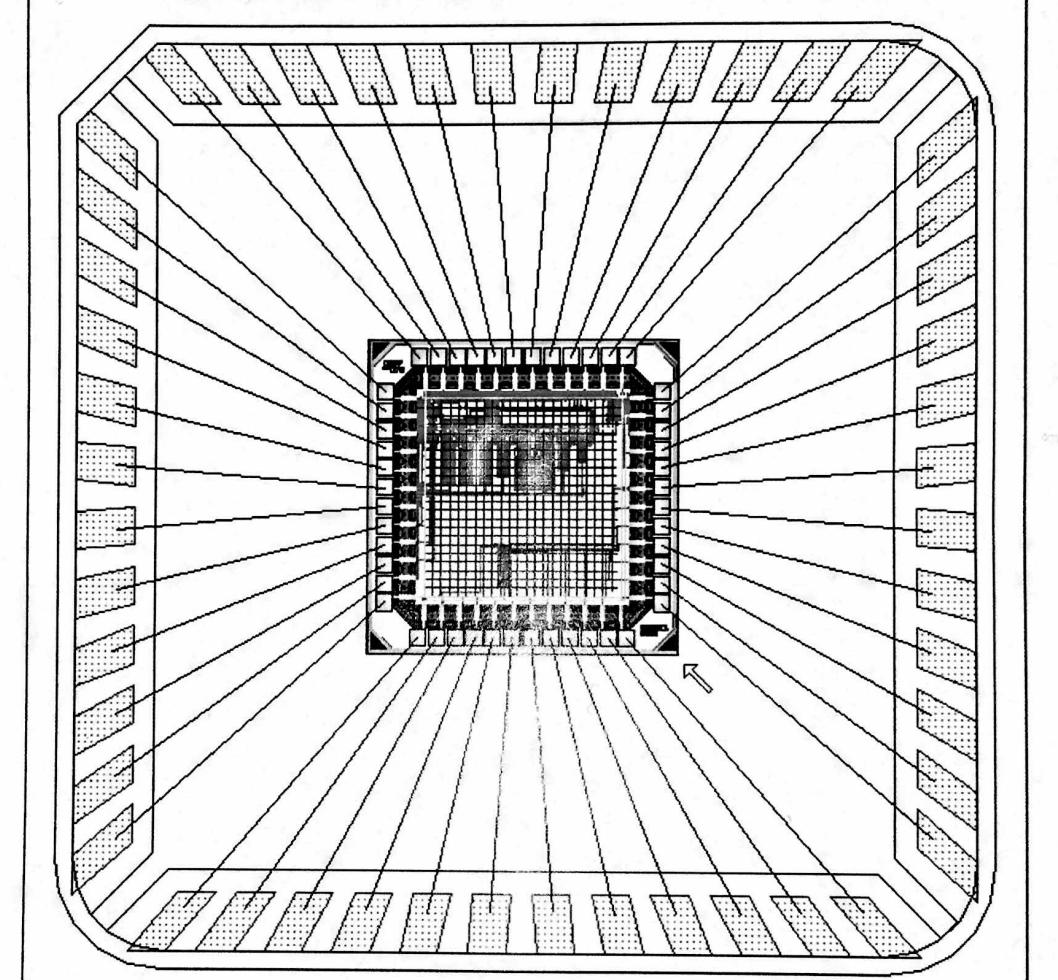
*Abstract—*This paper describes a new complementary metal-oxide semiconductor (CMOS) integrated circuit technology that utilizes a symmetrical double-diffused n-channel transistor. The features of the technology are the use of five masks, a self-aligned p-well diffusion and short channel n-MOS transistors. This results in a fifty percent reduction in p-well area as compared to conventional CMOS devices and lowers processing costs.





Wat

OK Carsten Wulff 2015-02-27

Remarks ↗ Arrow to the circuit name CMP28I151C5 (Right bottom corner of the circuit)	QFN48 6mm x 6mm										
48											
1											
<table border="1"><tr><td>Run S28I15_1</td><td>Date 24 February 2015</td></tr><tr><td colspan="2">Circuit CMP28I151C5 (RIVER_MPW1)</td></tr><tr><td>Sample Qty 15</td><td>Scale 10</td></tr><tr><td>Lid removable <input type="checkbox"/></td><td>Sealed <input checked="" type="checkbox"/></td></tr><tr><td>wire: free</td><td>Die attach</td></tr></table>		Run S28I15_1	Date 24 February 2015	Circuit CMP28I151C5 (RIVER_MPW1)		Sample Qty 15	Scale 10	Lid removable <input type="checkbox"/>	Sealed <input checked="" type="checkbox"/>	wire: free	Die attach
Run S28I15_1	Date 24 February 2015										
Circuit CMP28I151C5 (RIVER_MPW1)											
Sample Qty 15	Scale 10										
Lid removable <input type="checkbox"/>	Sealed <input checked="" type="checkbox"/>										
wire: free	Die attach										
<p>CMP Circuits Multi-Projets Multi-Project Circuits 46, avenue Felix Viallet 38031 GRENOBLE (FRANCE) http://cmp.imag.fr/</p>											

Back Forward Select Move Ruler (Default)

Cells

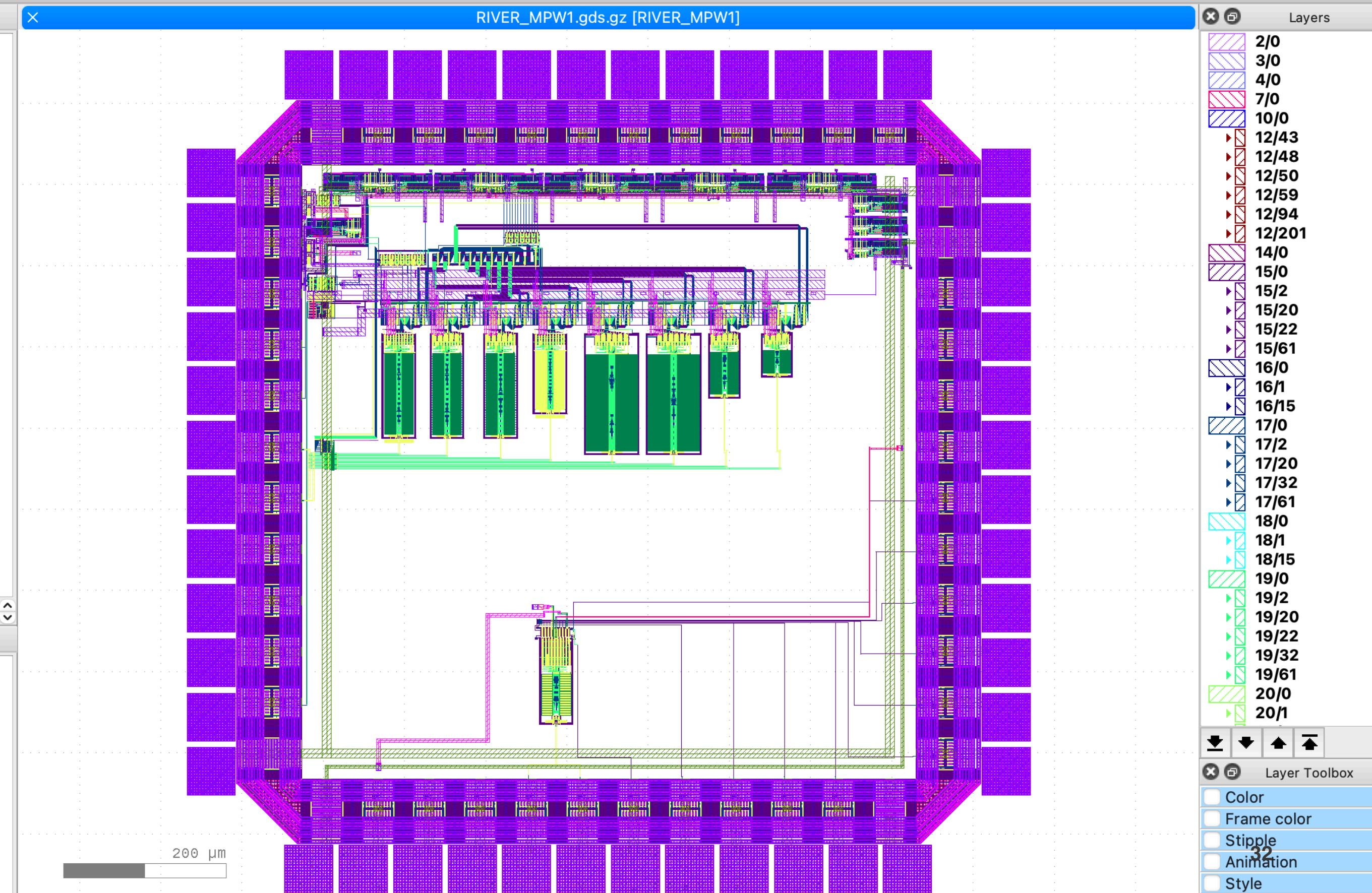
- ANA_CONNECT_B2B_DIODES_ESDSUB
- ANA_CONNECT_ESDSUB_FC_LIN
- ANA_CONNECT_IO_UHF_FC_LIN
- ANA_CONNECT_SUPPLY_1V8_GNDE
- ANA_CONNECT_SUPPLY_1V8_VDDE
- ANA_ESDSUB_RAILS
- ANA_M2_SHORT_RAIL
- ANA_MTOP_UHF
- ANA_UHF_FLEXFRAME_FLAT
- ANA_VIA4X_2X12
- ANA_VIA4X_2X2
- ANA_VIA4_2X12
- ANA_VIA4_2X4
- ANX1_CV
- ANX1_EV
- BASE_WB_6U1X2U2X2T8xLB
- BFX12_10B_CV
- BFX12_CV
- BFX1_CV
- C1N1M16F4C_EV
- C1N3M6F12C_EV
- C1P1M6F12C_CV
- C1P1M6F12C_EV
- CAP
- CAP32C_CV
- CAP32C_CV_0

Levels 0 .. 10

Libraries

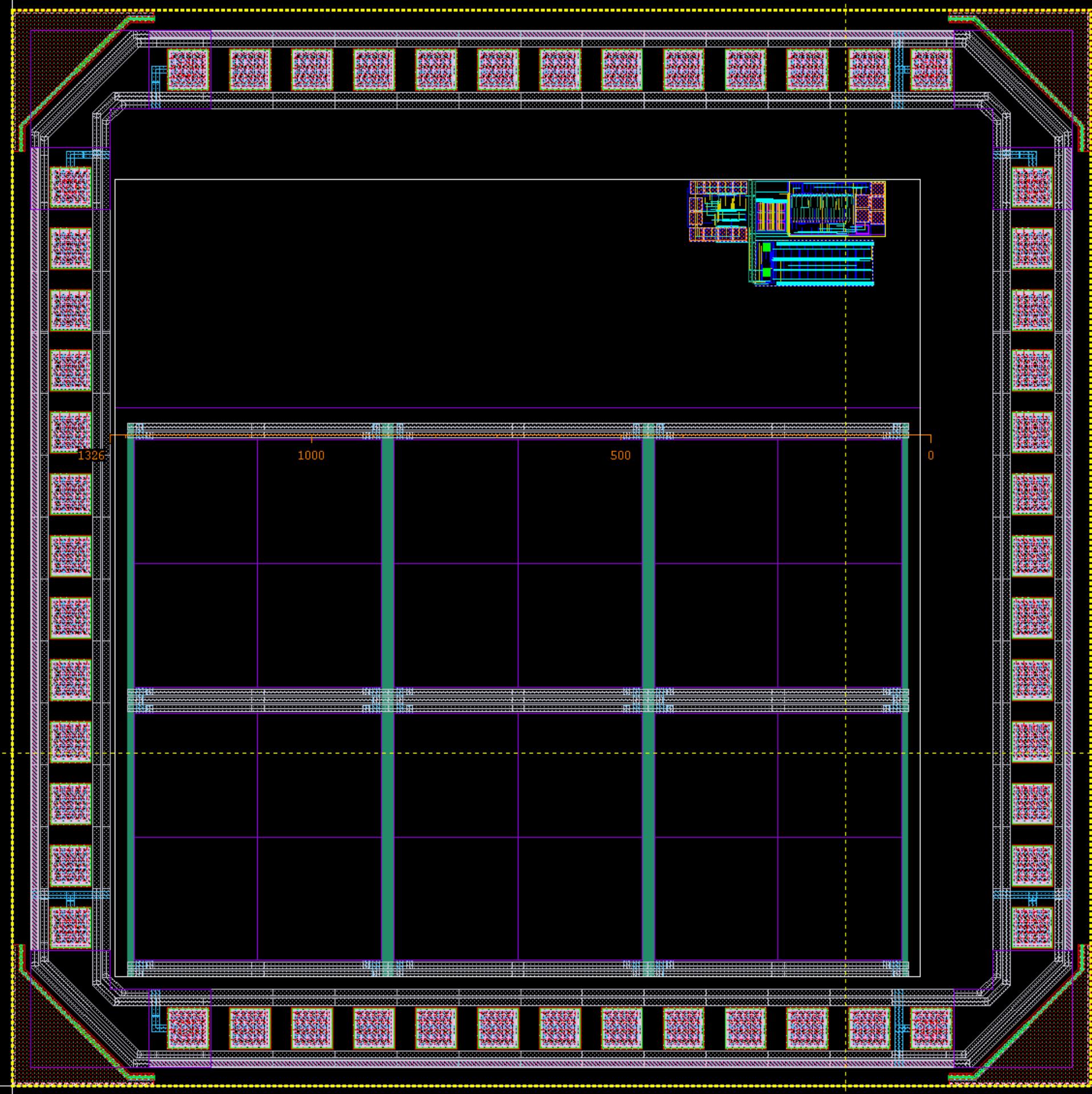
- ARC
- CIRCLE
- DONUT
- ELLIPSE
- PIE
- ROUND_PATH
- ROUND_POLYGON
- STROKED_BOX
- STROKED_POLYGON
- TEXT

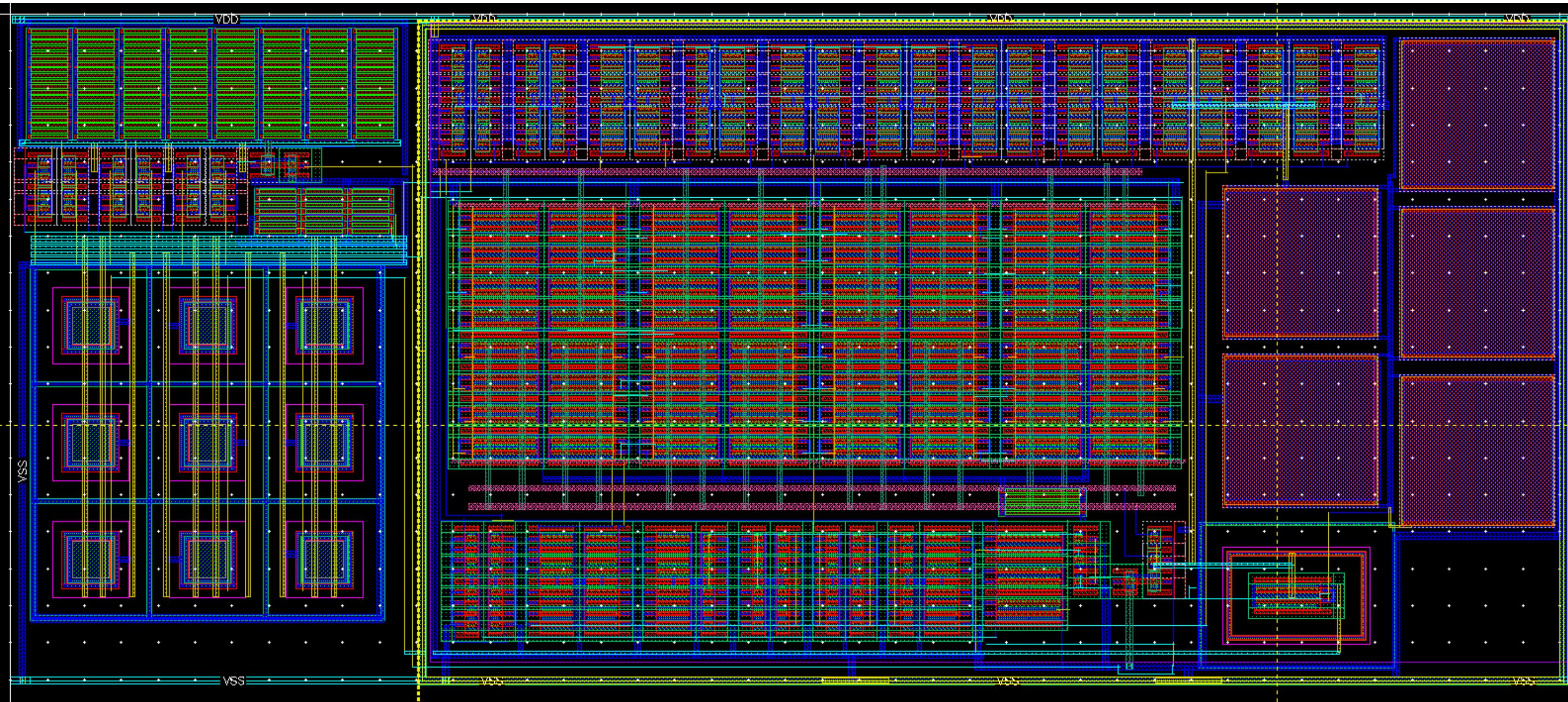
Carsten Wulff 2021

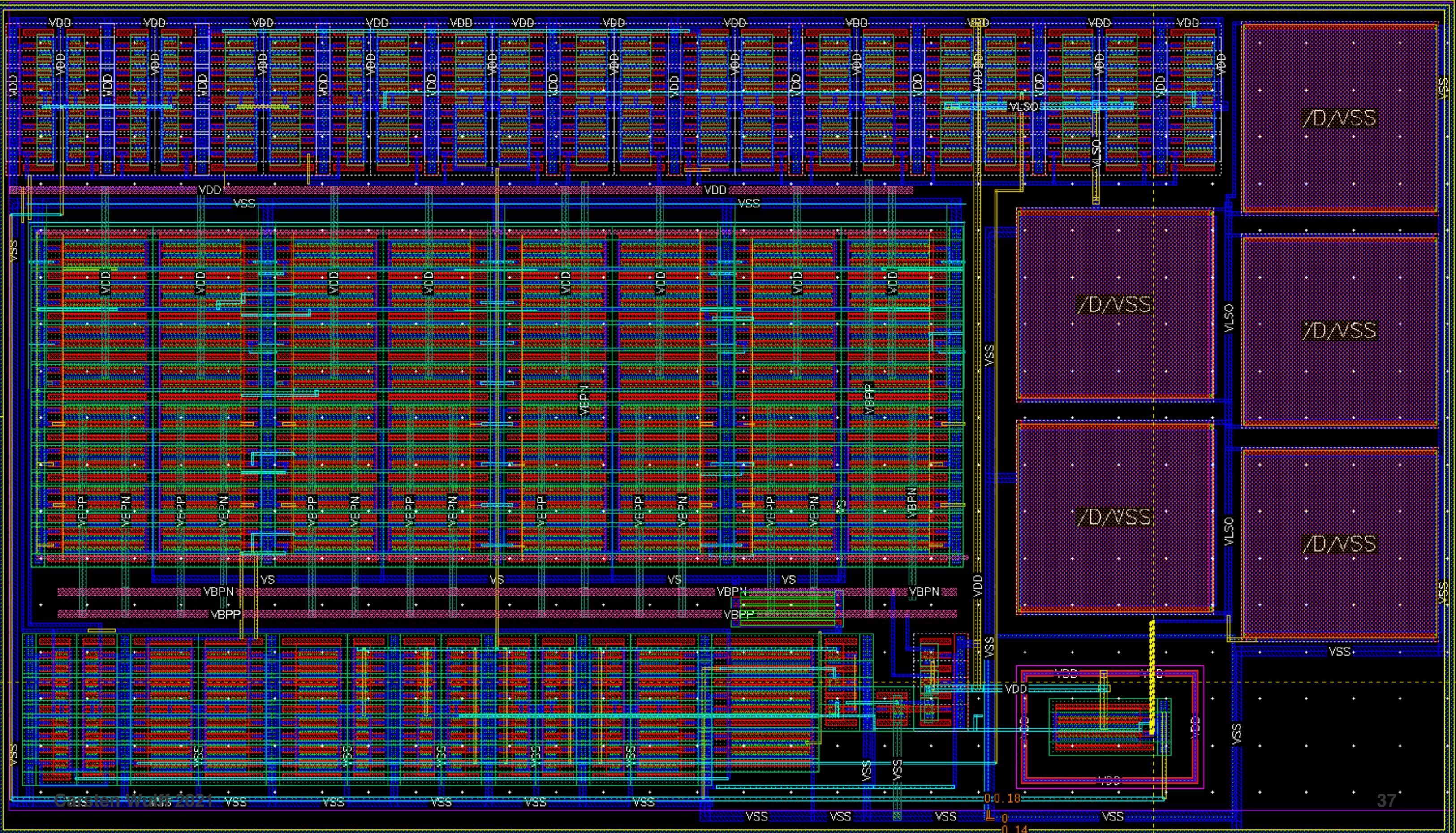


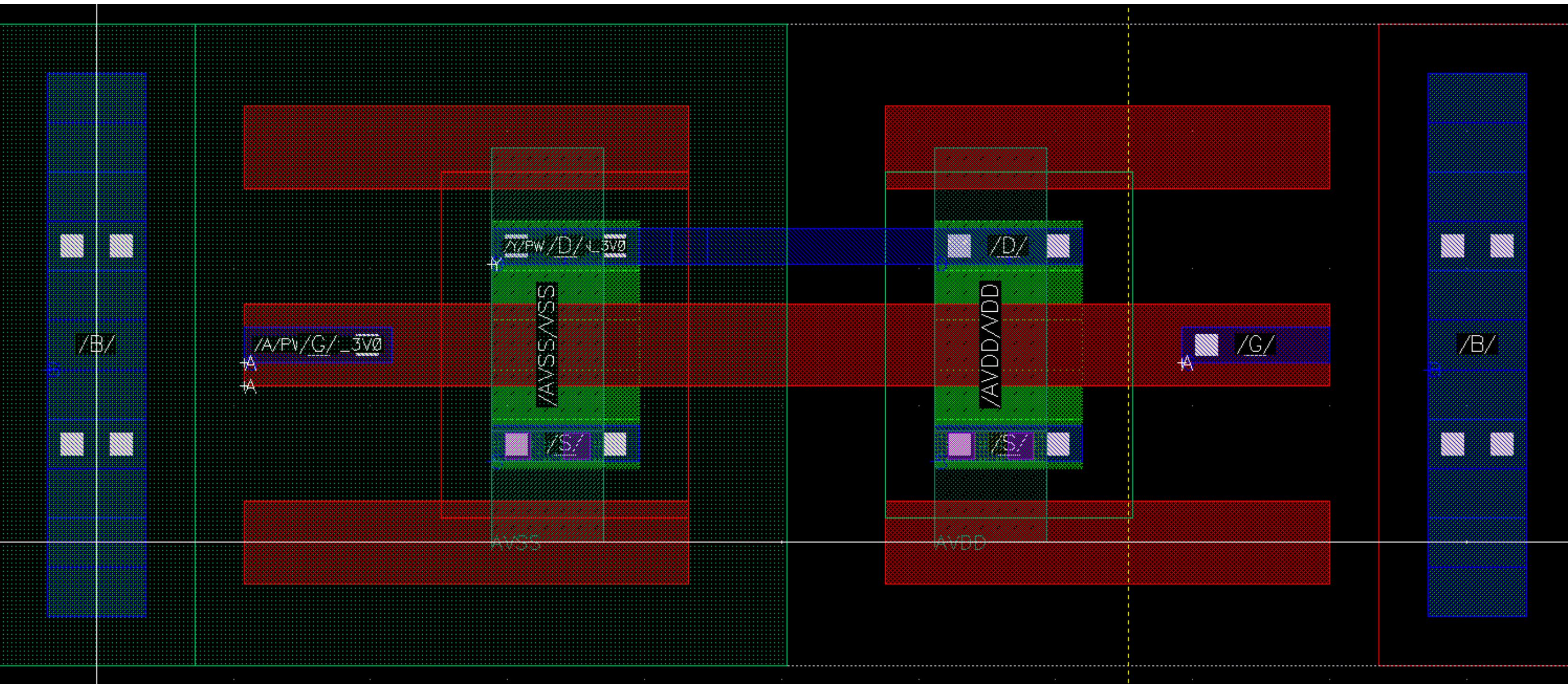
How do we go from idea to GDSII?

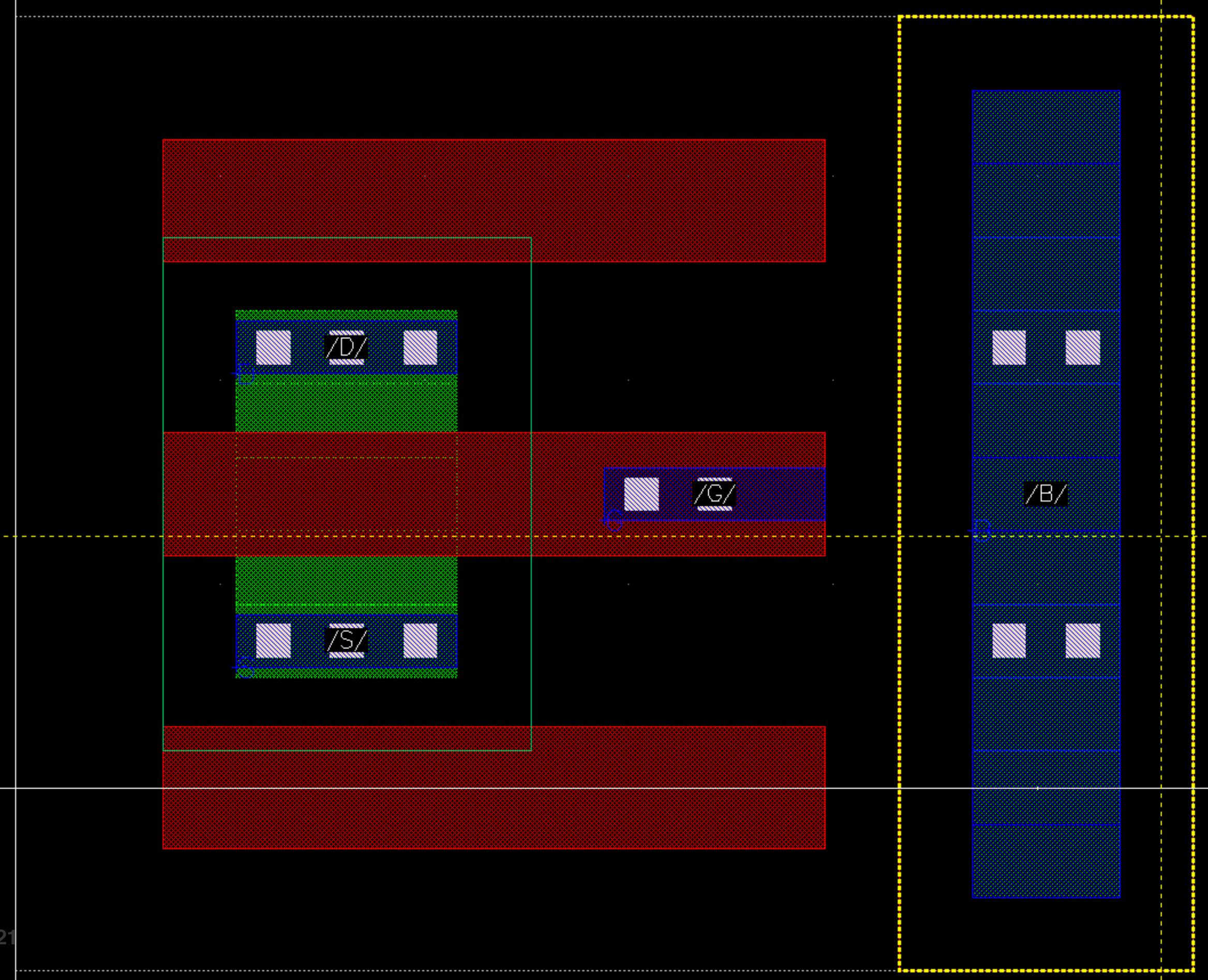
layout





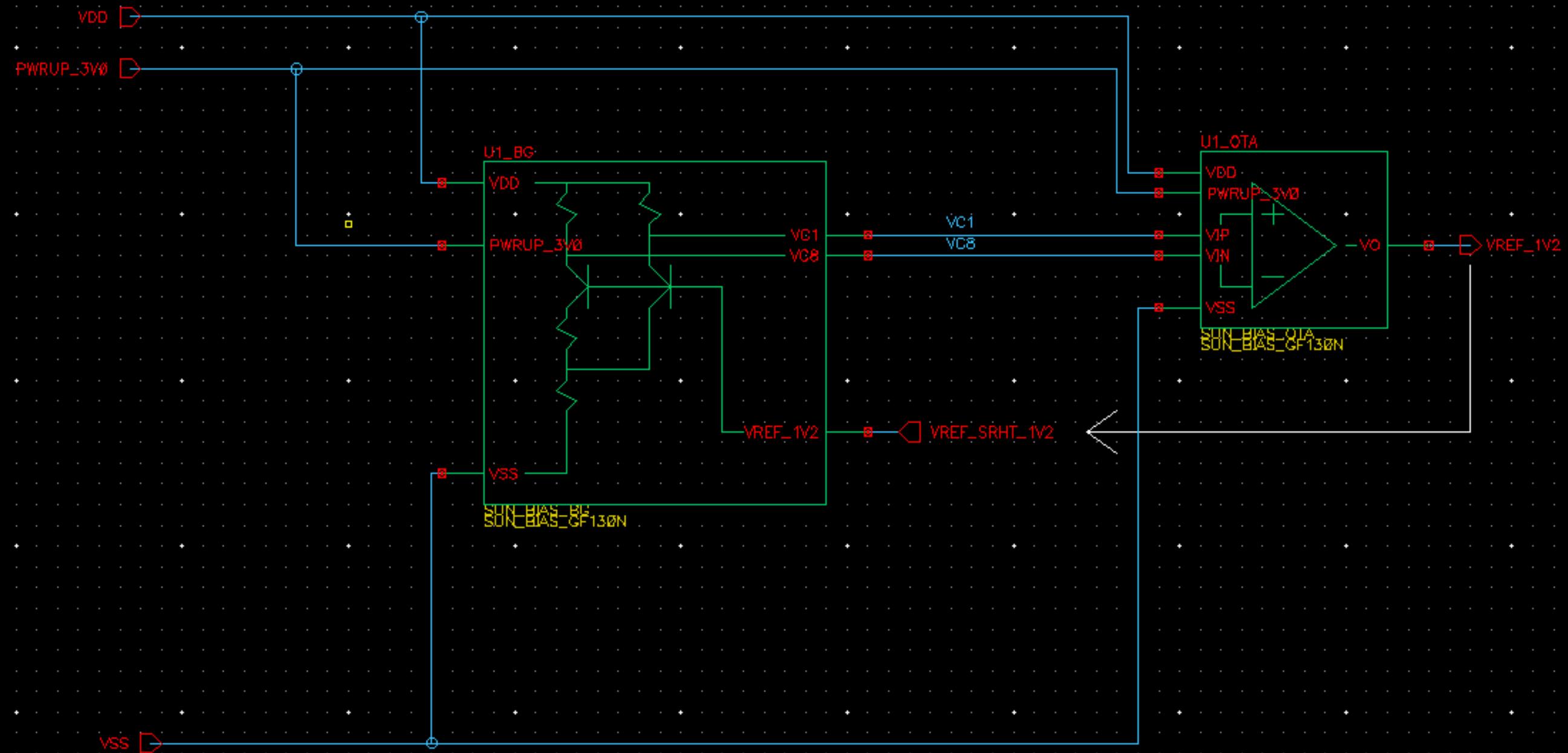






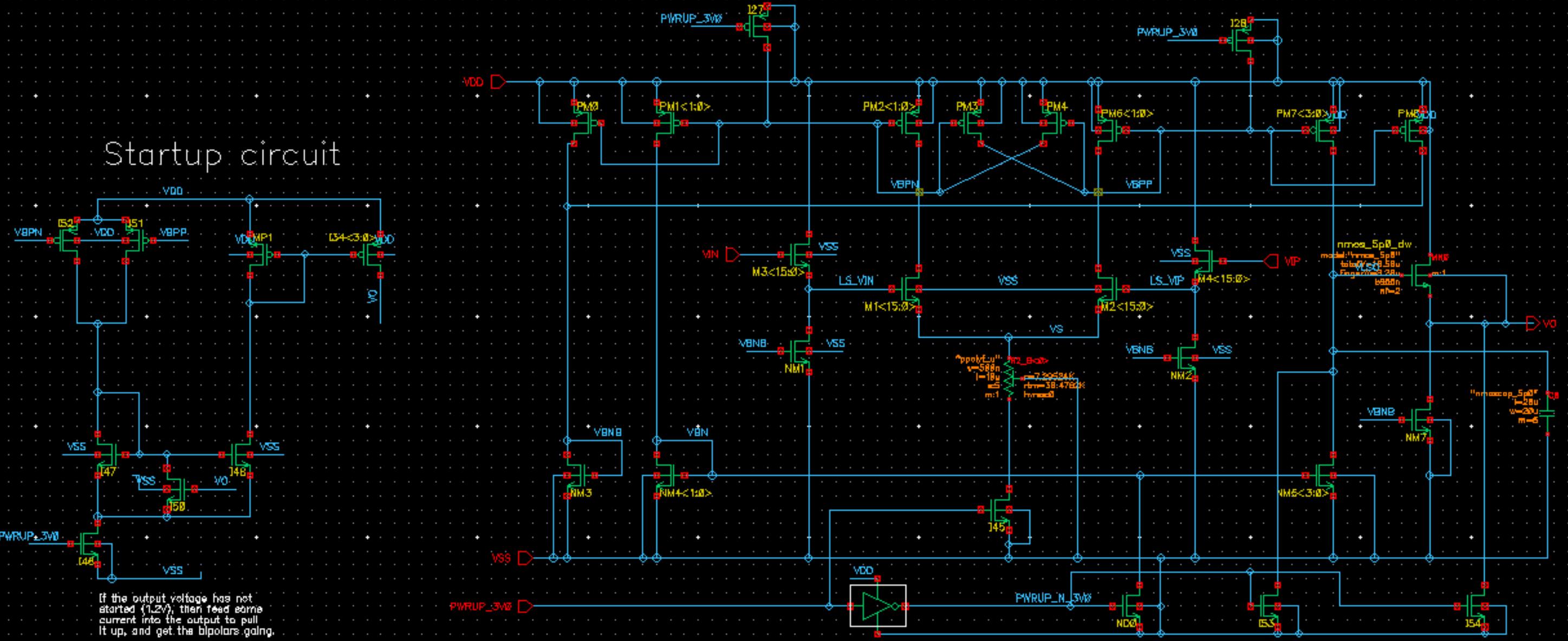
Design

Bandgap CORE



Current mirror OTA with level shifter input, positive feedback, and source follower buffer

Startup circuit



SUN_BIAS OTA	
Designer	wulff
Created	Mar 12 16:08:21 2021
Modified	Jun 19 13:13:13 2021
copyright	NTNU

AVSS



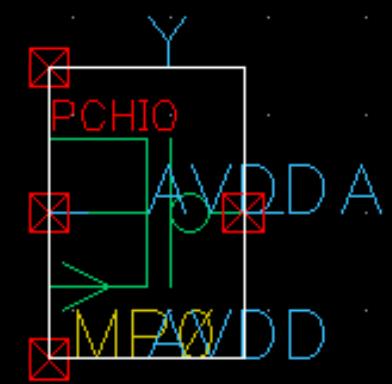
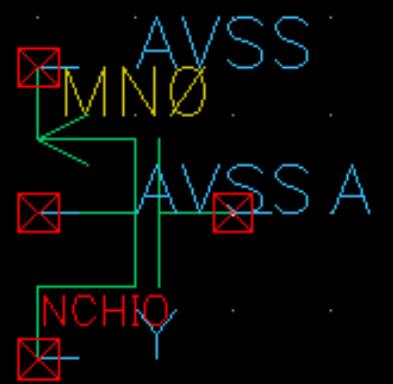
AVDD

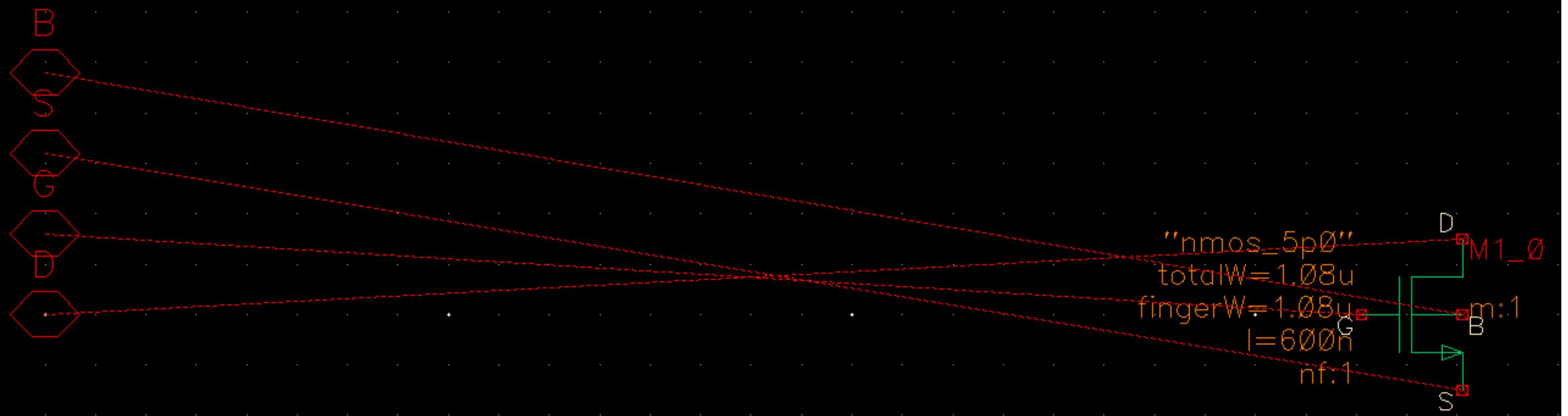


A



AVSSA





```

module counter(out, clk, reset);                                /* Generated by Yosys 0.9 (git sha1 1979e0b) */

    parameter WIDTH = 8;

    output [WIDTH-1 : 0] out;
    input      clk, reset;

    reg [WIDTH-1 : 0]   out;
    wire      clk, reset;

    always @ (posedge clk or posedge reset)
        if (reset)
            out <= 0;
        else
            out <= out + 1;

endmodule // counter

```

<https://github.com/wulffern/dicex/tree/main/sim/verilog/counter>

```

(* dynports = 1 *)
(* top = 1 *)
(* src = "counter.v:1" *)
module counter(out, clk, reset);
(* src = "counter.v:11" *)
wire [7:0] _00_;
...
input reset;
NOT _51_ (
    .A(_43_),
    .Y(_09_)
);
...
DFFSR _92_ (
    .C(clk),
    .D(_00_[7]),
    .Q(out[7]),
    .R(reset),
    .S(1'h0)
);
assign _43_ = out[0];
assign _44_ = out[1];
assign _45_ = out[2];
assign _00_[2] = _11_;
assign _46_ = out[3];
assign _00_[3] = _12_;
assign _47_ = out[4];
assign _00_[4] = _13_;
assign _48_ = out[5];
assign _00_[5] = _14_;
assign _49_ = out[6];
assign _00_[6] = _15_;
assign _50_ = out[7];
assign _00_[7] = _16_;
assign _00_[0] = _09_;
assign _00_[1] = _10_;
endmodule

```

Simulation

Virtuoso® ADE Assembler Reading: TB_SUN_BIAS_GF130N TB_SUN_BIAS maestro

Launch File Create Tools Options Run EAD Parasitics/LDE Window Calibre Help

cadence

No Parasitics/LDE No Sweeps Monte Carlo Sampling Reference:

Data View

- Sch_mc
- Sch_typ_istb_pwrdown
- Sch_etc_istb_pwrdown
- Sch_etc_main
- Sch_typical**
- Interactive.7
- Interactive.8
- Interactive.9
- Interactive.10
- Interactive.11
- Interactive.12
- Interactive.13
- Interactive.14
- MonteCarlo.0
- Ocean.0

Outputs Setup

Parameter	typical
bjt.scs	Bt
cap.scs	Ct
common.scs	Gt
diode.scs	Dt
mos.scs	Mtt
res.scs	Rt
supply.scs	Vt
temperature	t_temp
temperature.scs	Tt

85 rows

Test	Output	Spec	Weight	Pass/Fail	Min	Max	typical
MAIN	w_irref						
MAIN	w_vref						
MAIN	w_ibpsr						
MAIN	ibpsr_ymax	range 0.7u 1.3u		pass	1.039u	1.039u	1.039u
MAIN	inom_ymax				-6.156m	-6.156m	-6.156m
MAIN	vref_typ	range 1.17 1.23		pass	1.208	1.208	1.208
MAIN	w_vref_buff						
MAIN	vref_buff_typ	range 1.17 1.23		pass	1.202	1.202	1.202
MAIN	ibpsr_typ	range 0.7u 1.3u		pass	1.036u	1.036u	1.036u
MAIN	inom_typ				-5.942m	-5.942m	-5.942m
MAIN	ibpsr_ymin	range 0.7u 1.3u		pass	1.024u	1.024u	1.024u
MAIN	inom_ymin				-5.996m	-5.996m	-5.996m
MAIN	ibpsr_delta				15.12n	15.12n	15.12n
MAIN	ibpsr_xmax				85.4	85.4	85.4
MAIN	ibpsr_xmin				-40	-40	-40
MAIN	ibpsr_tdelta				125.4	125.4	125.4
MAIN	ibpsr_ppmc	range -200 200		pass	116.4	116.4	116.4
MAIN	vref_ymin	range 1.17 1.23		pass	1.205	1.205	1.205
MAIN	vref_ymax	range 1.17 1.23		pass	1.208	1.208	1.208
MAIN	vref_delta				2.921m	2.921m	2.921m
MAIN	vref_acc				241.8m	241.8m	241.8m
MAIN	vref_buff_ymax	range 1.17 1.23		pass	1.202	1.202	1.202
MAIN	vref_buff_ymin	range 1.17 1.23		pass	1.199	1.199	1.199
MAIN	vref_buff_delta				3.026m	3.026m	3.026m
MAIN	vref_buff_xmax				29.3	29.3	29.3
MAIN	vref_buff_xmin				125	125	125
MAIN	vref_buff_tdelta				-95.7	-95.7	-95.7
MAIN	vref_buff_ppmc	range -100 100		pass	-26.31	-26.31	-26.31
MAIN	vref_xmax				29.3	29.3	29.3
MAIN	vref_xmin				125	125	125

mouse L: (2) Configure what is shown in the table

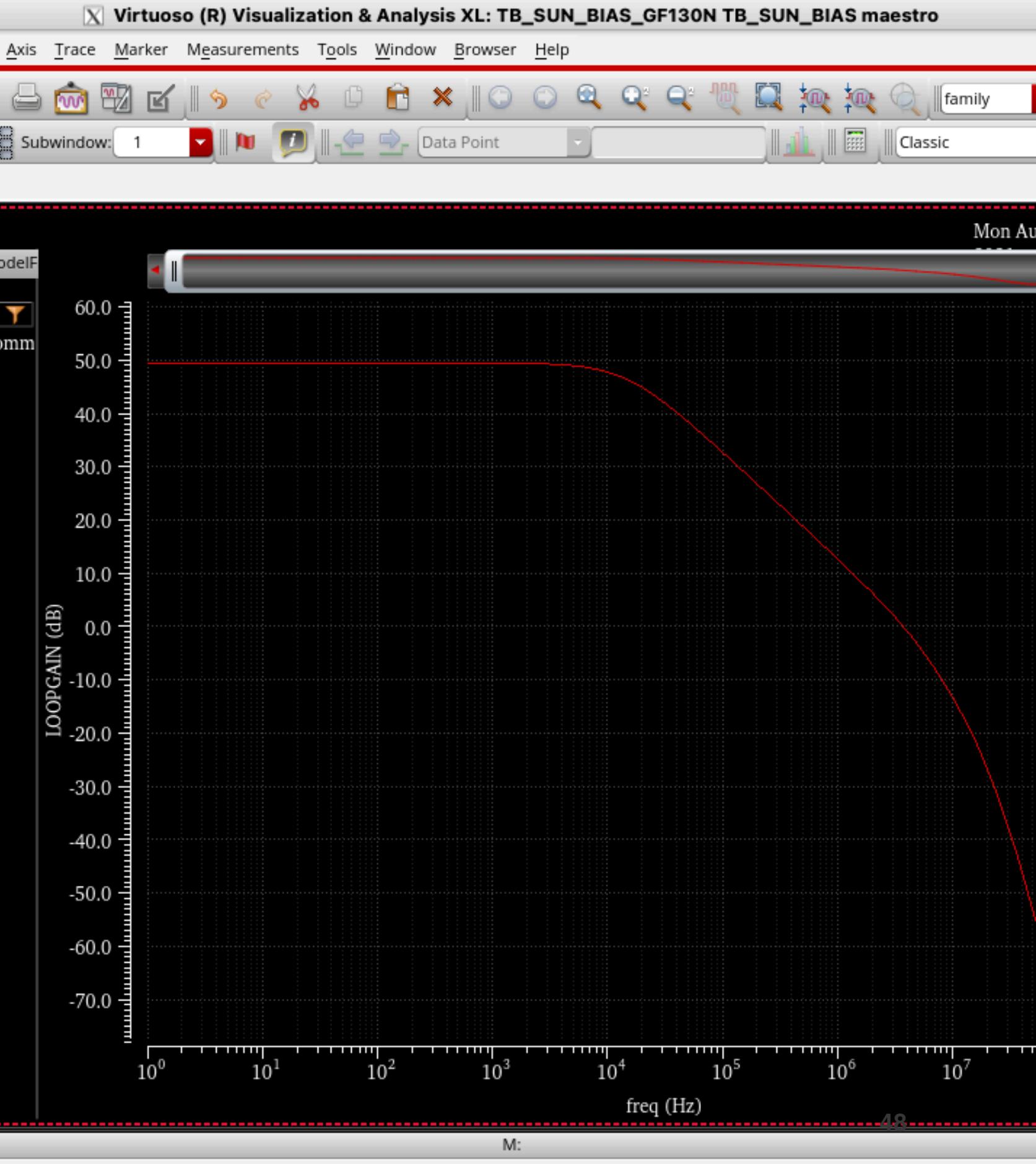
```

// Point Netlist Generated on: Aug 23 08:53:54 2021
// Generated for: spectre
// Design Netlist Generated on: Aug 23 08:53:53 2021
// Design library name: TB_SUN_BIAS_GF130N
// Design cell name: TB_SUN_BIAS
// Design view name: config
simulator lang=spectre
global 0
parameters t_pwrdown=2 t_pwrup=1 pwrup=1 TFALL=100u TRISE=100u vdde=3.0
include "$PROJECT/lib/spectre/common.scs" section=Gt
include "$PROJECT/lib/spectre/mos.scs" section=Mtt
include "$PROJECT/lib/spectre/res.scs" section=Rt
include "$PROJECT/lib/spectre/cap.scs" section=Ct
include "$PROJECT/lib/spectre/temperature.scs" section=Tt
include "$PROJECT/lib/spectre/supply.scs" section=Vt
include "$PROJECT/lib/spectre/bjt.scs" section=Bt
include "$PROJECT/lib/spectre/diode.scs" section=Dt

// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
// Library name: SUN_BIAS_GF130N
// Cell name: SUN_BIAS
// View name: lpe_c_only_coupled
// View type: maskLayout
subckt SUN_BIAS IBPSR_1U\$(25) IBPSR_1U\$(24) IBPSR_1U\$(23) \
    IBPSR_1U\$(22) IBPSR_1U\$(21) IBPSR_1U\$(20) IBPSR_1U\$(19) \
    IBPSR_1U\$(18) IBPSR_1U\$(17) IBPSR_1U\$(16) IBPSR_1U\$(15) \
    IBPSR_1U\$(14) IBPSR_1U\$(13) IBPSR_1U\$(12) IBPSR_1U\$(11) \
    IBPSR_1U\$(10) IBPSR_1U\$(9) IBPSR_1U\$(8) IBPSR_1U\$(7) \
    IBPSR_1U\$(6) IBPSR_1U\$(5) IBPSR_1U\$(4) IBPSR_1U\$(3) \
    IBPSR_1U\$(2) IBPSR_1U\$(1) IBPSR_1U\$(0) PWRUP_3V0 VDD VFBI VFBO \
    VREF_1V2 VREF_BUFF_1V2 VREF_BUFF_1V2_FB VREF_FB VSS
    U1_VI\|R2 (U1_VI\|VS1 U1_VI\|53 VSS) ppolyf_u l=1e-05 w=5e-07 par=1 \
    s=1 m=1 dtemp=0
...
... (~ 8000 lines)

VVDD (VDD VSS) vsource dc=vdde type=pulse val0=0 val1=vdde period=5 \
    rise=TRISE fall=TFALL
V1 (PWRUP_3V0 VSS) vsource dc=pwrup*vdde type=pwl wave=[ 0 0 (t_pwrup) 0 \
    (t_pwrup + 1n) vdde (t_pwrdown) vdde (t_pwrdown + 1n) 0 ]
...

```



```

module counter(out, clk, reset);

parameter WIDTH = 8;

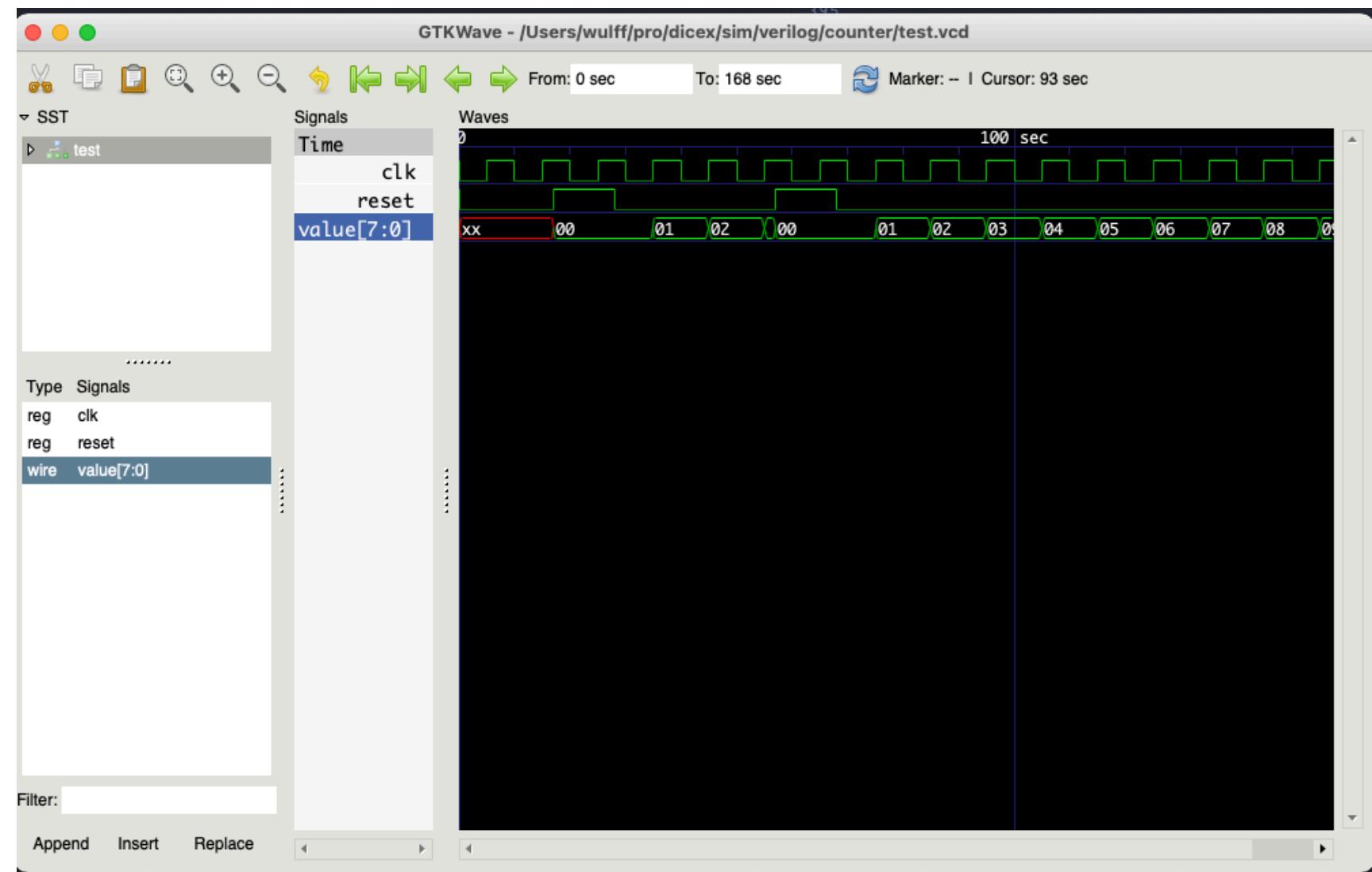
output [WIDTH-1 : 0] out;
input             clk, reset;

reg [WIDTH-1 : 0]   out;
wire              clk, reset;

always @ (posedge clk or posedge reset)
  if (reset)
    out <= 0;
  else
    out <= out + 1;

endmodule // counter

```



Want to learn more?

Preview of Advanced Integrated Circuits

[AIC - Layout](#)

[AIC - Schematic](#)

[AIC - General](#)

[AIC - cheatsheet](#)

Thanks!