# An 8-bit 60-MS/s 8.1mW Differential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology


## Abstract

We present the first differential comparator-based switch capacitor (CBSC) pipelined ADC. The switched-capacitor multiplying digital-to-analog converter (MDAC) use current sources and a comparator to do charge transfer. Continuous time bootstrapped switches are used in the first stage to reduce signal dependent switch resistance. A simple calibration correct for comparator delay variation due to manufacturing. Calibration reduces ramp overshoot, which dominate the non-linearity in CBSC ADCs. The ADC is produced in a 90nm low-power CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.1mW at 60MS/s.


## Introduction

DOWNSCALING of CMOS technology continue to challenge the analog designer. Reduced power supply, due to reliability concerns [1], and reduced transistor output resistance, due to shorter channels [2], lead

to low headroom and low intrinsic gain. As a consequence, high-gain operational amplifiers (opamp), the key component in most switched-capacitor circuits, is hard to design in nano-scale technologies.

Techniques like correlated level shifting [3], open-loop residue amplifiers [4], gain calibration [5], [6] and comparator-based switched capacitor circuits (CBSC) [7] have been developed to either make the opamp easier to design, or replace the opamp completely.

Introduced in [7], CBSC is a completely new approach to switched-capacitor circuits, it replaces the opamp with a comparator and a current source; to demonstrate the technique a prototype 10-bit 8-MS/s 2.5-mW pipelined ADC was presented. A year later a 200-MS/s 8-bit 8.5-mW Zero-Crossing-Based pipelined ADC, which replaced the comparator with a zero-crossing detector, was presented [8]. These implementations were explained in more detail in [9] and [10].

Both prototypes were single ended implementations. Single ended ADCs suffer under greater sensitivity to power supply noise and lower signal swings compared to a differential ADC.

We present a differential implementation of a CBSC ADC, and to the best of our knowledge, it is the first silicon proven differential CBSC. Although, simulation results of a pseudo-differential CBSC sigma-delta is detailed in [11].

The paper is organized as follows: Section 0.3 summarize opamp based switch capacitor circuits. Section 0.4 explain the CBSC circuits and detail a model of the output voltage of a CBSC MDAC. The circuit implementation is explained in Section 0.5. Calibration of the ADC is presented in Section 0.6 and Section 0.7 present the measurement results.

## Opamp Based Switched Capacitor Circuits

Switched capacitor circuits are prevalent in pipelined ADCs because of their robustness and accuracy. Doing arithmetic operations like summation, subtraction, and amplification is possible in SC circuit with high accuracy.

The accuracy of SC circuits is limited by capacitor matching, which can be accurately set in integrated circuits (on the order of 0.1 percent [12]).

SC circuits are usually designed with an opamp feedback loop as shown in Fig. 1. Most SC circuits have two clock phases, sampling and charge transfer.

Fig. 1 is a amplifier where the input is sampled in phase $p_1$, and charge is transferred from $C_1$ to $C_2$ in $p_2$ by forcing $V_x$ to ground. If the opamp has infinite gain the discrete time transfer function for Fig. 1 is a delayed

amplification

$$H_0(z) = \frac{C_1 + C_2}{C_2} z^{-1} \tag{1}$$

where the gain determined by the capacitance ratio.

With finite gain in the opamp the transfer function is

$$H_1(z) = H_0(z) \times \frac{1}{1 + (C_1/C_2 + 1)/A} \tag{2}$$

where $A$ is the DC gain of the opamp. For the remainder of this work we assume $C_1 = C_2$, so the amplifier has a gain of two.

Finite gain in opamp reduce the gain of the SC amplifier. Normally a gain error is not a significant problem, but in pipelined ADC a gain error cause static non-linearities, which reduce the resolution.

In technologies like $0.18\mu$m and $0.35\mu$m a high DC gain requirement pose few problems. It is trivial to make two stage amplifiers with enough gain for high accuracy systems. And if a folded-cascode amplifier does not have enough gain, one can use multiple stages, or gain boosting.

As the CMOS technology scales, however, it is increasingly difficult to achieve a high DC gain, due to the decreased output resistance of nano-scale transistors and reduced headroom.

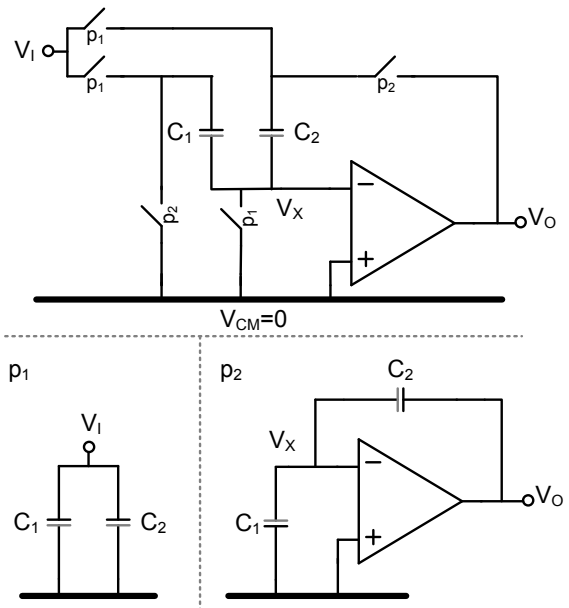



Figure 1: Switched capacitor amplifier with an operational amplifier

## Comparator-Based Switched Capacitor Circuit

It does not matter how a SC circuit arrive at the output voltage. What matters is that the output voltage is correct when the next stage samples, which is usually at the end of charge transfer.

Instead of an opamp a current source and a comparator can be used [7]. An opamp forces the virtual ground condition while CBSC charge the output with a current source and detect when virtual ground is reached. An example of a single ended CBSC is shown in Fig. 2, only charge transfer phase is shown, sampling phase is equivalent to opamp based SC.

First, the output is reset to the lowest voltage in the system (usually the negative supply (VSS)). This ensures that $V_X$ start below the virtual ground (common mode). The current sources are turned on at the start of reset and use reset to settle.

When reset ends the current source charge the output capacitance. The voltage at $V_O$ and $V_X$ rise until the comparator detect virtual ground ($V_X = V_{CM} = 0$). Due to the comparator delay it takes a moment for the current source to turn off, which results in a overshoot.

The overshoot can be corrected in several ways. One way is using two ramps [7], one fast and one slow, the fast ramp does an estimate of the output voltage, while a slow ramp in the opposite direction discharge the overshoot. Another is to change the threshold of the comparator to compensate for the overshoot [8], which is how our ADC is implemented. An overshoot can be completely cancelled if the ramp is linear.

A fundamental difference between opamp based SC and CBSC is that opamp based SC settle during charge transfer, CBSC never settle. The current from the current source is fully on until it is turned off, in an opamp based SC all currents in capacitors and switches (outside of the opamp) go asymptotically to zero as the opamp settles. In CBSC the current in capacitors and switches are in one of two states, constant or zero, and they are only zero when the final value has been determined. As a result, switch resistance cause offset and a non-linearity (switches have signal dependent resistance) [9], [10]. But effects can be minimized by splitting the current source [10], or reducing switch resistance. Reduced current helps, but the current in CBSC is proportional to frequency so high speed require high current.

The noise properties of comparator-based and zero-crossing-based converters has been exhaustively covered by [13] and [14] and will not be discussed in this work.

A analytical model of the output voltage is presented in the next section.

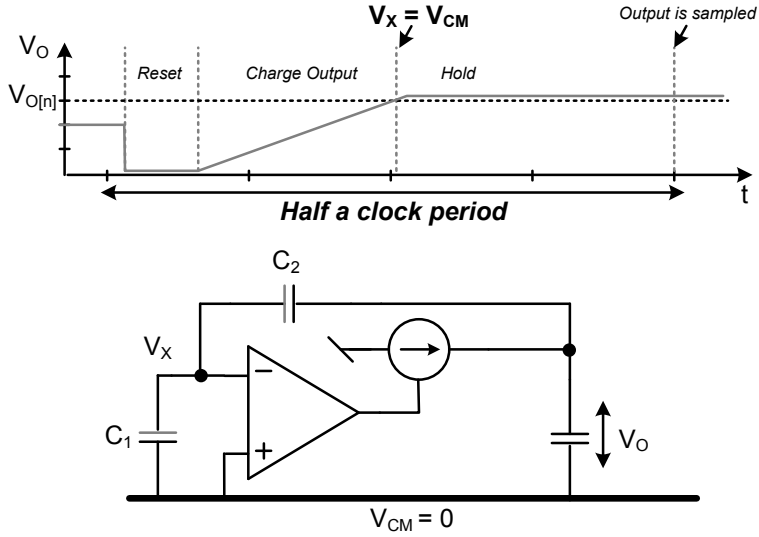



Figure 2: Comparator-based switched-capacitor circuit

## Output Voltage Model

Assume finite resistance in current source. Kirchhoff's current law give the differential equation

$$I_0 = C_O \frac{dV_O(t)}{dt} + V_O(t)/R_O \tag{3}$$

where $C_O$ is the capacitance at the output, $V_O$ is the output voltage, $I_0$ is the current in the current source and $R_0$ is the output impedance of the current source. Solving the differential equation yields.

$$V_O(t) = I_0 R_O \left(1 - e^{-\frac{t}{R_o C_O}}\right) \tag{4}$$

The time $t$ is the sum of $T_{V_I}$ — the time to charge to the ideal output voltage ($V_O(t) = 2V_I$)— and the comparator delay $T_D$. The ideal charge time $T_{V_I}$ is given by

$$T_{V_I} = -ln\left(\frac{-2V_I}{R_O I_0} + 1\right) C_O R_O \tag{5}$$

To compensate for the comparator delay the comparator threshold ($V_{CT}$) can be changed so the comparator start switching before $V_O = 2V_I$ is

reached. Accordingly, the charge time can be written as

$$t = -ln\left(-2\frac{V_I - V_{CT}}{R_O I_0} + 1\right) C_O R_O + T_D \tag{6}$$

Inserting (6) in (4) results in

$$V_O(t) = 2e^{-\frac{T_D}{R_O C_O}} V_I + I_0 R_O [1 - e^{-\frac{T_D}{R_0 C_O}} (1 + 2\frac{V_{CT}}{I_0 R_O})] \tag{7}$$

The gain in the MDAC should be two, but from (7) we see the gain is smaller than two ($2e^{-T_D/R_O C_O}$). This gain error will cause static non-linearities when a CBSC circuit is used in a pipelined ADC. The gain error is a function of the comparator delay, the output resistance and output capacitance.

The last factor in (7) is the overshoot.

# Implementation

The ADC is an 8-bit differential comparator-based switched capacitor pipelined ADC. It has continuous time bootstrapped input switches and comparator-based switched-capacitor MDAC. It differs from other CBSC ADC [8], [7] by being the first fully differential CBSC ADC. A system level diagram is shown in Fig. 3. The ADC has seven 1.5-bit pipelined stages and a 1.5-bit flash at the end.[1]

An on-chip non-overlapping clock generator produce the clock phases from an external clock. Reference voltages are generated off-chip. Digital error correction is performed off-chip in software for testability.

Each pipelined stage is controlled by a 22-bit calibration string, generated off-chip and written to the ADC through a serial interface. The circuit implementation of blocks in Fig. 3 are detailed in the following sections.

## Stage ADC/Comparator Design

Each stage in the pipelined ADC has a 1.5-bit analog-to-digital converter, often referred to as the sub ADC (SADC). The 1.5-bit architecture use redundancy to correct for offset errors in SADC comparators [15]. As a result, dynamic comparators can be used, which have large offsets but consume little power. In this converter the resistive divider dynamic comparator is used [16].

[1]The ADC was designed as a 10-bit ADC with eight stages and a 2 bit flash. But, measurements showed more noise than expected. So the MDAC in stage 8 was turned off and the output of the flash ignored.

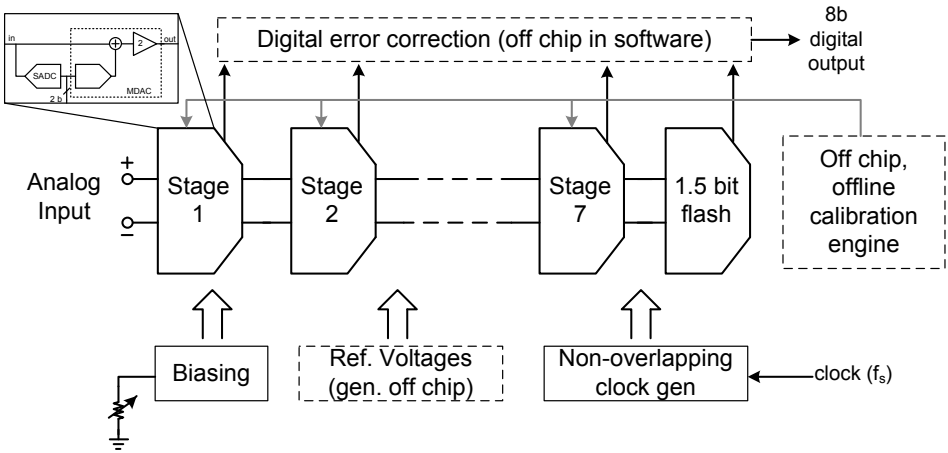



Figure 3: System level diagram of pipelined ADC

## Stage MDAC Architecture

Fig. 4 shows the MDAC of stage one and the sampling network of stage two. The stage operates on four phases $p_1$, $p_2$, $p_r$ and $p_{1a}$. An advanced clock phase $p_{1a}$, samples the input signal before $p_1$ turns off, this reduces the problem of signal dependent charge injection from $p_1$ switches. In phase $p_1$ the comparator is preset by forcing the comparator inputs to reference voltages $V_{RN}$ and $V_{RP}$, so the output of the comparator is known a the end of $p_1$. The output is reset in $p_r$, forcing $V_{XP} < V_{XN}$. The input switches in the first stage are continuous time bootstrapped switches.

## Continuous time bootstrapped switch

Bootstrapped switches are used to reduce the signal dependent charge injection and signal dependent switch conductance [17]. In bootstrapped switches a constant gate source voltage is applied to the switch. One method charges a capacitor to a fixed voltage when switch is off, and when the switch is turned on the capacitor is connected between the source and gate of the switch, thus acting as a battery to keep the gate source voltage constant [17].

Another approach is continuous time bootstrapping [18]. A source follower tracks the input signal with gate source voltage of the switch set by the gate source voltage of the source follower. Fig. 5 shows the continuous time bootstrapped switch. Thick oxide transistors (marked in Fig. 5 by thick gates) are used reduce reliability concerns.

The source follower $M_2$ is biased by $M_1$. An inverter ($M_3$ and $M_4$)

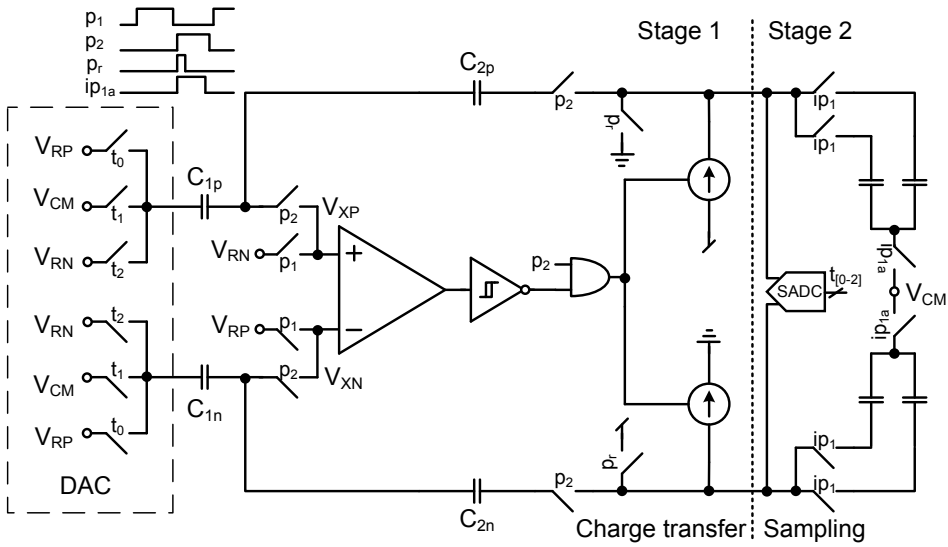



Figure 4: Stage one during charge transfer and stage two during sampling

control the gate voltage of the switch ($M_S$), the inverter switches between the level shifted input ($V_A$) and ground. When the switch is on ($p_1$ high) $M_5$ shorts the bulk of $M_S$ to the input, reducing the body effect and improving reliability (keeps gate bulk constant). When the switch is off $M_6$ shorts the bulk to ground to avoid forward biasing the bulk-drain PN junction.

## Comparator with adjustable threshold

A two stage continuous time amplifier (Fig. 6) with a differential first stage and single ended common source second stage is used as the comparator.

In phase $p_1$ the comparator inputs are reset to $V_{RN}$ and $V_{RP}$ (as shown in Fig. 4), so the output is known at the end of $p_1$. With preset the design of control logic between comparator and current sources is simplified. Phase $p_2$ start by resetting the MDAC outputs, this cause $V_{XN}$ to increase and $V_{XP}$ to decrease. When reset is complete the current sources start charging the MDAC outputs, as a result $V_{XN}$ falls and $V_{XP}$ rise. The comparator will start to flip when $V_{XN} = V_{XP}$.

Fig. 7 shows $V_{XN}$ and $V_{XP}$ as a function of time for different comparator thresholds ($V_{CT}$). The comparator should turn off current sources when $V_{XP} = V_{XN}$, but because the comparator has a delay ($T_C$) the current sources will turn off later, causing an overshoot (Fig. 7(a)). Adjusting the threshold of the comparator will change the amount of overshoot. If $V_{CT}$ is

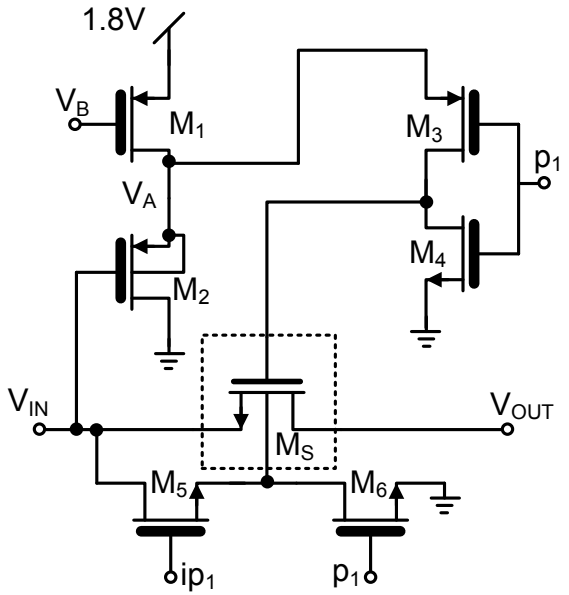



Figure 5: Continuous time bootstrapped switch

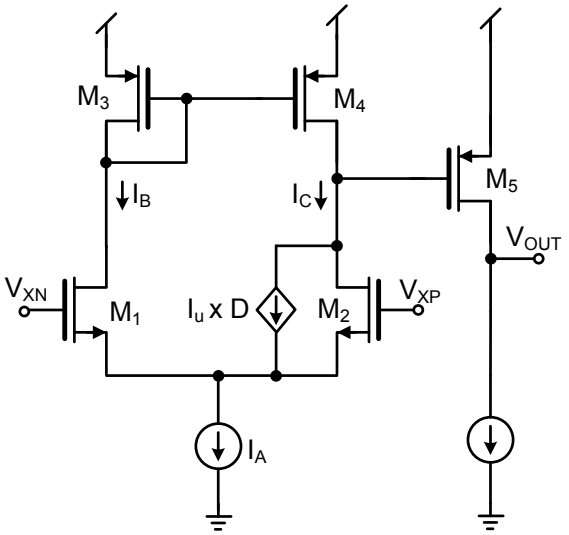



Figure 6: Comparator with adjustable threshold

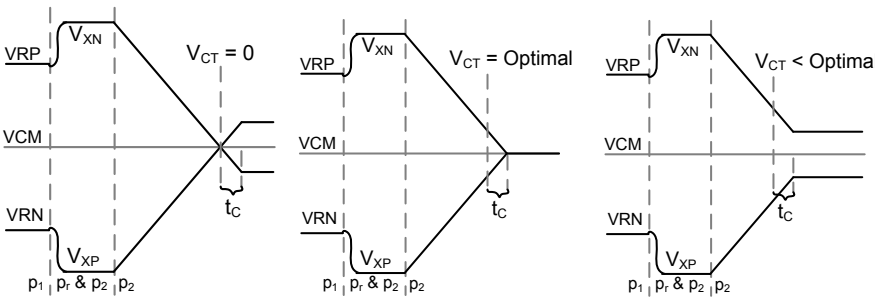
adjusted optimally there will no overshoot (Fig. 7(b)). If $V_{CT}$ is less than optimal the output undershoots (Fig. 7(c)). From the figure we see that a non-optimal threshold cause an offset in the MDAC output, as shown in (4). If the offset is small it is corrected by the digital error correction inherent to 1.5-bit stage architecture, the extra offset from the overshoot increase the demands on the dynamic comparators because the sum of offsets must be less than $\pm V_{REF}/4$ in a 1.5-bit stage.

The comparator threshold is controlled with a 6-bit current DAC in parallel with $M_2$, shown as a controlled current source. In Fig. 6 $I_u$ is a unit current and $D$ is an integer given by $D = 2^0b_0+2^1b_1+2^2b_2+2^3b_3+2^4b_4+2^5b_5$. The current in the current source $I_A$ is the sum of the two branch currents ($I_A = I_B + I_C$), the comparator threshold is defined as the differential input voltage when the branch currents are equal ($I_B = I_C$). Equal currents occur when

$$\beta V_{EFF,1}^2 = \beta V_{EFF,2}^2 + I_u \times D \tag{8}$$

where $\beta = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ and $V_{EFF,X}$ is the effective gate overdrive of transistors $M_X$. If $D = 0$ the currents are equal when the effective gate overdrive is equal, which occurs when the positive and negative inputs are equal. If $D > 0$ the currents are equal when the effective overdrive of $M_1$ is larger than the effective overdrive of $M_2$, which occurs when $V_{IN} > V_{IP}$.

The nominal delay of the comparator (including schmitt trigger and logic gates) is $T_C = 0.5ns$. With the 6-bit DAC the effective delay of the comparator can be controlled from $T_C = -0.9ns$ to $T_C = 0.5ns$.




(a) Comparator threshold equal to zero

(b) Optimal comparator threshold

(c) Comparator threshold less than optimal value

Figure 7: Voltage versus time for the nodes $V_{XN}$ and $V_{XP}$ as a function of comparator threshold

## Current sources

A linear ramp requires high output resistance in current sources. To that effect, we use regulated cascode current sources (Fig. 8). A PMOS current source is used for the pull up current, and a NMOS current source is used for the pull down current. Both the cascode and the common source transistor are turned off when the current source is turned off.

A single boost amplifier is shared between current sources to save power. The amplifier sees a variable capacitive load (the load varies with how many current sources are enabled), which affects settling and stability, both manageable challenges.

The current source is programmed with an 8-bit word. But it only has 6-bit resolution due to intentional overlap. The NMOS and PMOS sources are controlled separately. If the PMOS and NMOS currents are different the output common mode of the MDAC will be different from $(VDD - VSS)/2$. Simulations suggest that an active common mode control is unnecessary.

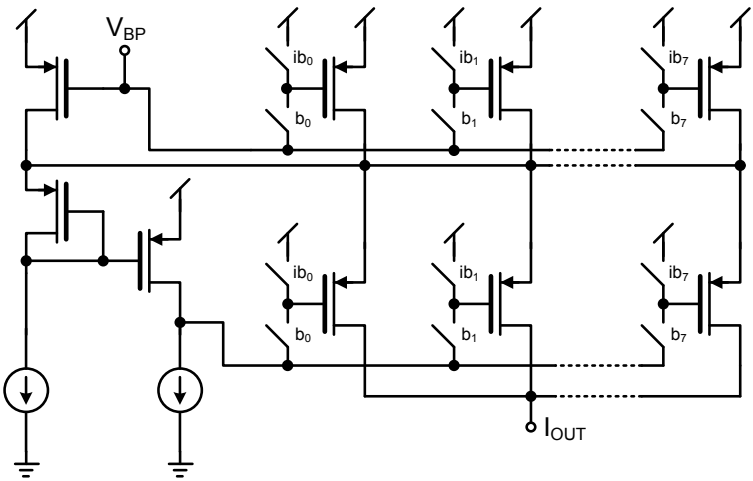



Figure 8: Regulated cascode current source with high output resistance

## Biasing circuitry, digital error correction and reference voltages

The pipelined core has simple bias circuitry with two external bias currents, one for all analog circuits and one to control the delay of current starved inverters used to generate the reset phase ($p_r$). Current mirrors are cascoded when possible. External reference voltages are used for testability,

so the power consumed by the references is not included in reported power dissipation. The digital outputs from the SADCs are brought off-chip by CMOS logic IO buffers. Synchronization, recombination and digital error correction is performed in software.

# Calibration

In CBSC some form of auto-zeroing or calibration is required. This can be seen from (7), the overshoot is proportional to $I_0$ and inversely proportional to the output capacitance of the MDAC. Both current and capacitance change with process corner.

Each stage has three calibration words, one for each current source and one for the comparator. The calibration word for the current sources is 8-bit, and 6-bit for the comparator threshold, in total, 22-bits per stage. All seven stages are calibrated, which results in $2^{154} - 1$ combinations, a large solution space.

It is impossible to test all combinations in such a large solution space.[2] So we use two different calibration algorithms: one deterministic time comparator threshold calibration, and a non-deterministic time genetic algorithm. The first only corrects for overshoot due to comparator delay, while the second also corrects for some of the mismatch between current sources.

## Deterministic time comparator threshold calibration

A flowchart of the calibration algorithm is shown in Fig. 9. The current source word $W_{I[N]}$ is the same for all stages, so all stages will have the same nominal current. Initially all currents are set to zero, $W_{I[0-7]} = 0$. The comparator threshold word $W_{C[N]}$ is also set to zero for all stages ($W_{C[N]} = 0$). The maximum value of the comparator threshold is $W_{CMAX} = 2^6 - 1$, and the minimum value is $W_{MIN} = 0$. $M$ and $N$ are the indexes of the inner and outer loop.

Calibration starts by turning on the current in the first stage ($W_{I[0]} = W_{IDEF}$, where $W_{IDEF}$ is a sufficient current for the speed of the ADC). The comparator threshold is set to half the distance between the maximum and minimum word given by

$$W_{C[N]} = \left\lceil \frac{W_{CMAX} + W_{CMIN}}{2} \right\rceil \tag{9}$$

[2] Assuming one combination could be tested each clock cycle it would take $48 \times 10^{30}$ years to test all combinations

The ADC is updated with the new calibration words — in the prototype the calibration algorithm is written in software and the calibration words are written to the ADC using a serial interface, however, the calibration algorithm can easily be integrated in hardware.

The mean value of the output is calculated using a window length of $L$. The run time is proportional to window length, and the window length set the accuracy of the mean. We assume the input signal is a zero mean sinusoid close to Nyquist, so a window length of $L = 2^B$ is sufficient. The sign of the calculated mean (plus a reference offset $x_{REF}$) is evaluated. If the offset is positive the comparator threshold is increased ($W_{CMIN} = W_{C[N]}$). If the offset is negative the comparator threshold is reduced ($W_{CMAX} = W_{C[N]}$). The inner loop index is updated ($M = M + 1$), and the search continues. The inner loop performs a binary search for the correct comparator threshold in each stage. The outer loop turns on more and more stages as the inner loop completes.

If we assume the time spent writing the calibration words to the ADC is insignificant the calibration algorithm will complete after $7 \times 7 \times 256 = 12.5k$ clock cycles. A genetic algorithm was used to verify that this calibration algorithm finds a solution close to optimum.

### Non-deterministic calibration

To verify the comparator threshold calibration a genetic algorithm is used. A genetic algorithm models evolution and has been shown to find solutions for large search spaces [19]. The disadvantage of the genetic algorithm is the non-deterministic run time, since it cannot be determined analytically how long it takes before a good solution is found. The genetic algorithm varies both current and comparator threshold in the ADC.

## Experimental Results

### Results of calibration

The input signal during calibration is a sinusoidal input close to the Nyquist frequency ($f_i = 29.4MHz$). Fig. 10 shows the measured integral non-linearity (INL) and differential non-linearity (DNL) for three different cases. Fig. 10(a) shows the INL and DNL for the default calibration words set before production based on simulation. Here the comparator threshold is too low, which results in an overshoot. For the un-calibrated case the ENOB is 2.4-bits.

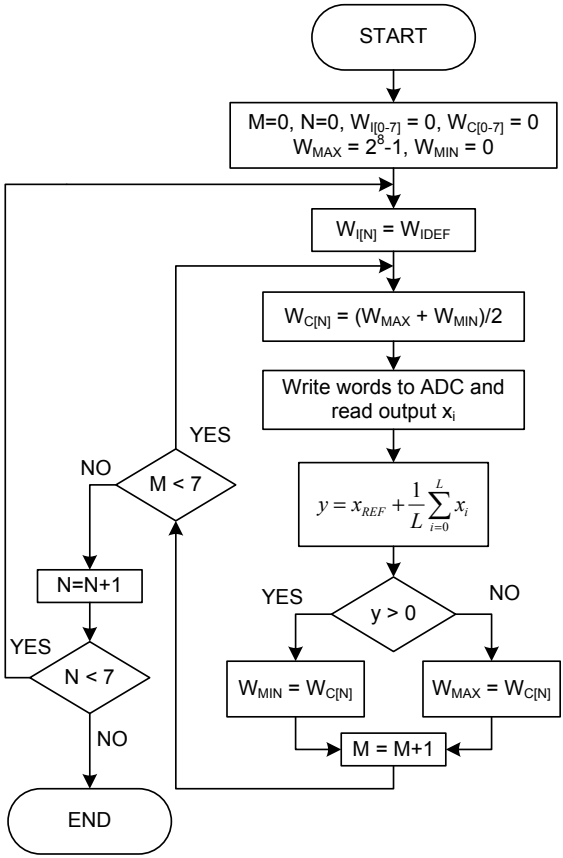
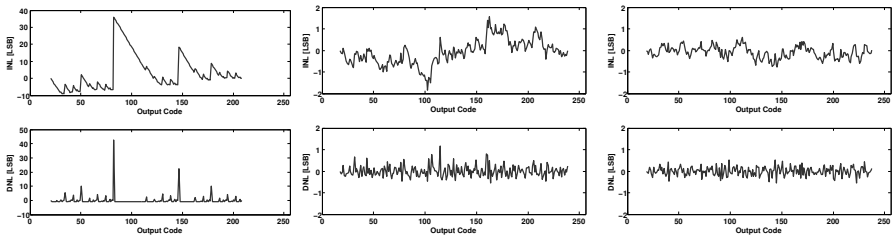



Figure 9: Deterministic time comparator threshold calibration

Using deterministic time comparator threshold calibration the INL and DNL improves from $+36/-9$ LSB to $+1.6/-1.8$ LSB, as shown in Fig. 10(b). With comparator threshold calibration the ENOB is 6.5-bit. The INL shows signs of a gain error, and multiplying the bits from the first stage by 1.022 improve the ENOB to 6.9-bit. From (7) this suggest that either the comparator delay is too long, the output resistance is reduced or capacitance is to low.

Using the genetic algorithm a better solution is found, shown in Fig. 10(c). The best solution improve the ENOB by 0.5-bit, resulting in a peak ENOB of 7.05-bit. This solution use less current in the first stage than used with comparator threshold calibration, which does increase the output resistance of the first current sources. According to (7) this would reduce the gain error, but reduced output resistance has not been confirmed as the cause of the gain error.

The best solution is used for the remainder of the measurements.




(a) No calibration, default values set before before production

(b) Deterministic calibration of comparator thresholds with current fixed

(c) Non-deterministic calibration of positive and negative current plus comparator threshold using a genetic algorithm.

Figure 10: INL and DNL for uncalibrated, offset calibration and genetic algorithm

## Measured Power and Accuracy

The micrograph of the ADC is shown in Fig. 12 and a summary of the ADC performance is shown in Table 1. It achieves a signal-to-noise and distortion ratio (SNDR) of 44.2-dB (7.05-bit) at Nyquist, with a sampling frequency of 60MS/s and a power dissipation of 8.1mW (6.4mW for ADC core and 1.7mW for clock generator and distribution), which result in a Walden figure

of merit of 1 pJ/step[3] and a Thermal figure of merit of 7.7fJ/step.[4] An input signal amplitude of -1 dBFS is used.

The ADC has a spurious free dynamic range of (SFDR) of 60-dB at Nyquist. The SNDR and SNR change little with input frequency, and the effective resolution bandwidth extend well above the Nyquist frequency (Fig 13). The SFDR change with frequency and is maximum at Nyquist, the calibration algorithm used this frequency and we assume that is why the SFDR best at that frequency.

A 8192 point FFT of the ADC output is shown in Fig 11. Coherent sampling and a Hanning window is used to avoid spectral leakage into neighboring FFT bins.

Simulation of the ADC showed a peak SNDR of 9-bits, but as [10], we measured more noise than expected. Some of the extra noise appear to be coming from digital IO. As [10] we noted a strong correlation between digital IO supply voltage and noise level in the ADC. In theory the power supply rejection is better in a differential design, which could suggest that there is mismatch between the differential paths in the ADC, but this has not been quantified.

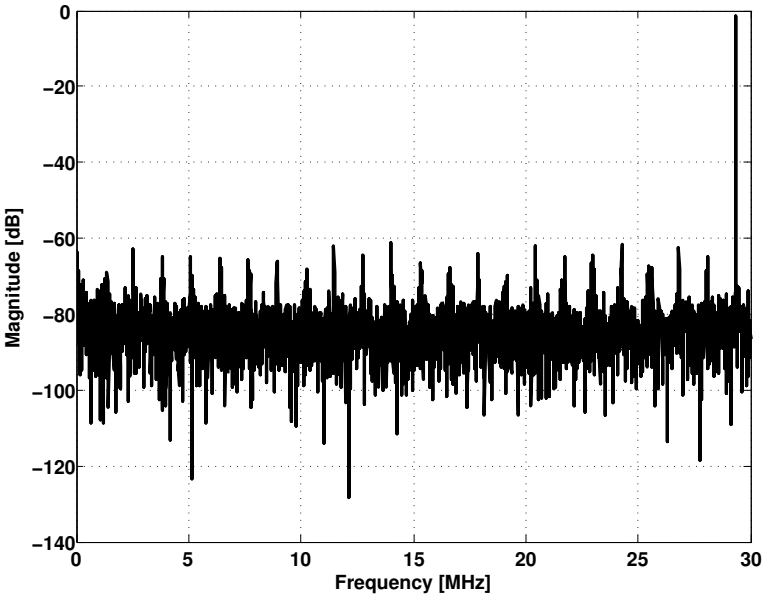



Figure 11: A 8192 point FFT of the ADC output

[3] $FOM = P/2^B f_S$
[4] $FOM = P/2^{2B} f_s$

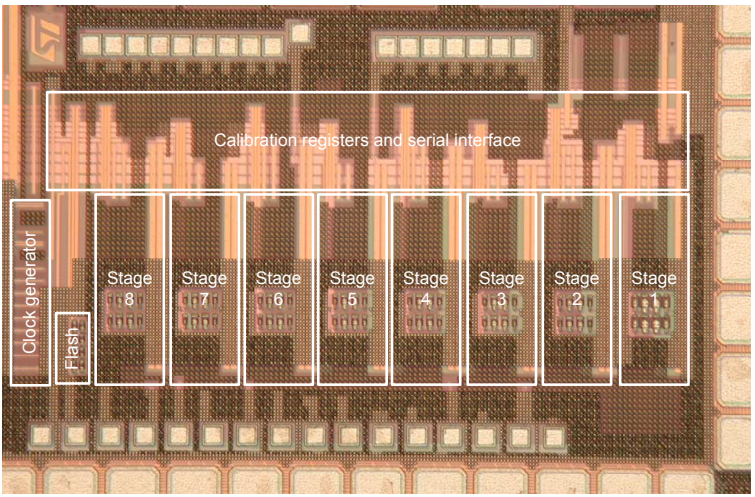



Figure 12: Chip micrograph. Stage 8 and flash are not used.

Table 1: Summary of calibrated ADC performance

| Technology | 1.2V/1.8V 90nm CMOS |
|---|---|
| Sampling Frequency | 60 MS/s |
| Resolution | 8 bits |
| Full scale input | 0.8V |
| Size | 0.85mm x0.35 mm |
| DNL (LSB) | 0.52 / -0.54 |
| INL (LSB) | 0.6 / -0.77 |
| SNR (29.4MHz input) | 44.5 dB |
| SNDR (29.4MHz input) | 44.2 dB |
| SFDR (29.4MHz input) | 60 dB |
| Analog power | 6.39mW |
| Clock power | 1.69mW |
| Waldon Figure of Merit | 1.0 pJ/step |
| Thermal Figure of Merit | 7.7 fJ/step |

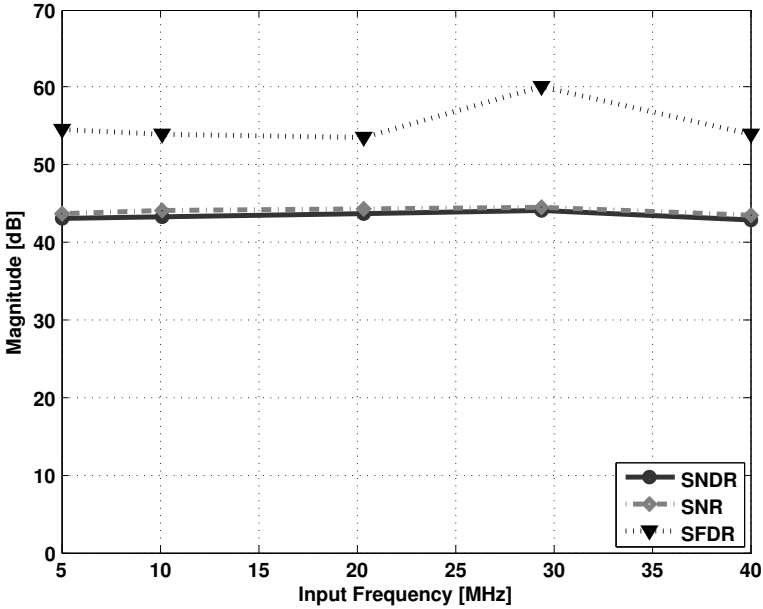



Figure 13: SNDR, SNR and SFDR versus frequency, sampling frequency is 60MS/s. Calibration words are constant.

# Conclusion

The first differential comparator-based switch capacitor (CBSC) pipelined ADC was presented. The switched-capacitor multiplying digital-to-analog converter (MDAC) use current sources and a comparator to do charge transfer. Continuous time bootstrapped switches were used in the first stage to reduce signal dependent switch resistance. A simple calibration correct for comparator delay variation due to manufacturing. Calibration reduce ramp overshoot, which dominate the non-linearity in CBSC ADCs. The ADC was produced in a 90nm low-power CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.1mW at 60MS/s.

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