Limits of ADC figure of merit

Carsten Wulff, Trond Ytterdal

Abstract

Expressions for limits of analog-to-digital converter (ADC) figure of merit (FOM), with and without parasitic capacitances, are derived and shown to be in good agreement with published ADC results. The FOM limit for linear settling is shown to be proportional to the number of bits in the ADC.

I. Introduction

Efficiency is one of the key measures of analog-to-digital converters. A more efficient ADC can translate into longer battery life, which we all want for our hand-held devices. For ADCs the power dissipation (P), sampling frequency (f_s) and effective number of bits (N) are combined to give a single measure of the efficiency, the figure of merit (FOM). For the figures of merit discussed here a smaller value is better. The historic figure of merit proposed by Walden [1] was (1)[1]

$$FOM = \frac{P}{2^N f_s} \tag{1}$$

This FOM is incorrect, however, if one assumes ADCs should be limited by thermal noise. A more correct figure of merit is

$$FOM = \frac{P}{2^{2N} f_s} \tag{2}$$

This figure of merit, the Thermal FOM, is based on the fact that in an ADC limited by thermal noise we must use 4 times the power if we add one bit of resolution, since the required sampling capacitance increases 4 times. A more in-depth argument is given in [2] on page 360.

Equation (2) will give a value for the FOM if one has the ADC parameters, but what is the limit of the FOM? How low FOM can we expect to get with future ADCs? We will in this paper derive expressions for the FOM limit and compare the limit to results from published ADCs, but first we have to derive the required sampling capacitance for a certain resolution.

[1]It was actually presented as $FOM = 2^N f_s/P$, but the inverse is the most used

II. Required Sampling Capacitance

We assume a switched capacitor based ADC where the input is sampled across a sampling capacitor (C), and that C is the only capacitor in the ADC. In such a system the thermal noise power can be represented as

$$\overline{V_{thermal}^2} = a_1 \times kT/C \tag{3}$$

where a_1 is a constant greater than one, k is Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitance. The thermal noise power determines how much power we must dissipate to get certain dynamic range. A certain dynamic range translates into a quantization noise power requirement. The thermal noise power should be less than the quantization noise power, but not too small, because a very small thermal noise power will cost in terms of power dissipation. We assume in this paper that the quantization noise power should be four times the thermal noise power.

$$\overline{V_{LSB}^2} = 4 \times \overline{V_{thermal}^2} \tag{4}$$

Here $\overline{V_{LSB}^2}$ is the quantization noise power, which can be calculated as

$$\overline{V_{LSB}^2} = V_{LSB}^2/12 = V_{PP}^2/(2^{2N} \times 12) \tag{5}$$

where V_{LSB} is the voltage step of the least significant bit (LSB) and V_{PP} is the peak to peak signal voltage. If we combine (3), (4) and (5) we get (6).

$$\frac{V_{PP}^2}{2^{2N} \times 12} = 4 \times a_1 \times kT/C \tag{6}$$

Solved for sampling capacitance (C) (6) becomes

$$C = a_1 \times \frac{48kT2^{2N}}{V_{PP}^2} \tag{7}$$

Using equation (7) we can calculate how large C must be for a certain number of bits resolution. For example for $V_{PP} = 1\ V, T = 300\ K$ we get $C_{[N=6]} = 0.8fF$, $C_{[N=12]} = 3.3pF$, and $C_{[N=14]} = 53pF$. Equation (7) contains one of the parameters (2^{2N}) we need for the FOM limit derivation, the other two are derived through the equations for linear settling of a single pole system.

III. Linear Settling FOM Limit

We assume the voltage across C must reach a final value within a certain accuracy, given by the LSB, and reach this accuracy within half the sampling period ($1/2f_s$). Assume a trans-conductance amplifier (an ideal transistor with resistive load $R_o = 1/g_m$) is used to drive the capacitance C. The amplifier has the transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + sC/g_m} \tag{8}$$

where V_o is the voltage across the capacitance, V_i is the input voltage to the amplifier and g_m is the trans-conductance. Assume the input is a unit step function $V_i(t) = V_{PP}u(t)$. The output will then be

$$V_o(t) = V_{PP} - V_{PP}e^{-g_m t/C}, t > 0 \tag{9}$$

Rewritten in terms of the settling error ($\epsilon = V_{PP} - V_o(t)$) we get

$$\epsilon = V_{PP}e^{-g_m t/C} \tag{10}$$

After settling this error should at maximum be one LSB, $\epsilon = V_{PP}/2^N$. The trans-conductance in (10) can be written as $g_m = \eta_1 2I_D/V_{EFF}$ where η_1 is a technology dependent constant (it depends on high field effects and short channel effects, η_1 is larger than 0 but less than 1), I_D is the drain current and V_{EFF} is the effective gate overdrive. Inserted into (10) together with (7) results in

$$\frac{V_{PP}}{2^N} = V_{PP}\, e^{\left(-\frac{\eta_1 2 I_D \frac{V_{PP}^2}{V_{DD}^2} V_{DD}^2}{2 f_s \frac{V_{EFF}}{V_{DD}} V_{DD} a_1 48 k T 2^{2N}} \right)} \tag{11}$$

Solved for FOM we get

$$FOM = \frac{I_D V_{DD}}{2^{2N} f_s} = \frac{N \ln(2) \frac{V_{EFF}}{V_{DD}}}{\eta_1 \frac{V_{PP}^2}{V_{DD}^2}} a_1 48 k T \tag{12}$$

An interesting part of (12) is that the figure of merit is proportional to the number of bits, this is a result of the increased settling time required for more bits. According to this equation, with additional bits it will be more difficult to get a good figure of merit, but this ignores the influence of parasitic capacitances.

IV. FOM LIMIT INCLUDING PARASITIC CAPACITANCE

Assume that an ADC has N stages, define M_0 as the number of nodes per stage and C_0 as the parasitic capacitance per node. The total parasitic capacitance in the ADC will then be

$$C_p = C_0 M_0 N \tag{13}$$

The parasitic capacitance (13) will add to the load of our trans-conductance amplifier, accordingly the load will be

$$C = a_1 \times \frac{48kT2^{2N}}{V_{PP}^2} + C_0 M_0 N \tag{14}$$

Inserted into (10)

$$\frac{V_{PP}}{2^N} = V_{PP}\, e^{\left(-\frac{\eta_1 2 I_D}{2 f_s \frac{V_{EFF}}{V_{DD}} V_{DD}} \frac{1}{\frac{a_1 48kT2^{2N}}{V_{PP}^2} + C_0 M_0 N} \right)} \tag{15}$$

And with some manipulation

$$FOM = \frac{N \ln(2) \frac{V_{EFF}}{V_{DD}}}{\eta_1 \frac{V_{PP}^2}{V_{DD}^2}} \left(a_1 48kT + \frac{C_0 M_0 N V_{PP}^2}{2^{2N}} \right) \tag{16}$$

For $C_0 = 0$ (16) reduces to (12). These two equations, (12) and (16), are based on numerous assumptions, and it is interesting to see how well the equations predict published results for ADCs.

V. COMPARISON WITH PUBLISHED RESULTS

The FOM limits have been compared to ADCs published in Journal of Solid State Circuits (JSSC) in the years 1975-2005 and ADCs published at the International Solid State Circuits Conference (ISSCC) in the years 2000-2008. The comparison is shown in Figure 1. We have used $V_{EFF}/V_{DD} = 1/8, V_{PP}/V_{DD} = 0.5, \eta_1 = 0.5, a_1 = 1, T = 300\ K$. Choosing the value for M_0 and C_0 is guesswork since they depend on ADC architecture and technology, but it is unlikely that $M_0 < 10$ and $C_0 < 1fF$. A more realistic model would arguably be $M_0 = 200$ and $C_0 = 10fF$. None of the published ADCs go below the FOM limit given by (12), but for high number of bits ($>$ 14-bits) they begin to approach the limit. At high number of bits it is more straightforward to achieve a good FOM because the required sampling capacitor becomes large and the parasitic capacitances become less important. However, for low to medium number of bits

($<$ 12-bits) the required sampling capacitance is so low ($<$ 4 pF) that the parasitic capacitances dominate. At 7 bits the best ADC is more than 100 times worse than the FOM limit. The parasitic FOM limit given by (16) match closely the form of the data points, the realistic model ($M_0 = 200, C_0 = 10fF$) enclose most of the data points, and the likely limit ($M_0 = 10, C_0 = 1fF$) enclose all. It should be noted that the four points between the two parasitic FOM limit lines are from ISSCC 2008, where a special session was held for high efficiency ADCs, these four ADCs are 10 times better than the rest of their class.

VI. Conclusion

Expressions for limits of ADC figure of merit, with and without parasitic capacitances, were derived and shown to be in good agreement with published ADC results. The FOM limit for linear settling was shown to be proportional to the number of bits in the ADC.

References

[1] R. H. Walden, "Analog to digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, 1999.

[2] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. John Wiley & Sons, 2005, no. ISBN-0-471-46585-2.

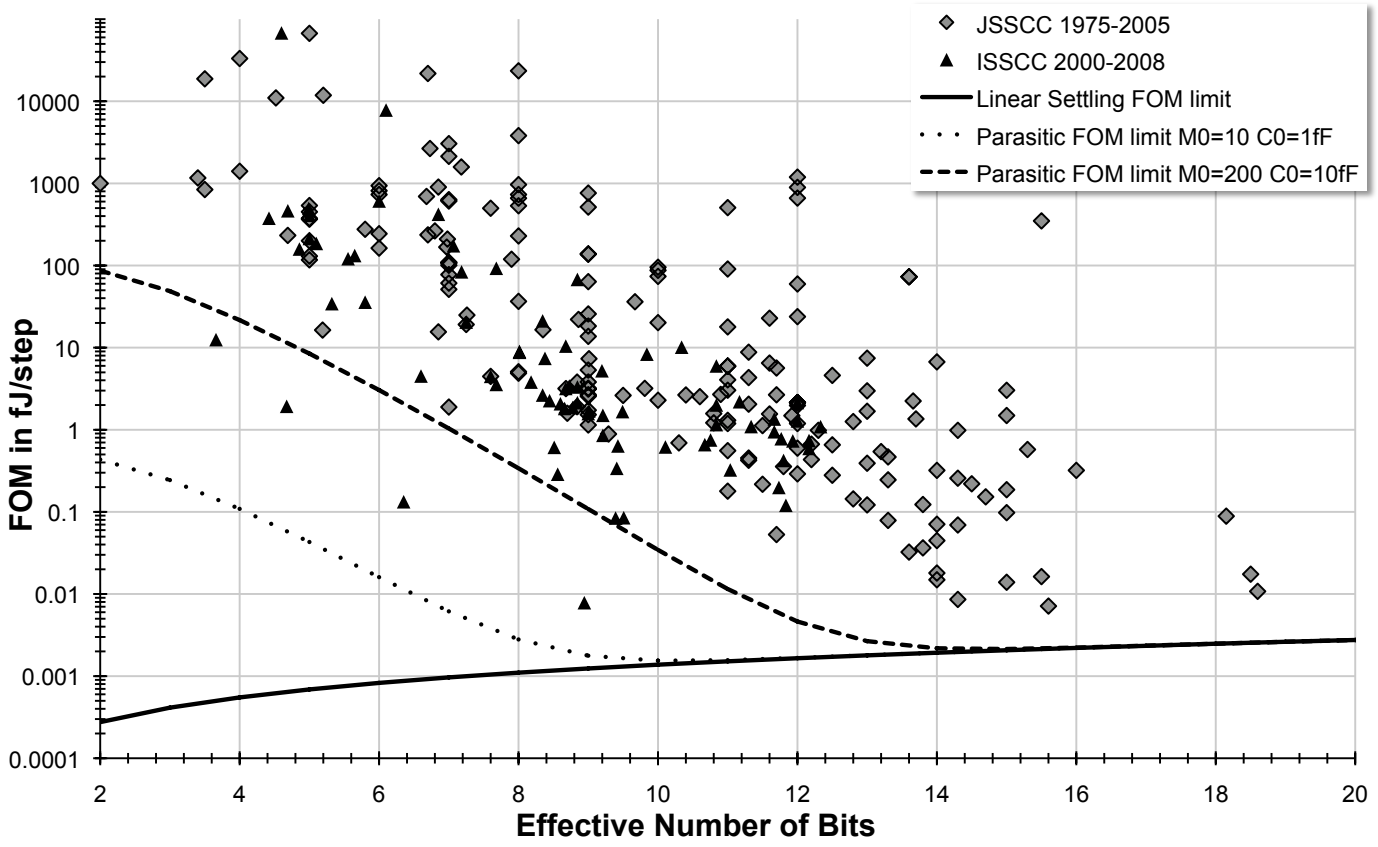
Authors' affiliations

Carsten Wulff (wulff@iet.ntnu.no) and Trond Ytterdal (ytterdal@iet.ntnu.no). Department of Electronics and Telecommunication, Norwegian University of Science And Technology (NTNU), 7491 Trondheim, Norway.

Figure captions

Figure 1: FOM versus bits for selected ADCs published in JSSCC in the years 1975-2005 and ADCs published at ISSCC 2000-2008 compared to the FOM limit and the parasitic FOM limit

Figure 1


JSSCC 1975-2005
ISSCC 2000-2008
Linear Settling FOM limit
Parasitic FOM limit M0=10 C0=1fF
Parasitic FOM limit M0=200 C0=10fF
FOM in fJ/step
10000
1000
100
10
1
0.1
0.01
0.001
0.0001
2
4
6
8
10
12
14
16
18
20
Effective Number of Bits