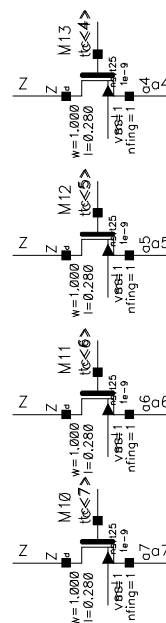
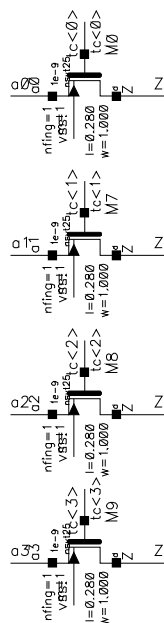


a0  
a1  
a2  
a3  
a4  
a5  
a6  
a7  
tc<0:7>



z

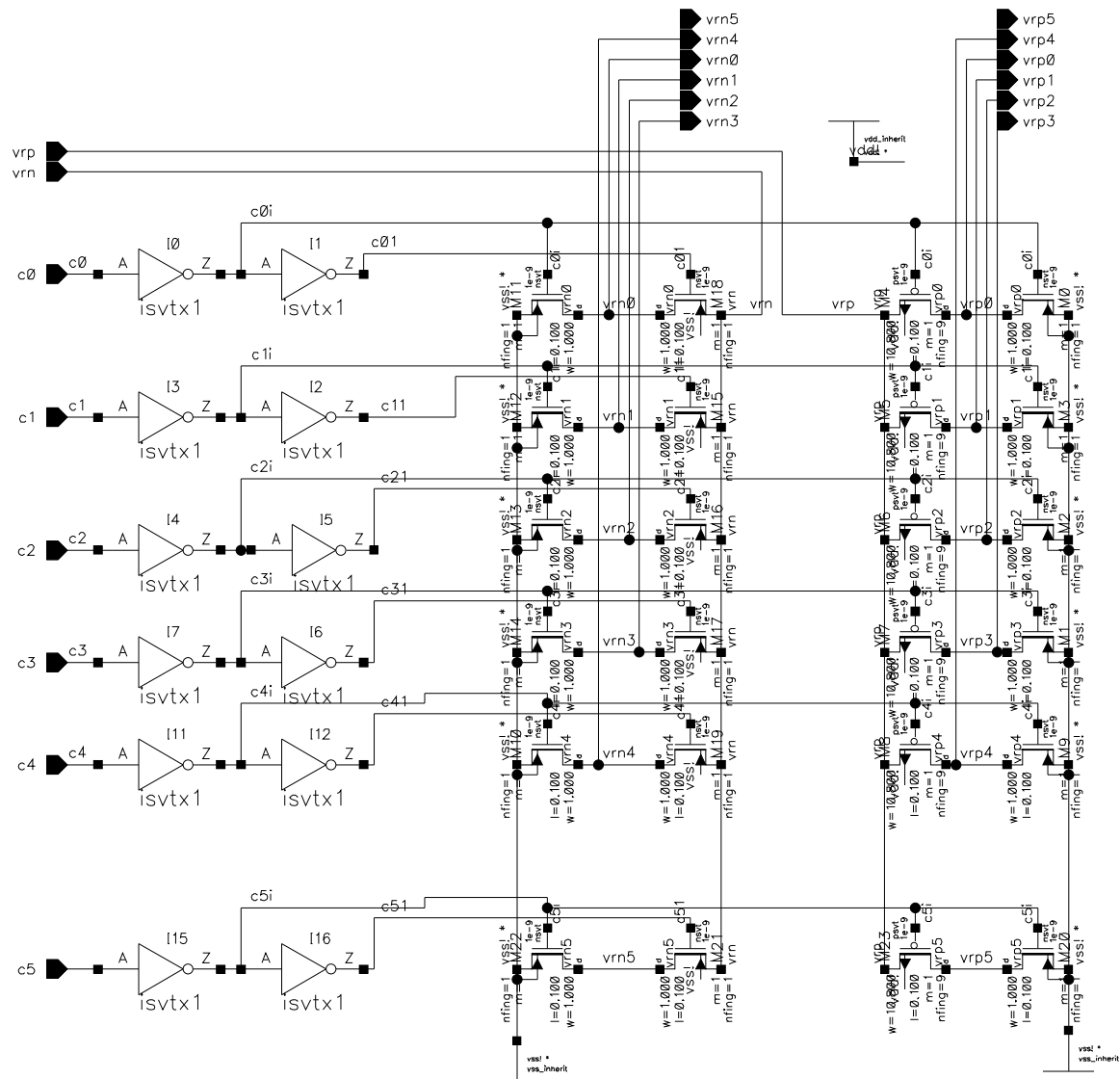
Title : Analog test output mux

SIZE  
A

DWG NO.

Date : Jul 16 13:10:36 2007  
Rev. :  
Author : Carsten Wulff

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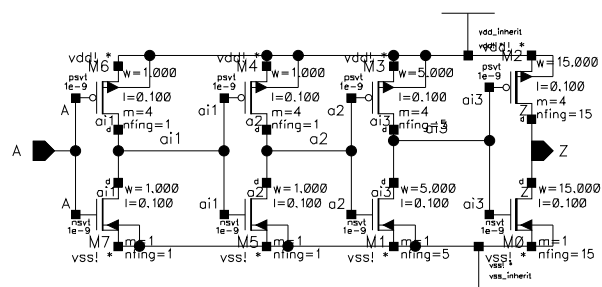
Title : Offset Control for Comparator

SIZE  
A

DWG NO.

Date : Jul 16 13:11:29 2007  
Rev. :  
Author : Carsten Wulff

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Title : Clock Buffer

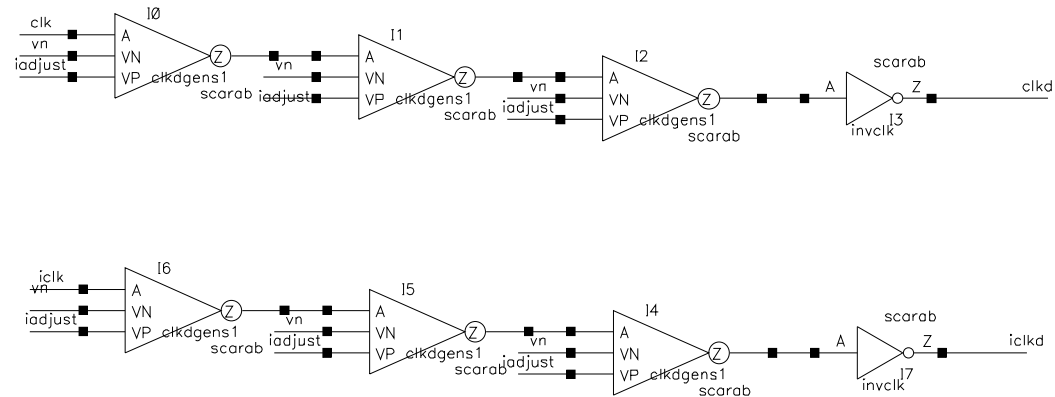
SIZE  
A

DWG NO.

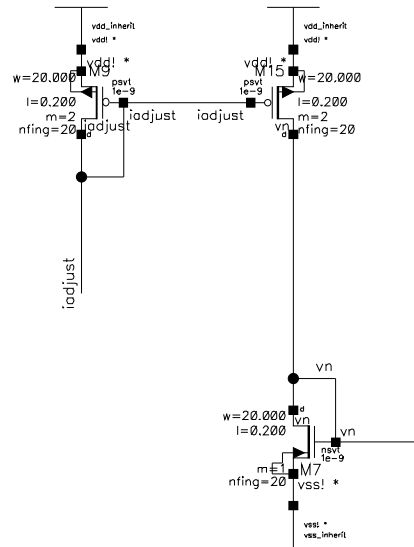
Date : Jul 16 13:08:21 2007  
Rev. :  
Author : Carsten Wulff

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clk  
iclk  
iadjust



clk  
iclk



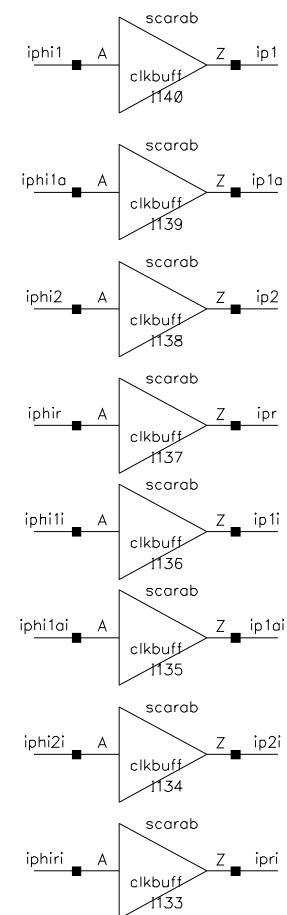
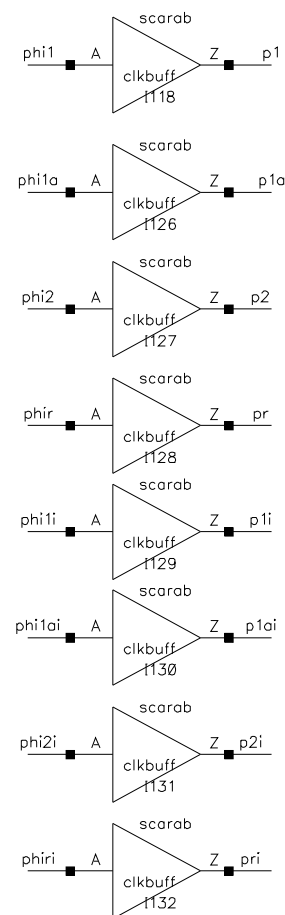
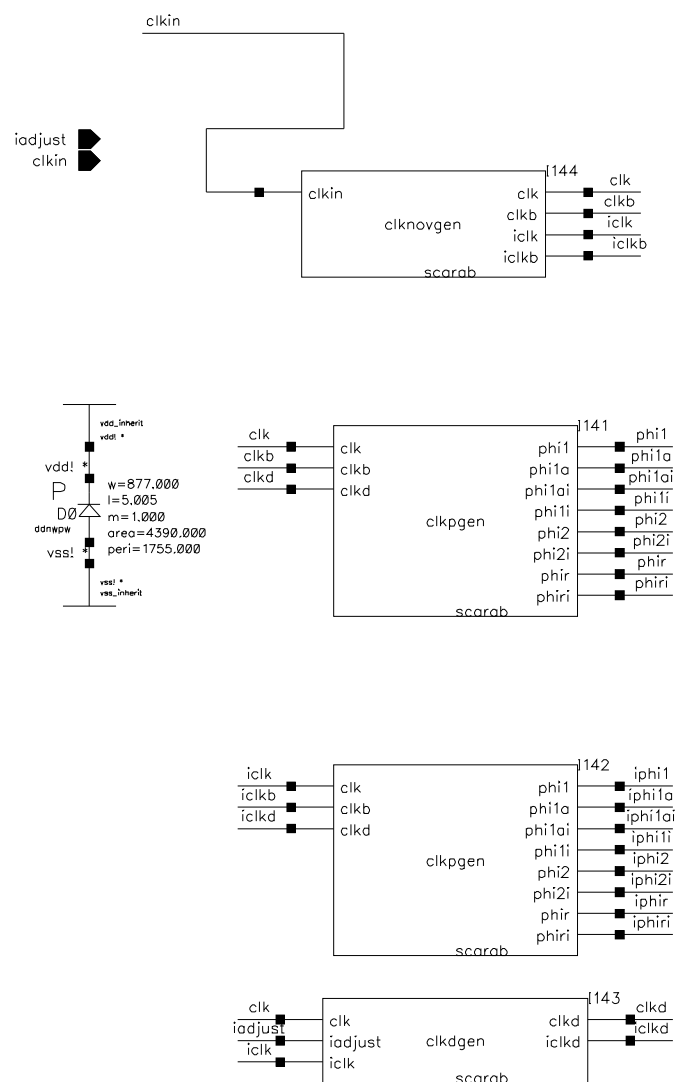
Title : Variable Delayed Clock Generator

SIZE  
A

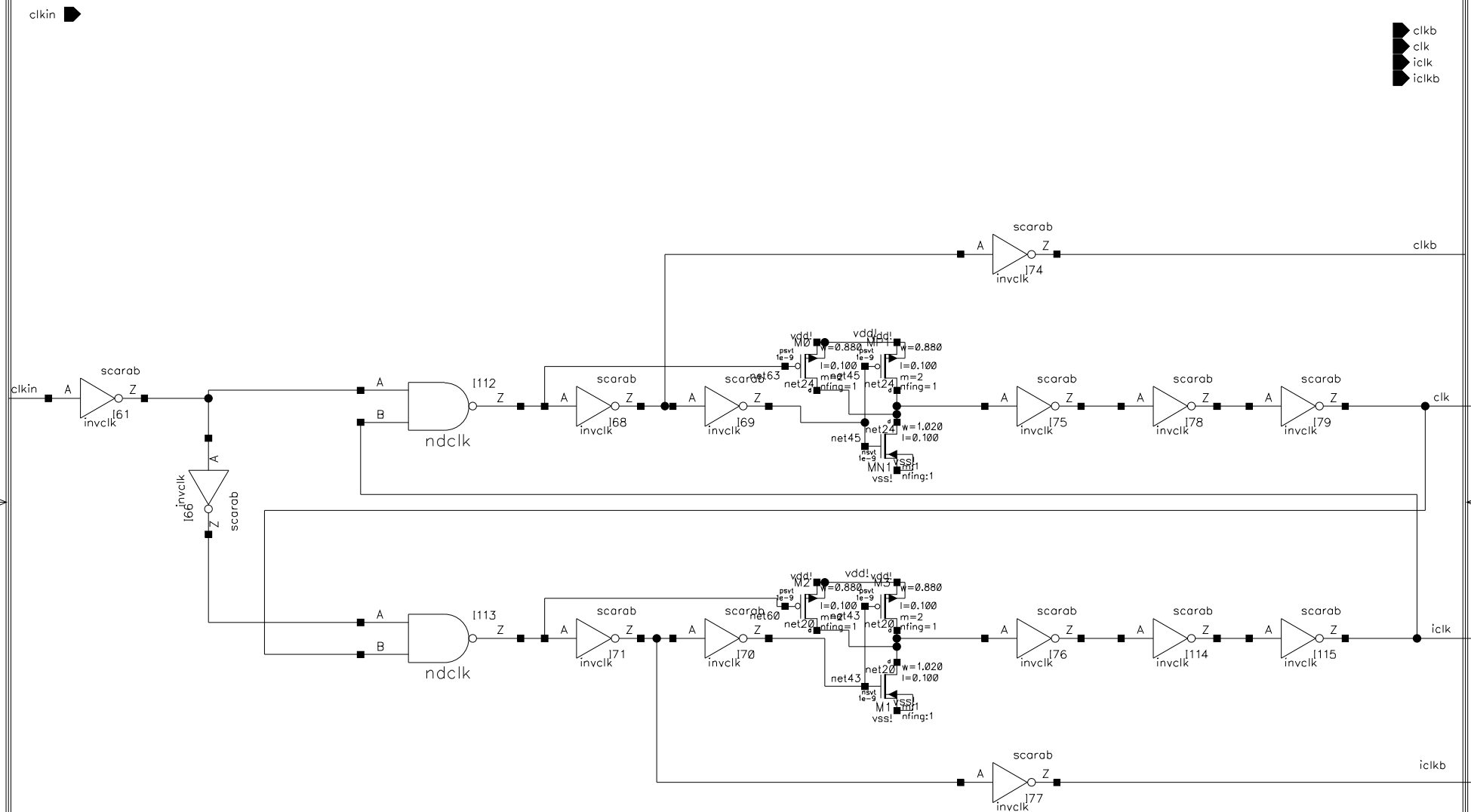
DWG NO.

Date : Jul 16 13:08:14 2007  
Rev. :  
Author : Carsten Wulff

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p1  
p1a  
p2  
pr  
p1i  
p1ai  
  
p2i  
pri  
ip1  
ip1a  
ip2  
ipr  
ip1i  
ip1ai  
ip2i  
ipri



Title : Non-overlapping clock generator

SIZE 

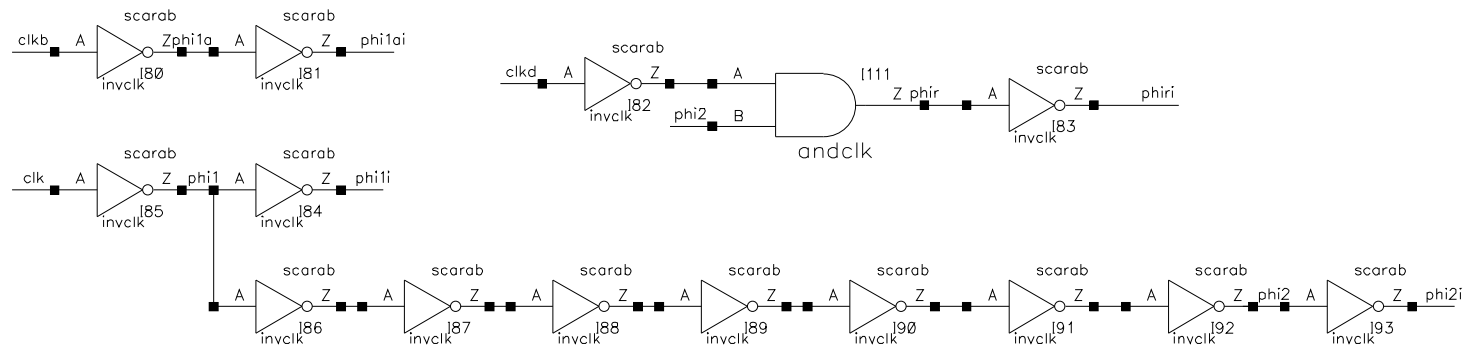
DWG NO.

Date : Jul 16 13:08:06 2007  
Rev. :  
Author : Carsten Wulff

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clkb  
clk  
clkd

phi1a  
phi1ai  
phi1i  
phi1i  
phi2  
phir  
phiri  
phi2i



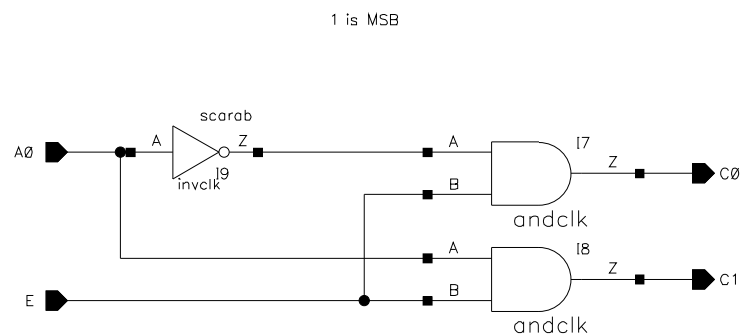
Title : Clock Phase Generator

SIZE  
A

DWG NO.

Date : Jul 16 13:08:09 2007  
Rev. :  
Author : Carsten Wulff

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Title : 1-2 decoder

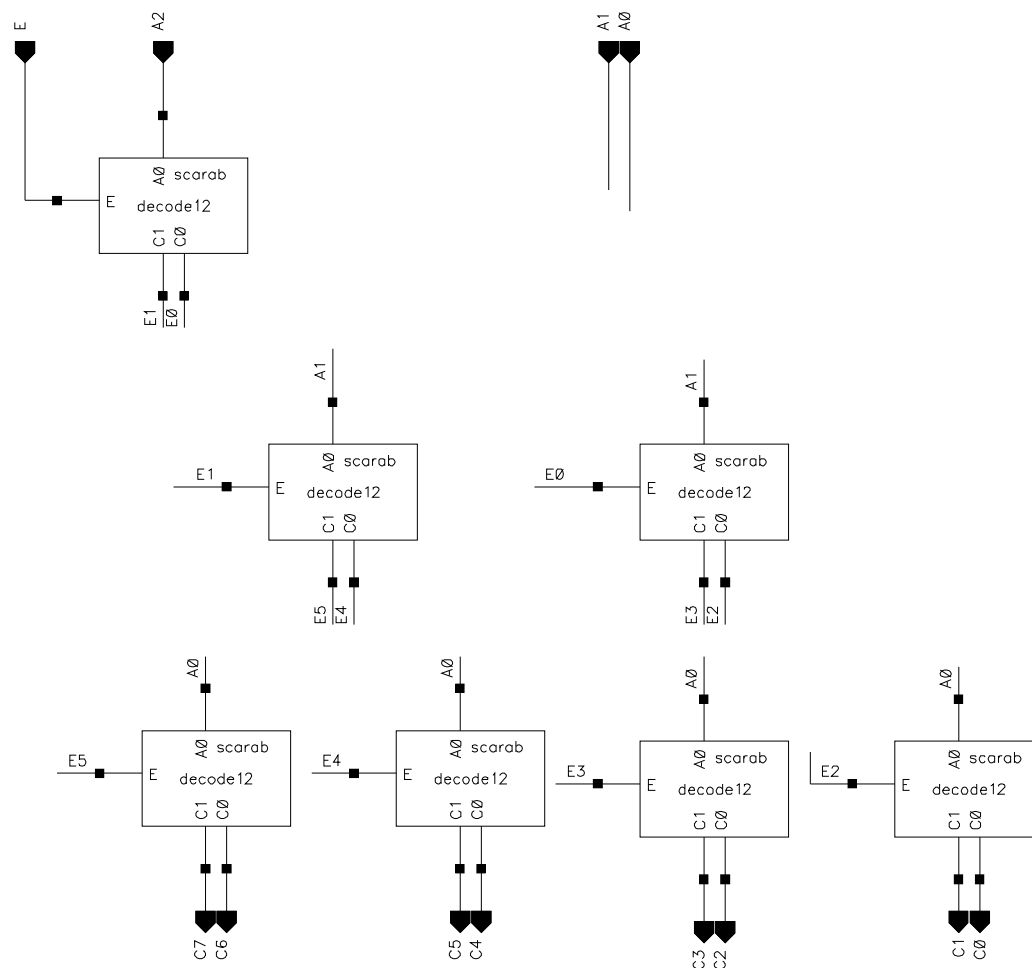
SIZE  
A

DWG NO.

Date : Jul 16 13:10:33 2007  
Rev. :  
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Title : 3-8 decoder

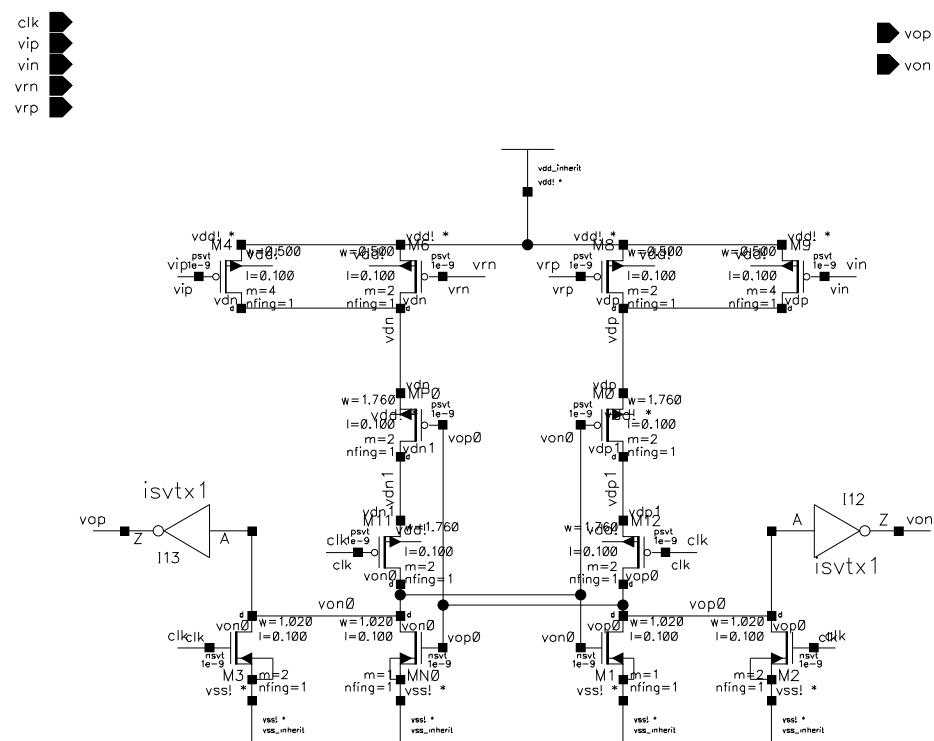
SIZE

A

DWG NO.

Date : Jul 16 13:10:31 2007  
Rev. :  
Author : Carsten Wulff

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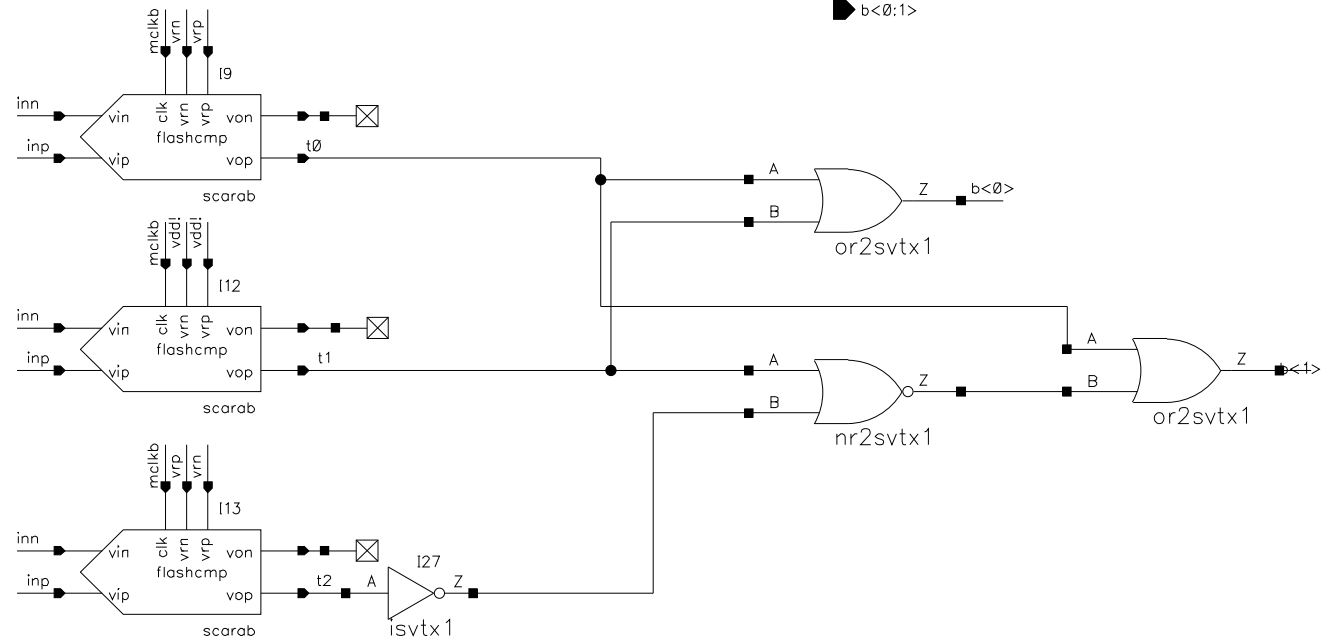
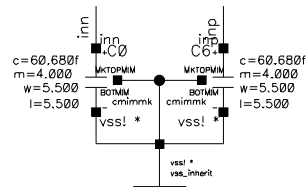
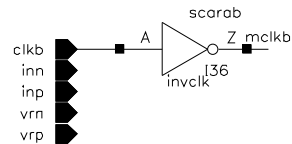
Title : Dynamic Comparator

SIZE 

DWG NO.

Date : Jul 16 13:08:29 2007  
Rev. :  
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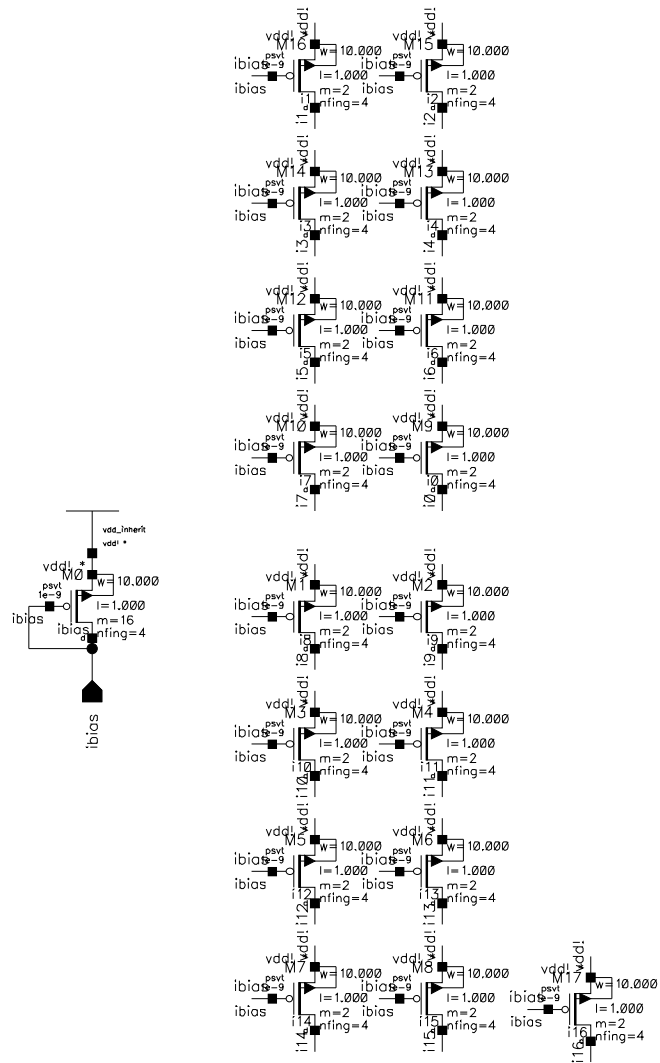
Title : Flash

SIZE  
A

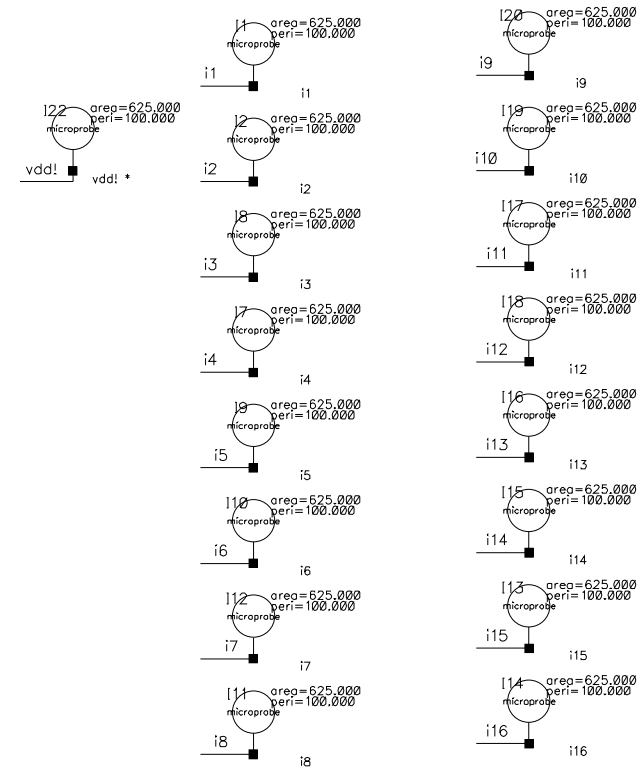
DWG NO.

Date : Jul 16 13:08:27 2007  
Rev. :  
Author : Carsten Wulff

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i1  
i2  
i3  
i4  
i5  
i6  
i7  
i8  
i9  
i10  
i11  
i12  
i13  
i14  
i15  
i16



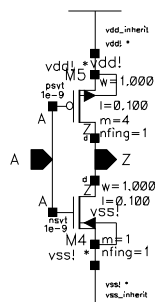
Title : icopy

SIZE  
A

DWG NO.

Date : Jul 16 13:08:00 2007  
Rev. :  
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Title : Inverter for Clock

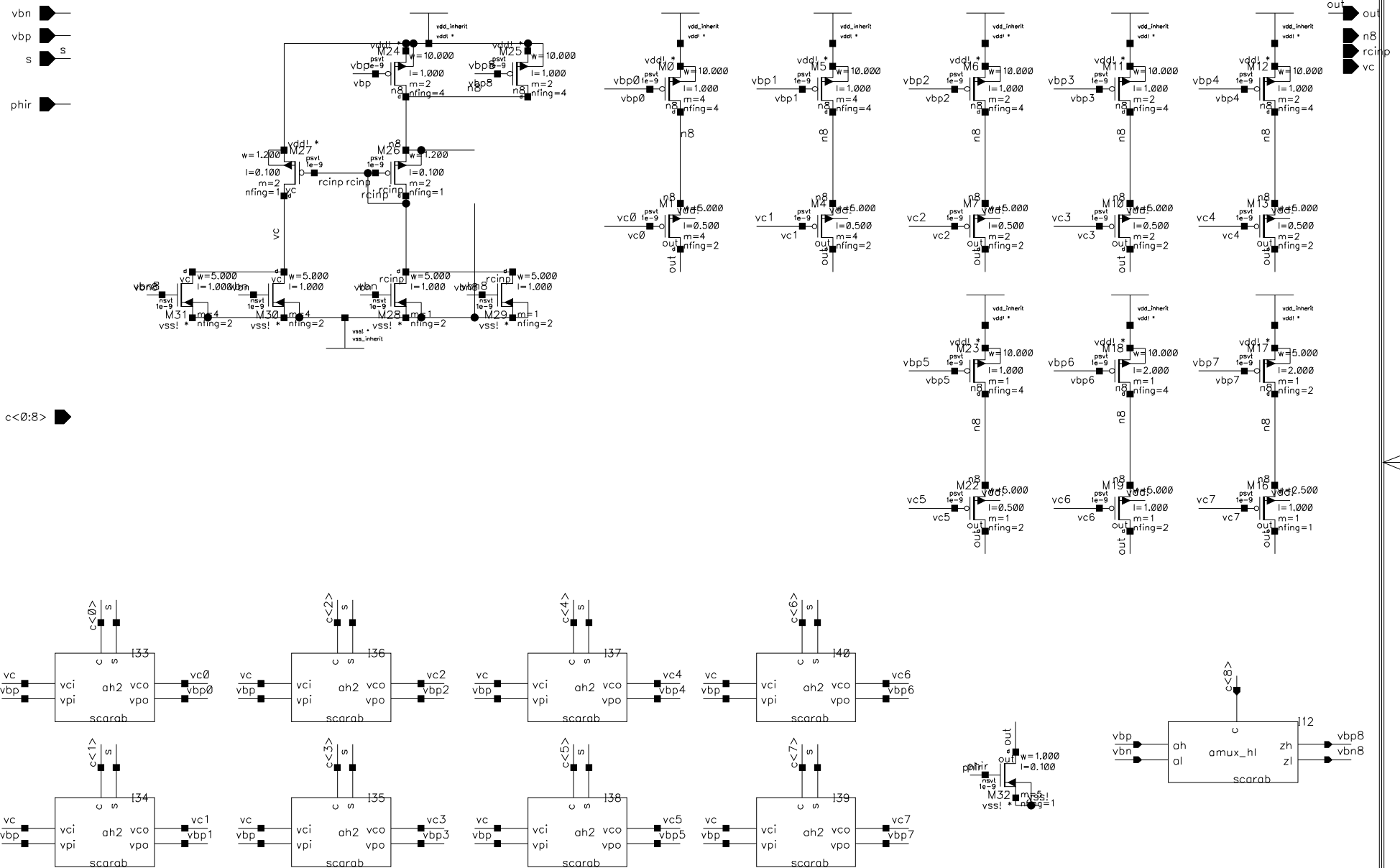
SIZE **A**

DWG NO.	
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Date : Jul 16 13:10:56 2007  
Rev. :  
Author : Carsten Wulff

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Title : pisrc

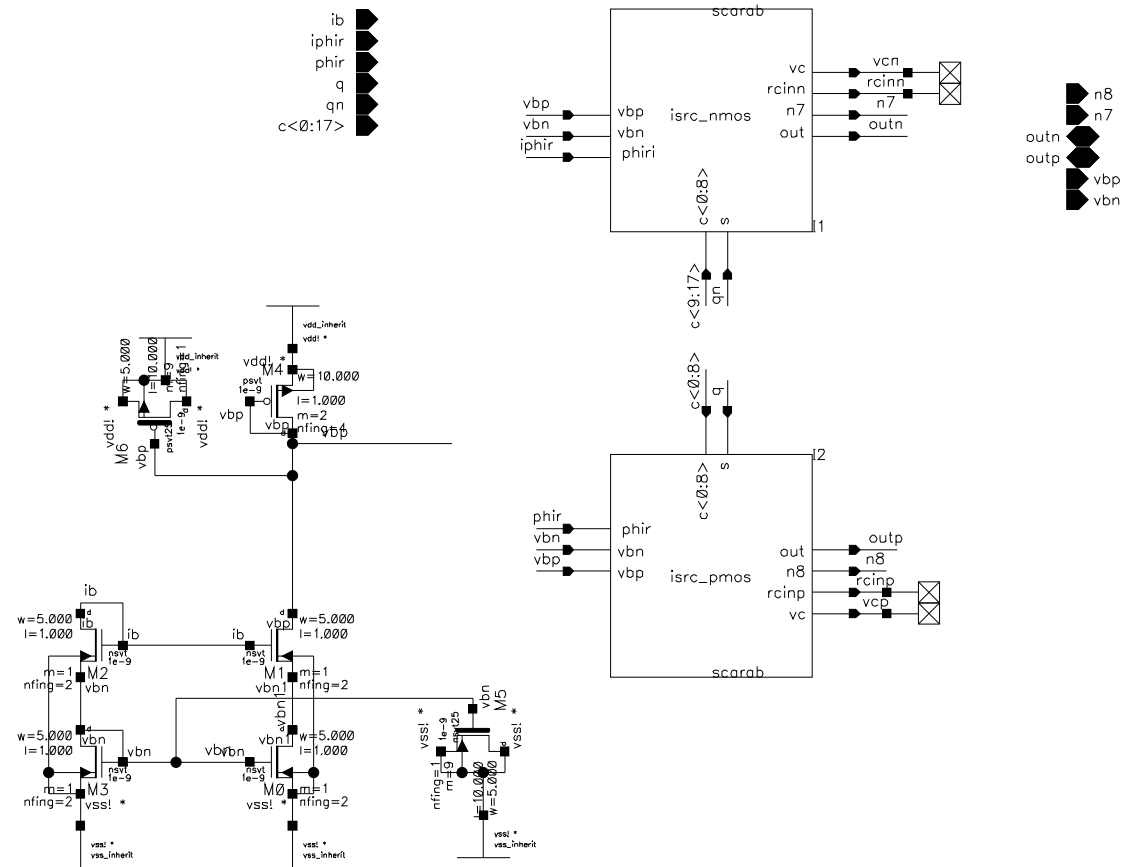
SIZE  
A

DWG NO.

Date : Jun 26 12:31:41 2007  
Rev. : 1  
Author : Carsten Wulff

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Parameters on schematic are out of date;  
Process Parameters File has been changed.



Title : High impedance current sources

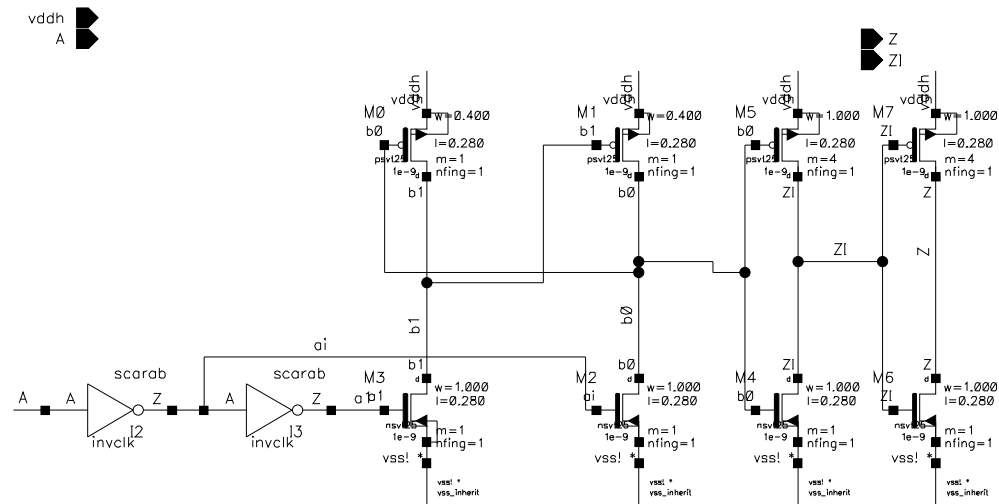
SIZE A

DWG NO.

Date : Jul 16 13:08:57 2007  
 Rev. :  
 Author : Carsten Wulff

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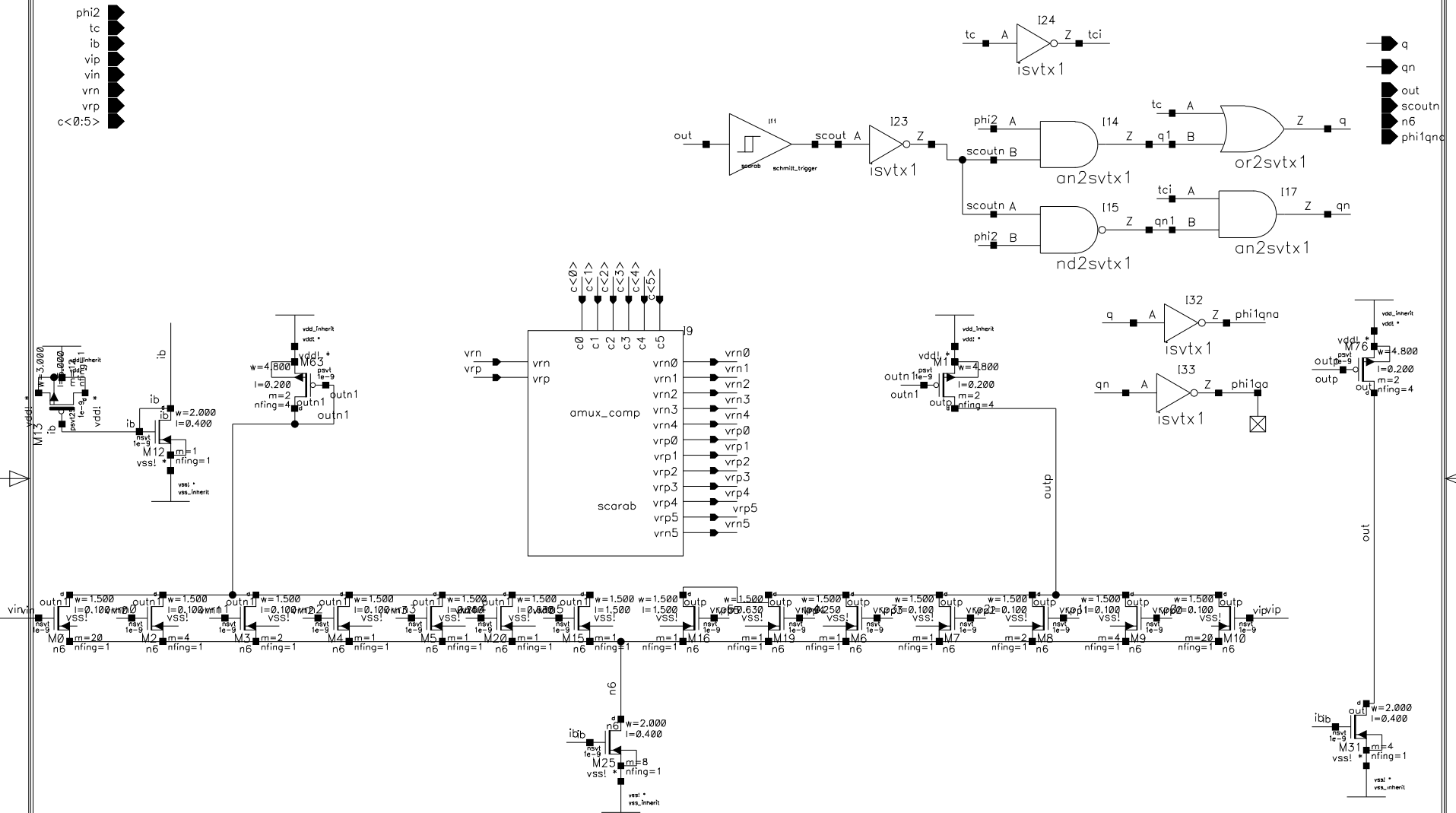
Title : test signal level shift

SIZE A

DWG NO.

Date : Jul 16 13:10:27 2007  
Rev. :  
Author : Carsten Wulff

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Title : mdacomp

SIZE  
A

DWG NO.

Date : Jul 16 13:11:24 2007  
Rev. : 1  
Author : Carsten Wulff

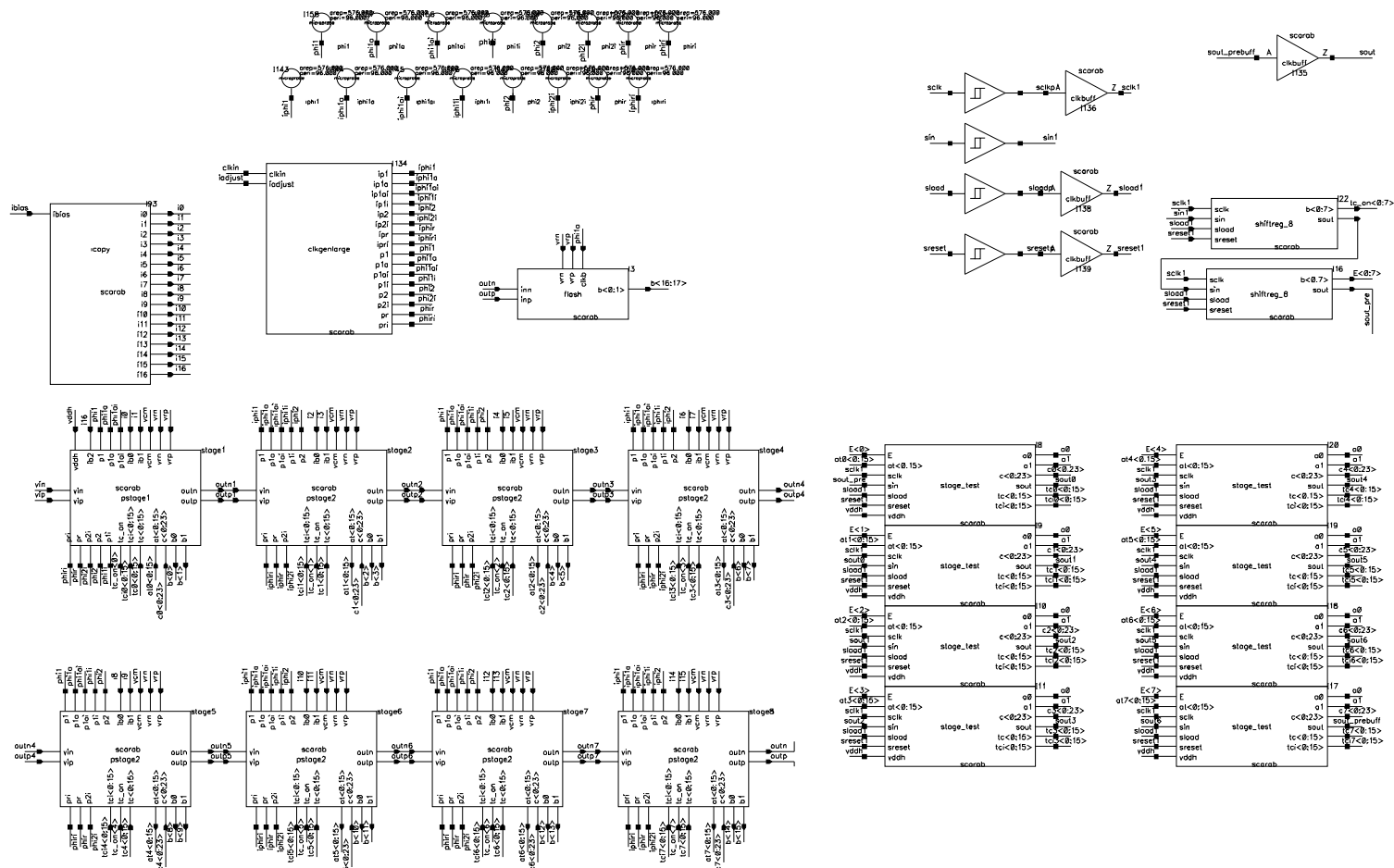
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Parameters on schematic are out of date;  
Process Parameters File has been changed.

sin  
sclk  
sreset  
sload

ibios  
ladjust  
clkin  
vrp  
vcm  
vin  
vip  
vdah

sout  
b<8:17>  
a0  
a1

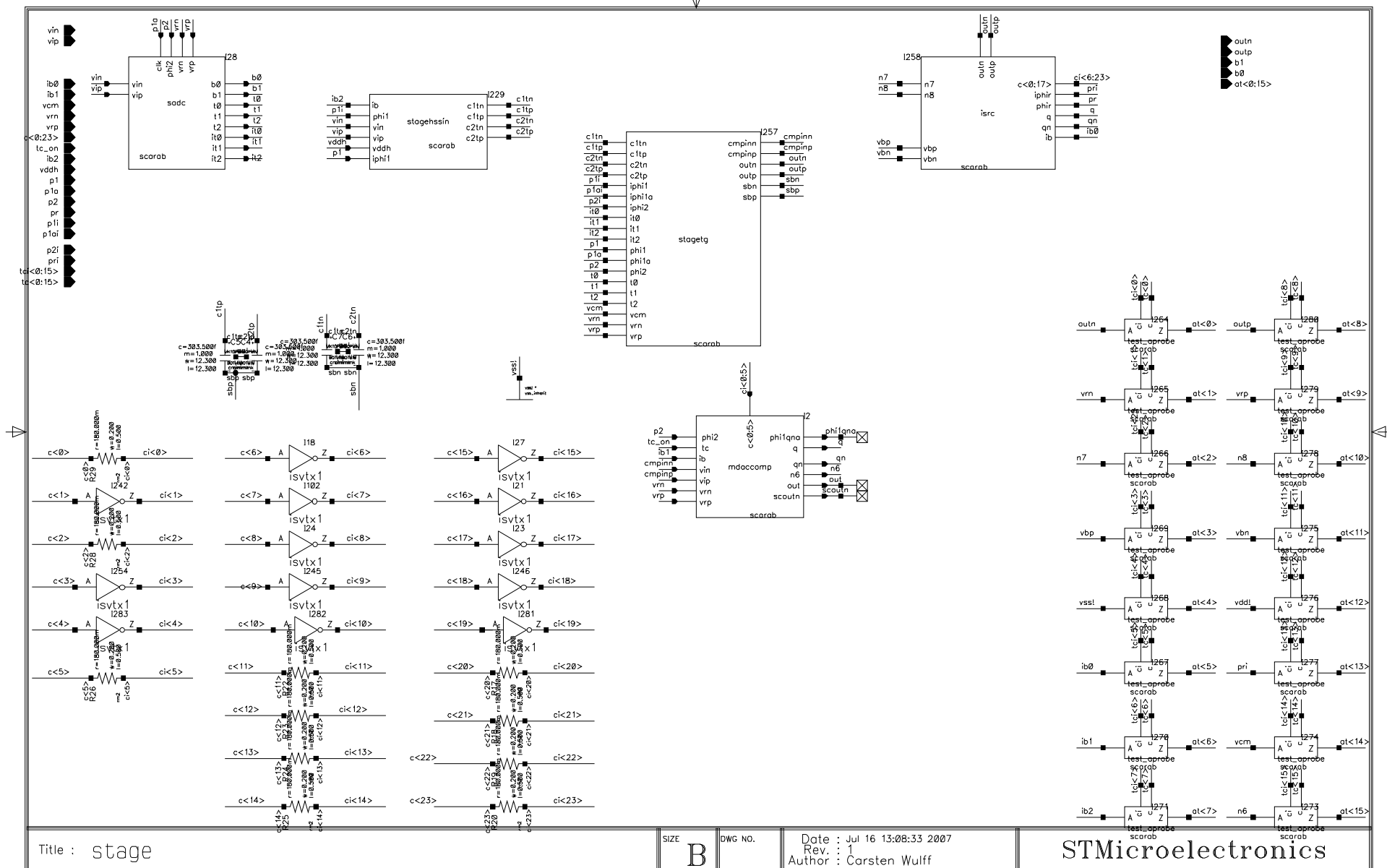


scarab

pstage1

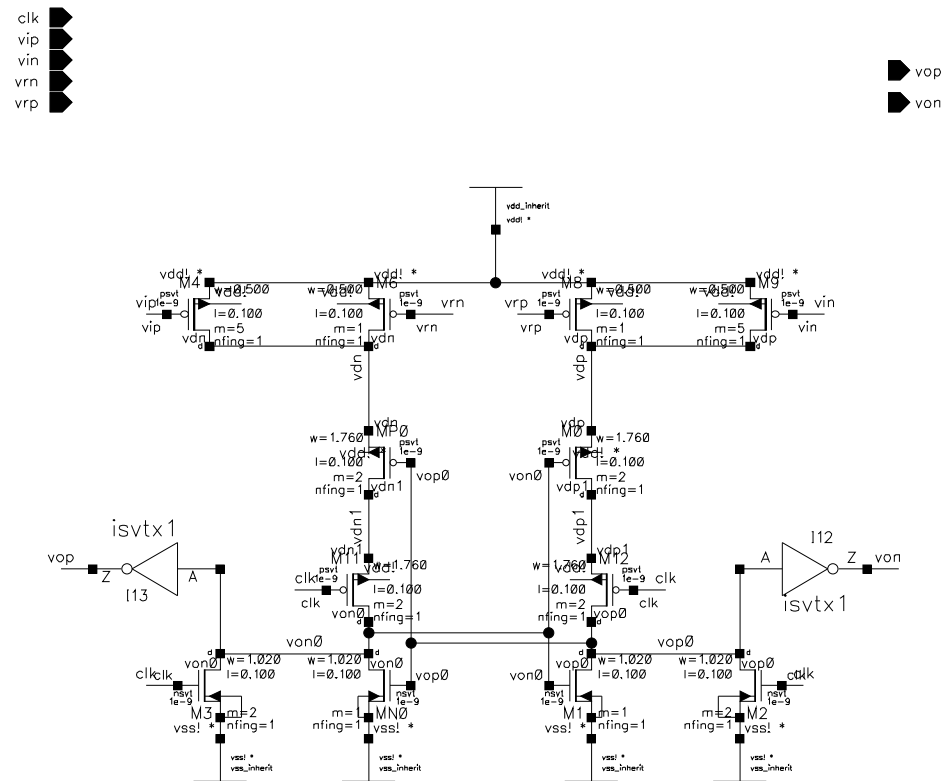
schematic

Sheet : 1/1





Parameters on schematic are out of date;  
Process Parameters File has been changed.



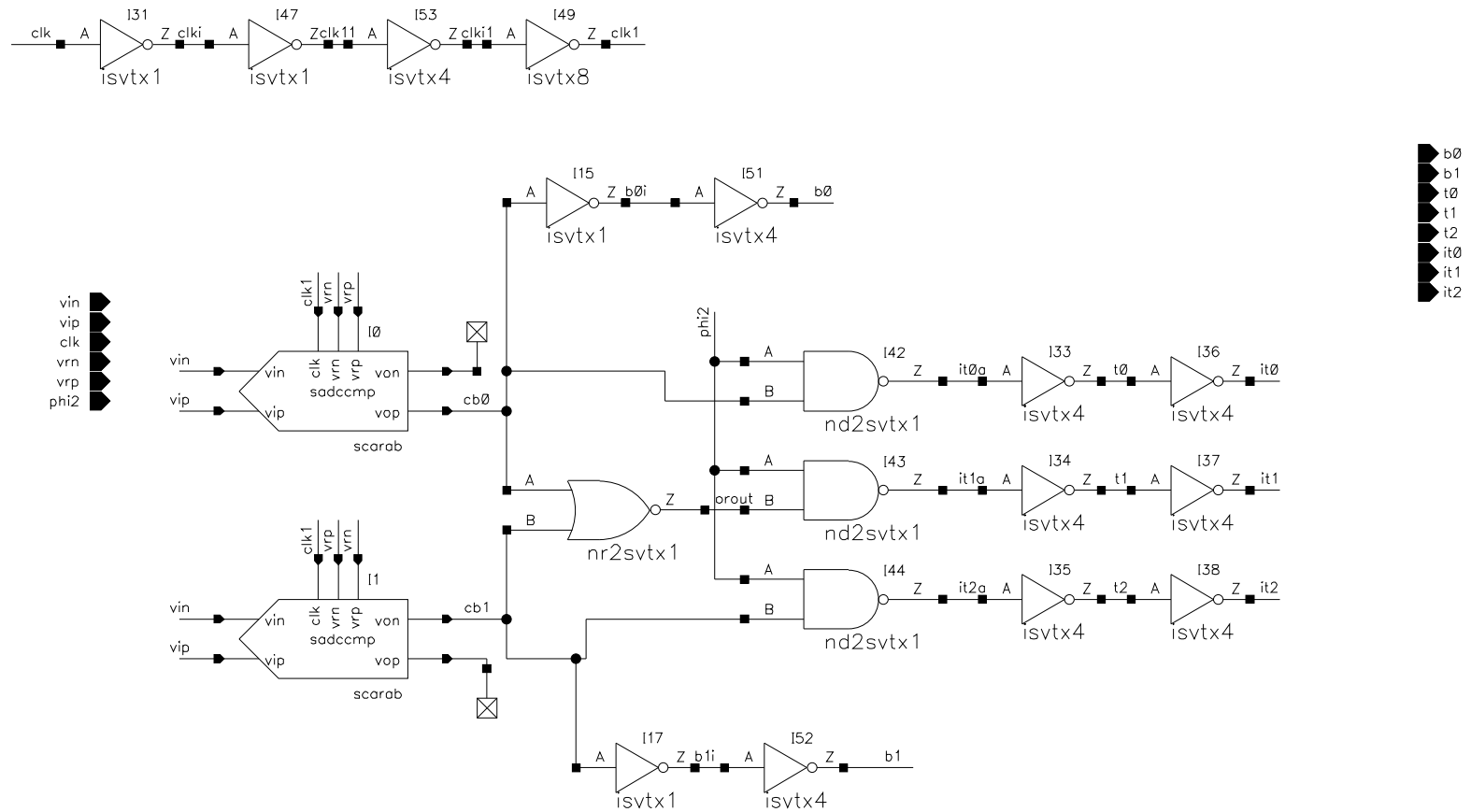
Title : Dynamic Comparator

SIZE  
A

DWG NO.

Date : Jul 16 13:08:37 2007  
Rev. :  
Author : Carsten Wulff

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Title : Sub ADC

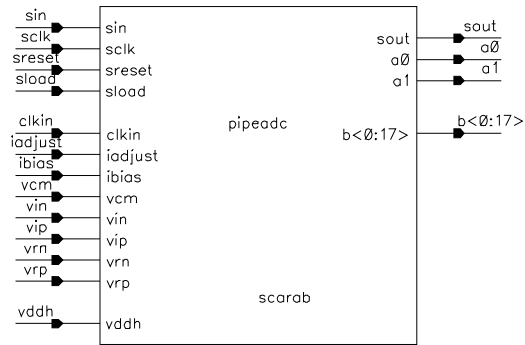
SIZE  
A

DWG NO.

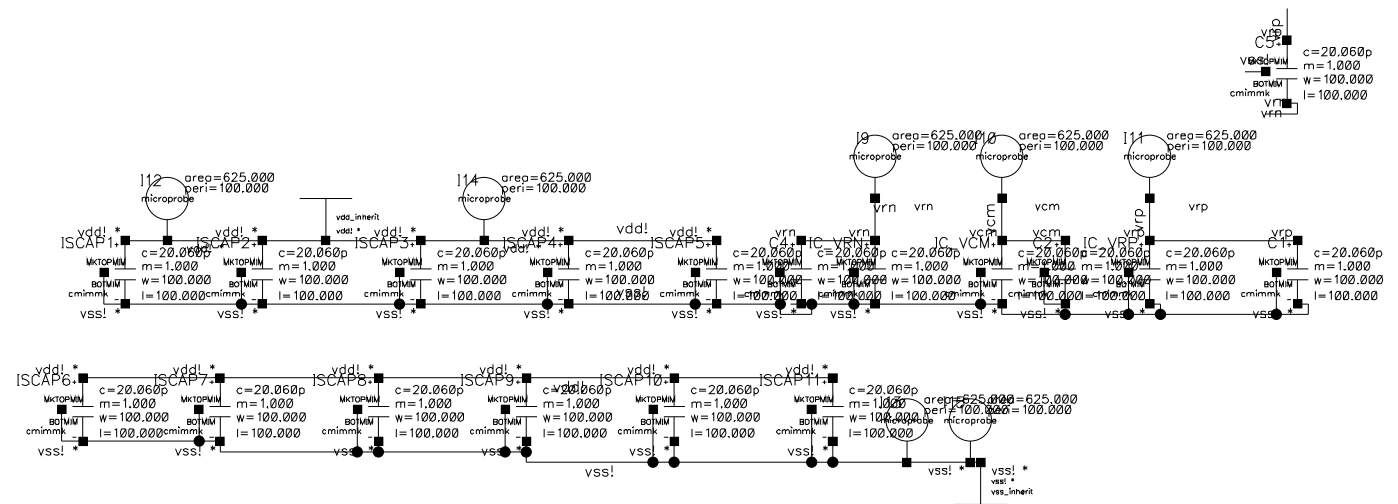
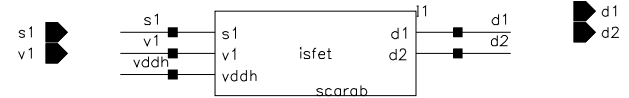
Date : Jul 16 13:08:54 2007  
Rev. :  
Author : Carsten Wulff

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sin  
sclk  
sreset  
sload  
  
clkln  
iadjust  
ibias  
vcm  
vin  
vip  
vrn  
vrp  
  
vddh



■ b<0:17>  
■ a0  
■ a1  
■ sout



Title : SCARAB\_NOPADS

SIZE  
A

DWG NO.

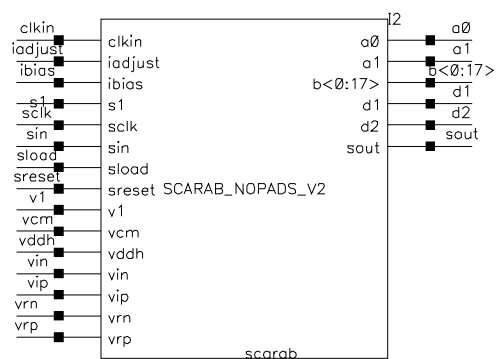
Date : Jul 17 09:53:33 2007  
Rev. :  
Author : Carsten Wulff

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sin  
sclk  
sreset  
sload  
s1  
clkkin  
iadjust  
ibias  
vcm  
vin  
vip  
vrn  
vrp  
v1  
vddh

b<0:17>  
a0  
d1  
a1  
sout  
d2



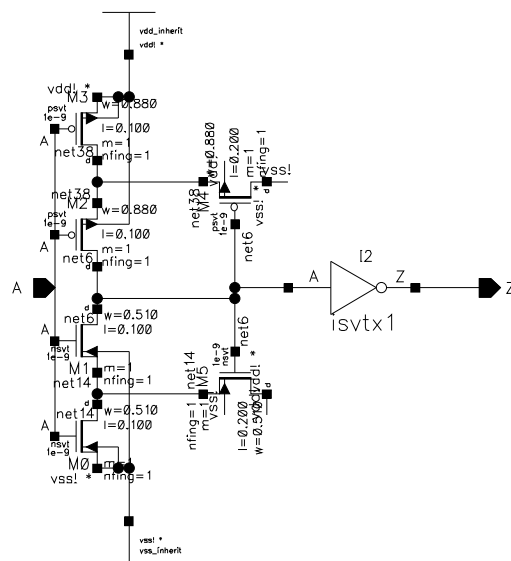
Title : SCARABP

SIZE  
A

DWG NO.

Date : Jul 16 13:43:39 2007  
Rev. :  
Author : Carsten Wulff

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Title : Schmitt Trigger

SIZE 

DWG NO.

Date : Jul 16 13:11:52 2007

Rev. :

Date : 2015-10-15 13:11:52 Z  
Rev. :  
Author : Carsten Wulff

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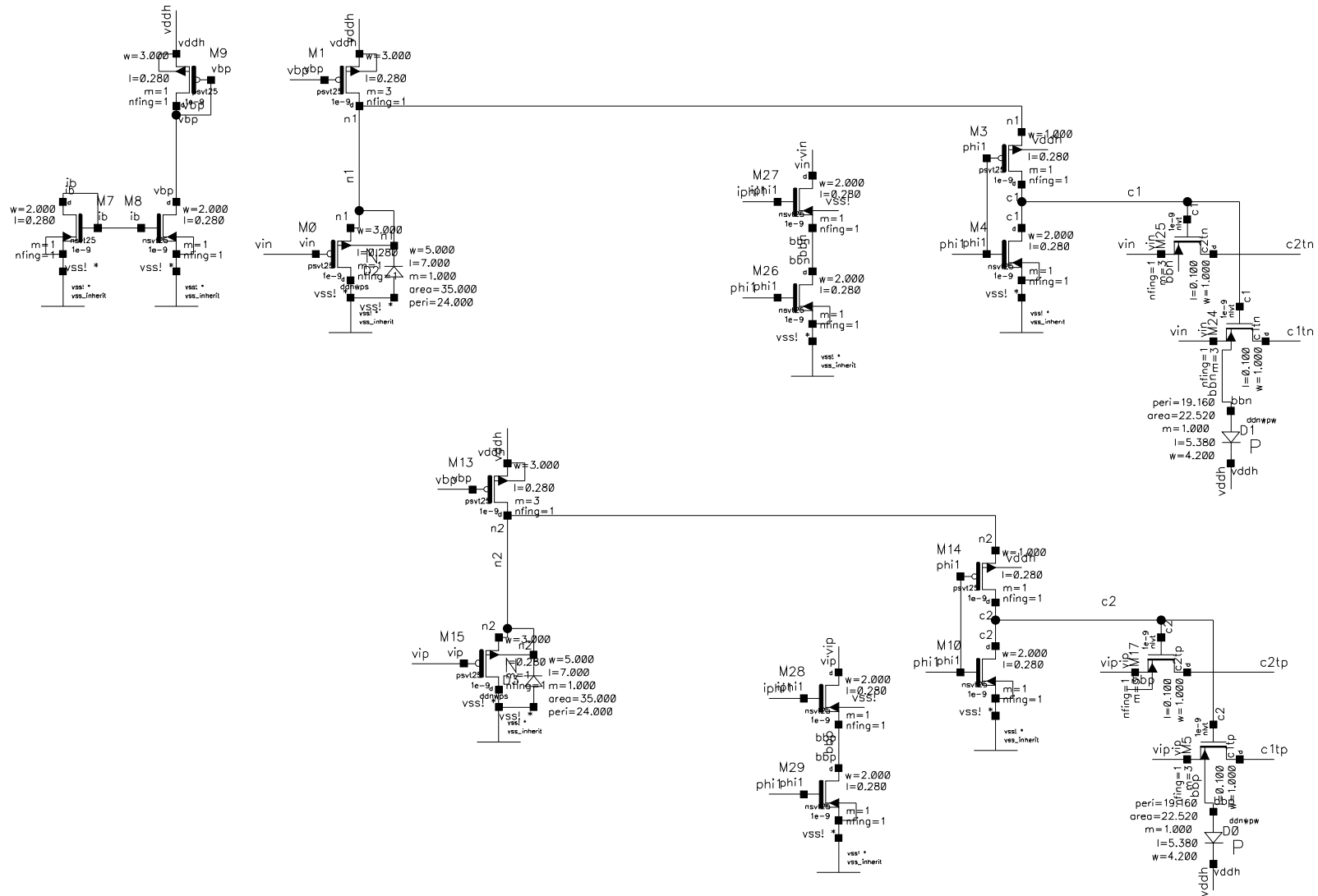
B

Date : Jul 16 13:10:18 2007  
Rev. :  
Author : Carsten Wulff

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iphi1  
vin  
vip  
phi1  
ib  
vddh

c2tn  
c1tn  
c2tp  
c1tp



Title : Continuous Time Bootstrapped Switch

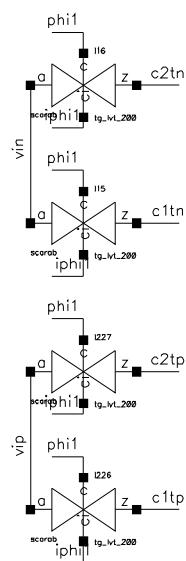
SIZE

DWG NO.

Date : Jul 16 13:08:44 2007  
Rev. :  
Author : Carsten Wulff

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vin  
vip  
phi1  
iphi1



c2tn  
c1tn  
c2tp  
c1tp

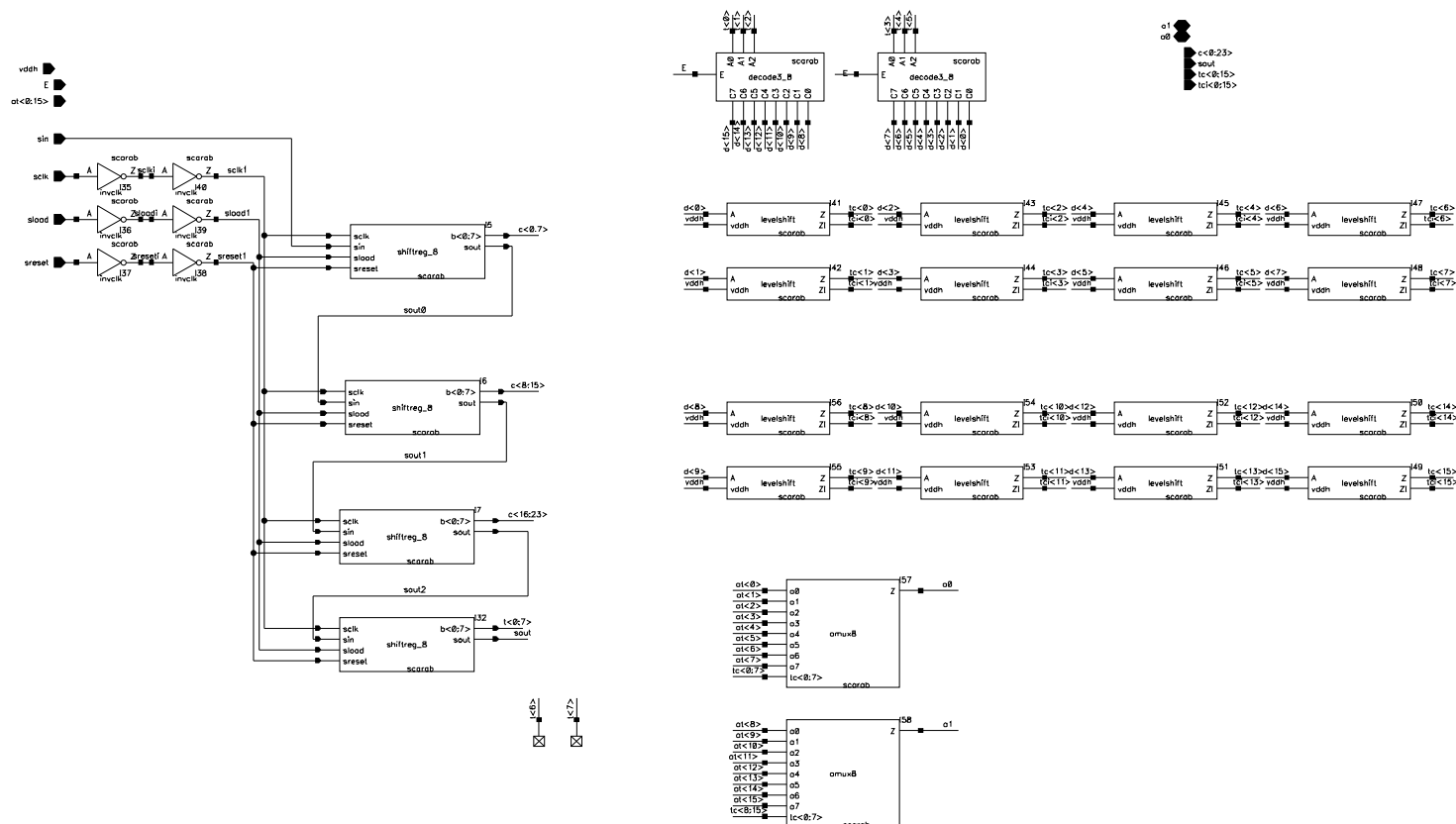
Title : Input switch

SIZE  
A

DWG NO.

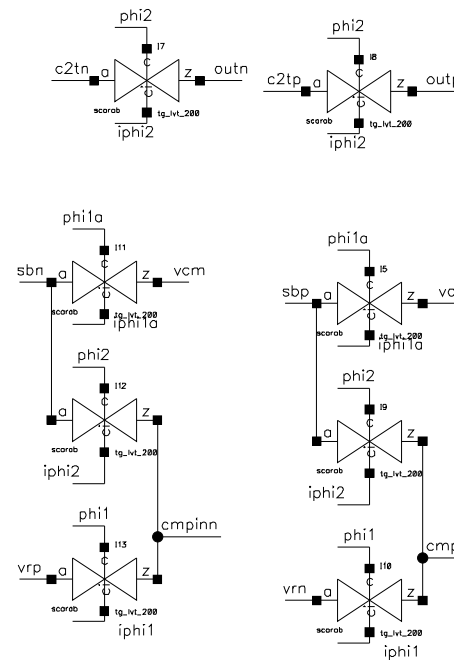
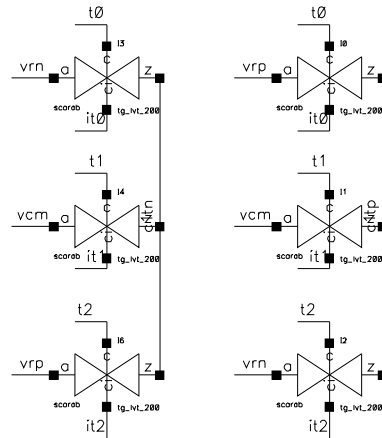
Date : Jul 16 13:11:04 2007  
Rev. :  
Author : Carsten Wulff

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phi1  
 phi1a  
 phi2  
 t0  
 t1  
 t2  
 vcm  
 vrn  
 vrp  
  
 c1tn  
 c2tn  
 c2tp  
 c1tp

iphi1  
 iphi2  
 iphi1a  
 it0  
 it1  
 it2



outp  
 outn  
 cmpinn  
 cmpinp  
 sbn  
 sbp

Title : Stage Transmission Gates

SIZE A

DWG NO.

Date : Jul 16 13:11:01 2007  
 Rev. :  
 Author : Carsten Wulff

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