

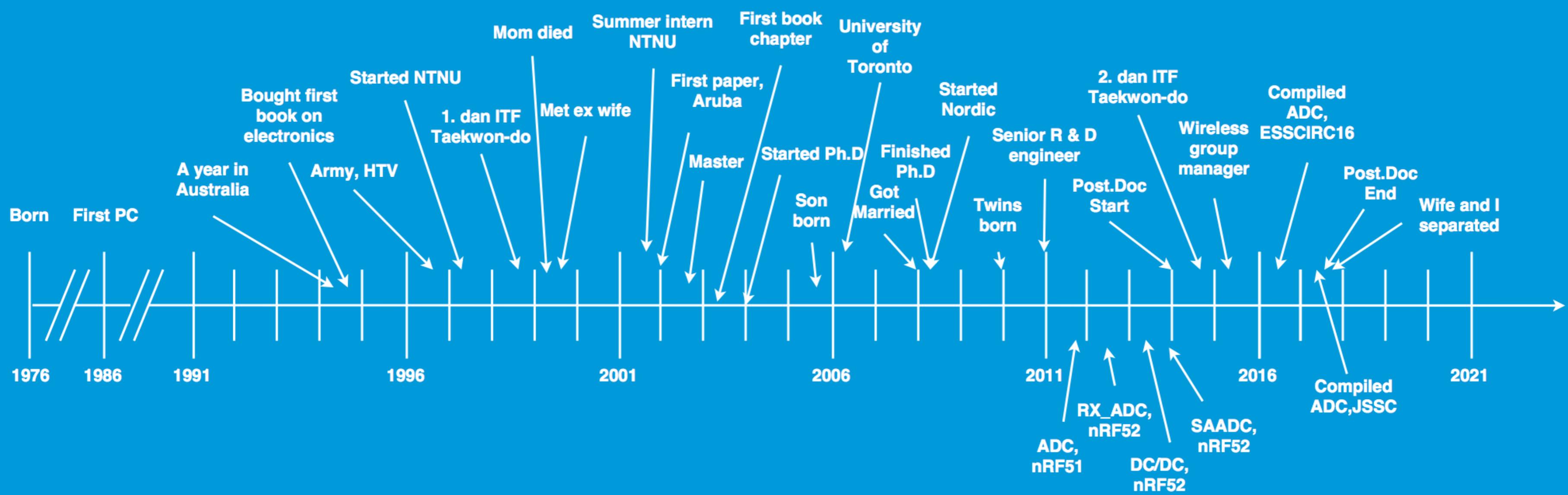
# Why do I work with electronics?

Specifically who are we, why do I do what I do, how it's made, and what we make



Carsten Wulff, 2018-08-29

# Who am I : Carsten Wulff



Who



# NORDIC SEMICONDUCTOR

Smarter Things



Svenn-Tore Larsen (CEO)  
Nordic Semiconductor  
659 employees



Svein-Egil Nielsen (CTO)  
R & D  
498 employees



Wireless  
37 employees

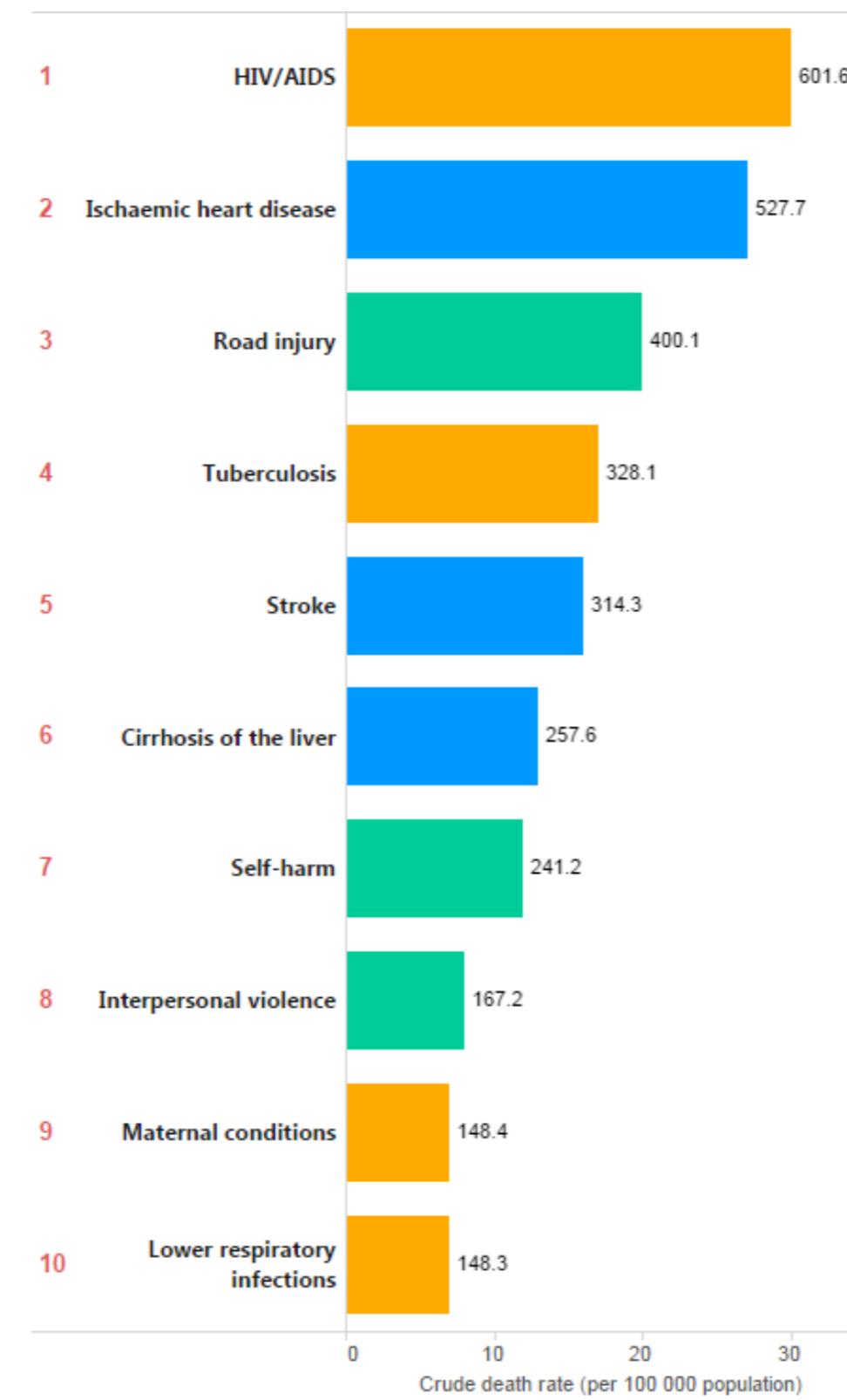
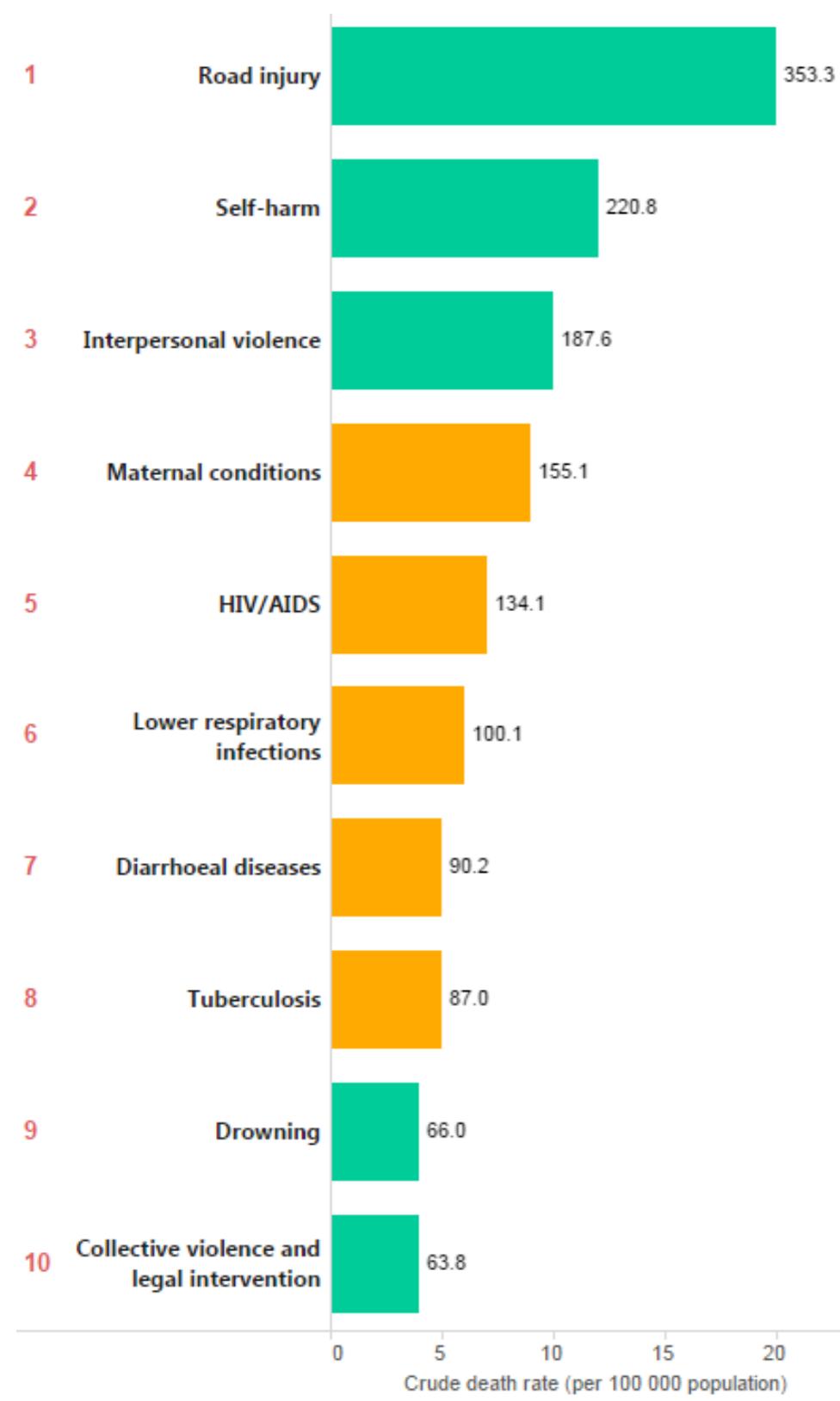


Why

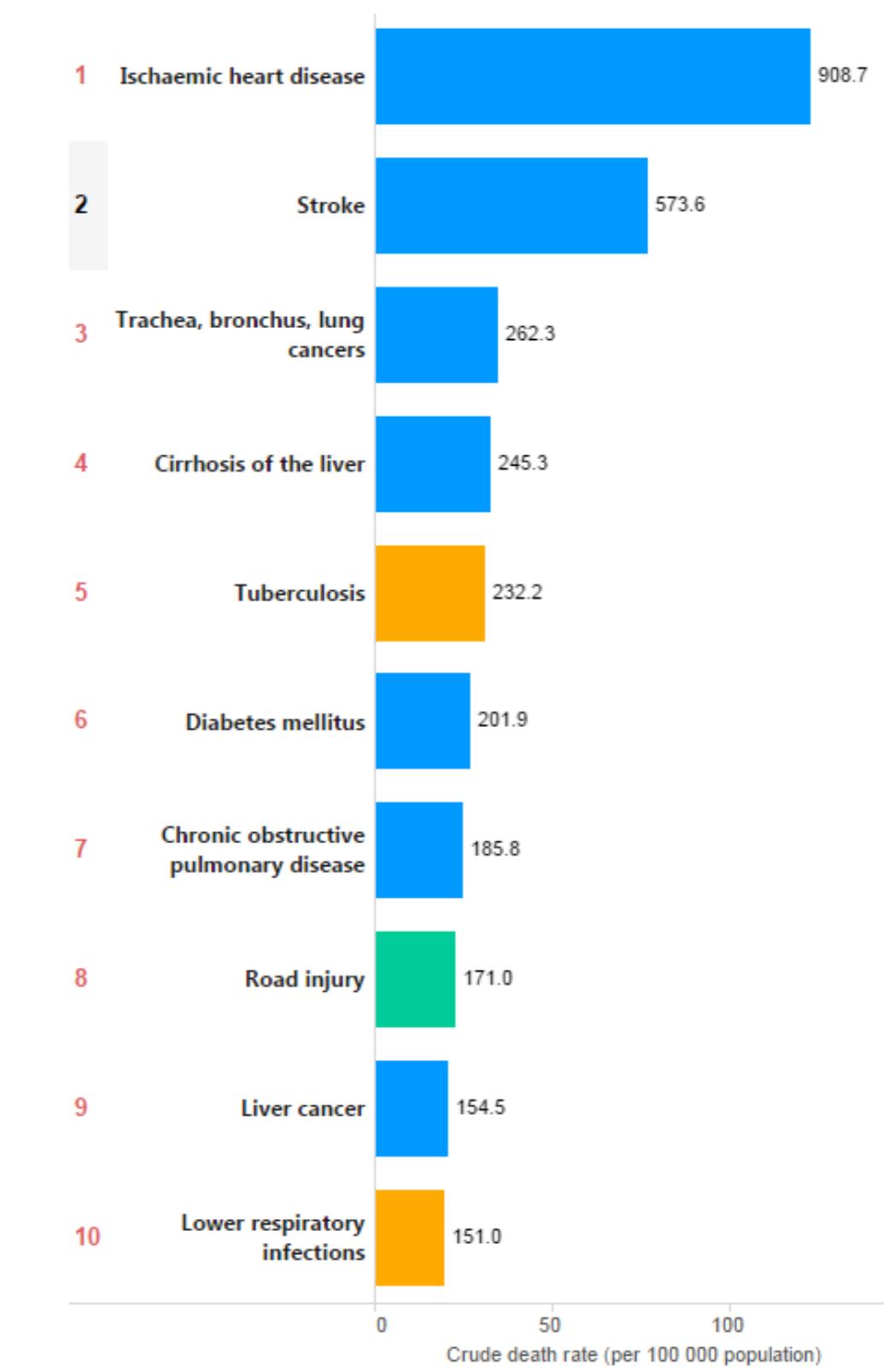
# Challenge Number 1



Source WHO



30 – 49 years of age



15 – 29 years of age

50 - 59 years of age

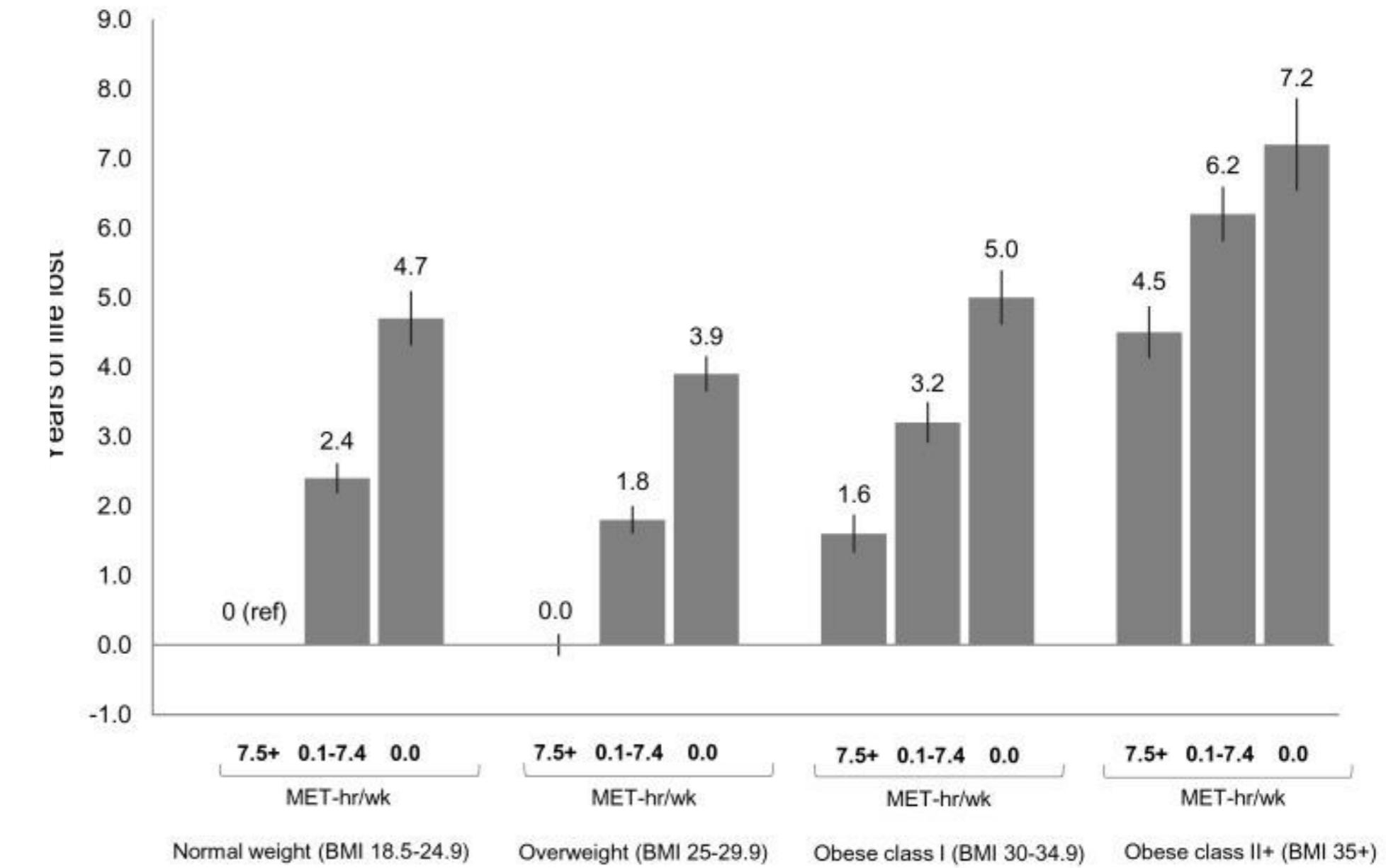
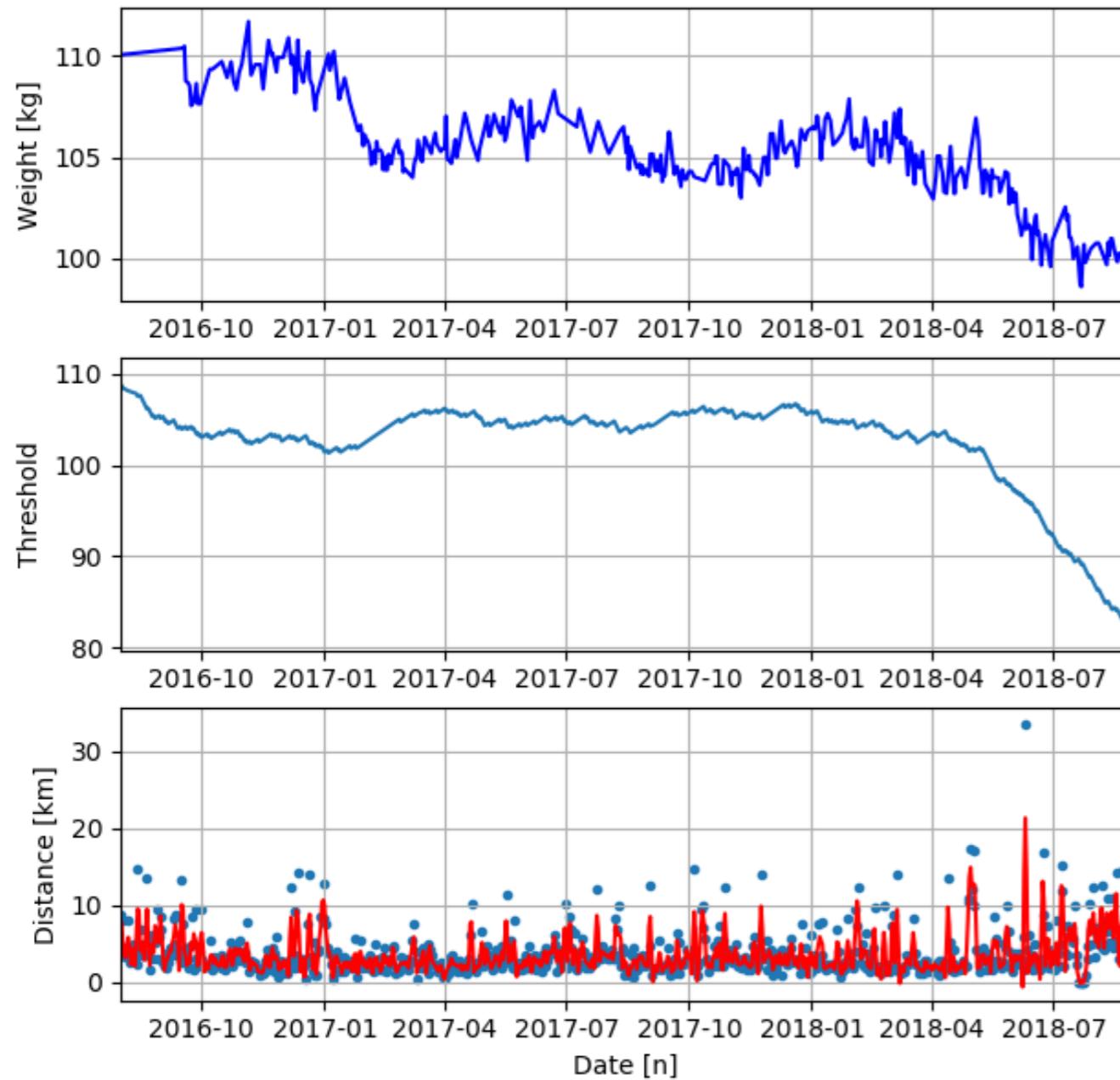
... cardiovascular diseases killed  
17.689 million people in 2015,  
that's 31.3% of all deaths ... WHO

# Personal motivation

Max: 2011 @ 122 Kg



# Activity matters



Threshold:

```
if( heart rate max on a day > 75 %){ thres[n] = thres[n-1] -0.3 }
else {thres[n] = thres[n-1] + 0.1 }
```

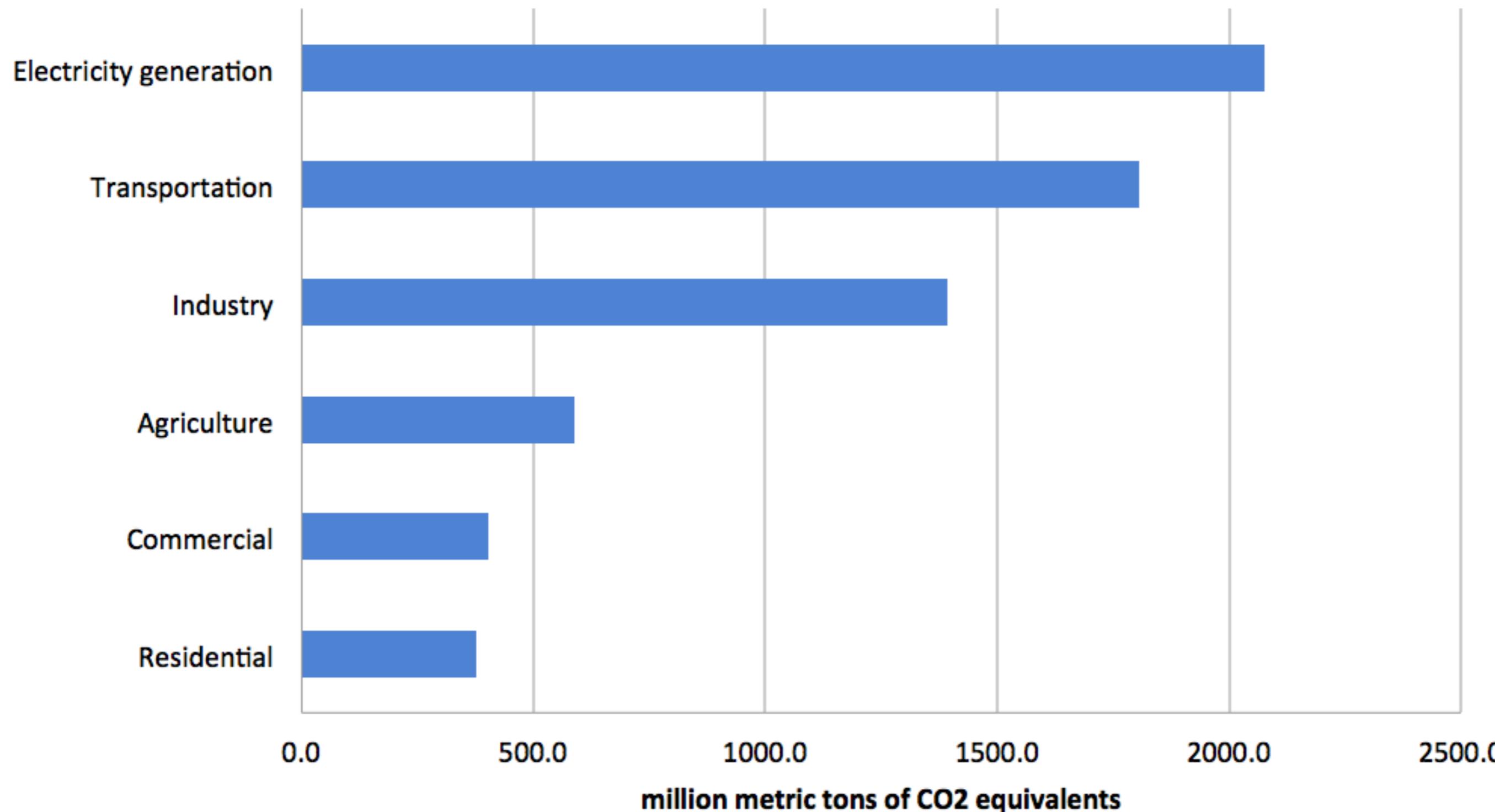
<https://www.ncbi.nlm.nih.gov/pubmed/23139642>



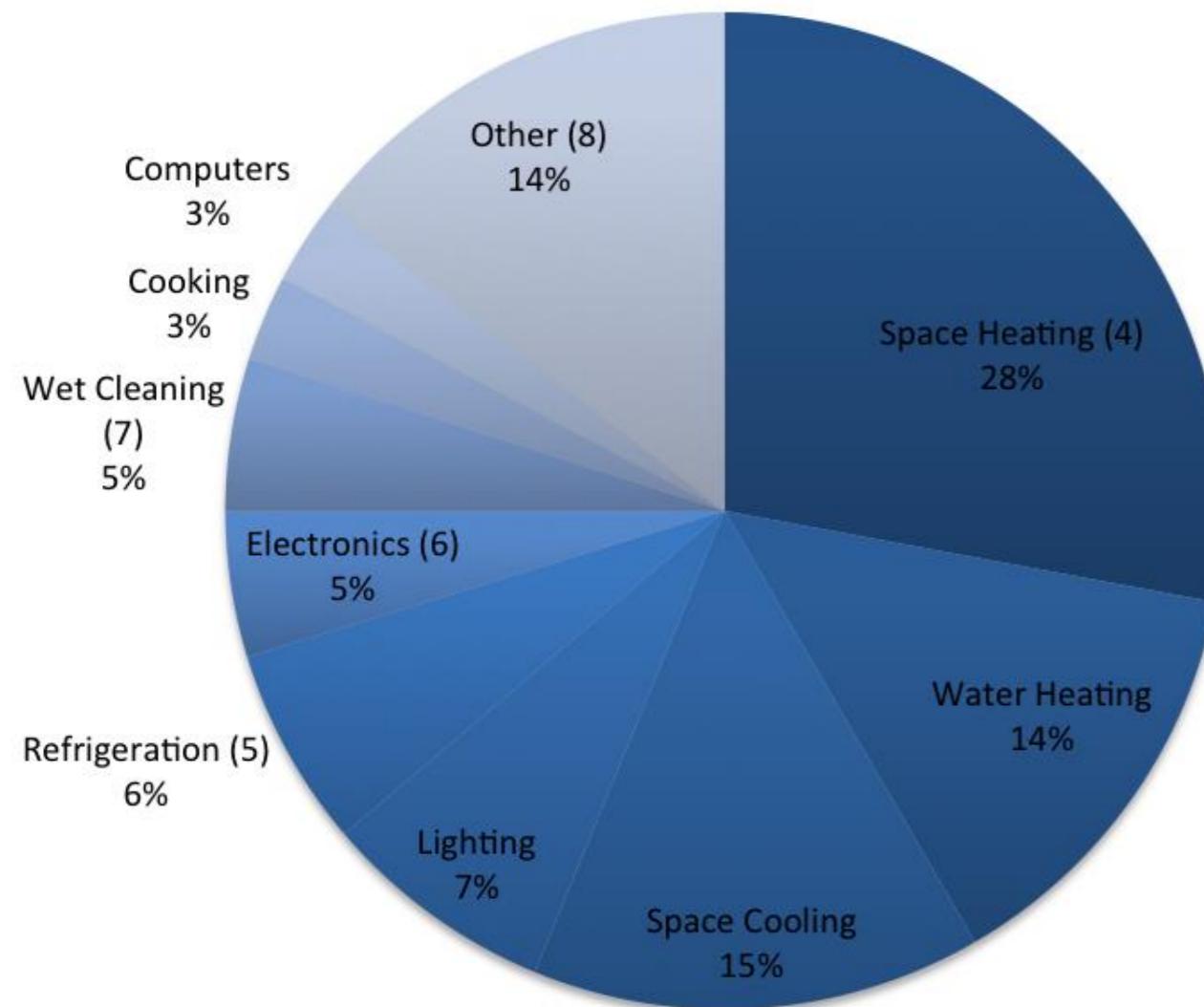


Challenge Number 2

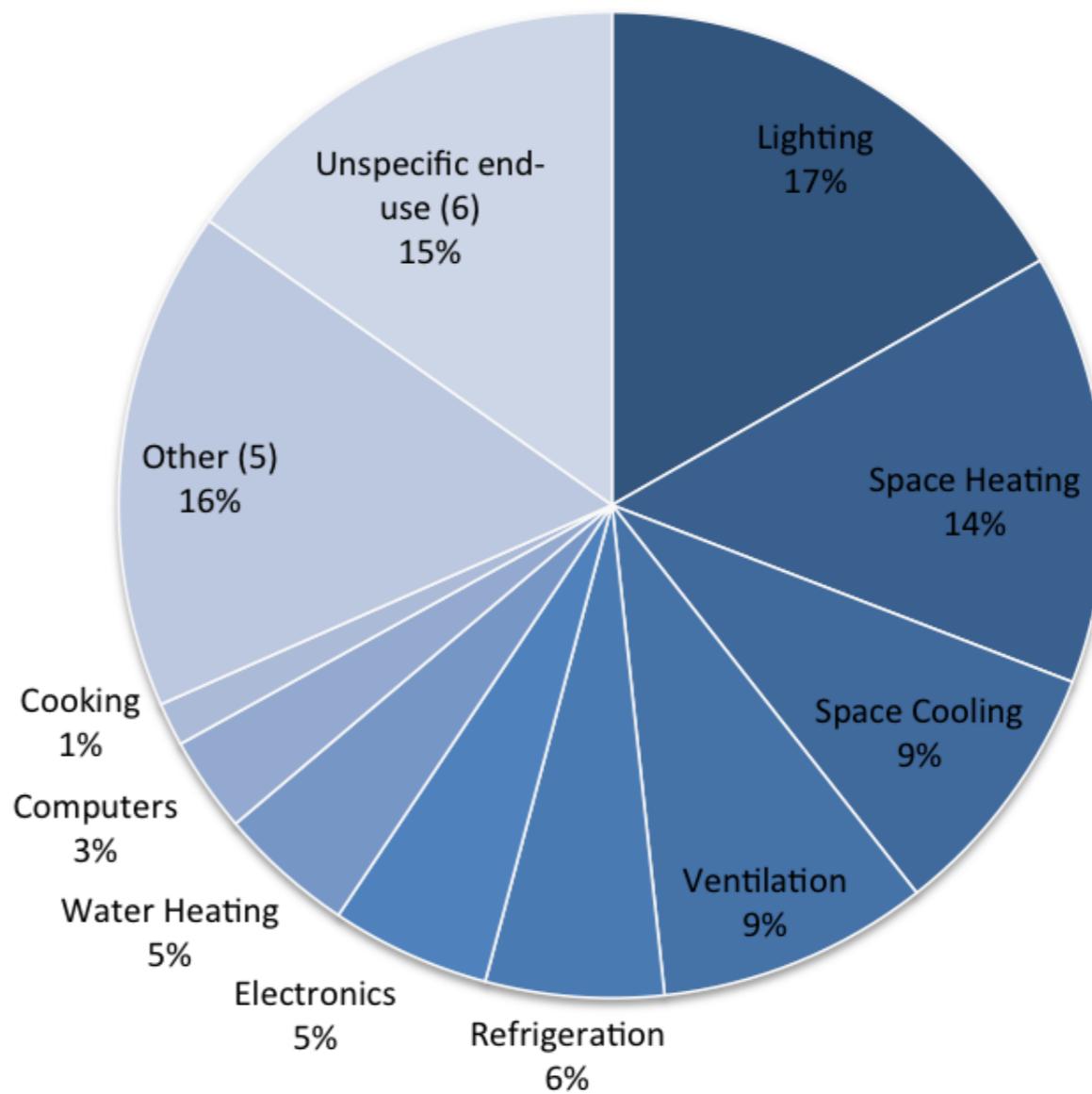
## CO2 emissions by source US



## Residential electricity usage U.S. 2015



## Commercial electricity usage U.S 2015



The primary way that IoT can help battle climate change is by reducing global energy consumption, which will in turn reduce carbon emissions.

— Michael Miller, *The Internet of Things: How Smart TVs, Smart Cars, Smart Homes, and Smart Cities Are Changing the World*

H O W

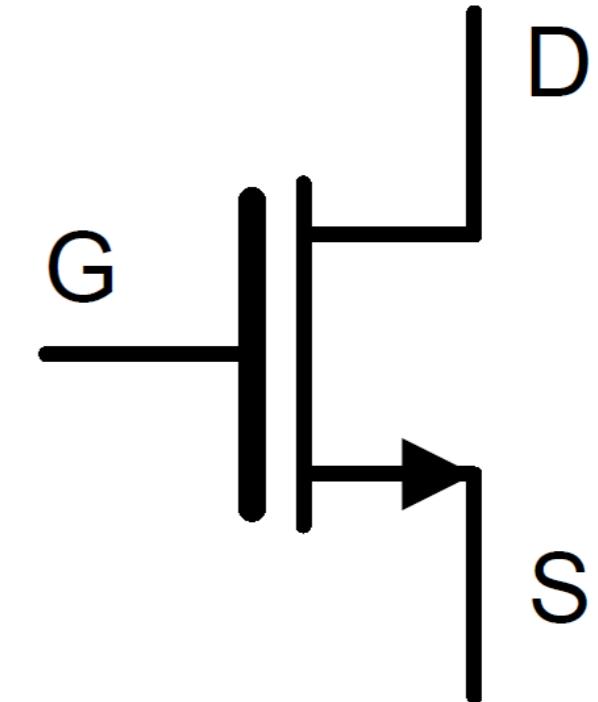
# Transistor



# Transistor

- › The most important device in an integrated circuit.
- › An extremely complicated device
- › Need computer models to describe the behavior accurately.
- › BSIM model published in 1987, 17 parameters to describe a transistor.

This is similar what you find in textbooks. Applies to 1um transistor lengths.



558

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-22, NO. 4, AUGUST 1987

## BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors

BING J. SHEU, MEMBER, IEEE, DONALD L. SCHARFETTER, FELLOW, IEEE, PING-KEUNG KO, MEMBER, IEEE, AND MIN-CHIE JENG

**Abstract** — The Berkeley Short-channel IGFET Model (BSIM), an accurate and computationally efficient MOS transistor model, and its associated characterization facility for advanced integrated-circuit design are described. Both the strong-inversion and weak-inversion components of the drain-current expression are included. In order to speed up the circuit-simulation execution time, the dependence of the drain current on the substrate bias has been modeled with a numerical approximation. This approximation also simplifies the transistor terminal charge expressions. The charge model was derived from its drain-current counterpart to

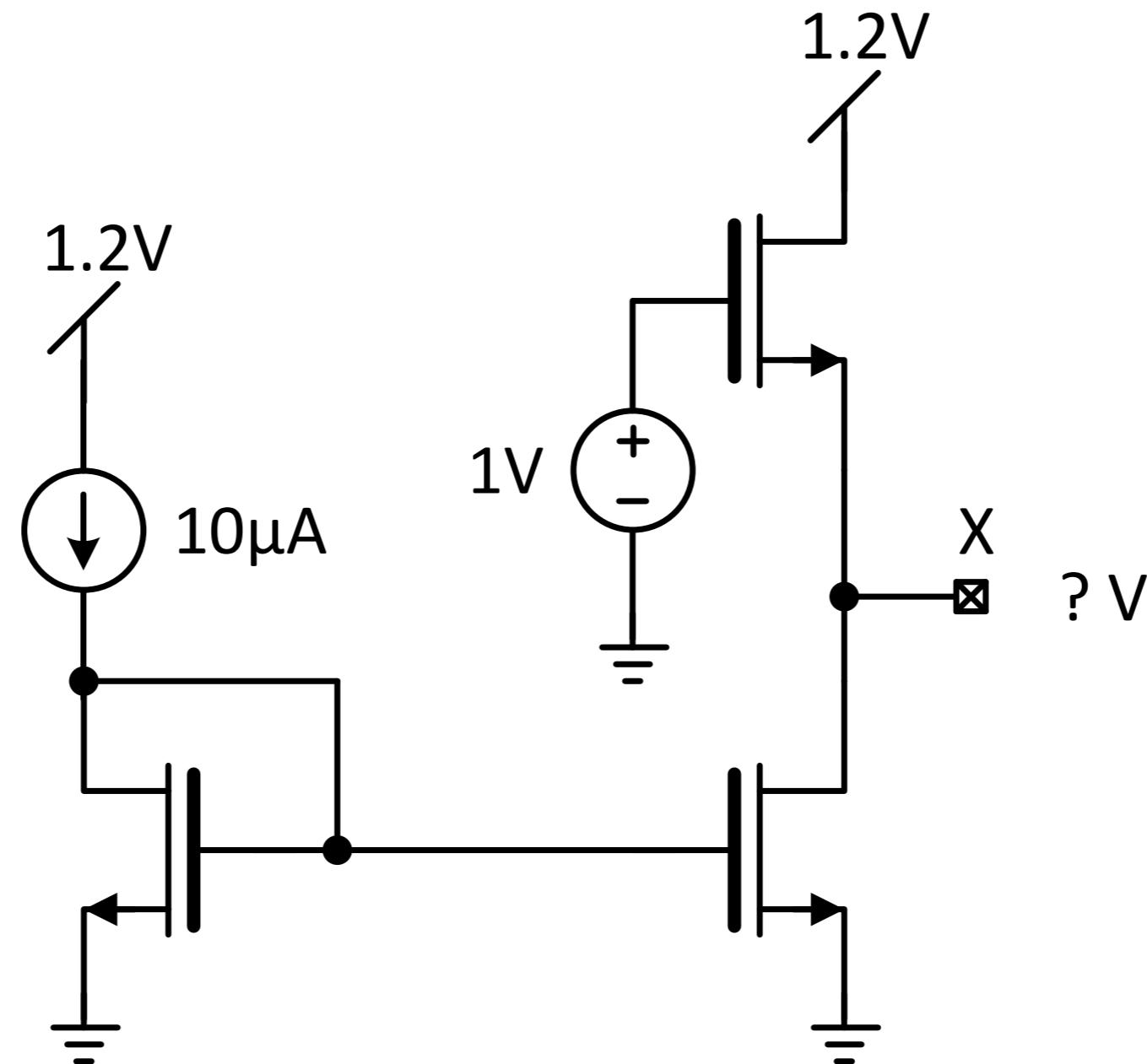
only as accurate as the models used. In the past, the SPICE2 program has provided three built-in MOS transistor models [6]. The Level-1 model, which contains fairly simple expressions, is most suitable for preliminary analysis. The Level-2 model, which contains expressions from detailed device physics, does not work well for small-geometry transistors. The Level-3 model represents an attempt to pursue the semi-empirical modeling approach

3. *Saturation Region [ $V_{GS} > V_{th}$  and  $V_{DS} \geq V_{D\text{SAT}}$ ]:*

$$I_{DS} = \frac{\mu_0}{[1 + U_0(V_{GS} - V_{th})]} \cdot \frac{C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2}{2aK}$$

# BSIM 4.5 = 284 parameters

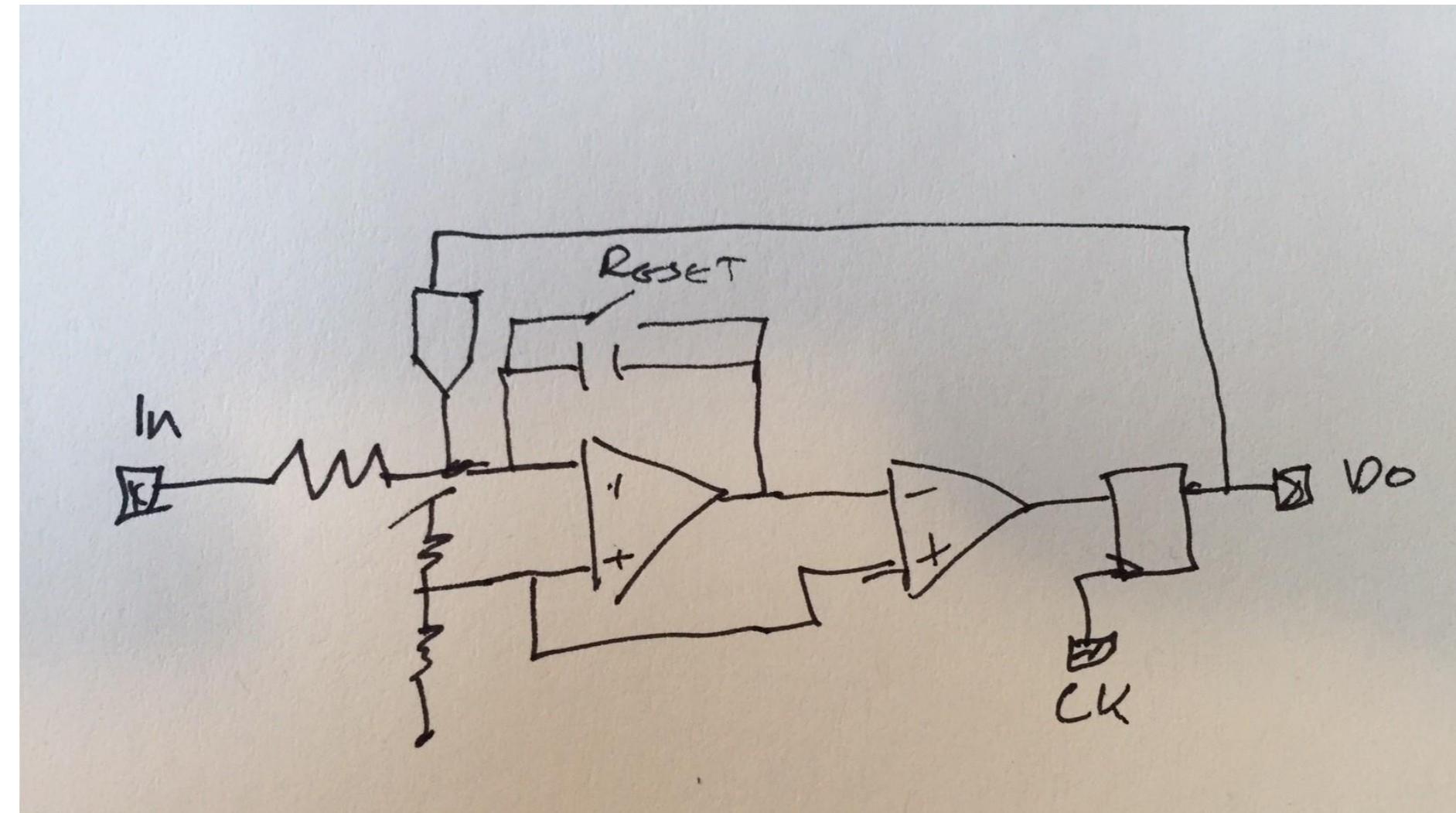
```
.MODEL N1 NMOS LEVEL=14 VERSION=4.5.0 BINUNIT=1 PARAMCHK=1 MOBMOD=0 CAPMOD=2 IGMOD=1 IGBMOD=1 GEOMOD=1 DIOMOD=1 RDMSMOD=0 RBODYMOD=0 RGATEMOD=3 PERMOD=1 ACNQSMOD=0 TRNQSMOD=0 TEMPMOD=0 TNOM=27 TOXE=1.8E-009 TOXP=10E-010 TOXM=1.8E-009 DTOX=8E-10 EPSROX=3.9 WINT=5E-009 LINT=1E-009 LL=0 WL=0 LLN=1 WLN=1 LW=0 WW=0 LWN=1 WWN=1 LWL=0 WWL=0 XPART=0 TOXREF=1.4E-009 SAREF=5E-6 SBREF=5E-6 WLOD=2E-6 KU0=-4E-6 KVSAT=0.2 KVTH0=-2E-8 TKU0=0.0 LLODKU0=1.1 WLODKU0=1.1 LLODVTH=1.0 WLODVTH=1.0 LKU0=1E-6 WKU0=1E-6 PKU0=0.0 LKVTH0=1.1E-6 WKVTH0=1.1E-6 PKVTH0=0.0 STK2=0.0 LODK2=1.0 STETA0=0.0 LODETA0=1.0 LAMBDA=4E-10 VSAT=1.1E 005 VTL=2.0E5 XN=6.0 LC=5E-9 RNOIA=0.577 RNOIB=0.37 LINTNOI=1E-009 WPEMOD=0 WEB=0.0 WEC=0.0 KVTHOWE=1.0 K2WE=1.0 KUOWE=1.0 SCREF=5.0E-6 VOFF=0.0 TVFBSDOFF=0.0 VTH0=0.25 K1=0.35 K2=0.05 K3=0 K3B=0 W0=2.5E-006 DVTO=1.8 DVT1=0.52 DVT2=-0.032 DVTOW=0 DVT1W=0 DVT2W=0 DSUB=2 MINV=0.05 VOFFL=0 DVTP0=1E-007 DVTP1=0.05 LPE0=5.75E-008 LPEB=2.3E-010 XJ=2E-008 NGATE=5E 020 NDEP=2.8E 018 NSD=1E 020 PHIN=0 CDSC=0.0002 CDSCB=0 CDSCD=0 CIT=0 VOFF=-0.15 NFACTOR=1.2 ETA0=0.05 ETAB=0 UC=-3E-011 VFB=-0.55 U0=0.032 UA=5.0E-011 UB=3.5E-018 AO=2 AGS=1E-020 A1=0 A2=1 BO=-1E-020 B1=0 KETA=0.04 DWG=0 DWB=0 PCLM=0.08 PDIBLC1=0.028 PDIBLC2=0.022 PDIBLCB=-0.005 DROUT=0.45 PVAG=1E-020 DELTA=0.01 PSCBE1=8.14E 008 PSCBE2=5E-008 RSH=0 RDSW=0 RSW=0 RDW=0 FPROUT=0.2 PDITS=0.2 PDITSD=0.23 PDITSL=2.3E 006 RSH=0 RDSW=50 RSW=150 RDW=150 RDSWMIN=0 RDWMIN=0 RSWMIN=0 PRWG=0 PRWB=6.8E-011 WR=1 ALPHA0=0.074 ALPHA1=0.005 BETA0=30 AGIDL=0.0002 BGIDL=2.1E 009 CGIDL=0.0002 EGIDL=0.8 AIGBACC=0.012 BIGBACC=0.0028 CIGBACC=0.002 NIGBACC=1 AIGBINV=0.014 BIGBINV=0.004 CIGBINV=0.004 EIGBINV=1.1 NIGBINV=3 AIGC=0.012 BIGC=0.0028 CIGC=0.002 AIGSD=0.012 BIGSD=0.0028 CIGSD=0.002 NIGC=1 POXEDGE=1 PIGCD=1 NTOX=1 VFBSDOFF=0.0 XRCRG1=12 XRCRG2=5 CGSO=6.238E-010 CGDO=6.238E-010 CGBO=2.56E-011 CGDL=2.495E-10 CGSL=2.495E-10 CKAPPAS=0.03 CKAPPAD=0.03 ACDE=1 MOIN=15 NOFF=0.9 VOFFCV=0.02 KT1=-0.37 KT1L=0.0 KT2=-0.042 UTE=-1.5 UA1=1E-009 UB1=-3.5E-019 UC1=0 PRT=0 AT=53000 FNOIMOD=1 TNOIMOD=0 JSS=0.0001 JSWS=1E-011 JSWGS=1E-010 NJS=1 IJTHSFWD=0.01 IJTHSREV=0.001 BVS=10 XJBVS=1 JSD=0.0001 JSWD=1E-011 JSWGD=1E-010 NJD=1 IJTHDFWD=0.01 IJTHDREV=0.001 BVD=10 XJBVD=1 PBS=1 CJS=0.0005 MJS=0.5 PBSWS=1 CJSWS=5E-010 MJSWS=0.33 PBSWGS=1 CJSWGS=3E-010 MJSWGS=0.33 PBD=1 CJD=0.0005 MJD=0.5 PBSWD=1 CJSWD=5E-010 MJSWD=0.33 PBSWGD=1 CJSWGD=5E-010 MJSWGD=0.33 TPB=0.005 TCJ=0.001 TPBSW=0.005 TCJSW=0.001 TPBSWG=0.005 TCJSWG=0.001 XTIS=3 XTID=3 DMCG=0E-006 DMCI=0E-006 DMDG=0E-006 DMCGT=0E-007 DWJ=0.0E-008 XGW=0E-007 XGL=0E-008 RSHG=0.4 GBMIN=1E-010 RBPB=5 RBPD=15 RBPS=15 RBDB=15 RBSB=15 NGCON=1 JTSS=1E-4 JTSD=1E-4 JTSSWS=1E-10 JTSSWD=1E-10 JTSSWGS=1E-7 JTSSWGD=1E-7 NJTS=20.0 NJTSSW=20 NJTSSWG=6 VTSS=10 VTSD=10 VTSSWS=10 VTSSWD=10 VTSSWGS=2 VTSSWGD=2 XTSS=0.02 XTSD=0.02 XTSSWS=0.02 XTSSWD=0.02 XTSSWGS=0.02 XTSSWGD=0.02
```



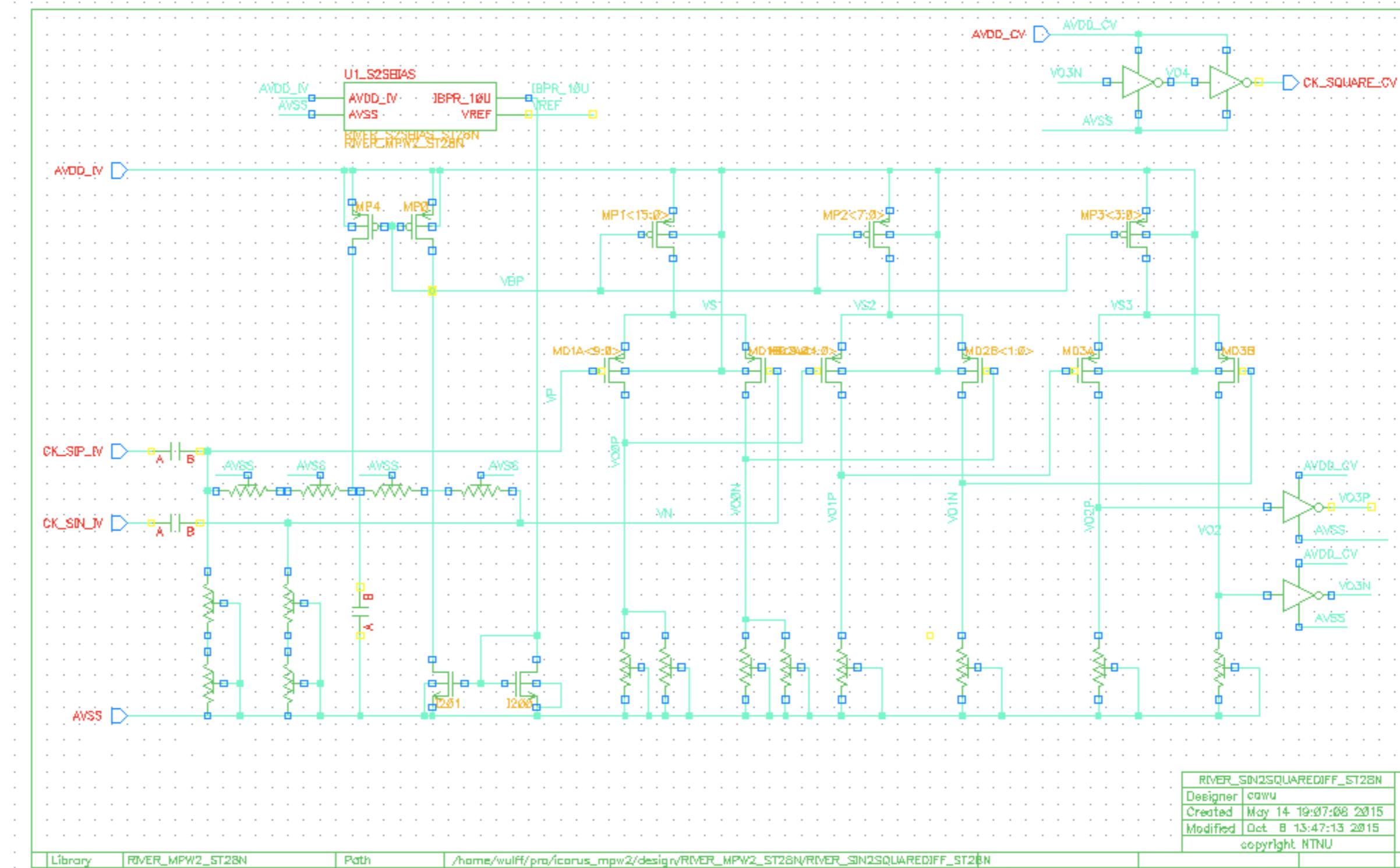
What is the voltage at node X?

# Analog Schematic Design

Typical start of design: paper and a pencil

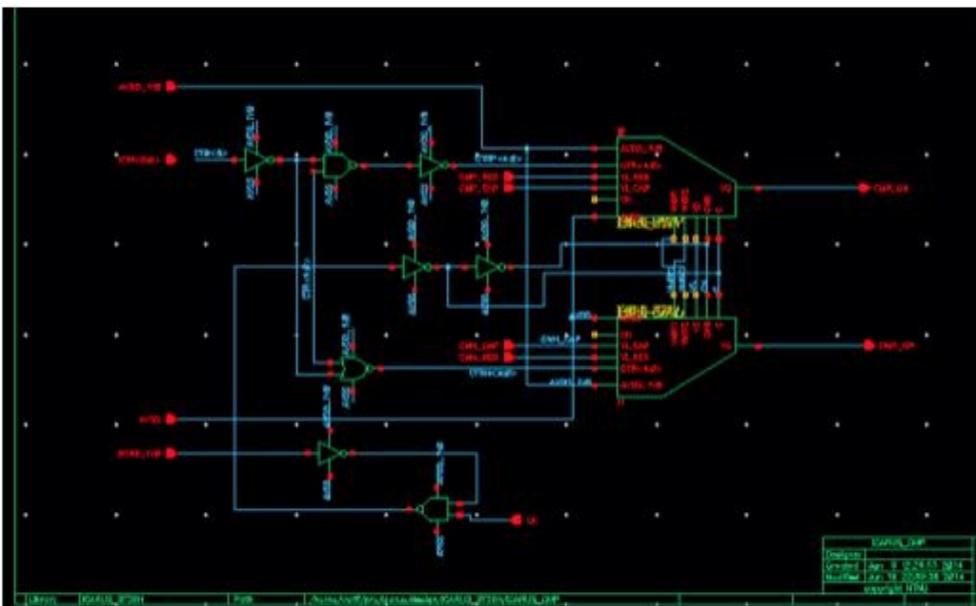


# Draw schematic

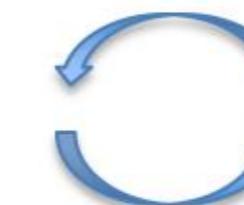
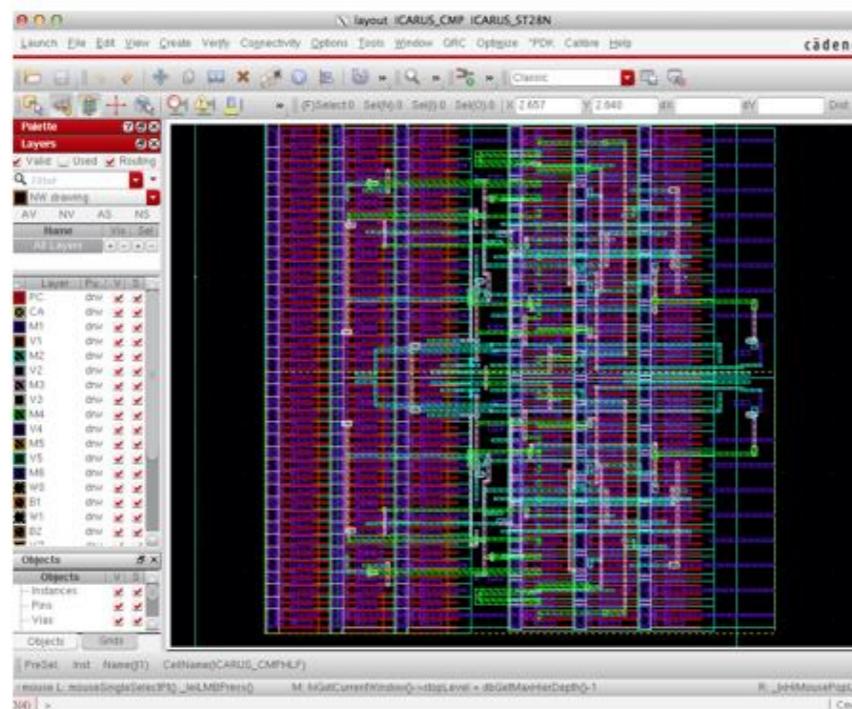


# Analog Design

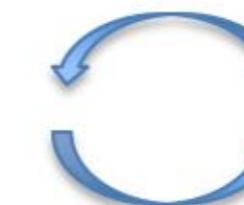
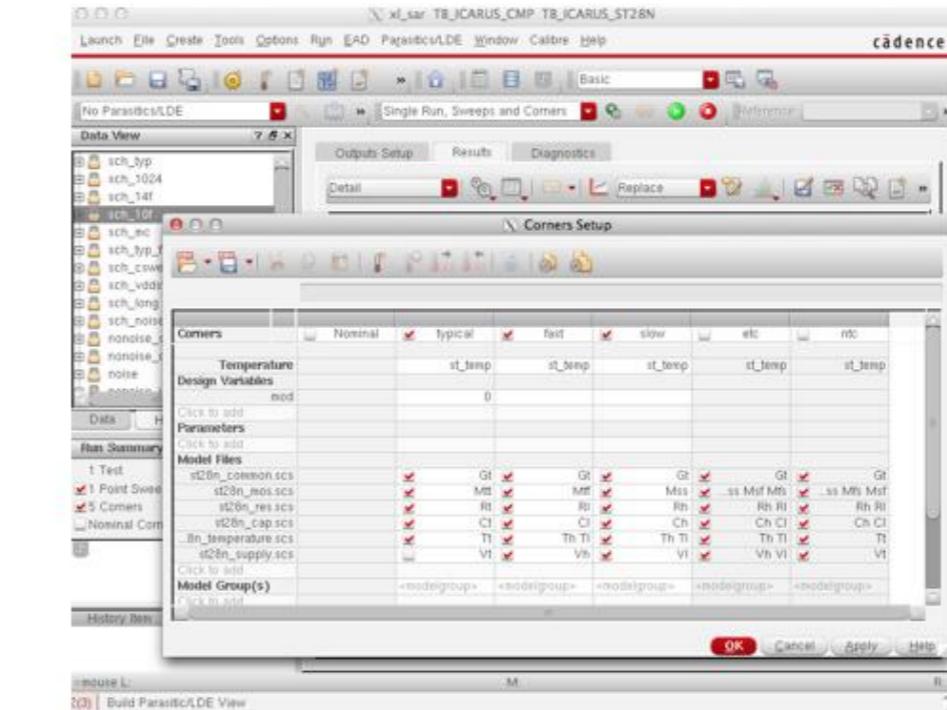
## Schematic



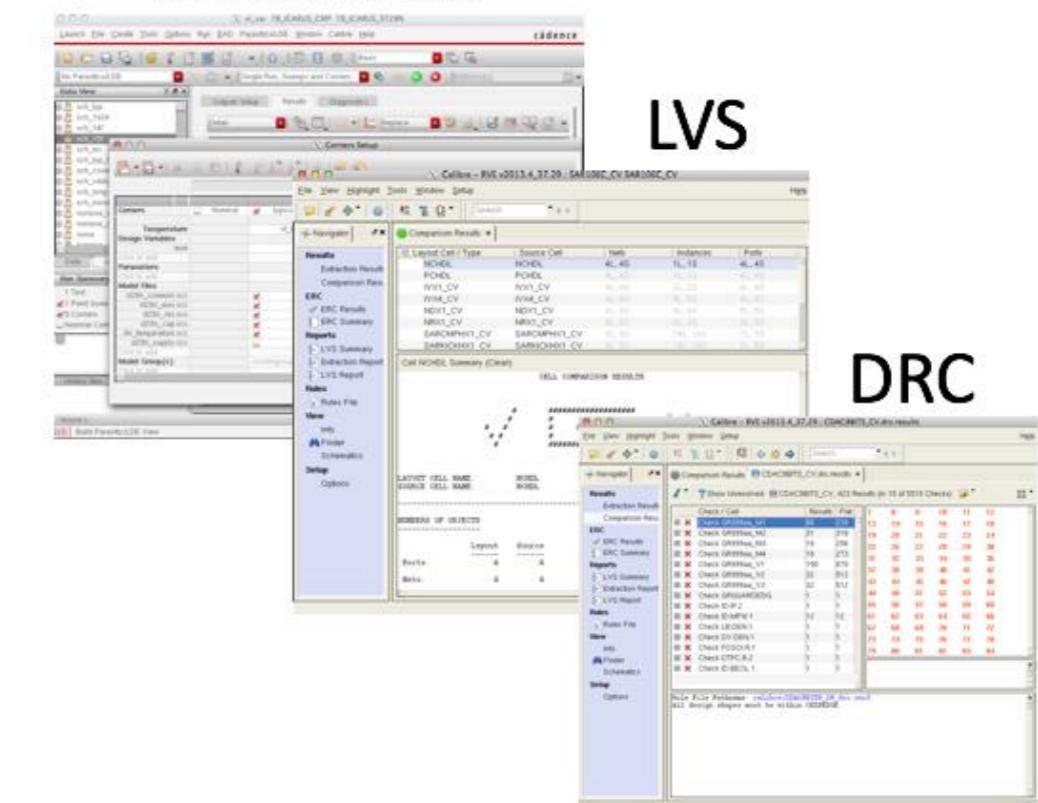
## Layout



## Simulation



## Simulation



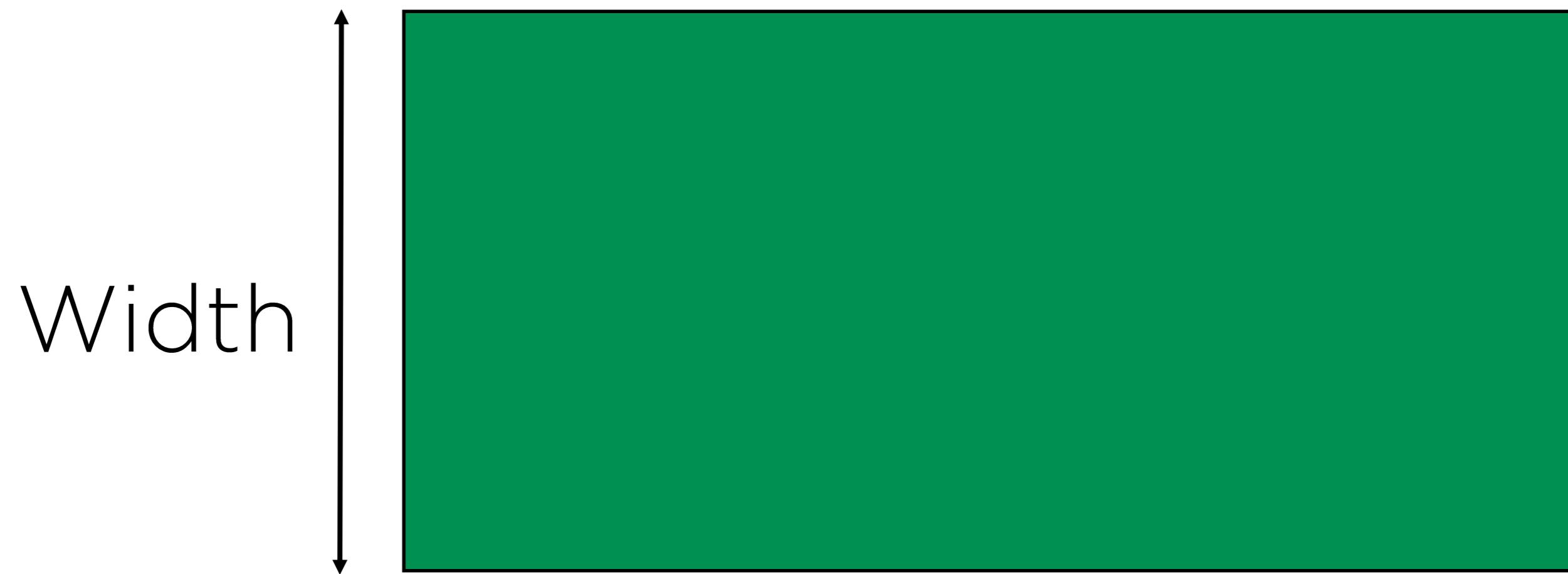
## LVS

## DRC

# Analog Layout Design

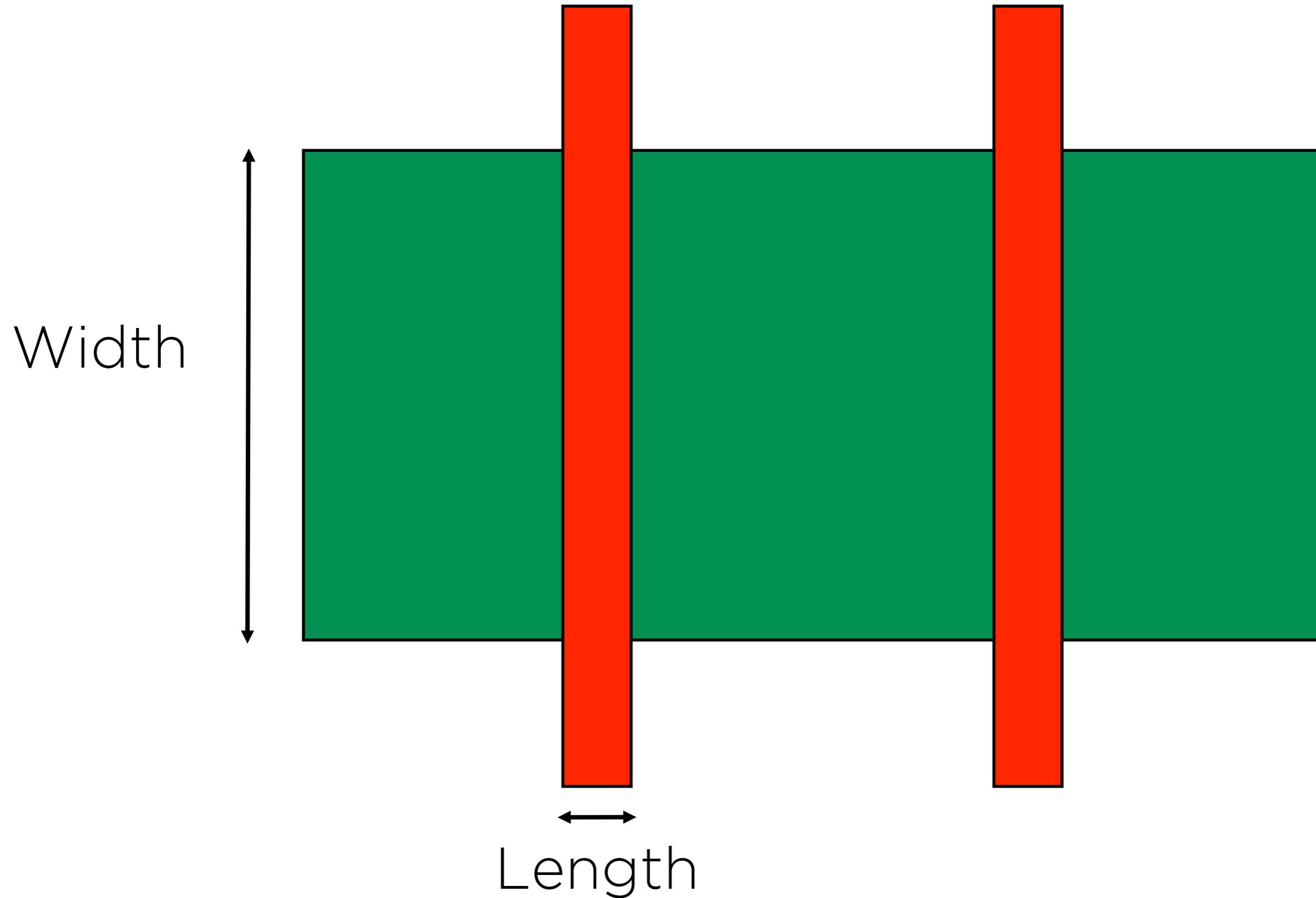
Making a GDSII file that can be sent to the foundry

# Transistor layout - Diffusion

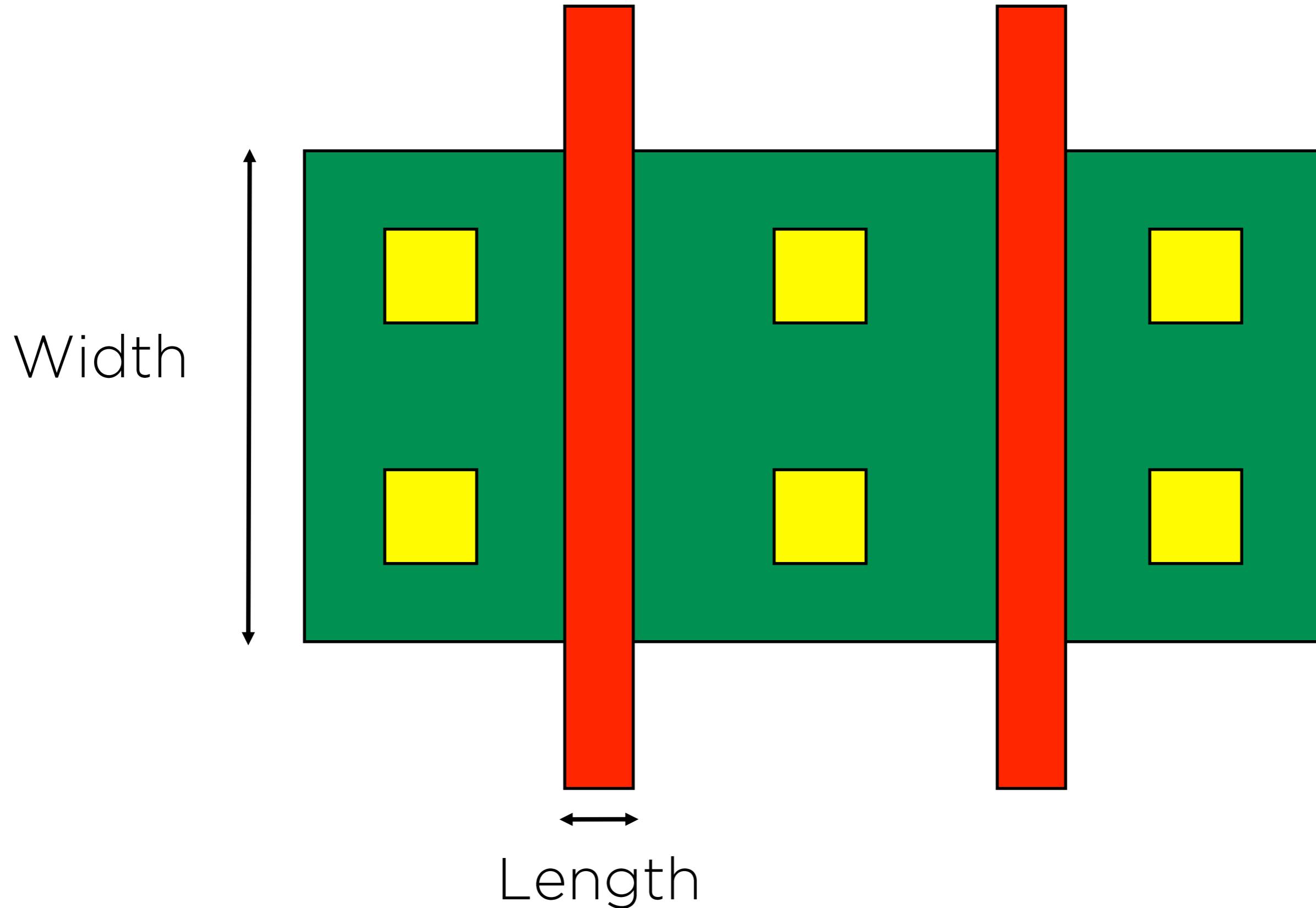


Marks the boundary of a transistor

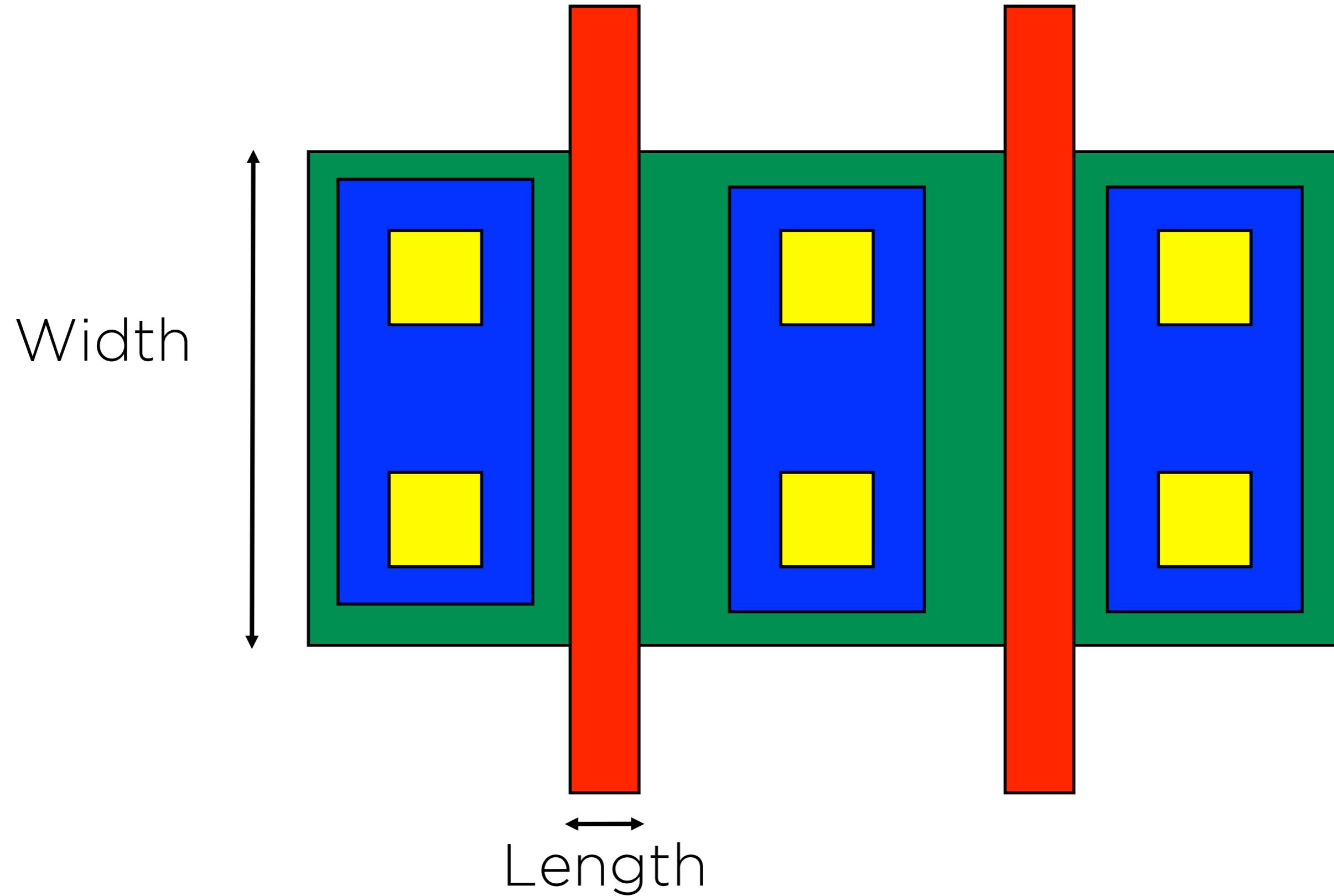
# Transistor layout - Gate



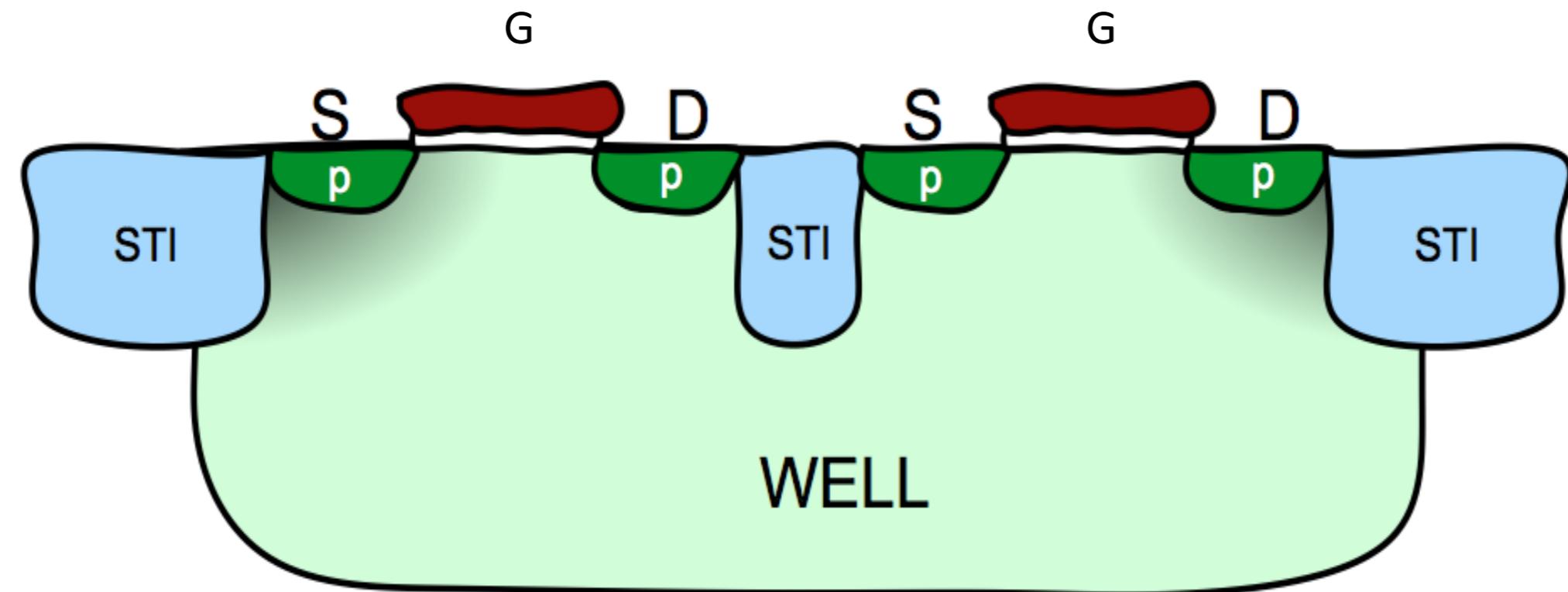
# Transistor layout - Contacts



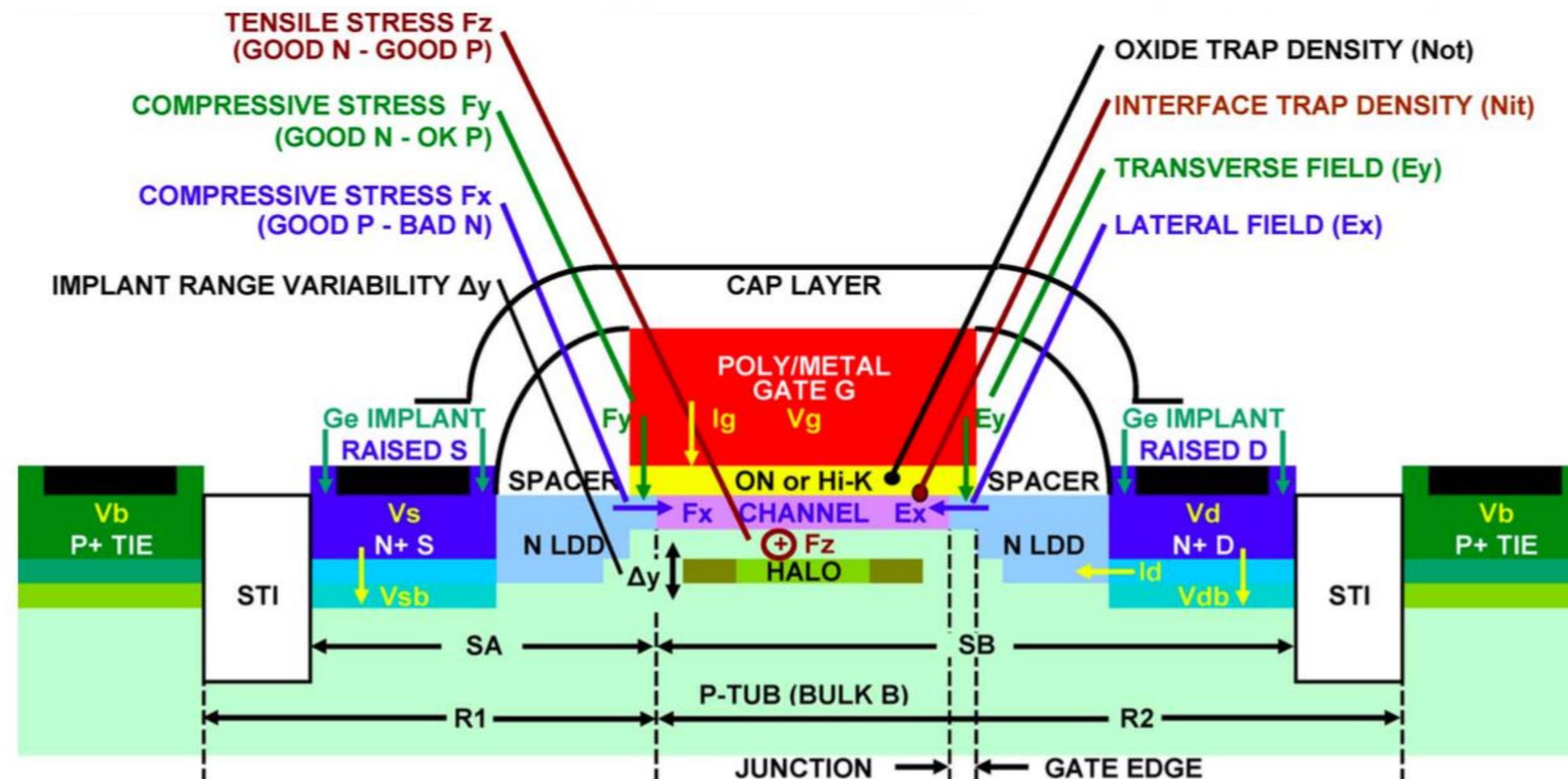
# Transistor layout - Metal 1

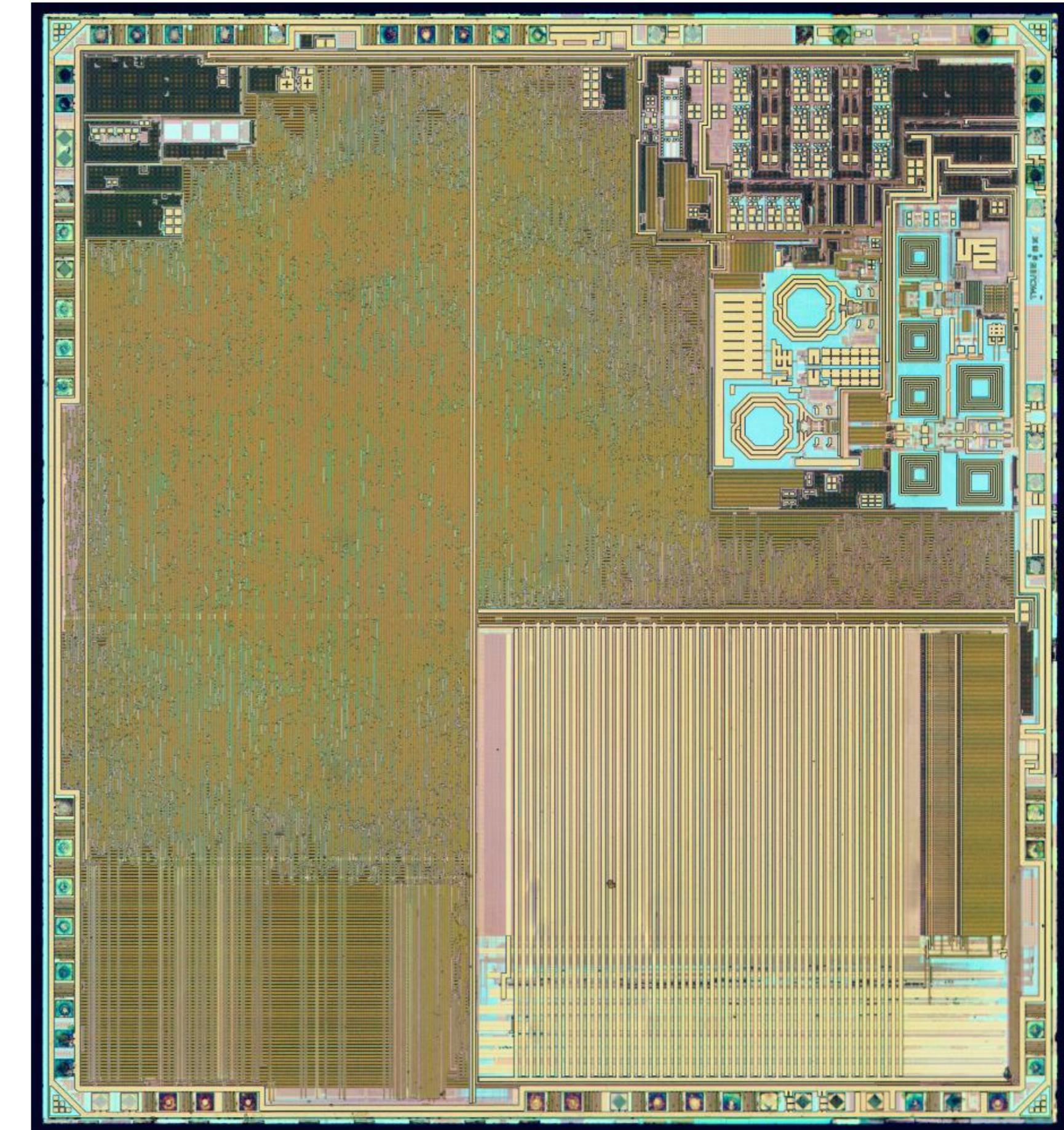


# Transistor cross section



# Real transistor cross section





# Algorithm

# Range in Wireless systems

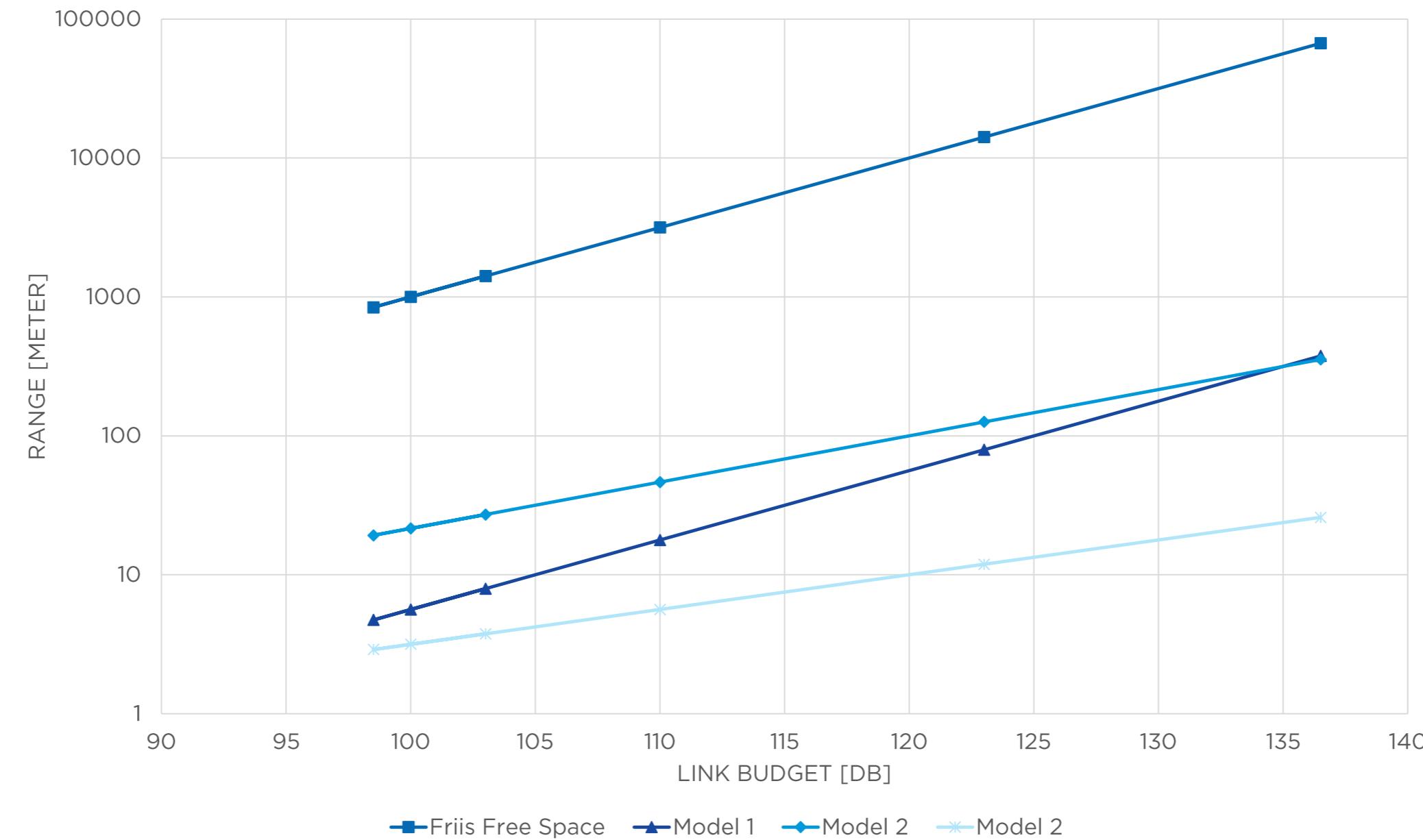
- › Assume antennas that transmit in a uniform fashion (isotropic) and without gain.
- › Assume free space
- › Friis Transmission Formula

$$FSPL [dB] = 20\log(Distance) + 20\log(frequency) - 20\log\left(\frac{4\pi}{c}\right)$$

$$\textbf{\textit{Distance at 2.4 GHz}} \sim 10^{\frac{FSPL [dB] - 40 \text{ dB}}{20}}$$

$$\textbf{\textit{Distance at 0.9 GHz}} \sim 10^{\frac{FSPL [dB] - 31 \text{ dB}}{20}}$$

# Link Budget



# Link budget = TX power - RX sensitivity

RX sensitivity = -174 dBm + 10 x log(datarate) + Noise Figure (NF) + Energy per bit/Noise (Eb/N0)



# Manufacturing ICs

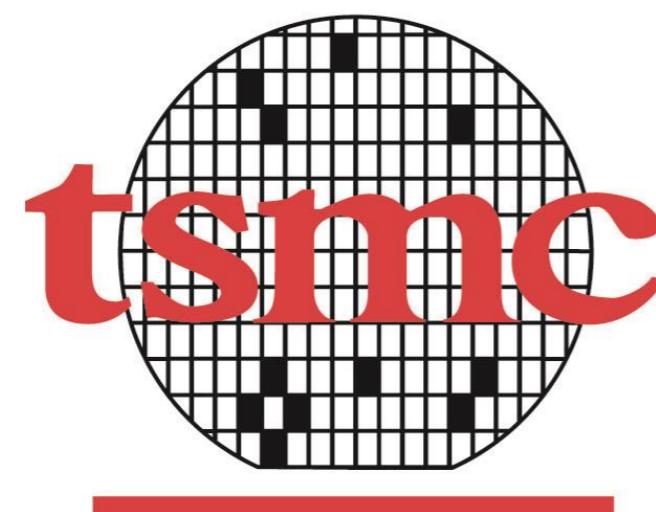
Extremely expensive



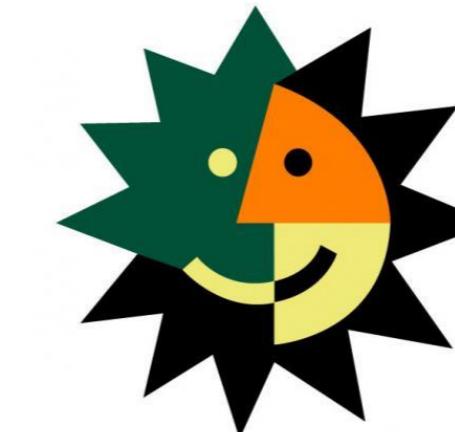
**NORDIC**  
SEMICONDUCTOR

Smarter Things

Fabless IC design: 659 (2018)



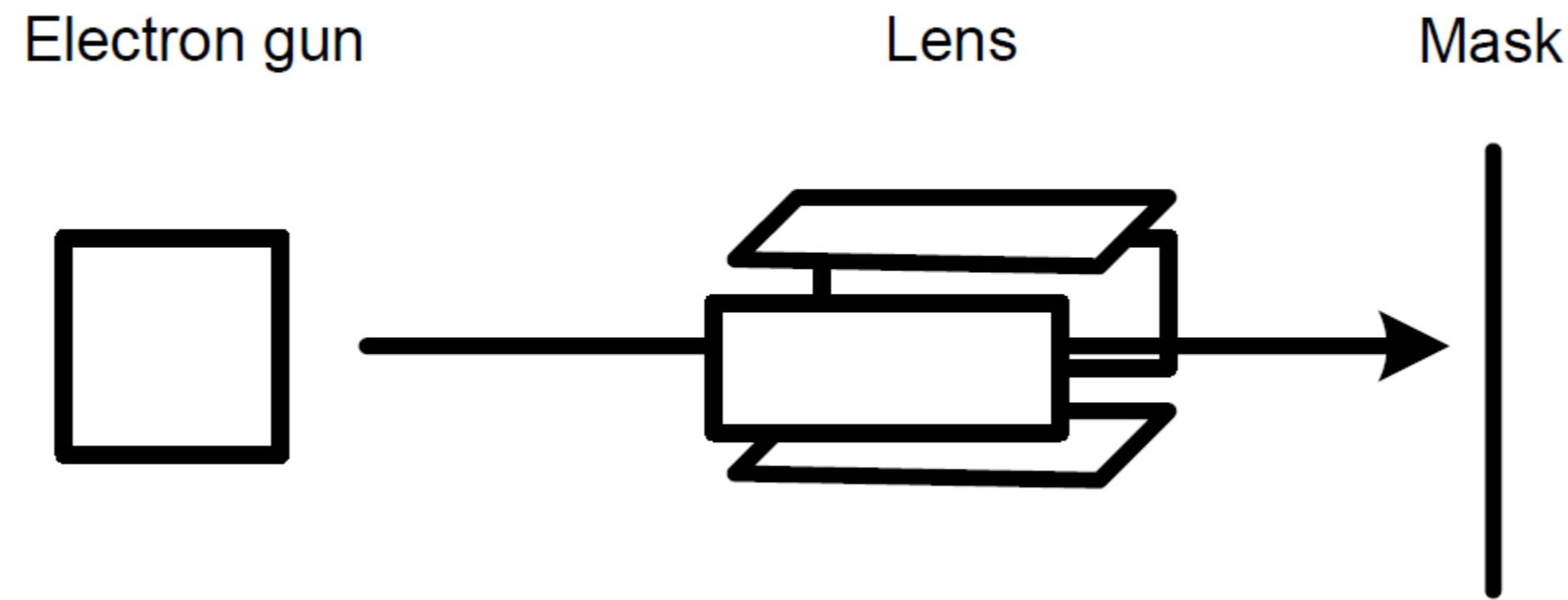
IC foundry: 46,968 (2016)



**ASE GROUP**

Packaging and test: 65,695

# Mask making



- Mask making is extremely expensive
- A normal chip has around 30 - 40 masks.

# Lithography

Today: 193nm argon fluoride excimer laser

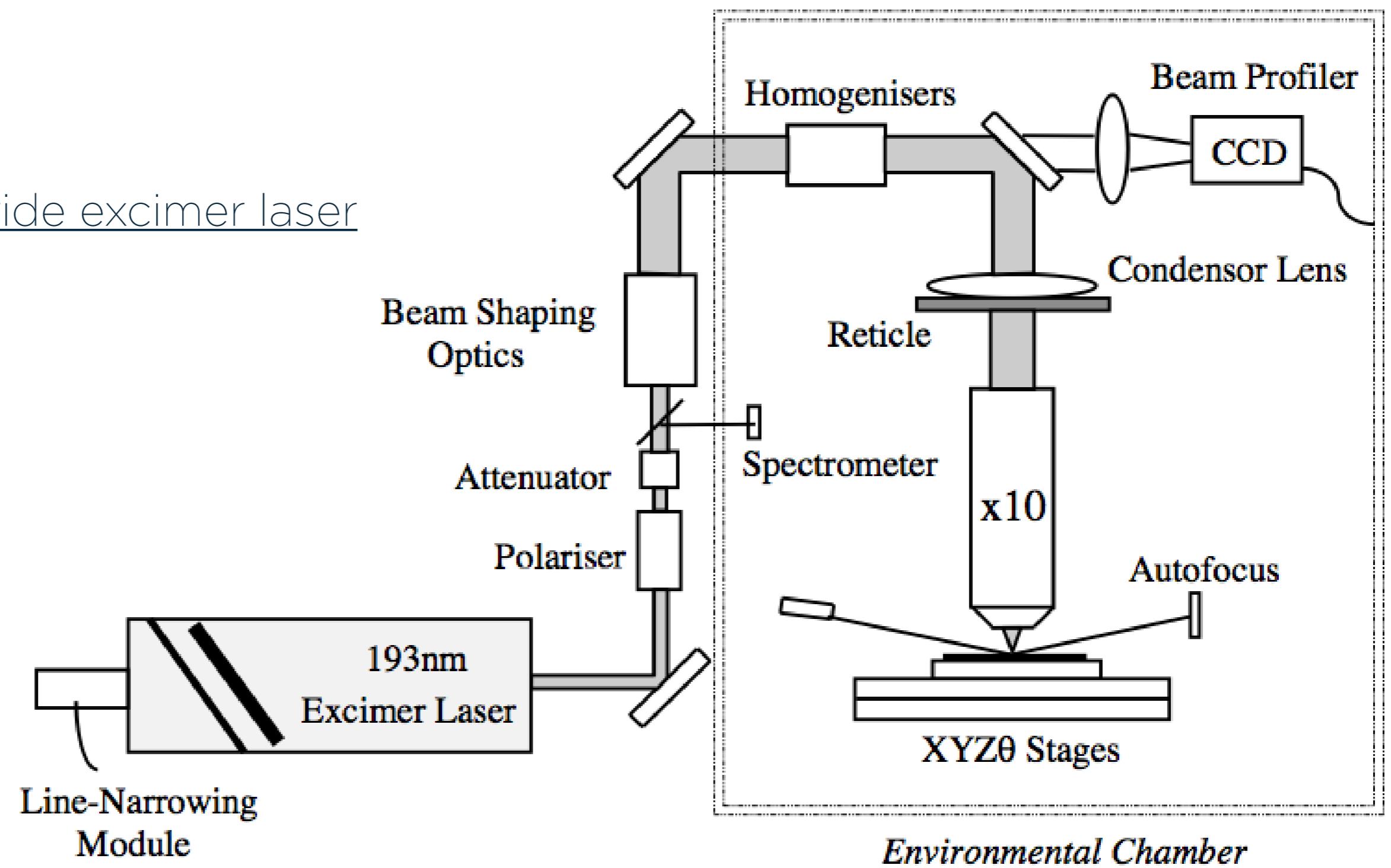
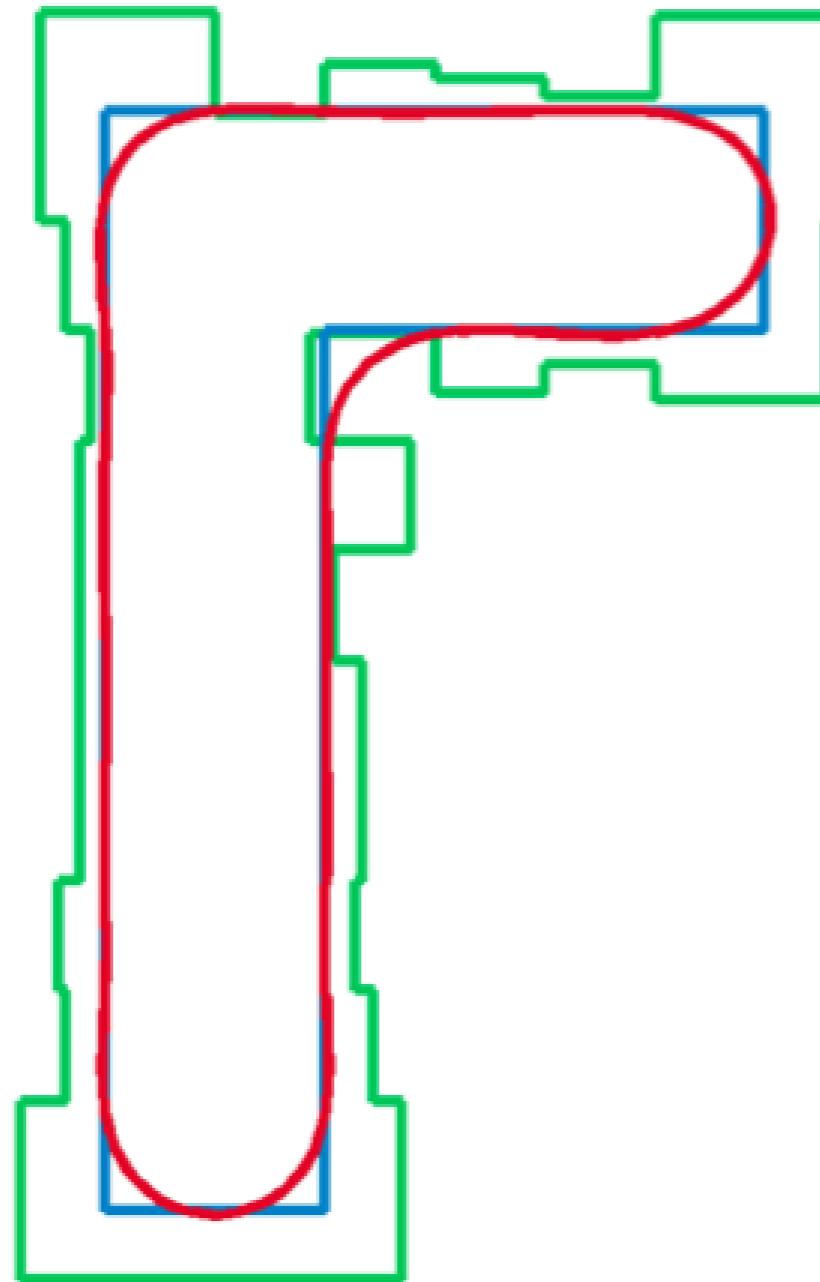


Figure 2. Schematic diagram of 193nm Microstepper

# Optical proximity correction



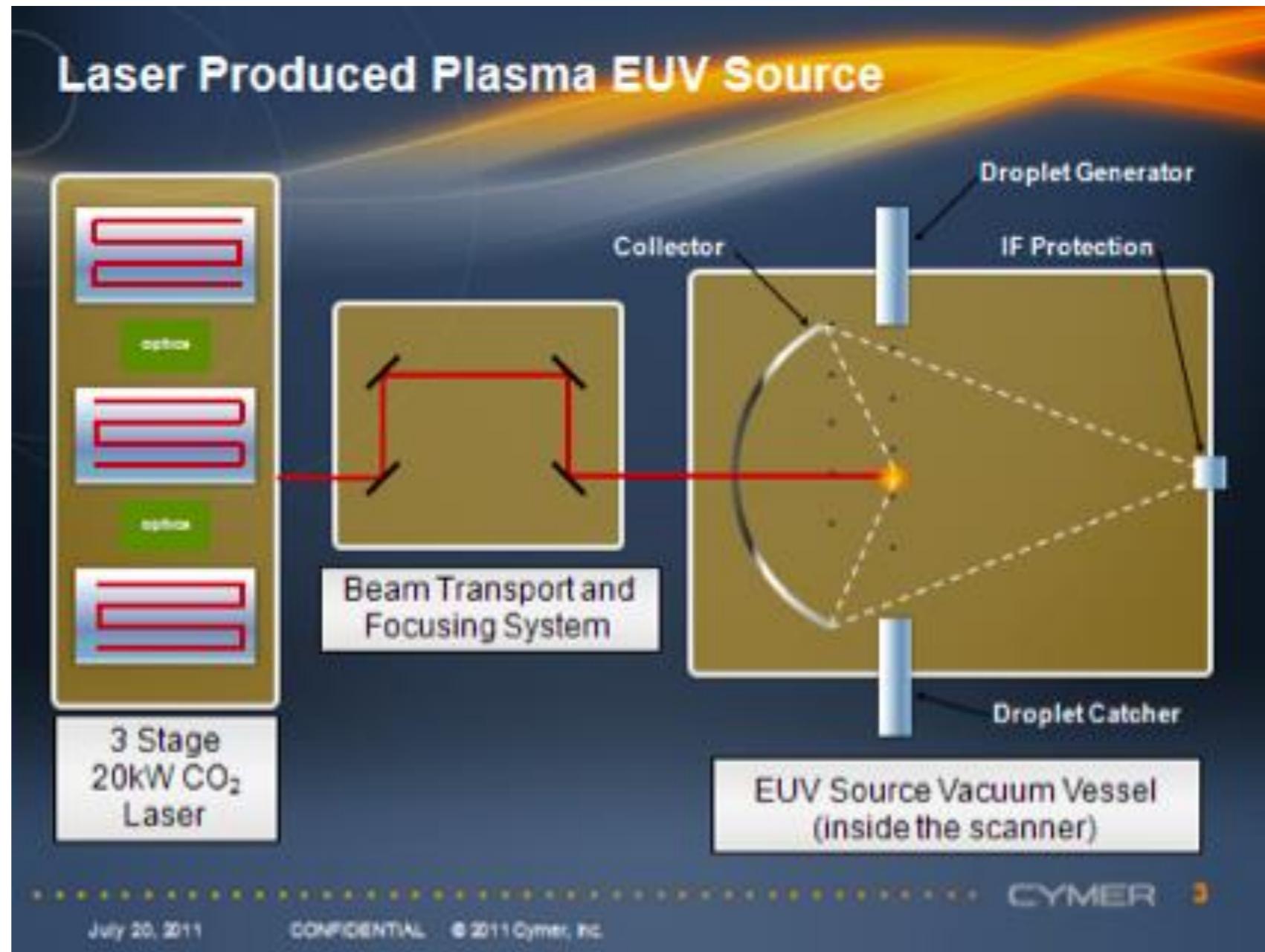
- The wavelength of the developing light is larger than minimum features ( $193\text{nm} > 20\text{nm}$ )
- Diffraction patterns affect the light intensity on the photo-resist
- Extensive calculations need to calculate how the mask should look to compensate for diffraction and processing inaccuracies

Blue = Pattern we draw in our CAD programs

Green = How the mask actually looks

Red = Pattern on chip

## Tomorrow (probably): Extreme ultra violet



[http://www.cymer.com/euv light sources/](http://www.cymer.com/euv_light_sources/)

EUV lithography

What

# Low power wireless product offering

## Low power short-range IoT

Bluetooth, 802.15.4/Thread, Zigbee and 2.4GHz RF SoCs

Advanced multiprotocol solutions

MUSD 228 revenue in 2017

## Low power cellular IoT

Multimode LTE-M / NB-IoT SiPs

Strategic investment since 2015

Sampling first lead customers now

## Connectivity and application

Highly integrated wireless SoCs with on-chip MCU

Wireless protocol stacks and application SDK



Integrated circuits (ICs)



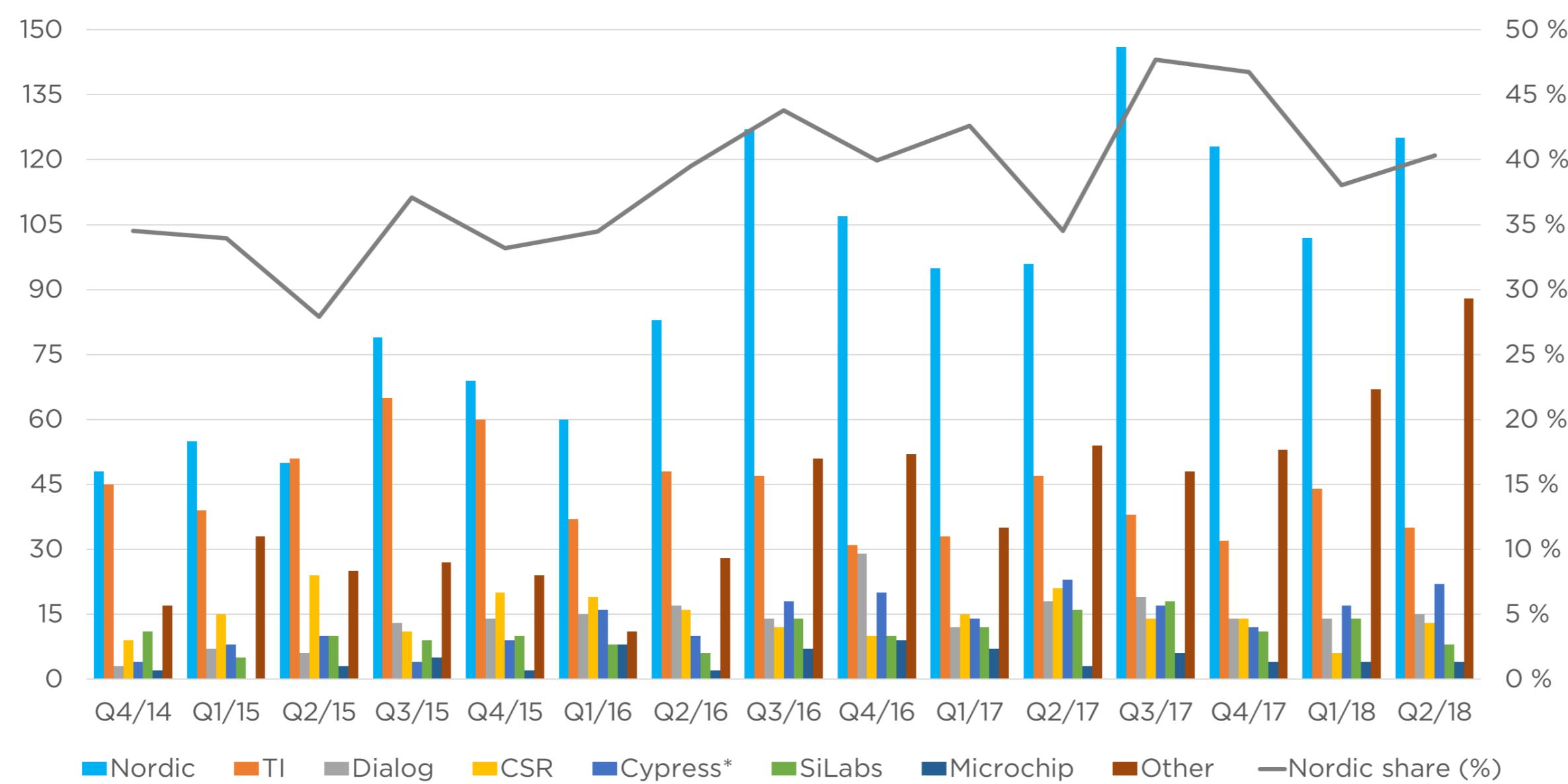
Embedded software



Development tools

# Leading and broad position in Bluetooth

Bluetooth low energy end-product certifications\*

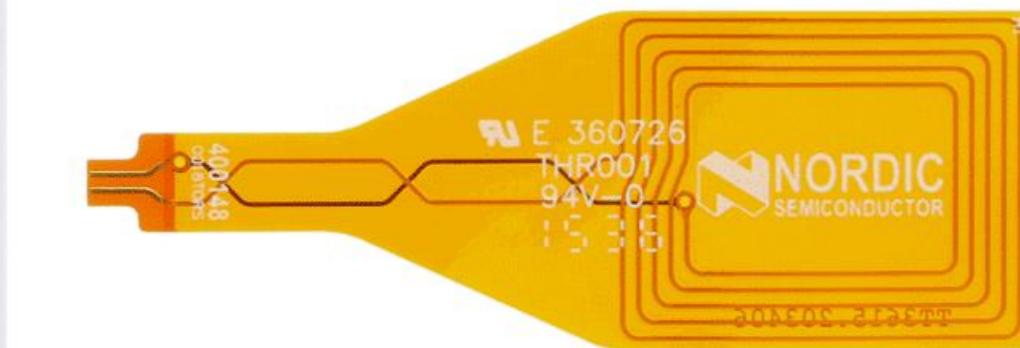
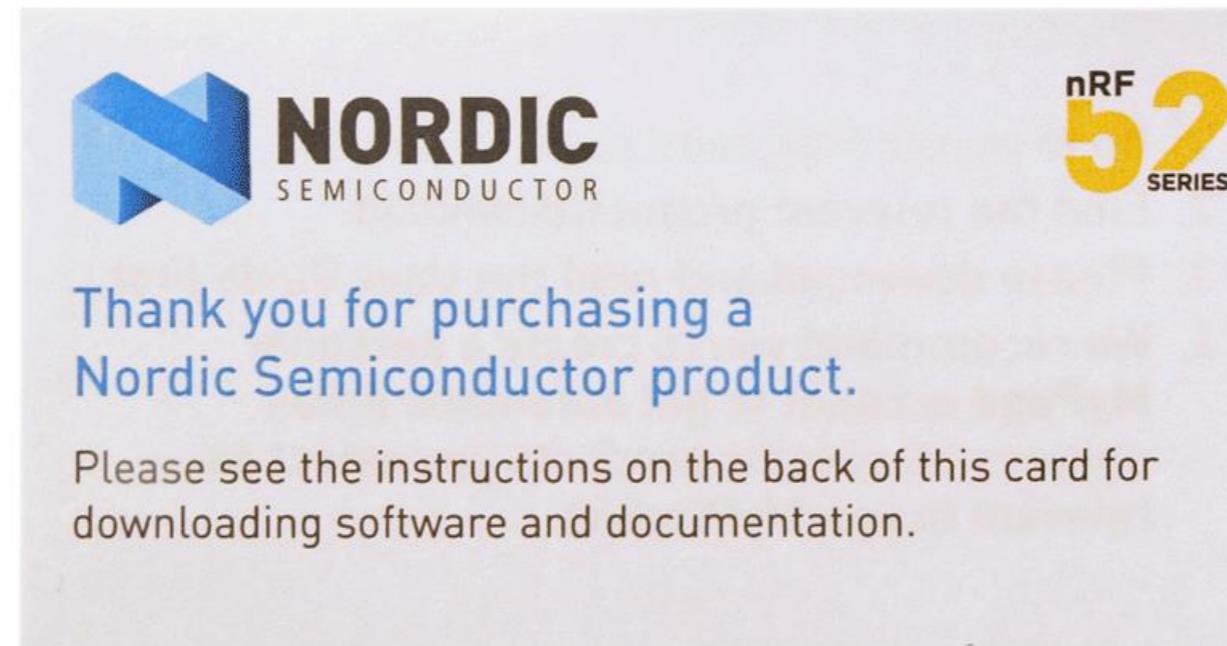
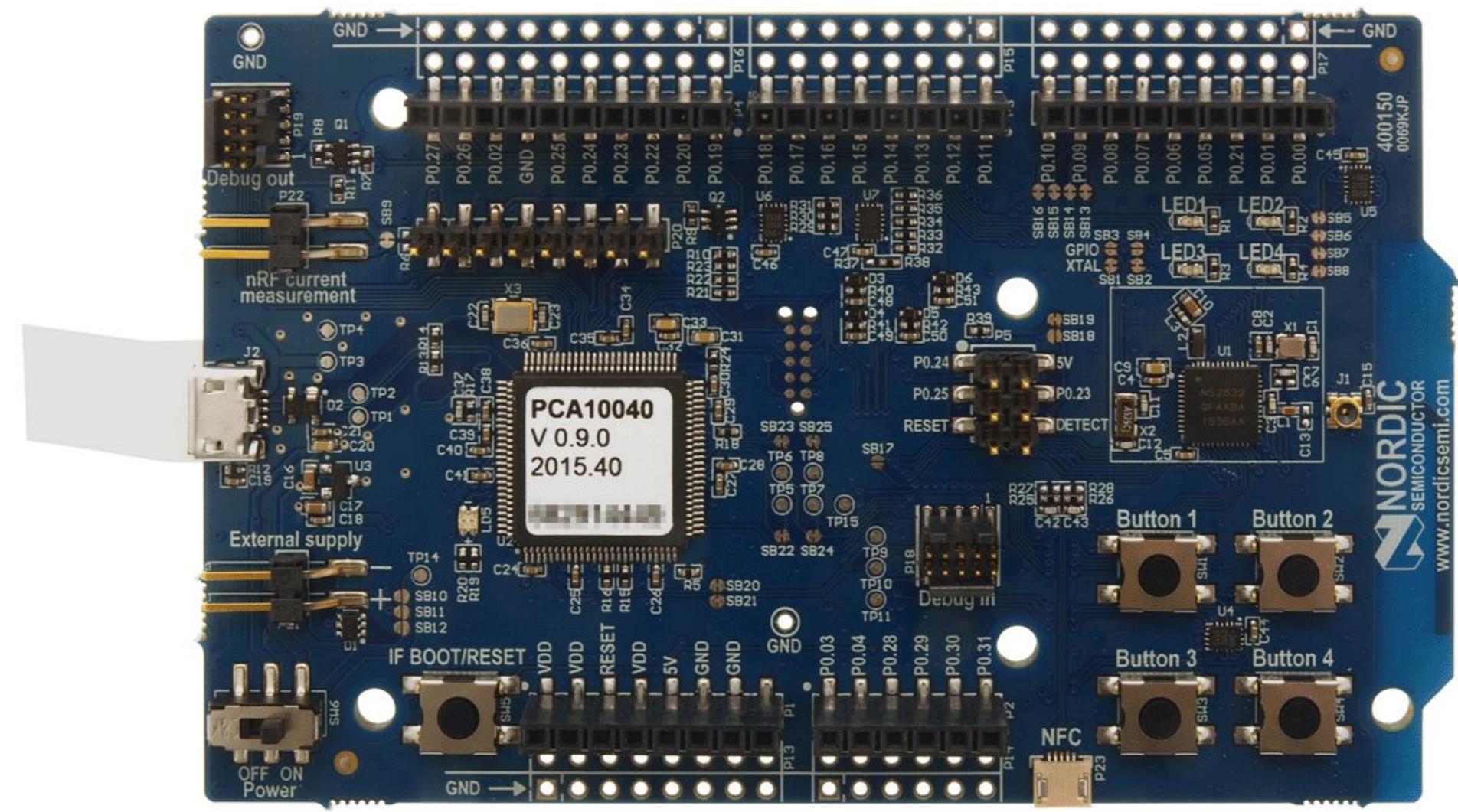


End-product  
certifications,  
Nordic Q2 18

125

+30%  
y-o-y

+23%  
q-o-q





**NORDIC**  
S E M I C O N D U C T O R

Smarter Things

Want to help me make  
a better world?

And have fun at the same time

<http://www.nordicsemi.com>

carsten.wulff@nordicsemi.no