1-Wire Transceiver Project Phase 1

Charles Helmich Ivan Bow Don Owen February 25, 2019

- 1 Description of Design
- 1.1 Functional Description
- 1.2 Logic Sizing
- 2 Waveforms of Sub-designs
- 2.1 Imbalanced Inverters
- 2.2 Pass-Mux
- 2.3 Balanced Inverters and Output Buffer
- 3 Waveforms and Measurements of full Transceiver
- 3.1 Propagation Delay
- 3.2 Rise Time
- 3.3 Fall Time