1-Wire Transceiver Project Phase 1

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Contents

1 Description of Design

1.1 Functional Description

The operation of the one-wire channel with a transceiver on either end will produce 3 possible voltages on the channel: 0, 5, and 2.5 volts. When both transceivers are sending the same value, the voltage on the channel will be that value, either 0 or 5 volts. When the transceivers are are sending opposite values, the value on the channel will be halfway between the two TX values because the external resistors will form a voltage divider. Based on these possible values on the channel it is straightforward to produce a logic table that unambiguously decodes what the received value at a transceiver is.

In order to differentiate between the 3 possible channel voltages we chose to design a pair of imbalanced inverters that have mid-point voltages that are either 1.25 or 3.75 volts, corresponding to halfway between 0 and 2.5 volts and halfway between 2.5 and 5 volts,

Channel	TX (local)	RX (remote tx)
0	0	0
2.5	0	5
2.5	5	0
5	5	5

Table 1: Voltage logic table

respectively. The inverter with a low V_m has a much stronger nFET than pFET and the high V_m is the opposite.

The n-strong inverter will be on when the channel voltage is 2.5 or 5 volts while the p-strong inverter will be on when the channel voltage is 2.5 or 0 volts. The next stage of the receiver uses the local TX signal to control a mux that selects either the n-strong or p-strong output. When the local TX is high, it selects the p-strong output. The p-strong output will be logically 1 when the channel is low (2.5V) and 0 when the channel is high (5V), corresponding logically to $\overline{\text{RX}}$. When the local TX is low, the n-strong output will be logically 1 when the channel is low (0V) and 0 when the channel is high (2.5V), corresponding logically to $\overline{\text{RX}}$.

We note that because we chose to design the mux with a single nFET and pFET the value passes through is degraded and not driven to the full 0-5V range. This does not have a significant impact on the function of the receiver because the later stages both invert and buffer the $\overline{\text{RX}}$ signal, giving it a full 0-5V swing. The final stage in the receiver is an inverter chain that rectifies the $\overline{\text{RX}}$ signal into an RX signal and buffers the output to drive non-trivial load capacitances.

1.2 Logic Sizing

1.2.1 Inverters

With the μ_0, V_{th}, and T_{ox}, parameters taken from provided model library, we calculated the theoretical width ratio of the pFET to the nFET for the for the 3 different V_m values used in our design according to the following formula:

$$\frac{K'_n}{2}\frac{W_n}{L}(V_m - V_{tn})^2 = \frac{K'_p}{2}\frac{W_p}{L}(V_{DD} - V_m - |V_{tp}|)^2$$

Based on that formula, we calculated the width ratios for imbalanced and balanced inverters that gave us the V_m values we needed for our design. These are shown in the table below.

V_m	W_p	W_n
1.25V	1	9.27
2.5V	3.125	1
3.25V	194.5	1

Table 2: Switching voltage ratios (first order approximation)

Because the above calculations only take into account the first-order effects specified in the model library, we also instantiated the inverter designs into a SPICE simulation and experimentally measured the width ratios that gave us the required V_m values. These are shown in the table below. These (or close approximations) are the width ratios that we used in the designs for the project.

V_m	W_p	W_n
1.25V	1	4.126
2.5V	2.258	1
3.25V	44.25	1

Table 3: Switching voltage ratios (simulated)

1.2.2 2-Transistor-Mux

The 2-Transistor Mux (2TMux) looks like a 1X balanced inverter in design, except with the supply of the nFET and pFET wired to the 2 signals to be multiplexed. When driven high, the gate selects the n supply signal to pass through and vice versa when low. This design will never produce a full 0-VDD voltage swing, but does allow us to mux the output of our imbalanced inverters with only 2 transistors and the TX signal, avoiding the cost of inverting the TX and creating a full transmission gate mux. The output of the mux is fed into a balanced inverter with a V_m of 2.5; this inverter will produce an almost rail to rail swing because neither transistor will ever be fully off and further buffering stages will restore the rail-to-rail swing.

1.2.3 Output Buffer

Based on the parallel plate capacitor model we calculated that the gate capacitance for the process was

$$C_{gate} = C_{ox} = \frac{\mathcal{E}_{ox}}{T_{ox}} = \frac{3.9 \times 8.854 \times 10^{-12}}{1.38 \times 10^{-8}} \times \frac{1\,\mathrm{m}^2}{1 \times 10^{12}\,\mu\mathrm{m}^2} = 2.48\,{}^{\mathrm{fF}}/_{\mu\mathrm{m}^2}$$

With a balanced 1X inverter design, the resulting capacitance was then

$$2.48\,{}^{\mathrm{fF}}/_{\mu\mathrm{m}^2} \times L \times (W_n + W_p) = 2.48\,{}^{\mathrm{fF}}/_{\mu\mathrm{m}^2} \times 0.6\,\mu\mathrm{m} \times (3\,\mu\mathrm{m} + 6.75\,\mu\mathrm{m}) = 14.5\,\mathrm{fF}$$

With an assumed output capacitance load of 20 pF the resulting fanout from the $\overline{\mathrm{RX}}$ signal to the load was approximately 1400. The optimal number of optimal-fanout stages is then $\ln(1400) = 7.2$. Because we needed to invert the $\overline{\mathrm{RX}}$ signal, we chose to use an odd and therefore inverting 7-stage output inverter chain with a ratio of 3x fanout per stage (for simplicity of design) to buffer the $\overline{\mathrm{RX}}$ signal to the assumed load capacitance on RX.

2 Waveforms of Sub-designs

2.1 Imbalanced Inverters

2.2 Pass-Mux

2.3 Balanced Inverters and Output Buffer

3 Waveforms and Measurements of full Transceiver

3.1 Propagation Delay

3.2 Rise Time

3.3 Fall Time